Optimization of In-line Semiconductor Measurement Rates: Balancing Cost and Risk in a High Mix, Low Volume Environment

By

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Submitted to the Department of Mechanical Engineering and the Sloan School of Management in Partial Fulfillment of the Requirements for the Degrees of

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Master of Business Administration

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Abstract

Due to a number of market development over the last decade, semiconductor manufacturing companies, including Intel Corporation, have added significant numbers of primarily high growth rate, high-mix, low-volume (HMLV) products to their portfolios. The rapid transition from high-volume manufacturing (HVM) to HMLV manufacturing has caused significant problems. Foremost, the needs of many HMLV customers are different from HVM customers and require different operational tradeoffs. Moreover, many of the HVM focused metrics, tools, systems and processes have proven ill-suited for managing the added complexities and more varied needs of HMLV customers.

This thesis examines many of the problems caused by introducing HMLV products into an HVM wafer fabrication facility (commonly referred to as a fab), and explores potential solutions such as improved cultural and organizational alignment; capacity management and setup elimination; and scheduling and work-in-process management to name a few. Although the discussion focuses on semiconductor operations, the concepts easily generalize to other companies struggling with achieving operational excellence (OpX) in an HMLV environment.

In addition to exploring the macroscopic HMLV issues, we also feature an in-depth analysis of one aspect of achieving OpX in the HMLV environment: the optimization of in-line metrology skip rates. Based on a review of the current methods, a new approach is suggested based on a Bayesian economic skip-lot model we call MOST/2.

In general, MOST/2 suggests that significant cost savings can be realized with only modest increases in the material at risk per excursion if measurement rates are further reduced. Compared with the other methods analyzed, the data indicates that MOST/2 provides superior cost/risk balanced results. For the 27 operations analyzed, results include annual costs savings of over $95,000, cycle time savings of over 5.3 hours per lot, operator savings of over 4.2 people per year and metrology capacity utilization rate reductions of over 65%.

Finally, a brief organizational study was conducted to identify political, cultural and strategic design changes that would bolster long-term operational excellence (OpX) in the HMLV environment. Suggested changes include better identification of customer needs, improved communication and linking between groups, modification and alignment of factory and performance metrics and the creation of a stand-alone HMLV organization.

Thesis Supervisors:	Professor Roy Welsch Statistics and Management Science
	Professor Duane Boning Electrical Engineering and Computer Science
Thesis Reader:	Professor David Hardt Mechanical Engineering

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Likewise, I have benefited immeasurably from the support, guidance and challenging thoughts and ideas of my fellow LFM and MIT Sloan classmates, staff and instructors. Thank you.

I dedicate this thesis to Amy Vallely and to my family and friends. Your encouragement, support and love have not only made my meager contributions possible, but also, more importantly, have made it all worthwhile.

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Chapter 1: Executive Summary and Organization of Thesis

This chapter provides a high-level summary of the thesis. Elements of the semiconductor business environment are discussed within the context of Intel Corporation's[1] strategy to increase the number of products and to decrease the average volume of products in its portfolio. A number of problems created by high-mix, low-volume (HMLV) operations are also discussed to provide context for the hypothesis that achieving operational excellence (OpX) in an HMLV semiconductor environment requires improvements in both the identification and servicing of customer needs as well as better people, processes, tools or systems to manage the increased complexity of HMLV operations.

To support the hypothesis, a case study of one of the major problems of HMLV operations, optimizing in-process metrology inspection rates, is examined and a new customer needs-focused complexity management method and tool are proposed. The results of the new methodology are compared with other options and are shown to provide superior outcomes. The chapter concludes with a description of the organization of the remainder of the thesis.

1.1 Executive Summary

Three major market developments have exerted pressure on Intel's strategy over the last decade: PC market saturation, performance overshoot and the emergence of the internet. Due in part to these changes, Intel has responded by acquiring or developing a significant number of primarily high growth rate, high-mix, low-volume (HMLV) products. For a number of reasons, Ireland Fab Operations (IFO) has been charged with the responsibility for manufacturing more HMLV products than any other factory in the 200/300 mm Wafer Manufacturing Group (WMG) network. The transition from high-volume manufacturing (HVM) to HMLV manufacturing in IFO has been dramatic; in 2003 the factory doubled the number of process technologies and tripled the number of products produced in the fab.

The rapid transition from HVM to HMLV manufacturing has caused significant challenges. Foremost, the needs of many HMLV customers are different from HVM customers and require different operational tradeoffs. Moreover, many of the HVM metrics, tools, systems and processes are ill-suited or incapable of managing the added complexities and more varied needs of HMLV customers. For example, it is no longer possible to review the status of all products or all customers in many of the regularly scheduled weekly meetings; on the tool and system side, several of the work-in-process (WIP) management processes and software packages struggle with how to properly manage the often-times competing interests of different requirements and delivery

[1] Intel Corporation, Intel, Intel386, Intel486, Celeron, Centrino, Pentium, Itanium, Xeon and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

schedules for multiple process technologies and products; and, on the metrics side, focus on high tool utilization rates and minimizing tool set-ups has slowed the cycle times of low-volume products and, in some cases, has threatened delivery schedules.

Due to these problems and others, an HMLV Working Group (WG) was established to investigate major HMLV related performance gaps and to insure that high-risk, high-leverage projects are prioritized, developed and properly staffed to close the gaps. Examples of some of the WG project groups reviewed in this thesis include: HVM/HMLV cultural and organizational alignment; capacity management and setup elimination; and improved scheduling and WIP management.

In addition, a case study of one of the most important projects in the improved scheduling and WIP management group is explored in detail: the optimization of in-line metrology inspection rates. The available methods are analyzed and found to be fundamentally inadequate. Consequently, a customer needs-focused complexity management method is developed and proposed: MOST/2. A comparative analysis of the different methods is conducted for 27 CD-SEM metrology operations. Table 1, below, shows a summary of two of the methods relative to the current, basic method. In all cases, MOST/2 provides superior cost/risk balanced results. Annual cost savings are expected to exceed $100,000 per year with only modest increases in the material at risk (MAR) per excursion.

CD-SEM Operation Totals (relative to current, basic method)	**Method 1 (MOST)**	**Method 2 (MOST/2 Rec)**
Change in MAR (per excursion)	444	317
Annual Tool Hour Savings	5001	5286
Reduction in Metro Capacity Utilization	63%	67%
Annual Labor Hour Savings	7945	8398
Annual Operators Saved	4.0	4.2
Estimated Cycle Time Savings (hours / lot)	5.3	5.3
Annual Cost Savings (Inspection & Excursion Costs)	$67,419	$75,422
Estimated Annual Holding Cost Savings (20% Cost of Capital)	$19,361	$19,682
Total Annual Cost Savings (Inspection, Excursion and Holding Costs)	**$86,780**	**$95,104**

Table 1: Comparative Results Summary of Measurement Optimization Methods

The MOST/2 results provide strong support for the hypothesis that achieving operational excellence in an HMLV environment requires improvements in both the identification and servicing of customer needs as well as better people, processes, tools or systems to manage the increased complexity of HMLV operations. Although not

discussed in detail in this thesis, the customer protection strategy, product and process flexibility, process control system, and forecasting improvement projects provide additional corroborating evidence. And, while significant progress has been made to align the IFO organization and capabilities with the challenges of HVM/HMLV operations, the strategic design, political and cultural environment at IFO needs to be further adapted to the HMLV environment to ensure long-term operational excellence.

1.2 Organization of Thesis

The layout of the thesis is as follows: Chapters 2-4 deal with the problems and challenges of HMLV manufacturing operations at a macroscopic level; Chapters 5-7 provide an in-depth analysis of one of the key high-leverage HMLV activities identified as a solution to some of the macroscopic issues, the optimization of in-line metrology inspection rates; and, Chapter 8 reviews some of the organizational problems caused by HMLV operations and suggests changes to IFOs organizational strategic design, political and cultural environment to successfully adapt to HMLV manufacturing. Finally, Chapter 9 summarizes the thesis and discusses conclusions and opportunities for future work.

In more detail, Chapter 2 provides background information on semiconductor manufacturing, Intel Corporation and some of the reasons that Intel is transitioning from an HVM to an HMLV manufacturing product portfolio. It also highlights IFOs role in the HMLV transition.

Chapter 3 provides an overview of some of the systemic effects of introducing HMLV products into an HVM-optimized factory. Impacts to traditional operational metrics caused by changes in customer needs and the added complexity of HMLV operations are discussed and strategic and tactical response options are examined. Chapter 3 concludes with a brief review of the steps taken at IFO to understand and anticipate the problems and challenges of HMLV operations.

Chapter 4 reviews some of the key activities identified by the IFO team to adapt to and excel at HMLV operations. It also highlights the importance of the improved scheduling and WIP management activity group to set the context for the detailed examination of one of the key related projects: the optimization of in-line metrology inspection rates.

Chapter 5 provides a richer context for why in-line process inspections are employed and when it may make sense to eliminate or to reduce them. Some of the reasons that HMLV products cause significant degradations in manufacturing metrics because of impacts to metrology operations are also discussed. Chapter 5 concludes with a review of the current metrology inspection rate methods and a discussion of how the current methods lead to undesirable results in the HMLV environment.

Chapter 6 provides the details of the MOST/2 in-process metrology inspection rate method and support tool. The relevant economics are discussed and a model sensitivity

analysis is performed to help users develop an intuition for the most important input variables and their impacts on model results.

Chapter 7 provides a comparative analysis of the current and proposed metrology inspection rate optimization methods. Labor and tool hours, annual inspection costs and the expected material at risk values are compared. In all cases, MOST/2 is shown to provide superior cost/risk balanced results for the HMLV environment.

Chapter 8 analyzes the challenges of transitioning from HVM to HMLV manufacturing operations from the organizational behavior strategic design, political and cultural perspectives. Recommendations are provided to better align the IFO organization with the goal of achieving and sustaining long-term operational excellence in the HMLV environment.

Chapter 9 provides a summary of the thesis topics and concludes with a review of the HMLV recommendations and the data supporting our hypothesis that achieving operational excellence in an HMLV semiconductor environment requires improvements in both the identification and servicing of customer needs, as well as better people, processes, tools or systems to manage the increased complexity of HMLV operations.

Chapter 2: Introduction to Intel's HMLV Challenge

This chapter provides background information on Intel Corporation and summarizes recent trends in product mix and product volumes. IFO is highlighted as the lead HMLV 200/300 mm WMG semiconductor wafer fabrication facility and future IFO product mix and volume projections are provided.

2.1 Intel Corporation[2]

Intel Corporation was co-founded by Bob Noyce and Gordon Moore on July 18, 1968. In the 35 plus years since that day, Intel has grown to become the world's largest semiconductor manufacturer. Intel's primary focus continues to be on designing, developing and manufacturing advanced integrated silicon technology solutions for the computing and communication industries. Its stated goal is to be the "preeminent building block supplier to the worldwide internet economy."[3] Intel strives to achieve this ambitious goal by providing chips, boards and other semiconductor components to the computer, server, networking and communications industries. In 2003, Intel served over 2000 direct customers through the coordinated efforts of just under 80,000 worldwide employees.

2.1.1 Intel's Products

Intel offers products at various levels of integration. At the component level, Intel designs and manufactures integrated circuits (commonly called ICs or semiconductors) which process electronic information in various ways. The integrated circuits are built on silicon chips etched with multiple layers of interconnected electronic switches. Well known examples of some of the very complex, highly profitable integrated circuits that Intel manufactures include the Intel386, Intel486, Celeron, Pentium, Itanium and Xeon microprocessors which serve as the "brains" of PCs and Servers.

Other major products include chipsets,[4] boards, wired Ethernet and wireless connectivity products, communication infrastructure products such as network processors

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[2] The industry summary and Intel background information provided in this section is summarized from Intel's 2003 10K filing.

[3] Intel's 2003 corporate mission statement is to "[d]o a great job for our customers, employees and stockholders by being the preeminent building block supplier to the worldwide internet economy." The mission statement is communicated to employees in numerous ways including a company badge insert that includes the workweek calendar, annual mission statement and company values.

[4] Microprocessors are sometime described as the "brains" of a PC. By extension, chipsets can be thought of as the PC's "nervous system." Chipsets send data from the processor to input display and storage devices and perform essential logic functions such as balancing the performance of the system.

and optical components, microcontrollers, flash memory,[5] cellular processors such as the ones used in mobile phones, application processors such as the ones used in handheld computing devices and PDAs, and cellular baseband chipsets.

2.1.2 Intel's Major Customers

Intel's major customers are Original Equipment Manufacturers (OEMs), PC and network communications product users and other manufacturers including a wide range of industrial and communications equipment companies.

Primary OEM customers include computer systems manufacturers Dell Inc. and Hewlett-Packard Company who contributed approximately 19% and 15%, respectively, of Intel's total 2003 sales. Other customers include cellular handset, handheld computing device, telecommunications and network communications equipment OEMs, a wide variety of small and large businesses, as well as individual users.

2.1.3 Intel's Organizational Structure

In 2003, Intel was organized into three groups: the Intel Architecture Group (IAG), the Intel Communications Group (ICG) and the Wireless Communications and Computing Group (WCCG). In late 2003, Intel announced that WCCG would be integrated into ICG in 2004 "to better coordinate product planning and customer focus between our communications infrastructure and wireless client efforts going forward."[6]

The Intel Architecture Group provides microprocessors, chipsets and board-level products for use in the desktop, mobile and server market segments. IAGs organizational structure mirrors the customer segments as the Desktop, Mobile and Enterprise Platform Product groups. In 2003, the IAG operating segment made up approximately 87% of consolidated net revenue. Microprocessor products within IAG accounted for approximately 73% of the total consolidated net revenues for the year.

The Intel Communications Group provides silicon and integrated networking and communication blocks for OEMs. ICG is organized around wired Ethernet products, wireless connectivity products, communication infrastructure products and microcontrollers such as those used in automotive systems. The consolidated 2003 net revenue for ICG was approximately 7% of the total.

The Wireless Communications and Computing Group provides flash memory for products such as mobile phones, PDAs and MP3 players, application processors for handheld computing devices, cellular processors, and cellular baseband chipsets. Net revenue for WCCG in 2003 was approximately 6% of the consolidated total.

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[5] Flash memory is a specialized type of memory component typically used to store program code and user data. The majority of Intel's flash memory is currently used in products such as mobile phones, PDAs and MP3 players.

[6] See Intel's 2003 10K filing if you are interested in additional information.

2.1.4 Intel's Manufacturing and Assembly

In 2003, over 75% of wafer manufacturing at Intel including its microprocessor, chipset, flash memory and networking silicon products was done in the U.S. at fabs in Oregon, Arizona, New Mexico, Massachusetts, California and Colorado. Outside the U.S., almost 25% of Intel's 2003 wafer manufacturing was conducted at facilities in Ireland and Israel including microprocessor, chipset, flash memory and networking silicon products. The Israel fab primarily manufactured chipsets.

In 2003, the majority of Intel's microprocessors and chipsets were manufactured using 130 nanometer (0.13 micron) process technology on 200 mm (8 inch) wafers. Setting the standard for the industry once again, Intel began selling microprocessors in December of 2003 manufactured using 90 nanometer process technology on 300 mm (12 inch) wafers. In addition, by year end Intel had two operational 300 mm fabs in Oregon and New Mexico with a third under construction and expected to come on-line in Ireland in 2004. Intel also announced plans in 2003 to build two additional 300 mm fabs in Oregon and Arizona with production starting after 2004. A summary of Intel's process roadmap showing the wafer size and process technology transitions is included below.

Process Name	T352	T252	T182	T132 T133	T0903	T0653
First Production	1995	1997	1999	2001	2003	2005
Lithography	0.35 um	0.25 um	0.18 um	0.13 um	90 nm	65 nm
Wafer Size (mm)	200	200	200	200 / 300	300	300

Table 2: Intel's Process Technology Roadmap[7]

In 2003, a substantial majority of Intel's component assembly and test operations was done in Malaysia, the Philippines, Costa Rica and China. In the third quarter, Intel announced plans to begin construction of an additional assembly and test facility in Chengdu, China.

2.1.5 Semiconductor Manufacturing

Semiconductor manufacturing is an extremely complex process. Over 300 individual process steps can be required to create the 15 to 30 or so layers required by most modern ICs. To manufacture ICs efficiently, many fabs have hundreds of different tools to meet the particular requirements of different products and process technologies. Because the equipment typically contributes to over half of the product cost, high fab capacity utilization is required for low cost production. As a result, most fabs operate 24 hours a day, seven days a week and 365 days a year.

[7] This chart has been adapted from: Fitzgerald, Mark F. Behind the Cleanroom: Silicon: Does Intel represent a trend? Bank of America Securities Equity Research, United States. Volume 142 (19 Jan. 2004). p. 3. To protect Intel confidentiality, I have assumed this representation to be accurate and true throughout the presentation of the thesis. Neither Intel nor I warrant its validity.

Although different product and process technologies require different tools and capabilities, most semiconductor manufacturing follows a typical cyclical and reentrant process flow. Figure 1 shows an example of a typical basic semiconductor fabrication sequence involves a repeated sequence of steps for most layers.

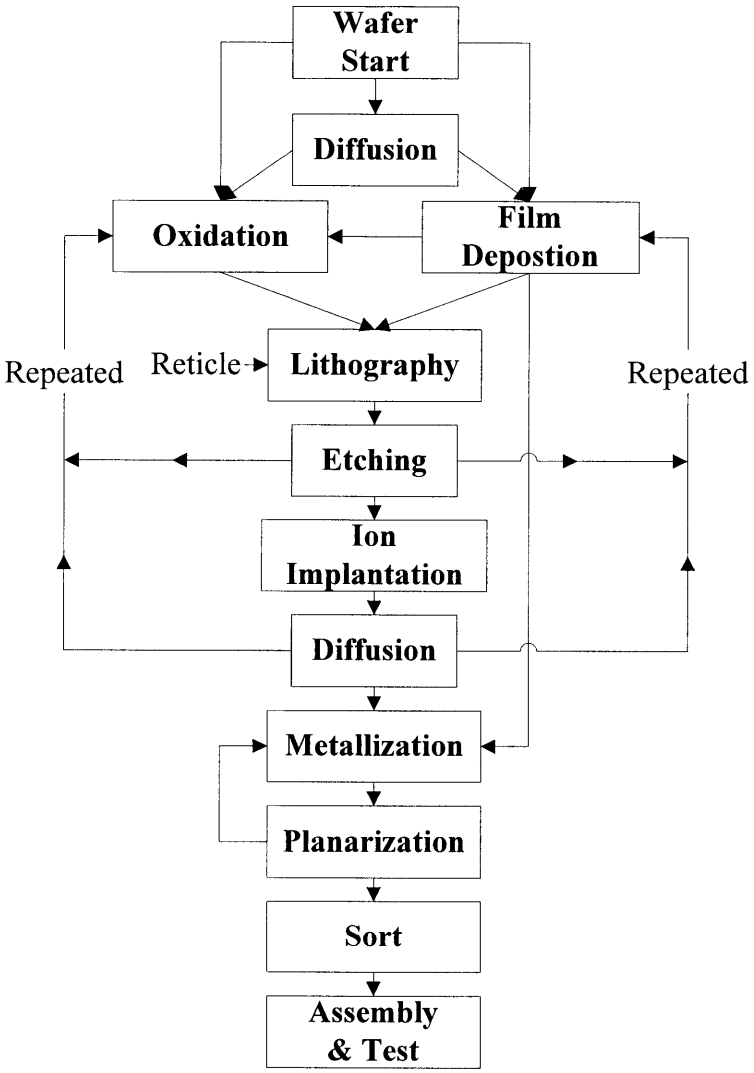

Figure 1: Example of Typical Fabrication Sequence for ICs[8]

The steps are usually grouped into four areas: Front End Processing, Back End Processing, Test, and Packaging. Front End Processing refers to steps in which the semiconductor devices or transistors are created and includes preparation of the wafer surface; patterning and the subsequent implantation of dopants to obtain the desired electrical properties; deposition or growth of a gate dielectric and deposition or growth of insulating materials to isolate neighboring devices. Back End Processing includes the steps necessary to interconnect the various devices to create the desired circuits and includes depositing various metal layers and insulating material to create the desired chip

[8] Serope Kalpakjian and Steven R. Schmid. Manufacturing Engineering and Technology. 4th Edition. Prentice-Hall Inc. Upper Saddle River, New Jersey. (2001). p. 926.

design. Following Back End Processing, the semiconductor devices are subjected to a variety of tests to insure compliance to functional, performance and reliability specifications. Finally, the wafer is cut into individual chips or die which are assembled into ceramic or plastic packages with pins or other connectors to enable their integration with, or attachment to other components or devices.

A typical Front End layer sequence involves several steps. The first is to spin photoresist[9] onto a wafer rotating at several thousand revolutions-per-minute to provide a uniform coating. The photoresist covered wafer is then prebaked to remove the solvent and to harden the photoresist. Next, the photoresist covered wafer is selectively exposed to ultra-violet light through a patterned reticle[10] to break down the organic molecules in the film. Following exposure, the wafer is developed to remove the exposed photoresist. This process is sometimes referred to as spin, expose and develop or SED for short. Prior to etching, the photoresist patterned wafer is typically post-baked to toughen and improve the adhesion of the photoresist to the wafer. Following an ion implantation or thin film deposition step, the photoresist is selectively stripped away or removed by exposure to oxygen plasma. This sequence is typically repeated for each layer to create the semiconductor devices and interconnects.

Although the physics behind each process is generally well understood, the vast number of transistors in modern ICs and the molecular scope of the operations make process control difficult. Interdependence and interaction effects between process steps, tools and products (for example, many processes are highly sensitive to product cross-contamination) further complicates high-yield, high-volume manufacturing.

2.1.6 Intel's Copy Exactly! Methodology

To manage the complexity of frequent rapid product ramps and to insure high yields and process stability are achieved and maintained throughout the Intel manufacturing network (commonly referred to as the Virtual Factory Network or VF), Intel adopted the Copy Exactly! methodology or CE! for short.[11]

Briefly described, CE! consists of structured process transfer and statistical matching methods, the use of best-known-methods (BKMs) throughout the VF, change management through control boards and a commitment to lockstep continuous improvement once full replication is achieved. In practice, CE! involves enormous cross-VF efforts to insure the matching of product yields and reliability metrics, manufacturing module operating characteristics and parametric data, as well as the physical process inputs such as: facilities, chemical and gas consumables, tool recipes and cleanliness, and the cleanroom environment.

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[9] Photoresist is a photosensitive organic liquid.

[10] A reticle or mask as it is also called is a patterned plate which contains the design required to create the layout desired for each lithography layer.

[11] For more information about Intel's Copy Exactly! methodology, see, for example, Mylnarczyk, Michele M. Achieving Synergy in Multi-site Microprocessor Manufacturing: An Analysis of a Copy Exactly Approach. LFM MIT Thesis. (June 1995).

Although CE! requires significant effort and commitment, the results have been impressive. Through CE!, Intel has achieved faster product and process ramps and higher product yields and reliability throughout the VF.

2.2 Intel Ireland Limited's Ireland Fab Operations

As summarized in Table 3, Intel Ireland Limited began operations in 1990. Semiconductor manufacturing started in Ireland a few years later with the addition of fab 10 in 1993; with the completion of fab 14, IFO took its current form as a high-volume manufacturing facility with approximately 156 thousand square feet of cleanroom. The cumulative price tag including various process upgrades was approximately $3.2 billion. In 2003, IFO supported both logic and flash memory products for the 0.35-0.13 micron product families for IAG, ICG and WCCG. As can be seen in Figure 2, Ireland's first 300 mm facility, Fab 24, is nearing completion and is expected to come on-line in 2004.

FAB Facility	First Year	Approx. Square Feet	People (including approx. 1000 contractors)	Approx. Cumulative Investment
IFO (FABs 10 & 14)	1993	156k	2200	$3.2B
F24	2004	160k	2000	$2.2B
Intel Ireland Total	**1990**	**316k**	**4200**	**$5.6B**

Table 3: Comparison of Intel Ireland Limited's Fabs

2.3 Intel's Changing Strategy: New Products, New Markets and HMLV Manufacturing

Historically Intel's strategy has been to deliver higher performing microprocessor products and their supporting chipsets to market first and to quickly ramp to high manufacturing volume. As a result, ramp rate, MHz and yield have been primary internal performance metrics. However, over the last 10 to 15 years, three major market developments have put pressure on Intel's strategy: PC market saturation, "performance overshoot"[12] and the emergence of the internet.

2.3.1 Market Saturation in the PC Segment

As a survey conducted by IBD/TIPP[13] in the second half of 2003 discovered, 79% of U.S. households have at least one PC. Moreover, "the percentage of non-PC

[12] The "performance overshoot" concept is from: Verlinden, Matthew C., Steven M. King and Clayton M. Christenson. Seeing beyond Moore's Law: Trends and Forecasts for the Semiconductor Industry. Semiconductor International. (July 2002). pp. 25-33 and 50-56. Additional discussion can be found in: Christenson, Clayton M. The Innovator's Dilemma: When Technologies Cause Great Firms to Fail. Harvard Business School Press. Boston, MA. (1997).

[13] TIPP is a unit of TechnoMetrica Market Intelligence. IBD was their polling partner.

Figure 2: Intel Ireland Limited's IFO and Fab 24

households is likely to remain fairly constant for the foreseeable future," says Raghavan Mayur, President of TIPP. He goes on to say, "It's more likely that current PC households will buy more PCs than households without a computer buying one... Many non-PC households don't feel they have the money to spend on a computer."[14] In other words, PC market penetration in the U.S. is reaching saturation levels. In addition, while trends in other developed nations appear to lag the U.S., they are not far behind. Market saturation helps explain the relatively low personal computer growth rates projected in Table 4. Intel's response, which is discussed in greater detail shortly, has been to seek out new growth markets.

2.3.2 Performance Overshoot

An additional challenge to Intel's historic strategy is explained by the performance overshoot phenomenon.[15] Briefly summarized, as the increasing performance of microprocessors has outstripped the needs of most mainstream users, the value that Intel has been able to capture with higher performing products has diminished. In other words, although customers continue to expect Moore's Law type advances in performance and price, they are no longer as willing to pay for the performance. Intel's launch of the more modular lower-performance Celeron processor in 1998, its first processor for the PC Value market segment, was a strategic response to the performance overshoot problem.

2.3.3 The Emergence of the Internet

The mainstream emergence of the internet in the 1990's put additional strains on Intel's historic strategy. With the emergence and development of the world-wide-web, in particular, many customers became more interested in the speed of their internet connections than in the speed of their PCs. In contrast to market saturation which limits market growth and performance overshoot which limits Intel's ability to capture wallet share, the emergence of the internet and world-wide-web created a shift in the source of customer value creation.

2.3.4 Intel's Changing Strategy

An interview released by Inforworld on February 11, 2000 with Intel CEO Craig Barrett captures a number of these problems and summarizes how Intel is adapting its strategy to meet the new product and market challenges.

> **InfoWorld:** In your mind, what ties these [IAG, ICG and WCCG] business segments together?
> **Barrett:** We've recognized very simply that the last decade was pretty much the decade of the personal computer. It was the driving force of computing and the

[14] Seitz, Patrick. 1/9/04: One-fifth of U.S. Households Lack PCs. http://www.glogontheweb.com/erin/articles/1008.aspx (29 Feb., 2004).
[15] Verlinden, Matthew C., Steven M. King and Clayton M. Christenson. Seeing beyond Moore's Law: Trends and forecasts for the semiconductor industry. Semiconductor International. (July 2002). pp. 25-33 and 50-56.

driving force for what we did. This is shaping up to be the decade of the Internet. Whatever it is, the Internet seems to be at the center of the action. Our goal is to be at the center of the action.

InfoWorld: Does that mean the PC era is over?
Barrett: My favorite phrase is the post-PC era. The world's probably going to sell 18 or 20 percent more PCs this year than they sold last year. Last year they sold 18 percent more than the year before. Now we sell more PCs than television sets. But somehow, it's now the post-PC era. Our core business is still a very important part of the world, and we want to be successful at that. But we also want to move with the center of gravity.

InfoWorld: How will new Internet segments manifest themselves?
Barrett: There are a number of pre-eminent building blocks that come in various forms. A great deal of our expertise happens to be building blocks in terms of integrated circuits – I mean, they're processors in PCs, they're processors in handheld devices, and network processors in the networking and communication infrastructure. We're going to adopt the same [strategic] model that we had in the PC space which is [to] provide the building blocks to a bunch of OEMs. If there's a void or vacancy there, we may go in and try to build an end product in that space, just to move the technology forward. But by and large, we don't want to go out and compete with our customers in a space that they have established as their region of operation.

As suggested by Barrett, Intel has expanded its strategy with investments in higher growth product and market segments. In particular, as reported in an October 15, 2001 Business Week article, "Barrett has pumped more than $10 billion into 34 acquisitions to bolster efforts in new markets, betting that those deals would help such units as the Communications Group and the Wireless Communications and Computing Group grow 50% annually."[16]

Table 4 offers some growth rate comparisons in different technology market segments to help put Intel's strategy in perspective. Although some of the communication and wireless technology segments are small by comparison to PCs or servers, their growth rate projections are phenomenal.

[16] Edwards, Cliff. Intel. Business Week. The McGraw-Hill Companies. (15 Oct. 2001). pp. 80-90.

Market Segments	2004 Market Size Projections in $billions	Annual Growth Rate Estimates
Servers	51	4%
PCs	185	6%
WLAN Chipsets	0.38 - 0.58	8 - 15%
NOR-type Flash	16.0 - 16.2	35 - 39%
Network Processors	1.8	66%
Communications Processors	0.087	248%
10GB Ethernets	0.185	255%

Table 4: Annual Growth Rate Forecasts and 2004 Market Projections by Technology Segment[17]

One of the direct consequences of Intel's strategic shift into new products and markets and the high number of acquisitions has been the creation of a very diverse product line. Initially, most of the manufacturing production of the acquired products and technologies remained with external subcontractors. However, in recent years, particularly since the most recent semiconductor downturn created excess manufacturing capacity, Intel has brought the manufacturing of a significant number of these products into the VF. While this may simply reflect Intel's desire to maintain high fab capacity utilization in a down economy, it likely also reflects Intel's desire to build its HMLV manufacturing capabilities.

Figure 3 provides a time series snapshot of Intel's HMLV transition. Each data point represents either an actual or planned operating point for the quarter and year identified by the data label. The vertical location of each data point indicates the average wafer-starts-per-week (wspw) per product and the horizontal location indicates the number of unique products expected in the 200/300 mm Virtual Factory for the quarter identified. Thus, a data point in the upper left-hand corner represents a high-volume, low-mix manufacturing quarter and a data point in the lower right-hand corner represents a quarter in which HMLV production occurred or is planned. As the data series indicate, Intel expects the 200/300 mm VF to be running nearly 50% more products by the second quarter of 2005 than it did in the third quarter of 2003. Moreover, the average weekly volume of wafer starts by product will be roughly 30% lower.

Another consequence of Intel's strategic shift into new products and markets is the need to recognize that many of its new customers have different requirements and interests than in the past. In particular, for many of the customers attracted by the HMLV products Intel has added to its portfolio, cost, time-to-market and responsiveness are now more important than ramp rate, MHz and yield. Intel's need to recognize and adapt its organization, metrics and culture to serve the more varied needs of both HVM and HMLV product customers is a theme we will return to in greater detail in later chapters.

[17] This data was aggregated from analyst, trade journal and company data compiled by InfoTech Trends. References for the various sources can be found in the bibliography.

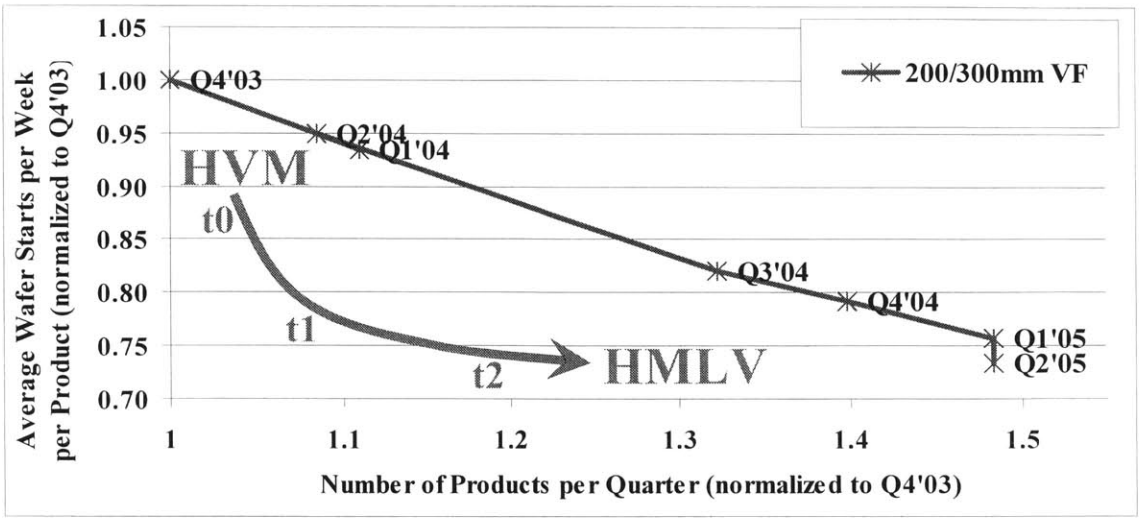

Figure 3: Intel's Transition from HVM into the HMLV Environment

2.4 Multi-Technology, High-Mix, Low-Volume Manufacturing at IFO

The product mix and volume trends at IFO mirror the rest of the VF but are generally accelerated. That is, IFO is the lead 200/300 mm WMG fab in the VF and is already operating in an HMLV environment.[18] Moreover, in 2003 IFO concurrently ran four different process technologies: T352, T252, T182 and T132. In addition, the 200 mm IFO fab manufactured both logic and flash memory products for IAG, ICG and WCCG. Although not captured in the HMLV transition figure below, concurrently running multiple technologies and serving multiple customers significantly complicates achieving operational excellence (OpX) in the MT-HMLV[19] environment. Some of the challenges are discussed in greater detail in the following chapters.

Figure 4 is interpreted in the same way as Figure 3. As can be clearly seen, the fabs selected for this graph are all transitioning from HVM to HMLV manufacturing to support Intel's product and market strategies. If we had included data from previous quarters, IFOs transition would be more pronounced but the end result is clear; IFO appears to have largely completed the transition to the HMLV environment. Average weekly product volumes have stabilized for the near term and only modest increases in

[18] To protect company confidentiality, we have avoided absolute references to Intel product mix and volumes. To a large degree, however, we believe that an absolute definition of what constitutes a high or low product mix, or high or low volumes is less important than a relative definition for several reasons. The first is that any definition would need to be adapted to the characteristics of the industry. The second is that the challenges and problems of operating in an HMLV environment, even within the same industry, largely depend on the particular tools, processes, metrics and other characteristics of a given facility.

[19] To emphasize the multiple customer or multiple technology complications of HMLV manufacturing we sometimes add the MT prefix to HMLV. But, for simplicity reasons, we generally refer to the topic using the simpler HMLV tag.

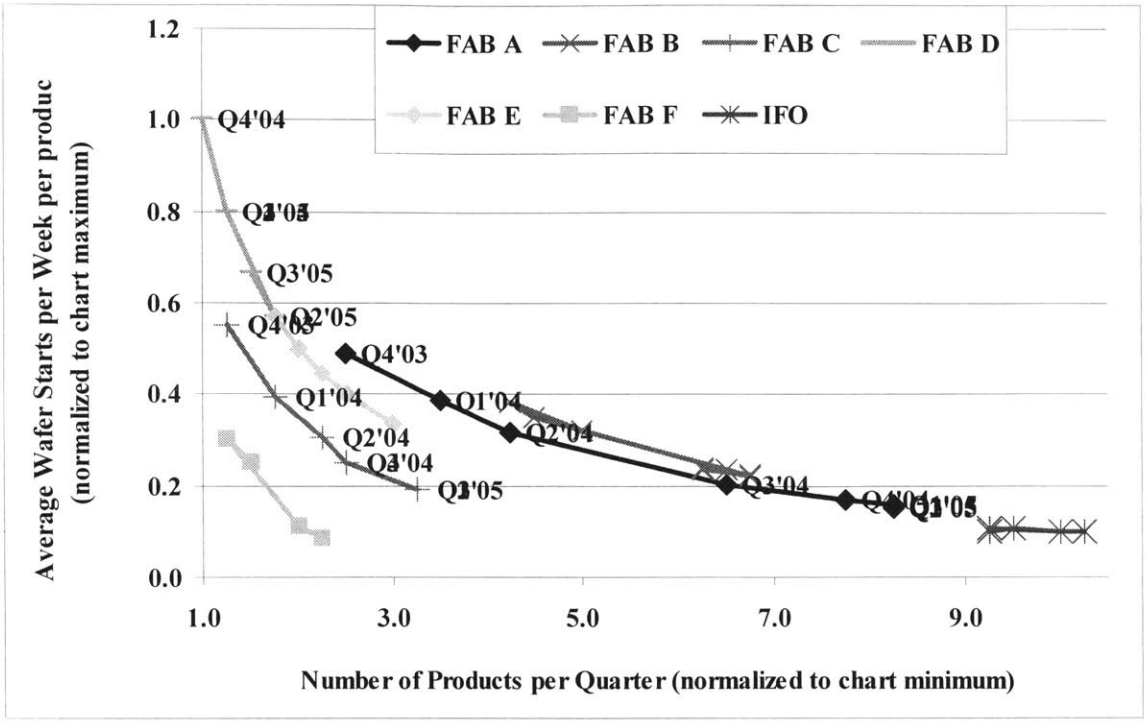

Figure 4: The VFs Transition from HVM into the HMLV Environment

the product mix are expected through the third quarter of 2005. The other fabs are trending toward IFOs current HMLV operating point and will need to embrace the changes we describe in the coming chapters to facilitate the transition.

In summary, a number of changes in the semiconductor business environment have prompted Intel to shift its strategy toward a more varied product portfolio of generally higher growth but lower volume products. The trend away from HVM and into the HMLV manufacturing environment continues for the foreseeable future and requires Intel to recognize and adapt its organization, metrics and culture to serve the more varied needs of both HVM and HMLV product customers. The problems are particularly pronounced for IFO which leads the 200/300 mm WMG VF in the HMLV transition. In the next chapter we explore the challenges and problems of HMLV manufacturing in greater detail.

Chapter 3: Challenges and Problems with HMLV Manufacturing

This chapter provides an overview of some of the challenges and problems of HMLV semiconductor manufacturing. The high-level systemic effects of HMLV operations and the different needs of IFOs HMLV customers are discussed. Impacts to traditional operating metrics due to both changing customer needs and the increased complexity are identified. Strategic and tactical response options are also examined. The chapter concludes with a brief history of IFOs response to the HMLV challenges and a description of the guiding principles that were used to select and respond to some of the current problems, and to anticipate future ones.

3.1 Changing Customer Needs

The change in Intel's strategy and the resulting HMLV product portfolio requires a new, more tailored focus to the varied needs of each customer. Intel must match its metrics and operational focus to each customer's expectations. Three examples help elucidate the challenge.

For a typical high-volume logic product like a microprocessor, key customer expectations include consistent high performance and reliability and quick ramps to high volume capacity. To achieve these metrics, the operational focus must be on quick product ramp and qualification, CE! throughout the VF, and rapid yield learning and constraint management for a relatively small number of processes, for a relatively short product life cycle of 12-18 months.

For a commodity product such as a LAN controller, however, customer expectations are on low cost, speed of delivery and service. For these customers, the operational focus needs to shift to order fulfillment, low cost and sufficient capacity to meet attach rates for a product life cycle closer to five years.

For specialty ICs such as optical silicon products, customer expectations include the rapid delivery of samples, low cost, an appropriate match of process technology and performance to the market segment, and long life support. The operational focus for these products needs to be on build-to-order, reduced time-to-market, low cost and the flexibility to manufacture many products with significant order variability, on a wide range of process technologies with product life cycles that may be five years or longer.

Although the challenge of meeting HMLV customer needs is often summarized by some of the HMLV Intel team members as "cost, time-to-market and responsiveness are now more important than yield, ramp rate and MHz," the reality is that Intel must match its metrics and operational focus to the varied needs of each of its different customers.

3.2 Systemic Effects of Introducing HMLV Products into an HVM Fab

The introduction of HMLV products into an HVM fab increases operational complexity in many ways. The introduction of HMLV products increases the number of customers, the number of metrics required to satisfy customer needs, the number of new product introductions (NPIs) and the number of setups. All of these effects increase the amount of system-wide variation. In general, there are only a few ways to accommodate the added variation while maintaining system performance: increasing inventory levels, increasing the available capacity or increasing the cycle time.[20] Alternatively, the negative systemic effects can be mitigated by increases in the efficiency and productivity of the manufacturing and support processes and personnel.

In general, HMLV manufacturing is more costly, requires longer cycle times and causes a decrease in customer service. Cost increases come from more setups, more masks, more package types, more product qualifications, more inventory and more direct and indirect headcount. Cycle time increases come from more setup and conversion downtime, more NPIs, more priority request lots and the increased complexities of HMLV WIP management. Decreases in customer service come from higher excursion sensitivity and lower forecast accuracy, to name just a few.

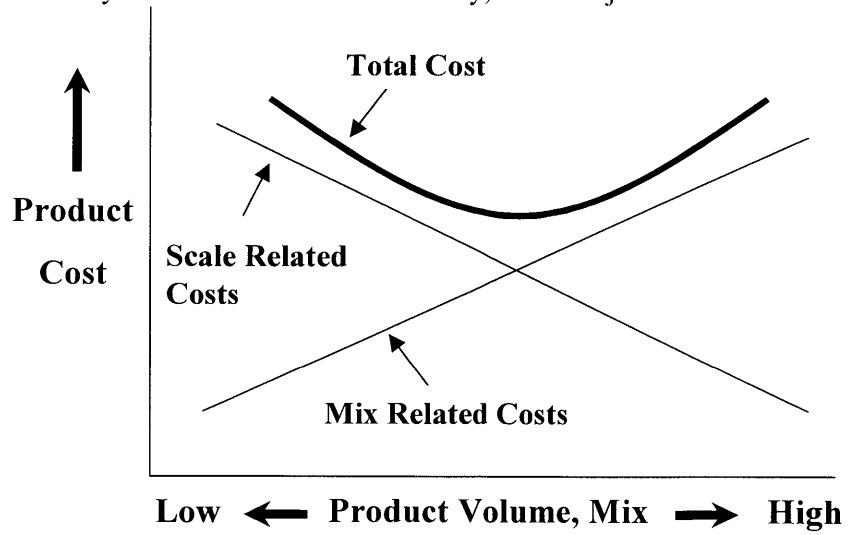

Figure 5: The Relationship between Product Costs, Volumes and Mix[21]

Some of these dynamics are discussed in greater detail in R. Mahoney's text on High-Mix, Low-Volume Manufacturing.[22] Figure 5, above, is adapted from the text and

[20] For a more detailed discussion of variability buffering, see: Hopp, Walace J. and Mark L. Spearman. Factory Physics. 2nd Edition. The McGraw-Hill Book Company. Boston, MA. (2001).
[21] Ibid. Figure 1.4.1 p. 6.
[22] R. Michael Mahoney. High-Mix, Low-Volume Manufacturing. Prentice Hall PTR. Upper Saddle River, New Jersey. (1997).

demonstrates how product costs change with mix and volume. Since Intel fabs are generally optimized for high-volume production, increases in mix and decreases in volume tend to increase product costs.

3.3 HMLV Impacts to Traditional Operating Metrics

As noted by a number of Intel's HMLV team members, the introduction of HMLV products causes conflicts in factory indicators. "[The] current factory measurement system [is] not aligned to HMLV needs...[significant] time [is] spent resolving conflicts...[it is] not obvious that [HVM and HMLV] can co-exist in the same factory."[23]

For logic products, there are relatively few new product introductions each year and the development cycle times are fairly predictable. In contrast, HMLV product manufacturing must accommodate many new products which typically have faster and less predictable development cycles. For logic products, large batch sizes and optimized die yields and die performance are required. But, for HMLV customers smaller batch sizes are required, yields are less important and the products typically only need to meet basic functional requirements. While logic products require high-volume output and a focus on constraints to ensure high equipment utilization, for HMLV products the output focus needs to be on order fulfillment and the equipment utilization focus needs to shift from high capacity utilization to high equipment flexibility.[24]

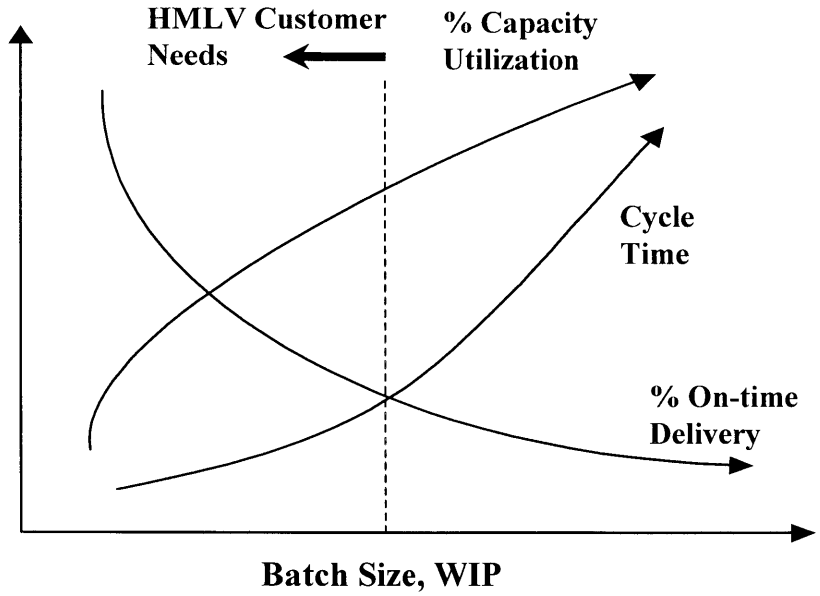

Figure 6: Effect of HMLV Customer Needs on Capacity Utilization, Cycle Time and On-time Delivery[25]

[23] Intel HMLV Business Strategy Team. Business Environment: High Mix / Low Volume. Revision 5.5 ww4302. p. 6.
[24] Ibid. p. 6.
[25] Adapted from Mahoney, Figure 2.7.1, p. 69.

Figure 6, adapted from R. Mahoney's text on High-Mix, Low-Volume Manufacturing, confirms the observations of the HMLV Strategy team. HMLV customer needs push for smaller batch sizes at the expense of equipment capacity utilization. Additional similar tradeoffs are discussed in greater detail in the chapters on metrology measurement rate optimization.

3.4 HMLV Strategic and Tactical Response Options

There are a wide range of strategic and tactical response options to the challenges and problems created by introducing HMLV products into an HVM fab. The most important, and one of the most difficult, is to create cultural and organizational alignment with the more varied HVM and HMLV customer needs. To create this alignment, senior staff involvement is necessary to either adapt the current metric and incentive systems or to devise new ones. In addition, since the tradeoffs between the options are often complex and dynamic, it is helpful if senior management establishes and empowers a cross-functional team to analyze the options and to implement the most advantageous solutions on an ongoing basis.

Other strategic options include allocating HMLV products to different or multiple fabs; developing and using multi-product wafers (MPW), multi-products lots or multi-product shuttles (MPL or MPS); creating HMLV-focused fabs or mini-fabs; reorganizing fabs from job shop style operations to work-cell based operations; changing the push-pull manufacturing boundary; reducing or streamlining NPIs; and reducing batch and or lot sizes. A number of these strategies have been explored by Intel, Intel competitors or have been analyzed in greater detail in the literature.[26]

Tactical options include design-for-HMLV development and manufacturing and delayed product differentiation, as well as improvements in scheduling and WIP management, capacity management and set-up elimination, process flexibility and tool conversions, customer protection and inventory placement strategies, and product and process control and health monitoring systems. Many of these tactical improvement options are discussed in greater detail in the next chapter.

3.5 IFOs Response to the Challenges of HMLV

In the second half of 2002, IFO senior leadership began to proactively engage the management staff in discussions about the impacts and challenges of HMLV manufacturing. Shortly thereafter, a Management Review Committee (MRC) was created with high-level cross-functional representation from the Planning; Sort; Manufacturing, Yield, Quality and Reliability; Engineering; and Manufacturing Engineering groups.

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[26] See, for example: Veeravagu, Asoka. The Development of an Optimal Manufacturing Strategy for Low-Volume Specialty Vehicles. LFM MIT Thesis. (June 2001)., Killian, Vida A. Impact of High-Mix, Low-Volume Products in Semiconductor Manufacturing. LFM MIT Thesis. (June 2003)., Sholtz III, Robert L. Strategies for Manufacturing Low-Volume Semiconductor Products in a High-Volume Manufacturing Environment. LFM MIT Thesis. (June 2002). or, Christenson, Verlinden and King, pp. 25-33 and 50-56.

Through the leadership of the MRC, IFO management developed a common understanding of the challenges of HMLV manufacturing and identified and aligned on a number of key response tactics. Figure 7 is an excerpt from the IFO 1st half of 2003 priorities list showing just one of the methods the HMLV MRC used to communicate the HMLV vision with the rest of the organization.

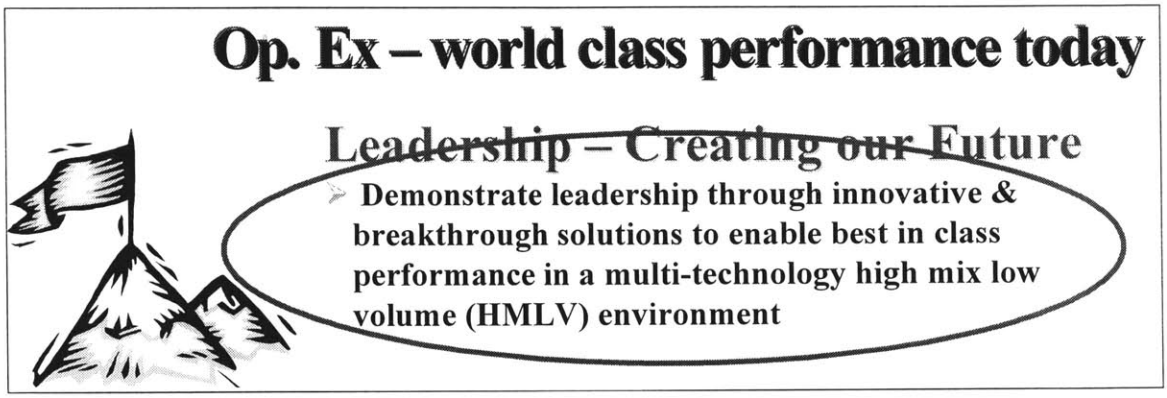

Figure 7: Excerpt from IFO H1 2003 Priorities

Starting in the third quarter of 2003, the MRC established and empowered a cross-functional working group to continue the HMLV efforts. In order to insure that all the HMLV related problems were identified and that plans were in place to close the gaps, the IFO HMLV WG initiated an HMLV education and gap analysis process. The guiding principles for the process were to insure that all of the IFO groups recognized and were adapting to both HVM and HMLV customer needs, and to create better processes and systems to manage the complexity: in particular, to improve efficiency, productivity, product cost and delivery.

3.5.1 The Gap Analysis Process

Figure 8 shows the basic IFO HMLV education and gap analysis process. All of the IFO groups affected by the HMLV transition were included in the analysis and over 230 gaps were identified. Although many gaps were already being addressed by various task forces and departmental-level efforts, the gap analysis method provided a consistent and comprehensive method to accomplish several objectives. The method helped to not only educate the organization and identify unaddressed gaps, but also to prioritize and align cross-functional efforts on the high-leverage and high-risk action items. Before long, the iterative gap analysis approach was dubbed the TopX process. The next chapter explores a number of the TopX activities in greater detail.

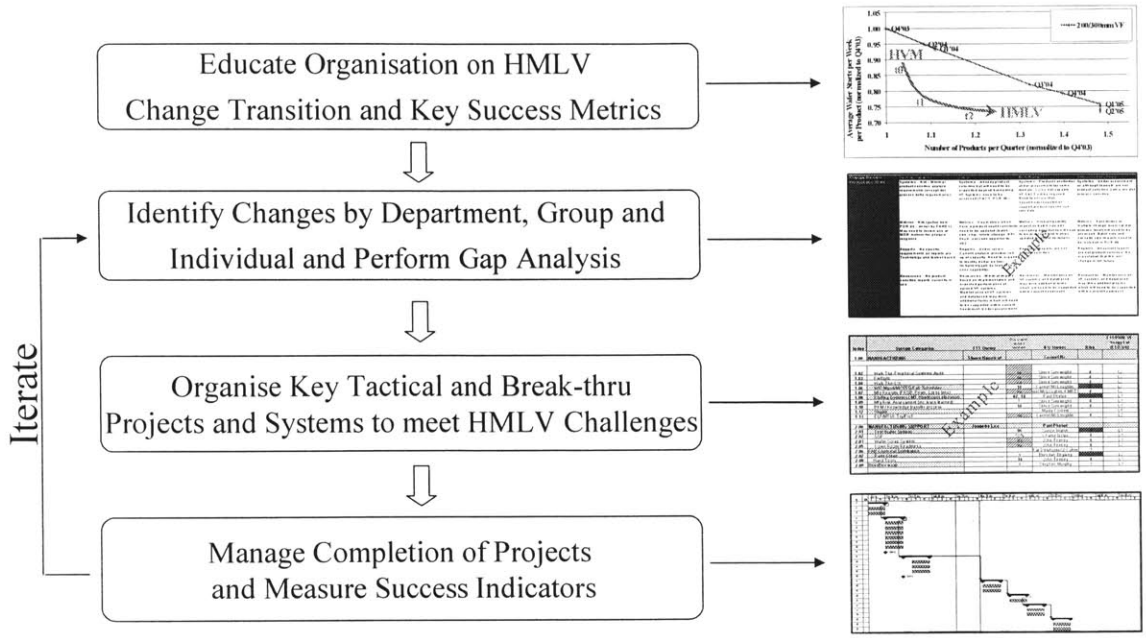

Figure 8: IFO HMLV Education and Gap Analysis Process

3.5.2 HMLV Strategies and Tactics Applied to Other Companies

Before concluding this chapter, it is worth noting that the majority of the problems and challenges of HMLV operations discussed in this chapter generalize to other companies and industries experiencing HMLV operations. While some of the tactics and strategies suggested are targeted specifically for the semiconductor industry, the concepts behind them still apply. In the case of multi-product-wafers, for example, an analogous strategy in a machining operation might be recognizing the possibility of bundling the manufacturing of a large and small product that use the same stock material and have similar volumes. In this way, tool setup time could be reduced. In addition, if designed well, it may also be possible to reduce waste material and cycle time.

Chapter 4: A Summary of the TopX IFO HMLV Activities

Up to this point we have focused on the basic context of Intel and IFOs HMLV challenges. Some of the high-level problems with HMLV semiconductor manufacturing were discussed and strategic and tactical responses suggested. We concluded the last chapter with a description of the gap analysis process used by IFO to identify and capture the most important problems that were not otherwise being addressed.

In this chapter we shift to some of the key activities identified to respond to the current and anticipated future problems. Many of the TopX activity groups are identified and some of the critical projects within each category are briefly discussed. We then begin our deep dive into one of the activity groups identified as high-leverage, improved scheduling and WIP management. In the following chapters we focus on a case study of one project within this category: the optimization of in-process metrology inspection rates.

4.1 HMLV Cultural and Organizational Alignment

The importance of high-level cross-functional buy-in to both the challenges of HMLV manufacturing and the best response options is critical. By starting the problem exploration process with the senior fab leadership and staff, all team members developed a common language and understanding of the problems. This facilitated not only the thoughtful identification of the need for new or changed metrics and the alignment of the sometimes conflicting organizational goals, but also the support and empowerment of the IFO HMLV WG to identify the key tradeoffs, and to make appropriate system-level and department-level changes. The ongoing success of the TopX activities will depend largely on the management recognition of, and the support given to the implementation teams.

Although other fabs may be tempted to shortcut the process and dive directly into some of the solutions suggested, we believe such an approach will undermine one of the most important and challenging aspects of managing the HMLV transition: engaging the senior leadership in an analysis of the cultural and organizational changes necessary to set the foundation for HMLV success.

4.2 HMLV Capacity Management and Setup Elimination

Some of the key HMLV capacity management and setup elimination activities include updating the capacity models and metrics for the product and volume mix, developing new capacity analysis tools, improving product and process flexibility and eliminating setups through more effective lot prioritization and batching.

Given the complexity of determining realizable run rates in a dynamic HMLV environment, new analysis and planning tools were developed. Ken Daly's October 2, 2003 ISSM paper on *Batched and Cascaded Run Rate Validation in a Multi-module*

Toolset provides an example of one such tool. Another useful internal document is Tami Maik, Pinhas Koren, Zahi Shaked and Efrat Aran's, *An Interactive Tool for Analyzing Capacity Scenarios.*

Significant improvements in product and process flexibility were key enablers of HMLV production in IFO. In 2002 and 2003, over 31 major process flexibility projects were completed to allow tool and process sharing for different product families and process technologies. In addition, several new systems were developed to improve in-process WIP visibility and to more accurately project future WIP positions. These systems enable tool and tester setups optimization and planning and help to insure that the fab consistently meets its customer commits. Some useful internal documents on process flexibility include Tami Maik, Pini Koren and Shmulik Perez's, *Being a Flexibile Fab – The Key for Long-term Success* and Paraic Mc Glynn and Mary O'Dea's, *How to Get Predictable Throughput Times in a Multiple Product Environment.*

4.3 HMLV Customer Protection Strategies

HMLV customer protection strategy activities were critical to manage the HMLV transition. Some of the activities include the dynamic scheduling of in-process lots to meet changing end-of-line target inventory levels and the more accurate forecasting of individual product manufacturing parameters for improved commits planning. Other important activities include the analysis of the batch size and lot scheduling processes and the analysis of finished goods inventory levels. Both activities helped IFO to manage the higher excursion sensitivities of many HMLV products.

4.4 HMLV Process Control System Improvements

To manage the complexities of more products and lower volumes, many tool sets adopted automated process control (APC) to respond to the nearly unmanageable number of product-modulated control parameters and frequent tool setups and configuration changes required. In addition, several new analytical software packages were implemented or adapted to the HMLV environment to improve the rapid identification and resolution of under-performing tools or processes.

4.5 HMLV Product and Process Health Monitoring Improvements

A vast number of changes had to be made to adapt the HVM designed product and process health monitoring systems to deal with the HMLV challenges. In addition, some of the product health metrics had to be adapted or changed to focus on high confidence supply or more integrated supply-based indicators.

Other key activities include the development of continuous product capabilities and robust data archiving procedures to avoid periodic re-NPI requirements. The dramatic increase in the number of overall NPIs required organizational changes as well. While some NPIs had been managed by ad-hoc processes and teams in the past, in the HMLV

environment it proved advantageous to establish formal ongoing cross-functional NPI teams to improve productivity and to accelerate the NPI and qualification processes.

4.6 HMLV Improved Scheduling and WIP Management

Although IFOs HMLV success in 2003 would not have been possible without many of the changes discussed so far, one of the highest leverage set of activities identified was improved scheduling and WIP management. Several of the key activities include the development of an improved goal calculation and segment inventory pace tool, the development of a technology and product based prioritization process and system upgrades and improvements to allow more frequent WIP tracking and lot dispatch updates.

4.6.1 Multi-Product Line Manager

Perhaps the most important of the complexity management scheduling tools being developed to cope with the HMLV challenge is Multi-Product Line Manager (MPLM). While MPLM bears some similarity to Samsung Electronics Corporation Limited's Short Cycle Time and Low Inventory in Manufacturing (SLIM) operations methodology, it goes much further. At its core, MPLM is an event-driven fab simulation and mathematical decision support tool. It dynamically monitors all of the current and expected process variables and provides users with a variety of manufacturing options that balance output, utilization and lot tardiness in different ways. But, MPLM provides more than a couple of manufacturing processing options based on a mathematical simulation. It also provides the detailed step-by-step implementation plans and system monitoring and support tools required to turn the chosen option into reality.

4.6.2 Skip-Lot Exploitation

Another key scheduling and WIP management improvement project is skip-lot exploitation. Since HMLV causes significant increases in tool setups, generally non-value added (NVA) in-process measurement rates and their related costs skyrocketed. By closely monitoring the events that control measurement rates, the skip-lot exploitation team discovered a number of ways to successfully reduce in-process measurement rates to levels much closer to their maximum skip rate targets.

While the skip-lot exploitation team helped reduce costly in-process measurements to rates closer to their targets, the metrology inspection rate team developed a new method to optimize the target rates for the HMLV environment. In the following chapters, the in-process metrology inspection rate optimization project and results are described in greater detail. The discussion that follows serves as a case study of the type of work required to adapt an HVM process and method to meet the challenges of the HMLV environment.

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Chapter 5: In-Process Metrology Inspection Rates and HMLV

In the last chapter we took it as a given that in-process metrology inspections are a necessary but costly activity. In this chapter we explore the topic in greater detail, starting with a discussion of why in-process inspections are employed and when it may make sense to eliminate or reduce them. We then explore some of the reasons that HMLV causes significant degradations in manufacturing metrics specifically because of HMLV-induced impacts to metrology operations. We conclude with a brief review of the metrology inspection rate optimization methods in use at Intel and a discussion of how the current methods lead to undesirable results in the HMLV environment.

5.1 Reasons for In-Process Inspections

There are three main reasons for in-process metrology inspections: process discovery and optimization; process control; and yield prediction and excursion management. In order to choose an appropriate sampling methodology, it is important to know which objective or objectives must be met.

The objective of process discovery and optimization is to understand how the machine and material states and properties affect device characteristics, product reliability, manufacturing performance and yields, and to tune the inputs to achieve the desired results. This is the primary objective at most development fabs and for HVM fabs during product or process ramps. During these stages it is important to collect as much data from as many steps in the process as possible to quickly maximize yields and to stabilize the processes. Large data volumes are also necessary to determine the coverage, accuracy or potential redundancy of process monitors and to estimate the statistical risks of reducing or elimination these monitors. Process discovery, however, is not strictly related to the development and ramp phases of the product lifecycle. Even mature and stable processes may need to return to the process discovery inspection regime to facilitate ongoing process improvements or to verify the effects of major process changes or events.

While many semiconductor processes are relatively stable and highly capable,[27] others degrade over time or are incapable of meeting the desired product specifications or process tolerances without regularly adjusting the process inputs. For these processes, a consistent feedback mechanism is required. In these cases, an appropriate control method must be chosen and a more detailed analysis performed to determine the measurement rates required to control the process. For more information on feedback control, see Box and Luceño's, "Statistical Control by Monitoring and Feedback Adjustment" or the other footnote references.[28]

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[27] Process capability is generally measured by a ratio of the allowable specification or disposition range and the range of the specification variable. The most common process capability ratios used at Intel, Cpk and Cpd, also adjust for the specification variable's distribution characteristics.

[28] Box, G. and A. Luceño. Statistical Control by Monitoring and Feedback Adjustment. John Wiley & Sons, Inc. New York. (1997).

For most stable and capable processes, however, the primary reasons for in-process measurements are for yield prediction and excursion management. The objectives here are to estimate the WIP yields and to detect, eliminate and control the costs of process excursions. This information helps manufacturing adjust wafer starts and processing plans to meet delivery schedules. The choice of an appropriate sampling plan in this regime depends on a number of factors such as: process capability; the amount, proximity and effectiveness of other process monitors; inspection tool capacities; staffing levels; inspections costs; and product value. The methods discussed in this thesis are appropriate when the in-process measurement objective is yield prediction and excursion management.

5.2 HMLV Causes Significant Increases in Metrology Inspection Rates

Figure 9 is a system dynamics model showing how HMLV manufacturing impacts fab metrics, processes and activities. The examples that follow demonstrate how to interpret the model.

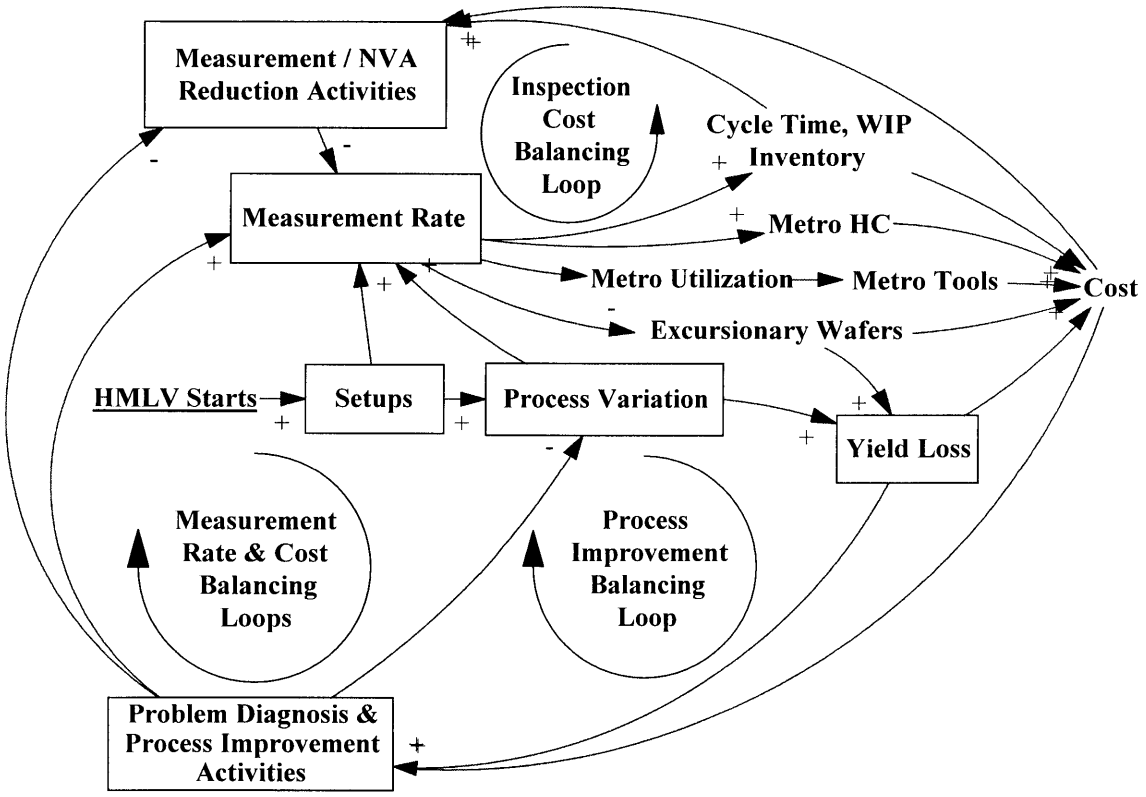

Figure 9: System Dynamics Model of HMLV Metrology Impacts

Hardt, D.E. Modeling and Control of Manufacturing Processes: Getting More Involved. ASME Journal of Dynamic Systems Measurement and Control, 115. (June 1993). pp. 291-300.
Siu T. Z. Cycle to Cycle Feedback Control of Manufacturing Processes. SM ME MIT Thesis. (Feb. 2001).
Ponchner, Karen. Implementing Advanced Process Control in a Copy Exactly! Environment. LFM MIT Thesis. (June, 2002).

As discussed previously, the introduction of more products requires more setups at product specific operations such as lithography. This cause and effect relationship is captured by the "+" next to the arrow between the HMLV Starts and Setups boxes. The positive arrow indicates that as the number of HMLV starts increase, setups also increase. Continuing in this way, we can see that as setups increase, measurements rates also increase. An increase in measurement rates in turn causes an increase in metrology (metro) headcount (HC) which in turn increases costs. As costs increase, management responds by increasing measurement and non-value added (NVA) reduction activities. Finally, as the measurement and NVA reduction activities increase, measurements rates decrease; the decrease is indicated by the "-" sign next to the arrow connecting these last two entities. Since we have returned to one of our earlier entities, measurement rates, we have now completed one full cause-and-effect loop.

If we imagine how the effects of this particular loop cause changes in fab operations over time, we can develop a deeper understanding of some of the dynamic effects of introducing more products into the fab. Summarized, the net effect of an increase in HMLV starts is to increases measurement rates initially. However, as measurement and NVA reduction activities increase, the process balances out provided the mitigation activities are of sufficient strength to counteract the HMLV impulse. The actual dynamics of the system depend on the rates of the various cause-and-effect linkages and on how they change over time. In particular, the stability and net increase (or decrease) in the measurement rates depends on the relative strength of the input and balancing forces. Because the HMLV caused increase in measurement rates is decreased by the NVA and measurement reduction activities, this cause-and-effect chain is referred to as a balancing loop; the balancing dynamics of this loop are indicated on the model diagram by the Inspection Cost Balancing Loop icon with the counterclockwise circular arrow.

Although the dynamics in general depend on the magnitude of the input and balancing forces, for this particular case it is worth noting that the three loops are all balancing and that the activities they describe exhibit diminishing rates of return. That is, while initial measurement reduction activities may be able to recover most of the initial increases in measurement rates, additional activities generally achieve only smaller, incremental levels of success. Said another way, the balancing forces are weaker than the input forces and only serve to mitigate the initial effect. This fact allows us to make some generalizations about the net effects of increased HMLV starts on the fab activities and metrics shown in the model. In particular, an increase in HMLV starts causes increases in both process variation and measurement rates. Increases in measurement rates and process variation, in turn, cause higher overall yield losses, longer cycle times, more WIP inventory, more metrology labor and higher metrology tool utilization. Depending on the increase in utilization, the increased measurement rate may also lead to the need for more metrology tools. Moreover, increases in HMLV starts increase the measurement/NVA reduction and the problem diagnosis and process improvement activities. In turn, both activities drive increases in either indirect labor or productivity levels. All of these effects cause increases in product and overall system costs.

To simplify the discussion so far, we have only discussed one of the cause-and-effect loops. But, as the multiple arrows coming out of the setups box and three balancing loops discussed above indicate, there are multiple effects of an increase in HMLV starts which must be considered to understand the overall dynamics of the system. Rather than exhaustively discussing all of the dynamics, we discuss only one more loop that is particularly pertinent to the discussion that follows before summing up.

The model can also be used to understand decreases in various parameters. But, care must be exercised in the interpretation. For example, lower measurement rates cause an increase in excursionary wafers, end-of-line yield losses and an increase in problem diagnosis and process improvement activities. These activities in turn cause increased measurements rates and reduced measurement reduction activities. These dynamics are summarized by the measurement rate and cost balancing loop icons.

Since measurement rates increase inspection related costs but decrease yield-loss related costs, a balance must be struck in either the problem diagnosis and process improvement activity or the NVA and measurement reduction activity mechanisms to insure that the system is both stable and cost effective.

Although we have only discussed a qualitative system dynamics model in this thesis, a more rigorous quantitative model of the system can be developed and used to tune the overall performance of the system.[29] The following chapter discusses the MOST/2 tool and method developed for this purpose. Before discussing MOST/2, however, we need to provide a little more background information to set the context. In particular, in the remainder of this chapter we discuss how Intel's measurement rates compare with their competitors. We also provide more information on the metrology process and measurement rate support and control systems. We conclude with a review of Intel's current metrology inspection rate methods and comments on how they perform in the HMLV environment.

5.3 Industry In-Process Measurement Rate Labor and Cycle Time Comparisons

Although it is difficult to find detailed verifiable information on product inspection rates for Intel and its competitors, a 2001 Non-Valued Added Benchmarking Survey conducted by Sematech's Manufacturing Methods Council provides some insight. The companies surveyed include Advanced Micro Devices; Hewlett-Packard Company; IBM; Motorola, Inc.; Texas Instruments Incorporated; Infineon; Philips; TSMC and Intel.

Pertinent findings from the self-reported survey include: the percentage of manufacturing direct hours spent on NVA functions such as measurements, inspections and tool checks; the percentage of product measurements; the percentage of lot cycle time spent on process measurements; and the almost uniform use of process-based

[29] Many good books have been written on system dynamics modeling. For additional information, see, for example: Sterman, John D. Business Dynamics: Systems Thinking and Modeling for a Complex World. The McGraw-Hill Book Company. Boston, MA. (2000).

measurements to control processes, detect excursions and disqualify poorly performing tools.

Relative to the group averages, in 2001 Intel reported spending approximately 10% more time on NVA operations and 5% more time on product measurements. But, Intel was close to the group average on the percentage of lot cycle time spent on product measurements. However, a comparison of Intel's average per-layer cycle times with averages of some of its competitors[30] indicates that the amount of product measurement related cycle time is likely well above average.

One of the most revealing comments in the survey is the following excerpt from one of the respondents.

> "We perform a significant amount of monitoring without clear or evident pay-backs...[m]any times we have found the NVA process was put into place due to a customer issue, scrap event, and/or a one time excursion and no one went back later to determine if true cost/value still holds..."

5.4 The Lithography Process Loop and Metrology Operations

As Figure 10 shows, the basic Lithography loop includes a number of metrology steps. After Spin/Expose/Develop, the registration check (REG) metrology step insures that the photoresist pattern has been properly aligned to the underlying wafer layers. The next metrology step shown on the diagram, CD-SEM DCCD, uses a critical dimension scanning electron microscope to do a design check of the critical dimensions (DCCD) of the photoresist-patterned wafer. As indicated, both of these steps can be reworked if problems are discovered. Finally, after ion implantation, etch, or film deposition, the photoresist is removed and the wafer proceeds to another CD-SEM tool for a final check of the critical dimensions (FCCD) of the device structures.

Although not shown or discussed in this thesis, there are additional metrology and inspection steps throughout the fab which would benefit from the optimization of their in-line inspection rates. In the interest of brevity we will focus on the optimization of CD-SEM metrology inspection rates for our analysis. It should be noted however that the tools and methods discussed can be directly applied to most of the other inspection processes.

[30] The comparison is based on: Competitive Semiconductor Manufacturing Benchmarking Report for the Period from 1996-2000. http://esrc.berkeley.edu/csm/CSM52_fig3.doc (3 March, 2003). Figure 3-21.

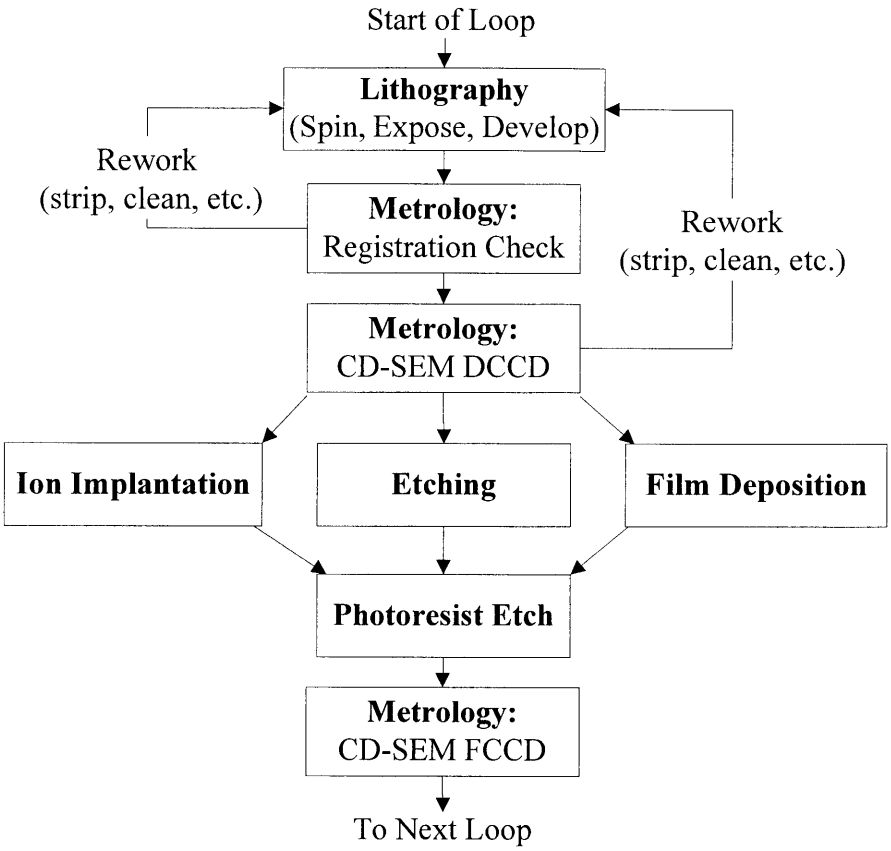

Figure 10: General Lithography Loop Sequence with Metrology Operations

5.5 The SkipLot5 System

The SkipLot5 System is an Intel developed software support tool that controls the routing of wafer lots based on the desired skip rate[31] at a given inspection step, recent inspection step results and a number of other controlling events. The basic algorithm is a state machine adapted from ANSI/ASQC Standard S1-1987 and others.[32]

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[31] For the purposes of this discussions and consistency with SkipLot5, skip rate is defined as the number of lots that are skipped for each lot that is measured. So, for skip rate = 5, the sequence would be MSSSSSMSSSSS…where M indicates a measured lot and S indicates a lot that is skipped. In some of the literature, skip rate refers to the size of the group, i.e., skip rate plus one. Where we have a need to distinguish between the two definitions, we refer to the first definition as the skip rate and the second as the skip group or group.

[32] Liebesman, B.S. and B. Saperstein. A Proposed Attribute Skip-Lot Sampling Program. Journal of Quality Technology, Vol. 15, No. 3. (July 1983).
Liebesman, B.S. The Development of an Attribute Skip-Lot Sampling Standard. Frontiers in Statistical Quality Control, 3rd Edition by Lenz et al. Physica-Verlag. Heidelberg, Germany. (1987).
American National Standard: An attribute skip-lot sampling program. ANSI/ASQC Standard S1-1987. American Society for Quality Control. (1987).

As Figure 11 shows, the skip-lot algorithm involves three states: qualification, skipping and re-qualification. Each state has a set of user defined input parameters to control how the machine behaves. When we discuss how to choose the optimum skip rate, we are generally referring to one of these parameters in particular: the maximum skip rate.

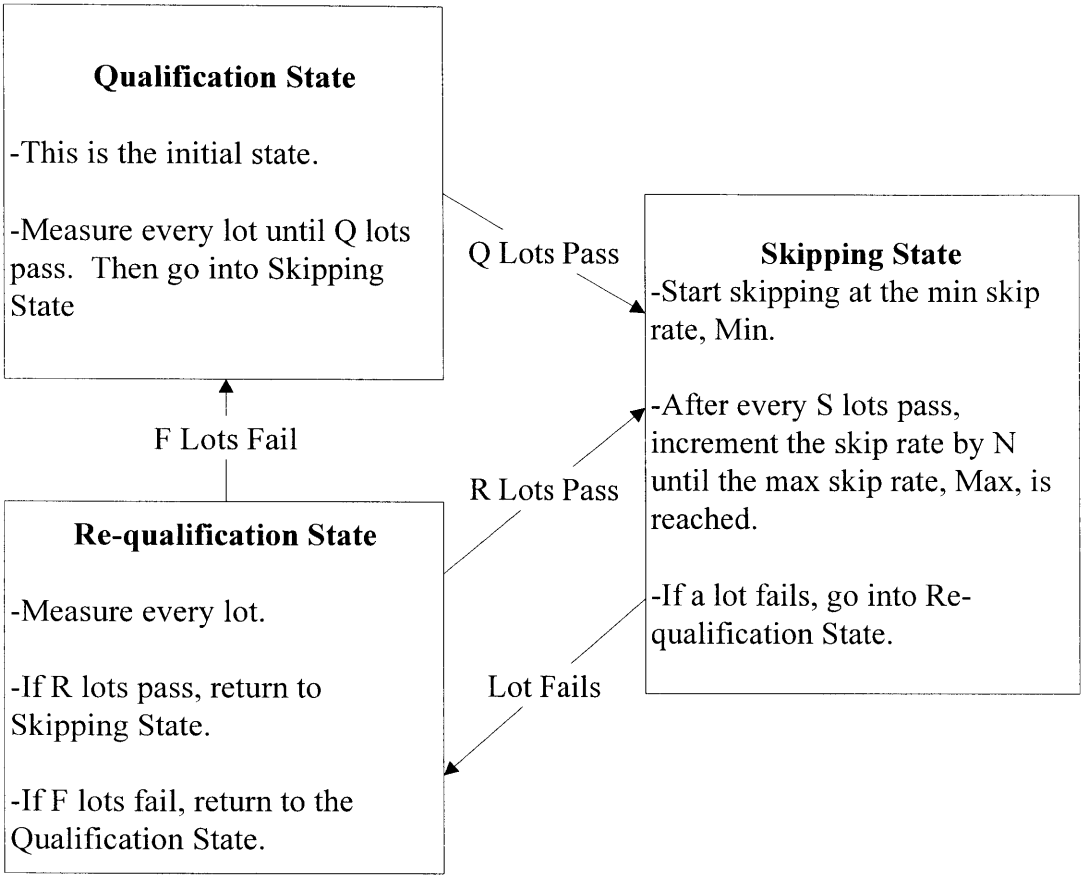

Figure 11: A Skip-Lot State Diagram

SkipLot5 incorporates the basic algorithm shown in Figure 11 into a full software control package which allows additional inputs such as tool, lot and process aggregation parameters; the maximum number of lots at risk; the maximum amount of time that can elapse between measurements, and other controlling events such as the need to re-qualify a process after a preventative maintenance or a change of the lithography reticle.

5.6 Intel's Current Inspection Rate Methods

Intel has a number of different general and specific inspection rate methods to meet the particular needs of individual process technologies and tools, and the different in-process inspection objectives. With the exception of a few operations, however, the majority of processes in IFO in 2003 determined their inspection rates based on a general

statistical worksheet developed by the Intel Statistics Users Group.[33] In late 2003, IFO began using a new monitor sampling and optimization tool, MOST, to better balance in-line inspection costs and risks at a few operations. Both methods are discussed in greater detail below.

5.6.1 The Basic Inspection Rate Method

The basic inspection rate worksheet consists of two parts. The first part is a structured questionnaire to validate that the method is appropriate to the inspection objectives and process characteristics. The questions help to insure that the monitor's objective is yield and excursion management and that the process monitors are not redundant or incapable of providing useful information. They also help to verify that the process is stable and in control. In particular, they check to make sure that the output variations are due to normal in-process variations rather than special or assignable causes.

The second part of the worksheet is a table that identifies the recommended SkipLot5 inspection rate parameters as a function of the process capability, percentage of out of disposition (OOD) events and other process conditions. The process capability ratio used for this purpose is Cpd.[34] It is typically calculated from the last one to three months of in-process data. Cpd is calculated as the minimum of $(UDL-\mu)/3\sigma$ or $(\mu-LDL)/3\sigma$ where UDL and LDL are the upper and lower disposition limits, respectively, μ is the process variable mean, and σ is the standard deviation. For most operations, several different process variables must be evaluated. Generally, the most conservative skip rate recommendation is used for the set of process variables evaluated. For processes that are marginally capable, other process operating characteristics are sometimes evaluated.

5.6.2 The MOST Inspection Rate Method

Over the last couple of years, several different engineering groups at Intel recognized that in many cases, the basic inspection rate method required more inspection than was cost effective. As a result, a monitor optimization and support tool, MOST, was

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[33] See, for example: Change [removed for confidentiality] Skip Rate Methodology from Cpd Based to MOST (ROI) Based. http://rrrdm01ea01p/pccb/website (17 June 2002). Alternatively, see: Amar, Ajay. Reduction of Process Monitoring in Semiconductor Chip Manufacturing. LFM MIT Thesis. (June, 1999). pp. 22-24. In addition to the basic method, there are a number of derivative methods that share the basic framework discussed.

[34] Most of the statistics literature refers to the ratio of the specification range to the distribution range as Cp. When corrected for the distribution mean as discussed above, the ratio is typically referred to as the Cpk. See, for example: Montgomery, Douglas C. Introduction to Statistical Quality Control. 4th Edition. John Wiley & Sons Inc. (2001). pp. 357-373. For many of the operations analyzed in this thesis, the processes do not have true specification limits. When this is the case, the process is typically set up using the disposition limits. For this reason, we have used the terminology Cpd to indicate that the ratio is with respect to the disposition limits rather than the true specification limits. When available, it is preferable to use the true specification limits.

developed. MOST includes several elements: BKMs and support materials; a simulation tool; and a probability based economic cost minimization model.[35]

The MOST model's basic inputs include distribution information for the percentage of out of control (%OOC) process events, the percentage of out of disposition (%OOD) events, the current process skip rate, the wafer value, the metrology tool's power to detect (PtD) a problem, the weekly wafer start volume, the inspection cost, and the end-of-line yield impact. Since the input parameters are not known with certainty, a Monte-Carlo type simulation is used. Briefly described, the simulation tool randomly[36] and independently chooses a value for each of the input parameters. The model chooses the parameters in such a way that over many simulations the input parameter distributions mimic their desired distribution shapes. For the MOST simulator, the input parameters are treated as triangle distributions: an inaccurate but computationally convenient and generally conservative choice.[37]

For each set of input parameters, MOST calculates the expected annual inspection and excursion costs and determines the skip rate that minimizes the total cost. For each calculation run, the minimum calculated skip rate is added to an optimum skip rate histogram. By repeating this process many times, a distribution of the optimum skip rates is developed for the full range of input parameters. For the MOST model, the process is typically repeated 300 times. The median of the optimum skip rate distribution is then calculated and used for the SkipLot5 max skip rate input parameter.

5.7 Shortcomings of Current Intel Metrology Inspection Rate Methods

There are positive aspects of both methods currently in use at Intel. The basic method is simple to use and requires only input parameters that are readily available from other fab systems. In addition, the basic method requires very few engineering judgments. And, both approaches are generally conceptually sound and conservative if followed properly. Although more complicated, the MOST method is a significant improvement over the basic method because it attempts to meet not only the customer's

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[35] Amar, Ajay. Reduction of Process Monitoring in Semiconductor Chip Manufacturing. LFM MIT Thesis. (June, 1999). pp. 22-24.
Bean, John W. Variation Reduction in a Wafer Fabrication Line through Inspection Optimization. LFM MIT Thesis. (June 1997).
Williams, Randy, Sridhar Seshadri, J. George Shanthikumar, Dadi Gudmundsoon and Arun Chatterjee. Challenging the Monitor Reduction Paradigm to Reduce Costs. Yield Management Solutions. (Spring 2000).

[36] No simulation tool can truly create an independent random distribution but the point is really somewhat academic provided the tool uses a sufficiently large number of runs with quasi-random starting seeds. This is the case for the MOST and MOST/2 simulators.

[37] If the true distribution is normal, a triangle distribution provides more heavily weighted tails. In this sense, it is conservative. However, the triangle distribution truncates the most extreme values so is less conservative in the upper and lower regions of the distribution. Moreover, if the distribution is better modeled as uniform, for example, the use of a triangle distribution grossly underestimates the likelihood of input parameters in the upper and lower portions of the distribution.

quality and reliability[38] objectives, but also their desire for low cost ICs. Unfortunately, both methods have poor support and implementation documentation and lack transparency. Moreover, neither tool adequately manages the complexities of the HMLV environment or allows users to make fully informed decisions about the benefits and risks of higher skip rates. In particular, as typically implemented in the fabs, both methods treat all wafers equally.[39] As a result, the current methods cause higher risks for low-volume and high-value products, and higher costs for high-volume, low-cost products. For these reasons, we have developed another model, MOST/2, which we discuss in detail in the following chapters. To pave the way, key characteristics of the basic and MOST methods are compared with the MOST/2 method in the table below.

[38] All of the Intel's chips are inspected at the end of the line to insure that their performance and reliability meet the customer's needs. As a result, decreases in the measurement rates in-process do not directly affect customers.

[39] The basic and MOST methods and the SkipLot5 system do not prohibit the calculation of optimal skip rates on an individual product or product group basis. However, to do so would be very labor intensive and prone to errors given the current systems. MOST/2 provides the necessary tools, analytical framework and supporting documentation to manage the complexity associated with calculating optimal skip rates on a product or product group basis.

Characteristics	Basic Method	MOST Method	MOST/2 Method	Comments
Process variation data used to estimate skip rate risks?	Yes	Yes: Cpd, OOD	Yes: Cpd, OOD	Both MOST methods estimate the number of OOD lots as a measure of risk.
Requirements and processes for collecting data specified?	No	Limited	Yes	MOST/2 provides data collection tools, procedures and update frequency suggestions.
Input parameter distributions accurately captured?	N/A	Limited	Yes	MOST models inputs as triangle distributions. MOST/2 uses the actual distributions.
Product or product group aggregations procedures specified?	No	No	Yes	MOST/2 provides suggestions for how to aggregate products and product groups.
Expected Material at Risk (MAR) used for cost/risk tradeoffs?	No	No	Yes	MOST/2 uses an improved probability estimate for MAR.
Relevant inspection costs captured?	N/A	Some	Yes	MOST/2 provides more accurate inspection costs.
Does method capture value added to wafers in process?	No	No	Yes	MOST/2 provides process step specific wafer cost values.
Does method capture the value of different products?	No	Limited	Yes	MOST/2 uses product or product groups costs in economic model.
Does method balance cost and risk?	No	Yes	Yes	MOST/2 provides cost vs. skip rate information.
Does method allow users to assess cost / risk balance?	No	No	Yes	MOST/2 provides cost curves and output variation information to allow cost/risk balancing.
Does method account for WIP to determine customer impacts?	No	No	Yes	MOST/2 uses WIP positions to assess potential for customer impacts.
Does method provide stability over time?	No	No	Yes	MOST/2 accumulates risk data to insure process stability.
Is the process fully automated?	No	No	No	The basic, MOST and MOST/2 methods require increasing levels of user effort.

Table 5: Comparison of Basic, MOST and MOST/2 Methods

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Chapter 6: A Customer Needs-Focused Complexity Management Tool and Method for In-Process Metrology Inspection Rate Optimization

In the last chapter we discussed some of the shortcomings of the current inspection rate methods and compared them with a proposed new method: MOST/2. In this chapter we discuss the details of MOST/2. The mathematics of calculating the risk of excursions, material at risk (MAR) and the potential for, and magnitude of customer impacts are provided. The relevant economics are explored including how to calculate inspection costs and how to determine the correct wafer value to use for a given manufacturing step. Particular attention is paid to how MOST/2 captures the more varied needs of HMLV customers and manages the complexity of different products, manufacturing processes and operational conditions. The chapter concludes with a sensitivity analysis and some examples to make the material more tangible and to help potential users develop some intuition for the method and tool.

6.1 Overview of MOST/2

The MOST/2 method is conceptually similar to MOST. Several product and process parameters are used to determine the risk of future excursions. A probability model is also used to determine the expected MAR. Combining the two, excursion costs are estimated and added to inspection costs to determine the total annual process costs as a function of the process skip rate. A simulation tool is used to calculate and plot the family of cost/risk tradeoff curves that result from the input parameter distributions. Through the supporting documentation and model, the relevant economics are captured by aggregating products into groups with similar characteristics, capturing the value of the product group based on the current environment, and accurately calculating the lot rework and inspection costs.

6.2 Calculating the Risk of Excursions

There is no easy way to predict the risk of future excursions. To the extent that historic operating conditions are similar to or worse than the conditions expected in the future, however, historic process data provides a good, generally conservative starting point. While this may seem like a large assumption, the continuous improvement and CE! culture at Intel make it fairly robust. Both MOST and MOST/2 recommend the use of historic data and engineering judgment to estimate future excursion risks.

Engineering judgment is necessary for two main reasons. First, when the source of an excursion has been identified and eliminated, it should no longer be counted in our estimates for the future. Second, when multiple lots have been affected by a single excursion event, we should only count the event once. Engineering judgment is necessary to insure that we accurately determine the number of excursion events that occurred in the past and which may occur in the future. When we refer to the number of excursions in the discussion below, we are specifically referring to the number of excursion events that may occur again.

To be clear, let us define A as the event that the process goes into excursion while processing a given lot. $P(A)$ denotes the probability of event A. As shown below, $P(A)$ is approximately equal to the quotient of the number of excursions and the number of lots through the process. The approximate relationship, of course, becomes exact as the number of lots processed goes to infinity. The relationship on the right is an alternative calculation method from MOST which uses the number of out-of-control ($\#OOC$) events, the number of out-of-disposition ($\#OOD$) events, the measurement rate, and the skip rate (the number of measurement lots divided by the total number of lots through the metrology loop) to arrive at a similar estimate.

$$P(A) \cong \frac{\#excursions}{\#lots\_thru\_metro} = \frac{\#OOC}{\#Measurements} \bullet \frac{\#OOD}{\#OOC} \bullet \frac{\#Measurments}{\#lots\_thru\_process}$$

Equation 1: The Probability the Process Goes into Excursion while Processing a Given Lot

But, why is the skip rate part of the calculation? Since we only measure a fraction of the lots, we have to estimate the results for the entire population based on the measured population. There are two basic approaches for how to do this. One approach is to assume that once a process goes into excursion, it stays in excursion until detected and corrected. An alternative approach is to assume that somehow an excursionary process can heal itself. While this last assumption may at first sound unlikely, it is not. Take, for example, an excursion due to a contamination particle on a lithography reticle that prevents the proper focus and exposure of the photoresist on the wafer. When the next lot from another product arrives, the reticle will be changed and the contamination particle will likely be dislodged. This may occur between metrology operations; in essence, the process has healed itself even though the problem was never detected at the in-process inspection step.

So, which assumption should we use? Which approach is more realistic? The reality is of course in the middle. Some excursion sources self-correct but others require intervention. To be conservative, we suggest that $P(A)$ should be calculated as the quotient of the number of excursion events and the number of lots through the metrology process. This corresponds to the assumption that a process that goes into excursion stays in excursion until detected and corrected. It also assumes that excursions detected for the measured population are representative of the entire population.

6.3 A Probability Model for Determining Material at Risk

In order to determine a probability model for the material at risk, a number of assumptions must be made. In particular:

1. Once a process goes into excursion it stays in excursion until detected and fixed.
2. All lots that go through an excursionary process are affected. Likewise, all wafers in an excursionary lot are affected.

3. The likelihood of a process going into excursion is independent of the lot being processed.[40]
4. The disposition limits are valid and any lot that is considered OOD will be considered excursionary.[41]

Let us define B as the event that the process goes into excursion sometime during the processing of a given measurement group[42] of size T. Since the chance of the process going into an excursion, $P(A)$, is independent for each lot, it is relatively straightforward to calculate $P(B)$ by summing the mutually exclusive ways that it could occur for a given measurement group. The equations below show the calculation.

$$P(B) = P(A) + (1 - P(A))P(A) + (1 - P(A))^2 P(A) + \ldots + (1 - P(A))^S P(A)$$

$$P(B) = P(A)\sum_0^S (1 - P(A))^n$$

$$P(B) = 1 - (1 - P(A))^{S+1} = 1 - (1 - P(A))^T$$

Equation 2: The Probability of a Process Excursion in a Measurement Group of Size T[43]

While $P(B)$ is the probability that the process has gone into excursion for a particular measurement group, another useful probability is $P(X_n \mid B)$. This is the probability that the process went into excursion while processing lot X_n given that there was an excursion in the measurement group. From Bayes' Theorem we know that:

$$P(X_n \mid B) = \frac{P(X_n)P(B \mid X_n)}{P(B)}$$

Equation 3: Bayes' Theorem

Since we have assumed the process cannot fix itself, $P(B \mid X_n) = 1$. This leaves only one other term to calculate, the probability the process first went into excursion while

[40] For some process steps, we expect product or other lot specific sensitivities. This does not mean we should throw the model out. The model will still be valid provided that the probabilities of an excursion during the processing of Lot A or Lot B are roughly the same. If there is reason to believe that the risk is significantly different, there are two general approaches. The preferable option is to treat the groups separately using the appropriate risk factor for each. An alternative option is to use the more conservative estimate of the risk for both products. Historically this has been the approach chosen, likely for its simplicity. For the MOST/2 model, we suggest an intermediate approach which is to group products of similar risk together and to use the most conservative risk estimate for each grouping.

[41] When true specification limits are known, they should be used in place of the disposition limits. The ideal case is to use limits that are just within the boundaries of the process cliff, that is, the point at which end-of-line yield or performance are affected. Since this information is rarely known, an alternative is to set the limit at as high or low a value as has been determined to have had no effect on the device characteristics.

[42] We use S to denote the skip rate and T to denote the skip group. For the sequence SSSMSSSM, the skip rate is three and the skip group or measurement group size is $S+1$ or four.

[43] The full derivation of this expression can be found in Appendix A.

processing lot X_n which we have denoted $P(X_n)$. This value we have already shown in Equation 2 to be $P(A)(1-P(A))^n$.

Putting it all together, we can now calculate the sum of $P(X_n \mid B) \bullet (\#Lots_n)$ from n = 0 to n = skip_rate, S. This gives us the expectation of the number of lots affected given that the process went into excursion while processing measurement group T. This quantity we denote as $E(\#Lots_n \mid OOD)$ and will abbreviate as N.

$$E(\#Lots_n \mid OOD) = \frac{P(A) \bullet T}{P(B)} + \frac{P(A)(1-P(A)) \bullet (T-1)}{P(B)} + \ldots + \frac{P(A)(1-P(A))^S \bullet (T-S)}{P(B)}$$

$$E(\#Lots_n \mid OOD) = \frac{P(A)}{P(B)} \sum_{n=0}^{S} (1-P(A))^n (T-n)$$

$$E(\#Lots_n \mid OOD) = T + \frac{(T-1)(1-P(A))^T}{P(B)} - \frac{1-P(A)-(1-P(A))^T}{P(A)P(B)}$$

$$N = E(\#Lots_n \mid OOD) = T + \frac{(T-1)(1-P(A))^T}{P(B)} - \frac{1-P(A)-(1-P(A))^T}{P(A)P(B)}$$

Equation 4: The Expected Number of Lots Effected Given an Excursion in a Measurement Group of Size T[44]

But, what happens if our measurement process does not always detect an excursion? That is, what if the metrology tool has a limited power to detect an excursion? This probability can also be estimated[45] and included in the probability model. Let's call C the event that our measurement process detects an out-of-disposition lot from an excursionary process. Similar to how we proceeded previously, we will now calculate the number of lots we expect to be at risk, the MAR, provided that our measurement tool has detected an OOD event and that our measurement tool has an imperfect ability to detect lots from an excursionary process. This quantity we denote as $E(\#Lots_n \_ OOD \_ C)$ and calculate as:

[44] The full derivation of this expression can be found in Appendix A.

[45] The probability of detecting an excursion, the power to detect (*PtD*), can be estimated using engineering judgment. It is generally helpful to compare the gauge capability of the measurement system with the magnitude of deviation expected in the measurement variable(s) when the process goes into excursion. For most processes, *PtD* is between 0.9 and 1.0.

$$E(\#Lots_n\_OOD\_C) = P(C)N + P(C)(1-P(C))(N+T) + \ldots + P(C)(1-P(C))^n(N+nT) + \ldots$$

$$E(\#Lots_n\_OOD\_C) = P(C)\sum_{n=0}^{\infty}(1-P(C))^n(N+nT)$$

$$E(\#Lots_n\_OOD\_C) = N + \frac{T(1-P(C))}{P(C)}$$

Equation 5: The Expected Number of Lots Effected Given an Excursion in a Measurement Group of Size T with Limited Power to Detect the Excursion[46]

At this point, the hard part is over. We can choose a convenient time period such as a year and can now calculate some interesting quantities. If we multiply *P(A)* by the number of lots that will go through the process, we have a good estimate of the number of excursions to expect in the coming year.

For each excursion, the equations we have developed allow us to calculate the number of lots that will be affected as a function of both the skip rate and our ability to detect the excursion. With the assumption that all wafers are affected in an excursionary lot and estimates of the die impacted for each wafer and the value of the wafer, we can now calculate the expected annual excursion cost as a function of the skip rate. The annual excursion cost as a function of T is shown in Equation 6 below where, $k = wafer\_value \bullet wafers\_per\_lot \bullet die\_kill\_ratio \bullet lots\_per\_year \bullet P(A)$.

$$Annual\_Excursion\_Cost(T) = k \bullet \left(\frac{T}{PtD} + \frac{S(1-P(A))^T}{1-(1-P(A))^T} - \frac{(1-P(A))-(1-P(A))^T}{P(A)(1-P(A))^T} \right)$$

Equation 6: Annual Excursion Cost as a Function of T[47]

But, provided *P(A)* is small, a much simpler equation can be determined for the MAR. When this approximation is used, the annual excursion cost equation as a function of T simplifies to the expression shown in Equation 7 below. Note that this equation is now linear in T, a fact that allow us to explicitly calculate the minimum cost skip rate and model sensitivities later on in this chapter.

$$T \bullet \left(\frac{k}{2} + k \bullet average\_run\_length \right) + \frac{k}{2} = T \bullet \left(\frac{k}{2} + \frac{k(1-PtD)}{Ptd} \right) + \frac{k}{2}$$

Equation 7: Annual Excursion Cost as a Function of T for $P(A) \approx 0$

[46] The full derivation of this expression can be found in Appendix A.

[47] The die kill ratio is an estimate of the number of die or chips that are lost on an excursionary wafer. It is estimated from historic end-of-line yield data.

6.4 Determining the Relevant Economics

There are two main economic factors which have an impact on the MOST/2 model: the inspection cost and the wafer value. Although both are conceptually straightforward, in practice it is difficult to determine the true economic impacts of higher or lower skip rates on excursion and inspection costs. The following sections provide some guidance by exploring the question, what actually happens if we increase or decrease the inspection rates?

6.4.1 Calculating Inspection Cost

In general, inspection costs include up front costs for the purchase, installation and qualification of the tool; ongoing operating costs such as electricity, consumables, maintenance and spare parts; and direct and indirect labor costs. Some also argue that the intangible costs of inspections such as longer cycle times, higher WIP levels, lower yields and even opportunity costs such as the loss of manufacturing floor space should be included as well. While we do not disagree on many of these points, we feel the more relevant question is to ask, what tangible costs will be saved in the short to medium-term if we reduce inspection rates by, for example, 50%?

From this perspective, we suggest that the most relevant tangible cost savings are in labor hours and reduced consumable and other spare parts expenses. Note, however, labor hours are only really saved if the manufacturing operators can be used elsewhere or if headcount levels are adjusted relative to production levels. Fortunately, Intel Ireland Ltd. is in a growth phase and has been able to immediately realize cost savings from higher skip rates by redeploying or re-tasking manufacturing inspection operators rather than hiring more operators.

When determining cost savings from reduced consumables and other spare parts expenses, the involvement of the engineering tool owners is crucial to determine what costs will and will not be saved. In some cases, higher skip rates allow a reduction in the number of inspection tools used and significant ongoing operating cost savings can be realized. However, a reduction in tools does not always translate into lower maintenance costs, in particular if the maintenance contract does not scale with the number of tools. In other cases even if half as many lots are measured, the tool must always remain on to prevent performance fluctuations. Even though measurement rates may be half of what they were before, consumables and spare parts related to the number of on-hours rather than the number of measurement-hours will be the same. For these reasons, it is very important to involve the individual engineering tool owners and ask the questions, what savings do you expect if we reduce inspection rates by, for example, 50%? What costs do you expect we will incur if we increase measurement rates by, for example, 50%?

Although there is considerable evidence suggesting that lower inspection rates lead to shorter cycle times, lower WIP levels and higher yields, in the interest of both conservatism and simplicity we have suggested that only labor and variable measurement

costs should be included in the net inspection cost parameter. In addition, because of the complexity of determining if measurement rate decreases will result in actual tool savings, we have suggested that the potential benefits of fewer inspection tools should be excluded for now. With some additional work, the net benefit of higher yields, shorter cycle times, lower WIP levels and fewer inspection tools could be quantified and added to the MOST/2 model to provide additional benefit to Intel.

6.4.2 Wafer Value Depends on the Business Environment

Although Intel's accounting system tracks the different fab cost components such as depreciation; payroll; gases and chemicals; maintenance contracts; direct materials; and masks on an aggregate level, product level costs are typically not determined. Moreover, a wafer's value depends not only on the costs required to produce it but also on the value it will generate for Intel when it is sold. For these reasons, it is usually rather difficult to determine the true economic value of a wafer for a particular product. In general, the choice of whether to use the variable cost of the wafer or some other value should depend on what the true economic impact is to Intel if a wafer lot fails to yield as many die as expected because of an excursion in the process. The next section explores the question of how to determine the potential for customer impact in greater detail.

6.4.3 Determining the Potential for Customer Impact

To determine the potential for customer impact due to higher skip rates, we must consider what happens when higher skip rates decrease the number of good die expected at the end of the line.

For many products, there is an end-of-line finished goods buffer. Provided that the lower die yield does not consume this buffer, there is no potential customer impact. In this case, the economic impact to Intel is the incremental or variable cost to replace the lost die by introducing more wafers and or by accelerating the WIP to maintain the buffer. For this to be true, however, we have implicitly assumed that there is sufficient manufacturing capacity to run additional wafer lots. In general, this is a safe assumption since some burst capacity is reserved in the planning of fab tools and processes and since most products are regularly started in the fab.

However, for low-volume products that are only started in the fab periodically, the risk is much greater. For these products, it is possible for a fab excursion to impact a significant proportion of the planned production. Moreover, if an excursion occurs and is not detected until the end of the line, a significant length of time could elapse before replacement wafer lots could be fabricated. For these reasons, either the inspection plans or the buffer strategy for low-volume products needs to be balanced with the risk of potential customer impacts.

If we expect the loss in die to consume the finished goods buffer, Intel may lose more than just the cost of the wafers: Intel may lose sales revenue.[48] Moreover, if the product is bundled with other components as in the case of support chips for microprocessors, the economic impact would be the loss of the bundled sale.

6.4.3.1 A Simple Model for Customer Impact

As the preceding discussion suggests, determining the potential customer and economic impacts of an excursion depends on the number of die that would be lost, the amount and placement of WIP and buffer inventory, the demand for the product and the sales value lost or incremental production costs expended by Intel to recover from the excursion.

The difficulty of taking into account all of these factors on an ongoing basis is a good example of some of the added complexities of operating in the HMLV environment. Although a more complicated automated model is suggested in the next section, a relatively simple model can be used to account for the complex cost and risk balance that must be found to optimize in-process metrology rates.

As described earlier, to effectively balance cost and risk in the optimization of in-line metrology rates, the characteristics of individual products or product groups must be considered. One size does not fit all. For products with different excursion risks, for example, we suggest that several product groups be created with similar excursion risks and that the product group should use the risk factor associated with the most risky product within the group. The basic concept of using the most conservative characteristic within each group should be extended to other factors as well.

A simple way to manage the complexity for multiple factors is to rank the products based on their risk characteristics and to aggregate products with similar risk characteristics into product groups. With the help of a product planner, it is a relatively straightforward exercise to build a weighted model for the characteristics shown in Table 6. Although not optimal, this process provides a relatively simple and straightforward way to accurately capture the true risks of higher skip rates for different products and customers.

[48] This assumes that the demand for the product is perishable. That is, that the absence of a particular product causes the buyer to cancel their order or to switch to another item. Depending on the product and customer, the assumption that the demand is perishable may or may not hold. In the interest of conservatism, however, we proceed with the assumption that all demand is perishable.

Key Product Characteristics	Factors to Consider
Strategic / Sole Source	Is product strategic, sole source or a new product introduction?
Yield / Excursion Risks	Historic yield and excursion rates
Wafer Values	Sales value, bundling, other dependencies
Product Volumes	High/low volume product, start strategy
Finished Goods Inventory	Size of current end-of-line inventory
Demand and Demand Variability	Historic demand and demand changes, cyclicality, current product life cycle stage, demand outlook
Time to Replace	WIP positions, inventory consumption and replenishment rates, process step

Table 6: Key Product Characteristics and Factors to Consider for Product Aggregation Groups

6.4.3.2 Automating the Decision Making Process

To reduce the complexity of managing different product risks and wafer values in the dynamic HMLV fab environment, however, we suggest that an automated tool should be developed to replace the frequent manual intervention that would otherwise be required. Although periodic review of some of the more qualitative factors would still be required, such a system would eliminate much of the work and subjective judgments necessary.

The basic process steps required to automate the process are relatively uncomplicated. For each metrology operation, use the yield and excursion risks to determine the expected number of die lost as a function of the skip rate, product volume and lot sequencing rules at that particular process step. Next, create an end-of-line inventory position chart over the excursion recovery period based on the WIP and buffer positions, the cycle times and the demand consumption rates. Finally, use the appropriate wafer value for the MOST/2 wafer value input parameter based on the minimum inventory position during the recovery period.

6.4.4 The Impact of Rework Loops

Up to this point we have ignored the impact of rework loops. Briefly summarized, for rework loops we must balance the added processing and inspection costs with the expected reduction in lost die at the end of the line. The probability model and basic framework discussed can be used for process steps with rework loops with the addition of parameters for the added inspection and lowered expected excursion costs. In general, since the added costs of rework are less than the end-of-line value of the chips saved, it makes sense to use skip rates no larger than the material that can be contained and reworked if an OOD lot is discovered. The decision of whether or not to rework OOC lots is more complicated. In general, if the control limits are well within the disposition limits and the excursion risk is low, it is better not to rework an OOC lot.

6.5 Balancing Cost and Material at Risk

In the first four sections of this chapter, we outlined a basic method for calculating the MAR as a function of skip rate based on the relevant economics of the HMLV environment and metrology process being optimized. In order to accurately capture the uncertainty in the input parameters, MOST/2 utilizes a Monte-Carlo type simulation tool. To allow users to actively balance the cost savings and risks of higher skip rates, MOST/2 provides a plot of the total expected annual process cost as a function of the skip rate.[49] In order to accurately capture the uncertainty in the output values due to the distributions of the input parameters, MOST/2 provides not only the expected cost versus risk curve, but also the curves corresponding to the upper and lower 2.5th percentiles of the output distributions.[50]

6.6 MOST/2: Putting it All Together

Table 7, Equation 8 and Equation 9 summarize the MOST/2 inspection cost parameters and equations. Table 8 shows the MOST/2 model input distribution parameters and variables. And, Equation 10, Equation 11 and Equation 12 show the economic calculations for the annual inspection cost, annual excursion cost and total annual cost as a function of T, respectively.

Before jumping into the details, it is worth noting that although the tables and equations in this section demonstrate the use of the MOST/2 model for a typical CD-SEM FCCD metrology operation, the basic framework can still be used for other operations: regardless of the industry. The model is most easily adapted for operations that currently employ in-line skip-lot sampling with full inspection at the end of the process. However, even if these conditions are not met, the basic analytical framework still applies. But, it is critical to first ensure that decreased measurement rates do not compromise customer quality. In addition, care should be exercised to insure that all the relevant economics of the decision are captured in the framework of the analysis.

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[49] Since the skip rate is directly proportional to the MAR and is almost equivalent for metrology tools with high *PtD* and low excursion risk values, these curves provide cost versus risk information. This allows users to actively evaluate the tradeoff.

[50] Actually, the curves corresponding to the lower 2.5th and upper 97.5th distribution parameter percentiles are provided for the output excursion slope, excursion intercept, and sample cost parameters. Combining the curves for each parameter percentile value then allows us to create the family of cost versus skip rate curves shown in the figure.

Parameters	Data Sources	Equations and Comments	Variable
Direct Labor Cost per Year	Finance	This should be the fully burdened cost expected for the next year. Historic values are a good proxy.	C_L
Variable Cost per Year	Finance	Include variable spare, warranty or other operating costs per year.	C_V
Actual Skip	Historic data	Note, measure rate is 1 / Skip Rate = #through_metro / #through_link. Use a recent historic value.	S_{Act}
Number of Measurement Operations	Process flow for product group	Some product groups return to the same metrology tool multiple times. This input parameter insures that the cost per measurement correctly accounts for re-entrant flows.	N_{Op}
Direct Labor HC per Year	Manufacturing supervisor and metrology tool cycle times	Allocate the number of operators assigned to all metrology operations by product group volume through the metology operation being analyzed. Verify labor hours match the product of the cycle time and product group volume.	HC
Wafers per Lot	Historic data	Use the average wafers per lot over the same period used to calculate Actual Skip.	N_{wpl}
Lots per Year	Historic data	Use the number of lots run in the past year.	N_{Lh}

Table 7: MOST/2 Lot Sampling Cost Worksheet

Equation 8, below, shows the inspection or sampling cost per metrology move. In this equation, C_L is the fully burdened cost per inspector per year, HC is the average number of inspectors per year, C_V is the total variable processing cost per year, R_M is the metrology move rate and C_M is the inspection cost per metrology move.

$$C_M = \frac{C_L \bullet HC + C_V}{R_M}$$

Equation 8: The MOST/2 Inspection or Sampling Cost Equation

R_M is calculated as shown in Equation 9 where N_L is the number of lots per year, N_{Op} is the number of different measurement operations that use the inspection tool being optimized and S_{Act} is the actual aggregate skip rate for the measurement period.

$$R_M = \frac{N_{Lh} \bullet N_{Op}}{S_{Act}}$$

Equation 9: The Metrology Move Rate Equation

Parameters	Data Source and Distribution Information	Equations and Comments	Variable
OOC Ratio	Adjusted historic data, use actual distribution or histogram data.	#OOC / #through_metro. Count multiple OOCs caused by a single problem only once. If the problem has been eliminated, do not count the event.	P_{OOC}
OOC Yield Impact Ratio	Adjusted historic data, use actual distribution or histogram data.	#OOC_yield_impacts / #OOC. Should be smaller than #OOD / #OOC.	P_{YI}
Excursion Probability	See excursion probability worksheet.	#OOD / #through_link. Alternatively, #out_of_spec / #through_link OR #yield_impacts / # through_link.	P_E
Die Kill Ratio	Adjusted historic data, use actual distribution or histogram data.	#die_lost / #typically_good. Die lost should be strictly due to the excursion at the evaluation layer. Use an accurate die out estimate from the same products for the same time period.	P_{DK}
Actual Skip	Historic data, use actual distribution or histogram data.	#through_link / #through_metro.	S_{Act}
Power to Detect	Use engineering judgment and tool capability data.	Estimate probability of detection from measurement system gauge capability and typical excursion characteristics.	PtD
Wafer Value	Use the customer impact tool.	Adjust for the capacity or demand constrained environment and other product group specific conditions.	C_W
Wafers per Lot	Historic data, use average wafers per lot over the analysis period.	Include rework and other split lots.	N_{wpl}
Lots per Year	Use a one year volume estimate.	Include re-entrant flows.	N_L
Lot Sampling Cost	See lot sampling cost worksheet.	This is the inspection or sampling cost value calculated in the sampling cost worksheet.	C_M

Table 8: MOST/2 Model Input Parameters

Now that we have a value for the lot sampling cost, we can calculate the annual inspection cost. Noting that T is both the inspection group size and the ratio of lots per metrology move, the annual inspection cost as a function of T is shown in Equation 10.

$$Annual\_Inspection\_Cost = \frac{C_M \bullet N_L}{T}.$$

Equation 10: The MOST/2 Annual Inspection Cost

If we substitute $k = C_W \bullet N_{wpl} \bullet P_{DK} \bullet N_L \bullet P(A)$, $P(A) = \max\left(P_E, \frac{P_{OOC} \bullet P_{YI}}{S_{Act}}\right)$, and $Arl = \frac{1 - PtD}{Ptd}$ where Arl is the average run length, the annual excursion cost as a function of T can be developed as shown in Equation 11.[51]

$$Annual\_Excursion\_Cost = T\left(\frac{k}{2} + k \bullet Arl\right) + \frac{k}{2}$$

Equation 11: The MOST/2 Annual Excursion Cost

Summing these two equations, we can now calculate the total annual cost as a function of T. Note that the excursion cost is linear with T and that the inspection or sampling cost varies inversely with T.

$$Total\_Annual\_Cost = \left(T\left(\frac{k}{2} + k \bullet Arl\right) + \frac{k}{2}\right) + \left(\frac{C_M \bullet N_L}{T}\right)$$

Equation 12: MOST/2 Total Annual Cost for a Typical CD-SEM FCCD Operation

6.6.1 Some Examples

As the tables and calculations in the preceding section show, with only a few input variables, worksheets, and equations, MOST/2 provides total annual cost curves as a function of the skip rate or skip group size. In this section, we provide a disguised example of the input parameters and their distributions, simulated output parameter distributions,[52] and cost versus skip rate curves.

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[51] In most cases, *P(A)* is calculated from the second term in the expression, $P(A) = \max\left(P_E, \frac{P_{OOC} \bullet P_{YI}}{S_{Act}}\right)$. In Equation 11 and the rest of the thesis, this is assumed to be the case. However, if a better estimate of the true excursion risk, P_E, is available, it should be used in place of the estimate derived from the probability of out-of-control and yield-impacting events and the actual skip rate. If there is uncertainty about which estimate is better, the conservative assumption is to use the larger of these two terms.

[52] The simulation package shown in the captions is Crystal Ball Professional Academic Edition (v5.5) made by Decisioneering, Inc. More information can be found at www.crystalball.com.

Parameters	Model Input (lot based)	Distribution Information				Variable
		Mean, E(x)	Std Dev	Min	Max	
OOC Ratio	% of OOCs (0 to 100)	0.25	0.06	0	0.5	P_{OOC}
OOC Yield Impact Ratio	% of OOCs that impact yield (0 to 100)	0.2	0.05	0	0.4	P_{YI}
Die Kill Ratio	% of die killed per wafer per excursion (0 to 100)	30	7.50	0	60	P_{DK}
Actual Skip	Actual skip rate (1 in N lots)	4	0.00	4	4	S_{Act}
Power to Detect	Power to Detect an Excursion (0 to 1)	0.95	0.01	0.9	1	PtD
Wafer Value	Wafer Value ($)	----	--	---	----	C_W
Lot Sampling Cost	Lot Sampling Cost ($)	1	0.01	0.95	1.05	C_M
Wafers per Lot	Wafers per Lot	25	0.25	23	25	N_{wpl}
Lots per Year	Lots per Year	10000	125.00	9500	10500	N_L

Table 9: Hypothetical Input Parameters for a Typical CD-SEM FCCD Operation

Figure 12 and Figure 13 provide examples of how these input parameter distributions are modeled by MOST/2 using Crystal Ball. Although only a normal distribution for the *OOC_ratio* parameter and a uniform distribution for the *Wafer_value* parameter are shown, the simulation tool allows engineers to use actual data to define the distributions or to create their own.

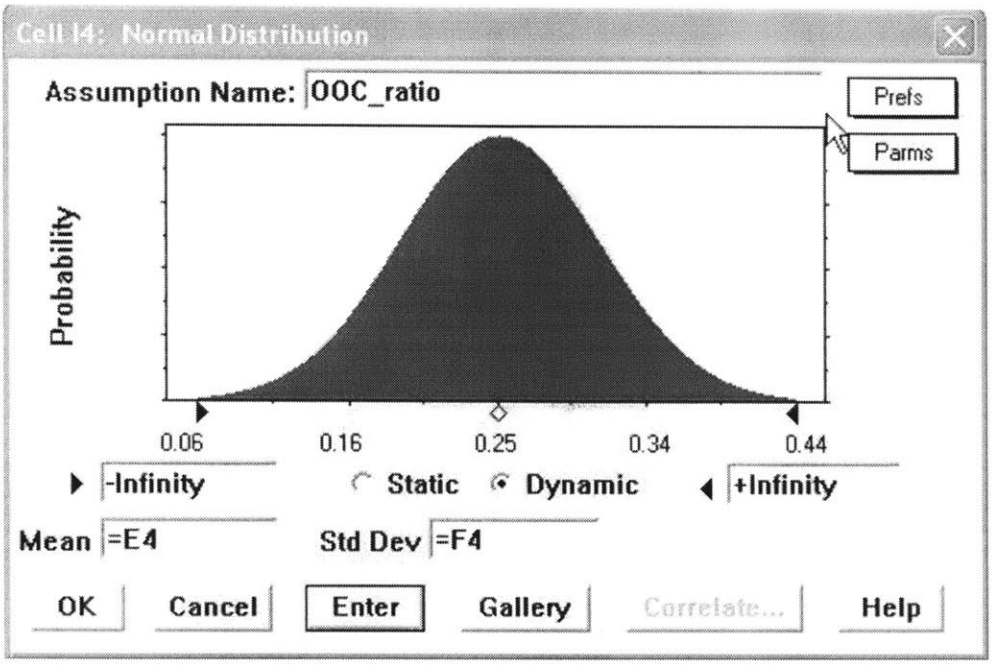

Figure 12: Example of MOST/2 *OOC_ratio* Input Distribution

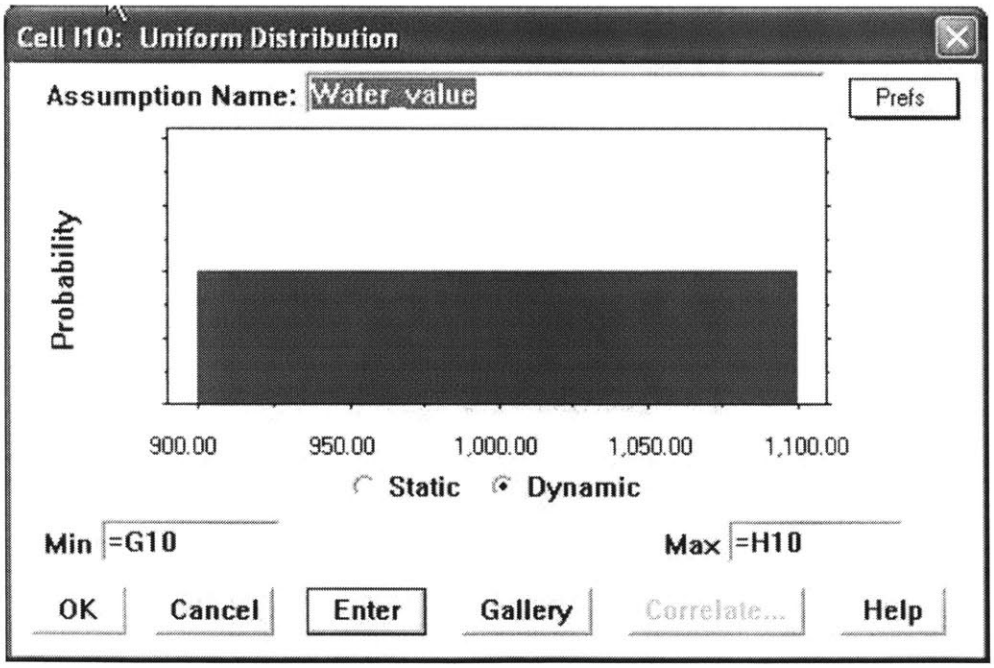

Figure 13: Example of MOST/2 *Wafer_value* Input Distribution

Figure 14 shows the output parameter distributions that result from the input parameters and distribution types listed in Table 9. The minimum cost sample group or *minrate*[53] is shown in the upper left. The other distributions shown are for the inspection cost parameter in the lower left (labeled sampling cost parameter in the figure), the excursion slope parameter in the upper right and the excursion intercept

[53] *minrate* cooresponds to T_{min} in Equation 13, below.

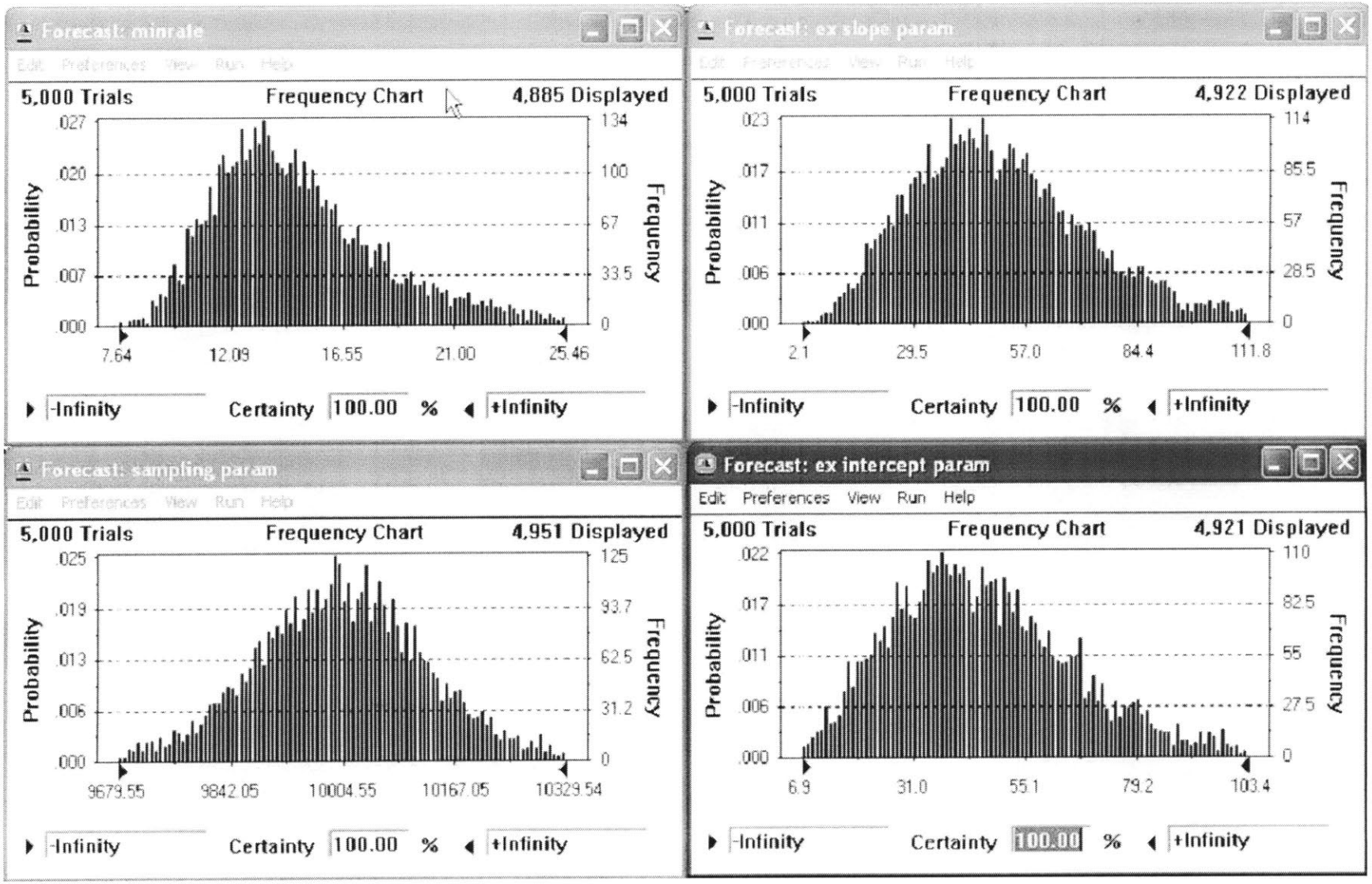

Figure 14: Example of MOST/2 Output Parameter Distributions

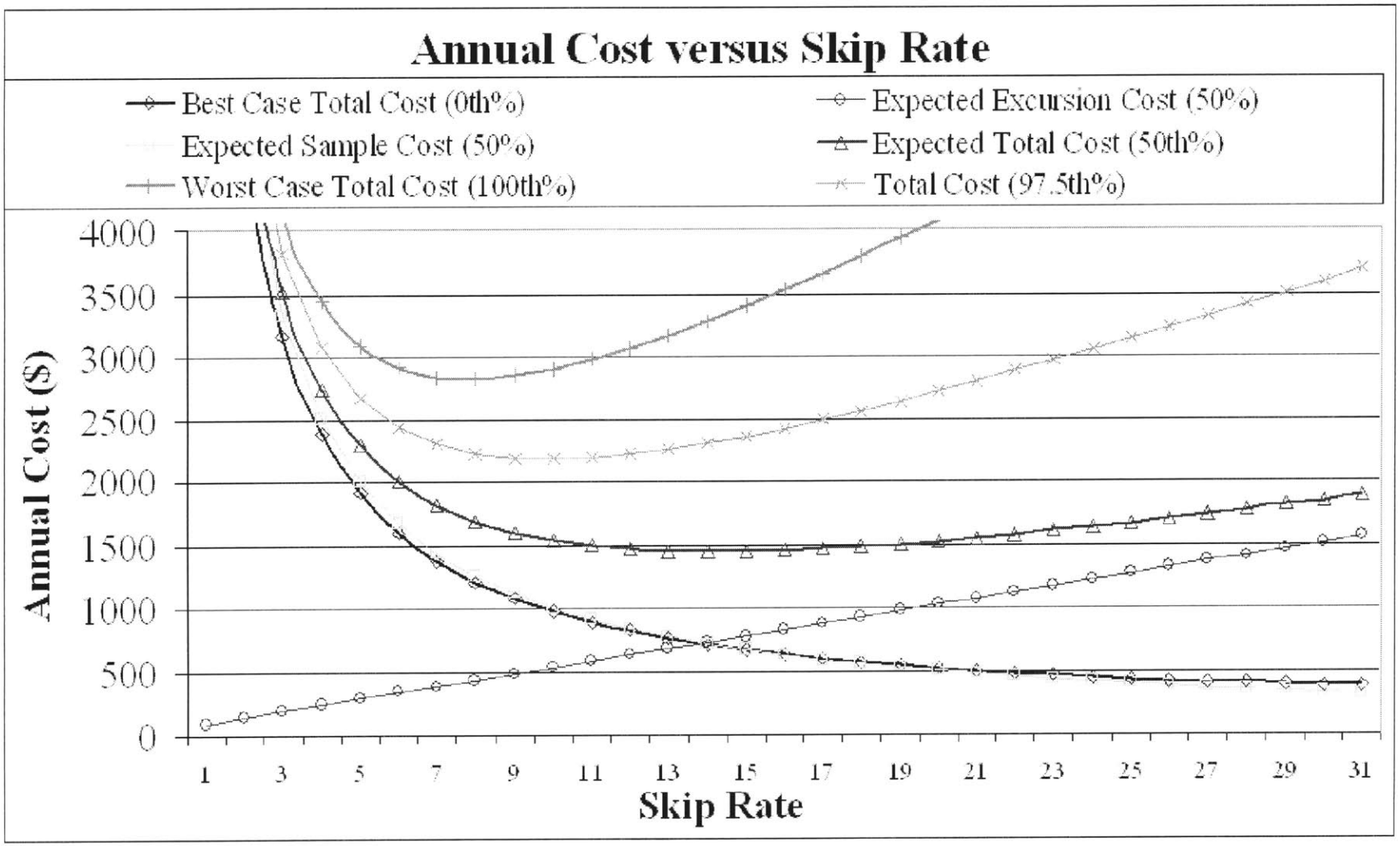

Figure 15: Annual Total Cost versus Skip Rate Curves for a Hypothetical CD-SEM FCCD Operation

parameter in the lower right.[54] As the *minrate* distribution indicates, for the input parameters shown the cost minimizing skip group size ranges from a low of about 7 to a high of about 26 with a median around 14.

While the distribution information is helpful, it does not distill the information into a format that allows the user to easily determine the skip rate that best balances the possible cost savings with the amount of MAR given the variations in input and output parameters.

Using Figure 15, however, it is a relatively straightforward exercise to choose an optimum cost/risk solution based on the user's risk preference. The line with the circle icons shows how the expected excursion cost increases with increased skip rates. As indicated by the 50^{th} percentile notation in the title block, the line is generated from the median output parameter excursion distribution. Likewise, the line with the square icons shows how the expected sampling cost decreases with increased skip rates. The line with the triangle icons is the sum of these first two curves and shows the expected total cost curve for this metrology operation. As can be observed, the lowest total cost solution of about $1400 per year occurs at a skip rate of approximately 14.

The remaining lines are also total cost curves. The curve with the plus icons represents the worst-case total cost curve. It is generated by setting the input parameters to their least favorable values. For the worst-case total cost curve, the minimum value of about $2800 per year occurs at a skip rate of approximately eight. Regardless of the user or organizations' risk preferences, Figure 15 provides the information required to make an intelligent cost and risk tradeoff. For example, perhaps an intermediate solution makes more sense such as the 97.5^{th} percentile of the output distributions. In this case if the user looks at the curve with the "X" icons, she will find that the lowest cost solution occurs at about $2200 per year with a skip rate of approximately ten.

6.6.2 A Sensitivity Analysis

As discussed previously and summarized in Equation 11, for $P(A) \approx 0$, the excursion cost formula is linear in T. In addition, as shown in Equation 10, the inspection or sampling cost varies with the inverse of T. Since the total annual cost is the sum of these two functions, it is a straightforward exercise to take the derivate of the total cost formula and set it equal to zero. If we then solve for T, we can determine the cost minimizing value for the skip group size as a function of the expected input variables. Equation 13 shows the result.

[54] The inspection cost, excursion slope, and excursion intercept parameters correspond with $C_M \bullet N_L$, $\left(\frac{k}{2} + \frac{k(1-PtD)}{PtD}\right)$, and $\frac{k}{2}$ from Equation 12, respectively.

$$T_{\min} = \sqrt{\frac{C_M \bullet S_{Act}}{C_W \bullet N_{wpl} \bullet P_{DK} \bullet P_{OOC} \bullet P_{YI} \bullet \left(\frac{1}{2} + \frac{1-PtD}{PtD}\right)}}$$

Equation 13: The Cost Minimizing Inspection Group Size

If we want to determine the model's sensitivity to the input parameters, we need only take the partial derivative of this equation with respect to the input parameter of interest. Since the minimum cost skip group size depends on so many factors, analyzing the model sensitivities is an important step to determine where the most time and energy should be spent to accurately determine the input parameters and their distributions. The figure below shows sensitivity formulas for each of the input parameters. The actual sensitivity values for the input parameters discussed in the preceding example are included in the figure for reference. Two values are shown for each input. The value on the left is $\frac{\partial T_{\min}}{\partial X_i}$ and the value on the right is $\frac{\partial T_{\min}}{\partial X_i} \bullet \Delta X_i$. Multiplying the sensitivity term by an estimate of the one-sigma standard deviation of the input variable, ΔX_i, provides a more realistic estimate of the sensitivity of the input variable.

There are several interesting things to note about the sensitivity values shown on the right side of Figure 16 for our hypothetical CD-SEM FCCD operation. The most sensitive terms for this operation are P_{DK}, P_{OOC}, and P_{YI}. All three terms are equally sensitive and are four orders of magnitude more sensitive than the others. So, considerable time should be spent to validate these parameters and their distributions.

The signs of each of each of the different sensitivity terms in Figure 16 are also noteworthy because they indicate how each term qualitatively affects the cost optimal skip rate, $T_{\min}$. For example, as C_M, S_{Act} or PtD increase, the cost optimal skip rate also increases. Alternatively, as P_{DK}, P_{OOC}, P_{YI} or C_W increase, the cost optimal skip rate decreases. Both results make intuitive sense.

Sensitivity Analysis Equations	$\frac{\partial T_{min}}{\partial X_i}$	$\frac{\partial T_{min}}{\partial X_i} \bullet \Delta X_i$
$\frac{\partial T_{min}}{\partial C_M} = \frac{1}{2} \bullet \sqrt{\frac{S_{Act}}{C_M \bullet C_W \bullet N_{wpl} \bullet P_{DK} \bullet P_{OOC} \bullet P_{YI} \bullet \left(\frac{1}{2} + \frac{1 - PtD}{PtD}\right)}}$	6.95	0.09
$\frac{\partial T_{min}}{\partial S_{Act}} = \frac{1}{2} \bullet \sqrt{\frac{C_M}{S_{Act} \bullet C_W \bullet N_{wpl} \bullet P_{DK} \bullet P_{OOC} \bullet P_{YI} \bullet \left(\frac{1}{2} + \frac{1 - PtD}{PtD}\right)}}$	1.74	0.00
$\frac{\partial T_{min}}{\partial C_W} = -\frac{1}{2} \bullet \sqrt{\frac{C_M \bullet S_{Act}}{C_W^{\,3} \bullet N_{wpl} \bullet P_{DK} \bullet P_{OOC} \bullet P_{YI} \bullet \left(\frac{1}{2} + \frac{1 - PtD}{PtD}\right)}}$	-0.01	-0.17
$\frac{\partial T_{min}}{\partial P_{DK}} = -\frac{1}{2} \bullet \sqrt{\frac{C_M \bullet S_{Act}}{P_{DK}^{\,3} \bullet C_W \bullet N_{wpl} \bullet P_{OOC} \bullet P_{YI} \bullet \left(\frac{1}{2} + \frac{1 - PtD}{PtD}\right)}}$	-23.16	-173.66
$\frac{\partial T_{min}}{\partial P_{OOC}} = -\frac{1}{2} \bullet \sqrt{\frac{C_M \bullet S_{Act}}{P_{OOC}^{\,3} \bullet C_W \bullet N_{wpl} \bullet P_{DK} \bullet P_{YI} \bullet \left(\frac{1}{2} + \frac{1 - PtD}{PtD}\right)}}$	-2778.60	-173.66
$\frac{\partial T_{min}}{\partial P_{YI}} = -\frac{1}{2} \bullet \sqrt{\frac{C_M \bullet S_{Act}}{P_{YI}^{\,3} \bullet C_W \bullet N_{wpl} \bullet P_{DK} \bullet P_{OOC} \bullet \left(\frac{1}{2} + \frac{1 - PtD}{PtD}\right)}}$	-3473.25	-173.66
$\frac{\partial T_{min}}{\partial PtD} = \frac{1}{2} \bullet \sqrt{\frac{C_M \bullet S_{Act}}{\left(\frac{1}{2} + \frac{1 - PtD}{PtD}\right)^3 \bullet PtD^{\,2} \bullet C_W \bullet N_{wpl} \bullet P_{DK} \bullet P_{OOC} \bullet P_{YI}}}$	13.93	0.17

Figure 16: MOST/2 Sensitivity Equations and Values for Hypothetical CD-SEM FCCD Operation

Chapter 7: A Comparative Analysis of Metrology Inspection Rate Optimization Methods

This chapter compares the metrology inspection rates determined by MOST/2 with the other optimization methods for several different CD-SEM metrology process steps in IFO. Labor and tool hours, annual inspection costs and the expected material at risk values are compared. MOST/2 is shown to provide superior cost/risk balanced results for the HMLV environment.

7.1 Total Inspection Cost and MAR Values for Metrology Inspection Rate Optimization Methods

Twenty-seven CD-SEM metrology inspection operations were analyzed using the basic, MOST and MOST/2 methods based on the generally prevailing IFO operating conditions in the second half of 2003.[55] For the MOST method, the recommended skip rates are used in the analysis. These rates correspond to the medians of the cost-optimal skip rate distributions.

Since MOST/2 allows the user to select the skip rate operating point on the cost versus risk curve, several different skip rates are discussed and depicted for each operation. Data identified as *MOST/2 Rec* refers to the cost optimum skip rate. Data identified as *MOST/2 0.9* refers to a slightly more conservative operating point which captures 90% of the cost savings and has lower risk. In addition, two more MOST/2 operating points are provided for comparison. *MOST/2 (=MOST MAR)*[56] refers to the MOST/2 operating point that has an equivalent amount of MAR as the MOST recommendation. *MOST/2 (=basic MAR)* refers to the MOST/2 operating point that has an equivalent amount of MAR as the basic method.

Figures 17-19 show the change in MAR and total annual inspection cost savings relative to the basic method. The MAR values represent the number of lots that are at risk per excursion for a given operation. The MAR changes are represented by the bar chart and use the left-hand scale. The total annual inspection cost savings represent the sum of the expected excursion and inspection costs saved each year for a given operation. The total annual cost savings are represented by the line chart and use the right-hand scale.

Operations G and H in Figure 17 provide interesting discussion examples. Operation G is an example of an operation with significant excursion risk. Although the MOST method recommends a skip rate which increases the MAR to save money, the MOST/2 method recommends a skip rate that increases the inspection cost to reduce the MAR below both the basic and MOST method operating points. This is a case where neither the basic nor the MOST method is conservative enough. For operation G, the

[55] To maintain Intel's confidential information but still show quantitative differences between the methods, all data has been reported as changes from the basic method in use. Moreover, some operating steps and input conditions that could be surmised have been disguised or modified.
[56] As you may recall, MAR is the amount of material-at-risk should the process go into excursion.

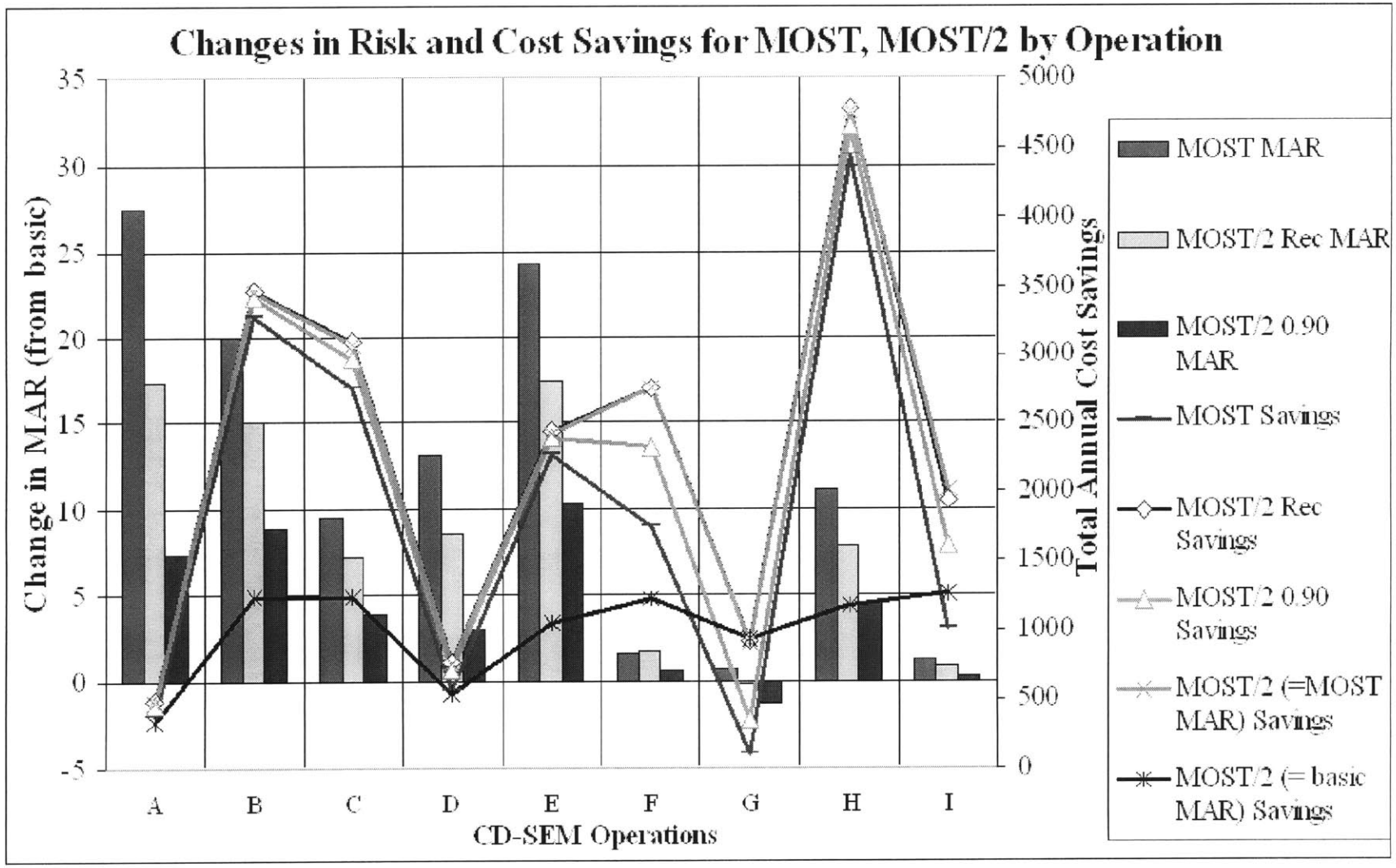

Figure 17: Changes in Risk and Cost Savings for MOST, MOST/2 for Operations A through I

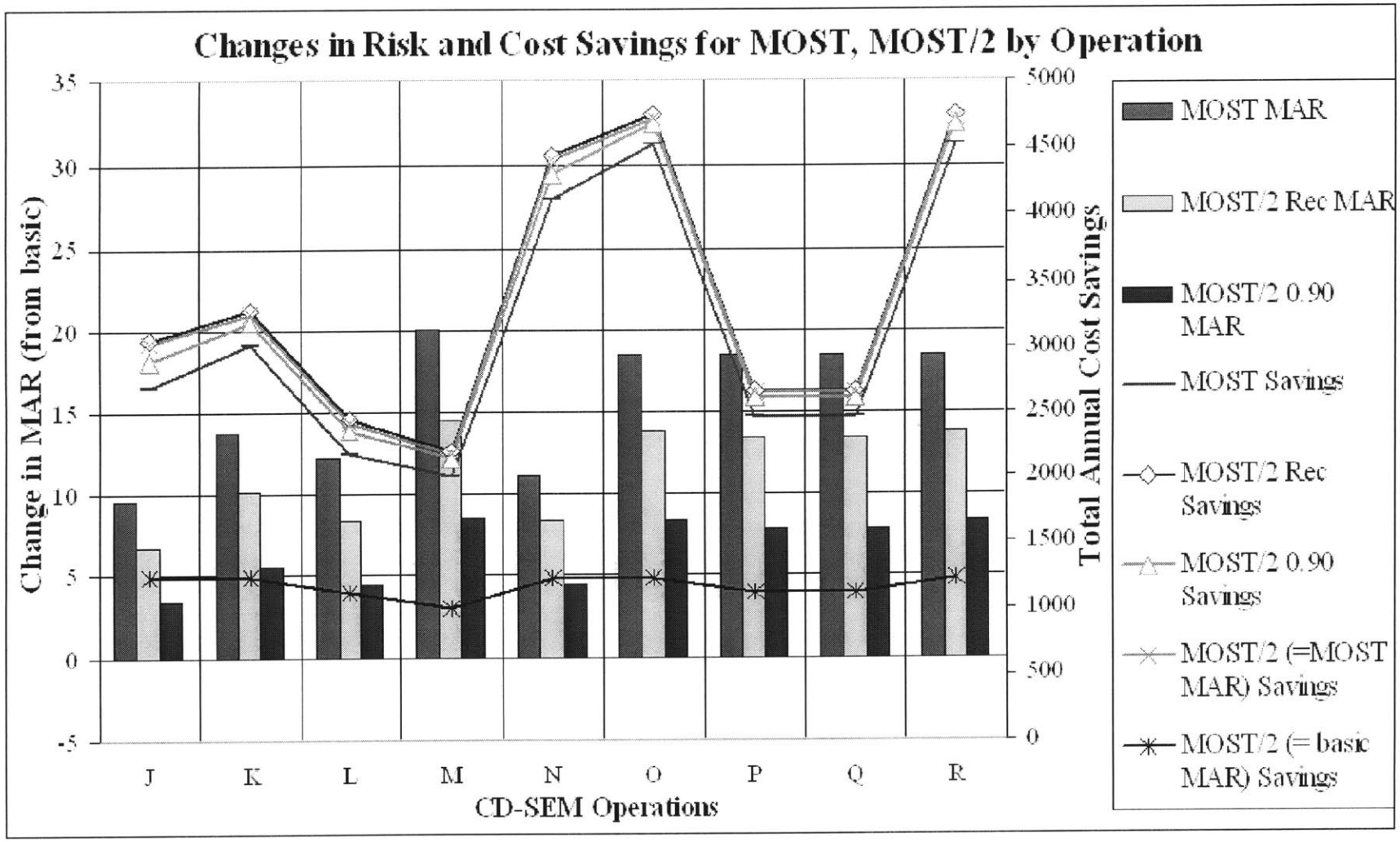

Figure 18:Changes in Risk and Cost Savings for MOST, MOST/2 for Operations J through R

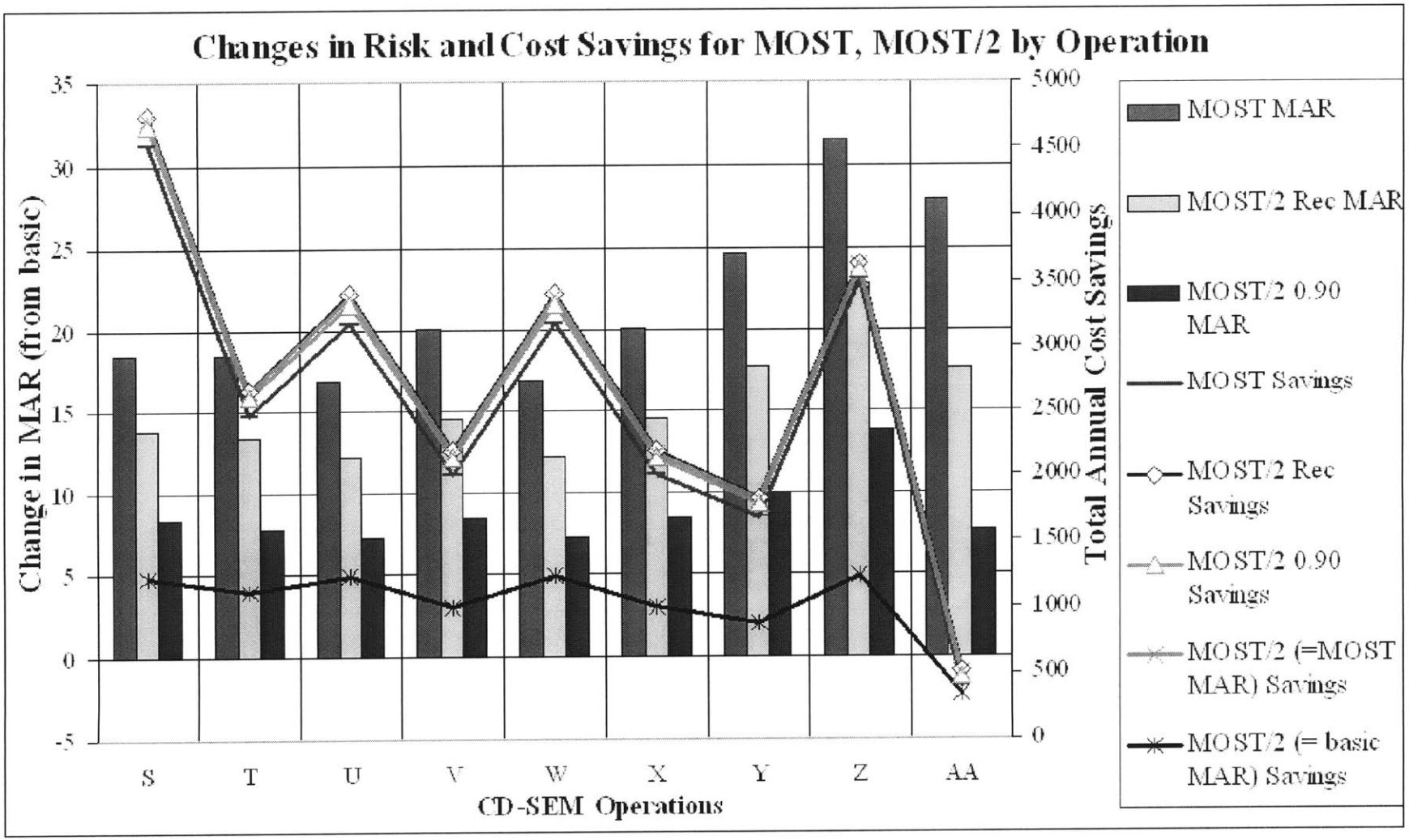

Figure 19: Changes in Risk and Cost Savings for MOST, MOST/2 for Operations S through AA

MOST and MOST/2 models (for all operating points depicted) both provide some cost savings over the basic method. However, the MOST/2 method provides the largest cost savings with equal or lower risk than the other methods.

Operation H is fairly representative of most of the operations analyzed. Roughly 11 more lots are at risk per excursion if the MOST skip rate is used. If the *MOST/2 Rec* skip rate is used instead, three fewer lots are at risk than if the MOST method is used. If the more conservative *MOST/2 0.9* skip rate is used, approximately three fewer lots are at risk than if the *MOST/2 Rec* skip rate is used. The total annual cost savings for the MOST and MOST/2 methods and operating points range from $4800 to $4400. The *MOST/2 Rec* skip rate has the largest cost savings and the MOST recommended skip rate has the smallest savings. If the MOST/2 operating points that correspond to the MOST MAR and basic MAR levels are chosen, the cost savings fall in between the MOST and MOST/2 savings that result from using the recommended skip rates. In short, MOST/2 again provides greater cost savings with lower or equal MAR levels than would result from using either the MOST or the basic method.

There are two key components to the MOST/2 method that allow it to provide superior results. The first is that the probability model more accurately captures the costs and risks of the HMLV environment in its economic analysis. The second is that by properly aggregating products into similar risk groups, the MOST/2 method allows higher skip rates for low-risk products, and lower skip rates for high-risk products. By not treating all products the same, MOST/2 allows reductions in both risk and cost. The analysis and data provided here only show the benefits of the improved probability and economic model. Since product aggregation groups vary by operation, for simplicity, all products have been aggregated into a single group in this analysis to allow a consistent and accurate comparison of the methods. In practice, proper product aggregation allows significant additional cost savings and risk reductions.

7.2 Tool and Labor Hour Savings for Metrology Inspection Rate Optimization Methods

The majority of the total cost savings from the MOST and MOST/2 methods are due to reductions in metrology labor costs. Although savings due to lower tool utilizations and the opportunity to reduce or eliminate CD-SEM tools are not captured in these models, it is possible to estimate the savings based on the reduced tool hours required. Figure 20 and Figure 21 show the annual tool hours saved over the basic method if we just take credit for the average tool time required between when a lot is introduced to the tool and when it is removed from the tool. Since metrology tools are rarely fully utilized, the actual time savings is in fact much larger. Our estimates provide an accurate lower bound.

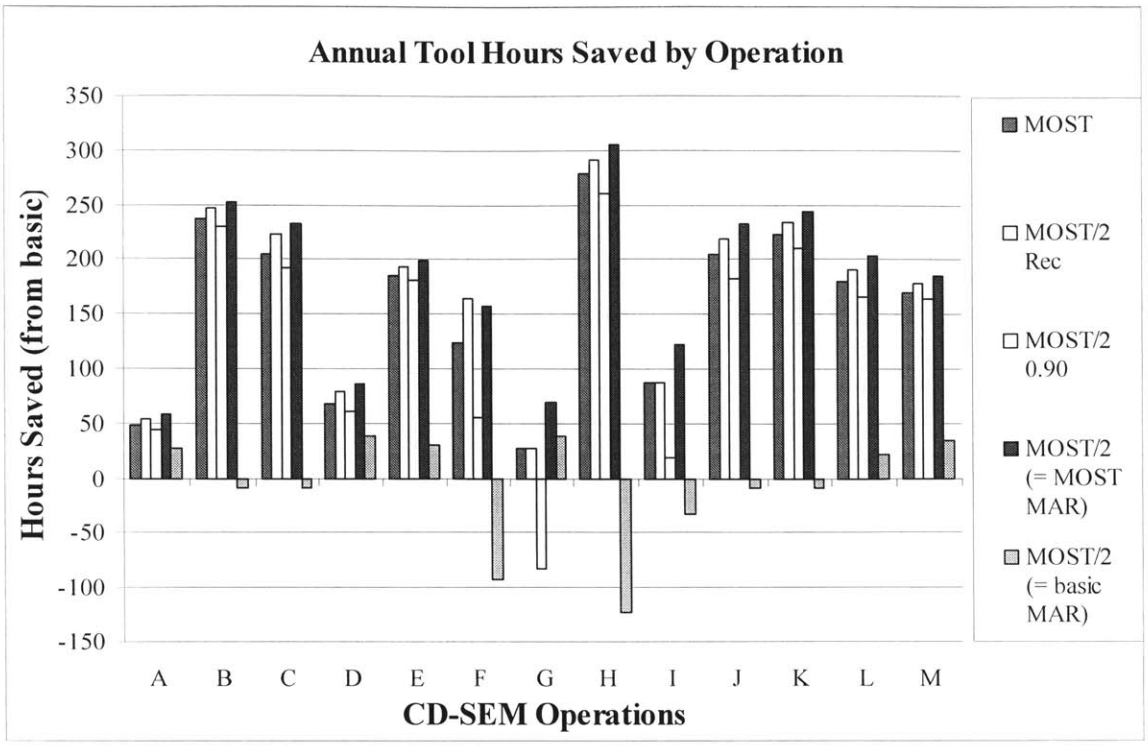

Figure 20: Annual Tool Hours Saved for MOST, MOST/2 for Operations A through M

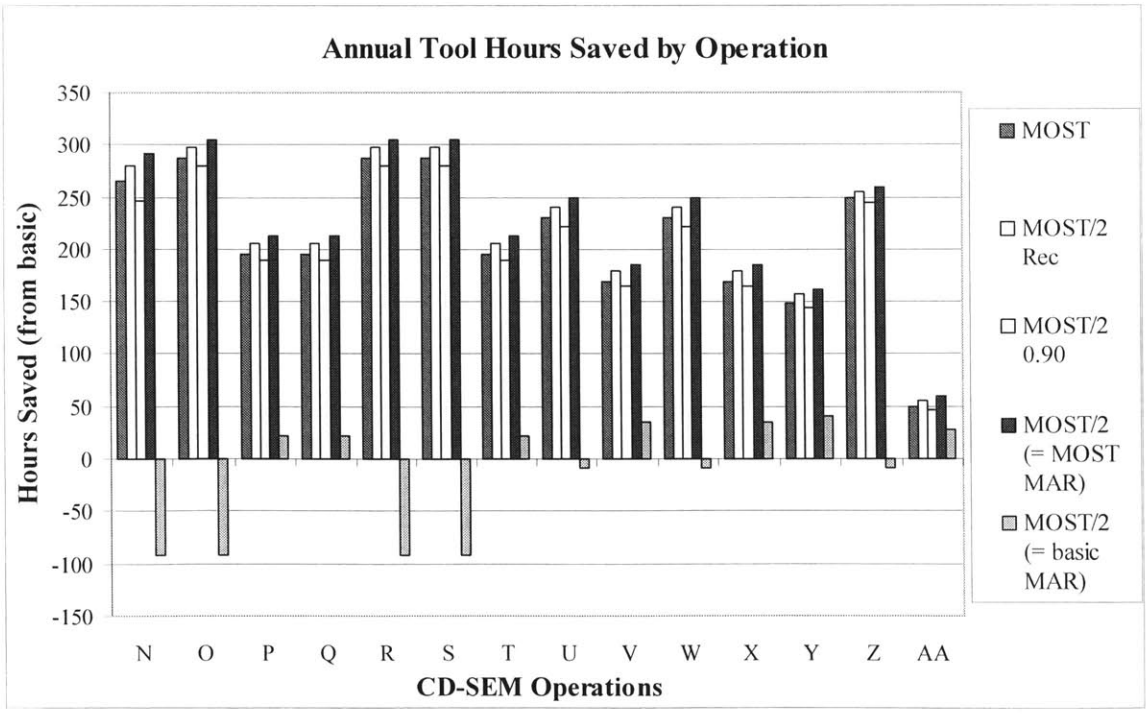

Figure 21: Annual Tool Hours Saved for MOST, MOST/2 for Operations N through AA

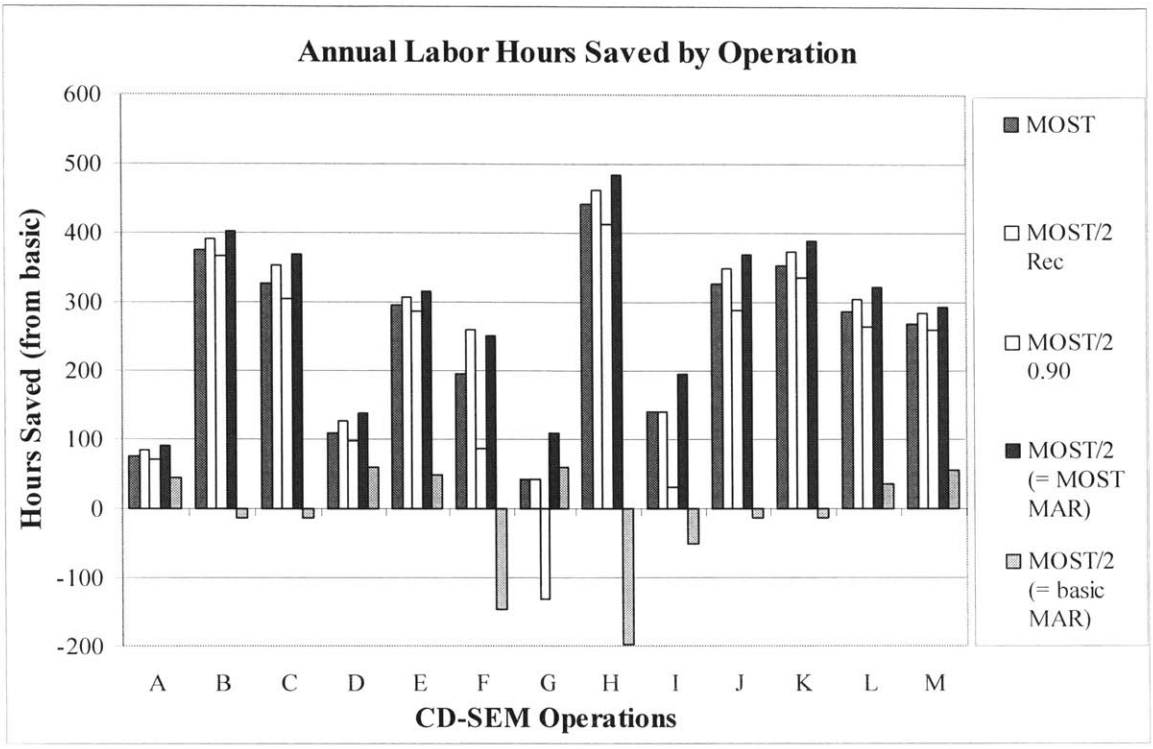

Figure 22: Annual Labor Hours Saved for MOST, MOST/2 for Operations A through M

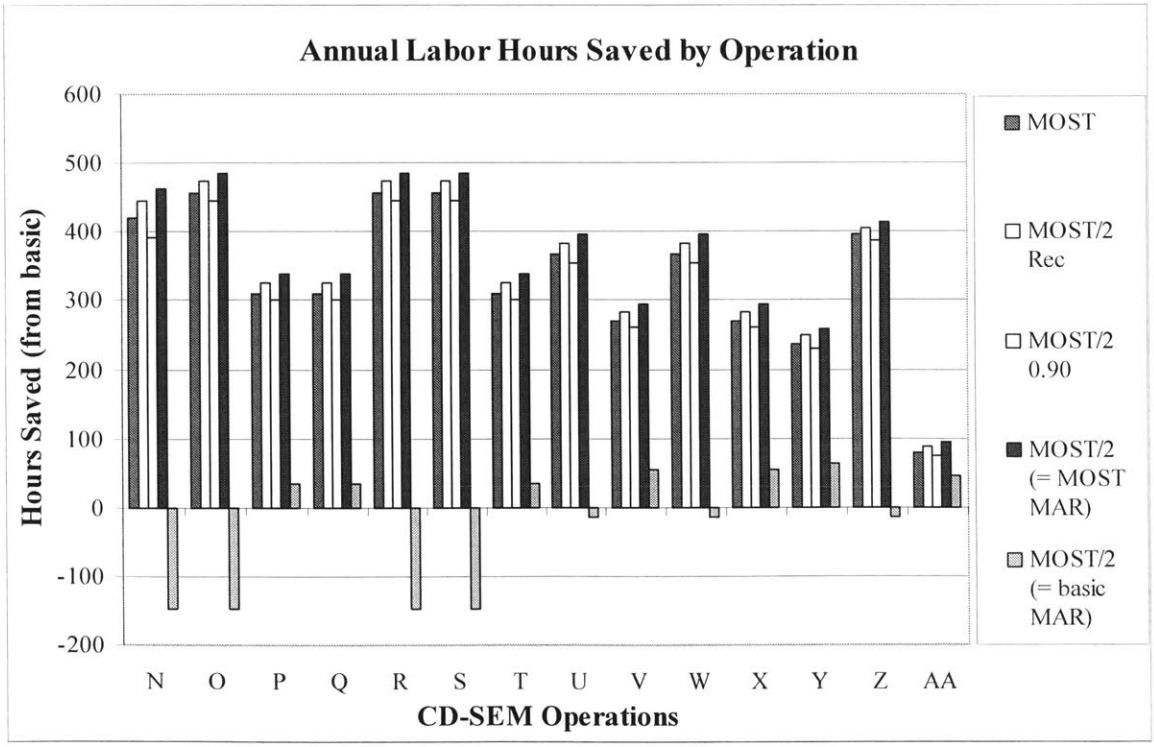

Figure 23: Annual Labor Hours Saved for MOST, MOST/2 for Operations N through AA

Figure 22 and Figure 23 show the annual labor hours saved by operation. The labor hours saved are calculated using the average operator time required for the measurement of each lot and include the logistics time required to introduce each lot to the tool, process the data, and move the lot to the next operation. Queueing time, which can be a significant multiple of the cycle time, is not included in these figures. So, the estimates are again conservative lower bounds of the realizable savings.

7.3 Summary of Metrology Inspection Rate Methods

A comparative summary of the inspection rate optimization methods is presented shortly. In addition to the change in MAR, total inspection and excursion cost, and the tool hour and labor hour savings already discussed, cycle time, tool utilization and holding cost savings are also estimated. The next section provides a brief description of the basic queueing model used to estimate cycle time, holding cost and tool utilization changes for the different inspection rate methods and operating points.

7.3.1 Analysis Methodology for Cycle Time and Holding Cost Estimates

To determine the impact to tool utilization, cycle time and the total inventory time in the system, a basic M/M/k Queueing model was employed.[57] Service rates were estimated from the average per-lot tool measurement times required and are assumed to be exponentially distributed. Arrivals are assumed to be Poisson and the number of tools and their utilization levels are based on historic levels. The calculation equations are summarized below.

[57] M/M/k is the notation used to signify that the queueing model assumes that arrivals are Poisson and service times are exponentially distributed. The k reflects the actual number of tools that process the WIP. The assumptions are fairly standard and conservative. For more information see:
Spearman, Mark L. and Wallace J. Hopp. Factory Physics. 2nd Edition. McGraw Hill. Boston (2000). pp. 264-283.

M/M/k Equations

λ = the mean arrival rate of the system
μ = the mean service rate per tool
k = the number of tools
n = number of units in the system
ρ = the capacity utilization, $\rho = \frac{\lambda}{k\mu}$
CoC = cost of capital = 20% per year

Probability that there are no units in the system:

$$P_0 = \frac{1}{\sum_{n=0}^{k-1} \frac{\left(\frac{\lambda}{\mu}\right)^n}{n!} + \frac{\left(\frac{\lambda}{\mu}\right)^k}{k!} \bullet \frac{k\mu}{k\mu - \lambda}}$$

The average number of lots in the waiting line:

$$L_q = \frac{\left(\frac{\lambda}{\mu}\right)^k \bullet \lambda\mu}{(k-1)! \bullet (k\mu - \lambda)^2} \bullet P_0$$

Little's Law: $L_q = \lambda \bullet W_q$ where W_q is the average time in the line.

Average Lots in the system: $L = L_q + \frac{\lambda}{\mu}$

Average time in the system: $W = W_q + \frac{1}{\mu}$

$$Inventory\_Holding\_Cost = C_W \bullet N_{wpl} \bullet CoC$$

$$Average\_Cycle\_Time = \frac{N_L \bullet N_{Op}}{S_{Act}} \bullet \frac{W}{N_L} = \frac{N_{Op} \bullet W}{S_{Act}}$$

Figure 24: M/M/k Queueing Model for Utilization, Cycle Time and Inventory Holding Cost Savings

7.3.2 Comparative Results Summary for MOST and *MOST/2 Rec*, *MOST/2 0.9*, *MOST/2 = MOST MAR* and *MOST/2 = basic MAR*

Table 10 shows the aggregate comparative results of the 27 operations analyzed using the basic, MOST and MOST/2 methods. Although we have neglected the added benefits that result from proper product group definitions, our analysis provides conclusive evidence that MOST/2 is a superior, cost and risk balanced method for determining metrology inspection rates in the HMLV environment. If the MOST/2 recommended skip rates are utilized at the 27 operations analyzed, IFO stands to save well over $100,000 per year with only modest increases in the amount of material at risk. In addition, four operators will be freed to work in other areas and capacity utilization of

the CD-SEM metrology tools will drop by over 67%. Moreover, cycle time will decrease by at least five hours per lot due to the reduced measurements. In addition, the actual cycle time savings are expected to be significantly greater due to reduced queueing at bottleneck lithography operations.

CD-SEM Operation Totals (relative to basic)	**MOST**	**MOST/2 Rec**	**MOST/2 0.9**	**MOST/2 =MOST MAR**	**MOST/2 =basic MAR**
Change in MAR (per excursion)	444	317	175	444	0
Annual Tool Hour Savings	5001	5286	4547	5543	(285)
Reduction in Metro Capacity Utilization	63%	67%	58%	70%	(4%)
Annual Labor Hour Savings	7945	8398	7223	8806	(453)
Annual Operators Saved	4.0	4.2	3.6	4.4	(0.2)
Estimated Cycle Time Savings (hours / lot)	5.3	5.3	5.1	5.4	(1.7)
Annual Cost Savings (Inspection & Excursion Costs)	$67,419	$75,422	$72,342	$74,986	$28,793
Estimated Annual Holding Cost Savings (20% Cost of Capital)	$19,361	$19,682	$18,811	$19,957	($6,195)
Annual Cost Savings (Inspection, Excursion and Holding Costs)	**$86,780**	**$95,104**	**$91,154**	**$94,943**	**$22,598**

Table 10: Comparative Results Summary of MOST, MOST/2 Inspection Rate Optimization Methods

Chapter 8: HMLV Transition Management Implementation Challenges

In this chapter the challenges of transitioning from high-volume manufacturing (HVM) to high-mix, low-volume (HMLV) manufacturing operations, and implementing new tools and processes in the CE![58] environment are analyzed. The strategic design, political, and cultural perspectives as described in Ancona, Kochan, Scully, Van Mannen and Westney's text on *Managing the Future: Organizational Behavior and Processes*[59] are used to structure the analysis.

Unlike the previous and following chapters, in this chapter I use the first person writing tense rather than the third person analytical tense to describe the challenges that I faced and that I perceive may be obstacles to future success. The views expressed are solely my own and, it should be clearly noted, are based on my experiences during a relatively short time at IFO: seven months. This chapter repeats some of the previous material and includes a brief summary of the background and project description so that the analysis can stand on its own. Additional information can be found in the relevant chapters.

8.1 Organizational Processes and the Three Lenses Analytical Framework

The field of organizational behavior has provided many ways to analyze the function of organizations. In this chapter I use one of the common analytical frameworks: a three lenses or three perspectives analysis to provide insight into the HMLV transition management challenge. This approach focuses on a strategic design, political and cultural analysis of the organization. None of the lenses is either right or wrong. They are intended as complements to each other to allow a richer understanding of the different elements that impact an organization and its ability to deal with the internal and external stresses brought about by change.

8.1.1 The Strategic Design Lens

The strategic design perspective focuses on "the flow of tasks and information ... how people are sorted into roles, how these roles are related, and how the organization can be rationally optimized to achieve its goals." Figure 25 shows the basic processes involved in strategic design: assessing how the business and organizational environment relate to the strategic intent, and matching these factors with the organizational design. From the strategic design perspective, core activities include determining how groups should be formed, how they should be linked and how they should be aligned or realigned. From this perspective, some of the reasons behind organizational ineffectiveness include a lack of clarity of goals, ineffective grouping, ineffective linking, lack of internal alignment, and lack of external fit.[60]

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[58] CE! stands for Copy Exactly! It is described in greater detail shortly.
[59] Ancona, Kochan, Scully, Van Maanen and Westney. Managing the Future: Organizational Behavior and Processes. 2nd Edition. South-Western College Publishing. Boston, MA. (1999).
[60] Ibid. pp. M-2: 7, 12-13.

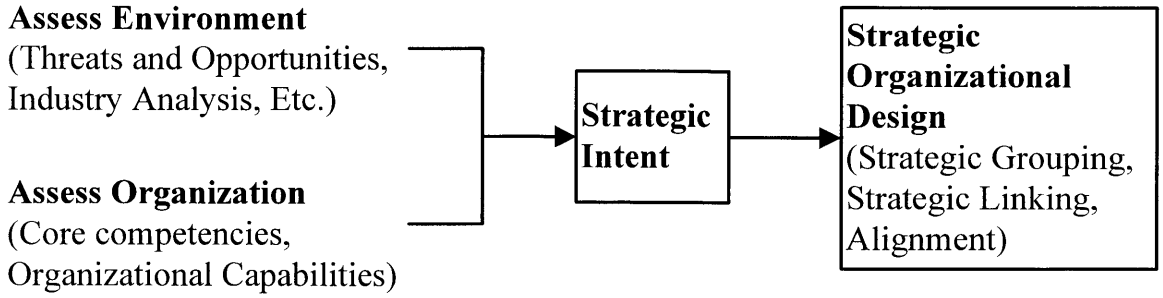

Figure 25: Processes in Strategic Design[61]

8.1.2 The Political Lens

The political perspective focuses on "how power and influence are distributed and wielded, how multiple stakeholders express their different preferences and get involved in (or excluded from) decisions, and how conflicts can be resolved." From the political perspective, core activities include "identifying and mapping the relationships between the different stakeholders; determining the interests and goals of the different stakeholders and the extent to which they conflict or are congruent; and assessing the amount and sources of power of the different stakeholders." The last activity is particularly important because the sources of power are often unclear and include not only formal authority and alliances but also such things as control over scarce resources, control over decision processes, gate-keeping or control over the flow of and access to information, as well as the organization's rules, structure, regulations and standard operating procedures.[62]

8.1.3 The Cultural Lens

The cultural perspective focuses on "how history has shaped the assumptions and meanings of different people, how certain practices take on special meaningfulness and even become rituals, and how stories and other artifacts shape the feel of an organization." It emphasizes "the inherent limitations of managerial authority and influence" and looks to cultural artifacts and rituals as a way to understand how "material (buildings, products, machines) and ideational (e.g., values, norms, ideologies) objects carry and transmit meaning to the people and organizations in which they are used." Although less tangible than the first two lenses, culture has enormous and pervasive impact on both the organization and the overall success of the business.[63]

[61] Ibid. p. M-2: 7.
[62] Ibid. pp. M-2: 8, 40, 43.
[63] Ibid. Figure 2.1 pp. M-2: 13, 64-65.

8.2 Intel and the HMLV Challenge

Over the last ten to fifteen years, three major market developments exerted pressure on Intel's strategy: PC market saturation, performance overshoot and the emergence of the internet. Due in part to these changes, Intel responded by acquiring and adding a significant number of primarily high-mix, low-volume (HMLV) products to its portfolio.

For a number of reasons, Ireland Fab Operations (IFO)[64] was charged with the responsibility for manufacturing more HMLV products than any other factory in the 200/300 mm Wafer Manufacturing Group (WMG) network. Because the factory, tools, systems, organizational processes, and business processes were originally designed and optimized for an HVM environment, the transition from HVM to HMLV operations has not been easy.

8.2.1 IFOs HMLV History

In the second half of 2002, senior plant management commissioned a Management Review Committee (MRC) composed of senior staff members from each of the major functional groups to proactively deal with the coming HMLV challenge. The MRC investigated the issue and identified a number of key tactics and strategies in the following quarters. During this time period, one of the MRC members heard about MIT Sloan's Leaders for Manufacturing (LFM) program and submitted an HMLV internship proposal. To my great pleasure, I was granted the opportunity to assist IFO with its HMLV transition challenge.

With my arrival at the end of the second quarter in 2003, the MRC transferred management responsibility to a working group (WG) composed of first line managers from each of the major functions. Responsibility for chairing the IFO HMLV WG was given to me with the support and sponsorship of one of the MRC staff members. The group's primary goal was to focus on and close any major gaps necessary to achieve the long-range forecasted product mix and volume commitments. An additional goal was to identify and implement high-leverage mid-term and long-term solutions to help the factory achieve Operational Excellence (OpX) in the HMLV environment.

8.2.2 Environmental Complications

When I arrived, several other major activities were underway which affected the overall business environment at Intel Ireland Limited. In addition to the introduction of more HMLV products in the fab, IFO began the qualification and ramp of a new far more sensitive process technology. Around the same time frame, construction of Fab 24, the first 300 mm wafer fab in Ireland, was completed and product ramp and qualification began. This latter activity is particularly important. Because Fab 24 is viewed as "Intel Ireland's future," Fab 24 activities garnered many of the most talented and experienced manufacturing and engineering personnel.

[64] Fabs 10 and 14 are collectively referred to as Ireland Fab Operations or IFO for short.

Primarily as a result of these two activities, there was a shortage of skilled manufacturing and engineering personnel to support the ongoing HMLV transition. And, although these problems were acknowledged by the HMLV MRC, resource and training options were ruled out-of-bounds in the HMLV WG charter: the solutions to these problems were reserved for other forums.

In addition, by the time the IFO HMLV WG was commissioned, several cross-functional task forces were already in place to address IFO metric impacts caused by the training and resource problems as well as the early part of the transition to HMLV production. Unfortunately, because the effects of the HMLV transition were poorly understood by many of the people at IFO, metric impacts were largely ascribed to the first two issues. Consequently, direct involvement of the HMLV team in the task forces was limited or discouraged. The net result was that the HMLV WG primarily focused on anticipated mid-term and long-term HMLV impacts rather than day-to-day factory performance problems, except where there were coverage gaps that did not fit into the existing task force frameworks.

Although in principle this freed the team from many fire-fighting and short-term problems, it also reduced the visibility of the team and diminished the perceived importance of the group's activities. Consequently, it was not surprising when HMLV WG team members failed to meet team commitments on multiple occasions because they had been pulled into the task forces to deal with more pressing, and higher visibility, short-term problems.

8.3 Strategic Design Challenges

Having already touched on the business environment in the preceding sections, analysis of IFOs strategic design continues with an assessment of IFOs organizational design and capabilities, and Intel and IFOs strategic intent.

At the highest level, Intel is organized in a product and business function matrix. Within IFO, people are organized primarily by function but sometimes by function, process technology and even by specific tool sets. As shown in Figure 26, the IFO HMLV WG has informal, indirect links to each of the functional organizations. As discussed shortly, it is worth considering whether this particular organizational strategic design is the most effective way to achieve long-term HMLV OpX at IFO. It is also worth noting that the WG has representation in, and links to the WMG and TMG HMLV teams. Maintaining and strengthening these ties will help to insure ongoing synergy between the HMLV teams.

Almost all roles are very clearly defined and detailed procedures and rules are in place to determine not just what work is completed but also how it is to be completed. The procedures for investigating and making changes are rigorously enforced to ensure lockstep, CE!, continuous improvement. In line with the CE! ideology (discussed in

greater detail below), both the organizational design and the individual roles at IFO closely mirror those at many of the other HVM factories.

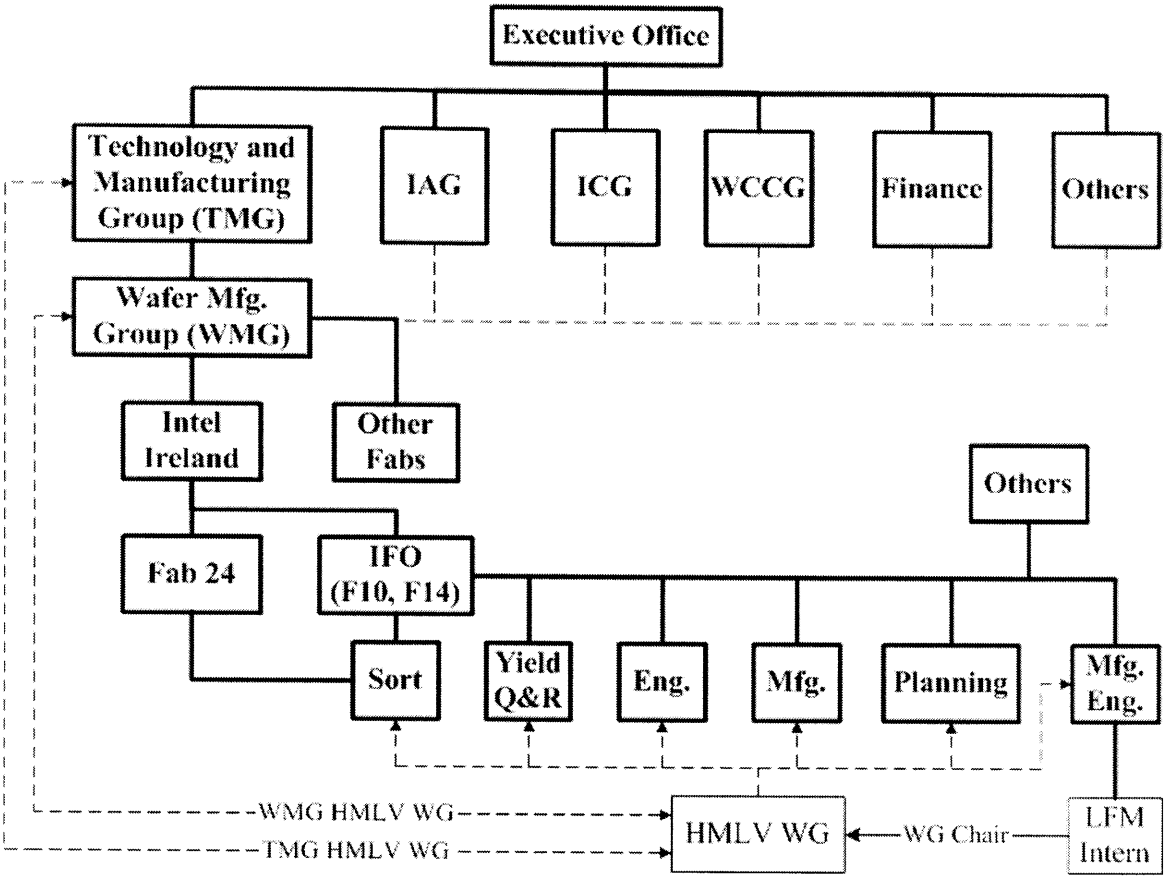

Figure 26: Organizational Chart with IFO HMLV WG Linkages

Historically, Intel's strategy has been to deliver higher performing microprocessor products and their supporting chipsets to market first and to quickly ramp to high manufacturing volume. Because the semiconductor business is cyclical and highly volatile and because product lifecycles are typically short (12-18 months), capital intensive capacity decisions are generally made well in advance of firm marketing build estimates or product introductions. Given the market uncertainty and high capital cost to build and ramp multiple fabs,[65] most companies initially have too little capacity to meet demand.

To optimize profits in the capacity constrained regime, Intel has focused its strategy, metrics and engineering efforts on process improvements that maximize chip performance and wafer and die yields. This enables not just more good-die-out during the initial product ramp and capacity constrained production regimes but also more good die

[65] Many products take several months or even quarters to break even and several years to fully recover depreciation costs. Moreover, many products make the majority of their profit in the first few quarters of production.

out over the product lifecycle of a high-volume product. This strategy meets both the customer's goal of obtaining the highest performing products as soon as possible and Intel's goal of maximizing profits. Overall, Intel's organizational strategic design has fit well with its strategy and the high complexity of manufacturing innovative new semiconductor products. In addition, the organizational capabilities necessary to support these goals have been effectively promoted through the CE! methodology and other efforts.

Intel's ability to implement and embrace the CE! methodology, in particular, has been a fundamental component of its ability to manage the complexity of frequent, rapid products ramps and to ensure high yields and process stability are achieved and maintained throughout the Intel manufacturing network (commonly referred to as the Virtual Factory Network or VF for short).

Briefly described, CE! consists of structured process transfer and statistical matching methods, the use of best-known-methods throughout the VF, change management through control boards, and a commitment to lockstep continuous improvement once full replication is achieved. In practice, CE! involves enormous ongoing cross-VF efforts to insure the matching of product yields and reliability metrics, manufacturing module operating characteristics and parametric data as well as the physical process inputs such as tool recipes and cleanliness, chemical and gas consumables, facility design, and the cleanroom process environment.

Although CE! requires significant effort and commitment, the results have been impressive. Through the CE! rules, procedures and the organizational strategic design, Intel has achieved faster product and process ramps and higher product yields and reliability throughout the VF. A key enabler of CE! problem solving and communication has been the mirrored organizational design of the different fabs. For example, if a layer owner for a given process technology and toolset in IFO has a problem, she already knows several of her direct VF counterparts that are processing the same or similar products on the same tools, in the same environment elsewhere. Moreover, she probably already has standing meetings with several of her counterparts to insure CE! and process matching between the fabs. The mirroring of organizational design and capability not only allows a much larger group of individuals to effectively focus on problem discovery and resolution, but also facilitates the communication and alignment of ongoing efforts to improve the processes.

Overall, Intel's mirrored, hierarchical, functional organizational structure has fit well with its strategic intent and environment. In particular, the strategic design facilitates the maintenance of manufacturing control in the complex semiconductor environment. And, the operational and organizational similarities between the HVM fabs make sense given the high degree of technical specialization required to maintain and operate the tools. However, the story is now changing for IFO.

Starting several years ago, IFOs strategic intent and operating environment began to diverge from the VF; by the end of 2003, IFO was processing more products than any

other fab in the 200/300 mm WMG network. IFO now holds a unique position in the VF as an HMLV fab and as a result, experiences problems that do not yet exist elsewhere. Moreover, many of IFOs HMLV customers have different needs than their HVM customers. In the words of one HMLV team member, "cost, time-to-market and manufacturing responsiveness are now more important than yield, ramp rate and MHz."

To meet the varied needs of both HVM and HMLV customers, IFO needs to analyze the cross-functional tradeoffs and choose operating points that meet each customer's needs. Both the metrics and the organizational strategic design need to be modified from the one-size-fits-all CE!, yield, ramp rate and MHz focused organization that worked so well for HVM manufacturing to a strategic design that better fits the needs of a mixed HVM/HMLV factory.

In particular, I believe that IFO should create a stand-alone HMLV organization composed of key thought leaders and influencers from the different functions. The group needs to be charged with and empowered to determine the best operating points for each product and customer on an ongoing basis. And, senior leadership needs to not only support the new function but also to revise the hierarchy of metrics and factory performance indicators to prevent the penalization of the other functional groups due to operational tradeoff decisions made by the HMLV team.

The first major task for the new HMLV organization should be the implementation and optimization of the Multi-Product Line Management system. While creating such a system-level focused cross-functional team will be difficult given the CE! environment, it is not without precedent. The Santa Clara development factory has already recognized the need for such an organization and has successfully created a cross-functional group to focus on system-level factory performance and operational tradeoffs.

At a higher level, senior leadership needs to develop a deeper understanding of the operational tradeoffs so that they can carefully communicate both internally and externally how the impacts of HMLV operations prevent or significantly complicate the achievement of some of the plan-of-record (POR) metrics in place for the HVM VF fabs. Internal communications need to include the revision or clarification of the factory operating philosophies to meet the challenges of HMLV operations. Again, such a departure would not be without precedent: in many ways Intel Israel has paved the way.

An anecdote may help to clarify some of these points. Of the 87 line items in the IFO Fab Operating Philosophies, only one line item used bold, underline or all caps: "We will drive **COPY EXACTLY!** in every applicable aspect of our work and our specs will reflect **COPY EXACTLY!**"[66] Although other items emphasize the importance of recognizing and meeting customer needs, the philosophies do not communicate the need to make complex tradeoffs or, in some cases, to accept more risk to achieve operational excellence in the HMLV environment. The result is a mixed or unclear message that leaves many engineers struggling with how to make decisions.

[66] Caine, Schlomo and Jim O'Hara. Ireland Fab Operating Philosophies. http://www-fab14.ir.intel.com/aboutus/Opsphil.ppt. (Mar. 18, 2004). p. 11.

For example, the MOST/2 monitor optimization project explored the cost and risk tradeoffs of reducing in-line measurement sampling rates. While many on the MOST/2 team felt that the optimal approach was to significantly reduce measurements (and product cost) at the potential risk of marginally lower yields and occasional excursions, others (such as the layer owners) were unwilling to do anything that might reduce yields or increase risk. Although they recognized the cost savings would benefit customers, they were unwilling to violate another factory philosophy: "[f]ix anything that is not right; no excursions, no excuses."[67] Although the MOST/2 objectives were clearly consistent with another of the stated philosophies, to "...reduce and eliminate measurements as stability is demonstrated, but consistent with the risks and liability of undetected problems,"[68] implementation has been difficult and slow. Nearly five months after MOST/2 was available, only two of the one hundred plus operations that would benefit from the new method have implemented the change.

Given the conservative yield-focused CE! culture and the mixed messages in the operating philosophies, this story is neither surprising nor, unfortunately, uncommon. The complex tradeoffs and higher risks required to achieve operational excellence in the HMLV environment need to be acknowledged by management and the operating philosophies and hierarchy of metrics changed to reflect the HMLV environment.

The political and cultural challenges of selectively breaking out of the CE! ideology are not to be taken lightly. Failure to reconcile the operating philosophies and culture with the challenges of HMLV operations may prevent the achievement of OpX, even if a stand-alone HMLV organization is created and empowered and the POR metrics appropriately renegotiated and revised for the operating environment.

The following sections continue the analysis of IFOs organizational behaviors and processes from the complementary political and cultural perspectives.

8.4 Political Design Challenges

From the political perspective, achieving HMLV operational excellence is no less challenging than when viewed through the strategic design lens. Figure 27 shows a map of many of the project stakeholders. Those indicated by a "+" are generally favorably disposed to the change. Those with a "~" are indifferent and those with a "-" are opposed to the change effort. As the stakeholder map indicates, many have mixed feelings about different aspects of the change.

The Yield and Engineering groups, for example, are both in favor of and opposed to some of the suggestions of the HMLV WG. Overall, the Engineering group has been supportive of team efforts and recognizes the importance of increasing tool sharing and process flexibility, for example. But, they are under significant pressure to meet the basic

[67] Ibid. p. 8.
[68] Ibid. p. 9.

demands of HMLV operations let alone implement many of the highly complex and time consuming activities identified by the team to move closer to OpX.

In contrast, many engineers in the Yield group view HMLV as a threat. HMLV operations generally increase system-wide manufacturing variation which has direct detrimental impacts on many of the yield performance metrics. The high product mix and data scarcity problems prevent many of the yield analysis tools from working as well as they have for HVM products, which reduces the effectiveness and perceived importance of yield analysis. While the Yield group is very interested in being involved in the HMLV WG and in improving their tools and processes for the HMLV environment, they are not generally favorably disposed to the tradeoffs suggested by some of the analyses conducted by the HMLV WG. Analyzing the situation from the political perspective yields some insight into why the groups have different dispositions to the HMLV WGs efforts.

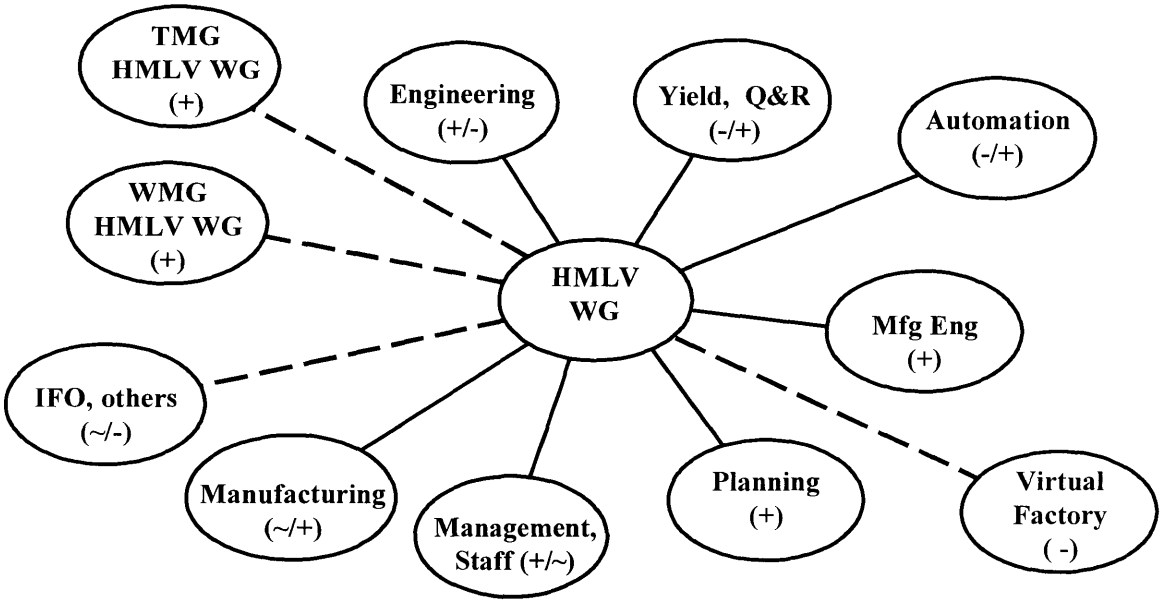

Figure 27: Stakeholder Analysis Map

The Engineering and Yield groups currently wield significant political power. All major changes and even many minor changes require their approval or support. In fact, it is not unusual for meetings to be cancelled or decisions to be postponed if the Yield team member can not attend. The diminished influence of this group due to the reduced importance of high product yields for many HMLV customers is and will continue to be viewed as a personal and or organizational threat.

Perhaps more importantly, because yield has been the highest factory priority up to this point in time and other needs were optimized subject to the maintenance of high yields, there are a lack of formal or informal mechanisms for evaluating tradeoffs such as faster time-to-market and lower product costs at the expense of even modest reductions in product yields. The significant sustained efforts to convince some yield engineers that the

MOST and MOST/2 measurement rate methods were truly in the best interest of Intel is one good example.

Another group with significant political power is the factory automation team. Many factory improvements, particularly those that help engineering and manufacturing to manage the complexities of the HMLV environment, require automation support. Consequently, the automation team has significant political power due to their ability to prioritize automation activities. To better align the overall interest of the factory, I recommend that the prioritization of automation activities should be included in the scope of the proposed HMLV team. Or, at a minimum, the team should have an influential automation manager to facilitate the resolution of the resource contention conflicts that are likely to arise.

Since many decisions in the current organization are made by mid- and staff-level managers, it is imperative that the proposed HMLV team also include one or more influential staff-level managers. An example helps to elucidate how the management level control of decisions in the current organization can create internal conflicts. Although one of the HMLV WG members was aware that product and process flexibility were key HMLV initiatives, the team member found a way into the staff-level Manufacturing Excellence (MEx) agenda to present flexibility options rather than working through the HMLV WG team. Whether the WG member chose such a path because staff-level involvement in the WG had diminished or because of the opportunity for more visibility in MEx, the negative results were the same. The importance of aligning both tangible and intangible goals and rewards with the desired organizational structure and the desired behaviors can not be overstated. It is a crucial part of designing a more optimal organizational strategic design and political environment.

Perhaps the biggest political challenge that the HMLV transition presents has already been briefly touched on. Senior factory leadership must manage its external communications very carefully. Although efficiency and productivity improvements can largely mitigate the negative impacts to factory performance caused by HMLV in the short-term, it can not reduce or eliminate them. Moreover, the CE! structure in place nearly guarantees the rapid dissemination of efficiency and productivity improvements. The increased system-level variation caused by HMLV operations will drive increases in some combination of cycle time, capacity or inventory. On the one hand, communicating these impacts may prevent the sourcing of future HMLV products in IFO. On the other hand, failing to understand or communicate the tradeoffs may result in unobtainable factory commitments and ongoing organizational underperformance.

The inherent political conflicts with both options are formidable. The best, albeit difficult, approach to manage these conflicts is to point out the high fixed organizational and system-level costs required to achieve OpX in the HMLV environment. Since IFO has already managed the initial transition, the incremental costs of sourcing additional HMLV products at IFO are likely much lower that the costs of introducing HMLV products to other facilities. The only way to maintain this advantage in the long-term, however, is to bolster investments in the core HMLV competencies of improved

organizational and operational flexibility and efficiency, and improved customer needs-focused complexity management tools.

8.5 Cultural Design Challenges

HMLV presents significant cultural challenges as well. To a large degree, the CE! methodology has become the single most formative and informative aspect of Intel's culture. It is not uncommon for employees to interrupt a brainstorming problem session by interjecting "CE!" into the discussion. In the best cases, this causes the group to reflect on who should be involved from other VF teams to insure buy-in across the network. More often, however, it causes teams to fall into line with the currently accepted approach.

Although the importance of CE! in the success of HVM at Intel should not be glossed over, it can provide an impediment to creative efforts to define and implement new ways to meet, for instance, the more varied needs of HMLV customers.

An example from my experience illustrates the point. One of the first ways I considered to meet the elevated importance of delivery and service for HMLV customers was to explore how finished goods inventory levels were established. My intent was to make sure that the inventory levels were appropriate for HMLV customer demand patterns. I soon discovered that the inventory levels were very similar for many products regardless of the product demand pattern, demand outlook or customer involved. The reason to the best of anyone's memory, I was told, was to maintain a consistent process for all products. While this approach may have worked for the capacity constrained product regimes common in the past, such an approach and the rationale for unquestioningly maintaining the current inventory levels are impediments to achieving OpX in the HMLV environment.

Another set of cultural challenges is imbedded in a very common artifact. Each employee badge contains a list of Intel's core values: Customer Orientation, Risk Taking, Great Place to Work, Results Orientation, Discipline and Quality. If the detailed descriptions of these values are considered, it becomes clear that while most values are congruent with the imperatives of HMLV, there are also inherent conflicts. For example, the quality value suggests that every employee "strive to achieve the highest standards of excellence and to do the right things right." For many HMLV products and customers, striving to provide the highest quality product would result in an uncompetitive or less competitive product cost.

To resolve the conflicts with CE! and to align employees to the wide range of HVM and HMLV customer needs, IFO senior leadership needs to embark on a major communications effort. Mechanisms for communicating the goals of both HVM and HMLV manufacturing need to be developed. It may also be helpful to devise a new artifact or artifacts to embody the flexibility and other attitudes, behaviors and approaches necessary to enable cultural HMLV OpX.

In summary, to enable the continued successful transition of IFO from an HVM to a mixed HVM/HMLV manufacturing operation, a number of changes in the organizational strategic design, political and cultural environment are suggested. IFO senior management should consider creating and empowering a stand-alone HMLV organization to analyze cross-functional operational problems and to implement solutions which optimize the systemic tradeoffs for the different needs of HVM and HMLV customers. IFOs new goals need to be communicated and the political and cultural impacts need to be addressed through appropriate new metrics and factory indicators. Senior leadership also needs to develop a deep understanding of the operational tradeoffs and to carefully and explicitly communicate HMLV impacts both internally and externally. And, tactics need to be developed to address the political and cultural challenges of selectively breaking out of the CE! methodology.

Chapter 9: Summary and Conclusions

In Chapters one through four, we discussed some of the macroscopic issues of achieving operational excellence in a high-mix, low-volume environment. In Chapters five and six, we performed an in-depth analysis of one of the key aspects of achieving OpX in the HMLV environment: optimizing in-process metrology inspection rates. Because the existing methods did not effectively manage some of the complexities of operating in a mixed HVM/HMLV environment, the MOST/2 method was proposed. In Chapter seven we performed a comparative analysis of the different methods and found that MOST/2 provides superior cost/risk balanced solutions. Because of the important role of organizational, political and cultural alignment in achieving and maintaining OpX in the long-term, Chapter eight analyzed the current situation and provided recommendations to insure future success. In this chapter, we provide a quick summary of many of the HMLV topics discussed and conclude with a brief revisit of our hypothesis and the supporting data.

9.1 Thesis Summary

Over the last ten to fifteen years, three major market developments exerted pressure on Intel's strategy: PC market saturation, performance overshoot and the emergence of the internet. Due in part to these changes, Intel responded by acquiring and adding a significant number of primarily high-mix, low-volume (HMLV) products to its portfolio.

For a number of reasons, IFO was charged with the responsibility for manufacturing more HMLV products than any other factory in the 200/300 mm WMG network. The addition of HMLV products to the IFO product portfolio caused significant challenges.

Foremost, the needs of many HMLV customers are different from HVM customers and require different operational tradeoffs. Moreover, because the factory, tools, systems, organization processes and business processes were originally designed and optimized for HVM, many of the systems and tools were incapable, and the people ill-prepared to manage the complexities and tradeoffs required to achieve OpX in the HMLV environment.

Through a structured gap analysis process, the IFO HMLV WG identified over 230 problems that might prevent the attainment of future product mix and volume commitments. The problems were aggregated into major activity groups and projects were prioritized and resourced based on risk and leverage. Among the high-risk, high-leverage activities identified, improved scheduling and WIP management was identified as critical.

Consequently, one of the projects within the improved scheduling and WIP management activity group, the optimization of in-process metrology inspection rates,

was chosen and analyzed in depth as a case study of how to achieve one element of OpX in the HMLV environment.

The reasons that HMLV products cause significant degradations in factory metrics and performance were analyzed and determined to be largely the result of impacts to metrology operations based on the current inspection rate methods. The current methods were described and analyzed and key shortcomings were identified: primarily the failure to account for the relevant economics, product specific risks, and product and customer specific HMLV needs.

A customer needs-focused, complexity management tool and method for in-process metrology inspection rate optimization was proposed: MOST/2. The economic and probability analysis framework were described in detail and a sensitivity analysis was provided to help users understand the most important input variables and their contributions to the model's results.

A comparative analysis of metrology inspection rate optimization methods was conducted for 27 of the roughly 115 similar operations currently in evaluation at IFO. MOST/2 was shown to provide superior cost/risk balanced results for the HMLV environment. With only modest increases in the material at risk per excursion, key results of using MOST/2 for the 27 operations analyzed include annual costs savings of approximately $95,000, cycle time savings of at least 5.3 hours, operator savings of at least 4.2 people per year, and metrology capacity utilization rate reductions of approximately 65%.

These results provide strong support for the hypothesis that achieving operational excellence in an HMLV semiconductor environment requires improvements in both the identification and servicing of customer needs as well as better people, processes, tools or systems to manage the increased complexity of HMLV operations. The short descriptions of other high-leverage HMLV activities and projects provide additional corroborating evidence.

Finally, an analysis of the organizational strategic design, political and cultural environment at IFO was performed. Many of the recommendations of that analysis are summarized below.

9.2 Thesis Conclusions and Recommendations

Achieving operational excellence in the multi-customer, multi-technology, multi-product HMLV environment requires not only the recognition of the different needs of HVM and HMLV customers but also improved tools, processes and systems to help factory personnel manage the increased complexity.

Moreover, future success requires an ongoing focus on the leadership and organizational strategic design, political and cultural environment required to create the foundation for long-term HMLV operational excellence.

IFO senior management should create and empower a stand-alone HMLV organization. The organization should include influential managers from each of the major functional groups and should be chaired or coached by a strong staff-level manager. The focus of the group should be on analyzing cross-functional operational problems and implementing solutions which optimize the systemic tradeoffs for the different needs of HVM and HMLV customers.

Realistic but challenging HMLV-focused goals need to be communicated to the factory and the political and cultural impacts need to be addressed through appropriate new metrics and factory indicators. Senior leadership also needs to develop a deeper understanding of the operational tradeoffs so that they can carefully and explicitly communicate HMLV impacts externally. And, tactics need to be developed to address the political and cultural challenges of selectively breaking out of the CE! methodology.

9.3 MOST/2 Suggested Future Work

MOST/2 should be fully implemented at metrology steps not controlled through other mechanisms (such as automated process control) for all of the stable manufacturing products, processes and technologies. Moreover, a modified version of MOST/2 should be developed and applied for the other factory NVA steps. Automation support should be enlisted to streamline the collection and dynamic updating of product or product group specific input variables. If a product specific implementation can not be supported, more product aggregation groups should be created to maximize inspection and excursion cost savings and to minimize the material at risk.

9.4 HMLV Suggested Future Work

The organizational strategic design, political, and cultural environmental changes recommended are critical enablers of long-term HMLV operational excellence. The TopX[69] activities need continuing support. Two of the most important, high-leverage projects are MPLM and Product/Process Flex. In addition, senior-level support is required to remove some of the current roadblocks preventing the optimization of finished good inventory levels based on the product demand pattern, demand outlook and customer or customers involved.

9.5 Applicability of Thesis Findings to Other Companies and Industries

Although we have focused primarily on the challenges of transitioning an HVM semiconductor fab into the HMLV environment, many of the lessons learned easily generalize to other companies and industries. While many of the specific challenges will depend on the particular situation, the general challenge of learning how to manage the greater complexity inherent in HMLV operations is universal as is the importance of recognizing and meeting the needs of all types of customers.

[69] The TopX activities are the high-risk or high-leverage gap-closing projects determined by the HMLV WG to help IFO achieve OpX.

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Appendix A: Derivation of Formulas

This section provides additional details and some derivations for equations presented or developed in the thesis.

Derivation of Equation 2: The Probability of a Process Excursion in a Measurement Group of Size *T*

As defined, *P(A)* is the probability that the process goes into excursion while processing a given lot. *B* is the event that the process goes into excursion sometime during the processing of a given measurement group of size *T*. Since the chance of the process going into excursion during the processing of any given lot is independent, we can determine *P(B)* by summing the mutually exclusive ways it can occur for a given measurement group.

$$P(B) = P(A) + P(A) \bullet (1 - P(A)) + P(A) \bullet (1 - P(A))^2 + ... + P(A) \bullet (1 - P(A))^S$$

$$P(B) = P(A) \bullet \sum_{N=0}^{S} (1 - P(A))^n$$

Substituting *b* for 1-*P(A)* and S_n for $\sum_{n=0}^{S} b^n$, we have:

$$S_n = 1 + b + b^2 + ... + b^S$$

$$bS_n = b + b^2 + b^3 + ... + b^S + b^{S+1}$$

$$S_n = bS_n = S_n(1 - b) = 1 - b^{S+1}$$

$$S_n = \frac{1 - b^{S+1}}{1 - b}$$

Plugging the original values back in and simplifying for *P(B)*, we have now derived the expression for Equation 2.

$$P(B) = P(A)S_n = \frac{P(A) \bullet [1 - (1 - P(A))^{S+1}]}{1 - (1 - P(A))} = \frac{P(A) \bullet [1 - (1 - P(A))^{S+1}]}{1 - 1 + P(A)}$$

$$P(B) = \frac{P(A) \bullet [1 - (1 - P(A))^{S+1}]}{P(A)} = 1 - (1 - P(A))^{S+1} = 1 - (1 - P(A))^T$$

Derivation of Equation 4: The Expected Number of Lots Effected Given an Excursion in a Measurement Group of Size T

P(A) and *P(B)* are defined as in Equation 2 and the preceding derivation. As discussed in Section 6.3, we can now use Bayes' Theorem to find the expected number of lots at risk given that an OOD event has occurred during the processing of measurement group T as follows:

$$E(\#Lots_n \mid OOD) = \frac{P(A) \bullet T}{P(B)} + \frac{P(A)(1-P(A)) \bullet (T-1)}{P(B)} + \ldots + \frac{P(A)(1-P(A))^S \bullet (T-S)}{P(B)}$$

$$E(\#Lots_n \mid OOD) = \frac{P(A)}{P(B)} \sum_{n=0}^{S} (1-P(A))^n (T-n)$$

If we break this expression into two parts and substitute b for 1-*P(A)* again, it is clear that the first sequence is the same as before.

$$E(\#Lots_n \mid OOD) = \frac{P(A)}{P(B)} \sum_{n=0}^{S} (1-P(A))^n (T-n)$$

$$E(\#Lots_n \mid OOD) = \frac{P(A)}{P(B)} \sum_{n=0}^{S} b^n (T-n)$$

$$E(\#Lots_n \mid OOD) = \frac{P(A) \bullet T}{P(B)} \sum_{n=0}^{S} b^n - \frac{P(A)}{P(B)} \sum_{n=0}^{S} b^n \bullet n$$

$$E(\#Lots_n \mid OOD) = \frac{P(A) \bullet T}{P(B)} \bullet S_n - \frac{P(A)}{P(B)} \sum_{n=0}^{S} b^n \bullet n$$

$$E(\#Lots_n \mid OOD) = \frac{P(A) \bullet T}{P(B)} \bullet \frac{(1-b^{S+1})}{1-b} - \frac{P(A)}{P(B)} \sum_{n=0}^{S} b^n \bullet n$$

$$E(\#Lots_n \mid OOD) = \frac{P(A) \bullet T \bullet (1-(1-P(A))^{S+1})}{P(B) \bullet (1-(1-P(A)))} - \frac{P(A)}{P(B)} \sum_{n=0}^{S} b^n \bullet n$$

Ignoring the first term for the time being, if we now substitute D_n for $\sum_{n=0}^{S} b^n \bullet n$, the second term becomes $\frac{P(A)}{P(B)} D_n$. Proceeding as we did with the previous sequence,

$$D_n = 0 + b + 2b^2 + 3b^3 + \ldots + Sb^S$$

$$bD_n = b^2 + 2b^3 + \ldots + (S-1)b^S + Sb^{S+1}$$

$$D_n - bD_n = D_n(1-b) = b + b^2 + b^3 + \ldots + b^S - Sb^{S+1}$$

$$D_n(1-b) + Sb^{S+1} = b + b^2 + b^3 + \ldots + b^S = \sum_{n=1}^{S} b^n$$

Substituting E_n for $\sum_{n=1}^{S} b^n$, we have:

$$D_n(1-b)+Sb^{S+1}=E_n=b+b^2+b^3+\ldots+b^S$$
$$bE_n=b^2+b^3+\ldots+b^S+b^{S+1}$$
$$E_n-bE_n=E_n(1-b)=b-b^{S+1}$$

So, $E_n=\dfrac{b-b^{S+1}}{1-b}$ and, $D_n=\dfrac{b-b^{S+1}}{(1-b)^2}-\dfrac{Sb^{S+1}}{1-b}$.

Finally, if we substitute T for S+1, plug the original value for b into the equation and simplify, we find the following expression.

$$E(\#Lots_n \mid OOD)=\frac{P(A)\bullet T\bullet(1-b^{S+1})}{P(B)\bullet(1-b)}-\frac{P(A)\bullet(b-b^{S+1})}{P(B)\bullet(1-b)^2}+\frac{P(A)\bullet S\bullet b^{S+1}}{P(B)\bullet(1-b)}$$
$$=\frac{P(A)\bullet T\bullet(1-b^T)}{P(B)\bullet(1-b)}-\frac{P(A)\bullet(b-b^T)}{P(B)\bullet(1-b)^2}+\frac{P(A)\bullet S\bullet b^T}{P(B)\bullet(1-b)}$$
$$=\frac{P(A)\bullet T\bullet(1-(1-P(A))^T)}{P(B)\bullet(1-1+P(A))}-\frac{P(A)\bullet((1-P(A)-(1-P(A))^T)}{P(B)\bullet(1-1+P(A))^2}+\frac{P(A)\bullet S\bullet(1-P(A))^T}{P(B)\bullet(1-1+P(A))}$$
$$=\frac{P(A)\bullet T\bullet(1-(1-P(A))^T)}{P(B)\bullet P(A)}-\frac{P(A)\bullet(1-P(A)-(1-P(A))^T)}{P(B)\bullet P(A)^2}+\frac{P(A)\bullet S\bullet(1-P(A))^T}{P(B)\bullet P(A)}$$

Recognizing that $P(B)=1-(1-P(A))^T$, $T\text{-}1=S$ and canceling terms, we finally achieve the simplified expression shown in Equation 4.

$$=\frac{P(A)\bullet T\bullet P(B)}{P(B)\bullet P(A)}-\frac{P(A)\bullet(1-P(A)-(1-P(A))^T)}{P(B)\bullet P(A)^2}+\frac{P(A)\bullet S\bullet(1-P(A))^T}{P(B)\bullet P(A)}$$
$$E(\#Lots_n \mid OOD)=T-\frac{1-P(A)-(1-P(A))^T}{P(B)\bullet P(A)}+\frac{(T-1)\bullet(1-P(A))^T}{P(B)}$$
$$N=E(\#Lots_n \mid OOD)=T-\frac{1-P(A)-(1-P(A))^T}{P(B)\bullet P(A)}+\frac{(T-1)\bullet(1-P(A))^T}{P(B)}$$

Derivation of Equation 5: The Expected Number of Lots Effected Given an Excursion in a Measurement Group of Size *T* with Limited Power to Detect the Excursion

With *N* defined as in Equation 4 and the preceding derivation, we can now address the question of how our ability to detect an excursion affects the total amount of material at risk. Let's call *C* the event that our measurement process detects an out-of-disposition lot from an excursionary process. Since we have assumed that the process cannot fix itself, there are a number of mutually exclusive ways that this event could occur. The most likely way is that the process became excursionary during the current measurement group and that we detected the problem at the first inspection opportunity. In this case, the amount of material at risk would be *N*. Alternatively, the process may have became excursionary during the previous measurement group and we failed to catch it on the first inspection opportunity; but, we succeeded on the second inspection opportunity. In this case, the amount of material at risk would be $N + T$.

As shown below, these are components of the first two terms of an infinite series. The sum of this series is the total amount of material at risk provided that our imperfect measurement tool has detected an excursionary lot. We denote this infinite series as $E(\#\,Lots_n\_OOD\_C)$ and calculate its sum as follows:

$$= P(C) \bullet N + P(C) \bullet (1 - P(C)) \bullet (N + T) + \ldots + P(C) \bullet (1 - P(C))^n \bullet (N + nT) + \ldots$$

$$= P(C) \bullet \sum_{n=0}^{\infty} (1 - P(C))^n \bullet (N + nT)$$

Substituting g for 1-$P(C)$, we have:

$$E(\#\,Lots_n\_OOD\_C) = P(C) \bullet \sum_{n=0}^{\infty} g^n \bullet (N + nT) = P(C) \bullet N \bullet \sum_{n=0}^{\infty} g^n + P(C) \bullet T \bullet \sum_{n=0}^{\infty} g^n \bullet n$$

Substituting F_n for $\sum_{n=0}^{\infty} g^n$ and G_n for $\sum_{n=0}^{\infty} ng^n$, we again find that:

$$F_n = 1 + g + g^2 + \ldots + g^n$$

$$gF_n = g + g^2 + g^3 + \ldots + g^n + g^{n+1}$$

$$F_n - gF_n = F_n(1 - g) = 1 - g^{n+1}$$

$$F_n = \frac{1 - g^{n+1}}{1 - g}$$

and,

$$G_n = 0 + g + 2g^2 + 3g^3 + \ldots + ng^n$$

$$gG_n = g^2 + 2g^3 + \ldots + (n-1) \bullet g^n + ng^{n+1}$$

$$G_n - gG_n = G_n(1 - g) = g + g^2 + g^3 + \ldots + g^n - ng^{n+1}$$

$$G_n(1 - g) + ng^{n+1} = g + g^2 + g^3 + \ldots + g^n = \sum_{n=1}^{\infty} g^n$$

Substituting H_n for $\sum_{n=1}^{\infty} g^n$, we have:

$$G_n(1-g)+ng^{n+1} = H_n = g+g^2+g^3+...+g^n$$
$$gH_n = g^2+g^3+...+g^n+g^{n+1}$$
$$H_n - gH_n = H_n(1-g) = g-g^{n+1}$$

So, $H_n = \frac{g-g^{n+1}}{1-g}$ and, $G_n = \frac{g-g^{n+1}}{(1-g)^2} - \frac{ng^{n+1}}{1-g}$.

Taking the limit as *n* goes to infinity, we have:

$$\underset{n->\infty}{Lim}(F_n) = \frac{1-g^{n+1}}{1-g} = \frac{1}{1-g} - \frac{g^{n+1}}{1-g} = \frac{1}{1-g} - 0 \text{ for -1 > } g \text{ > 1 and,}$$

$$\underset{n->\infty}{Lim}(G_n) = \frac{g-g^{n+1}}{(1-g)^2} - \frac{ng^{n+1}}{1-g} = \frac{g}{(1-g)^2} - \frac{g^{n+1}}{(1-g)^2} - \frac{ng^{n+1}}{1-g} = \frac{g}{(1-g)^2} - 0 - 0 \text{ for -1 > } g \text{ > 1.}$$

Substituting $g = 1-P(C)$, putting it all together and simplifying yields Equation 5, below.

$$E(\#Lots_n\_OOD\_C) = P(C)\bullet\sum_{n=0}^{\infty} g^n \bullet (N+nT)$$

$$E(\#Lots_n\_OOD\_C) = P(C)\bullet N\bullet\sum_{n=o}^{\infty} g^n + P(C)\bullet T\bullet\sum_{n=0}^{\infty} ng^n$$

$$E(\#Lots_n\_OOD\_C) = P(C)\bullet N\bullet \underset{n->\infty}{Lim}(F_n) + P(C)\bullet T\bullet \underset{n->\infty}{Lim}(G_n)$$

$$E(\#Lots_n\_OOD\_C) = \frac{P(C)\bullet N}{1-g} + \frac{P(C)\bullet T\bullet g}{(1-g)^2} = \frac{P(C)\bullet N}{1-1+P(C)} + \frac{P(C)\bullet T\bullet(1-P(C))}{(1-1+P(C))^2}$$

$$E(\#Lots_n\_OOD\_C) = N + \frac{T\bullet(1-P(C))}{P(C)}$$