Analyzing Sampling Methodologies in Semiconductor Manufacturing

by

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Bachelor of Science in Mechanical Engineering
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Submitted to the Sloan School of Management
and the Department of Mechanical Engineering
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and
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ABSTRACT

This thesis describes work completed during an internship assignment at Intel Corporation's process development and wafer fabrication manufacturing facility in Santa Clara, California. At the highest level, this work relates to the importance of adequately creating and maintaining data within IT solutions in order to receive the full business benefit expected through the use of these systems.

More specifically, the project uses, as a case example, the sampling methodology used in the fab for metrology data collection to show that significant issues exist relating to the software application database and business processes concerning data accuracy and completeness. The organizational challenges contributing to this problem will also be discussed.

Various recommendations were undertaken to improve the application's effectiveness. As part of this effort, plans for an online reporting tool were developed allowing much greater visibility into the system's ongoing performance. Initial data updates and other improvements resulted in a reduction in both product cycle times and required labor hours for metrology operations.

Without a rigorous focus on the accuracy and completeness of data within manufacturing execution systems, the results of continuous improvement activities will be less than expected. Furthermore, sharing information relating to these projects across geographical boundaries and business units is vital to the success of manufacturing organizations.

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CHAPTER 1 – INTRODUCTION & OVERVIEW

1.1 Project Overview

Many manufacturing companies are dealing with rapidly changing markets and industries. The most successful ones will be those that can deliver new and improved products to the customers at a faster pace than the competition – at a profit. Typically, manufacturing execution systems, necessary to keep pace with the industry's changing landscape, are weighted down by their own complexities causing great difficulties during their implementation or modification. This situation is especially true for those industries where product life cycles are getting shorter and the variety and complexity of the products are increasing.[1]

> "While U.S. manufacturers recognize the importance of speed and flexibility, many are impeded by efforts to become more agile producers. Even highly automated plants and factories struggle to overcome difficulties in adapting or reconfiguring production operations to accommodate design changes and new product lines. Idiosyncrasies in manufacturing software and incompatibilities among software applications are a primary source of costly delays..."[2]

This thesis deals with these issues at a high level while using one particular example as a case study. The project undertaken at Intel's process development and semiconductor fabrication facility in Santa Clara, California involves the information technology application for their sampling methodology used for metrology data collection. Several issues exist with the accuracy and completeness of data due to the system design, organizational structure, and business processes. Each one of these will be discussed in later chapters.

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[1] Christopher, Neil. National Institute of Standards and Technology. Technologies for the Integration of Manufacturing Applications (TIMA). 22 May 2003. 17 Mar. 2004 <http://www.atp.nist.gov/www/press/9705tima.htm>.

[2] ibid

1.2 Project Motivation

This project was motivated by the desire to improve one of the high mix, low volume challenges discussed in Chapter 2 – increased inspection requirements. Early in the internship assignment, it came to management's attention that the measurement rates for specific products at metrology operations were much higher than expected. Therefore, it was believed that by studying the data, systems, and business processes inherent to Intel's sampling methodology, improvements could be made to reduce the impact that the increased number of measurements caused by an increased product mix will have on D2's labor requirements and cycle time.

1.3 Organization of the Thesis

This paper is divided into six subsequent chapters.

Chapter 2 discusses Intel Corporation, its products, and its latest strategy for entry into the demanding consumer electronics business. The technology development activities of semiconductor manufacturing at Intel are discussed with a review of the organization where the project work was completed.

Chapter 3 briefly reviews the complex semiconductor manufacturing processes in order to present these to a reader new to the topic. Metrology operations are then introduced providing special attention to those metrology areas studied during the project.

Chapter 4 reviews widely accepted sampling plans and, more importantly, Intel's current practices and application of their skip lot sampling methodology.

Chapter 5 begins with a discussion of a quality audit and includes a detailed system analysis of Intel's skip lot sampling plan. It presents the outcome of a quality review for this system, focusing on perceived versus actual measurement rates and includes a special study of transient data resulting from bringing equipment online after downtime events. This allows a comparison of the results of the analysis to actions taken

in the fab. Finally, it reviews a reporting tool to improve the accessibility and availability of measurement rate data in the future.

Chapter 6 provides a cultural perspective on the above issues and the internship assignment, in particular.

Finally, Chapter 7 includes specific recommendations for improvement, the implementation status, a possible future project, and general observations regarding the flow of information within and across organizations.

CHAPTER 2 – PROJECT BACKGROUND & DESCRIPTION

This chapter outlines details regarding Intel Corporation including its products, basic strategy for continued growth, and manufacturing operations as well as background materials specific to the project. This sets the stage for further chapters discussing quality assurance and sampling plans at the D2 research and development semiconductor wafer fabrication facility.

2.1 Intel Corporation Overview

Intel is the world's largest semiconductor chip manufacturer and holds a commanding lead over its nearest competitors with an estimated 80% share of the worldwide microprocessor market.[3] Fiscal year sales were just over $30 Billion with net income exceeding $5.6 Billion due to gross profit margins over 60%.[4]

The company's primary focus is to design, develop, manufacture, and market computing, networking, and communication products with the following corporate mission:

> "Do a great job for our customers, employees and stockholders by being the preeminent building block supplier to the worldwide Internet economy."[5]

Intel's major product categories include microprocessors, chipsets, motherboards, wired and wireless connectivity products, flash memory, and both processors and chipsets for the cellular and handheld computing industries. At the end of 2003, the corporation was divided into three primary business units: Intel Architecture, Intel Communications Group (ICG), and the Wireless Communications and Computing Group (WCCG). Each segment works to develop improved integrated circuits and silicon solutions in support of the corporate goal.

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[3] Carbone, Jim. "Microprocessors Show Signs of Life as Demand Builds." Purchasing. 20 Nov. 2003: 17-18. Business Source Elite. EBSCOhost. 15 Mar. 2004. Keyword: Intel market share.

[4] Edelstone, Mark L. (4 Mar. 2004). Intel Corp. Fine-Tuning EPS Estimate Lower. Equity Research Note. Morgan Stanley. Retrieved 15 Mar 2004 from InvestText Plus Database.

[5] Intel Corporation. "From Silicon to Software." Intel's Quality System Handbook, 15 Mar. 2004 <http://developer.intel.com/design/quality/quality.htm>.

The Intel Architecture organization accounted for roughly 87% of the company's revenues in 2003 – 73% specifically from the microprocessor business. Within this group, technology solutions are developed using its microprocessor, motherboard, and chipset capabilities for the personal computing and server markets. The Intel Communications Group and Wireless Communications and Computing Group accounted for 7% and 6% of consolidated 2003 net revenues, respectively.[6]

2.1.1 Intel Operations

The Technology and Manufacturing Group (TMG) is responsible for all of Intel's manufacturing operations and technology development activities worldwide. Manufacturing facilities are located in the United States, Israel, Ireland, Malaysia, the Philippines, China, and Costa Rica.

Fab Sort Manufacturing (FSM) and Assembly Test Manufacturing (ATM) report to TMG as well as several other organizations in charge of technology development, system manufacturing, and other support services. Fab Sort Manufacturing is responsible for Intel's wafer fabrication and sort facilities while Assembly Test Manufacturing controls the remaining activities of assembly and final test.

Each fab is assigned a set of products requiring various technologies and processes that it will manufacture based on the limitations and utilization of its existing equipment. For instance, Fab A may be dedicated to certain flash memory products while Fabs B and C utilize their resources to produce various microprocessor products. This would result in Fabs B and C being part of the logic "virtual factory" since they manufacture the same or similar (logic) products. The results of yield and output improvement projects are shared among all members of the "virtual factory" after being implemented at one facility. Within this "virtual factory" framework, changes to processes and equipment at all manufacturing sites are tightly controlled to ensure each

[6] Intel Corporation. (27 Dec 2003). "Form 10-K." Annual Filing with the United States Securities and Exchange Commission, Retrieved 10 Mar 2004, from Thomson Research Database.

facility is as similar to the others for resource sharing, benchmarking, improved yield learning, increased speed to capacity ramp, and optimal manufacturing flexibility.[7]

2.1.2 Supply Chain Perspective for Semiconductor Manufacturing

In order to convert silicon into packaged electronic components, four basic factory operations are necessary: wafer fabrication, wafer sort, packaged component assembly, and final test (reference Figure 2.1). Intel uses a die bank (an inventory of fabricated and cut wafers) as an interface between their push-based strategy (wafer fab and sort) and their pull-based strategy (assembly and final test).

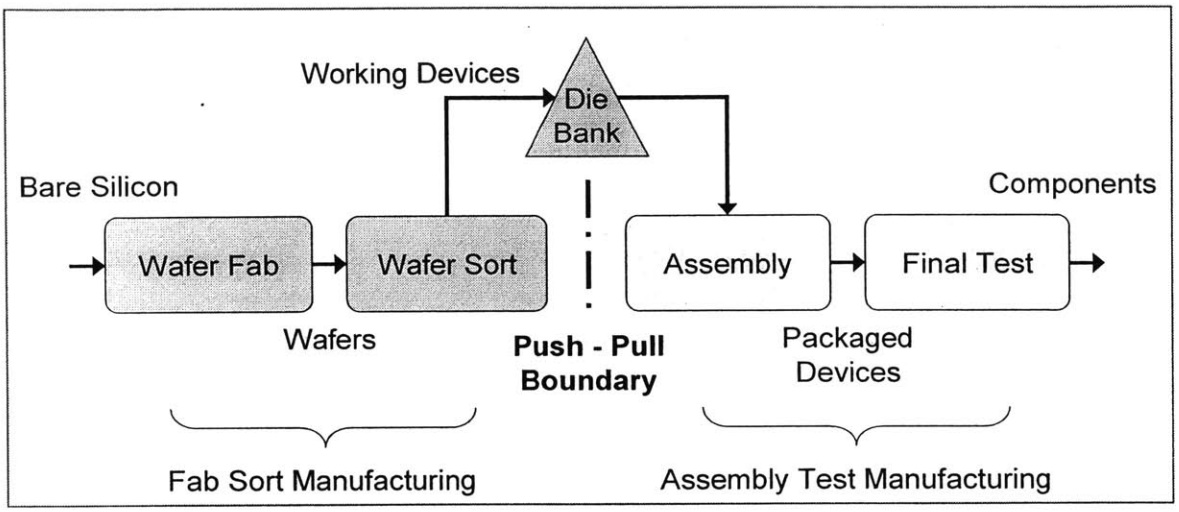

Figure 2.1: Semiconductor Manufacturing Supply Chain at Intel.[8]

Within the wafer sort operation, each die (or microprocessor chip) on completed wafers is tested for functionality and performance. These wafers are then cut to separate the individual chips and sorted based on the test results. The good chips are sent to the die bank for future retrieval by assembly operations. Packaged devices are the result of the assembly process where individual die are mounted and prepared for use in customer applications. Prior to shipment, each one of these packaged microprocessors is tested again for functionality and performance in the final test operation.

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[7] Ponchner, Karen. "Implementing Advanced Process Control in a Copy EXACTLY! Environment." Thesis. Massachusetts Institute of Technology, 2002. 24-26.

[8] Adapted from Atherton, Linda F., and Robert W. Atherton. Wafer Fabrication: Factory Performance and Analysis. Boston: Kluwer Academic, 1995. 6.

2.2 Technology Development

This section discusses the different phases of semiconductor manufacturing including technology development. Specifically, the charter of Intel's California Technology Manufacturing D2 organization is explained to describe the context for this thesis project.

2.2.1 The Different Phases of Semiconductor Manufacturing

Yield management is critical to the success of a wafer fab. The yield learning cycle varies significantly between the different phases of semiconductor manufacturing. Figure 2.2 represents the expectations for yield improvements between these different phases: exploratory research and development, process development, yield learning during manufacturing ramp, and yield monitoring of a stable manufacturing process.

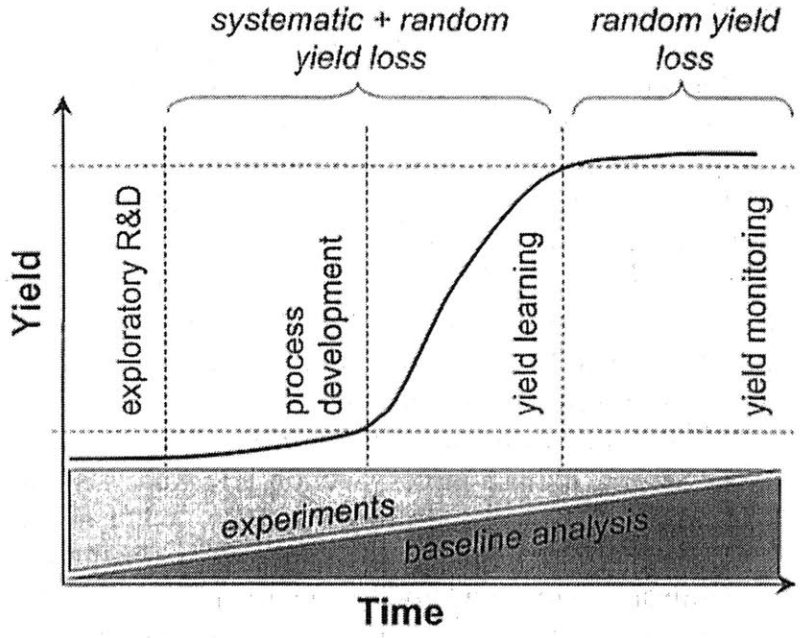

Figure 2.2: Different Phases of Semiconductor Manufacturing.[9]

During the first stage of research and development, relatively few measurements are taken for quality assurance since the primary purpose of this timeframe is to determine product feasibility through experiments. As the product progresses through the

[9] Diebold, Alain C., ed. Handbook of Silicon Semiconductor Metrology. New York: Marcel Dekker, Inc., 2001. 679-681.

process development phase into manufacturing ramp, measurements and data collection processes are critical to maximize opportunities for yield learning. For this reason, data collection procedures are typically automated to gather the necessary information for improving yield. The number of measurements taken and time invested in metrology are at a maximum during this phase. The inspection process has a critical role in improving fab yield and cost effectiveness at this time by enabling both the early discovery of defects and the corrective action necessary to avoid similar mistakes. At this point in the manufacturing process maturity, additional inspections lead to fewer defects and higher yields. Finally, when the manufacturing processes mature and stabilize, the number of measurements needed to maintain optimized levels of yield is reduced for cost reasons.

2.2.2 California Technology Manufacturing

During the process development phase, Intel uses technology development (TD) organizations to define the manufacturing processes prior to transferring the products and processes to high volume manufacturing fabs. One of these groups is California Technology Manufacturing (CTM) located in Santa Clara, California. CTM includes Intel's 200 mm process development wafer fab, known as D2, where this thesis work was performed. The following section describes D2's primary purpose and role within Intel and CTM.

2.2.3 D2 Charter

The D2 wafer fab has a vision to deliver leading edge silicon processes to accelerate and broaden Intel's competitive leadership. In order to do this, their charter has three distinct goals:

- Develop process technologies
- Ensure successful transfers of new technologies to the virtual factory
- Maintain a stable manufacturing base for rapid deployment of the new products and process technologies to the virtual factory

D2 is one of the few Intel fabs focused on both high volume manufacturing and technology development for new processes. As a production facility, it joins the virtual

factory's attempts to improve yield learning while also helping to fulfill production volume requirements. Because of its dual purpose, there is an important need for resources to focus on the high mix, low volume challenges discussed in the next section.

2.3 A Changing Market

Over the last several years a gradual shift has been realized for an ever-increasing demand of flash products and more variations to the memory product family.

2.3.1 Intel Aggressively Enters the High Mix, Low Volume Market

Worldwide chip sales are projected to increase by 25% in 2004[10] due to the rising popularity of consumer electronic devices such as cellular phones, flat panel televisions, portable music and video players, and wireless home networking. With this surge of increased demand for digital content, the chip designers and manufacturers are placing a high priority on product development projects to enter this business. *Business Week* magazine reports that Walden Rhines, the CEO of chip design software maker Mentor Graphics, "expects chip companies to create 20% to 50% more new versions during the current upturn than in past recoveries."[11] Product development for these new markets is focused on the following four key areas:

- Finding ways to include more functionality onto smaller chips
- Capturing additional market opportunities with improved packaging
- Identifying new types of integrated circuitry
- Improving materials and manufacturing processes

Craig Barrett, Intel's CEO, has created a new plan to include Intel chips in every digital product available on the market. This corporate strategy has been tagged the "Intel Everywhere" plan by *Business Week* in contrast to the previous "Intel Inside"

[10] Kharif, Olga. "A Whole New World of Chips." Business Week Online 21 Jan. 2004. 13 Mar. 2004 <http://www.businessweek.com/technology/content/jan2004/tc20040121_4923_tc139.htm>.
[11] ibid

marketing campaign.[12] "Barrett fully intends to upend the status quo in communications and consumer electronics markets. Think of Intel as the silicon arms dealer."[13]

To meet this challenge, new products for the communications markets are being developed by Intel's research and development fabs. There is "a lot more variety [in chips] than there has ever been," quotes *Business Week* of Brian Matas, an analyst for the semiconductor consulting firm IC Insights.[14] Due to the types and numerous markets ready for entry, each of these new product variations will ultimately be produced in lower volumes than the typical Intel Architecture microprocessor product family. This has and will continue to force Intel's manufacturing environments to deal with a higher mix of products at lower volumes.

2.3.2 Challenges of High Mix, Low Volume Manufacturing

As suggested by the product-process matrix described by Hayes and Wheelwright[15] in 1979, it would be difficult to simply assign high mix, low volume products to Intel's existing high volume manufacturing facilities. This situation requires an analysis of the manufacturing characteristics required to efficiently run a high mix, low volume manufacturing environment. Some of the many problems an existing high volume semiconductor manufacturing facility would encounter when producing components of a high mix in lower volumes are listed below.[16]

- Reduced yield – High volume fabs allow benefits to be gained and improvements to be made over time as learning occurs. When a facility is forced to run a lower volume of many more products, this learning effect cannot be realized (through repetition of running the exact same product over and over) in order to significantly improve the product yield.

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[12] Edwards, Cliff, Moon Ihlwan, and Andy Reinhardt. "What is CEO Craig Barrett Up To? Hint: It's About Much More than Computers." Business Week Online 8 Mar. 2004. 10 Mar. 2004 <http://www.businessweek.com/magazine/content/04_10/b3873001_mz001.htm>.
[13] ibid
[14] Kharif, Olga. "Memory: Beyond Flash and DRAM." Business Week Online 21 Jan. 2004. 14 Mar. 2004 <http://www.businessweek.com/technology/content/jan2004/tc20040121_9640_tc139.htm>.
[15] Hayes, Robert, and Steven Wheelwright. "Link Manufacturing Process and Product Life Cycles." Harvard Business Review 1979.
[16] Scholtz III, Robert L. "Strategies for Manufacturing Low Volume Semiconductor Products in a High Volume Manufacturing Environment." Thesis. Massachusetts Institute of Technology, 2002. 10-11.

- Increased inspection requirements – These low volume products require an increased level of inspection to ensure a high quality product is delivered to the customer.

- Increased setup costs – The higher mix of lower volume products requires extra setups to be performed taking away valuable equipment utilization time.

- Increased number of new product introductions – The new product introduction (NPI) process is designed to optimize the manufacturing environment for a given product when it is first produced at a new facility. This NPI process is time-consuming and resource intensive. With the large amount of products beginning to enter Intel's manufacturing facilities, many more NPIs will result than in recent history, demanding additional time and resources.

2.3.3 HMLV Summary

In summary, Intel has chosen a new strategy to aggressively enter the consumer electronic device and communications markets. Due to the nature of this new arena, several product variations, each of relatively low volume, will be required to meet customer demands. As a result, Intel is now faced with a high volume manufacturing organization that must learn to incorporate high mix, low volume products into its existing manufacturing infrastructure.

CHAPTER 3 – SEMICONDUCTOR MANUFACTURING AND METROLOGY

This chapter introduces the manufacturing processes and complex nature of semiconductor wafer fabrication facilities followed by a review of semiconductor metrology operations.

3.1 Semiconductor Manufacturing

3.1.1 Manufacturing Overview

Semiconductor manufacturing consists of a complex sequence of processes that build three-dimensional structures onto the surface of single-crystal silicon wafers. This manufacturing process includes many processing steps where layers of various materials are deposited onto the wafer for specific reasons. Each layer is then patterned and connected to underlying layers. Figure 3.1 shows a schematic of the typical process flow.

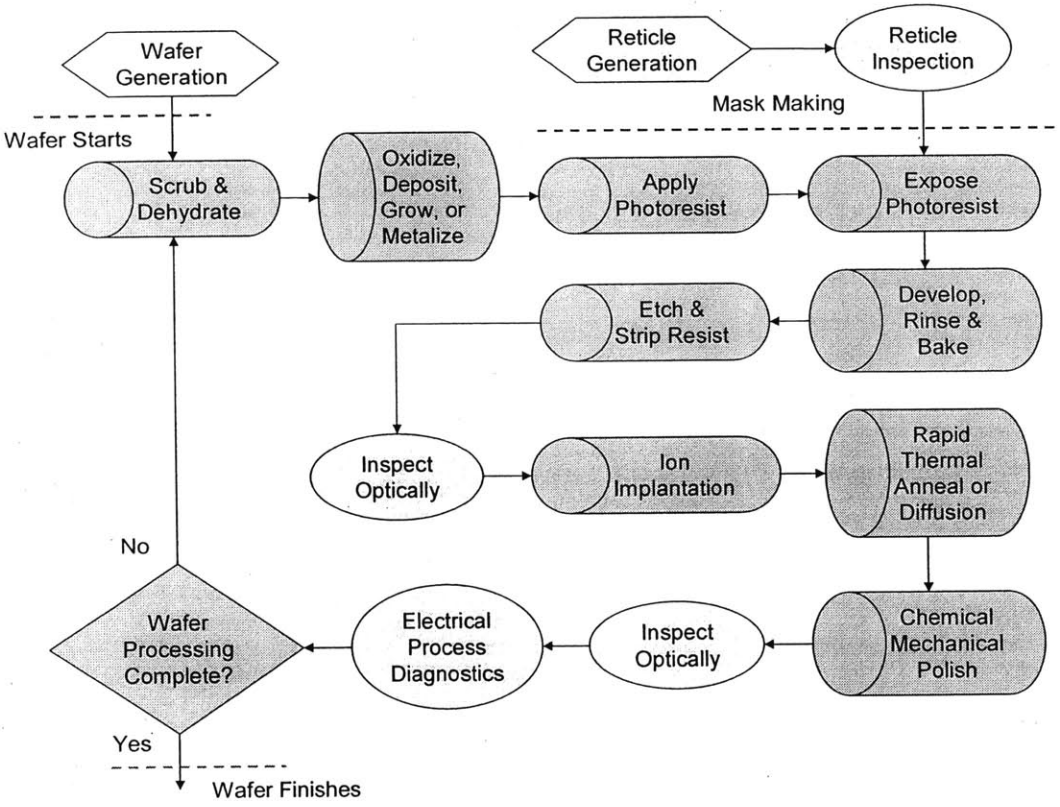

Figure 3.1: Representation of a Typical Semiconductor Fabrication Line.[17]

[17] Adapted from Doering, Robert, and Yoshio Nishi, eds. Handbook of Semiconductor Manufacturing Technology. New York: Marcel Dekker, Inc., 2000. 25.

A sequence of several hundred steps is necessary to complete this highly re-entrant manufacturing process. Figure 3.2 is a schematic of the re-entrant nature of a typical microprocessor product between the six major processing steps. These steps are discussed in more detail in the next section.

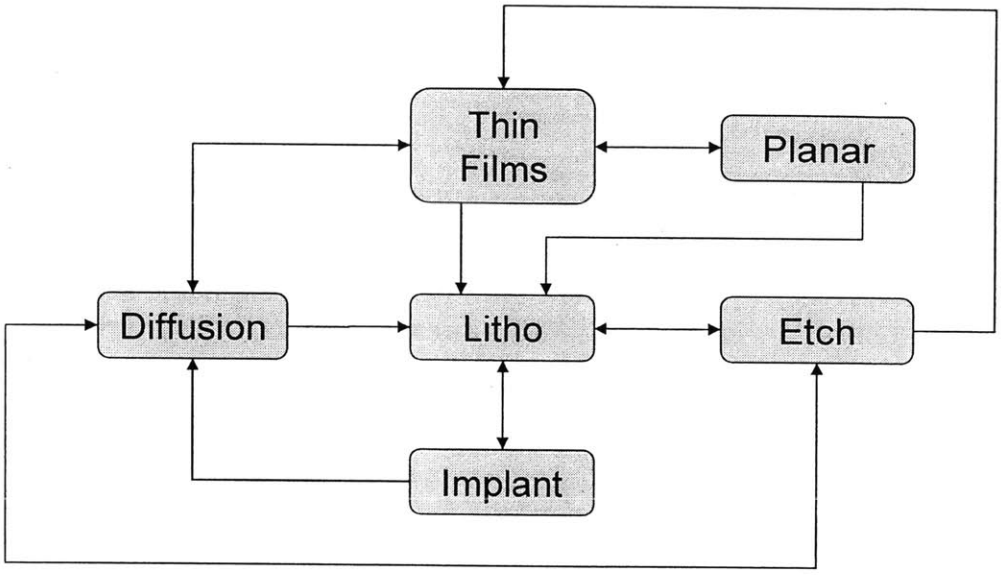

Figure 3.2: Re-entrant Nature of Semiconductor Processing.[18]

3.1.2 Wafer Fabrication Processes and Equipment

As indicated above, there are six primary processes involved with microprocessor production: diffusion, thin films, implant, photolithography (litho), etch, and planar. Each one of these is explained below.

- Diffusion – In the diffusion area, wafers are heated in the presence of reactive gases to grow layers on the wafer surface or un-reactive gases to "drive" implanted materials to their desired depth.

- Thin films – Thin films are deposited onto the wafer surface using chemical vapor deposition, sputtering, or an electroplating process.

[18] Adapted from Quirk, Michael, and Julian Serda. Semiconductor Manufacturing Technology. Upper Saddle River, NJ: Prentice Hall, 2001, 201.

- Implant – In order for silicon to conduct electricity, impurities are implanted into the surface of the wafer by way of the ion implantation process.

- Litho – Patterns are printed onto masks (or reticles) which are then transferred to the wafer surface through the process of spinning resist onto the wafer, exposing the resist using the reticle, and developing the resist.

- Etch – Etching takes place in an acid bath (wet etch) or in an oxygen plasma environment (dry etch). This etching process removes the resist pattern from the wafer.

- Planar – During the planar or polishing steps, chemical and mechanical processing of the wafer removes surface topography ensuring a smooth and flat surface for further processing.

Semiconductor manufacturing is highly technical work accomplished by specialized equipment within a fabrication facility's clean room for minimum exposure to particulate contamination. In advanced fabs, as many as fifty different types of equipment may be necessary to complete this entire process. A brief summary of the major classifications of equipment types is shown in Table 3.1.

Table 3.1: Semiconductor Equipment Types and Applications.[19]

Equipment Type	Application
Deposition	Deposit thin film layer on wafer surface
Etching	Remove thin film layer from wafer surface
Photoresist	Apply photoresistive organic polymer film
Photolithography	Inscribe pattern on photosensitive layer
Resist Development	Remove image from patterned coating
Wafer Clean	Remove unwanted layer or particles
Plasma Etching	Etch underlying layer according to pattern resist
Resist Stripping	Remove photoresist layer of hardened organic film
Ion Implantation	Implant dopants into exposed layer
Oxidation	Grow silicon dioxide layer
Diffusion	Introduce dopants into exposed layer
Chemical Vapor Deposition	Deposit layers of dielectrics, metals, or semiconductors
Sputtering	Deposit layers of dielectrics or metals
Chemical-Mechanical Polishing	Smooth or remove a patterned layer

3.2 Semiconductor Metrology

Variations during the integrated circuit manufacturing process can result in defects in the semiconductor device's performance. At times, these product variations can result in dramatic reductions to a fab's yield. Therefore, manufacturing of integrated circuits includes metrology operations after each major processing step to improve the yield learning cycle (and ultimately, the fab's yield). These metrology steps verify that particle contamination is within certain parameters and product design requirements are being met.

There are two main types of metrology operations studied during the course of this work at Intel's D2 process development wafer fab: photolithography (litho) metrology and defect metrology. Combined, these metrology operations account for roughly 30% of the total number of steps in the manufacturing sequence and

[19] Atherton, Linda F., and Robert W. Atherton. Wafer Fabrication: Factory Performance and Analysis. Boston: Kluwer Academic, 1995. 7-9.

approximately 39% of the cycle time required to complete the semiconductor device.[20] The different types of metrology operations are briefly described in the next two sections.

3.2.1 Photolithography (Litho) Metrology

After the value-add processing step is completed for each litho layer, various problems are identified through four types of metrology operations: macro inspect, develop check, critical dimension verification, and image placement. For most products and layers, all four of these metrology operations are completed resulting in numerous occasions where manufacturing technicians handle the wafers checking for different defect types.

- Macro inspect – During this operation, a metrology technician uses special equipment to rotate the wafer under a monochromatic light to visually detect easily identifiable issues (at the macro level) resulting from the resist processing steps.

- Develop check – An optical microscope is used for the develop check operation to inspect wafers for resist pattern defects or other anomalies only visible under magnification.

- Critical dimension verification – A scanning electron microscope (SEM) is used to measure the critical dimensions of pre-defined features to verify they are within product parameters.

- Image placement – This step (known as registration) determines the amount of overlay between the current layer and an alignment layer underneath. Three common errors are shown in Figure 3.3.

[20] Data taken from a typical product (P8xB) manufactured at D2 in December 2003.

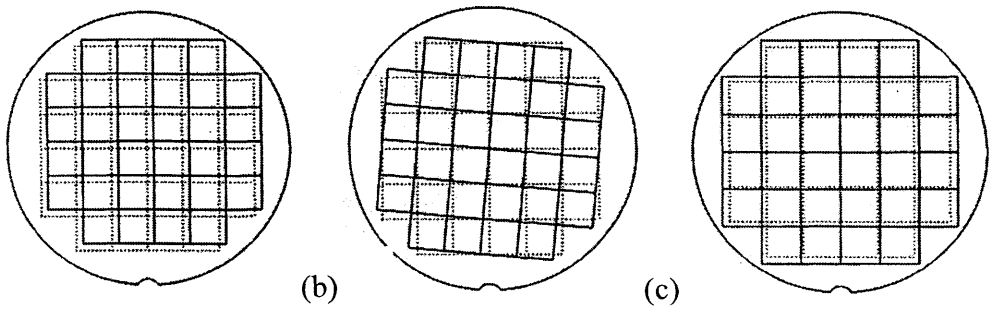

Figure 3.3: Examples of (a) Translation, (b) Rotation, and (c) Magnification Defects.[21]

3.2.2 Defect Metrology

Litho metrology involves identification of errors specifically associated with the photolithography processes such as spinning resist onto the wafer, exposing the resist using the reticle, and developing the resist. This second major classification of metrology, defect metrology, deals with other types of defects that negatively impact product value or functionality leading to lost revenue. These defects can be particles or other imperfections on the wafer that are not intended to be there or any feature missing from the wafer. These defects need to be located as early as possible during the manufacturing process allowing for fewer wafers to be affected, a faster feedback loop for problem resolution, and a lower cost of production.

Typically, either an optical microscope or a SEM would be used to initially inspect wafers and locate the existence of defects such as those shown in Figure 3.4. Defect review tools are also used to further inspect and characterize the nature of unknown material enabling the root cause of the defect to be isolated and contained. The equipment used for defect review is similar to the optical microscopes and SEMs. However, the purpose of their use is to verify that a "detected" defect truly exists and to provide for element classification.

[21] Doering, Robert, and Yoshio Nishi, eds. Handbook of Semiconductor Manufacturing Technology. New York: Marcel Dekker, Inc., 2000.

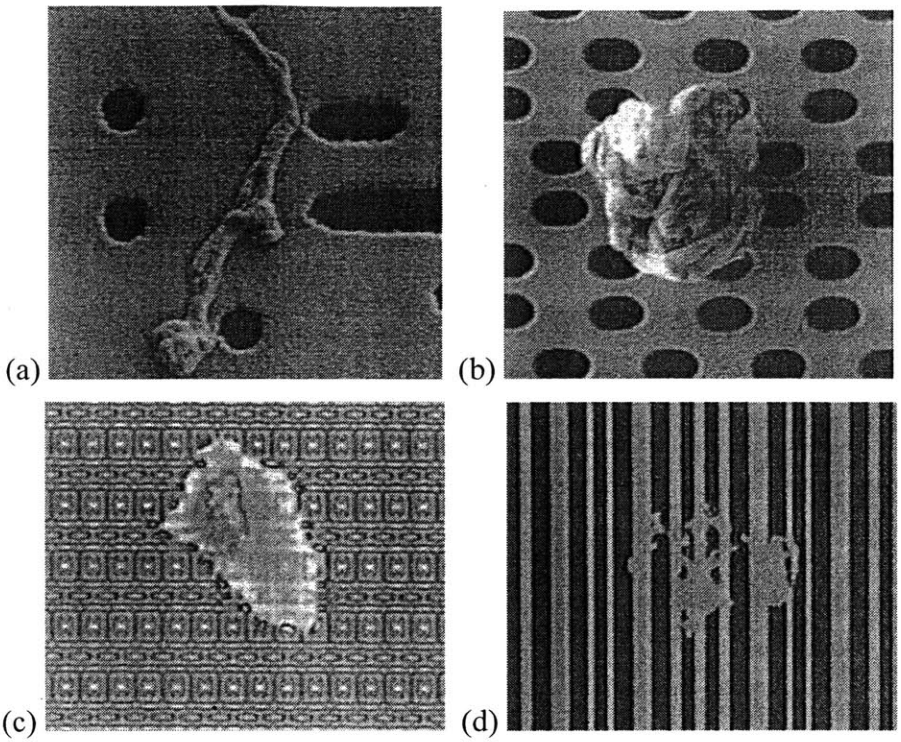

Figure 3.4: Examples of Particulate (a & b) and Missing Pattern (c & d) Defects.[22]

[22] Diebold, Alain C., ed. Handbook of Silicon Semiconductor Metrology. New York: Marcel Dekker, Inc., 2001. 693.

CHAPTER 4 – SAMPLING PLANS

The previous chapter presented an overview of semiconductor manufacturing, its complexities, and typical metrology operations necessary to improve yield learning. This chapter deals specifically with different methods to gather the inspection data while also reducing the impacts these activities have on manufacturing costs and productivity.

4.1 Acceptance Sampling

There are three approaches to the decision-making process regarding product lot quality:[23]

- Accept lots without any form of inspection
- Inspect all lots and remove, rework, or replace defective units
- Implement the use of acceptance sampling for lot quality review

Accepting lots without inspection would typically only be done for those processes that have been consistently proven to be in control over a long period of time. At the other end of the spectrum, all lots may be inspected in those cases where critical product features must be tightly controlled or when the process capability is inadequate to meet specifications. In between, acceptance sampling may be used for the following types of situations:[24]

- When the testing procedure is destructive – making 100% inspection clearly impractical
- When the costs of 100% inspection are relatively high
- When the inspection and analysis process takes a relatively long period of time
- When a reduction from 100% inspection is desired, but the process capability does not warrant zero inspections.
- When product liability justifies continuous monitoring

[23] Montgomery, Douglas C. Introduction to Statistical Quality Control. New York: John Wiley & Sons, 1985. 351-354.
[24] ibid

Intel semiconductor metrology operations fall into the third and fourth categories above. A large amount of time is necessary for some test results to be returned to the technician who is making processing decisions (e.g. continue running the batch under current conditions or tweak the equipment settings to produce a better product). This can result in unwanted equipment idle time adversely affecting fab capacity, cycle time, and costs. Furthermore, due to the increasing shift towards high mix, low volume manufacturing, discussed in chapter 2, efforts have been initiated to reduce the quantity of measurements taken throughout the manufacturing process while still requiring some form of ongoing monitoring.

Many advantages to acceptance sampling plans exist when compared to 100% inspection plans. These include a decreased number of inspections resulting in lower production costs, less metrology labor involvement, and less product manipulation where unnecessary product damage could result. However, there is also an increased opportunity for accepting "bad" lots and rejecting "good" lots. Another disadvantage is that the learning cycle gained from the data collected during the inspection process is slowed due to the reduced number of measurements.

Therefore, the key to gathering data is to do so frequently enough that process changes are captured but not so often that the activity of data collection and analysis is too expensive to be useful. Many different types of inspection methodologies are used within manufacturing operations for the purpose of accepting or rejecting product based on adherence to a standard. Some of the more common acceptance sampling methods are described in the following sections for the purpose of providing context for Intel's acceptance sampling system.

4.2 Lot-by-lot Acceptance Sampling by Attributes

This section explains various types of lot-by-lot acceptance sampling plans using attribute data to classify items as either defective or non-defective based on pass/fail conditions.

4.2.1 Dodge-Romig Sampling Plans

Two types of sampling plans were developed by H. F. Dodge and H. G. Romig that use a set of sampling inspection tables specifically for lot-by-lot inspection: lot tolerance percent defective (LTPD) and average outgoing quality limit (AOQL). The LTPD sampling plan provides protection for the downstream customer in that it involves a risk no greater than the specified amount of accepting any given lot of unsatisfactory quality. AOQL sampling plans are designed for those situations where there is little interest in the quality level of individual lots. Here, protection is provided to the customer in terms of the average outgoing quality for the product over a series of lots.[25] Both of these systems can be developed with the single and double sampling procedures explained in the following sections.

4.2.2 Single Sampling Plan

A single sampling plan is a decision-making process where one sample of n units is randomly chosen from a given lot. An acceptance number c is used to determine the disposition of the entire lot. If more than c defective items are found in the sample, the lot is rejected. Otherwise, the entire lot is accepted for further processing or delivery to a customer.

4.2.3 Double Sampling Plan

A double sampling plan is similar with additional complications. After the initial sample is evaluated, the entire lot is accepted, rejected, or submitted for a second sample. In those cases where a second sample is necessary, the information from both samples is used to disposition the lot. The parameters that define this type of sampling plan are a sample size for the first and second samples (n_1 and n_2), an acceptance number for the first sample (c_1), and an acceptance number for the combined samples (c_2).

If the number of defects observed in the first sample (d_1) is less than c_1, then the lot is accepted. The lot is rejected if d_1 exceeds c_2. In those situations where d_1 is between c_1 and c_2, a second random sample of size n_2 is required. At this point, the lot is

[25] Dodge, Harold F. "Notes on the Evolution of Acceptance Sampling." American Society for Quality Control (1973).

accepted if the combined number of defects observed in both samples ($d_1 + d_2$) is less than c_2 and rejected if it is larger than c_2.

4.2.4 Multiple Sampling Plan

A multiple sampling plan is similar to the double-sampling plan except in the case where more than two samples may be necessary to disposition a given lot. After any stage of the sampling process, if the number of total defects observed ($\sum d_i$) is less than or equal to the acceptance number for that particular stage (c_j), then the lot is accepted. The lot is rejected after any stage of sampling if the total number of defects observed is greater than the acceptance number for that stage. If neither situation occurs, then sampling continues until all stages of sampling are satisfied.

This sampling method is complex to implement but can result in cost savings associated with the sampling process since the sample sizes are typically smaller than single or double sampling plans.

4.2.5 Switching Procedures between Normal, Tightened, and Reduced Inspection

Military standard 105D (or the civilian equivalent ANSI/ASQC Z1.4) provides for different inspection levels based on the specified acceptable quality level (AQL). Normal inspection is used at the start of the measurement activity and under normal conditions where the manufacturing process is producing acceptable results. Tightened inspection levels are required when quality degrades. Reduced inspection can be implemented with exceptionally good product quality.

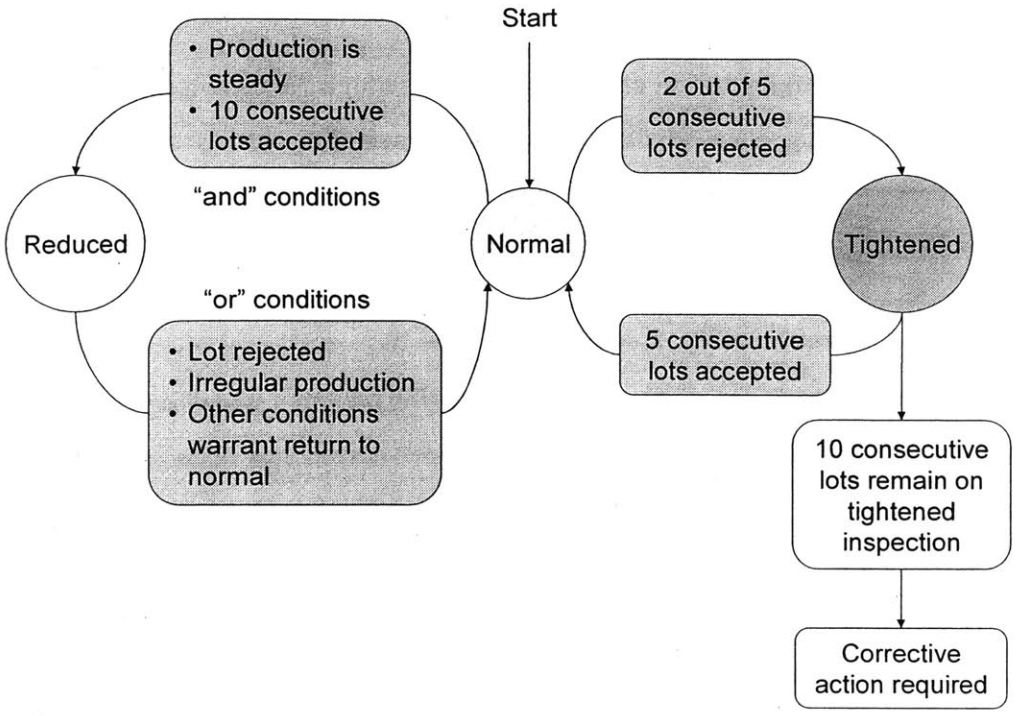

Figure 4.1: Switching Rules for Normal, Tightened, and Reduced Inspection.[26]

The criteria specified in Figure 4.1 are used to determine whether or not it is appropriate to switch from one state to another. For example, when the inspection process is operating under tightened conditions, the observation of five consecutive acceptable lots allows a switch to the normal operating conditions. The difference between normal, tightened, and reduced inspection conditions involves changes to the lot size (n) and acceptance number (c). Full tables specifying these various inspection systems are available in MIL-STD 105D and reprinted in Montgomery (1985).

4.3 Acceptance Sampling by Variables

Variables sampling plans specify the product to be sampled and the criteria for decision-making using measurements to identify the quality characteristics of certain product features. Typically, this is accomplished based on the sample average and sample standard deviation where lot acceptance depends on the sample average in relation to the upper or lower specification limit.

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[26] Adapted from Montgomery, Douglas C. Introduction to Statistical Quality Control. New York: John Wiley & Sons, 1985. 389-392.

4.4 Continuous Sampling Plans

In some manufacturing environments, the natural formation of lots does not exist. Therefore, sampling plans involving continuous sampling versus lot sampling are used for processes consisting of a nearly continuous flow of products. Several different plans of this type are presented below.

4.4.1 The First Continuous Sampling Plan, CSP-1

The CSP-1 plan specifies a clearing interval (i) and a sampling frequency (f). The process includes intervals of 100% inspection alternating with periods of random sampling from the continuous flow of products. During the 100% inspection period, once i consecutive units are found to be free from defects, random sampling at the rate of frequency f begins. When a defect is identified at any point during the sampling stage, 100% inspection resumes. Figure 4.2 shows these alternating periods of 100% inspection and acceptance sampling.

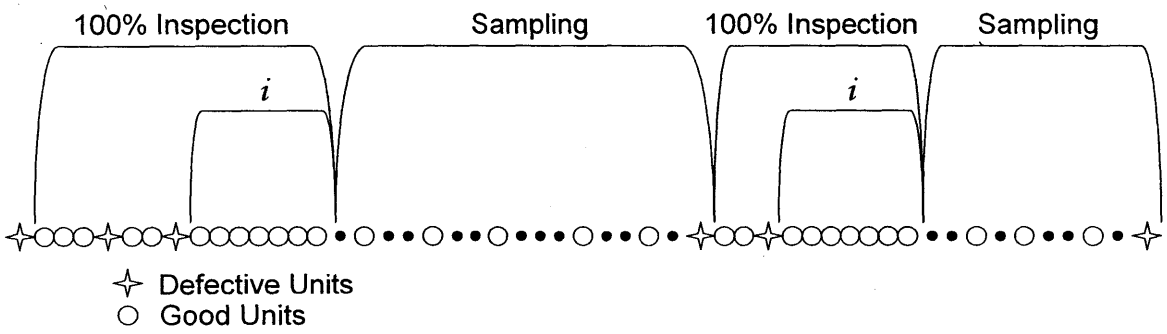

Figure 4.2: Alternating Periods of 100% Inspection and Sampling, CSP-1.[27]

4.4.2 Continuous Sampling Plans, CSP-2 & CSP-3

The CSP-1 acceptance sampling plan explained above requires the return to 100% inspection for any defect identified within the sample. This is equivalent to an acceptance number (c) equal to zero in a single sampling plan. However, it may not always be necessary to take action (such as returning to 100% inspection) when a defect is found. The CSP-2 and CSP-3 plans were developed for these situations.

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[27] Dodge, Harold F. "Notes on the Evolution of Acceptance Sampling." American Society for Quality Control (1973).

Another parameter called the clearing interval (k) is added which allows for sampling to continue as long as multiple defects are not found too close to each other. During sampling, no action is taken with the identification of the first defect. Only if multiple defects are found within k samples, does the process return to 100% inspection. A schematic of the CSP-2 procedure is shown in Figure 4.3.

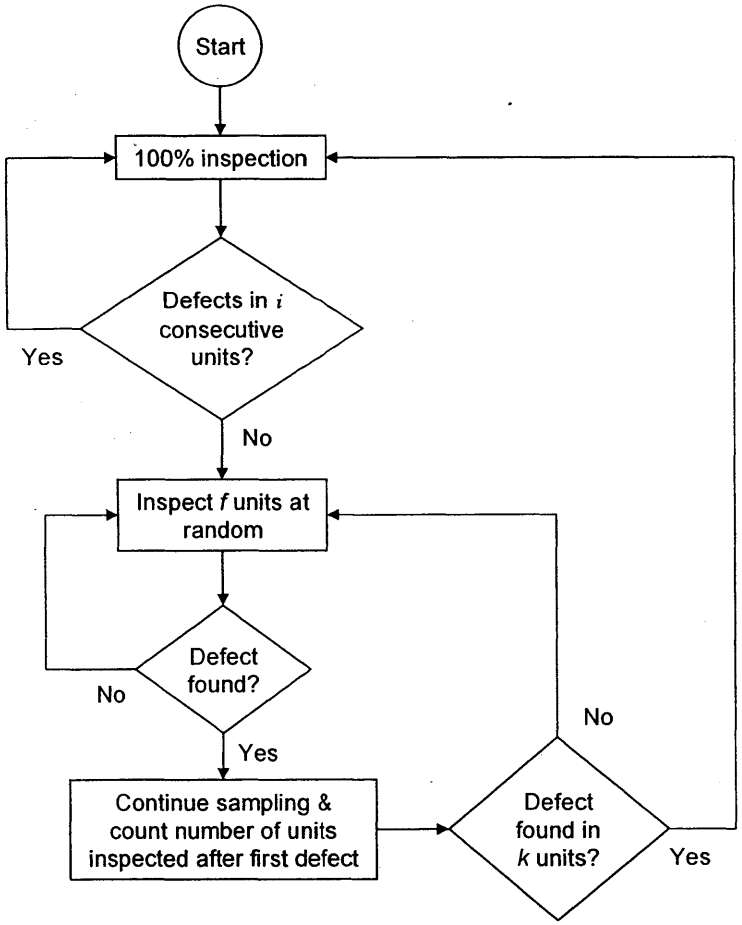

Figure 4.3: CSP-2 Sampling Procedure.[28]

The CSP-3 sampling plan differs slightly from the CSP-2 plan in that it also includes the inspection of the next four units after the first defect is found. If a defect is found within this mini-clearing interval, the process returns to 100% inspection.

[28] Adapted from Montgomery, Douglas C. Introduction to Statistical Quality Control. New York: John Wiley & Sons, 1985. 468-470. and Stephens, Kenneth S. "Volume 2: How to Perform Continuous Sampling (CSP)." The ASQC Basic References in Quality Control: Statistical Techniques. Milwaukee: American Society for Quality Control, 1986. 12.

4.4.3 Additional Continuous Sampling Plans

In addition to CSP-1, CSP-2, and CSP-3, several other continuous sampling plans have been developed and used over time. The more relevant ones are presented here.

- CSP-A plans are based on the CSP-1 concept but includes a stopping rule, identified by parameter *a*. This stopping rule limits the total number of defects that can be found within a production run. When more than *a* defects are found, production and inspection are suspended until the cause of the high rate of defective units is identified and corrected.

- CSP-M, or multi-level continuous sampling, is a continuation of CSP-3 type plans. Multiple levels of successive reductions to the sampling inspection rate (*f*) are allowed after zero defects are found on *i* consecutive units. Successive increases to the sampling rate are required when defects are found. This reduction and increase to the sampling frequency are done exponentially with integer powers of *f*.

- CSP-T, or tightened multi-level continuous sampling, is similar to CSP-M. However, the sampling rate *f* is reduced geometrically by one half when zero defects are found within *i* consecutive units.

4.5 Skip Lot Sampling Plans

Skip lot sampling plans are an extension of the continuous sampling plans reviewed in earlier sections. Basically, these types of plans apply the same methodology described in the continuous sampling section to lots instead of to individual units. They have had extensive industrial application and are very useful in providing for reduced inspections.[29]

Skip lot sampling (SkSP-1) is similar to CSP-1 in its primary plan parameters: the number of lots required to qualify for skip lot inspection (*i*), the fraction of lots inspected during skip lot inspection (f_2), and the fraction of lots inspected during the temporary

[29] Montgomery, Douglas C. Introduction to Statistical Quality Control. New York: John Wiley & Sons, 1985. 476.

interruption of skip lot inspection (f_3). This program consists of three different states shown in Figure 4.4.

- State 1 – Not qualified for skipping, lot-by-lot inspection (100% inspection of lots)
- State 2 – Qualified for skip lot inspection (when some lots pass by or skip inspection)
- State 3 – Re-qualifying for skipping due to temporary interruption

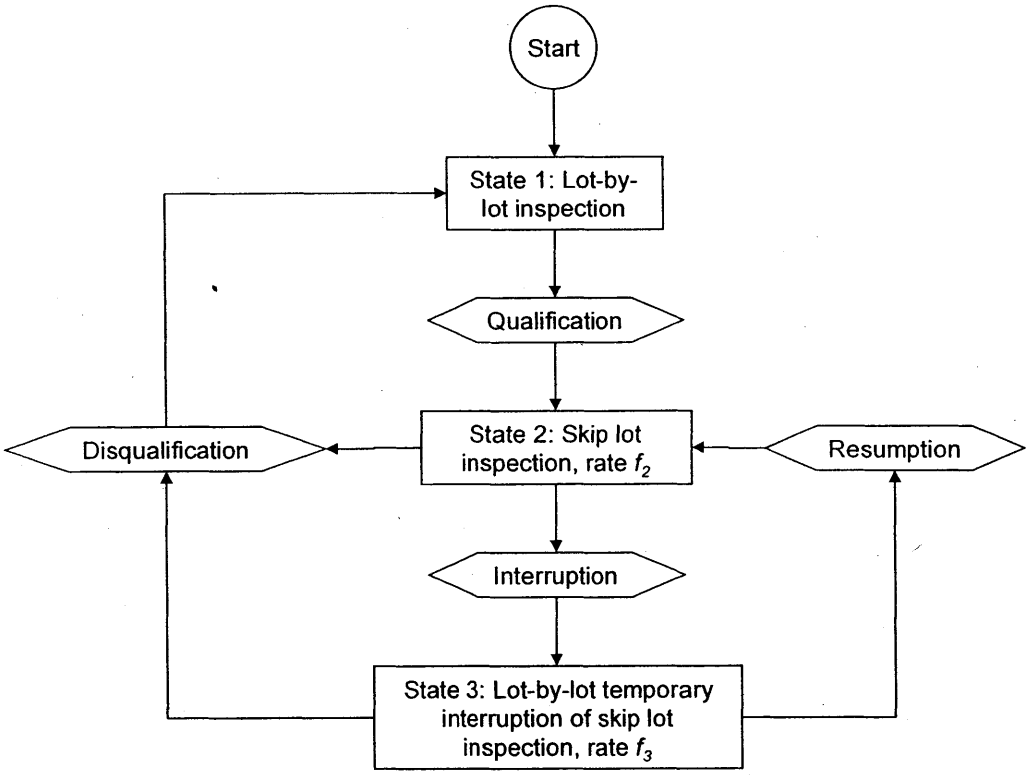

Figure 4.4: The Basic Structure of a Skip Lot System.[30]

At any given time, one of these three states is active. Switching rules protect against accepting "bad" lots while also minimizing the frequency of switching between the states. Once a product has qualified for skip lot inspection by having had i consecutive lots accepted during lot-by-lot inspection, the process is qualified for

[30] Liebesman, Burton S., and Bernard Saperstein. "A Proposed Attribute Skip-Lot Sampling Program." Journal of Quality Technology July 1983: 132.

skipping and enters state 2. While in state 2, the inspection frequency f_2 determines how many lots are inspected. Any rejected lot forces the process to state 3 where the inspection frequency f_3 is used. Regular skip lot inspection resumes with four consecutive accepted lots. Furthermore, when processing from state 2, skip lot inspection is disqualified if two lots are rejected within ten consecutive inspected lots, forcing a return to 100% inspection.[31]

4.6 Intel's Sampling Process

The acceptance sampling plan in place at Intel's wafer fabrication facilities is a combination of skip lot sampling and a variation of the tightened multi-level continuous sampling plan (CSP-T). This system basically works within the parameters of the skip lot program; however, there is a continual change to the fraction of lots inspected during skip lot inspection (f_2).

Using Intel's system, s lots are skipped followed by a single lot that gets inspected. There are three differences between Intel's system and CSP-T. First, the fraction of lots inspected is not geometrically reduced by half for each successfully accepted sequence of i consecutive lots. Instead, the skip rate s is incremented upward by one or more units after every successfully accepted lot. Second, a rejected lot returns the skip rate s back to its minimum value instead of slowly incrementing toward f_2 as defined by CSP-T. Third, random sampling is not performed. Intel uses a very organized approach of "skip s lots, and then measure one."

By increasing the skip rate upward by one or more units, Intel's sampling methodology is much more conservative than both the CSP-M and CSP-T plans. This implies more sampling and inspection will be performed with the Intel skip rate process. Furthermore, the non-random nature of Intel's system exposes the manufacturing process and quality system to errors or other defects that occur with regularity.

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[31] ibid

4.6.1 The SkipLot5 Application[32]

SkipLot5 is the name of the IT application at Intel that gives users the ability to define when lots can skip various metrology operations in the manufacturing process flow. It functions in coordination with Intel's WorkStream system[33] enabling WorkStream users to easily recognize which lots require measurements and which lots may skip the metrology operations. The SkipLot5 application is intended to allow lots to be processed quickly while taking a limited and controlled amount of risk.

In order to use this application, process engineers define a specific amount of risk to be taken based on statistics for a given set of circumstances. Skip rates are assigned based on the process capability (Cpk value). For example, a skip rate of four (measure one, then skip four) would be typical for a product, route, and operation combination having a process capability value of 1.4. The statistics necessary to run the application are then entered into the SkipLot5 database via WorkStream (automatic updates for manufacturing data), the SPC++ system[34] (automatic updates for measurement results), and manual interfaces (data entry and skip algorithm definitions). Based on this data, the SkipLot5 application controls the movement of lots at metrology operations by forcing them to move through or allowing them to skip any given operation.

The SkipLot5 system is a state machine as described in Chapter 4.5. The algorithm starts in state 1 where it will remain until a predetermined number of lots (i_1) are tested and accepted. If any out of control instance is recorded during this period, the counters are reset until another consecutive set of i_1 lots are accepted. At this point, the system switches to state 2. In state 2, skipping is allowed at the minimum skip rate (s_{min}) specified in the database. Once a lot is measured and accepted, the skip rate s increments upward by the rate change unit (r) until the maximum skip rate (s_{max}) is reached. If the result of a tested lot is found to be out of control, the algorithm automatically shifts to state 3. While in this re-qualification stage, if a predetermined number of lots (i_3) are

[32] Intel Corporation. "SkipLot5." User's Guide, 1998.
[33] WorkStream is the manufacturing shop floor application that technicians and engineers use to schedule and process lots within the fab manufacturing environment.
[34] SPC++ is a system that monitors and controls processes in the manufacturing facility. It detects when equipment is operating outside of specified parameters enabling process engineers to be warned of the problem to take corrective action.

tested and accepted, the system returns to state 2 at s_{min}. Otherwise, any out of control lot returns the program back to state 1 where 100% inspection is required.

It should be noted that skip rates, defined by s, and measurement rates, indicated by m, are often interchangeable depending on the purpose of the discussion. It is beneficial to provide a conversion between the two:

$$m = \frac{1}{s_{Average} + 1}$$

Therefore, a measurement rate of 20% results from having an average skip rate of four – measure one, then skip four.

Data within the application is maintained through the use of tables and a user interface controlled by the Information Systems department. Those tables relevant to this document are explained here.

- Test Type table – Table 4.1 provides a sample SkipLot5 test type data table. This table contains the pieces of data necessary to define a given test type including: Qual – the number of lots that must be accepted for the system to qualify for skipping (i_1), ReQual – the number of lots that must be accepted for the system to re-qualify for skipping (i_3), Rate Chg – the rate change interval (r), and the maximum (Max Rate) and minimum (Min Rate) skip rates (s_{max} and s_{min}). The Max Risk data field identifies the maximum number of lots that may be present ("at risk") between the value-add processing step and the metrology operation. The Max Interval column indicates the maximum number of hours that may pass between successive measurements for each given test type. A measurement is forced once either the Max Risk or Max Interval values are exceeded.

Table 4.1: Sample SkipLot5 Test Type Data Table.[35]

Test Type Name	Qual	Re-Qual	Rate Chg	Max Rate	Min Rate	Max Risk	Max Interval
TTN-01	1	1	1	4	1	12	168
TTN-02	1	1	2	4	2	12	168
TTN-03	5	3	1	10	6	25	168
TTN-04	3	3	1	10	6	25	168
TTN-05	2	3	1	10	6	25	168
TTN-06	5	1	1	6	2	12	168
TTN-07	1	1	1	4	1	50	168
TTN-08	1	1	2	4	2	50	168
TTN-09	1	3	2	4	1	50	168
TTN-10	3	1	2	6	2	50	168
TTN-11	1	1	2	4	1	50	168
TTN-12	1	1	1	10	6	50	168

- Decision Point table – A decision point is the reference to a combination of route and operation at which point the decision to skip a metrology operation will be made. These decision points link metrology operations to value-add processing points and are associated with a particular test type. Table 4.2 shows this association between test types (Test Type Name), value-add routes (VA Route), value-add operations (VA Oper), test routes, and metrology operations (Test Oper). Each one of these decision points can be activated or made inactive by way of the column on the far left hand side of the table (A). This active flag allows skipping to be manually interrupted in those cases where known excursions exist in the fab. In these situations, an engineer can deactivate the skipping algorithm for the appropriate decision points in order to force 100% inspection during the length of the excursion. For instance, Table 4.2 shows the fifth entry for value-add route TTN-05 and value-add operation SR-B2 to be inactive since the A column contains an *N* for "not active."

[35] The test type names and test type data have been changed for confidentiality purposes.

Table 4.2: Sample SkipLot5 Decision Point Data Table. [36]

A	Test Type Name	VA Route	VA Oper	Test Route	Test Oper
Y	**TTN-01**	SR-A1	Oper-110	SR-A1	Oper-115
Y	**TTN-02**	SR-A1	Oper-220	SR-A1	Oper-225
Y	**TTN-03**	SR-A1	Oper-420	SR-A1	Oper-425
Y	**TTN-01**	SR-B2	Oper-110	SR-B2	Oper-115
N	**TTN-05**	SR-B2	Oper-220	SR-B2	Oper-225
Y	**TTN-06**	SR-B2	Oper 550	SR-B2	Oper-555
Y	**TTN-07**	SR-B2	Oper-560	SR-B2	Oper-565
Y	**TTN-02**	SR-B5	Oper-120	SR-B5	Oper-125
Y	**TTN-03**	SR-B5	Oper-220	SR-B5	Oper-225
Y	**TTN-04**	SR-B5	Oper-420	SR-B5	Oper-425
Y	**TTN-05**	SR-B5	Oper-550	SR-B5	Oper-555
Y	**TTN-02**	SR-C4	Oper-420	SR-C4	Oper-425

The counters that control the actions of the SkipLot5 system are reset whenever a measurement is out of control, when inventory levels of lots waiting to be measured reach the maximum at risk value, and when the time since last inspection exceeds the maximum allowable time interval. Each one of these events forces the next lot entering the given operation to be measured. There is also the possibility that downtime events, such as preventative maintenance or reticle changes, could force the counters to reset. This changes the skip inspection sequence. This nuance of the system will be investigated in Chapter 5.

4.6.2 The MOST Model[37]

The Monitor Optimization and Sampling Tool (MOST) is an automated model used to optimize sampling frequency for measurements. Most of Intel's wafer fabs use a simple table from the "Monitor Reduction Worksheet"[38] to identify skip rates based solely on process capabilities.

However, a few locations have implemented the MOST model to minimize total sampling costs by balancing excursion costs and sampling costs. The cost of an excursion is calculated using the costs for finished wafers, labor, spare parts, and warranty contracts. The cost of a given sampling plan is a function of many factors

[36] The test type names, value-add routes, value-add operation numbers, test routes, and test operation numbers have been changed for confidentiality purposes.
[37] Intel Corporation. "MOST Concept Presentation." Corporate Presentation, 2003.
[38] Intel Corporation. "Monitor Reduction Worksheet." Statistics Users Group Initial Assessment. 2001.

including the current skip rate, historical percentage of product out of control, and the probability of detecting an excursion. Using this type of data (and more), the model runs hundreds of times and selects the minimal total sampling cost for each simulation. As a result, the MOST model determines optimal skip rates that are then used as the parameters for the SkipLot5 application.

The key differentiator between fabs that use the MOST model and those that do not is that those using the model are optimizing their sampling rates for a minimum total sampling cost. The remaining facilities set their skip rate s based on historical statistical data of their process capabilities. In effect, these facilities are minimizing risk as opposed to minimizing total sampling costs. Both methodologies use the SkipLot5 application to control the implementation and execution of the acceptance sampling plans.

CHAPTER 5 – QUALITY AUDIT

This chapter first introduces the concept of a quality audit. The results of an extensive audit on D2's data, systems, and business processes involved in Intel's acceptance sampling methodology are then discussed. This material serves as a case study for those instances where manufacturing execution systems fail to provide the expected results due to a breakdown in data management, system design, and/or business process execution.

5.1 What is a Quality Audit?

> "Quality Audit – A systematic and independent examination to determine whether quality activities and related results comply with planned arrangements and whether these arrangements are implemented effectively and are suitable to achieve objectives."[39]

The quality audit is a tool that management teams can use to evaluate and analyze their quality systems to either verify their effectiveness or to identify gaps needing improvement. If conducted properly, the results of a quality audit can provide objective evidence about different aspects of a given quality system.

In general, three parties are involved in the audit: the client, the groups being audited, and the auditor. The client is the organization that recognizes the need for a system review and requests the auditor to perform his/her activities.

Two major types of quality audits exist. The suitability quality audit evaluates and compares a quality program against a standard used for reference. The conformity quality audit validates the implementation, execution, corrective action, and follow-up activities against the defined quality program's design.[40]

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[39] Mills, Charles A. The Quality Audit: A Management Evaluation Tool. New York: McGraw-Hill Company, 1989. 1-2.
[40] ibid

5.2 Analysis of the SkipLot5 System

For this particular project, D2's Manufacturing Systems Engineering group within the Operations organization sponsored the effort as the client. The activities performed at D2 were of the conformity quality audit type where repeated, periodic audits were completed to verify continuing compliance and to track improvement progress over time. Furthermore, only the D2 facility was reviewed making this a location-oriented quality audit. Due to the focused nature of the location-oriented quality audit, this technique is very beneficial to analyze the interactions of the various groups and processes involved.[41]

The basis of the project was to determine the causes of several problems identified during a quick analysis performed early in the internship assignment. At that time, the measurement rates experienced within the fab environment for a fairly stable and mature product were much higher than expected. Therefore, the project's goal was to provide a corrective action plan in order to improve labor requirements and cycle time for the metrology areas. This was accomplished by determining the baseline measurement rates, troubleshooting the results, and working with and communicating to the various engineering groups involved in the process. A means for reducing the amount of manual analysis over the long-term was also provided.

5.2.1 Process for the D2 Measurement Rate Analysis

The measurement rate analysis performed at D2 was accomplished by first developing an analysis tool that assisted in gathering the necessary data from several unlinked databases. As a starting point, it was necessary to determine how much D2 was actually measuring relative to the expected measurement rates entered into the SkipLot5 database.

The following is a step-by-step description of the process used to build this analysis tool.

- Select appropriate routes: Identify the routes that carry a majority of the inventory by using information from an inventory-based database. This step limits the analysis to these high volume routes while maximizing the impact of the results

[41] ibid, 33-34.

by focusing only on the active product flows. In high volume manufacturing facilities, this step would probably not be necessary since all products would most likely be included in the analysis.

- Determine operation sequence: Download the sequence of operations for each of these routes. This data provides access to detailed information for the routes of interest. In particular, it is necessary to know the operation numbers, operation descriptions, and the functional areas and clusters assigned to these operations. This information is used in a spreadsheet as the foundation for the analysis.

- Locate the number of wafers processed through each operation: Determine how many wafers were processed by each operation for a given route over the time period of the study. The CTOP database[42] provides the necessary information. After copying only the relevant detail into the analysis spreadsheet, the next several steps can be performed.

- Calculate the measurement rates: Calculate the measure rate percentages for all non-value add metrology operations in the routes of interest.

    - Identify all of the non-value add metrology operations: The route information is filtered using functional area and cluster data in order to isolate those operations assigned to the metrology categories.

    - Identify associated value-add processing steps to determine those operations that trigger the decision points: The decision point tables from the SkipLot5 database are then used to identify most of the processing steps associated with each of the non-value add operations identified above. It is also necessary to rely on experiential knowledge to locate the remaining value-add processing steps and to associate these with the appropriate non-value add metrology operations due to incomplete data in the decision point tables. (This issue will be discussed in subsequent sections.) Finally, the measurement rates are calculated by dividing the number of wafers processed through each

[42] CTOP tracks and records data for manufacturing including such information as the number of wafers processed or reworked and their processing times.

metrology operation by the number of wafers processed through its associated value-add processing operation.

- Troubleshoot results

A simplified sample of the resulting analysis is shown in Table 5.1 for clarification purposes.

Table 5.1: Simplified Measurement Rate Analysis.[43]

Operation Number	Operation Description	Operation Category	Wafers Processed	Measure Percentage	Value-Add Operation
Oper-220	A	Diffusion A1	5141		
Oper-230	B	Diffusion A2	5666		
Oper-235	C	Diffusion Optical	3881	100%	
Oper-420	D	Thin Films B1	5456		
Oper-510	E	Planar E1	5771		
Oper-590	F	Litho L1	6716		--
Oper-595	G	Litho Macro Inspect	6506	**97%**	Oper-590
Oper-605	H	Litho Develop Check	6506	**97%**	Oper-590
Oper-615	I	Litho SEM	6602	**98%**	Oper-590
Oper-625	J	Litho Registration	6279	**93%**	Oper-590
Oper-720	K	Etch K1	6821		
Oper-690	L	Etch K2	6506		
Oper-730	M	Etch M1	6502		--
Oper-810	N	Diffusion P1	7237		
Oper-905	O	Defect Inspect	1575	**24%**	Oper-730
Oper-995	P	Defect Review	525	**8%**	Oper-730

In this sample analysis, it is clearly evident that the litho metrology operations (numbered Oper-595, Oper-605, Oper-615, and Oper-625) are not skipping – due to either their qualification status (not qualified to skip) or inaccurate data entered into the SkipLot5 tables. On the other hand, the defect metrology operations (numbered Oper-905 and Oper-995) are skipping with average measurement rates of 24% and 8%, respectively. For operation number Oper-905, this would roughly correspond to an average skip rate (s) of three – skip three, measure one.

The resulting measurement rates for several routes in multiple product categories were tracked over time using actual performance data from fab operations. In addition, several engineering groups were included in the problem resolution process in order to

[43] The operation numbers, operation descriptions, category names, and wafers processed have been changed for confidentiality purposes.

reduce the measurement rates, where possible, allowing for a reduction of metrology labor requirements.

5.2.2 Measurement Rate Analysis Results Summary

After analyzing the data, it was possible to conclude that approximately 60% of the opportunity for improvement was simply due to incomplete data in the application's database tables. Another 25% of the potential improvements were directly due to correct but inactive entries in the tables. The remaining 15% improvement can be attributed to the method by which skip rates are set at D2. (The D2 facility does not utilize the MOST model explained in section 4.6.2. Therefore, an argument can be made that the intended skip rates are less than optimal requiring additional cycle time and labor to complete the manufacturing process.) These estimates were determined after the engineering evaluation was completed for the P8xA product. Therefore, it was possible to distinguish between those opportunities that were capable of skipping but were not due to data inaccuracies and those metrology operations that were not qualified to skip. The remaining data presented here will discuss those operations qualified to skip but not skipping as expected.

After the initial assessment, it was clearly evident that the D2 facility was not taking full advantage of skip opportunities using the SkipLot5 application. Results of the entire study further reveal this fact. Figure 5.1 displays a summary of the analysis results in terms of percentage of cycle time that could potentially be saved for each of the major product families studied.

In order to develop the results summarized in Figure 5.1, multiple studies were completed for each stable product family running at D2 (i.e. P8xA, P8xB, and P8xC). The process described in Section 5.2.1 was completed. This then allowed for a comparison between the expected measurement rates and actual measurement rates at the individual product, route, and operation level. Differences between the expected and actual measurement rates were then used to calculate a potential cycle time opportunity assuming the expected measurement rates were put into practice. Finally, the data were aggregated by metrology type and product family.

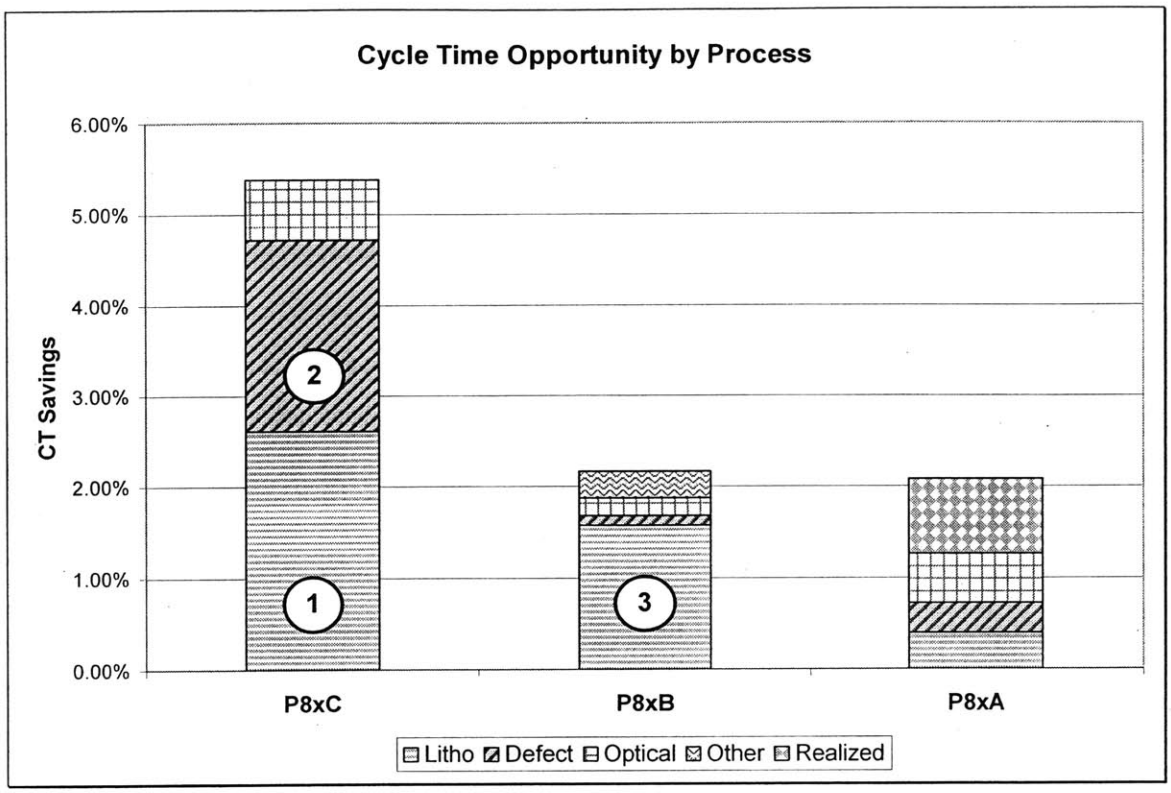

Figure 5.1: Analysis Results in Terms of Potential Cycle Time Savings.

The information in Figure 5.1 exposes the major opportunities for improvement for each of the product families (e.g. P8xA, P8xB, and P8xC) by metrology area. The 5.4% of cycle time that could be saved for P8xC would be a significant improvement to this fairly new, but stable product. The biggest source of potential cycle time savings is attributed to litho metrology (represented by the horizontal stripes) for P8xC. The next two largest opportunities come from defect metrology (represented by the cross-hatching) for P8xC and litho metrology for P8xB. In order to realize this potential cycle time improvement, the inaccurate or incomplete data in the SkipLot5 application that is keeping the route and operation combinations from skipping must be manually corrected in the database tables.

During the third quarter of 2003, an intense effort was conducted to improve the cycle time of the P8xA product. These results can be seen by the 'Realized' category in Figure 5.1 (indicated by the diamond pattern). Here, nearly 1% of cycle time improvement was accomplished in large part due to efforts of many engineers and

metrology personnel to correct data omissions and errors in the SkipLot5 database. The measurement rate analysis completed for this thesis was used to help identify the many metrology operations and routes with unexpectedly high measurement rates and to troubleshoot the potential reasons why this was occurring. Similar efforts for the remaining products and metrology areas will be needed to produce the potential results outlined in Figure 5.1.

The major goals of this project were to improve both cycle time and labor requirements for the metrology areas. The results of this study can also be viewed in terms of labor reductions (reference Figure 5.2). These numbers were calculated in similar fashion to those in Figure 5.1. However, instead of determining the cycle time savings using the difference between the expected and actual measurement rates, labor scripts were used to determine the total amount of time that could be saved. These labor scripts identify the various times it takes to process the difference types of operations. The total time saved is then converted to effective people weeks (EPW) given standard work hours. The resulting Pareto chart shows the priorities for realizing labor savings opportunities: first P8xB litho metrology, second P8xC defect metrology, and finally P8xC litho metrology.

Overall, the labor requirements for products P8xB and P8xC could be reduced by 3.2% and 2.8%, respectively. A total labor reduction of just over 7% was identified for D2. This could be roughly equivalent to $325k of savings for labor costs. However, actual savings were not realized because these man-hours were redeployed to perform metrology functions for the higher priority technology development lots.

These improvements can be achieved through better management of the SkipLot5 database and business processes. Specific recommendations for improvement will be discussed in detail in subsequent sections.

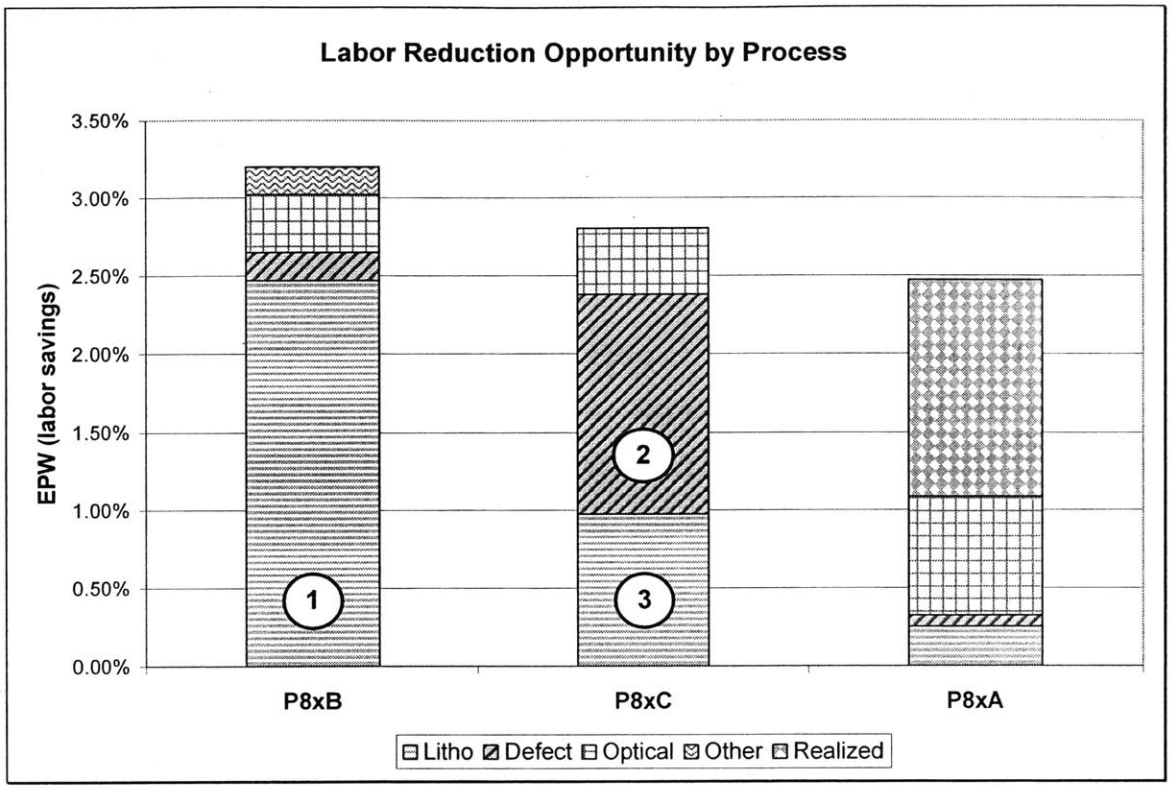

Figure 5.2: Analysis Results in Terms of Potential Labor Savings.

5.3 SkipLot5 System Quality Audit Overview[44]

Several primary challenges with the SkipLot5 application were identified throughout this project. These include the design of the system and its interfaces, the business processes for data creation and maintenance, ownership of the process, and the lack of visibility into the performance of the SkipLot5 application as it relates to activity within the fab.

5.3.1 System Design

As indicated by the analysis results, one of the largest problems deals with data management. Due to the design of the system, the data creation process makes it very difficult to keep the system tables accurate. As indicated earlier, the SkipLot5 application works in conjunction with the WorkStream database. However, the two

[44] This section is provided as an overview of the quality audit results of D2's SkipLot5 quality system. Due to the nature of some of the recommendations, it is not intended to serve as a detailed quality audit final report.

systems run in parallel to each other. Therefore, every time a new route is created in WorkStream, this same data needs to be manually entered into the SkipLot5 application data tables. When route R with metrology operations X, Y, and Z are added to the WorkStream system, new entries need to be manually entered to associate test types to route R and each metrology operation X, Y, and Z with their respective value-add processing steps. In a similar manner, each time a metrology operation or a value-add step referenced by a metrology operation is added or changed in any active route at the facility, it is necessary to recognize this change has occurred and manually update the SkipLot5 system tables.

This issue is especially troubling considering one of the three goals of the D2 facility is to develop processes capable of manufacturing new products with cutting-edge technologies. Therefore, engineers at D2 are constantly investigating better processes by which to produce the desired product. This process development mindset results in dozens of daily changes to routes and operations compounding the inherent problems due to the system design. This situation has caused hundreds of data inaccuracies and omissions reducing the effectiveness of the SkipLot5 system.

5.3.2 Business Processes

Other important factors to consider are the extent to which the business processes are robust enough to overcome the problems outlined above and how well these processes are executed. In order to accomplish the data entry and maintenance steps, it is necessary for several different organizations to work together. At the highest level, representatives from Operations, Equipment Engineering, Integration Engineering, and Metrology Engineering must coordinate their work to determine when a skip rate should be implemented or changed for a given combination of route, operation, and equipment. Forms are then typically completed to indicate the desired change and sent through an approval process to the Information Systems department via an online change request system. The entire process can take several days, if not weeks, to complete. During this time, the metrology technicians in the fab must continue to perform many more measurements than necessary until the pending change request is completed.

5.3.3 Ownership

Moreover, no single group owns and controls this process of analyzing, updating, and verifying data within the SkipLot5 system. The Metrology department does so for some types of tests and measurements. For others, a combination of Functional Area Managers within the Operations department, Equipment Engineers, and Integration Layer Owners is needed to review measurement rates, determine the appropriate action, and request the database tables to be updated. Without this ownership from a single group, the necessary coordination to maintain the data in the system and monitor the SkipLot5 application's performance becomes somewhat more complicated.

5.3.4 Visibility into System's Performance

Performing the manual measurement rate analysis takes a very long time and many labor hours of intense data gathering, analysis, and issue identification. Therefore, a system capable of presenting potential opportunities for measurement rate improvement is needed allowing information to be immediately available to the user.

During this project, the only system available to provide visibility into measurement rates at D2 was a reporting function through a VAX system. These reports show the actual measurement rates and a four-week rolling average for a variety of metrology operations. However, there are two major disadvantages to using this system for measurement rate improvement activities. First, this data comes directly from the SkipLot5 database. Only data entered into the application database tables will be presented here for review. Therefore, any potential skip opportunity that has resulted from missing data in the application data tables would simply not be reported using the VAX reporting function. The analysis results from section 5.2.2 indicate this type of error to be on the order of 60% of the total problem. Of all of the opportunities for improving measurement rates, six out of every ten were due to incomplete data in the database. A large majority of these errors were due to entire routes that were never entered into the SkipLot5 data tables. Hence, this reporting tool was determined to be inadequate due to its data source.

Second, only product-based results are shown. The granularity of the detail can only partition information for a particular product – not individual routes. This, again, dramatically limits the usefulness of these reports for troubleshooting actions since all of the inaccuracies are at the route and operation level. Therefore, the reporting tool could not show the level of detail necessary to identify these routes and operations requiring data updates.

After exploring alternatives to the above reporting tool including investigating the development of a new, stand-alone system, a very useful reporting tool was discovered to already be in use at Intel's Fab 18 in Israel. This system allows the user to select several variables narrowing the output to the desired information. These filters include: level of reporting (i.e. entire fab or specific products), functional areas, routes of interest, and time interval. The resulting report is very similar to the manual measurement rate analysis tool developed for D2 and explained in section 5.2.1.

5.4 Transient Data Study

The review of Intel's SkipLot5 acceptance sampling program was intended to make the necessary improvements to reduce measurement rates affecting both labor requirements and product cycle time. However, the SkipLot5 application is not used in all cases to determine which lots get measured. In some situations, other factors may exist that force manufacturing technicians to perform additional metrology operations. This section deals with the hypothesis that measurement rates can be further reduced by limiting the number of measurements caused by events outside of the SkipLot5 system. The study will be limited to the particular case of downtime events for reticle changes.

5.4.1 Current Practices

Fab specifications require manufacturing technicians to run setup wafers (requiring additional measurements and analysis) if a particular tool does not process a given layer for a few days or if preventative maintenance activities have been performed on the tool. In many instances, there are standing requirements for lots to be measured at the develop check and registration metrology operations after downtime events occur for certain products, layers, and toolsets, regardless of the acceptance sampling system

results. For example, lots from the P8xA product family are required to be measured on 80% of the litho layers after preventative maintenance activities are completed. The study that follows will investigate the need to perform these additional measurements after reticle changes for a particular litho toolset.

5.4.2 The Group Short Run Individual X and Moving Range Control Chart

In order to study the transient effects of data resulting from downtime events, data were gathered from a specific litho tool during the month of November 2003. During this time, three products were processed using this equipment in several runs of many small batches. To change from one product and layer to another, the equipment experiences downtime during the necessary reticle change. Measurement data associated with the lots processed immediately after the reticle changes were identified and studied to determine if any conclusions could be made about D2's policy of measuring the first lot through a tool after a downtime event.

It was beneficial to use the decision tree shown in Figure 5.3 to select the most appropriate control chart for this study. First, five different characteristics were chosen to be monitored for each product: x shift (xS), y shift (yS), x magnification (xM), y magnification (yM), and field rotation (F). These relate to the registration (or overlay) of the image placement from one layer to the next (reference section 3.2.1 on Litho Metrology and Figure 3.3). Next, a subgroup of one unit is used since only the initial lot processed after each reticle change is included in the study. Finally, the five characteristics have the same average target for each product; however, the products were determined to have different standard deviations.[45] This information results in the use of the group short run individual X (IX) and moving range (MR) control chart.

[45] The difference between the product standard deviations was greater than the 30% rule of thumb derived from Fair, Douglas C., and Stephen A. Wise. Innovative Control Charting. Milwaukee: ASQ Quality P, 1998. 51.

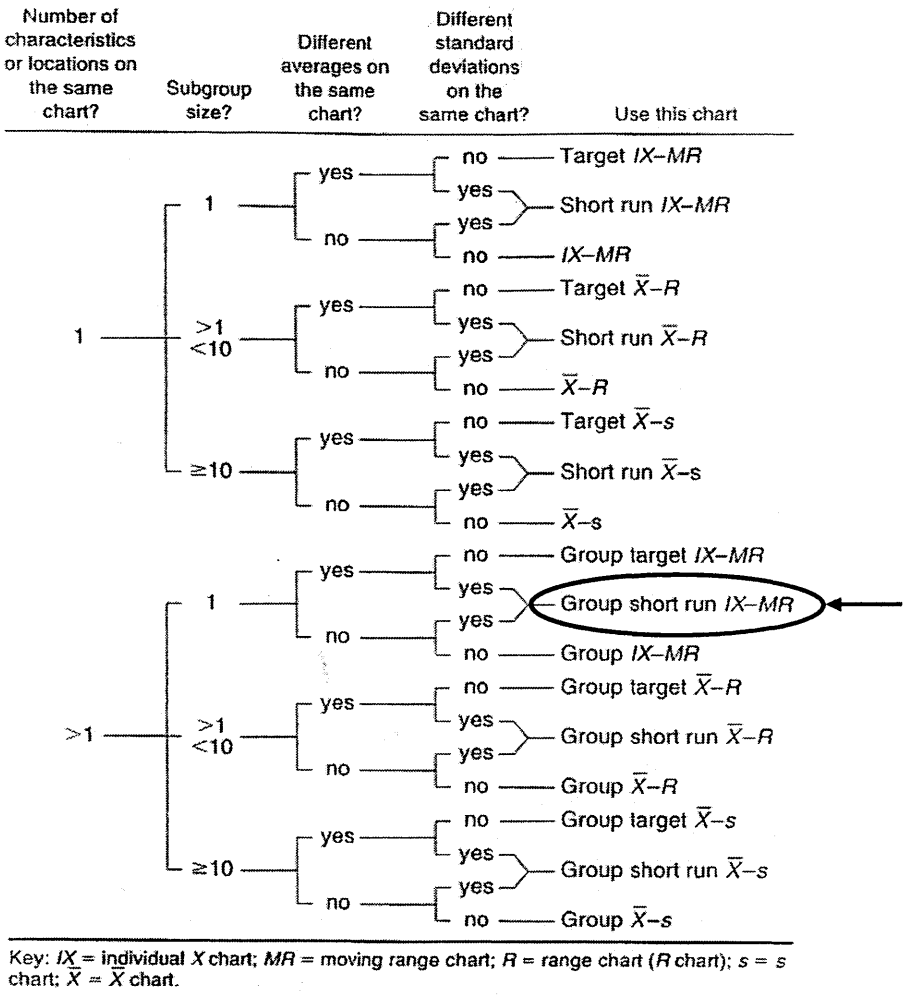

Figure 5.3: The Control Chart Decision Tree.[46]

Since there are three products and five characteristics involved with this transient data study, fifteen basic control charts would be necessary to review and analyze the data without utilizing the group control chart. This translates into additional work, analysis, and review of data. However, a group control chart can be used to evaluate multiple characteristics on the same chart. Group charts are based on the traditional control charts: the individual X and MR (moving range) chart, the $\overline{X}$ and R (range) chart, and the $\overline{X}$ and s (standard deviation) chart. The difference between the basic control charts and the group control chart is that several characteristics, parameters, or process streams can be combined onto the same chart.

[46] Fair, Douglas C., and Stephen A. Wise. Innovative Control Charting. Milwaukee: ASQ Quality P, 1998. 50.

"Group charts are an ingenious method for combining a number of subgroups from different sources in a single simplified chart...the technique used is broadly acceptable."[47]

Changes in individual measurements can be detected through effective use of the group short run IX chart. This method considers each product's target value, average, and standard deviation. The plot points on the IX chart are then transformed into a unitless ratio by subtracting from each measurement the average target IX value ($\overline{IX}$) and dividing the result by the average target moving range ($\overline{MR}$). The following formula describes this calculation for the IX plot points.[48]

$$\frac{IX - \text{Target } \overline{IX}}{\text{Target } \overline{MR}}$$

In a similar fashion, the group short run MR chart can detect changes in the standard deviation of multiple characteristics. This chart plots the moving ranges calculated by the absolute difference between two consecutive IX values transformed by the plot point formula above.

5.4.3 Interpretation of the Results

The process for developing this group chart follows:[49]

- Logically combine data into subgroups
- Calculate the plot points
- Plot and separately connect the maximum and minimum points
- Label each point based on the characteristic causing the maximum or minimum value

Using this process, the group short run IX chart depicted in Figure 5.4 and the group short run MR chart shown in Figure 5.5 are the result.

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[47] ibid, 175.
[48] ibid, 239-252.
[49] ibid, 175-181.

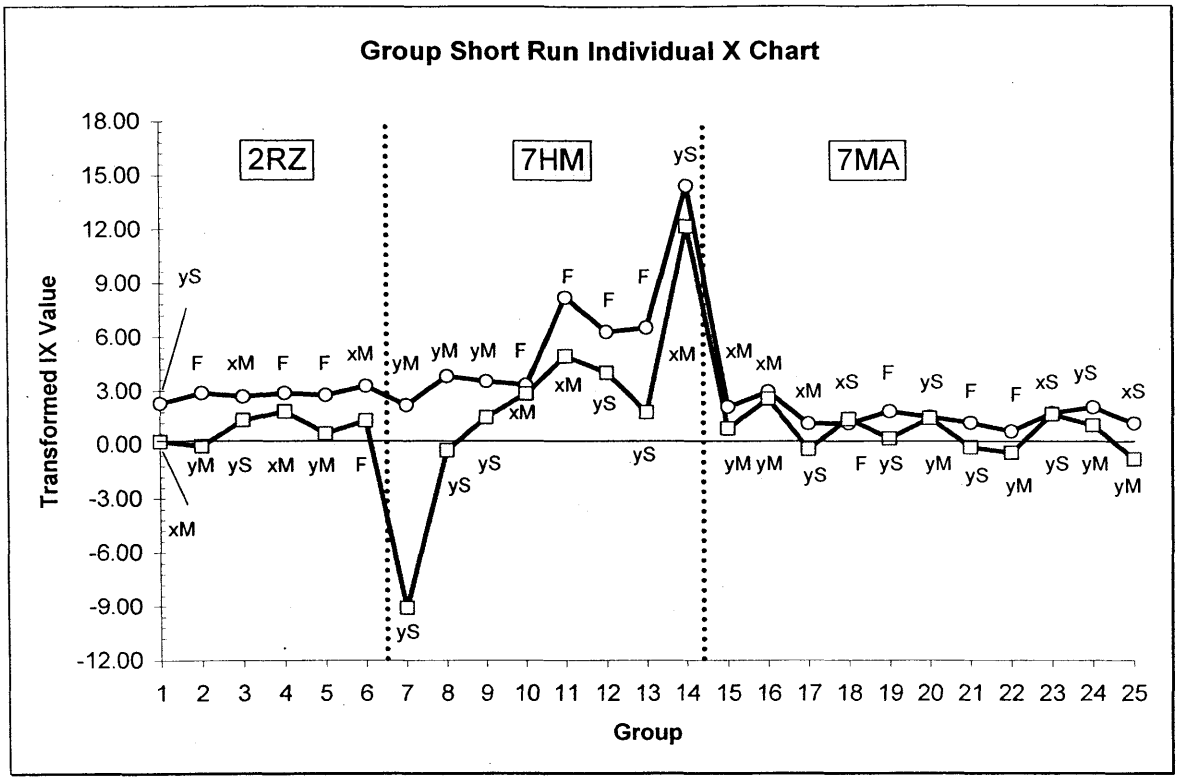

Figure 5.4: Group Short Run Individual X Chart.

Several observations are apparent after review of the group short run IX chart shown in Figure 5.4. The following trends have been identified based upon rules of thumb for identifying issues when characteristics appear in a given position four consecutive instances or with the frequent appearance of any characteristic type at either the minimum or maximum position.

- The y shift (yS) characteristic for product 7HM is in the minimum position five out of eight times. This may indicate that the y shift characteristic for 7HM is generally lower than its target value.
- A possible shift occurred toward the end of the 7HM product subgroup causing the y shift characteristic to become the maximum value – larger than its target value. The y shift characteristic seems to be particularly erratic for the 7HM product family.
- The field rotation (F) characteristic exists in the maximum position for four consecutive plot points for the 7HM product. This run indicates that the average field rotation is greater than its target for this product.

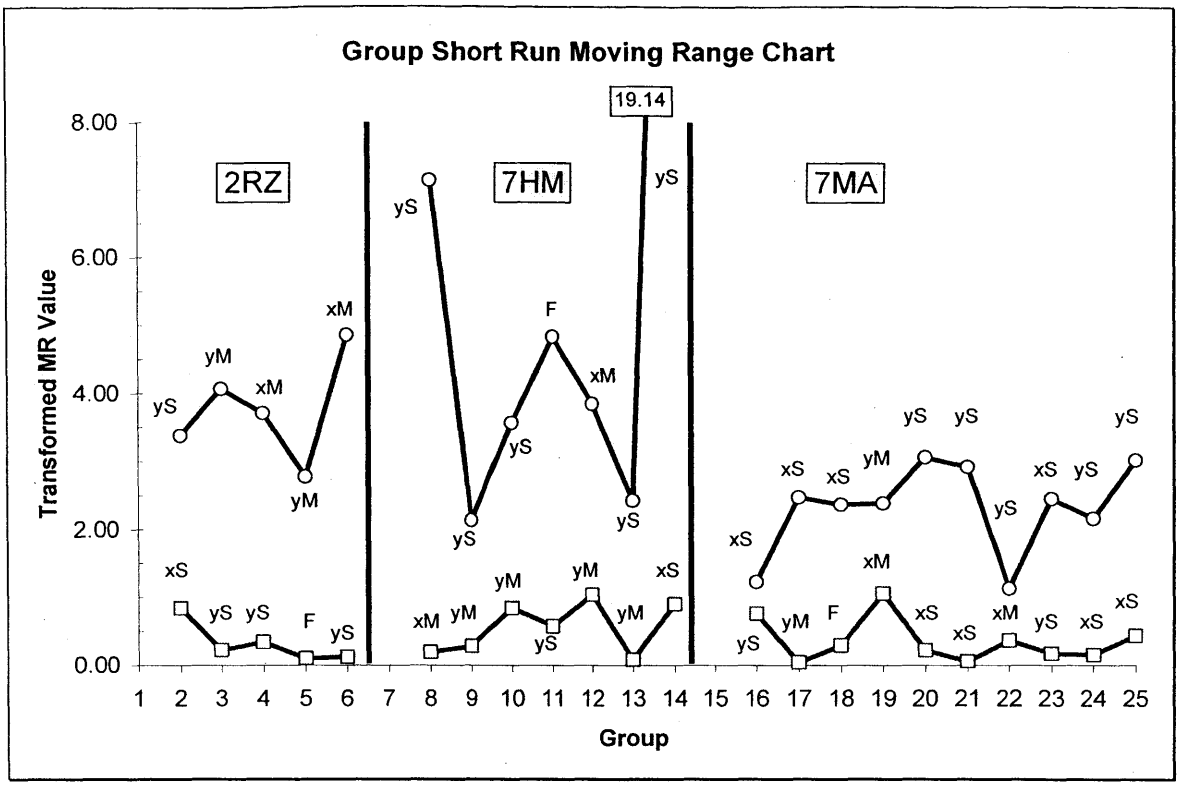

Figure 5.5: Group Short Run Moving Range Chart.

The following observations result from a review of the group short run MR chart shown in Figure 5.5.

- There is a run of four consecutive magnification (xM and yM) plot points in the maximum position for product 2RZ. This indicates that there is significantly more variation in the magnification characteristic for 2RZ.
- The shift (xS and yS) characteristics for product 2RZ are in the minimum position four out of five times. This may indicate that the shift characteristics for 2RZ exhibit the lowest variability of the characteristics being studied.
- The shift (xS and yS) characteristics for products 7HM and 7MA are in the maximum position fourteen out of seventeen times. This indicates that there is significantly more variation in the shift characteristic for these products.
- The magnification (xM and yM) characteristics for product 7HM are in the minimum position five out of seven times. This may indicate that the magnification characteristics for 7HM exhibit the lowest variability of the characteristics being studied for that product.

- The first and last plot points for product 7HM show very large values for the y shift (yS) characteristic. This demonstrates the high variability and process shift discussed for the 7HM y shift values noticed on the group short run IX chart.

Based on data from this analysis, the resulting group short run IX and MR control charts, and the above interpretations, it is suggested that D2 should continue forcing the first lots processed on tools after reticle changes to the registration operations. Of particular concern are the erratic nature of the y shift characteristic for product 7HM, the greater than target field rotation characteristic for product 7HM, the variation of magnification plot points for product 2RZ, and the variation in the shift characteristics for products 7HM and 7MA. Therefore, the hypothesis that measurement rates can be further reduced by limiting the number of measurements caused by events outside of the SkipLot5 system does not seem to be valid for reticle changes. Further study is necessary for those measurements required by D2's policy of measuring the first lot through a tool after preventative maintenance activities.

CHAPTER 6 – ORGANIZATIONAL CHANGE

This chapter provides a reflection on the project experience and evaluates the organization in terms of three lenses: the strategic design lens, the political lens, and the cultural lens (reference Figure 6.1).[50]

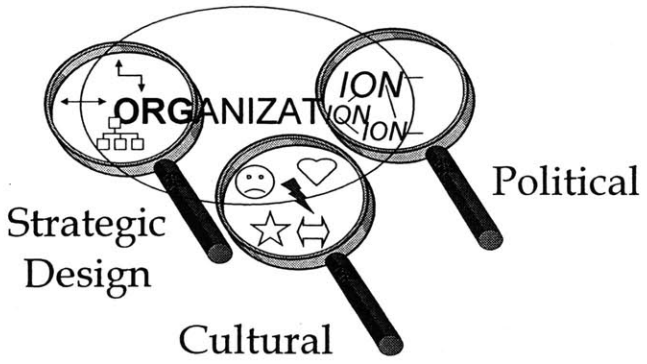

Figure 6.1: The Three Lenses.[51]

6.1 Strategic Design Lens

6.1.1 Organizational Strategy

I reported through Manufacturing Systems Engineering (MSE) during the length of the project. The MSE group reports into the Operations department and is charged with improving velocity or throughput time for products being manufactured at D2. The group does this through the implementation and maintenance of various IT systems. First, this project needed to directly benefit fab operations. Second, as a result of my initial investigations, there was interest to develop a new system that would support the reduction of fab measurement rates and improve visibility of the SkipLot5 application's performance as described in Section 5.3.4.

This project fit into the group's purpose very well. It was intended to improve factory velocity and required the development and implementation of an IT system enabling an ongoing evaluation of Intel's skip lot system.

[50] Chapter 6 is written in the first person tense allowing the author to reflect on his personal experiences and observations related to the three lenses and managing change during the internship assignment.
[51] Carroll, John S. "Introduction to Organizational Analysis: The Three Lenses." 2002. 13.

6.1.2 Organizational Needs

As explained in Chapter 2, the new corporate direction is requiring drastic improvements for manufacturing operations dealing with the increasingly higher mix of lower volume products. The project helped these issues by identifying multiple opportunities where measurement rates could be safely reduced without affecting product quality. As a result, the metrology technicians who were typically dealing with unnecessary steps in the manufacturing process could be refocused on the higher priority technology development lots moving through the fab.

More specifically, at the beginning of the analysis, D2 was falling behind its cycle time goals for a particular product, P8xA. The company was in jeopardy of missing critical customer delivery dates. As part of the corrective action plan, the project outlined in this thesis was given high priority because it was recognized to have great potential of improving cycle times and enabling the fab to meet its delivery dates.

It is interesting to note that the engineering process for updating incorrect or incomplete data in the SkipLot5 application data tables was only completed for one of the three products included in the study – P8xA. At the end of the internship assignment, the opportunities identified by the analysis for products P8xB and P8xC still had not been evaluated by the various engineering departments in order to properly update the SkipLot5 data. Therefore, the potential savings identified for these products were not realized during the internship. Clearly, the P8xA product had a "burning platform" requiring engineers to dedicate time and energy to improve the cycle time metric allowing D2 to meet customer delivery dates. The P8xB and P8xC products had no such impetus driving the engineering groups to evaluate the potential measurement rate improvement opportunities. Therefore, due to this and other cultural reasons, this work did not get accomplished.

6.1.3 Organizational Structure

The Manufacturing Systems Engineering (MSE) and Operations groups were in complete alignment with each other. In fact, they held morning "huddles" prior to the daily Operations meetings in order to ensure alignment.

However, it was much more difficult to get adequate visibility and exposure to other groups not reporting through Operations. Separate engineering managers ran these organizations and either did not clearly see the benefit of their groups being involved in the project or took an ambivalent "wait and see" approach. This organizational structure, coupled with the fact that no single group "owned" the metrics that the project attempted to improve, was detrimental to its progress and results.

6.1.4 Necessary Changes

Due to the infeasible option of dramatically changing the reporting structure of those involved in the project, the appointment of a single person or role as the "Skip Lot Czar" would be very beneficial. Since the Operations group stands to gain the most benefit from this project, it makes sense to identify a person within Operations for this assignment. An Operations appointee would be motivated to continue the data analysis in order to eliminate unnecessary measurements in the fab. Prior to my involvement, there was no visibility to the problem of higher than expected measurement rates. Therefore, it would be advantageous for the facility to have a person in this role focusing on the issues and pushing for improvements on a monthly or quarterly basis.

6.2 Political Lens

6.2.1 Stakeholder Analysis

There were several stakeholders involved with the internship project at Intel's process research and development wafer fabrication facility. The stakeholder map in Figure 6.2 depicts these key individuals. As can be seen by the number of people shown in the map, there were several different organizations involved with the project for a variety of reasons.

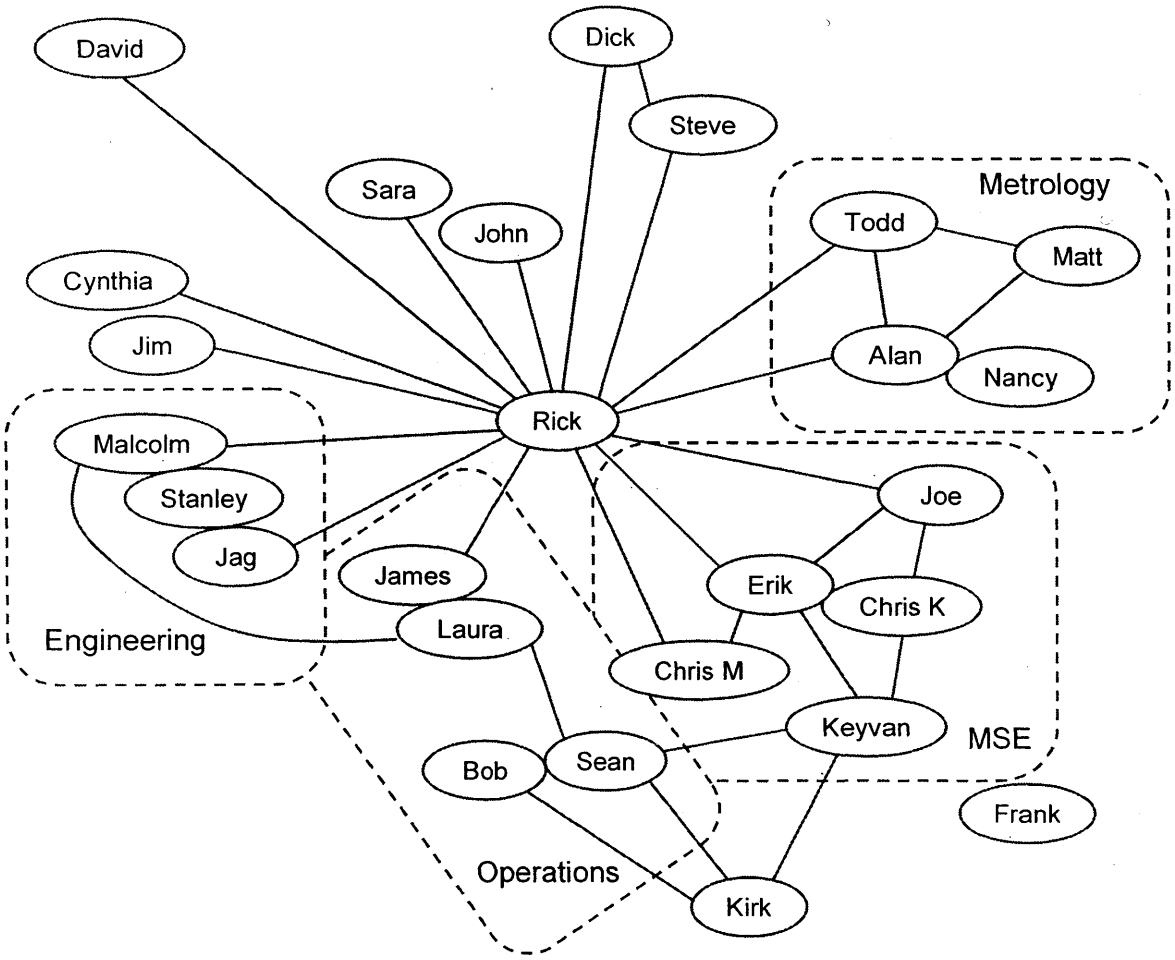

Figure 6.2: Stakeholder Map.

One common theme that can be inferred from the stakeholder map is the fact that there seemed to be little interaction between the different groups (Engineering, Operations, MSE, and Metrology) as far as my project was concerned. This may have contributed to some of the difficulties encountered during the implementation with regards to completing the P8xB and P8xC evaluations and data updating process as explained in Section 6.1.2.

In general, the project encountered only minor resistance from a few employees who realized a successful implementation would increase their workload. This added activity would result from the continual changes and updates necessary to maintain "clean" data within the SkipLot5 database. Many of the remaining individuals were simply too busy with their daily activities to get directly involved in the project.

6.2.2 Conflicts and Resolution

Eventually, the results of the initial analyses were reviewed in a standing meeting called the Velocity Coordination Meeting (VCM). Members from each of the key organizations were invited to attend the VCM to review ongoing projects that would improve cycle time. Time in these meetings focused on this measurement rate reduction project was used to highlight those tasks that needed accomplished to realize the benefits outlined by the analysis. Unfortunately, time in the VCM only created short-term interest in the project.

It was obvious that executive management acceptance and support was going to be necessary in order to compel the entire organization to complete their part of the corrective action plan. The facility Plant Manager gave this needed support during the final weeks of the internship assignment. In the months after the conclusion of the internship assignment, a full-time employee was hired into MSE primarily to continue the measurement rate reduction efforts. This action not only indicates the importance of continuing the analysis efforts but also shows management support for the ongoing project through the increase to MSE's headcount.

6.3 Cultural Lens

6.3.1 Reinforcement of Norms, Values, and Basic Assumptions

This project directly reinforced the norms for Manufacturing Systems Engineering and Operations. The MSE group was charged with creating and maintaining IT solutions that would benefit daily operations and decision-making. Therefore, the project's long-term goal of implementing a web-based reporting tool allowing measurement rates to be clearly evident is in alignment with the MSE group's charter. Along similar lines, Operations continually tries to improve its own metrics such as cycle time and labor efficiency. This thesis project provides these benefits in the short-term and on an ongoing basis.

On the other hand, this project goes against the norms and values for the engineering groups. Since D2 is a process research and development facility, the engineers typically focus their attention on the newest, cutting-edge technologies. It is

understood that these newer technologies require more measurements to increase the learning effect during the products' infancy. However, the project highlighted situations where this single focus on new technology was causing extraneous measurements for the fab with respect to relatively stable and mature products. The opportunities identified point directly to those cases where inaccurate or incomplete data was entered into the manufacturing systems for exploratory, pilot routes. This situation often resulted from an expectation that pilot routes for technology development lots would run a minimal amount of product. In reality, these pilot routes could remain active for several weeks or months producing a large proportion of the facility's production. It is my belief that the engineering groups were reluctant to give the project the credit and attention it deserved due to their focus on developing new products via application of the latest technology.

6.3.2 Information Sharing

During my time at Intel, I realized there was very little sharing of ideas, systems, tools, or methods across organizations and geographies. Intel operates using the well-known "Copy Exactly!" methodology. However, this typically only applies to the equipment, recipes, and maintenance procedures used throughout the "virtual factory." Decision-making processes, reports, and automated IT systems were not common from one facility to the next. For example, D2 developed and used its own tools for tracking inventory and priority lots while other fabs used their own systems. Additionally, access to many internal websites was restricted keeping out all but those that absolutely required the information.

This internship project was evidenced by a lack of information sharing. After working to develop a reporting tool specifically for D2, I (accidentally) discovered that Intel's Fab 18 in Israel had already developed the very tool we were attempting to create. Their version had been running in pilot mode for a full year and had recently been shared with only Fab 17 in Massachusetts and Fab 24 in Ireland. Employees at D2 were unaware of its existence.

I believe the organizational structure at Intel reinforces a culture that prevents the proactive sharing of information throughout the company. Part of this is due to the many locations in which Intel operates. However, in my opinion, the cultural aspect of

every employee acutely focusing on his/her own work leaves little time or reward for sharing knowledge across organizational boundaries. Intel's merit-based, results-oriented policies also contribute to this phenomenon.

CHAPTER 7 – RECOMMENDATIONS AND CONCLUDING REMARKS

This chapter discusses specific recommendations for improvement of the SkipLot5 quality system, one possible future project, and general observations regarding the flow of information within and across organizations.

7.1 Recommendations

Many recommendations were the result of the quality audit performed on Intel's SkipLot5 quality system. Some of these are described below and separated into both short-term and long-term recommendations based on the ease of implementation.

7.1.1 Short-Term Recommendations

Most of the short-term recommendations that resulted from the analysis have been implemented by D2. These ideas enable the organization to continue analyzing and reviewing measurement rates based on the performance of the SkipLot5 application and the associated business processes.

Keeping the analysis results up-to-date and gaining the appropriate amount of visibility in the right forums is very important. Otherwise, those combinations of products, routes, and operations identified as opportunities for improving measurement rates will most likely never get accomplished. To deal with this ongoing (short-term) issue, the Manufacturing Systems Engineering group at D2 has hired a full-time employee primarily to continue the measurement rate data analysis.

As a means to improve the business processes by which data gets created and maintained in the SkipLot5 data tables, the MSE group has been added to the approval process for all route and operation change requests. This additional step in the approval process creates a review specifically intended to ensure that changes made in the WorkStream system also get the necessary updates in the parallel SkipLot5 system. This change in conjunction with the ongoing measurement rate data analysis activities should dramatically improve data completeness and accuracy in the SkipLot5 application. A

few long-term recommendations are also suggested to alleviate the need for this extra review and time investment by the MSE personnel.

Clear ownership and ongoing responsibility for D2's measurement rates is absolutely necessary. Outside of the infeasible option of dramatically changing the reporting structure for those involved in the project, it was recommended that the organization appoint a "Skip Lot Czar" as discussed in Chapter 6.1. This recommendation provides for a single, knowledgeable manager to focus on the measurement rate issues on a periodic basis. It would be this person's responsibility to ensure that the analyses are kept up-to-date and that proper visibility is provided to the problem. Obviously, it is necessary to select a manager with the proper authority and respect within the organization for this role.

Finally, a simpler tool to review the measurement rate data and to identify opportunities for improvement is required. Therefore, it was recommended that D2 implement the measurement rate reporting tool developed by Fab 18 (reference Section 5.3.4 on Visibility). It is expected that this implementation will be complete during the second quarter of 2003.

7.1.2 Long-Term Recommendations

These long-term recommendations are much more difficult to accomplish since they involve complex improvements to the system architecture by the Information Systems organization.

Once the Fab 18 measurement rate reporting tool is implemented and running smoothly, improved productivity can result from additional enhancements to this system. For instance, it is possible to save time involved with identifying potential opportunities for improvement by adding data to the report necessary to make these decisions. For instance, the engineering and metrology personnel use baseline criteria to determine when routes and operations can begin skipping. These criteria can be based on rework or percentages of the amount of out of control product. Whenever these values are beyond the given threshold, no skipping is allowed; therefore, no further analysis would be necessary. By providing this type of data (and integrating with the additional systems

supplying the data), engineers and metrology personnel could immediately recognize those instances that would truly represent opportunities to improve the measurement rates.

The association of processing steps to metrology operations must be manually entered into the decision point tables for every product and route of interest. Therefore, the data maintenance could be streamlined by enabling the use of route wildcards for decision point data table entries. For instance, instead of entering the same association between processing step P and metrology operation M for each individual route in the fab, one entry would suffice by using a route wildcard, processing step P, and metrology operation M. This would dramatically reduce the size of the decision point table from roughly 17,000 lines to approximately 1,200. This is a much simpler group of data to maintain and keep accurate.

As described in section 5.3.1, the WorkStream system and SkipLot5 application are separate systems that run in parallel to each other. This makes it very difficult to keep the SkipLot5 tables accurate. Therefore, every time a new route is created in WorkStream, this same data needs to be manually entered into the SkipLot5 application. Integrating these two systems would greatly improve the cumbersome data creation and maintenance process. Of course, this would take a large effort on behalf of the Information Systems group and business users.

Finally, it would be beneficial for Intel to add a change control process for active flags in the SkipLot5 decision point table. As described in Section 5.2.2, a full 25% of the identified opportunities for measurement rate reduction result from correct but inactive entries in the SkipLot5 tables. Therefore, a closed loop system is needed to ensure that these flags are re-activated once the excursion forcing them to be set to inactive ends.

7.2 Future Project Opportunity

The best opportunity for a future project deals with measurement rate optimization. The analysis project described in this document was an attempt to improve

measurement rates by correcting incomplete or inaccurate data, improving business processes, and suggesting recommendations to enhance the value gained by the systems controlling the process. Once this work is complete, however, benefit can still be realized by implementing a method to optimize the measurement rates used as the SkipLot5 system parameters. Section 4.6.2 describes the Monitor Optimization and Sampling Tool (MOST model) used in some of Intel's fabs to automate the selection of optimal sampling frequencies. A majority of wafer fabs, including D2, identify skip rates based solely on process capabilities. The total cost of sampling and the number of measurements can be minimized by balancing excursion costs and sampling costs. This suggested project would only apply to D2's stable product producing at relatively high volumes. The implementation of this MOST methodology would not be appropriate for products running very low volumes.

7.3 Concluding Remarks

This thesis has dealt with a specific case study at Intel describing a project meant to improve measurement rates for a high mix, low volume process development wafer fab. In general, the information technology application controlling Intel's measurement rates and skip lot system involves inaccurate and incomplete data, outdated system architectural design, and inadequate business processes for data maintenance and performance reporting.

These types of troubles are not specific to only Intel's SkipLot5 application. From this and other experience, general conclusions can be reached regarding management information systems, their system architecture, the data necessary to produce good results, and the business processes used to control these systems. This section reviews some of these general conclusions for information systems and knowledge sharing across organizations.

> "Information is today's key resource...Without accurate information even the most sophisticated plants can only provide a greater quantity of the product least required, at the wrong time."[52]

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[52] Sartori, Luca G. Manufacturing Information Systems. Trans. Frank L. Rossi. Reading, Massachusetts: Addison-Wesley Company, 1988, 1-2.

> "An enormous amount of information is generated and used during the design, manufacture, and use of a product to satisfy customer needs...Thus it is reasonable to suppose that the use of information technology can enable substantial improvements in the operation, organization, and effectiveness of information-intensive manufacturing processes and activities."[53]

Information systems are not always designed and implemented in a manner allowing their intended benefits to be fully achieved. Several common pitfalls occur when a company designs its own software system, modifies an existing system, or implements one ready for installation. The interesting question to consider is "How do these IT systems and their practical applications fail to meet expectations over time?"

The system's architecture is one key to this question. There is a high need for IT systems to allow for rapid changes in products, product mix, transaction volumes, and even unanticipated events such as a facility consolidation or changes in corporate strategy. Without this capability, manufacturing execution systems can quickly become extinct legacy systems that serve as more of an impediment than an enabling tool for productivity, cost, and quality improvements. In the Intel case study, the fact that the SkipLot5 application and the WorkStream system ran in parallel to each other for data creation and maintenance became troublesome for the high mix, low volume product mix evident at D2. Visibility or foresight into tomorrow's uses and business requirements is necessary to better predict possible transformations in the manufacturing landscape and to design systems capable of handling these potential changes.

Another problem area with management information systems is the enormous complexity of these solutions. Often it is necessary to add new systems for specific purposes (e.g. order scheduling and prioritization, materials receipt notification, lot tracking). Each time another IT application is added to the manufacturing environment, it becomes more difficult to seamlessly integrate these solutions and more difficult to deliver the intended results. Every integration point introduces additional opportunities for errors or failures to occur. The system schematic of Intel's fab manufacturing

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[53] Committee to Study Information Technology and Manufacturing. Information Technology for Manufacturing: A Research Agenda. Washington, D.C.: National Academy P, 1995, 2.

execution systems shown in Figure 7.1 is an example of the complex and varied system interactions that can exist in a manufacturing facility. Obviously, this is an extremely complicated IT solution that requires skillful and experienced technicians to maintain and modify as the business climate changes.

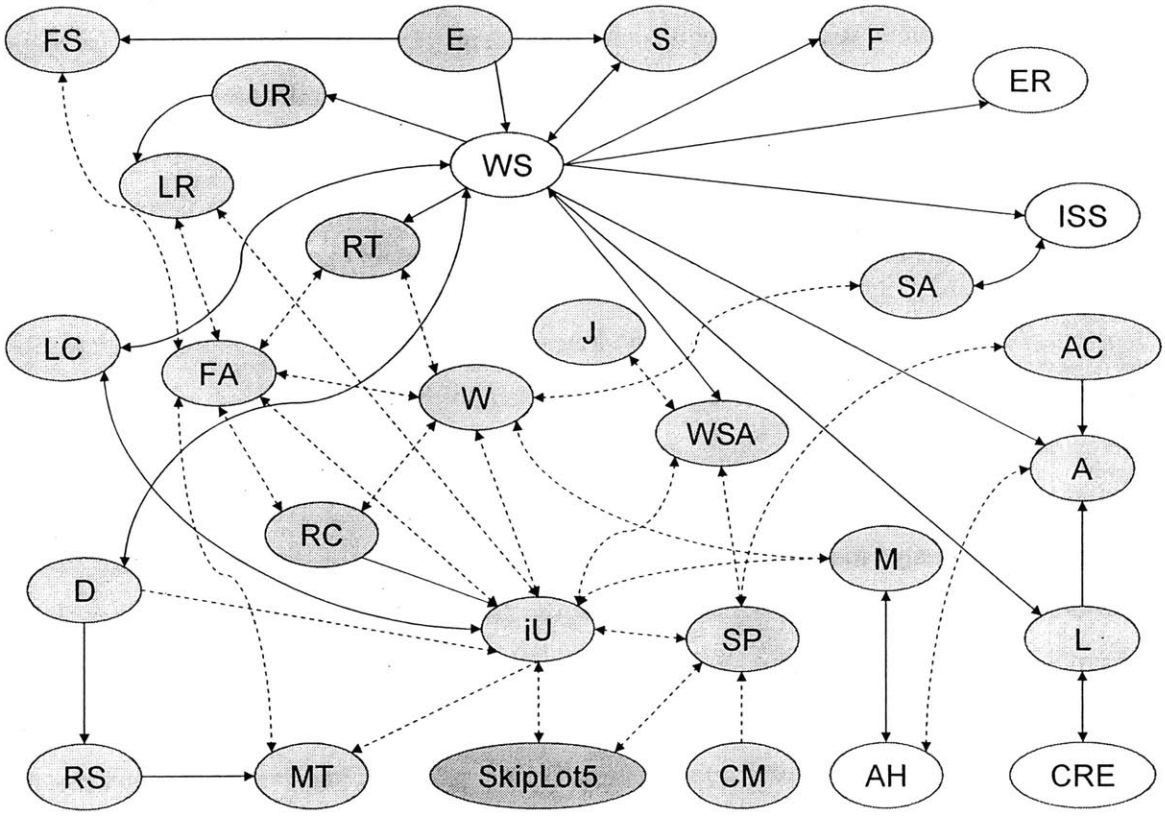

Figure 7.1: Schematic of Intel's Fab Manufacturing Execution Systems.

The previous two topics deal directly with the system architecture of the IT solution in place. On the business process side, it is critical to also have integrity and reliability of the shared data within the IT solution. Any IT application is only as good as the data it contains. Without data integrity, users of the systems may question the output and begin to use their own judgment without regard to the manufacturing execution system. In order to avoid processes that seem to "work around" the system design, it is necessary to ensure the data entered into and maintained within the IT applications is accurate and complete. To do so, the designers of the system must create robust business practices that are easy to follow. This requires active involvement of both information technology personnel and business process experts during the implementation of new systems to guarantee the usefulness of the end product.

In a similar fashion, it is also necessary to have a group or single point of contact acting as the overall business process owner. This system ownership provides the oversight required to recognize errors in the system and to take corrective action. When this ownership does not exist, situations described in the quality audit results summary of Chapter 5 may result where the IT solution fails to deliver its expected benefits.

Finally, it is entirely necessary for multi-national and multi-site corporations to share the knowledge gained through experience from dealing with these IT systems. Having a common system architectural design and a successful best practices exchange program will improve a company's chances of receiving the full system benefits. Lack of knowledge sharing across organizational boundaries can cause disparate solutions to be developed at several facilities all trying to solve similar problems. These situations add complexity to the overall corporate IT solution and waste valuable resources through the duplication of development and implementation efforts.

Contained in this section are a few issues that should be considered when evaluating IT systems in preparation for an effort to change the system landscape. Failing to adequately consider any one of these difficulties could, over time, result in an outcome that is less than desired and fails to meet business requirements.

7.4 Conclusion

In conclusion, there are two main themes addressed in this thesis important to manufacturing operations. The first is the significance of developing and maintaining a robust quality management system. This thesis discusses many of the quality management tools available to gather inspection data while also reducing the impacts these activities have on manufacturing costs and productivity. The key to collecting this information is to do so frequently enough to capture process changes but not so often that the activity of data collection and analysis is too expensive to be useful. This thesis also discusses inspection methodologies that go beyond the relatively simple, commonly used control chart to address more detailed and complex acceptance sampling models.

The second main theme addressed in this thesis is the need for supportive information technology systems. It is critical to use these IT solutions in an effective manner to enable manufacturing operations to continually improve and adjust to dynamic corporate expectations. This thesis reviews the importance of adequately creating and maintaining data within manufacturing execution systems in order to receive the full business benefit expected through the use of these management tools. Furthermore, sharing knowledge across geographical boundaries and business units gained through experience from dealing with these IT systems is vital to the success of manufacturing organizations.

BIBLIOGRAPHY

Amar, Ajay. "Reduction of Process Monitoring in Semiconductor Chip Manufacturing." Thesis. Massachusetts Institute of Technology, 1999.

Ancona, Deborah. Draft manuscript "Leadership in an Age of Uncertainty." Managing for the Future: Organizational Behavior and Processes. Comp. D Ancona, et al. Cincinnati, OH: South-Western College.

Atherton, Linda F., and Robert W. Atherton. Wafer Fabrication: Factory Performance and Analysis. Boston: Kluwer Academic, 1995.

Carbone, Jim. "Microprocessors Show Signs of Life as Demand Builds." Purchasing. 20 Nov. 2003: 17-18. Business Source Elite. EBSCOhost. 15 Mar. 2004. Keyword: Intel market share.

Carroll, John S. "Introduction to Organizational Analysis: The Three Lenses." 2002.

Christopher, Neil. National Institute of Standards and Technology. Technologies for the Integration of Manufacturing Applications (TIMA). 22 May 2003. 17 Mar. 2004 <http://www.atp.nist.gov/www/press/9705tima.htm>.

Committee to Study Information Technology and Manufacturing. Information Technology for Manufacturing: A Research Agenda. Washington, D.C.: National Academy P, 1995.

Diebold, Alain C., ed. Handbook of Silicon Semiconductor Metrology. New York: Marcel Dekker, Inc., 2001.

Dodge, Harold F. "Notes on the Evolution of Acceptance Sampling." American Society for Quality Control (1973).

Doering, Robert, and Yoshio Nishi, eds. Handbook of Semiconductor Manufacturing Technology. New York: Marcel Dekker, Inc., 2000.

Edelstone, Mark L. (4 Mar. 2004). Intel Corp. Fine-Tuning EPS Estimate Lower. Equity Research Note. Morgan Stanley. Retrieved 15 Mar 2004 from InvestText Plus Database.

Edwards, Cliff, Moon Ihlwan, and Andy Reinhardt. "What is CEO Craig Barrett Up To? Hint: It's About Much More than Computers." Business Week Online 8 Mar. 2004. 10 Mar. 2004 <http://www.businessweek.com/magazine/content/04_10/b3873001_mz001.htm>.

Fair, Douglas C., and Stephen A. Wise. Innovative Control Charting. Milwaukee: ASQ Quality P, 1998.

Hayes, Robert, and Steven Wheelwright. "Link Manufacturing Process and Product Life Cycles." Harvard Business Review 1979.

Intel Corporation. "Defect & Yield Basics." Instructor Guide, 2001.

Intel Corporation. (27 Dec 2003). "Form 10-K." Annual Filing with the United States Securities and Exchange Commission, Retrieved 10 Mar 2004, from Thomson Research Database.

Intel Corporation. "From Silicon to Software." Intel's Quality System Handbook, 15 Mar. 2004 <http://developer.intel.com/design/quality/quality.htm>.

Intel Corporation. "Integrated Circuits Manufacturing." New Employee Orientation Program, 2001.

Intel Corporation. "Lithography Area." Photolithography Training Materials, 2003.

Intel Corporation. "Monitor Reduction Worksheet." Statistics Users Group Initial Assessment. 2001.

Intel Corporation. "MOST Concept Presentation." Corporate Presentation, 2003.

Intel Corporation. "SkipLot5." User's Guide, 1998.

Kharif, Olga. "A Whole New World of Chips." Business Week Online 21 Jan. 2004. 13 Mar. 2004 <http://www.businessweek.com/technology/content/jan2004/tc20040121_4923_tc139.htm>.

Kharif, Olga. "Memory: Beyond Flash and DRAM." Business Week Online 21 Jan. 2004. 14 Mar. 2004 <http://www.businessweek.com/technology/content/jan2004/tc20040121_9640_tc139.htm>.

Liebesman, Burton S., and Bernard Saperstein. "A Proposed Attribute Skip-Lot Sampling Program." Journal of Quality Technology July 1983: 130-140.

Mills, Charles A. The Quality Audit: A Management Evaluation Tool. New York: McGraw-Hill Company, 1989.

Montgomery, Douglas C. Introduction to Statistical Quality Control. New York: John Wiley & Sons, 1985.

Ponchner, Karen. "Implementing Advanced Process Control in a Copy EXACTLY! Environment". Thesis. Massachusetts Institute of Technology, 2002.

Quirk, Michael, and Julian Serda. Semiconductor Manufacturing Technology. Upper Saddle River, NJ: Prentice Hall, 2001.

Sartori, Luca G. Manufacturing Information Systems. Trans. Frank L. Rossi. Reading, Massachusetts: Addison-Wesley Company, 1988.

Scholtz III, Robert L. "Strategies for Manufacturing Low Volume Semiconductor Products in a High Volume Manufacturing Environment." Thesis. Massachusetts Institute of Technology, 2002.

Shim, Richard, and John G. Spooner. "Intel Envisions TiVo-like Wireless PCs." CNET News.com 3 Mar. 2004. 3 Mar. 2004 <http://news.com.com/2100-1042-5168666.html?part=dht&tag=ntop>.

Stephens, Kenneth S. "Volume 2: How to Perform Continuous Sampling (CSP)." The ASQC Basic References in Quality Control: Statistical Techniques. Milwaukee: American Society for Quality Control, 1986.