The Effects of Strain on Carrier Transport in Thin and Ultra-Thin SOI MOSFETs

by

Isaac Lauer

B.S., Electrical Engineering
The Pennsylvania State University, June 1999

M.S., Electrical Engineering
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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Thin-body MOSFET geometries such as fully-depleted SOI and double-gate devices are attractive because they can offer superior scaling properties compared to bulk and thick-body SOI devices. The electrostatics of a MOSFET limit how short of a gate length can be achieved before the gate loses control over the channel. In bulk-like devices, the device designer keeps the gate in control with gate oxide scaling and doping profile design. In thin-body geometries, silicon thickness is a new, powerful scaling parameter. Much like with gate oxide scaling, the electrostatics improve with thinner films. This means that the limits of scaling thin-body devices are closely tied with the limits of scaling silicon film thickness.

Electrical transport appears to be one of the limiting factors for scaling body thickness. As the silicon film thickness is reduced into the ultra-thin regime, where the film is thinner than the bulk inversion layer thickness, quantum confinement effects begin to be observed. For the most part, these effects act to degrade mobility, reducing performance and making further scaling less rewarding.

This work focuses on finding methods to maintain good mobility in ultra-thin silicon films. Thin and ultra-thin body relaxed SOI and biaxially strained SOI MOSFETs were constructed and measured with and without the application of mechanical uniaxial strain to examine the interaction between strain and thin-film effects. The band splitting induced by the application of strain is found to at least partially mitigate the mechanisms responsible for degrading electron mobility in ultra-thin films. Additionally, the enhancement seen with uniaxial strain is found to further enhance mobility in biaxially strained films. Finally, the effective mass change caused by uniax-

ial strain is found to cause the mobility modulation to have a directional dependence, especially in already biaxially strained films.

Thesis Supervisor: Dimitri A. Antoniadis
Title: Ray and Maria Stata Professor of Electrical Engineering

Acknowledgments

I would first like to thank my advisor, Professor Dimitri A. Antoniadis for his mentorship and support through the good times and bad. Developing the fabrication process for the ultra-thin devices involved failed lot after failed lot with little apparent progress between them, but Dimitri was patient enough to let me sort out the details and eventually get some good working devices.

I would also like to thank the rest of my thesis committee, Professor Judy Hoyt and Professor Tayo Akinwande. Judy offered a lot of great insights into the physics behind strained silicon that would have taken me a long time to figure out without her help. Tayo always seemed to be able to figure out what I was explained to him before I thought I was finished explaining it, and then ask an insightful question or two about important details I hadn't even thought of yet.

I would like to thank the staff of the Microsystems Technology Laboratory (MTL) for keeping the lab running and helping me with my processing. I would like to specifically acknowledge the staff members I worked personally with: Bernard Alamariu, Dan Adams, Paul Tierney, Joe Walsh, Bob Bicchieri, Eric Lim, and Vicky Diadiuk. I'd also like to acknowledge the computer staff who are definitely under-appreciated for their role in keeping this place running: Mike Hobbs, Bill Maloney, Mike McIlrath, Ike Lin, and Myron (Fletch) Freeman. I'd also like to thank Debb Hodges-Pabon for her job as MTL's "mom" and sanity watchdog.

I feel very fortunate that the list of friends and colleagues I've had at MIT is very long, so I'd like to thank Dr. Andy Wei, Dr. Tony Lochtefeld, Dr. Jim Fiorenza, Dr. Leonard Dvorson, Dr. John Kymissis, Andy Ritenour, Ali Khakifirooz, John Hennessey, Osama Nayfeh, Jae-Kyu Lee, Ryan Lei, Tonya Drake, Ingvar Aberg, Maggie Xia, Cait Ni Cleirigh, Muyiwa Alubuyide, Leo Gomez, Andy Fan, Mark Spaeth, Joyce Wu, Niamh Waldron, John Fiorenza, Dennis WArd, and the rest of MTL. All of these people have had to put up with a lot.

Doing experimental research in the semiconductor field can become very expensive, so I would like to gratefully thank the Silicon Research Corporation (SRC) for funding

me throughout my graduate career. The SRC reviews and conferences have been invaluable for meeting people in my field outside of MIT.

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Chapter 1

Introduction

When I started my graduate work at MIT, the computer I used in my office had a 233 megahertz processor. The computer that I am now typing this thesis on has a 2.53 gigahertz processor, and there are much faster systems currently available. This rapid advancement in computer performance that we have seen over the past few decades is due almost entirely to increasing the performance of the MOSFETs that serve as the switches used to perform the computations. We have been able to scale MOSFETs to smaller dimensions and higher performance at an exponential rate. However, as in all systems, an exponential growth rate cannot be sustained indefinitely. While many have predicted the immediate doom of MOSFET scaling only to be proven wrong, we all know it is coming. It is just more difficult to predict when that will be because many billions of dollars are invested in ensuring that it won't be soon.

This thesis is one of many that looks at the ultimate limits of MOSFET scaling and what we can do to prolong it using unconventional means. Specifically, I have investigated the relationships between strain and film thickness to carrier transport in silicon. I have built long-channel thin and ultra-thin body MOSFETs on SOI and biaxially strained SOI substrates. I then studied their response to mechanical uniaxial strain. Analyzing the results gave me a better understanding of the effects of strain, quantum confinement in ultra-thin films, and their interaction. Armed with this knowledge, I have made some comments on the scalability and transport characteristics of the materials I have studied.

1.1 Overview of this Work

Chapter 2 reviews background information on electrostatics and transport in strained and unstrained silicon MOSFETs. The electrostatics of thin-film devices are briefly reviewed as motivation for studying the physics of transport in sub-10 nm films. Transport theory for ultra-thin films and biaxially-strained films is reviewed, and the effects of uniaxial strain on carrier effective mass are described.

Chapter 3 presents the experimental procedures used to fabricate and characterize the devices examined in this work. Local channel thinning, Kelvin MOSFETs, and the application of uniaxial strain by bending are covered.

Chapter 4 presents device characteristics for thick body strained SOI devices, confirming that mobility enhancement is maintained through device processing and that the strained silicon thickness is not as limited as in the strained silicon / silicon germanium system.

Chapter 5 shows the effects of applying uniaxial strain to various Si material systems for both NMOS and PMOS devices. Mobility is measured in thin and ultra-thin SOI and strained SOI MOSFETs while uniaxial strain is applied either parallel or perpendicular to the direction of current flow.

Chapter 6 concludes the thesis by examining the results of this work in the context of CMOS manufacturing. Film thickness scalability and carrier transport are commented upon.

Chapter 2

Theory

This chapter provides background material and motivation for studying carrier transport in ultra-thin and strained silicon MOSFETs. A brief overview of the electrostatic advantages of thin-film devices is given. Then, the dependence of short-channel effects on film thickness is presented to show that for deeply-scaled devices, ultra-thin films are required.

Next, carrier transport theory is reviewed. The mechanisms that degrade mobility in ultra-thin films are presented. This degradation of mobility motivates the study of techniques that improve mobility and their applicability to ultra-thin films. To alleviate the degraded mobility in ultra-thin films, the enhancement of mobility with biaxial and uniaxial strain is considered. The current theories for the mechanisms of strain enhancement of mobility are presented. These theories provide physical insights to the experimental results obtained in later chapters.

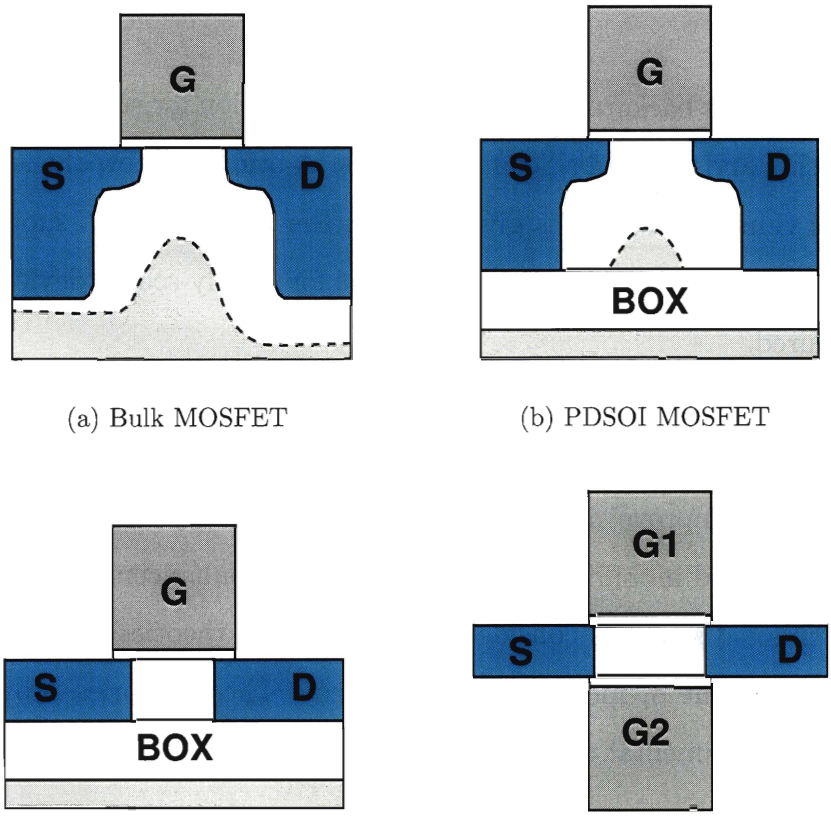
2.1 Electrostatics

Current commercial applications of MOSFET technology rely on bulk and thick-film SOI devices. Transitioning from these types of devices to those based on ultra-thin silicon films would require significant investment in process technology and circuit design. However, it appears that the added scalability benefits may make such a transition desirable. This section compares and contrasts different MOSFET geome-

tries to motivate study in ultra-thin silicon based devices.

2.1.1 Types of MOSFETs

There are currently four general approaches to MOSFET fabrication of logic CMOS. These approaches are: Bulk CMOS, partially-depleted (PD)SOI CMOS, fully-depleted (FD)SOI CMOS and double-gate CMOS. Other approaches are usually derivative of these main approaches. A schematic cross-section view of each type of device is given in Figure 2-1.



(a) Bulk MOSFET

(b) PDSOI MOSFET

(c) FDSOI MOSFET

(d) Double-gate MOSFET

Figure 2-1: Cross-sectional schematics of different logic MOSFET geometries.

Bulk and PDSOI devices scale in a similar manner. PDSOI has the advantages of isolation between the bodies of different devices and reduced parasitic capacitance at the expense of floating body effects. Both technologies are now widely used in industry, but further scaling of these devices is becoming difficult rapidly.

FDSOI CMOS is similar to PDSOI CMOS, except the SOI film thickness is reduced to the point that the entire film is depleted. In this case, floating body effects are nearly eliminated [1]. However, FDSOI can have poorer scaling potential than bulk because of the lack of screening from the back of the channel unless the film is kept very thin [2]. Also, threshold voltage is strongly dependent on the SOI film thickness which is too thin to be well controlled within the tolerances used to fabricate bulk and PDSOI devices. However, for studying transport in thin films, these are the simplest devices to fabricate and as such are the basis of the experimental results in this thesis.

Double gate CMOS has shown the highest potential for scaling. The channel is controlled from either side, leading to increased electrostatic integrity and suppressed short-channel effects [3]. In fact, the lower vertical electric field in the channel further increases drive current by decreasing the degradation of mobility due to scattering at the gate oxide interface [4]. Additionally SOI film thickness for double-gate can be approximately twice that of FDSOI due to the channel being controlled from either side.

Similar to double gate devices are tri-gate [5] and surround-gate [6] devices. Their operation is similar to double gate, but they can tolerate a slightly greater film thickness. The channel thickness in a cylindrical surround-gate structure can be approximately 35% higher than that of double gate [7], while tri-gate devices fall between double-gate and surround gate.

2.1.2 Electrostatics in Thin Film SOI Structures

One important similarity between the FDSOI structure and the double-gate structures is the reliance of electrostatics on silicon film thickness. By thinning the silicon film, the drain to channel junction capacitance is reduced, which improves short channel effects. The results of some simple simulations are provided here to illustrate the effects of scaling film thickness.

V_T roll-off is defined as the difference in threshold voltage between a long-channel device and a short-channel device. The effects of silicon film scaling on V_T roll-off

are shown in Figure 2-2. The V_T roll-off has an approximately linear dependence on film thickness.

Drain-induced barrier lowering (DIBL) is defined as the difference between the equilibrium threshold voltage of a short channel device and its threshold voltage at some high drain potential. DIBL is often given in units of mV/V where the V_T shift is normalized by the drain potential applied. Since DIBL is often nonlinear, the normalization may be misleading, and DIBL is defined here as $V_T(V_D=1.0V)$-$V_T(V_D=0.1V)$. The effects of silicon film scaling on DIBL are shown in Figure 2-3. DIBL has a strong dependence on film thickness, and for short gate lengths, small changes in channel thickness have a large impact on DIBL.

The subthreshold swing of a device is a metric of how well it turns off. The subthreshold swing is defined as the inverse slope of the $\log(I_D)$-V_G curve in the region below the threshold voltage and is given in units of mV/decade. The effects of silicon film scaling on subthreshold slope are shown in Figure 2-4. Like DIBL, subthreshold slope has a strong dependence on film thickness, but for sufficiently thin films subthreshold slope becomes less sensitive to the film thickness.

DIBL appears to be the most demanding requirement on silicon film thickness. In these simulations, when a silicon film thickness is chosen such that DIBL is kept below the value specified by the ITRS (International Technology Roadmap for Semiconductors) high-performance worksheet [8], subthreshold slope and V_T roll-off meet or exceed ITRS requirements.

From these plots it is clear that to have good electrostatics in very short devices it is necessary to scale the film very thin. For the FDSOI case presented in these simulations, the film thickness needs to be less than one third of the gate length. For a double-gate structure, the thickness can safely be increased to about one half of the gate length [1]. It is clear that maintaining electrostatic integrity in deeply scaled devices of this type requires very thin films.

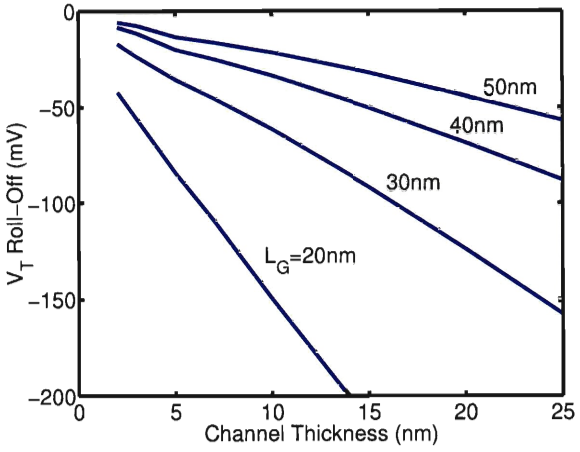


Figure 2-2: V_T roll-off vs. T_{Si} for a FDSOI device. T_{ox}=1 nm.

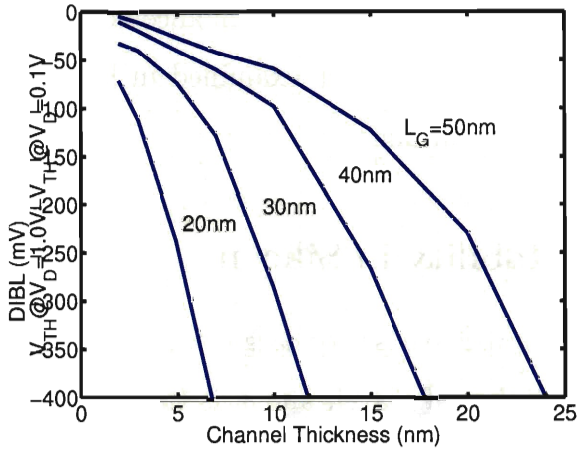


Figure 2-3: DIBL vs. T_{Si}. for a FDSOI device. T_{ox}=1 nm.

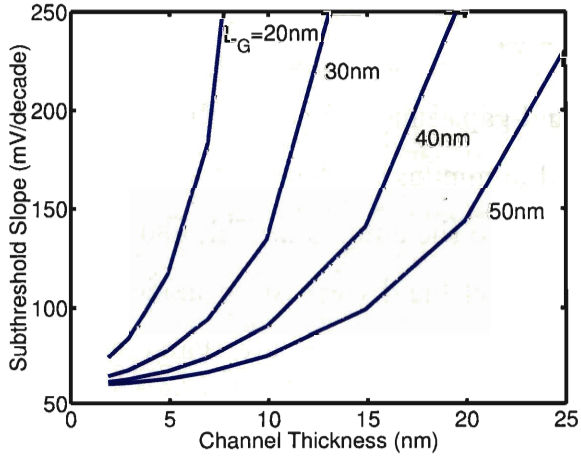


Figure 2-4: Subthreshold swing vs. T_{Si} for a FDSOI device. T_{ox}=1 nm.

2.2 Transport Theory

While electrostatic concerns would suggests that it would be advantageous to use the thinnest film possible, mobility suffers as the film gets thinner. This tradeoff limits the performance benefits of further scaling gate length of ultra-thin silicon devices below the point at which the silicon of the required film thickness begins to exhibit lower mobility.

This section reviews carrier transport theory. Electrons will be considered first, and the differences for holes will be summarized afterwards. Some introductory material is reviewed to explain mobility in a MOS inversion layer. Then, the current theories for the mobility degradation that occurs in ultra-thin silicon films are explained. Finally, the mechanisms of mobility enhancement with biaxial and uniaxial strain are also covered because they are examined in later chapters as methods of improving mobility in ultra-thin films.

2.2.1 Electron Mobility in Silicon

Mobility is defined as $|\frac{q\tau}{m^*}|$, where q is the charge of the carrier, m^* is the effective mass of the carrier in the direction of travel, and τ is the mean time between scattering events for that carrier. The parameters that can be changed to influence mobility are effective mass and scattering rates.

Electron Effective Mass

Silicon is an indirect band-gap semiconductor with a band structure given in Figure 2-5. The conduction band minimum is offset from the Γ point in k-space, and appears parabolic for energies close to the minimum. This allows the constant energy surfaces of just above the conduction band edge to be modeled by six ellipsoids as shown in Figure 2-6. The pairs of ellipsoids (N) are characterized by Equation 2.1. Each ellipsoid is defined by three effective masses, m_x, m_y, m_z, which are given by $m_\ell = 0.92m_0$ in the longitudinal direction and $m_t = 0.19m_0$ in the other two, where m_0 is the free electron mass (9.11×10^{-31} kg).

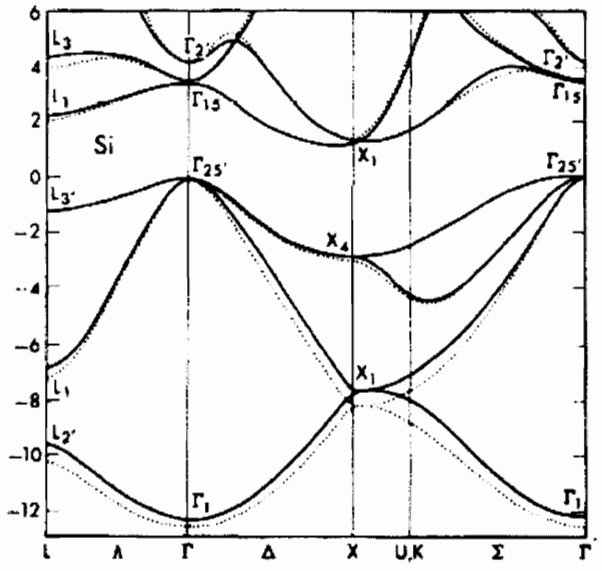


Figure 2-5: Band structure of silicon[9].

$$E_N(\mathbf{k}) = E_c + \frac{\hbar^2}{2}\left(\frac{(k_x \pm k_{x,0})^2}{m_x} + \frac{(k_y \pm k_{y,0})^2}{m_y} + \frac{(k_z \pm k_{z,0})^2}{m_z}\right) \tag{2.1}$$

The effective mass of a carrier in a periodic crystal is inversely proportional to the curvature of the bands in the direction the carrier is traveling and is given by Equation 2.2.

$$m^* = \hbar^2\left(\frac{\partial^2 E_N(k)}{\partial k^2}\right)^{-1} \tag{2.2}$$

When we combine Equations 2.1 and 2.2, we can find the effective mass for each valley for travel in any direction. For example, the effective mass in the k_x direction for the x valleys is m_ℓ, while for the y and z valleys it is m_t. To find the total effective mass, the reciprocal masses are weighted by their corresponding valley's fractional occupancy, added, and then the sum is inverted. Since there is equal occupancy in all valleys for the bulk case, we find that for travel in k_x direction, the total effective mass is

$$m^* = \left(\frac{2}{6m_\ell} + \frac{4}{6m_t}\right)^{-1} = 0.26m_0 \tag{2.3}$$

In fact, as long as the occupancy is equal, we can determine that the effective

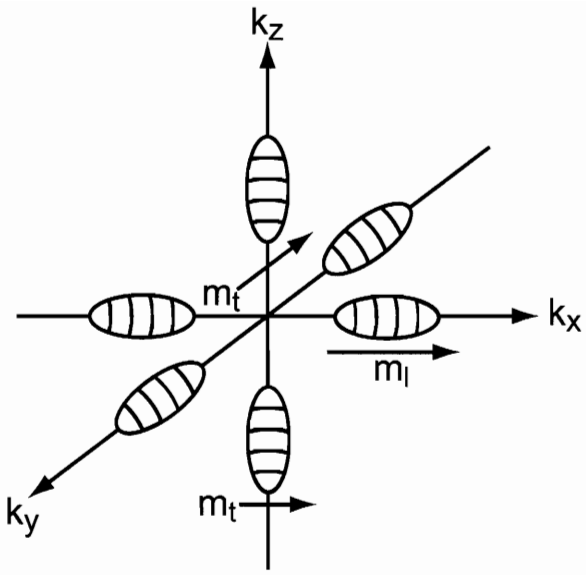


Figure 2-6: K-space ellipsoids of constant energy of just above the conduction band edge.

mass is isotropic in all directions and is always equal to $0.26m_0$.

Scattering Rates

In bulk silicon, the main scattering mechanisms are phonon scattering, and coulombic scattering by ionized impurities and other charge centers. The scattering rates are additive, meaning that the time between scattering events is given by

$$\frac{1}{\tau_{total}} = \sum_n \frac{1}{\tau_n} \tag{2.4}$$

where n indexes the different scattering mechanisms.

Coulombic scattering is important for determining bulk mobility. Its contribution to inversion layer mobility is minimal for the lightly-doped structures discussed in this work due to screening. However, the same formulation is used for scattering by interface charges that becomes important to inversion layer mobility.

The two types of phonons that occur in silicon are acoustic phonons and optical phonons. Carriers interact with optical phonons when they are traveling at high velocity, for instance near the drain of a MOSFET biased in saturation. Interac-

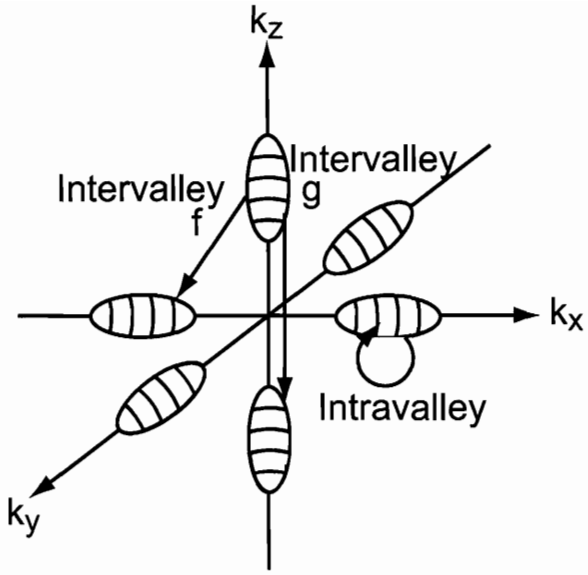


Figure 2-7: Diagram showing intravalley and intervalley scattering processes. Intervalley scattering can occur between valleys along the different axes (f scattering) or the same axis (g scattering).

tion with optical phonons is the mechanism that causes velocity saturation in this case. However, at low lateral field the carriers have negligible interaction with optical phonons. For this work, only low lateral field mobility is examined, so optical phonon scattering will not be considered.

Acoustic phonon scattering is the dominant scattering mechanism of concern in this work. These scattering events can result in the carrier scattering within a valley (intravalley scattering), or from one valley to another (intervalley scattering) as depicted in Figure 2-7. The formulation of these scattering rates will be done in the context of an inversion layer.

2.2.2 Electron Mobility in an Inversion Layer

Carriers in a MOS inversion layer are confined by the electric field applied by the gate. This confining field appears as a potential well to the carriers contained within it. The carriers become quantized in the well, with their energy and wave-functions determined by Schrödinger's equation. Since the location of the carriers is dependant on the shape of the well, and the shape of the well is dependent on the location of the

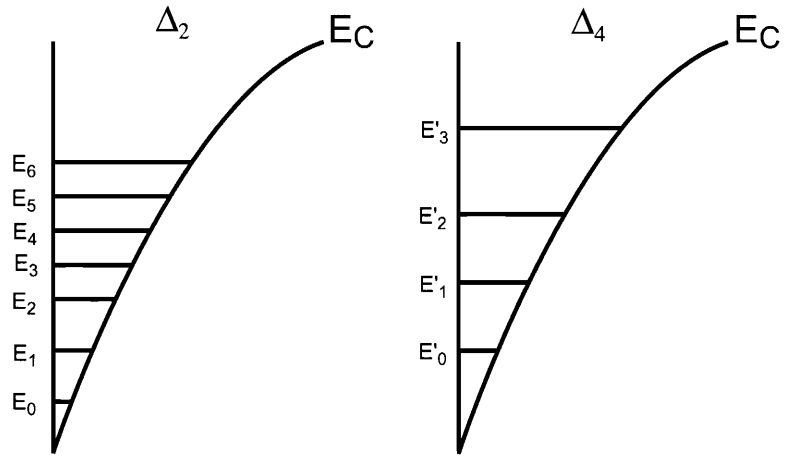


Figure 2-8: Schematic representation of the confinement-induced split in energy levels between the Δ_2 and Δ_4 valleys.

carriers through Poisson's equation, it is necessary to solve the system self-consistently in order to determine the carrier distribution.

Effective Mass in an Inversion Layer

Silicon MOS devices are typically built on wafers with a (100) orientation, so this section will discuss the inversion layer of a (100) surface. In this case, we define the direction of the electric field applied by the gate to be the z direction. The effective mass that is used when solving Schrödinger's equation is that in the direction of the confining electric field and is referred to as the quantization mass. Since the valleys that point in the k_z direction show a higher quantization mass (m_ℓ) than the others (m_t), they are quantized at more closely spaced energy levels. Then, the degeneracy of the carrier population in the bands is split into the twofold degeneracy of the k_z valleys, referred to as the Δ_2 valleys, and the fourfold degenerate k_y and k_z valleys, referred to as the Δ_4 valleys. An illustration of the split in energy levels between the Δ_2 and Δ_4 valleys is given in Figure 2-8. The aggregate effective mass in the direction of current flow (conduction effective mass) of the carriers in the inversion layer becomes

$$m^* = \frac{N_{\Delta_2} + N_{\Delta_4}}{\left(\frac{N_{\Delta 2}}{m_t} + \frac{N_{\Delta_4}}{m_{\Delta_4}}\right)} \tag{2.5}$$

$$m_{\Delta_4} = \left(\frac{1}{2m_\ell} + \frac{1}{2m_t}\right)^{-1} = 0.315m_0 \tag{2.6}$$

where N_{Δ_2} and N_{Δ_4} are the number of carriers present in each of the valleys as determined by simultaneously solving the Schrödinger and Poisson equations. As the electric field is increased, the energy difference between the energy levels of the Δ_2 and Δ_4 valleys is increased so the proportion of carriers in the Δ_2 valleys becomes higher. The conduction effective mass remains isotropic in the plane and becomes smaller due to the increased occupancy (from repopulation) of the Δ_2 valleys.

Scattering in an Inversion Layer

The primary mechanisms of scattering considered here for a silicon inversion layer are phonon scattering and surface scattering caused by surface charge and surface roughness.

Intravalley phonon scattering occurs when a carrier transitions between different subbands within the same valley. The equations for intravalley and intervalley scattering rates are taken from [10], and are presented here in a more shorthand notation for clarity. For actual calculations please refer to the source reference. The intravalley scattering rates between the ith and jth sub-band are given by

$$\frac{1}{\tau_{ac}^{i,j}(E)} = \frac{m_d D_{ac} kT}{\hbar^3 \rho s_l W_{i,j}} \tag{2.7}$$

$$W_{i,j} = \left(\int \xi_i^2(z)\xi_j^2(z)dz\right)^{-1} \tag{2.8}$$

where T is temperature, k is Boltzmann's constant, D_{ac} is the acoustic deformation potential, ρ is the mass density of the crystal, and s_l is the longitudinal sound velocity. Here, m_d is the density-of-states-effective-mass, given by $\sqrt{m_\ell m_t}$ for the Δ_4 valleys and by $\sqrt{m_t m_t}$ for the Δ_2 valleys. ξ_i is the wavefunction of carriers in the ith sub-

band. The total scattering rate for an electron in the ith sub-band with energy E is given as

$$\frac{1}{\tau_{ac}^{i}(E)} = \sum_{j} \frac{U(E - E_j - E_c)}{\tau_{ac}^{i,j}(E)} \tag{2.9}$$

$$U(x) = 1 \ (x \geq 0), \quad U(x) = 0 \ (x < 0) \tag{2.10}$$

where U(x) is the unit step function. From these equations, we see that the intravalley scattering rates are related to the density of states effective mass and the overlap between the wave functions of carriers occupying the different subbands. The factors that can affect intravalley scattering are effective mass and the confining potential. Changing the effective mass impacts both the density of states effective mass and the shape of the wavefunctions. Changing the shape of the well affects only the shape of the wavefunction.

Intervalley phonon scattering occurs when a carrier transitions to another valley. This scattering rate is given by

$$\frac{1}{\tau_{inter}^{i,j}} = \sum_{k}^{f} \frac{f m_d D_k^2}{\hbar \rho E_k W_{i,j}} \left(N_k + \frac{1}{2} \pm \frac{1}{2} \right) \times \frac{1 - f(E \mp E_k)}{1 - f(E)} \times U(E \mp E_k - Ej - E_c) \tag{2.11}$$

where the f index accounts for the different scattering mechanisms ($\Delta_2 \rightarrow \Delta_4$ f-phonons, $\Delta_4 \rightarrow \Delta_2$ f-phonons, $\Delta_4 \rightarrow \Delta_4$ f-phonons, and $\Delta_4 \rightarrow \Delta_4$ g-phonons) represented in Figure 2-7. From this equations we see that the intervalley scattering rates are related to the density of states effective mass, the overlap between the wavefunctions of the initial and final states, and the energy difference between the initial and final states. This is similar to the dependence of intravalley scattering, except there are more possible states to scatter to, and a relative change in energy between different valleys that does not affect the shape of the well will impact the f-phonon scattering rates.

Surface roughness scattering occurs at the interface between the silicon and the

gate dielectric. The scattering rates are given by Fischetti and Laux [11] as

$$\frac{1}{\tau_{SR}^{i,j}(k)} = \frac{\Delta^2\Lambda^2}{2\hbar^3}\kappa_j[E_i(k) - E_j]U[E_i(k) - E_j] \times \int_0^{2\pi} K(\theta)^2|S[q(\theta)]|^2|\Gamma_{i,j}[q(\theta)]|^2 d\theta \tag{2.12}$$

$$|S(q)|^2 = (1 + q^2\Lambda^2/2)^{-3/2} \tag{2.13}$$

$$K(\theta) = \sqrt{\frac{cos^2\theta}{m_\ell} + \frac{sin^2\theta}{m_t}} \tag{2.14}$$

where Δ is the RMS interface step height, and Λ is the autocorrelation of the step distance, and θ is the polar angle of the scattering event. $\Gamma_{i,j}(q)$ relates the overlap of wavefunctions of the initial and final states with the interface. q(θ) is the magnitude of the phonon wave vector. $\kappa_j(E)$ is a correction factor for the jth sub-band that accounts for non-parabolicity of the bands.

From these equations, we can see that the surface-roughness scattering rates depend on the roughness of the interface, defined through Δ and Λ, on effective mass, and on the shape of the carrier wavefunctions. Because surface roughness is in general a fixed parameter for the silicon/silicon dioxide interface, the parameters that affect surface roughness scattering are those that change effective mass and the carrier wave functions.

An additional scattering mechanism that occurs at the silicon/oxide interface is coulombic scattering by fixed charge at the interface. This same formulation can be used to determine the coulombic scattering rates caused by doping in the channel. While in the lightly-doped structures studied here, these rates are negligible, short-channel devices have highly-doped channels and therefor exhibit more coulombic scattering. The scattering rates are given by Fischetti and Laux as

$$\frac{1}{\tau_{coulomb}^{i,j}(k)} = \frac{e^4 N_r}{8\pi\hbar^3\epsilon^2}\kappa_j[E_i(k) - E_j]U[E_i(k) - E_j] \times \int_0^{2\pi} \frac{H_{i,j}[q(\theta)]}{q(\theta)^2} K(\theta)^2 d\theta \tag{2.15}$$

$$H_{i,j}(q) = \int_0^\infty \int_0^\infty \xi_j(z)\xi_j(z')I_q(z,z')\xi_i(z)\xi_i(z')dz'dz \tag{2.16}$$

where for scattering by interface charges

$$I_q(z,z') = e^{-q(z+z')} \tag{2.17}$$

From this description, we can see that the number of charge centers (N) has a linear effect on the scattering rate. The form factor $H(q)$ takes account of the overlap between the charge centers and the carriers. Coulombic scattering can be modulated by changing the number of charge centers (doping or interface quality concerns), or by changing the position of the carriers with respect to the charge centers. For instance, applying a high electric field moves the carriers closer to the surface where they interact more with the interface charge.

Inversion Mobility in Strained Films

For biaxially tensile strained (100) silicon, the Δ_2 valleys are lowered in energy compared to the Δ_4 valleys as pictured schematically in Figure 2-9. This leads to increased occupancy in the Δ_2 valleys which yields two beneficial effects for mobility. The first is that the Δ_2 valleys have a lower conduction effective mass, so increasing their fractional population leads to a lower aggregate conduction effective mass. The other beneficial effect is that the energy split between the Δ_2 and Δ_4 valleys leads to less f-phonon scattering between them. Because the effective mass and shape of the confining well remain the same, intravalley phonon scattering is not affected.

However, increasing the population of the Δ_2 valleys acts to move the average distance of the carriers closer to the silicon/oxide interface, which should increase the amount of interaction between the carriers and surface charges and surface roughness. This seems to indicate that biaxial strain should not be beneficial at high vertical fields, which does not agree with experimental evidence. This discrepancy has led to difficulty in modeling the enhanced mobility in biaxially strained silicon and remains a point of contention [12].

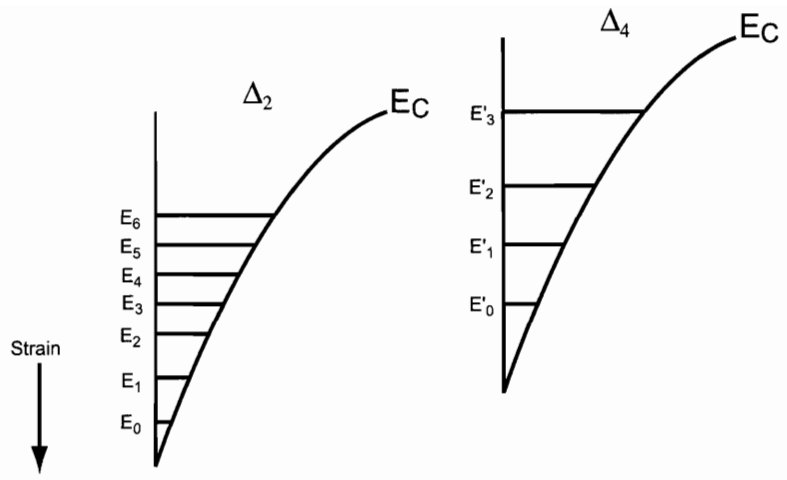


Figure 2-9: Schematic representation of the band-splitting that occurs with biaxial strain to the conduction band of silicon in an inversion layer.

For (100) silicon with uniaxial tensile strain in the [100] direction, the k_x valley is raised while the k_y and k_z valleys are lowered. This breaks the degeneracy of the Δ_4 valleys. For electron travel in the [100] direction, the aggregate effective mass is lowered due to the increased occupancy of the k_y and k_z valleys which contribute m_t to the effective mass. For travel in the [010] direction, the aggregate effective mass is higher than in the [100] direction and can be higher than in the unstrained case (depending on strain and confining field) due to the higher occupancy in the k_y valleys which contribute m_ℓ in this direction. The aggregate effective mass of electrons traveling in the [110] direction is relatively unaffected. As in the biaxial strain case, f-phonon scattering is reduced due to the split in the energy levels.

Currently, the most relevant crystal and strain orientation to examine is uniaxial [110] tensile strain on (100) silicon wafers. MOSFETs are generally built on (100) silicon wafers where the direction of current flow is parallel to a [110] equivalent direction. Process-induced strain is then used to apply uniaxial strain parallel to the direction of current flow. In this case, the net effect is to raise the Δ_4 valleys and lower the Δ_2 valleys, in a completely analogous fashion to biaxially strained silicon. However, the off-axis deformation of the crystal structure leads to deformation of the band structure that results in a change in the effective mass of electrons in the Δ_2 valleys. Figure 2-10(a) shows the anisotropic response of the effective mass to [110]

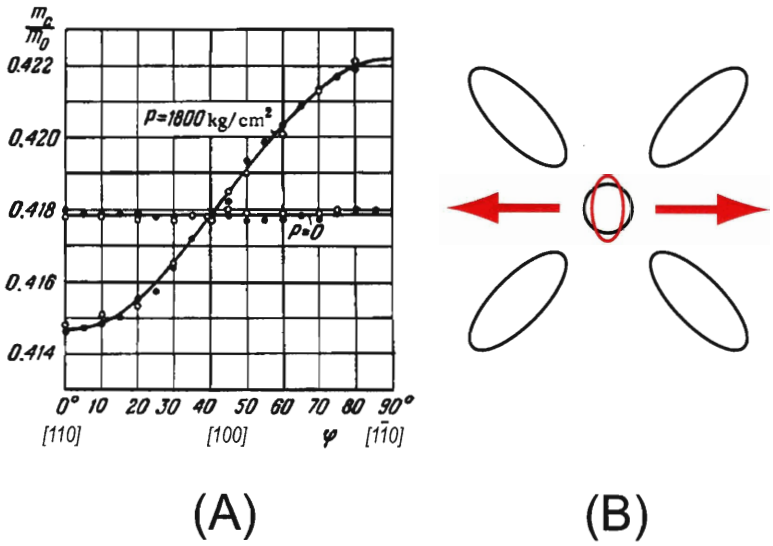


Figure 2-10: (a) Cyclotron resonance effective mass vs. applied magnetic field angle for carriers in the Δ_2 valleys with and without an applied uniaxial compressive stress. Change in effective mass is fit by the curve $\Delta m^*/m = a + bcos\phi$ [13]. (b) Projected view of the Δ valleys of silicon onto the (100) plane. Tensile strain in the [110] direction results in reduction of the effective mass in the [110] direction, an increase in the effective mass in the [1$\bar{1}$0] direction, and relatively little change in the [100] direction. The effective mass in the [001] direction (quantization effective mass) remains constant.

strain. For tensile strain, the result is that the effective mass is lower in the direction of applied strain, and higher perpendicular to it, as depicted in Figure 2-10(b). The effects that this change in effective mass have on mobility are shown experimentally in Chapter 5.

Electron Mobility in Ultra-Thin Films

When an SOI film is thinned below the equilibrium inversion layer depth, the carriers are confined by the thickness of the film rather than the electric field. This affects the wave-function and energy of the carriers.

Because the Δ_4 valleys have a lower quantization effective mass, they have a larger wave-function compared to carriers in the Δ_2 valleys for the same confining well. As the potential well is made smaller by thinning the film, the carriers in the Δ_4 valleys are affected first and more strongly, raising their energy more quickly than the Δ_2 valleys, as shown in Figure 2-11. This leads to increased occupancy of the Δ_2 valleys,

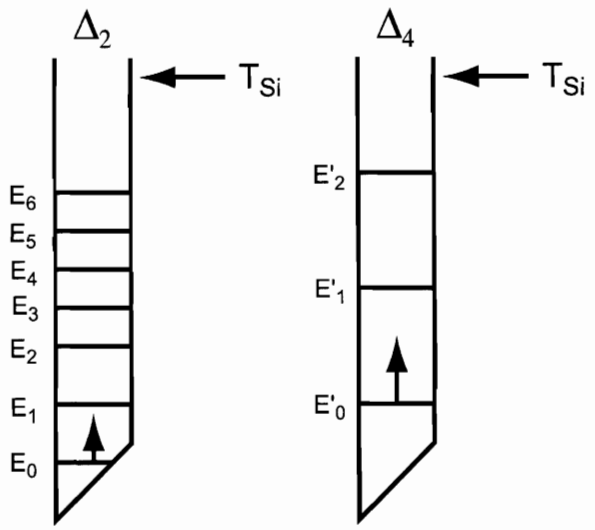


Figure 2-11: Schematic representation of the confinement-induced split in energy levels between the Δ_2 and Δ_4 valleys caused by thinning in the film. The energy of the states in the Δ_4 valleys will increase more with reduced film thickness than those in the Δ_2 valleys.

analogous to what occurs in biaxially strained silicon. However, because of the change in energy levels within the valleys unlike for the biaxial strain case where the energy levels within the valleys are relatively unaffected by the strain, intravalley phonon scattering is affected. Also, the confinement leads to more total phonon scattering. The confinement in real space leads to dispersion in k-space, which allows the carriers to interact with more phonons.

The net result of the decreasing effective mass but increased phonon scattering is the phonon-limited mobility vs. silicon film thickness shown in Figure 2-12. Below about 15 nm, the mobility begins to drop. However, there is a range of thickness between 3-4 nm where the mobility is increased over bulk due to the transfer of carriers to the Δ_2 valleys. Below this thickness, the Δ_2 valleys become confined by the film, and the resulting increase in phonon scattering drastically reduces the mobility.

A scattering mechanism that is unique to ultra-thin films is "δT_{SOI} scattering" [14]. These scattering events occur due to the local change in conduction and valence band energies caused by thickness variation. The difference in band energy between between thicker and thinner regions acts as a potential barrier that can scatter carriers. The

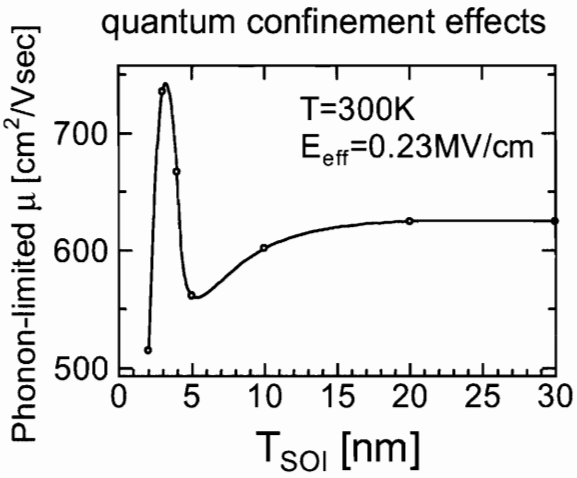


Figure 2-12: Phonon limited mobility vs. silicon film thickness [10]. While quantum confinement acts to degrade mobility, for a range of thickness the energy splitting between the Δ_2 and Δ_4 ground state energies results in higher mobility.

relationship is similar to the scattering that occurs in AlAs/GaAs quantum wells [15] where the scattering rates are

$$\tau_{\delta T} \propto \frac{T_{well}^6}{\Delta^2 \Lambda^2} \tag{2.18}$$

where T_{well} is the thickness of the confining well and Δ and Λ characterize the interface roughness as defined earlier. For SOI, T_{well} is T_{SOI}, meaning that the scattering rate increases very quickly as the silicon film is thinned. While phonon scattering typically overwhelms this effect, it does act to degrade room-temperature mobility and the T_{SOI}^6 dependence can be observed at low temperature.

Electron Mobility in Ultra-Thin Strained Films

Because most of the mobility degradation seen in ultra-thin films occurs in the Δ_4 valleys first, applying strain to the system to re-populate carriers into the Δ_2 valleys should be highly beneficial. If sufficient strain is applied to move the majority of the carriers into the Δ_2 valleys, quantum size effects should not degrade electron mobility until the film is less than 3 nm because of the higher quantization mass in these valleys. One of the goals of this thesis is to experimental examine the impact of strain on carriers in ultra-thin films.

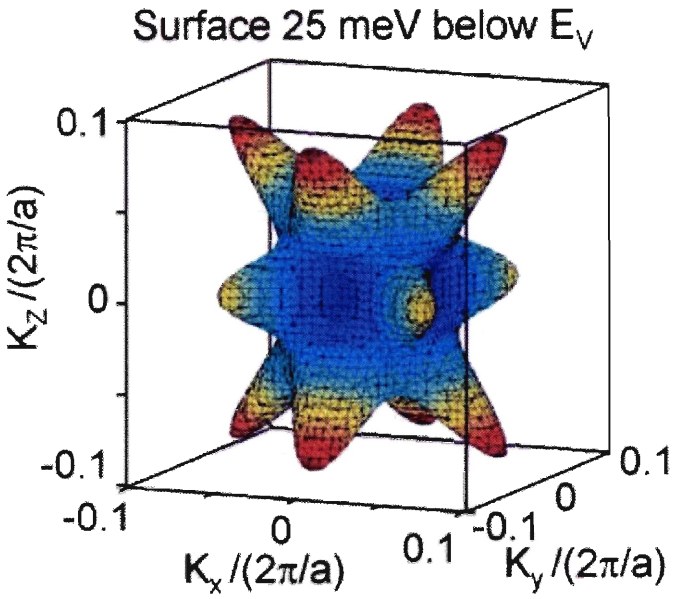


Figure 2-13: Valence band structure of silicon showing the warped nature of the bands [17].

2.2.3 Hole Mobility

Compared to electrons, the physics that governs hole transport is less intuitive. The following is a brief overview of the effects that govern hole mobility.

The conduction band for silicon has two degenerate subbands at its maximum at the Γ point, the "light hole" band ($m^* = 0.16m_0$), and the "heavy hole" band ($m^* = 0.49m_0$). Since the maximum is at the Γ point, the surfaces of constant energy for holes are not split into six sub-bands like for electrons. However, energy surfaces for the light hole and heavy hole bands are "warped" by their degeneracy at $\mathbf{k} = \mathbf{0}$. The shape of the constant energy surface of just below the valence band edge is shown in Figure 2-13. Because of this warping, more sophisticated theory such as $\mathbf{k} \cdot \mathbf{p}$ perturbation must be used to determine the effective mass of holes [16].

Scattering rate calculations for holes have the same dependencies as for electrons. Changes in the density of states effective mass, the shape of the wavefunctions, and the split in energy between the initial and final states all effect the phonon scattering rates for holes.

The application of strain affects hole mobility by deforming the band structure and lifting the degeneracy of the light and heavy hole bands. Like for electrons, the

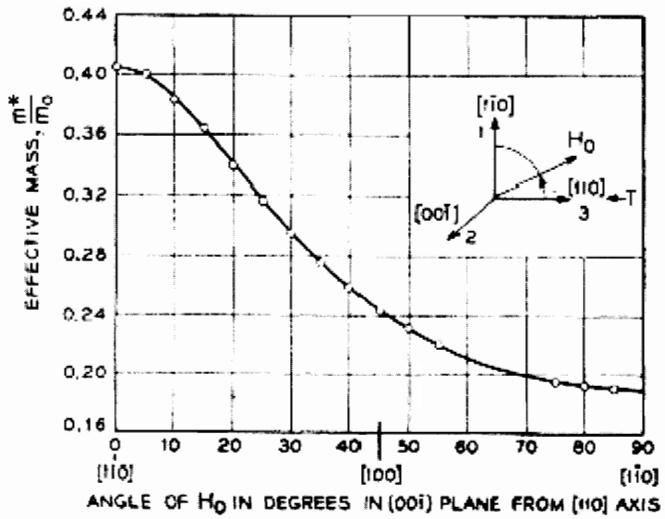


Figure 2-14: Change in hole cyclotron resonance effective mass with 2270 kg/cm^2 stress applied parallel to the [110] direction [16]

application of [110] uniaxial strain to a (100) oriented wafer leads to an anisotropic change in the effective mass, as shown in Figure 2-14. Thompson et al. have found the main contribution to increased hole mobility with compressive strain to be band deformation (decreased effective mass) for uniaxial strain and band-splitting for biaxial strain [17].

Because the quantization mass of the light holes is lower than that of heavy holes, they become thickness-confined first as the film is thinned. This raises their energy level, which repopulates carriers into the heavy hole band. This results in a higher aggregate conduction effective mass for holes, in contrast with the advantageous band repopulation that occurs for electrons because of the favorable anisotropy of the Δ_2 valleys. The result is that holes suffer from thickness-induced mobility reduction in films thicker than that which effect electrons because of the lower quantization effective mass of the light holes. This also results in a monotonic decline in hole mobility with film thickness, as shown in Figure 2-15.

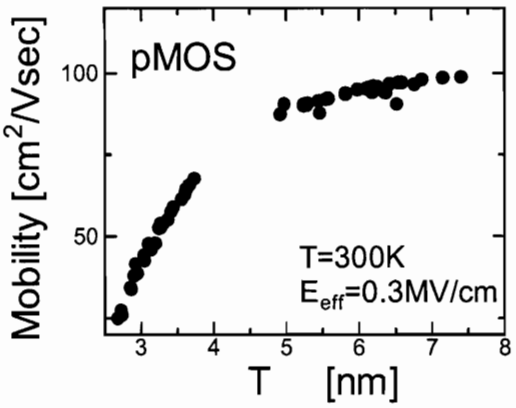


Figure 2-15: Hole mobility vs. silicon film thickness [14]. Hole mobility declines monotonically with reducing film thickness.

Chapter 3

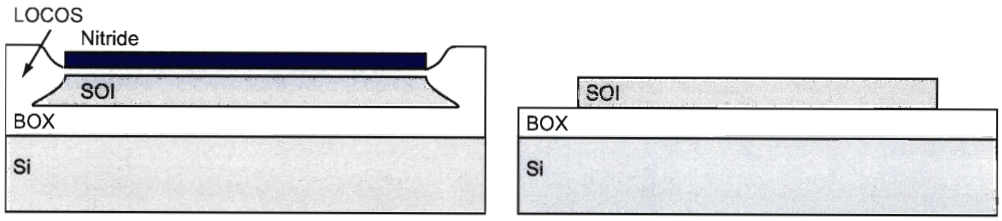
Experimental Procedures

Various types of MOSFETs were fabricated to examine carrier transport in inversion layers. The effects of uniaxial strain and film thickness on mobility were then examined. This chapter provides details of the techniques used to build and characterize the MOSFETs used to collect the results presented later in this thesis.

3.1 FDSOI Device Fabrication

A simple four-mask process was used to fabricated devices with channels thicker than about 8 nm. Under ideal conditions, a full MOSFET flow can be completed in under two weeks. Because of this fast turn-around time, this was the preferred process for examining relatively thick films.

First, a new SOI or SSDOI wafer is thinned to a desired starting thickness by thermally oxidizing the top silicon layer and then chemically etching the grown oxide. Since there are currently some not well understood mechanisms that impact the oxidation rate of extremely thin films, this oxidation is done in iterative steps to achieve the desired thickness. Starting wafers first undergo full RCA cleaning (of which the SC1 step removes some silicon), then oxidation at 800°C for two hours, growing 10 nm of oxide and consuming approximately 5 nm of the silicon film in the process. The wafers are then measured by spectrographic ellipsometry to determine exactly how much oxide was grown and how much silicon film was consumed. The



(a) LOCOS Isolation (b) Mesa Isolation

Figure 3-1: Isolation methods used for FDSOI device fabrication.

wafer is then cleaned in the SC1 step of the RCA, but since an oxide layer is still present the silicon film is protected from chemical etching. The oxide is then dipped off in 50:1 H_2O:HF, and the wafer is cleaned in the SC2 step of the RCA clean. A new thermal oxide is then grown and the process is repeated until the film reaches the desired thickness.

Once the SOI film is thinned to the desired thickness, isolated device islands are defined. Both LOCOS (Figure 3-1(a)) and mesa (Figure 3-1(b)) isolation were used in these experiments. Wafers which received mesa isolation simply had the active area patterned by etching the silicon film to the buried oxide. Wafers which received LOCOS isolation had a thin stress-relief oxide (SRO) grown on them (the remaining oxide from the last thinning step was often used), a nitride film deposited and patterned, then a thermal oxide grown to the buried oxide in the region where the nitride was removed. The remaining nitride is then stripped in hot phosphoric acid.

After isolation a gate oxide is grown and polysilicon is deposited and patterned. The wafers are RCA-cleaned and any remaining oxide on the surface is stripped in HF between the SC1 and SC2 steps. A new thermal oxide is then grown, usually at 800°C in a dry oxygen ambient, with a target thickness of approximately 4 nm. In-situ phosphorus-doped polysilicon is then deposited as the gate material. Often, the gate material is deposited at 560°C and is initially amorphous rather than polycrystalline.

Photoresist is then patterned on the polysilicon, and the gate material is etched in a multi-step process in a magnetically-enhanced reactive ion etch (MERIE) system

	De-scum	De-ox	Main Etch	Over-etch
Power (W)	75	75	350	75
B Field (G)	50	50	50	50
Pressure (mT)	200	100	200	100
CF_4 (sccm)	0	20	0	0
HBr (sccm)	0	0	20	40
Cl_2 (sccm)	0	0	20	0

Table 3.1: Gate etch recipes.

as summarized in Table 3.1. First, due to the high selectivity of subsequent etches to photoresist, a low-power high-pressure oxygen plasma "de-scum" step is used to remove any photoresist residue in the open areas of the pattern. Then, due to the high selectively of the subsequent etches to oxide, a low-power C_2F_4 plasma is used to remove any native oxide or oxide grown during the de-scum step ("de-ox"). Then a high-power Cl_2+HBr plasma is used as a timed main etch to remove about 80% of the polysilicon. The main etch step has a high etch rate and provides a highly anisotropic etch, but its selectivity to oxide is not enough to allow it to stop on a thin gate oxide. A low-power HBr plasma is then used as a timed over-etch step to remove the remaining polysilicon and stop on the gate oxide. While the over-etch has a low etch rate and is fairly isotropic, it has a selectivity of polysilicon to oxide of >100:1.

The photoresist is then stripped in an oxygen plasma, and the wafers are cleaned in a modified RCA clean where the SC1 step is replaced with piranha (3:1 H_2SO_4:H_2O_2) and no HF dip is performed. Then, a 10-15 nm screen oxide is deposited by LPCVD, and the wafers are sent to an external vendor for ion implantation of the source and drain regions. Typical conditions for ion implantation are a dose of 5×10^{14} As ions at 35 keV. The thickness of the screen oxide was adjusted based on the underlying film thickness so that the peak of the implant could be located in the film using a reasonable implant energy. Otherwise, the implant time becomes very long, and a good deal of sputtering of the surface can occur.

Once the wafers return from ion implantation, they are cleaned in two successively cleaner piranha baths and are then RCA cleaned. A thick (100-200 nm) LTO layer is then deposited, and the dopants are then activated in a rapid thermal anneal (RTA).

The RTA cycle has two stages in order to limit dopant degradation at the polysilicon grain boundaries. First, the temperature is ramped to 750°C and is held for 20 seconds. During this time the amorphous silicon crystallizes into polysilicon. The temperature is then spiked to 1050°C for 5 seconds during which time the dopants are activated.

The devices are then finished by metallization. First, via holes are patterned and etched. Then 100 nm Ti / 500 nm Al are sputtered. It has been found that thinner Ti does not serve as a sufficient barrier to Al diffusion during the subsequent sintering step. If the Al comes in contact with the silicon it tends to laterally creep many microns and short the source/drains of the devices together. The Ti/Al is then patterned by a dry plasma etch in Cl_2 or in a wet PAN etch (Phosphoric acid, Acetic acid, Nitric acid) to remove aluminum followed by a dilute HF or BOE (Buffered Oxide Etch) mixture that removes the underlying Ti. The photoresist is then ashed and the devices are finished by sintering in forming gas. This sintering step must be performed at >450°C for >30 minutes to remove interface states that degrade mobility and subthreshold slope.

While the above process offers quick turn-around and simplicity, it was found that devices below about 8 nm could not be contacted. Others have reported contacting films this thin, so the problem appears technological rather than fundamental. One solution that was found was to use in-situ doped polysilicon for the contact material beneath the Ti/Al stack. This may indicate that voids are formed during the silicidation that occurs during the final forming gas anneal, although un-sintered devices also showed no contact to the channel. This seems to indicate that the silicon film is removed during the contact etch, and the enhanced filling ability of the polysilicon deposition is responsible for the working contacts. Because the only in-situ doped polysilicon available was phosphorus dopes, this process was only employable on NMOS devices.

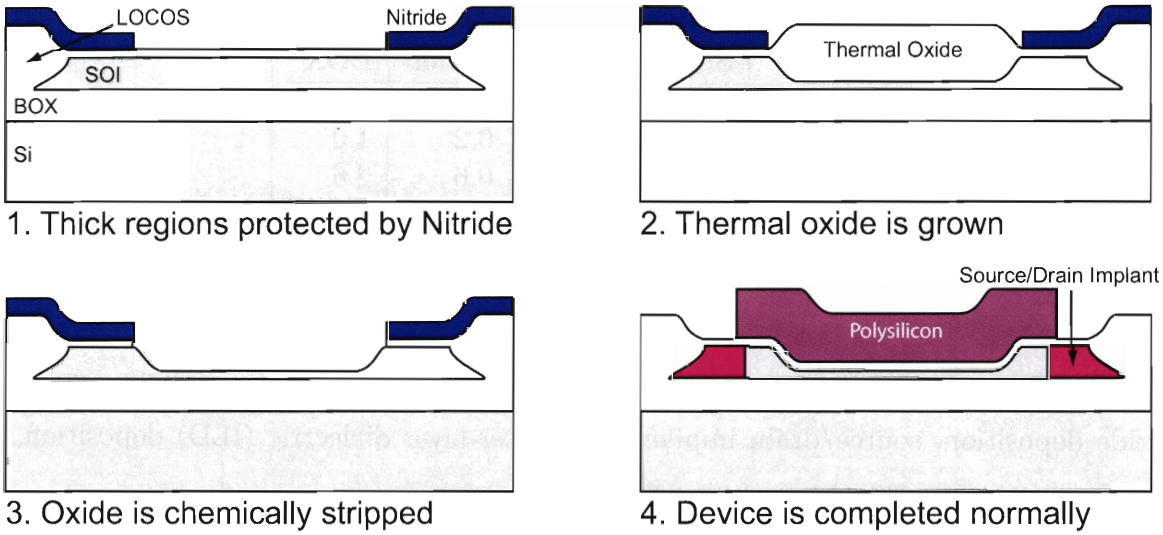


Figure 3-2: Process for locally thinning the channel while leaving the source/drains thick.

3.2 Locally-Thinned Channel Fabrication

While polysilicon-first metalization allows contact to thin films, it was determined that since only the channel region needs to be thin, a process could be used which keeps the source/drains thick. This allows for less stringent control of certain processing steps and adds minimal complexity. In a short-channel device, other techniques like raised source/drains and self-aligned silicides would have to be employed to limit series resistance. However, for measuring mobility, long channel devices are used, so locally-thinning the channel was chosen as the preferred method.

First, LOCOS is performed. In this case, an isolation implant (1×10^{14} boron at 20 keV) is performed prior to the LOCOS oxidation in order to eliminate edge leakage that was observed in prior experiments.

Next, the channel is selectively thinned (Figure 3-2). This is analogous to a LOCOS process. The remaining SRO from LOCOS is left in place as a SRO for the thinning, and a nitride layer is deposited and patterned in a region of the active area. Within wafer splits are performed by removing the nitride over the entire active area to yield a fully-thinned device. Some active areas remain covered by nitride and receive no thinning. Repeated oxidation and oxide stripping are then used to thin the channel to the desired thickness.

	Starting Wafer		After Thinning	
	Silicon	BOX	Silicon	BOX
Mean	28.7	155	8.5	156
Std. Dev.	0.4	1.0	0.2	1.0
Range	1.8	4.7	0.6	2.6

Table 3.2: Ellipsometry data indicating an improvement in SOI film uniformity with thinning. All units are in nm.

The device is then completed as before, with gate stack and patterning, screen oxide deposition, source/drain implantation, inter-layer dielectric (ILD) deposition, dopant activation, Ti/Al based metallization, and forming gas anneal.

3.3 Self Limiting Oxidation

It has been observed that during the successive oxidation and oxide stripping process, the SOI film long-range uniformity across the wafer improves. An example showing the difference between starting uniformity and uniformity after thinning using dry oxidation performed at 800°C is given in Table 3.2. Since it is also observed that as the film becomes thinner, the oxidation rate goes down. For instance, an oxidation performed at 800°C for 120 minutes grew 9.6 nm of oxide on bulk wafers and SOI wafers with a 30 nm thick silicon layer, and grew 9.3 nm on an SOI wafer with a 15 nm thick silicon layer. From these observations, it is apparent that there is some self-limiting oxidation mechanism occurring in these thin films.

Self-limited oxidation has previously been observed and used in the study of silicon nano-wires [18]. In these experiments, cylindrical pillars are oxidized until a rod of silicon only a few atoms in diameter is left. This process is rather robust and repeatable despite limitations in lithography and furnace control because the oxidation rate of the silicon decreases quickly as the pillar is oxidized. However, this appears to be due to 2D stress effects that one would not expect to see in the oxidation of a planar film.

Although this effect has been observed in planar films and patented [19], the physical mechanism responsible for the improvement in uniformity with thinning is

still unknown. A possible explanation is that interstitials injected into the silicon during the oxidation process accumulate in the SOI film and inhibit the oxidation rate. Since oxidizing the silicon surface requires silicon atoms to break bonds with their neighboring silicon atoms and for the bond to remain open until it reacts with an oxygen atom, a high concentration of interstitials would increase the likelihood that a bond will be formed with a free silicon atom rather than an oxygen atom, and hence decrease the oxidation rate. The thinner regions would have a higher concentration of interstitials and hence oxidize slower. The net effect would be to make the film more uniform during oxidation.

A potential problem with this hypothesis is that it has been reported that at least under certain conditions, the buried oxide layer is transparent to interstitials. Experiments were performed that use the growth of oxidation stacking faults as a metric for determining the interstitial concentration in an SOI film [20]. An analytical model was developed to explain these results that indicates that silicon self-interstitials react at oxide interfaces to form SiO molecules that have a high diffusivity in SiO_2 [21]. However, the stacking fault experiments were performed at much different oxidation conditions than those of this work (950°C steam oxidation, 1040°C wet oxidation, and 1100°C dry oxidation). Because the diffusivity of silicon atoms in SiO_2 is an order of magnitude lower than that of SiO molecules, if the formation of SiO molecules is suppressed at lower temperature, the buried oxide will no longer appear as a sink for the interstitials. Because of the importance that film thickness uniformity plays in the manufacturability of thin silicon devices, further research should be done to investigate the mechanism responsible for improved global uniformity during SOI thinning.

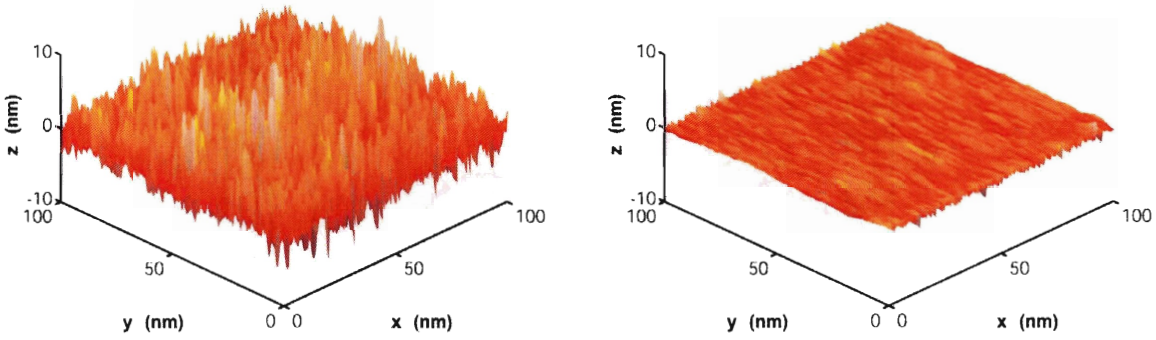
3.4 Oxidative Smoothing

For a device with a thin channel to function, the local roughness of both top and bottom surfaces of the film must be much smaller than the film thickness or the channel will not be continuous. The top surface of the SOI wafers is usually very smooth.

The SIMOX wafers used for the initial ultra-thin SOI experiments presented in this thesis had a starting top surface roughness of <0.3 nm according to the manufacturer. However, the interface between the silicon and the buried oxide layer did not have a surface roughness specification, and was expected to be rougher than the top interface due to the wafer fabrication method.

In order to examine the surface roughness of the wafers, atomic force microscopy (AFM) was used. To examine the top surface, AFM was performed on a piece without any preparation, and one that had the native oxide stripped in dilute HF. In both cases the surface was found to have an RMS roughness of about 0.3 nm, which is close to the specification from the manufacturer. To examine the bottom interface, a sample had the native oxide stripped and the silicon layer removed in tetramethyl ammonium hydroxide (TMAH). This procedure exposes the top surface of the buried oxide for AFM. On the SIMOX wafer examined here, the bottom interface roughness was found to be almost 8 nm as pictured in Figure 3-3(a).

With a bottom surface roughness of over 8 nm, devices with a channel thickness of less than 10 nm would be rather impractical to study since the thickness variation is a significant proportion of the total device thickness and the channel would not be a continuous film. However, it is known that oxidation smoothes silicon surfaces [22], and that oxidation can occur at the interface between the silicon and the buried oxide [23]. During the thinning process, oxidation occurs at both interfaces, smoothing them. After thinning, the RMS roughness of the buried oxide interface was found to be around 0.5 nm as pictured in Figure 3-3(b), close to the roughness of the top interface, while the top surface roughness stayed approximately the same. While a perfectly smooth interface would be ideal, the smoothing of the back interface during the thinning process brings the thickness uniformity of the silicon to a level at which studying ultra-thin films is practical.



(a) Buried oxide interface before thinning.

(b) Buried oxide interface after thinning.

Figure 3-3: AFM images of the top surface of the buried oxide layer of a SIMOX SOI wafer before (8.0 nm RMS roughness) and after thinning (0.5 nm RMS roughness) by oxidation of the top surface.

3.5 Dealing with Series Resistance

While an effort was made to minimize series resistance in the ultra-thin SOI devices, the final series resistance was still large enough to cause substantial problems for mobility extraction. An effective solution to this problem was to perform measurements on a specially designed MOSFET designed to negate series resistance effects [24]. Figure 3-4 provides a plan-view schematic of such a device. By measuring the voltage at two points along the channel, the effective V_{DS} along the channel is inferred as

$$V'_{DS} = (V_1 - V_2)\frac{L}{L_{LR}} \tag{3.1}$$

The mobility is then extracted using the effective V'_{DS} as

$$\mu_{eff} = \frac{L}{W}\frac{I_D}{V'_{DS}}\frac{1}{Q_{inv}} \tag{3.2}$$

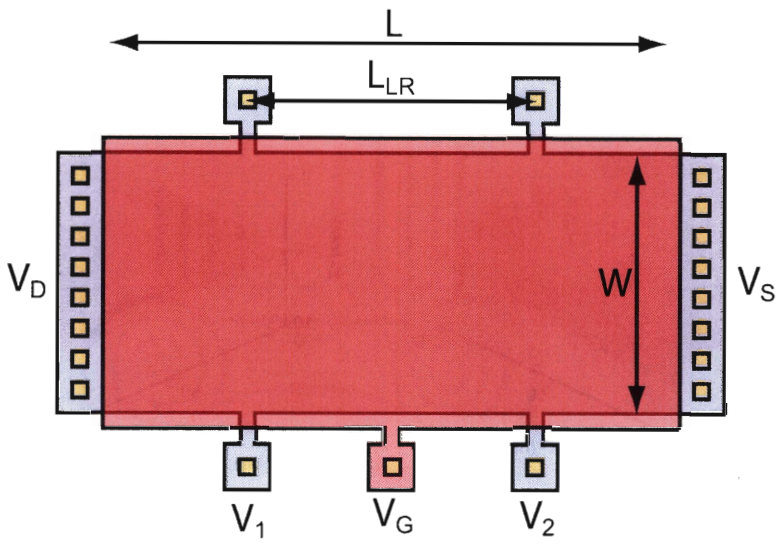
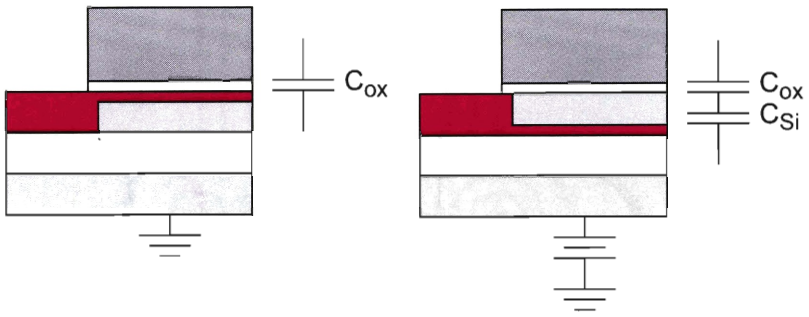


Figure 3-4: MOSFET structure allowing Kelvin measurements.

3.6 Film Thickness Extraction

Film thickness was extracted by matching CV measurements with different back-biases to 1D Poisson-Schrödinger simulations using the "Schred" simulator [25]. At sufficiently low front-gate bias, a high bias on the substrate can induce an inversion layer at the back interface. In this case, the capacitance between the front-gate and the inversion layer is the series combination of the oxide capacitance and the silicon depletion capacitance as shown in Figure 3-5(b). When the film is relatively thick, a plateau in the CV forms for a range of front-gate biases (Figure 3-6(a)), and the silicon film thickness can be extracted analytically using the difference between the maximum capacitance and the plateau and the ratio of the dielectric constants of silicon and oxide. When the film becomes thinner, the plateau shrinks and eventually disappears as the film thickness approaches the inversion layer depth (Figure 3-6(b)). Once this occurs, the threshold voltage shift with back-bias becomes a strong function of film thickness due to electrostatic and quantum confinement effects.

By employing Schred simulations that the electrostatic and quantum confinement effects of thin films into account, gate oxide thickness, silicon thickness, and buried oxide thickness were extracted. An optimizer for Schred was in the Python [26] scripting language to expedite the extraction process. Gate oxide thickness was extracted from



(a) No applied back-gate bias. (b) High back-gate bias.

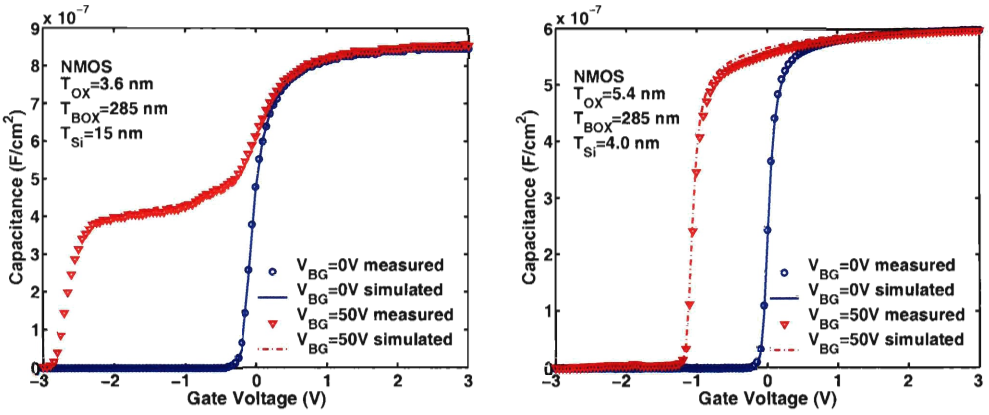
Figure 3-5: Location of the inversion layer with and without applied back-gate bias.

the maximum capacitance, while silicon thickness and buried oxide thickness were solved self-consistently while optimizing the threshold voltage and threshold voltage shift with back bias. Examples of simulations matched to the measured data data are shown in Figure 3-6(a) for a thick SOI device and in Figure 3-6(b) for and ultra-thin SOI device. Because the threshold voltage shift with back-bias is a strong function of film thickness as shown in Figure 3-8, this technique gives an accurate estimation of the film thickness. The electrically extracted values for film thickness closely match the values expected from ellipsometric measurements made during device processing. A cross-section TEM of the device measured in Figure 3-6(b) is shown in Figure 3-7, showing that the actual film thickness of a device after processing matches very closely with the value extracted electrically. The similarity in smoothness between the silicon/gate oxide and silicon/buried oxide interfaces is also apparent.

3.7 Applying Uniaxial Strain

Uniaxial strain was applied in a four-point bending apparatus schematically pictured in Figure 3-9. The wafer was cut into strips in order to be bent. The procedure used was to coat the wafers in photoresist to protect the surface from massive particle contamination, then strips were cut out using a die saw. The resist was then removed in a solvent rinse that removes most of the particles created during the sawing process.

The strips are then bent by displacing the center points of the bending apparatus



(a) T_{Si} = 15 nm. (b) T_{Si} = 4.0 nm.

Figure 3-6: CV characteristics with and without applied back-gate bias with corresponding Schred simulations.

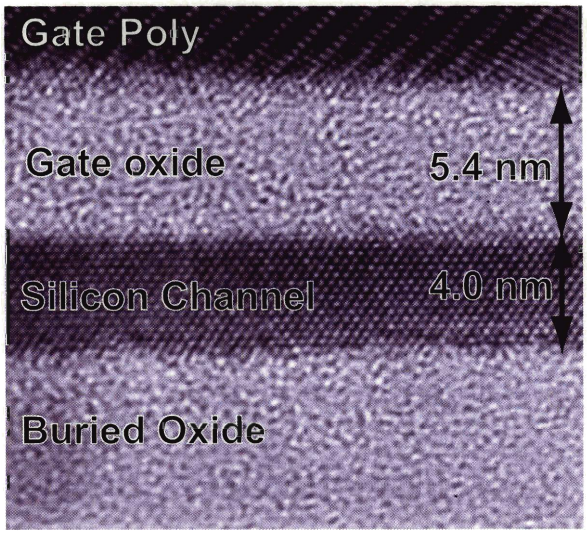


Figure 3-7: XTEM image of an ultra-thin SOI device. The electrically extracted values for film thickness match quite well with the value extracted by XTEM. The film varies in thickness by around 0.1 nm.

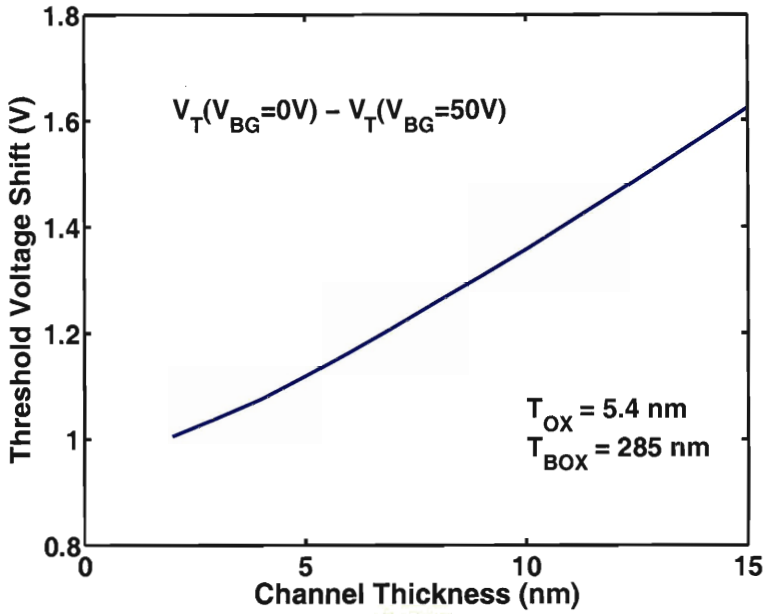


Figure 3-8: Threshold voltage shift with back bias vs. channel thickness calculated with Schred. Errors in the estimation of the threshold voltage shift are on the order of millivolts, so the error in film thickness estimation using this technique is less than the actual film thickness variation.

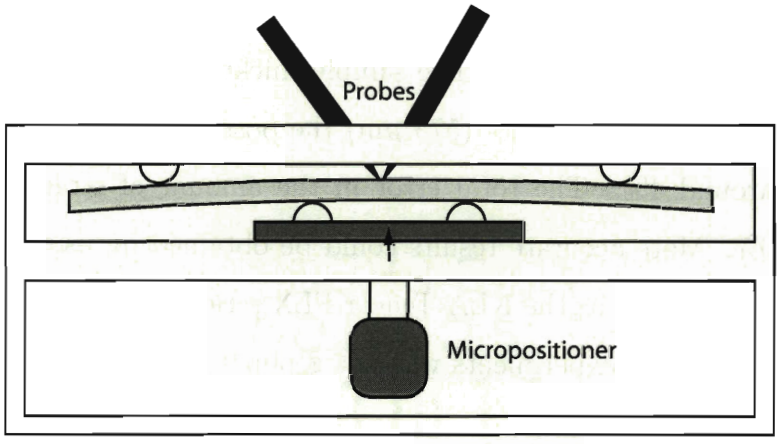


Figure 3-9: Schematic drawing of the four-point bending apparatus used to apply uniaxial strain.

using a micropositioner. An initial zero point is determined by raising the sample on the moving points until the sample is in contact with all four points. Any initial strain in the system caused by inaccurate initial positioning can fortunately be neglected due to the linear response to strain shown in Chapter 5. If there was a nonlinear response, the zero point would have to be more carefully chosen. The radius of curvature of the bend can be calculated geometrically from the amount of displacement between the inner and outer points using the position of three of the points to define a circle. The strain is then calculated as

$$\epsilon = \frac{T}{2R} \tag{3.3}$$

where T is the sample thickness and R is the radius of curvature calculated geometrically from the displacement of the moving points. The rotation of the sample was checked by optically aligning points 2 cm apart to an accuracy of better than 50 μm, giving a possible rotational error of less than 0.15°. Errors in strain estimation could arise from inaccurate estimation of the radius of curvature and uncertainty in the sample thickness. The moving points are self leveling, so the uncertainty of the displacement of the points is only due to experimental error in the positioning of the dial of the micropositioner which is on the order of 5%. Since for small values of displacement the strain is linearly related to the point displacement, this leads to an uncertainty of 5% in the strain. The sample thickness was determined to within 25 μm, so for the thinnest samples (575 μm) the possible error in sample thickness estimation is around 4%. The total error in the amount of strain estimate is on the order of 10%. More accurate results could be obtained by using an optical flex measurement system such as the KLA-Tencor FLX series [27]. However, the bending apparatus used for these experiments was not geometrically compatible with such a system.

It is important to note that the application of strain in one direction induces Poisson strain in the other two. The relationship between the applied strain and the induced strain is the constant known as Poisson's ratio. Fortunately, for this work

where [110] strain is applied to the (100) plane, Poisson's ratio is about 0.04 [28], so the Poisson strain is negligible. However, for other strain directions, Poisson's ratio can be as high as 0.28, at which point the Poisson strain should be considered.

Chapter 4

Strained Silicon Directly on Insulator

As seen in Chapter 2, ultra-thin silicon films have reduced carrier mobility due to quantum confinement effects. It would be advantageous to use an alternate channel material that has higher mobility to regain this lost mobility. Biaxially strained silicon pseudomorphically grown on lattice mismatched silicon germanium substrates is known to demonstrate higher mobility than unstrained silicon. At the time of this work, it had just been demonstrated that a strained silicon film could be transfered from a silicon germanium substrate to a handle wafer, creating a Strained Silicon Directly on Insulator (SSDOI) wafer.

This chapter presents some of the early device work done on SSDOI wafers that demonstrated that the material is suitable for building MOSFET devices and that the mobility enhancement over bulk is maintained after SSDOI substrate fabrication and a full MOSFET process. In addition, the film thickness and thermal budget constraints seen in bulk strained silicon/silicon germanium substrates seem to be alleviated in an SSDOI system.

4.1 SSDOI Substrate Fabrication

SSDOI substrates were provided by AmberWave Systems Inc. The "20%" SSDOI substrates were fabricated by direct transfer of a 50 nm strained silicon film from a relaxed $Si_{0.8}Ge_{0.2}$ graded buffer to a handle wafer as shown in Figure 4-1 [29]. Similar approaches have also been demonstrated by other groups [30, 31, 32]. Strained silicon films were epitaxially grown on a relaxed silicon germanium virtual substrate that had been planarized by chemical mechanical planarization (CMP) [33]. Wafers were implanted with hydrogen and wafer-bonded to an oxidized bulk silicon handle wafer. The bonded pair was annealed and the strained silicon/relaxed silicon germanium film released onto the handle wafer. A bond-strengthening anneal was performed at 800 °C for one hour. The solid-state germanium diffusion is negligible during this process, with a characteristic diffusion length of 0.4 nm and minimal strained silicon film relaxation. The remaining relaxed silicon germanium was removed by a combination of low temperature ($< 800°C$) steam oxidation and wet etching. The final strained silicon film thickness for a typical wafer was measured by ellipsometry to be 43.3 nm with a standard deviation of 2% across the wafer. The top surface roughness was measured by atomic force microscopy (AFM) to be 0.44 nm RMS on a 10×10 μm scale (Figure 4-2). No crosshatch was observed on the final SSDOI wafer surface due to the superior planarity of the polished silicon germanium virtual substrate. The tensile strain level of the SSDOI substrates is robust and fully maintained even after annealing at 1100 °C for 80 minutes as confirmed by UV-Raman measurements [34]. High thermal budget anneals of this type are not possible in bulk strained silicon/silicon germanium systems due to germanium diffusion.

4.2 Processing Conditions

Fully-Depleted n-MOSFETs were fabricated on the SSDOI substrates to investigate carrier transport and SSDOI film quality. As described in Chapter 3, the devices were built using a simple four mask process utilizing mesa isolation. The source/drain

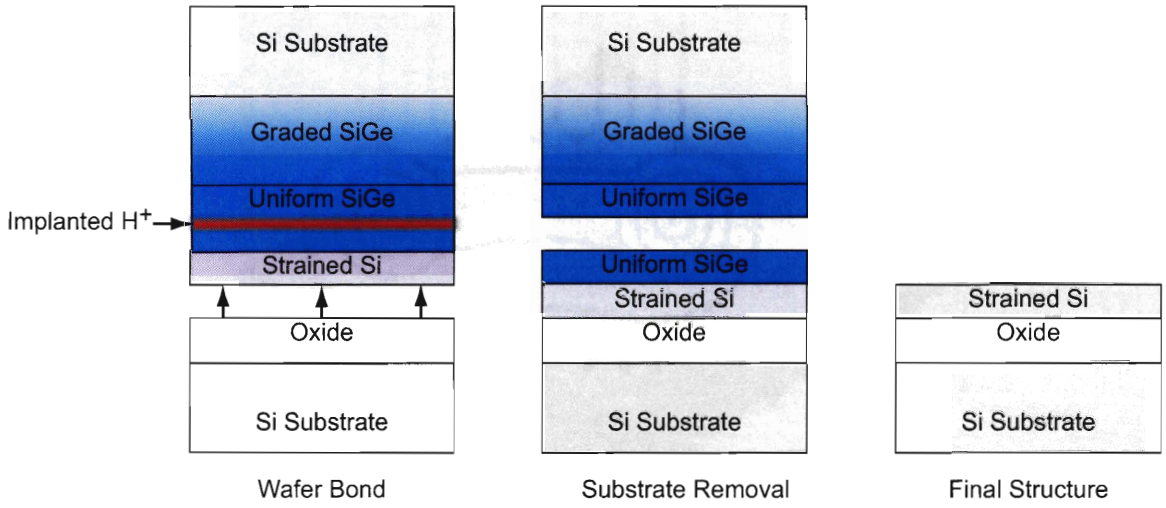


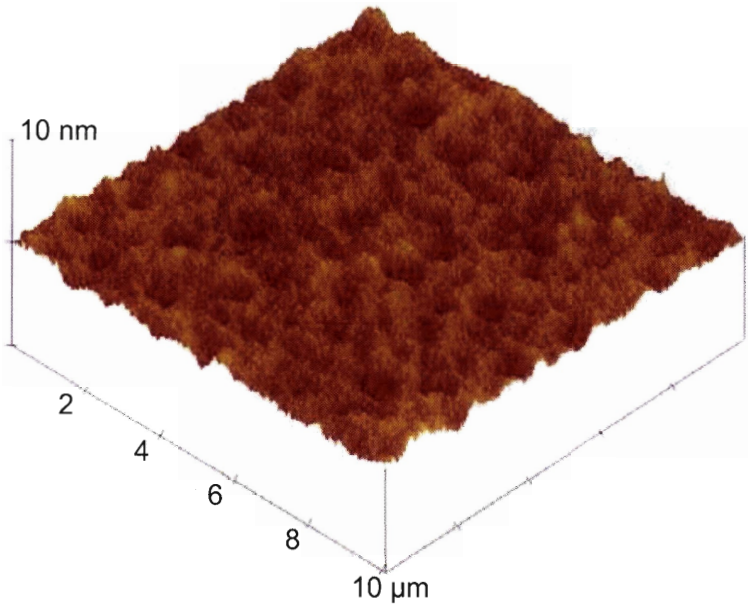
Figure 4-1: Fabrication process for SSDOI substrates.

areas were implanted with arsenic and activated by RTA for 5 s at 1080 °C. The gate oxide thickness was 9.4 nm and the remaining strained silicon film thickness after processing was 25-35 nm, both measured by ellipsometry. A cross-section TEM image of a completed device is shown in Figure 4-3. The gate oxide and film thickness as measured by TEM are in agreement with the ellipsometry data.

4.3 Device Results

Completed MOSFETs were measured and found to have good devices results. Transfer characteristics of a long-channel device are shown in Figure 4-4. The 66 mV/decade subthreshold slope is indicative of a fully-depleted device with good interface quality. Capacitance vs. voltage characteristics (Figure 4-5) show an effective oxide thickness (EOT) of 9.4 nm that matches the value given by ellipsometry and no visible poly depletion, indicated good dopant activation.

Figure 4-6(a) shows mobility vs. inversion layer density for 20% SSDOI compared to 20and control bulk silicon devices. SSDOI shows 112% enhancement over bulk silicon at $N_{inv} = 1 \times 10^{13}\ cm^{-2}$. Some enhancement is observed over bulk strained silicon/silicon germanium due to the lower effective field in SSDOI for equivalent inversion layer charge density. Figure 4-6(b) shows mobility versus effective field for



RMS = 0.44 nm

Figure 4-2: AFM image of the SSDOI wafer surface. RMS roughness is less than 0.5 nm.

SSDOI devices compared to bulk strained silicon/silicon germanium devices, control bulk silicon devices, and the universal curve for electrons in silicon [35]. Effective field was determined by $E_{eff} = (Q_b + 0.5Q_i)/\epsilon_{Si}$ where Q_b is the depletion charge. 20% SSDOI devices show the same enhancement over bulk silicon as bulk strained silicon/silicon germanium once effective field is taken into account, indicating that the biaxial tensile strain of the film has been fully maintained through device processing.

4.4 Misfit Dislocations

Figure 4-7 shows transfer characteristics of submicron length n-MOSFETs on three different substrates: 20% bulk strained silicon/silicon germanium below the critical thickness, 20% bulk strained silicon/silicon germanium above critical thickness, and 20% SSDOI with strained silicon far above critical thickness, with as-grown strained silicon film thicknesses of 12.5 nm, 20 nm, and 50 nm respectively. Plan-view trans-

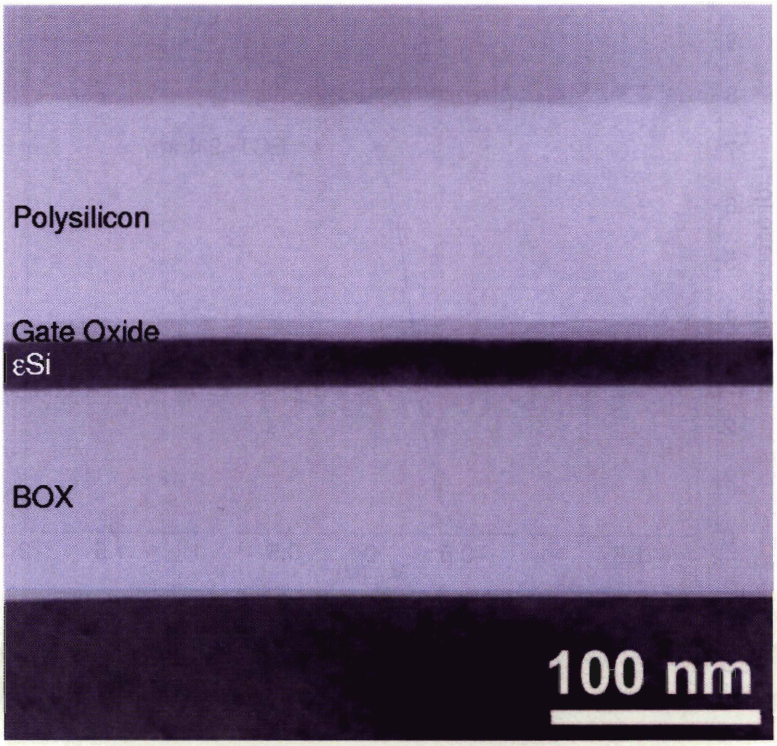


Figure 4-3: Cross-section TEM of an SSDOI device after processing. The gate oxide thickness is 9 nm and the silicon film thickness is 25 nm.

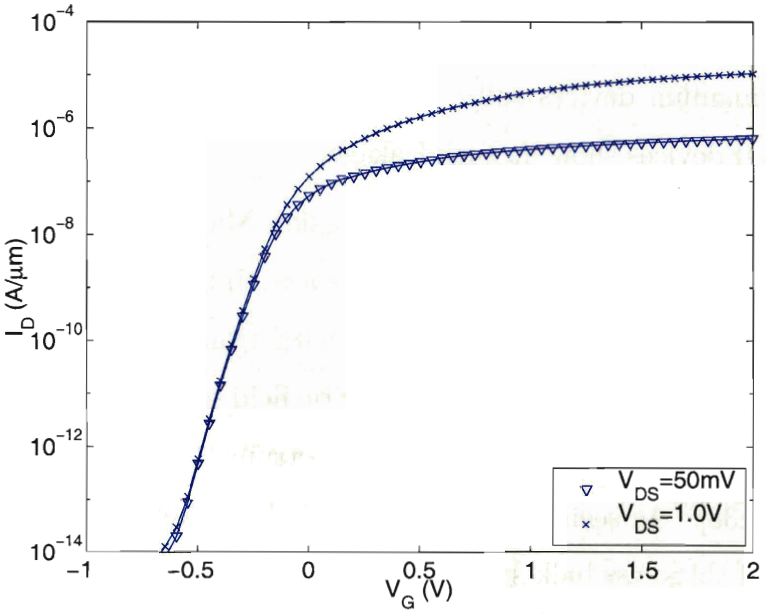


Figure 4-4: Transfer characteristics of a 50×50μm SSDOI n-MOSFET. Subthreshold slope is 66mV/decade due to the fully-depleted channel.

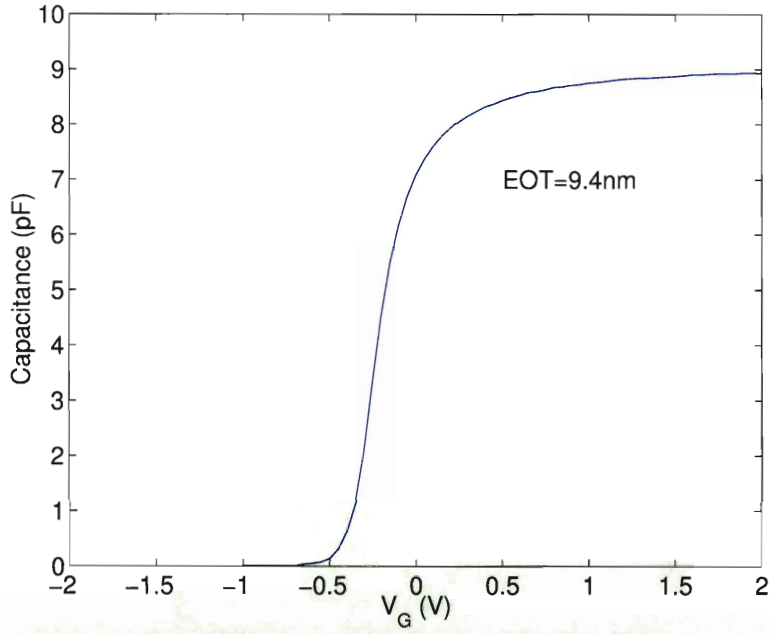
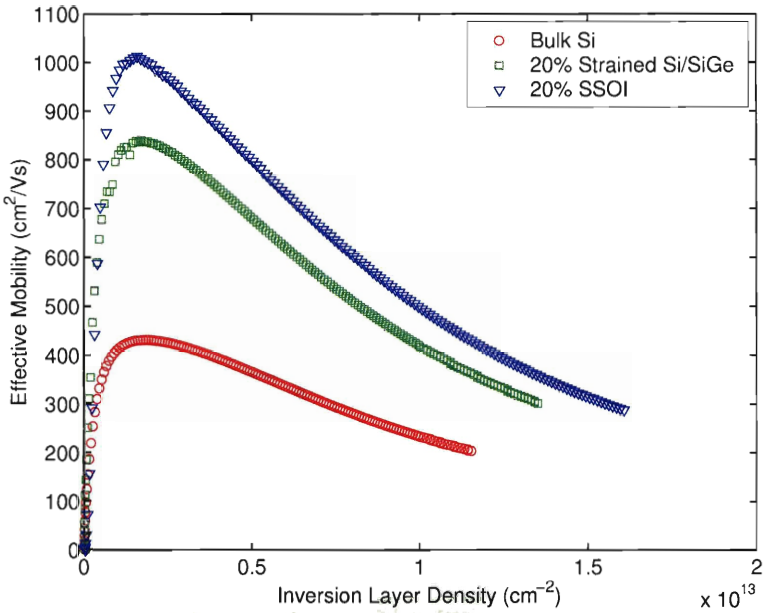


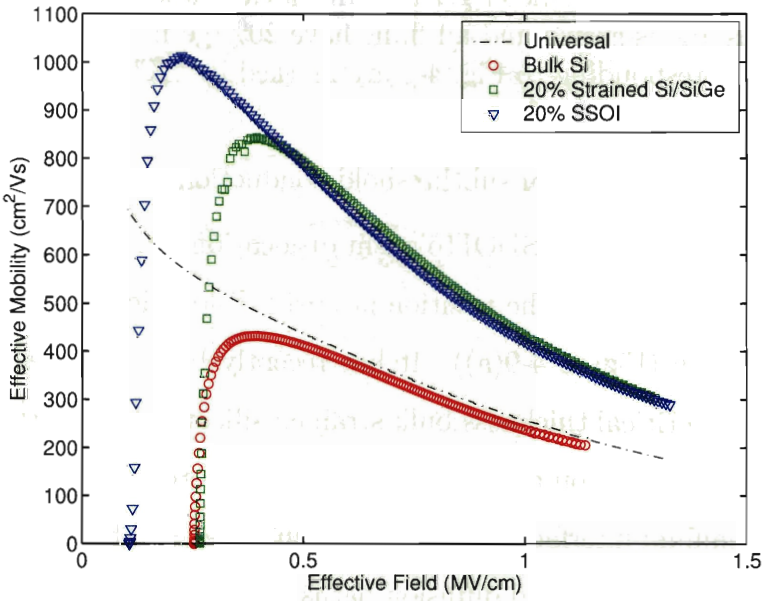
Figure 4-5: C_{GSD} for a 50×50μm SSDOI n-MOSFET. EOT is 9.4nm, matching ellipsometry and indicating low poly depletion and good dopant activation.

mission electron microscopy examination confirmed that the subcritical thickness bulk strained silicon/silicon germanium films were misfit-free, while the supercritical thickness bulk strained silicon/silicon germanium and SSDOI films had misfit dislocation spacings of several microns [37]. While supercritical thickness bulk strained silicon/silicon germanium devices suffer from high subthreshold leakage, supercritical thickness SSDOI devices show no such leakage.

To study this result further, Photon Emission Microscopy (PEM) was used to study leakage current paths in the different devices. In PEM, a long exposure micrograph of an electrically biased device is taken with a camera with a cooled, low noise CCD imager. Carriers accelerated by the electric field scatter and and give off energy in the form of photons with a broad energy spectrum (1.2-2.4 eV) that are collected by the camera [38]. As seen in Figure 4-8(c), light emission is highly localized for the supercritical thickness bulk strained silicon/silicon germanium device, indicating misfit dislocation-induced leakage. However, the off-current distribution is uniform along the channel width for the subcritical thickness bulk strained silicon/silicon germanium devices in Figure 4-8(b) and the supercritical thickness SSDOI devices in



(a)



(b)

Figure 4-6: Electron mobility for 50 × 50 μm bulk, 20% bulk strained silicon/silicon germanium (T_{Si}=12.5 nm), and 20% SSDOI devices (T_{Si}=50 nm). SSDOI displays enhancement over both bulk silicon and and bulk strained silicon/silicon germanium vs. inversion layer charge density (a), but similar enhancement vs. effective field (b), indicating that the tensile strain of the SSDOI film was maintained through device processing [36].

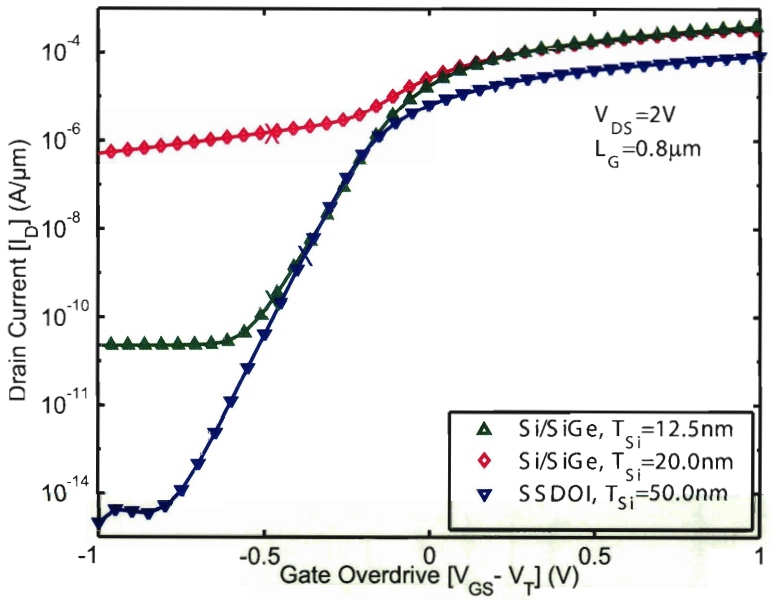
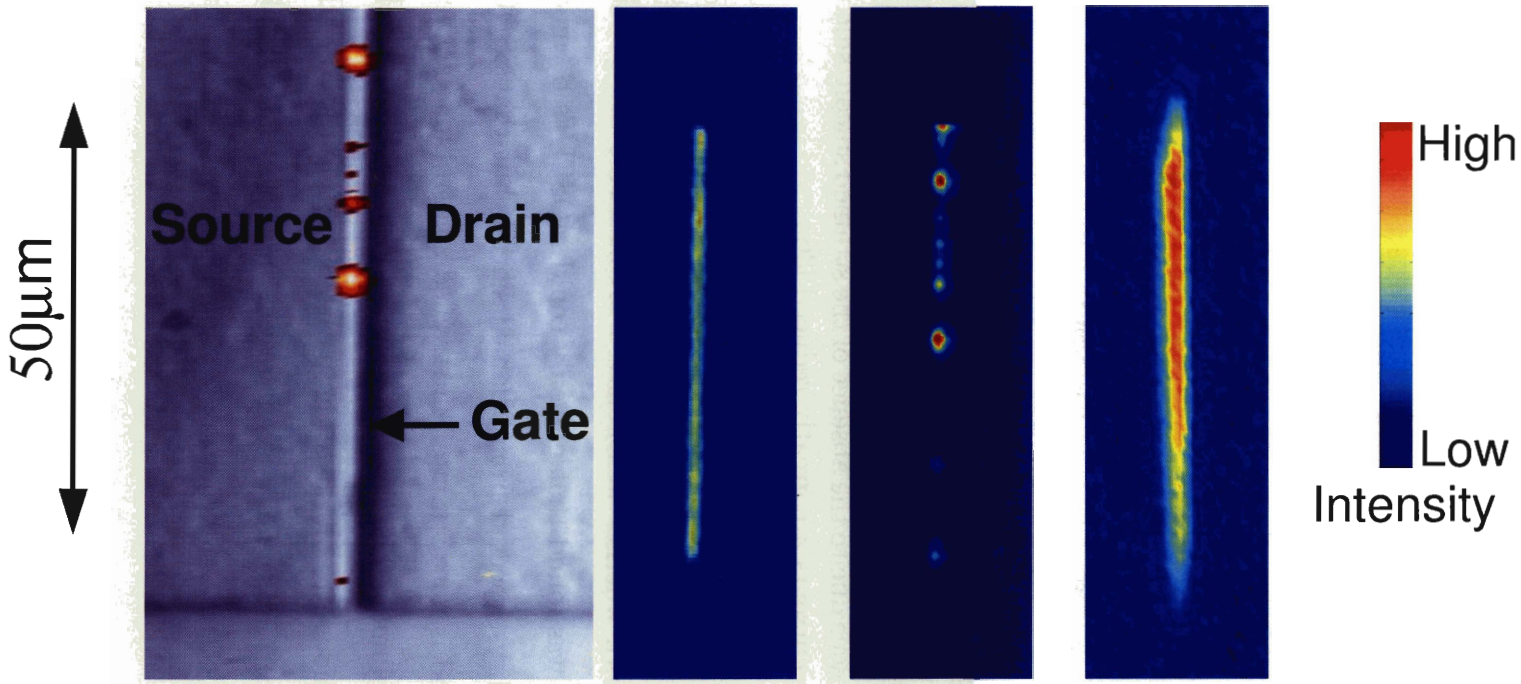


Figure 4-7: Comparison of transfer characteristics for bulk strained silicon/silicon germanium devices below the critical thickness (12.5 nm), above the critical thickness (20.0 nm), and SSDOI above the critical thickness (50.0 nm). Excess leakage is only observed in strained silicon/silicon germanium devices above the critical thickness. Layer thicknesses are as-grown and all films have 20% germanium equivalent strain. Bias conditions corresponding to Fig. 4-8 are marked by "X" on each curve [36].

Figure 4-8(d), indicating normal subthreshold conduction.

The apparent immunity of SSDOI to misfit dislocation-induced leakage current can be understood by considering the position of misfit dislocations in the silicon/silicon germanium structure (Figure 4-9(a)). It has recently been shown that the leakage mechanism in supercritical thickness bulk strained silicon/silicon germanium devices is localized enhanced diffusion along misfit dislocation cores found at the strained silicon/silicon germanium interface [37], a theory reinforced by the fact that dislocation cores are known to serve as rapid diffusion paths [39]. It appears that SSDOI devices are not affected by misfit induced leakage because the misfit dislocation cores at the strained silicon/silicon germanium interface and the associated enhanced diffusion paths are eliminated during the SSDOI wafer fabrication process leaving only threading dislocation segments (Figure 4-9(b)). While the remaining threading dislocation segments may have an impact on device yield or reliability and should be studied further, we have seen no detrimental effects thus far.



(a) Merged image (b) Si/SiGe, T_{Si}=12.5nm (c) Si/SiGe, T_{Si}=20.0nm (d) SSDOI, T_{Si}=50.0nm

Figure 4-8: In the merged reflected light and emitted light image of a strained silicon/silicon germanium MOSFET gate region (a) emitted light emerges near the gate in discrete locations highlighting misfit dislocation-induced leakage paths. PEM images of n-MOSFETs with subcritical (b) and supercritical strained silicon film thicknesses (c) on bulk strained silicon/$Si_{0.8}Ge_{0.2}$, and supercritical strained silicon film thicknesses on 20% SSDOI (d) show the relative uniformity of light emission when the devices are biased in subthreshold as marked in Figure 4-7. Uniform emission in (b) and (d) indicates that subcritical bulk strained silicon/silicon germanium and supercritical SSDOI do not have misfit dislocation induced leakage paths, while the non-uniform emission in (c) is due to misfit dislocation-induced leakage in supercritical bulk strained silicon/silicon germanium [36].

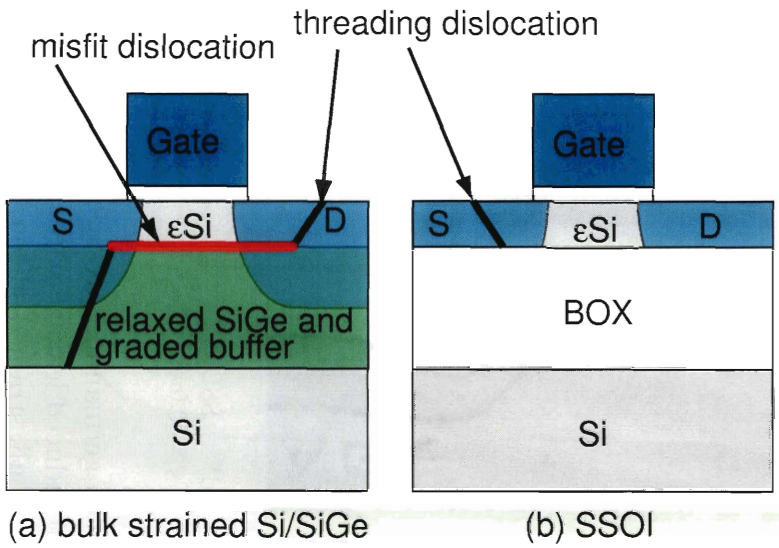


Figure 4-9: Schematics of (a) bulk strained silicon/silicon germanium device and (b) SSDOI device with supercritical strained silicon thicknesses. Diffusion along the misfit dislocation core shorts source (S) and drain (D) for the bulk strained silicon/silicon germanium device, greatly elevating leakage current. In contrast, misfit dislocations cores do not exist in the SSDOI device due to the absence of the strained silicon/silicon germanium interface and leakage currents are greatly reduced [36].

4.5 Conclusions

Prior to this work, it was unknown whether well behaved MOSFETs could be fabricated on SSDOI substrates. It was found that not only could MOSFETs be made that showed the improved mobility expected from strained silicon, but that SSDOI has superior thermal stability and is not as limited in strained silicon film thickness as strained silicon/silicon germanium is. This revelation hinted at the ability to make SSDOI wafers with films thick enough to fabricate the partially-depleted MOSFETs that are currently used in production. In fact, recent results indicate that partially depleted devices can be built on SSDOI, and that nontrivial circuits benefit from this technology [40].

Chapter 5

Applying Uniaxial Strain

Process-induced uniaxial strain has become an important method of increasing MOSFET performance in recent years. By using techniques such as stressor films [41] and replacement source/drains [42] it is possible to increase on-current by means other than traditional scaling. Because of the importance of this technique, the impact of uniaxial strain on new material systems must be examined when considering their possible implementation.

SOI and SSDOI NMOS and PMOS devices with relatively thick and ultra-thin channels were studied. Kelvin-structure MOSFETs were measured with different levels of uniaxial strain mechanically applied using the bending apparatus described in Chapter 3. By applying mechanical uniaxial strain rather than process-induced strain, it is possible to directly study the effects of the strain separate from the effects of processing, and it is possible to vary the magnitude of tensile and compressive strain on the same device. Uniaxial strain can also be applied perpendicular to the direction of current in the device, something that is impractical with current methods used to produce process-induced strain.

5.1 NMOS Device Results

Electron mobility vs. charge density for devices without any applied uniaxial strain is shown in Figure 5-1. The curves for bulk and thick SOI overlay each other as

expected since they have undoped channels and were co-processed. Thick SSDOI shows enhanced mobility over bulk and thick unstrained SOI. The ultra-thin SOI and SSDOI devices experience mobility degradation from quantum confinement effects.

Figure 5-2(a) shows change in electron mobility vs. inversion layer density for a bulk NMOS device with multiple values of uniaxial strain applied parallel to the channel direction (longitudinal strain), while Figure 5-2(b) shows the effects of uniaxial strain applied perpendicular to the channel (transverse strain). The enhancement with longitudinal strain is relatively constant with inversion layer density. However, for transverse strain, the level of enhancement is less and it falls off with increasing inversion layer density. The same characteristics are shown in Figure 5-3 for SSDOI. SSDOI devices exhibit less enhancement with longitudinal strain than bulk devices, but the level of enhancement is still relatively constant with inversion layer density. For transverse strain, the mobility is actually reduced, and gets increasingly worse with increasing inversion layer density.

Electron mobility modulation vs. strain for NMOS bulk, thick and thin SOI, and thick and thin SSDOI are summarized in Figure 5-4 for longitudinal strain and in Figure 5-5 for transverse strain respectively. Bulk and thick SOI devices show very similar characteristics as expected. Thin SOI devices exhibit the highest sensitivity to uniaxial strain. All devices exhibit markedly different response to longitudinal and transverse strain. This anisotropy of the mobility modulation is most apparent in the SSDOI devices where longitudinal tensile strain enhances mobility while transverse tensile strain degrades mobility.

5.1.1 Electrons in Ultra-Thin SOI

The dependence of mobility enhancement on film thickness may be explained by examining mechanism of mobility degradation in thin films in detail. Figure 5-6 shows the wave functions of electrons in the Δ_2 and Δ_4 valleys for bulk and a 5 nm thick film. The wave function of the electrons in Δ_4 valleys of the bulk device is broader than the thickness of the 5 nm film. This leads to thickness-induced confinement of the carriers in the SOI device that degrades mobility through increased phonon scattering

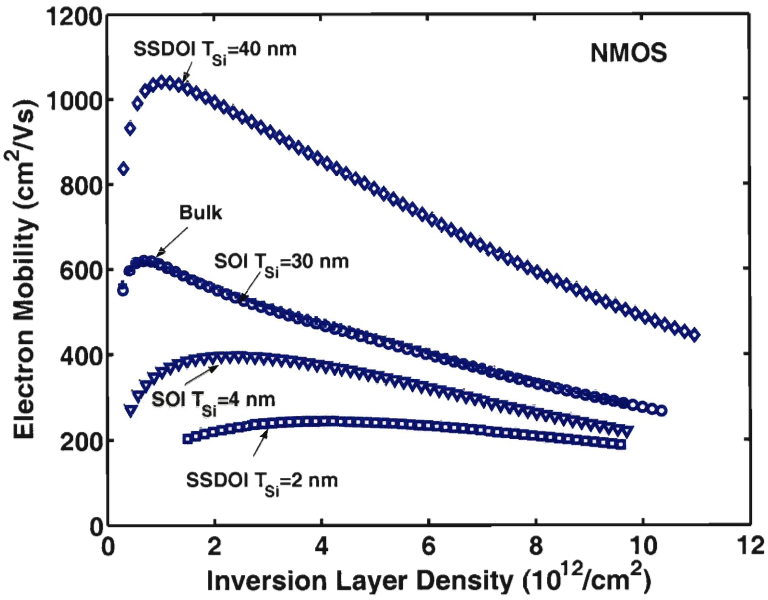
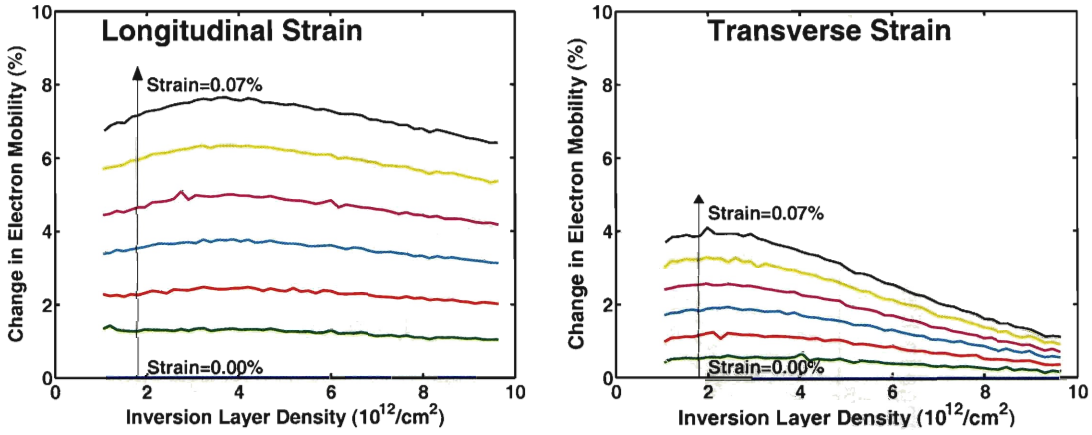


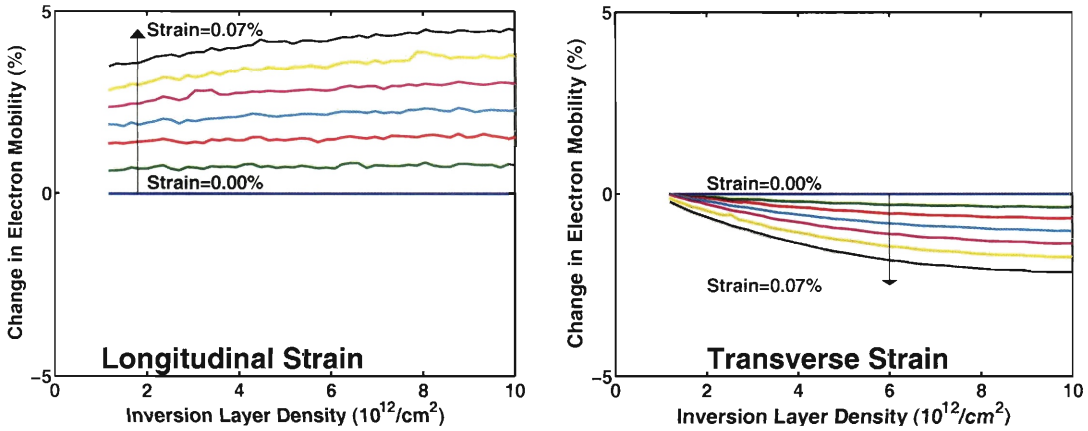
Figure 5-1: Electron mobility vs. inversion layer density with no applied strain. Thin devices exhibit lower mobility due to surface roughness and quantum confinement effects.



(a) Longitudinal Strain

(b) Transverse Strain

Figure 5-2: Percent change in electron mobility vs. inversion layer density for increasing levels of (a) longitudinal and (b) transverse tensile strain applied to a bulk NMOSFET. Band splitting arguments cannot explain the difference between (a) and (b). Longitudinal strain yields a relatively constant enhancement vs. inversion layer density, while transverse strain loses enhancement at high inversion layer density.



(a) Longitudinal Strain

(b) Transverse Strain

Figure 5-3: Percent change in electron mobility vs. inversion layer density for increasing levels of (a) longitudinal and (b) transverse tensile strain applied to a thick SSDOI NMOSFET. While longitudinal strain enhances mobility, transverse strain degrades it.

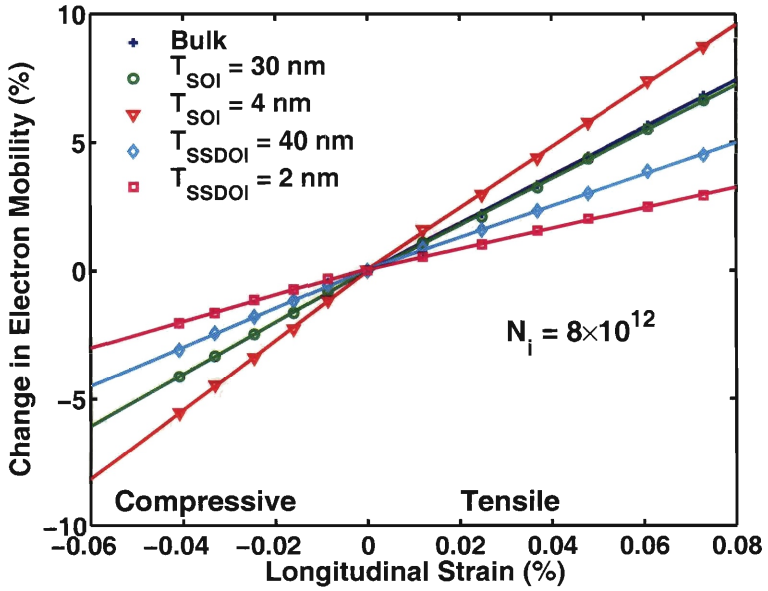


Figure 5-4: Percent change in electron mobility vs. level of applied longitudinal strain. Thin SOI devices show the most sensitivity to strain. SSDOI devices do receive enhancement from additional tensile strain.

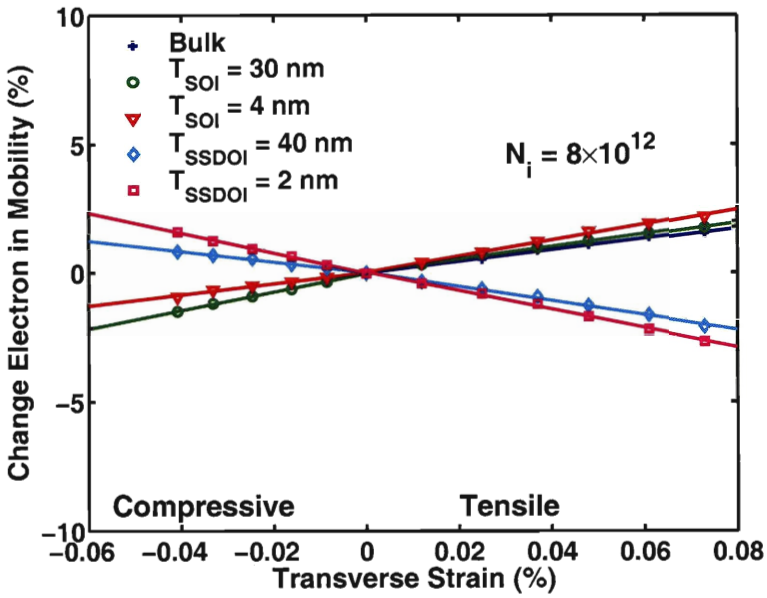


Figure 5-5: Percent change in electron mobility vs. level of applied transverse strain. SSDOI mobility is enhanced by transverse compressive strain.

and increased interaction with the buried oxide interface. However, the electrons in the Δ_2 valleys have a narrower wave function due to their higher quantization mass and are nearly unaffected by the thickness of the film. The application of strain splits the energy levels of the valleys further, resulting in lower occupation of the degraded Δ_4 valleys. Therefore, strain enhances mobility in thin films not only by transferring carriers to valleys with lower effective mass, but also transferring carriers out of valleys suffering from thickness-induced confinement.

5.1.2 Anisotropic Electron Mobility Modulation

For (100) silicon with strain applied in the [110] direction, electron repopulation due to band-splitting does help explain electron mobility modulation [44], but it cannot explain its anisotropy. All the the Δ_4 valleys should be affected equally by strain in the [110] direction. Irie et al. observed this effect and found that it was independent of temperature, thus eliminating anisotropic phonon scattering as the cause [45]. The remaining explanation is an anisotropic change in effective mass.

Early work on uniaxial strain in bulk silicon using cyclotron resonance character-

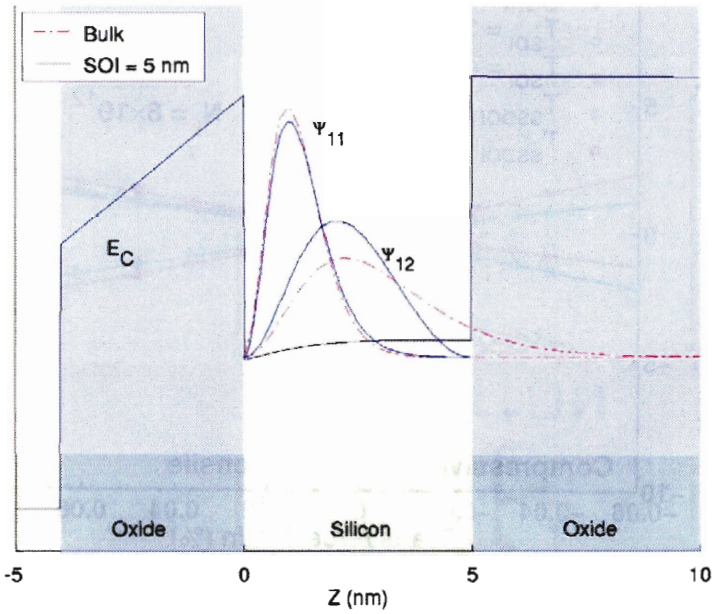


Figure 5-6: Schred simulation of the wavefunctions of electrons in the Δ_2 valleys (Ψ_{11}) and Δ_4 (Ψ_{12}) valleys of a bulk and ultra-thin SOI device for $N_i = 1 \times 10^{13}/cm^2$. Carriers in the Δ_4 valleys suffer from confinement while carriers in the Δ_2 valleys are relatively unaffected [43].

ized the change in effective mass with [110] strain for electrons [13]. The Δ_4 valleys see little effect, while the Δ_2 valleys see an angular dependent change in effective mass as shown in Figure 2-10. Since there is little band distortion from the biaxial strain, the distortion caused by uniaxial strain on SSDOI is likely to be similar to the bulk case. Because of the already pronounced band-splitting in the SSDOI devices, a larger proportion of the carriers are populated in the Δ_2 valleys and experience the effective mass change, explaining why SSDOI shows the greatest anisotropy in electron mobility.

5.2 PMOS Device Results

Hole mobility vs. charge density for devices without any applied strain is shown in Figure 5-7. The thick SSDOI devices show enhanced mobility over the thick SOI devices, while the ultra-thin SOI and SSDOI suffer from quantum confinement.

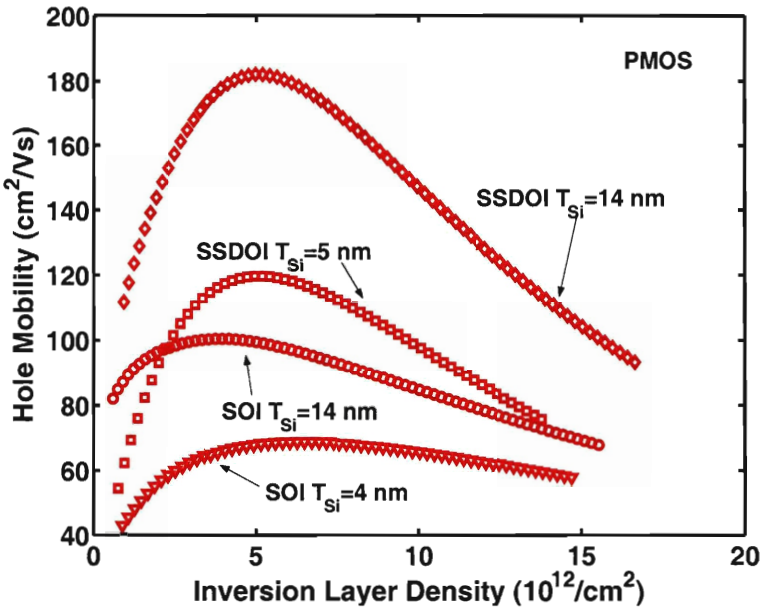
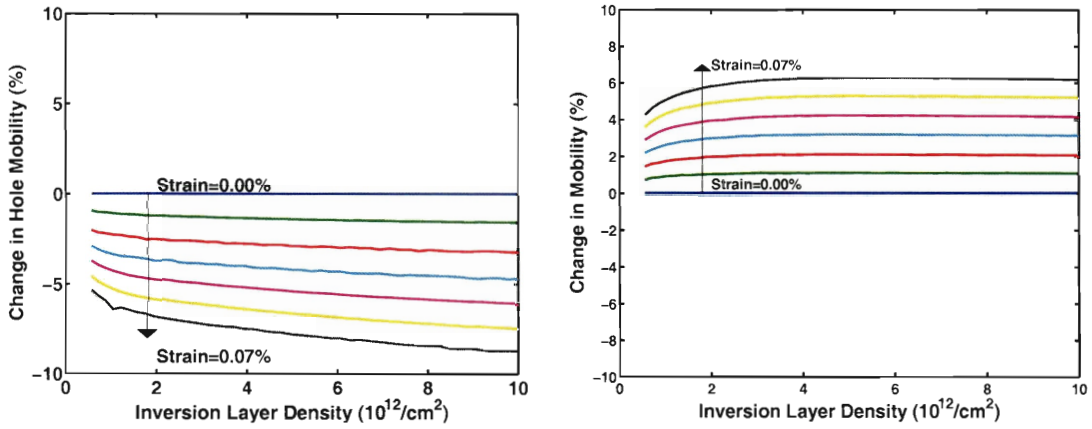


Figure 5-7: Hole mobility vs. inversion layer density with no applied strain. Thin device mobility is degraded by quantum confinement and surface roughness.

Mobility modulation vs. strain is summarized for thick and thin PMOS SOI and SSDOI in Figure 5-9 for longitudinal strain and in Figure 5-10 for transverse strain. The PMOS SSDOI devices exhibit similar levels of enhancement with applied tensile uniaxial strain regardless of strain direction or film thickness.

The insensitivity of the uniaxial strain dependence of hole mobility modulation to film thickness is markedly different from the corresponding dependence for electrons. The majority of the mobility enhancement that holes experience from uniaxial strain is from the effective mass change rather than sub-band repopulation. This means the sub-band repopulation caused by thickness-induced confinement has little impact on the response of the mobility to strain. Unlike the case of electrons in ultra-thin silicon films where the strain-induced repopulation helps offset the thickness-induced mobility degradation, the repopulation that occurs for holes has a smaller impact on mobility than the effective mass change. Therefor, the dominant mobility modulation mechanism is the same for thick and ultra-thin films and they show a similar response.

The different response seen in hole mobility to uniaxial strain in SOI and SSDOI is more difficult to predict. Compared to the conduction band, the valence band structure of silicon experiences more distortion from both uniaxial and biaxial strain [17].



(a) Longitudinal Strain

(b) Transverse Strain

Figure 5-8: Percent change in hole mobility vs. inversion layer density for different levels of (a) lateral and (b) transverse strain.

Since low levels of biaxial strain degrades hole mobility while high levels enhance it, it is reasonable that while longitudinal uniaxial tensile strain degrades SOI hole mobility, it enhances SSDOI hole mobility.

5.3 Discussion

Table 5.1 summarizes the gauge factor (defined here as % change in mobility / % tensile strain) for all of the devices measured at high inversion layer density. Also included is the gauge factor from Zhao et al. for partially-depleted SOI devices [46]. The results here have a slightly larger gauge factor than the work of Zhao, most likely because Zhao makes no attempt to correct for series resistance.

By converting stress to strain using a value of 170 GPa for Young's modulus for the [110] direction on the (100) plane [28], the piezoresistance coefficients of bulk silicon (not an inversion layer) from the literature [47] can be compared to these gauge factors. The gauge factor for electrons in an inversion layer is higher than that of the bulk material and displays more anisotropy, most likely due to the higher population of the Δ_2 valleys in an inversion layer. For holes, the longitudinal gauge factor for bulk piezoresistivity and unstrained SOI is similar, while the transverse gauge factors

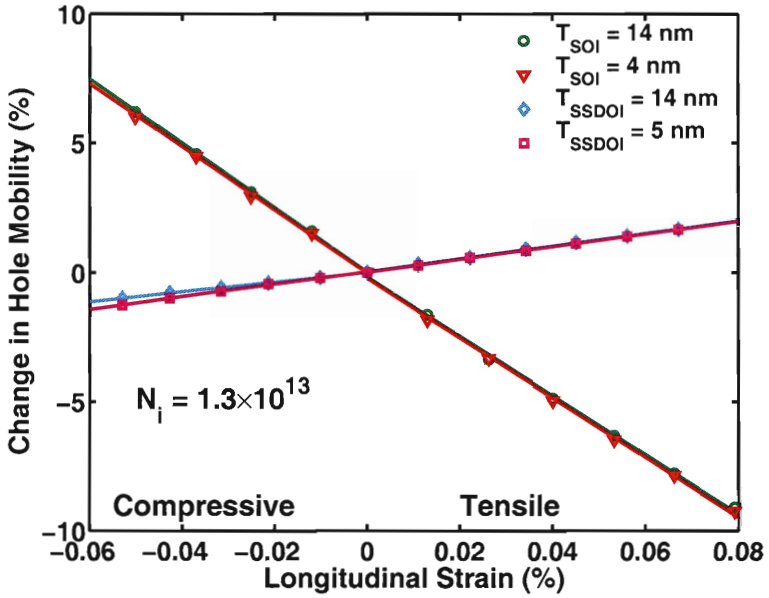


Figure 5-9: Percent change in hole mobility vs. level of applied longitudinal strain. SSDOI devices mobility is enhanced by longitudinal tensile strain while SOI device mobility is degraded.

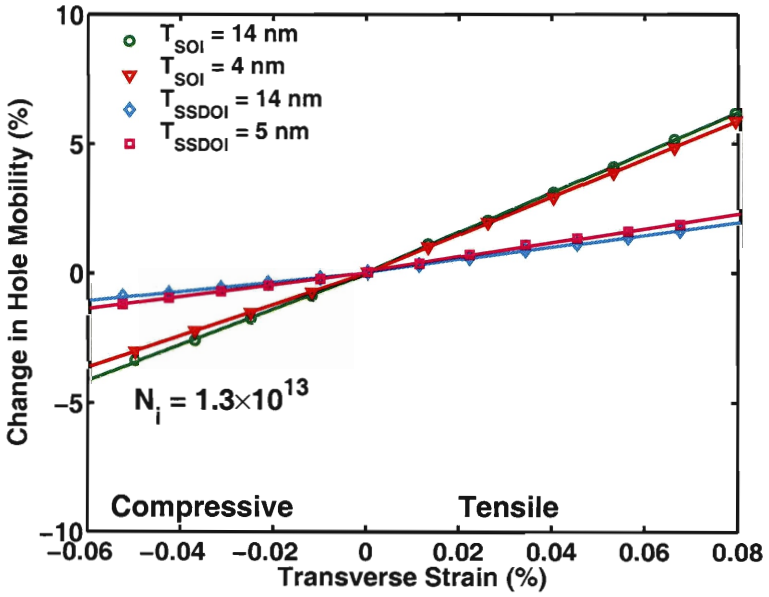


Figure 5-10: Percent change in hole mobility vs. level of applied transverse strain. All PMOS device mobilities are enhanced by transverse tensile strain.

	NMOS		PMOS	
	longitudinal	transverse	longitudinal	transverse
Bulk	93	22		
Zhao, PDSOI [46]	80	19	-110	62
Thick SOI	91	25	-115	77
Ultra-Thin SOI	119	31	-116	73
Thick SSDOI	62	-28	24	24
Ultra-Thin SSDOI	40	-36	24	28
Smith, piezoresistance [47]	53	30	-122	112
Hensel, effective mass [13, 16]	8	-10	-55	51

Table 5.1: Mobility, piezoresistance, and effective mass gauge factors for strain applied longitudinal or transverse to the channel. Positive numbers indicate enhancement with tensile strain while negative numbers indicate enhancement with compressive strain. Mobility gauge factor (% change in mobility / % tensile strain) is given for high inversion layer density. Piezoresistance coefficients (% change in resistance / % tensile strain) and change in effective mass (% change in effective mass / % tensile strain) are included for reference.

differ. This may be due to the difference in populations of the light hole and heavy hole bands between the bulk material and an inversion layer.

Similarly, the change in effective mass of carriers in the Δ_2 valleys found by Hensel et al. [13, 16] can be converted to a gauge factor for comparison to these results. The change in effective mass for electrons appears small compared to the change in mobility observed. However, it must be noted that while effective mass occurs explicitly in the equation for mobility ($\mu = |qm^*/\tau$), it also occurs indirectly in τ by appearing in all scattering rate calculations, leading to a stronger than linear relationship (which is different for each scattering mechanism). It is interesting to note that for electrons in unstrained silicon, where the band splitting caused by uniaxial strain still results in considerable carrier repopulation, the gauge factor is positive in both the longitudinal and transverse directions. The gauge factor is lower in the transverse direction than the longitudinal direction, which is the manifestation of the increased effective mass in that direction competing with the increased mobility conferred by the lower scattering rates caused by the band splitting. In biaxially strained silicon, most of the electrons are already present in the Δ_2 valleys, so the

additional band-splitting from the application of uniaxial strain is less beneficial, leading to the mobility gauge factor showing the same sign dependence as the effective mass. For holes, the effective mass change has a similar magnitude in the longitudinal and transverse directions, much like the piezoresistance coefficients. However, the split in degeneracy between the light hole and heavy hole bands in an inversion layer leads to a different dependence. For biaxially strained silicon, the starting band structure before the application of uniaxial strain is different than in bulk silicon, making the difference between the response of hole effective mass in unstrained silicon with uniaxial strain and the response of hole mobility in SSDOI to uniaxial strain unsurprising.

5.4 Conclusions

Since longitudinal uniaxial strain is the most common type of strain utilized for performance enhancement, it is interesting to note that while for unstrained films it is advantageous to apply tensile strain to NMOS and compressive strain to PMOS, both NMOS and PMOS SSDOI benefit from tensile strain, making uniaxial strain integration in SSDOI potentially simpler.

In this work a large anisotropy in the electron mobility is observed when uniaxial strain is applied to NMOSFETs. This results from a change in effective electron mass with uniaxial strain. The anisotropy is most pronounced in biaxially strained silicon because the existing band splitting repopulates most of the carriers into the Δ_2 valleys that exhibit the mass anisotropy.

For values of uniaxial and biaxial strain that give similar long channel electron mobility enhancement, the uniaxial case will have a lower effective mass and will therefore have greater improvement in short-channel current than the biaxial case.

In addition, it is found that uniaxial tensile strain applied along the channel direction benefits both NMOS and PMOS SSDOI, making uniaxial strain integration potentially simpler in that technology.

Chapter 6

Conclusions

The data presented earlier in this these provide insight into some of the mechanisms that govern mobility in strained and thin films. This chapter looks deeper into some of the implications that these observations have on the prospects of ultra-thin film devices.

6.1 Film Thickness Variation

The characteristics of thin film devices are very dependent on film thickness. Short channel effects such as DIBL change dramatically for slightly different values of film thickness. Threshold voltage is also strongly dependent on film thickness, and as such small variations in film thickness lead to large fluctuations in threshold voltage. The concern addressed most directly by the work presented here is the strong dependence of mobility on film thickness.

When so many important device characteristics are tied so closely to one parameter, variations in the parameter can have a huge impact on the device. In this case, variations in film thickness will severely impact performance, repeatability, and yield.

Thankfully, silicon has properties that seem compatible with maintaining good film uniformity. On a global level, thinning the film through oxidation results in improved uniformity. On a short-range level, oxidation smoothes the film on both the top and bottom interfaces. There does appear to be a minimum surface roughness

that could limit the minimum practical silicon film thickness. Oxidation experiments on initially smooth and initially rough (100) silicon surfaces resulted in a convergence at a 0.3 nm surface roughness [48], hypothesized to be due to the random diffusion and reaction of oxygen at the silicon/oxide interface.

It is encouraging to note for electrons that the strong dependence on film thickness occurs when the carriers are confined by the film rather than the electric field. This means that the effects that we see in threshold voltage and mobility degradation can be postponed to thinner silicon films by the application of biaxial strain. If biaxial strain is used to re-populate carriers into the Δ_2 valleys, the effective "size" of the electrons is much smaller than if they were in the Δ_4 valleys. SSDOI should not suffer from strong shifts in threshold voltage and mobility at the same film thickness as SOI. The sensitivity of threshold voltage on film thickness (defined as $\frac{\delta V_T}{\delta T_{Si}}$) versus film thickness for unstrained silicon, silicon with carriers only in the Δ_2 valleys and for silicon with carriers only in the Δ_4 valleys, calculated using the Schrödinger-Poisson solver Schred [25], is given in Figure 6-1. The case with carriers only found in the Δ_4 valleys is the extreme case of biaxial compression. For reasonable values of strain, the response would fall between the extreme case and the unstrained silicon case. For biaxial compression, we see increased sensitivity to film thickness that would make process control in this thickness regime very difficult. The case with carriers only in the Δ_2 valleys is analogous to using biaxially tensile strained silicon. In this case, we see an advantageous reduced sensitivity to film thickness variations in the range of 4-10 nm thick films.

6.2 Uniaxial Strain

The observation that uniaxial stain impacts carrier mobility by different mechanisms than biaxially strain is important in that while both result in increased low lateral-field long-channel mobility, the impact on short channel performance should be expected to be different.

Short-channel devices built on biaxially strained silicon wafers have significantly

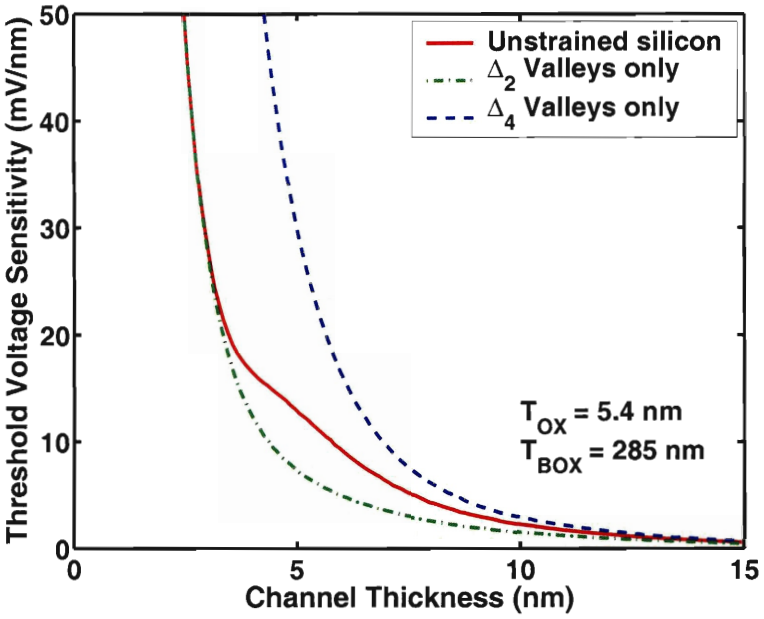


Figure 6-1: Threshold voltage sensitivity vs. film thickness for electrons. The unstrained silicon case is straddled by the case where electrons are only allowed in the Δ_2 valleys (extreme biaxial tension case) and where electrons are only allowed in the Δ_4 valleys (extreme biaxial compression case). Biaxially tensile strained silicon should show reduced sensitivity to film thickness variations than unstrained silicon for the range of 4-10 nm.

less current enhancement over similar bulk devices than the enhancement in long-channel mobility would indicate [49]. Possible explanations for this are strain relaxation during processing, the increased importance of coulombic scattering in the highly-doped channels of short-channel devices, and the effects of the ratio between gate length and mean-free-path leading to quasi-ballistic transport.

When the carriers are transported from the source to the drain without scattering, the device is said to be ballistic and the current in the device is given by Assad et al. [50] as

$$I_D = WC_{ox}(V_{GS} - V_T)v_{inj} \tag{6.1}$$

where v_{inj} is the injection velocity given for the degenerate case as

$$v_{inj} = \frac{4\hbar}{3m_c}\sqrt{2C_{ox}(V_{GS} - V_T)/q\pi} \tag{6.2}$$

In this case, the drain current is independent of gate length and mobility. The reduced scattering rates that improve mobility in biaxially strained films become irrelevant in a device where no scattering occurs. The repopulation into the Δ_2 valleys will cause some improvement in current as the conduction mass (m_c) in the Δ_2 valleys is lower and will hence somewhat increase the injection velocity. While silicon MOSFETs do not operate at the ballistic limit, they do operate at 30-40% of the ballistic limit [51], making the injection velocity an important parameter.

While the mobility enhancement from biaxial strain has not translated fully to current enhancement in short channel devices, improving performance by adding uniaxial strain to these devices has been very successful. Process-induced strain is added towards the end of device processing so strain relaxation should be minimal. The change in effective mass caused by uniaxial strain enhances mobility regardless of the scattering mechanism. This is especially important when the channel is highly doped as it is in short-channel devices because of the importance of coulombic scattering. Also, the change in effective mass caused by uniaxial strain increases the injection velocity, so it directly increases current even in a fully ballistic MOSFET.

6.3 Conclusions

In conclusion, it appears that to scale thin-film based NMOS devices to their fullest potential, both biaxial strain and uniaxial strain should be employed together. Biaxial strain results in more electrons being populated in the Δ_2 valleys. This allows less sensitivity to film thickness due to the reduced spatial extent of their wavefunction. Uniaxial strain further enhances the transport characteristics of the resulting film by modulating the electron effective mass.

6.4 Contributions from this work

- Developed techniques for fabricating ultra-thin body MOSFETs.
- Demonstrated some of the first SSDOI MOSFETs.
- Confirmed enhanced mobility in SSDOI MOSFETs.
- Discovered apparent immunity of supercritical SSDOI to misfit defects.
- Developed methodology for electrically extracting SOI film thickness from C-V characteristics taken using applied substrate bias and matching them with Schrödinger-Poisson simulations.
- Discovered that ultra-thin NMOSFETs exhibit more mobility enhancement from tensile uniaxial strain than bulk or thick SOI.
- Performed first study of the effects of uniaxial strain on thick SSDOI and ultra-thin SSDOI.
- Investigated in-plane mobility anisotropy caused by the application of uniaxial strain for electrons and holes.

6.5 Suggestions for Future Work

- Investigate the limits of oxidative smoothing. Is 0.3 nm the limit?

- Determine the mechanism responsible for the improvement of global SOI thickness uniformity during oxidation. Determine the oxidation conditions that maximizes this effect.
- Examine the response of mobility to higher values of uniaxial strain.
- Compare the mobility vs. SOI thickness dependence of unstrained films with that of uniaxially and biaxially strained films.
- Calibrate electron mobility models that include uniaxial strain to the data presented in Chapter 5. The mobility modulation is larger than the effective mass modulation is expected to be. When all of the scattering terms are accounted for in detail, does the change in effective mass fully explain the data?
- Model the band structure of holes with both biaxial and uniaxial strain applied at the same time and compare with the data from Chapter 5.

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