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Active Pixel Sensors for X-ray Astronomy

by

Matthew Cohen

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Abstract

An active pixel sensor array, APS-1, has been fabricated for the purpose of scientific x-ray detection. This thesis presents the results of testing the device. Alternate design architectures are explored. Recommendations are made for a next-generation sensor.

CCDs have been the dominant x-ray sensor in astronomy for over ten years. Limitations inherent to CCDs are starting to become important. Active pixel sensors (APS) provide an alternate architecture that may solve these problems.

APS-1 is a first-generation sensor designed by Lincoln Laboratory's Advanced Silicon Technology Group. APS-1 is fabricated in a fully depleted silicon-on-insulator (FDSOI) technology. FDSOI is especially well-suited to produce a scientific x-ray imager. The device includes sixteen different pixel variations to determine the processing parameters that can produce the best imager. Dark current, noise, and responsivity of the various pixel designs was measured using an electronics system adapted from a CCD test system. X-rays were detected at room temperature.

Ordinary active pixels have high noise levels ($\sim$ 70 electrons). Many pixel designs capable of lower noise have been presented in the literature. Active reset, pixel-level CDS, and CTIA pixel designs are discussed in detail and simulated.

A second-generation sensor from Lincoln Laboratory, using pixel-level CDS, is discussed. This device, APS-2, will be available for testing in 2006. APS-2 simulation results are presented. It is expected to have an input-referred noise of less than five electrons, near the performance of modern CCDs.

Thesis Supervisor: Mark W. Bautz
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I also must thank my co-supervisor Kent Lundberg. Dr. Lundberg took me on as a thesis advisee relatively recently, when I discovered that I needed to have a co-supervisor. He, more than anyone, is responsible for this being a complete thesis. Dr. Lundberg kept pushing me to get more accomplished, even when I didn't seem to be listening. He has devoted a significant amount of time to this project even though it is not related to his research. Thanks for sticking with me.

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We celebrated my 'graduation' over two months ago, and now I'm actually finishing. Thanks for encouraging (i.e. nagging) me to get my work done.

I also need to thank my wonderful girlfriend Emily for sticking with me during these last few months. I first met Emily as this project was really getting underway. Originally, she thought this would be done by early May. Then mid-June. Finally it's August, and the thesis is actually finished, and I can spend some time with her again. She's been incredibly supportive and I couldn't have done this without her.

Well, there you have it. To paraphrase Wayne Campbell...I hope you find this thesis whimsical, yet relevant, with an underlying revisionist conceit that belies the thesis's emotional attachments to the subject matter. Party on!

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Contents

Chapter 1

Motivation: From CCD to APS

Since the launch of the ASCA mission in 1993, the detector of choice in x-ray astronomy has been the *charge-coupled device* (CCD) [1]. CCDs offer very low-noise performance and high quantum efficiency, with well-understood radiation-tolerance characteristics. CCDs are a mature technology, and they are the reason behind the great success of the Chandra X-ray Observatory, Hubble Space Telescope, and other ground- and space-based astronomical observatories.

Nevertheless, CCDs are far from ideal. The effects of radiation damage are known all too well: the CCDs aboard Chandra were damaged by radiation encountered just after launch, resulting in increased dark current and decreased spectral resolution. Other limitations inherent in the CCD architecture include long readout times, the need for thick optical blocking filters, and the inability to integrate signal processing circuitry on the same die as the CCDs [2]. A new technology, *active pixel sensors* (APS), potentially offers solutions to all of these problems.

1.1 The CCD

Invented in 1969, the CCD was originally intended as a memory element [3]. The CCD is essentially an analog shift register: charge packets are pumped across the CCD in response to changing voltages on a series of electrodes. By placing photosensitive elements throughout the device, the CCD can be used as an image sensor, its primary

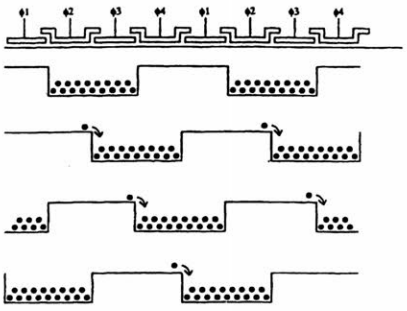


Figure 1-1: A four phase CCD. As the electrodes are pulsed in sequence, charge packets are shifted down the line (shown here in vertical succession) [4]

application today.

Modern CCDs are composed of side-by-side MOS capacitors. A four-phase CCD is shown in Figure 1-1. Each clock phase is individually pulsed, creating high- and low-potential regions in the substrate, resulting in charge being dumped from beneath one electrode to the next. Once the charges reach the end of the row, they go through another shift register, until the data from each pixel in each row has been shifted out of one output node. CCDs are operated using *correlated double sampling* to reduce noise. Scientific CCDs have low enough noise that they are capable of measuring the quantity of charge generated by an incident x-ray, with an error of only a few electrons, RMS, allowing the x-ray photon energy to be determined very precisely.

The most recent x-ray CCD mission, Astro-E2 [5, 6], uses CCDs with 1026 rows and 1024 columns, with a 24 μm pixel pitch, and four parallel output nodes. Noise is less than 2.5 electrons RMS at a readout rate of 41 kpix/sec. Both front-illuminated and back-illuminated CCDs are present on Astro-E2. The front-illuminated devices have depletion regions of 60–65 μm, as compared with 40–45 μm on the back-illuminated ones. The back-illuminated devices collect photons in the range 0.3–10 keV; front-illuminated devices have a lower limit of 0.6 keV. The CCDs have excellent spectral response, exhibiting a full-width half-maximum of approximately 130 eV for incident photons at 5.9 keV; the level of the spectral peak is 45 times its width [1, 7].

Although extremely high performance CCDs exist, the limitations of the devices

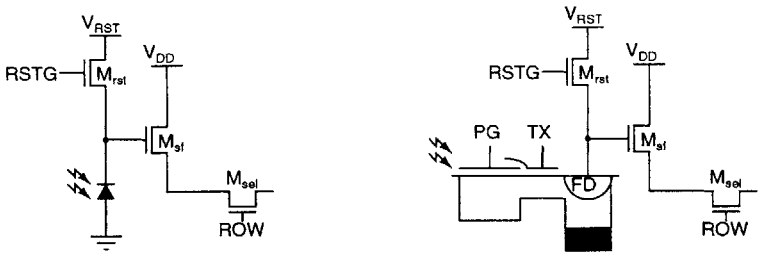
are becoming apparent. In a CCD like the one in Figure 1-1, each packet of charge must be transferred four times per pixel*; consequently, CCDs must have a very high charge transfer efficiency (CTE), the percentage of charge to be successfully transferred per phase. CTE must typically have a minimum of at least five nines (0.99999) [4]. To achieve such high CTE, the clocking voltages must be precisely controlled both in time and magnitude, with voltages on the order of 15 V typical of scientific devices [8].

Since only one pixel can be read at a given time, the time to read the whole CCD is typically several seconds. Long readout times can lead to loss of data through pileup, where two x-ray photons strike a pixel before readout can be completed. There is consequently a maximum x-ray intensity that can be observed with a CCD, with brighter sources causing frequent pileup.

X-ray CCDs are sensitive to IR, visible, and UV radiation also. Although these lower energy photons create much smaller charge packets than x-rays (typically one electron per photon [9]), accumulating charge from too many out-of-band photons in an exposure leads to loss of precision in measuring x-rays. To prevent this data corruption, large, fragile filters are used to block out-of-band radiation. The heavy shielding used to prevent contamination also reduces the amount of soft (low energy) x-rays reaching the detector. Soft x-rays are important scientifically, so it is undesirable to lose this data. If the readout speed could be increased, the required filter would be much smaller, and less likely to interfere with soft x-rays.

CCD fabrication processes are generally not capable of producing CMOS electronics, which means that all signal processing must be done off chip, on dedicated circuit boards. These boards add greatly to the power consumption and mass of space-based telescopes. An ideal detector would incorporate CMOS analog and digital processing on the same die as the detectors.

*Modern CCDs use three phases, reducing charge transfers by 25%. Charge packets may still be transferred thousands of times.



(a) Photodiode (b) Photogate

Figure 1-2: Standard three-transistor APS pixels. Pixels consist of photodetector, reset transistor, source follower, and row-select switch. After the reset transistor turns off, charge integrates on the photodetector. The source follower acts as a buffer, and the row-select switch is used to choose which pixel to read out. The photodetector may be (a) a photodiode or (b) a photogate.

1.2 The Active Pixel Sensor (APS)

One recent challenger to the CCD is the active pixel sensor (APS). The active pixel sensor is descended from the original MOS image sensors, which, like the CCD, were invented in the late 1960s [10]. The original MOS sensors were *passive pixel sensors*. Each passive pixel contained a photodiode and an access transistor. At the bottom of each column was an integrating amplifier.

Passive pixel sensors were plagued with problems, including high noise, slow readout, and lack of scalability. The solution was to add an amplifier within each pixel. This new device is the active pixel sensor. The APS pixel solves the noise, speed, and scalability issues of the passive pixel sensor [4, 10]. APS imagers still suffer from higher fixed pattern noise than CCDs, but active pixel sensors are catching up with respect to noise, dynamic range, and responsivity [10].

The standard CMOS active pixel consists of three transistors and a photodetector (Figure 1-2). The photodetector is typically a photodiode or photogate. The reset transistor, M_{rst}, pulls the detector back up to a high voltage after readout. Signal is buffered through a source follower, M_{sf}, with M_{sel} serving as a row-select switch, allowing the pixel to be multiplexed onto a column bus.

One major advantage of APS imagers are that they can be fabricated in standard CMOS processes, allowing complex signal processing to be included on the same chip

as the sensors. Single-chip cameras that incorporate sensors, processing, and A/D conversion have been produced [8].

Many other advantages exist when astronomy is considered as a primary application. Charge packets do not need to be transferred across the whole array, but rather across a single pixel. Since the integrity of the charge packet is most vulnerable to radiation during transfer [2], APS imagers are much less vulnerable to radiation. It is also possible to read out each column simultaneously, creating much shorter readout times. As described earlier, quicker readout reduces pileup and out-of-band contamination, along with other benefits such as less noise due to dark current, and possibly higher operating temperature. Due to fast readout, an APS telescope will not need a blocking filter, greatly improving its reliability and ability to detect soft x-rays. Since it is CMOS-based, an APS imager does not need tightly controlled, high voltages, like a CCD does.

Although it is very promising, APS is still an immature technology. Commercial CMOS processes do not produce active pixel sensors suitable for x-ray detection; x-ray imagers have different requirements than visible ones. Thick depletion regions are needed to efficiently absorb x-rays. Dynamic range is typically important for visible imagers, while the dynamic range of a typical x-ray sensor is on the order of 70 mV. Noise is one of the most important metrics for scientific sensors. Commercial APS devices typically have read noise on the order of 50 electrons; much lower noise is necessary for a device to have scientific value.

This thesis is the beginning of attempts to surmount the difficulties involved in creating an x-ray active pixel sensor. Chapter 2 discusses a first-generation APS imager designed and fabricated at Lincoln Laboratory. Chapter 3 presents a system I designed to test this device. Results of testing are presented in Chapter 4. Various advanced pixel designs are explored in Chapters 5 and 6. Chapter 7 discusses a second-generation APS imager designed at Lincoln Laboratory. Conclusions and recommendations for future work are presented in Chapter 8.

Chapter 2

First Generation sensor: APS-1

Lincoln Laboratory's Advanced Silicon Technology Group has designed and fabricated a first generation x-ray active pixel sensor. This device, known as APS-1, is described in this chapter.

2.1 Process Overview

APS-1 was fabricated in a 0.35 μm, 3.3V fully depleted "Imaging/Silicon-on-Insulator" (I/SOI) process [11]. The I/SOI process is optimized for low-voltage CCDs with integrated, on-chip CMOS devices. APS-1 is an experimental design to determine the quality of active pixel sensor that could be fabricated using this process.

SOI transistors are fabricated in a thin silicon layer atop a buried layer of silicon dioxide. Beneath the oxide layer is the handle wafer, a thick layer of silicon which provides mechanical support. Each device is fabricated in its own island of silicon. The resulting isolation between each transistor results in lower parasitic capacitances and higher radiation tolerance as compared to bulk CMOS [12]. In SOI, transistors of opposite polarities can be very close without risk of latchup, whereas bulk CMOS devices must be far apart. Figure 2-1 illustrates some of the advantages of SOI over bulk designs.

SOI processes are typically classified as either partially depleted (PDSOI) or fully depleted (FDSOI), depending on the thickness of the transistor layer. The more

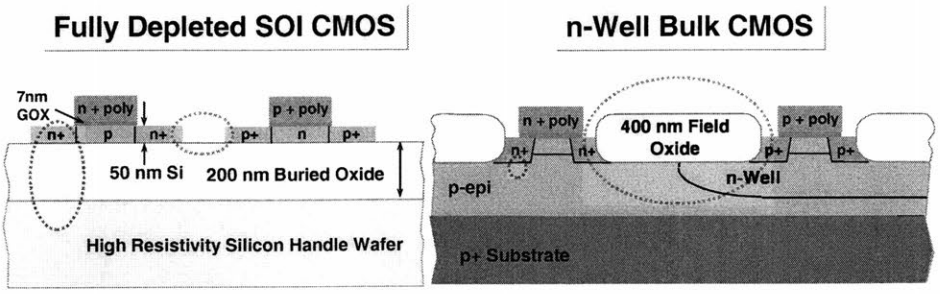


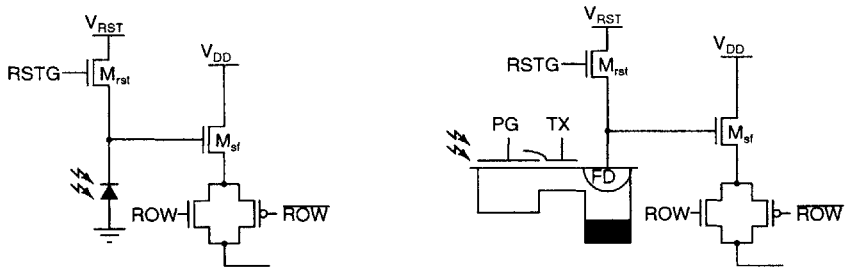
Figure 2-1: A comparison of SOI and bulk CMOS processes. The figure on the left shows two SOI transistors, the 50nm BOX region, and the handle wafer. The figure on the right shows two bulk CMOS devices. In SOI, substrate coupling is minimal due to the thick oxide, while bulk devices have a small depletion region for isolation. In SOI, transistors of different polarities be tightly packed due to the absence of field oxide and lack of wells. In bulk CMOS, n-type and p-type devices must be kept far apart to avoid latchup. Image courtesy of Lincoln Laboratory.

common variety is PDSOI; because of the thicker layer of silicon (typically greater than 0.15 μm [13]), a portion of the channel is not depleted. The result is a parasitic BJT with a floating base in parallel with the SOI MOSFET. This BJT manifests itself through the *floating-body effect*, which causes leakage currents, threshold changes, hysteresis, and other problems.

FDSOI processes offer several improvements over PDSOI. Since the entire channel (typically less than 0.10 μm thick [13]) is depleted, the floating body effect is greatly reduced. Parasitic capacitances are smaller. Second-order effects such as short-channel and narrow-channel effects decrease, subthreshold slope is improved, and transconductance is larger. However, FDSOI transistors tend to have worse threshold voltage matching due to the dependence on the channel thickness [12].

Lincoln Laboratory's I/SOI is an FDSOI process. The I/SOI process differs from ordinary FDSOI processes in that it uses the thick handle wafer as a photosensitive region. Since the photodetector is located in a different layer than the readout electronics, fill factor can be kept high despite the addition of more transistors per pixel. The buried oxide layer provides important isolation between the photodetectors and other nodes of the circuit.

Another benefit of the SOI nature of this process lies in the size of the detector



(a) Photodiode (b) Photogate

Figure 2-2: APS-1 four-transistor pixels. Pixels consist of photodetector, reset transistor, source follower, and row-select switch. After the reset transistor turns off, charge integrates on the photodetector. The source follower acts as a buffer. The complementary row-select switch is used to choose which pixel to read out. The photodetector may be (a) a photodiode or (b) a photogate.

depletion regions [2]. Photodetectors in bulk APS devices have depletion regions less than 1 μm thick. In order to efficiently detect x-rays, much larger depletion regions are needed. Modern x-ray CCDs have depletion regions on the order of 50 μm. It is possible to obtain depletion depths of this magnitude in the I/SOI photodetectors by biasing the handle wafer properly, greatly improving quantum efficiency.

2.2 Imager Design

APS-1 is a 256×256 pixel array. Pixel pitch is 12 μm. The APS-1 pixel is similar to the standard APS pixel (Figure 1-2), except that the row-select transistor is replaced by a CMOS transmission gate (see Figure 2-2). The absence of well isolation allows transistors of both polarities to fit easily within a single pixel, resulting in improved performance. In bulk APS devices, extra transistors in each pixel are avoided since they hurt fill factor. SOI devices can potentially be back-illuminated, with nearly 100% fill-factor. Although APS-1 is front-illuminated, the extra transistor was included due to the potential for back-illumination.

A simplified schematic of the imager is shown in Figure 2-3.

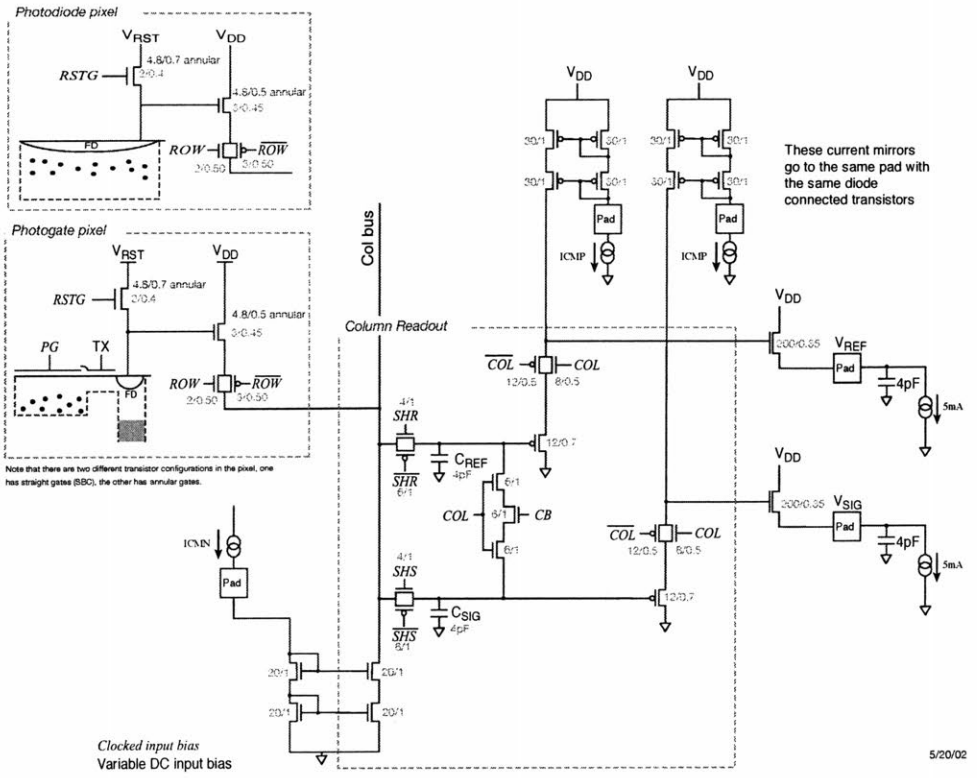


Figure 2-3: Simplified schematic of APS-1. 4-T pixels are shown in upper left. Delta-difference sampling is implemented on a column level, with parallel readout chains for signal and reference levels. Also shown are some connections to pads for external current source biasing. Image courtesy of Lincoln Laboratory.

2.2.1 Pixel variations

The imager is a 256×256 array, divided into 16 subarrays (Figure 2-4), each of which differs in doping, geometry, or photodetector type (see Table 2.1).

Photodetectors

APS-1 pixels use two different types of photodetectors. PD1–PD12 use photodiodes, while PG13–PG16 use photogates.

The simpler of the photodetectors is the photodiode (Figure 1-2(a)). Photons incident on the photodiode generate photocurrent. The reverse-biased diode acts as a capacitor, storing the generated charges. The voltage on the capacitor is the input to

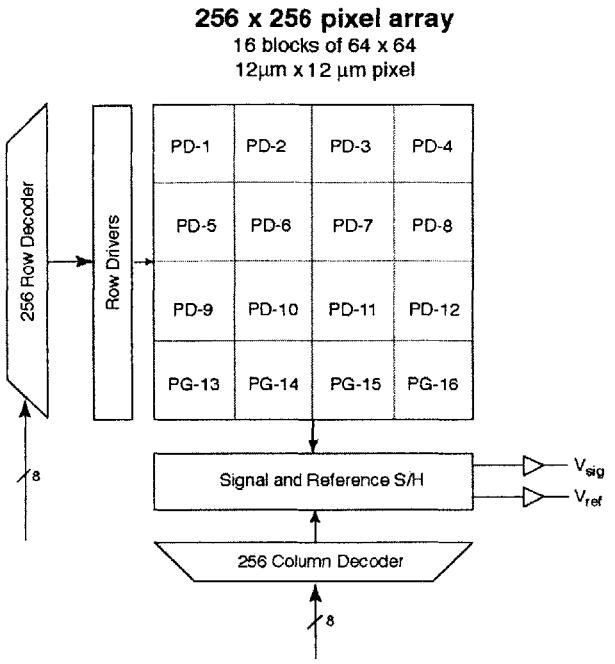


Figure 2-4: APS-1 is divided into 16 subarrays, each 64x64 pixels.

the source follower. The end result is that light on the photodiode causes the voltage at the pixel output to fall.

After a suitable exposure length, or *integration period*, the output voltage is sampled. Transistor M_{rst} is then turned on, resetting the pixel. Typically, a sample is taken immediately after reset also, for use in a double sampling scheme such as *delta-difference sampling* [14], where the two voltage levels will be subtracted later in the readout chain. Note that in this scheme the signal and reset levels are from two different exposures. They are therefore uncorrelated, and this subtraction will not eliminate reset noise. The only way to do a true correlated double sampling would be to store a whole frame of data on chip, which is impractical.

The operation of a photodiode APS pixel is shown in Figure 2-5 as three separate scope traces. In darkness, with the exception of a pulse due to the diode being reset, the waveform is nearly flat. With low light incident on the pixel, the output voltage drops over time. Bright light causes the voltage to reach a saturation point before it can be reset.

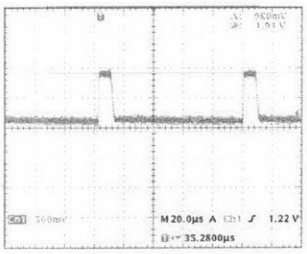
Detector	Type	BCCF Implant	SCP Implant	Bulk LOCOS	SOICS Implant	SOI-CMOS Gate Shape	TX Gate Length
PD-1	PD					Straight	
PD-2	PD	Y				Straight	
PD-3	PD		Y			Straight	
PD-4	PD			Y		Straight	
PD-5	PD				Y	Straight	
PD-6	PD	Y			Y	Straight	
PD-7	PD		Y		Y	Straight	
PD-8	PD			Y	Y	Straight	
PD-9	PD				Y	Annular	
PD-10	PD	Y			Y	Annular	
PD-11	PD		Y		Y	Annular	
PD-12	PD			Y	Y	Annular	
PG-13	PG				Y	Annular	1.0–1.3 μm
PG-14	PG				Y	Annular	0.5–1.35 μm
PG-15	PG					Annular	1.0–1.3 μm
PG-16	PG					Annular	0.5–1.35 μm

Table 2.1: Pixel variations in APS-1. Pixels differ in implant types, geometries, photodetector types, and transistor sizes.

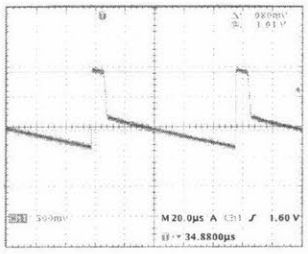
Photogates are an alternative to photodiodes. In these devices, charge integrates in a deep potential well underneath a photogate. Separating the accumulating charge from the output node is the transfer gate, typically biased near $V_{DD}/2$. While the voltage on the photogate is high, integrated charge will remain beneath the photogate. Pulsing this voltage low dumps the charge across the transfer gate, onto the floating output node, which is the input to the source follower. Each pixel is essentially a miniature CCD, with very short charge transfer distances [8].

Photogates have several advantages over photodiodes. The equivalent capacitance of a photogate can be much smaller than that of a photodiode. Reset noise, the main noise source in an active pixel sensor, is proportional to the square root of this capacitance. Consequently, photogates are typically less noisy than a photodiode, without any other changes to the readout circuitry.

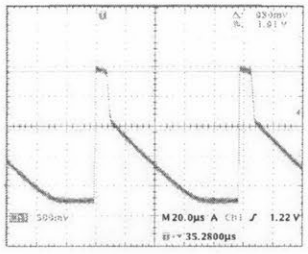
More significantly, it is possible to do true CDS with a photogate. The problem with using CDS with a photodiode is that it is necessary to store the reset level for every pixel in the array, and there is no way to include a full frame buffer and still maintain a high fill factor. The photogate, with its separate integration node and readout node, provides exactly this sort of structure. Using CDS completely



(a) Photodiode in darkness



(b) Photodiode in low light



(c) Photodiode in bright light

Figure 2-5: Oscilloscope traces of the output waveform from photodiodes. (a) Photodiode in darkness. It is periodically reset, but the waveform is otherwise nearly flat. (b) Pixel under low light. The incident photons create a current that causes the output voltage to decrease. (c) Pixel in bright light. The photodiode's output saturates.

eliminates reset noise.

The main problem with photogates is their larger size. The photogate and transfer gate are both essentially transistors, meaning that the photogate pixel has nearly twice the size of a photodiode pixel, reducing fill factor. Additionally, not all process technologies are capable of producing photogates.

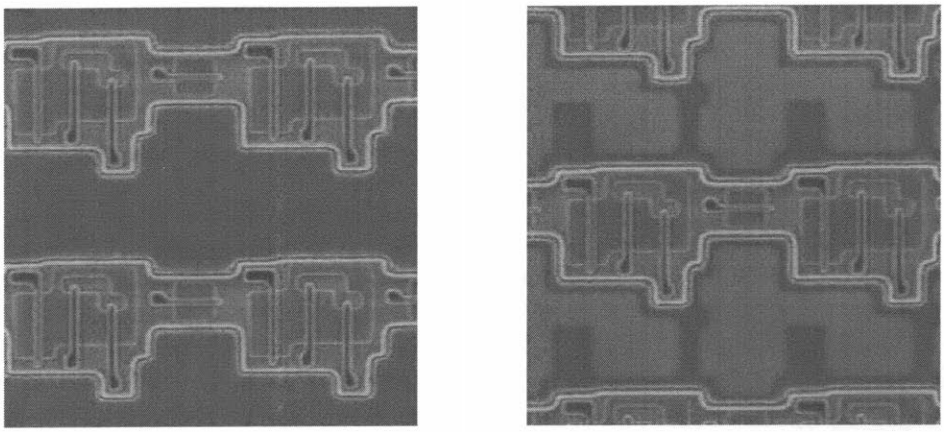
Implants and LOCOS

PD2, PD6, and PD10 pixels contain a buried channel/charge funnel (BCCF) implant in the active region of the diode in an attempt to minimize surface-state effects. BCCF is a phosphorus implant with an energy of 125 keV, a dose of 1.25×10^{12} cm^{-2}, and a tilt of 10 degrees.

PD3, PD7, and PD11 use a scupper (SCP) implant. The SCP implant is similar to the BCCF implant, but at a much higher dose: it is a phosphorus implant at an energy of 150 keV, a dose of 1.0×10^{14} cm^{-2}, and a tilt of 10 degrees.

PD4, PD8, and PD12 have extra regions of local oxidation of silicon (LOCOS). The LOCOS regions are in the bulk, above the diode region (see Figure 2-6).

All pixel types from PD5–PG14 contain an extra SOI channel stop (SOICS) implant. The SOICS implant consists of 100 keV boron, with a dose of 5.0×10^{12} cm^{-2}, at a tilt of 10 degrees. It is implanted underneath the SOI transistors to try to minimize dark current from the BOX/handle wafer interface.

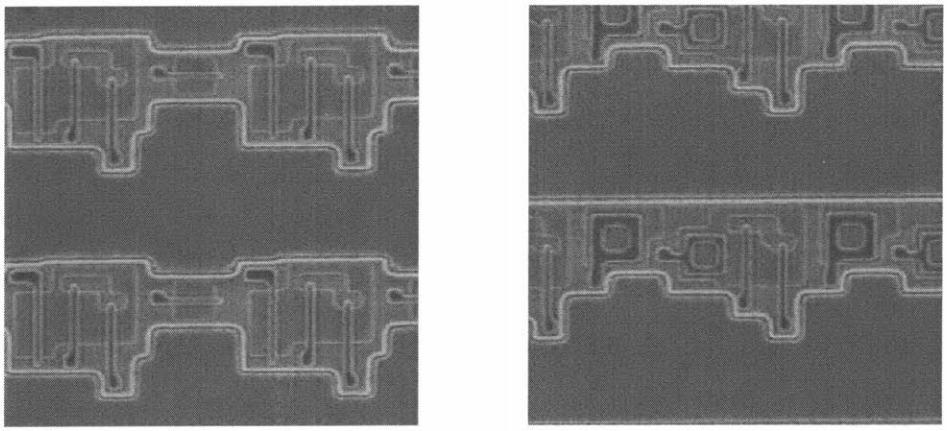


(a) Pixel without LOCOS (b) Pixel with LOCOS

Figure 2-6: (a) SEM of PD1. The gates of the four transistors are visible. (b) SEM of PD4, using LOCOS. The lighter gray regions in the bulk are the extra oxidation.

Geometry

PD1–PD8 use straight-gate transistors, while PD9–PD12 use annular-gate devices. The differences are illustrated in Figure 2-7. Conventional MOSFETs use straight gates. The gate polysilicon is a straight line dividing the diffusion region into a source and drain. The polysilicon overlaps the edges of the diffusion to ensure that the source and drain are not shorted. However, different characteristics at the diffusion sidewall cause this edge region to act as a parallel FET with a lower threshold voltage. The result is that straight-gate devices have high leakage currents. Annular gates are one attempt to solve this problem [15]. In annular-gate transistors the polysilicon gate creates a donut-shaped, or annular, division between source and drain. One terminal is entirely surrounded by poly and then by the other transistor terminal. The parasitic FET at the diffusion sidewall is now shorted out; its source and drain regions are at the same potential. Annular transistors should have much lower leakage currents than straight-gate devices. PD9–PD12 use annular transistors for the reset transistor and the source follower. Annular transistors occupy a slightly larger area than conventional ones.



(a) Pixel with straight gates

(b) Pixel with annular gates

Figure 2-7: (a) SEM of PD1. The gates of all four transistors in each pixel are straight. These transistors are prone to leakage along the edges of the diffusion. (b) SEM of PD9. The gates of the reset transistor and the source follower are annular. The region where the gate overlaps the diffusion border is shorted since both sides of the parasitic FET are at the same potential, resulting in less leakage.

2.2.2 Output Circuitry

Delta-difference sampling [14] is implemented on the column-level. This sampling strategy entails parallel chains for reading out a signal level (pre-reset) and a reference level (post-reset). The row-select switches within each pixel multiplex that row onto the column circuitry. Separate sample-and-hold switches for the signal (SHS) and reference (SHR) levels capture the appropriate voltages onto C_{SIG} and C_{REF} respectively. Each pixel in the selected row is then multiplexed onto the single set of output pads via the column select switches COL and $\overline{COL}$. Normally the two output levels would be subtracted externally.

An additional feature in the column circuitry is the crowbar switch CB. After V_{sig} and V_{ref} have been read out, it is possible (though not necessary) to pulse the crowbar high, briefly shorting the two sampling capacitors. Ideally, the resulting levels on each would be midway between the signal and reset levels. However, threshold variations and other mismatches between the two chains result in a non-zero difference voltage even after the crowbar is pulsed. The new difference voltage may be subtracted from the original difference voltage, resulting in lower fixed pattern noise.

Note that V_{sig} and V_{ref} are sampled onto two different capacitors. True CDS requires that a single sampling capacitor be used. In addition, photodiodes operate in read-then-reset mode, so the sampled reset level will actually be the reset level for the subsequent integration. Since it is impossible to store that voltage on chip throughout the integration, however, there is no way to do CDS with photodiodes.

Crowbar Analysis

It is instructive to see how the crowbar reduces fixed pattern noise. Refer to Figure 2-3 for the schematic. The signal chain contains three source followers, only one of which is guaranteed to match for the signal and reset samples (the in-pixel source follower is the same for both). Let the gains of these source followers be A_1, A_2, and A_3 for the signal path, and A_4, A_5, and A_6 for the reset path. Let the input-referred signal voltage be V_s, and the input-referred reset voltage be V_r. The output voltages are given by

$$V_{sig} = A_1 A_2 A_3 V_s \tag{2.1}$$

and

$$V_{ref} = A_4 A_5 A_6 V_r. \tag{2.2}$$

Without crowbarring, the input seen by the video electronics (assuming a differential first stage) would be the difference between these,

$$V_{in} = V_{sig} - V_{ref} = A_1 \left(A_2 A_3 V_s - A_5 A_6 V_r \right), \tag{2.3}$$

making use of the fact that $A_1 = A_4$. Crowbarring connects the inputs of the second source followers together. Charge is split between the two capacitors C_{SIG} and C_{REF}, so that the new capacitor voltages are given by

$$V_{CSIG} = V_{CREF} = \frac{A_1 \left(V_s C_{SIG} + V_r C_{REF} \right)}{C_{SIG} + C_{REF}}. \tag{2.4}$$

The output voltages produced by charge sharing are given by

$$V_{sig} = A_2 A_3 \frac{A_1 \left(V_s C_{SIG} + V_r C_{REF}\right)}{C_{SIG} + C_{REF}} \tag{2.5}$$

and

$$V_{ref} = A_5 A_6 \frac{A_1 \left(V_s C_{SIG} + V_r C_{REF}\right)}{C_{SIG} + C_{REF}}. \tag{2.6}$$

These are the crowbarred voltages, which are used as inputs to the same differential stage used for the original levels. The resultant difference signal is subtracted from the original difference signal. The input to the video electronics is therefore

$$V_{in} = A_1 \left[A_2 A_3 V_s - A_5 A_6 V_r - \left(A_2 A_3 \frac{\left(V_s C_{SIG} + V_r C_{REF}\right)}{C_{SIG} + C_{REF}} - A_5 A_6 \frac{\left(V_s C_{SIG} + V_r C_{REF}\right)}{C_{SIG} + C_{REF}} \right) \right]. \tag{2.7}$$

The goal is a signal directly proportional to $V_{sig} - V_{ref}$. To realize this goal, first make the simplifying assumption that the capacitors are not mismatched, i.e. $C_{SIG} = C_{REF}$. Equation 2.7 then simplifies to

$$V_{in} = A_1 \left(A_2 A_3 V_s - A_5 A_6 V_r - \frac{A_2 A_3 V_s}{2} - \frac{A_2 A_3 V_r}{2} + \frac{A_5 A_6 V_s}{2} + \frac{A_5 A_6 V_r}{2} \right). \tag{2.8}$$

Gathering terms with V_s and V_r gives the final result,

$$\begin{aligned} V_{in} &= A_1 \left[V_s \left(\frac{A_2 A_3}{2} + \frac{A_5 A_6}{2} \right) - V_r \left(\frac{A_5 A_6}{2} + \frac{A_2 A_3}{2} \right) \right] \\ &= A_1 \left(\frac{A_2 A_3}{2} + \frac{A_5 A_6}{2} \right) \left(V_s - V_r\right). \end{aligned} \tag{2.9}$$

As desired, the input to the video board amplifier is proportional to $V_s - V_r$, with the gain given by

$$Gain = A_1 \left(\frac{A_2 A_3}{2} + \frac{A_5 A_6}{2} \right). \tag{2.10}$$

This gain is equal to the average gains of the individual signal and reset chains. If the capacitors C_{SIG} and C_{REF} are not precisely matched, there will be some mismatch-related errors, but this is a secondary effect, as integrated capacitors can be matched quite well.

2.3 Summary

APS-1 is an active pixel sensor imager optimized for x-ray detection. As the I/SOI process is new, 16 different pixel variations were included in the array in order to determine what creates the best sensor. Extensive testing will reveal how each change influences the performance of APS-1.

Chapter 3

Test Setup

The Lincoln Laboratory-fabricated device APS-1 was tested using a modified version of the electronics from the Astro-E2 x-ray telescope. This chapter provides an overview of the Astro-E2 electronics as well as the modifications that allow these electronics to operate APS-1.

3.1 Astro-E2 XIS Overview

Much work has been done by the MIT CCD lab staff in preparation for the launch of the fifth Japanese x-ray astronomy satellite, known as Astro-E2 [6]. Astro-E2 contains, as one of its instruments, the X-ray Imaging Spectrometer (XIS) [5]. A team from MIT designed the analog electronics and CCDs for XIS. These electronics have become the standard CCD test platform in the lab, and as such it was desirable to attempt to run APS-1 using the XIS system. Adapting the XIS electronics for APS-1 necessitated substantial modifications to the electronics. The XIS system consists of three circuit boards: controller, driver, and video. The box containing these boards is connected to a Sun SPARCstation equipped with a DSP card, and an additional box (electrical ground support equipment, or EGSE) to simulate the interface with the rest of the spacecraft. Figure 3-1 is a block diagram of the XIS electronics.

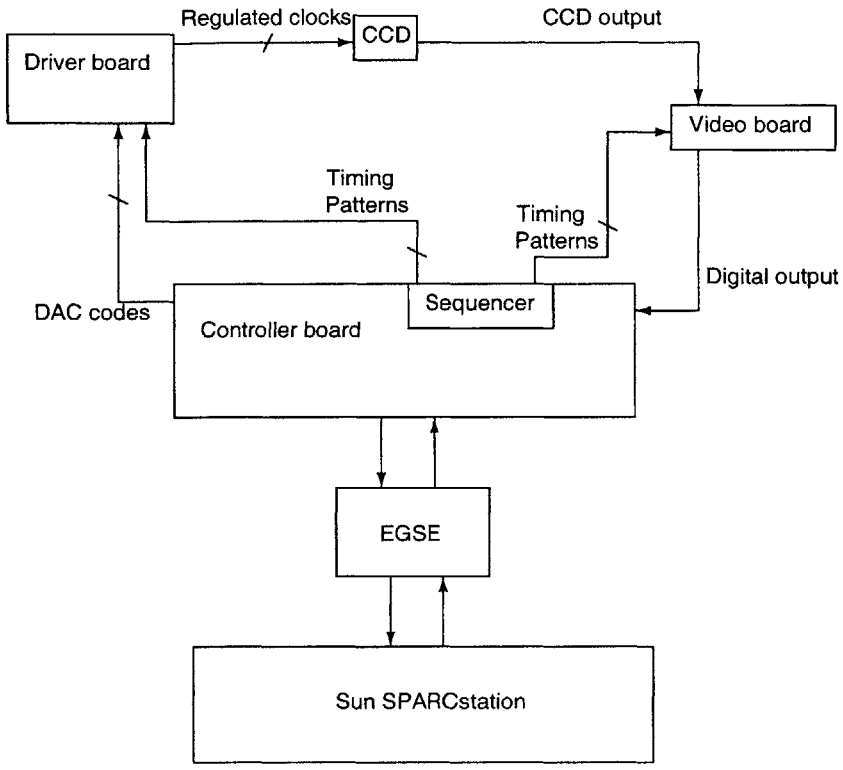


Figure 3-1: Block diagram of the XIS electronics. The controller board issues commands and timing information throughout the system. The driver board provides tightly regulated clocking and DC voltages to the CCD. The video board reads the CCD and performs A/D conversion, sending the data back to the controller and eventually back to the user.

3.1.1 Controller Board

The controller board is responsible for interfacing with the SPARCstation. Commands are received from the workstation and sent over the backplane to other boards in the system. The controller board is home to two other important systems: the housekeeping (HK) and sequencer.

Housekeeping

The HK system allows the XIS operator to monitor voltages and temperatures in the system, which would be otherwise impossible for an in-flight spacecraft. All important voltages on all the boards are multiplexed onto the HK bus on the backplane. When

the controller board receives a request for a particular measurement, the MUXes are set appropriately and the correct signal is routed to the controller, where a 16-bit A/D converter captures the value and sends it back to the Sun.

Sequencer

From the point of view of the operator, the most interesting part of the controller board is the sequencer. The sequencer is used to provide precise control over CCD timing through the use of 16 control lines, called S-lines. The sequencer is connected to two small memories, known as the PRAM and SRAM. The PRAM stores a program for the sequencer to execute. The PRAM instruction set is quite small, limited to loops, jumps, and three variations of SRAM reads. The SRAM contains the actual waveforms for the S-lines.

Each SRAM location contains 48 bits of timing for each of the 16 lines. A typical example is shown in Figure 3-2. This figure comes from an actual data file used to program the SRAM. Note that the timing patterns for each of the control lines are given by a simple binary choice, which translates to 0 or 5 volts at the output of the sequencer. The sequencer runs on a 1,966,080 Hz clock, resulting in each timing bit lasting 508 ns, or one *pixel minor cycle*. A *pixel cycle* is composed of 48 pixel minor cycles. Each SRAM location stores one pixel cycle, or 24.384 μs, worth of data.

The simple variety of sequencer read command, `SEQ`, simply reads one pixel cycle worth of data and outputs it to the S-lines, while blocking any external commands received. The second variety, `SEQE`, is identical to `SEQ` but allows processing of any external commands received. The third form, `SEQI`, allows the user to specify an additional system-level command, typically a DAC change to occur at the same time.

3.1.2 Driver Board

The main purpose of the XIS driver board is to provide precisely regulated voltages for the clock* waveforms required by the CCD. The CCD is essentially an analog

*In this context *clock* does not necessarily refer to a strict periodic square-wave clock, but rather any waveform consisting solely of high and low levels.

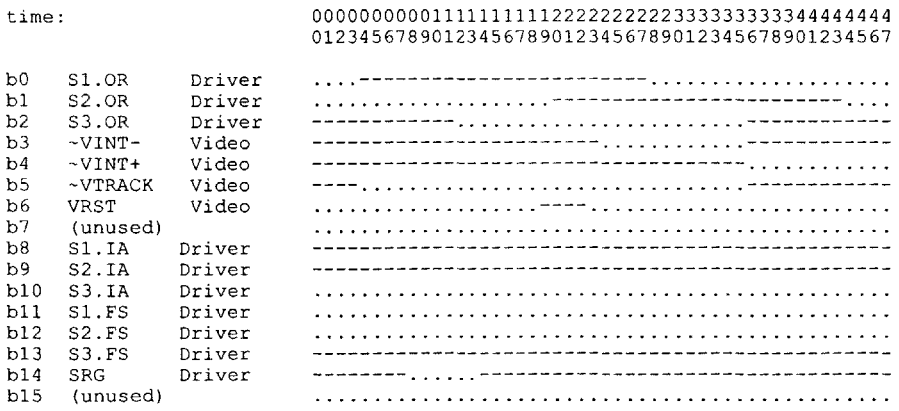


Figure 3-2: Sample SRAM input for a CCD. The timing patterns for each of the 16 S-lines are clearly illustrated using dashes and dots. Each SRAM entry contains 48 timing bits for each of the 16 lines.

shift register, and as such its performance is very dependent on having the correct voltages applied. To that end, the driver board contains 16 8-bit DACs. In some cases, two or three are actually used together to create bipolar signals. While the actual DAC outputs range from 0 to 2.5 V, amplification boosts the outputs to a typical range of approximately 0 to 13 V. The amplified, buffered DACs are known as the regulated DAC outputs, or just regulated outputs. Regulation circuitry for different DAC channels can vary widely depending on the needs of that particular signal.

The S-lines from the controller board arrive at the driver board via the backplane. On the driver board the clocks are used as the control inputs to analog switches. The switches select between different regulated voltages (determined by the DACs), sending these voltages to the CCD inputs. This arrangement of switches and DACs allows the sequencer, with its digital outputs consisting of either 0 or 5 V, to control a digital signal that may vary from -2 V to +13 V. The analog levels and timing patterns are separately programmable, allowing them to be fine-tuned independently of each other.

As a safety measure, the driver board power supply is partitioned into several local supplies, each of which has its own current limit set. If a current limit is exceeded, a switch is flipped, lowering the power supplies to a safe level. The only way to clear

current limiting is through a system reset. Limits range from 6 mA up to 97 mA.

3.1.3 Video Board

Capture, processing, and packaging of data from the CCD is done by the video board. Figure 3-3 is a block diagram of the video board analog electronics. Once per pixel cycle the video board initiates an A/D conversion. The video board contains four 16-bit A/D converters (each XIS CCD contains four output nodes). A programmable 16-bit bias may be subtracted from the data immediately after A/D conversion, and this bias may be different for different A/D channels. Bias subtraction is useful because the whole 16-bit word is not sent back to the SPARCstation. Instead, the two least significant bits are always removed, and the user then has a choice of receiving the upper 12 or lower 12 remaining bits. If a sample appears to be out of range when operating in the low-range mode, it may be possible to save the data by performing the subtraction while still in 16-bit form. The truncation from 16 bits is due to the fact that XIS is intended to be operated in space. Bandwidth and power are limited, and on the XIS the two LSBs do not provide useful data.

Since the CCD operates in a CDS mode, the video board needs to subtract two samples before A/D conversion. The subtraction is accomplished by combining current steering and an integrator. When the reset level is being read out, a current proportional to the reset level is fed into an opamp-C integrator. Next, the signal level is read out, with a current mirror being used to reverse the direction of the current into the integrator, effectively subtracting the two signals. This subtraction cancels out reset noise from the CCD, as well as helping to suppress flicker noise and thermal from the amplifiers and switches.

There is another gain stage prior to the A/D. The purpose of this gain stage is to set the digital response at 1 ADU/e^-. The ability to count photoelectrons allows the XIS to operate as a spectrometer, revealing not just the locations but also the energies of incident photons.

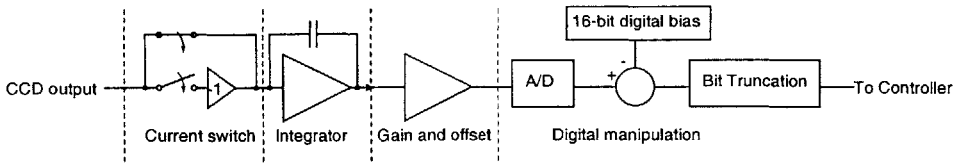


Figure 3-3: Block diagram of CCD video chain. The CCD reset level is integrated onto the capacitor. The switches flip, and the signal level is then integrated onto the capacitor with an opposite polarity, performing the required subtraction. The resulting signal is sent through a final gain stage to set the overall response at 1 ADU/e^-. After A/D conversion a programmable bias may be subtracted. Finally, four of the 16-bits are removed and the result is sent to the controller board and eventually the EGSE and the SPARCstation.

3.2 APS-1 and XIS Electronics

The reader should refer to Figure 2-3 for a schematic of APS-1.

3.2.1 APS-1 Requirements

Many CMOS-level clocks are needed for APS-1. Specifically, signals *SHS*, *SHR*, and *CB*, as well as *COL* and *ROW* are ordinary digital signals. Since APS-1 is a 256×256 pixel array, *COL* and *ROW* are actually internally generated, decoded versions of 8-bit column and row address signals. With some care *RSTG* and *PG* can be considered ordinary digital signals too. Counting all of these signals brings the total number of CMOS clocks up to 21.

Not shown in Figure 2-3 is the full number of DC voltages needed. Besides V_{DD} and V_{RST}, three other power supplies, V_{DDD}, V_{DDMAXA}, and V_{DDPG} are needed. Internal logic is powered by V_{DDD}; protection diodes and some photogate circuitry are powered by V_{DDPG}; the output transistors (shown in Figure 2-3 with drains connected to V_{DD}) are actually connected to V_{DDMAXA}. A DC bias is needed for the transfer gate *TX*. To ensure optimal performance from the photogate pixels, it is possible to change the voltage that appears on the photogate when *PG* is high by setting the proper bias voltage on the *PGBIAS* line. A voltage *SCP* is also needed to bias the scupper, a special diode that collects excess electrons from leakage currents, especially around the edge of the device.

Name	Description	Clocked/DC/Current
ROW[7 : 0]	Row address bits	Clocked
COL[7 : 0]	Column address bits	Clocked
RSTG	Pixel reset signal	Clocked
SHS	Sample/hold signal level	Clocked
SHR	Sample/hold reset level	Clocked
CB	Crowbar signal	Clocked
PG	Photogate signal	Clocked
V_{DDD}	Digital supply	DC
V_{DDPG}	Protection diodes and PG supply	DC
V_{DD}	Pixel source follower voltage rail	DC
V_{RST}	Reset voltage rail	DC
V_{DDMAXA}	Output transistor voltage rail	DC
V_{DDPG}	Protection diodes and PG supply	DC
TX	Bias on transfer gate	DC
SCP	Bias on scupper diode	DC
PGBIAS	Allows higher bias on PG	DC
I_{CMN}	Current source for column biasing	Current
I_{CMP}	Current sink for column biasing	Current
V_{SIG}	Signal output voltage	Current
V_{REF}	Reset output voltage	Current

Table 3.1: Required signals for APS-1 operation. The device requires 21 clocked CMOS level waveforms, 9 DC biases, and 4 current sources.

Besides the CMOS clocks and DC voltages, four current sources are needed. The current load on the first source follower stage is set by I_{CMN}, while the load for the second stage is set by I_{CMP}. Current loads are required at the outputs V_{SIG} and V_{REF}.

A summary of required signals in shown in Table 3.1.

3.2.2 XIS Modifications

The XIS electronics have been modified so that the regulated DAC outputs from the driver board are available on the device as DC voltages. The sequencer is used to control the digital lines. The front-end of the video board has been changed to provide current source biasing for the output transistors. XIS project engineer Dick Elder assisted in the analog design work.

Figure 3-4 is a block diagram of the modified XIS electronics.

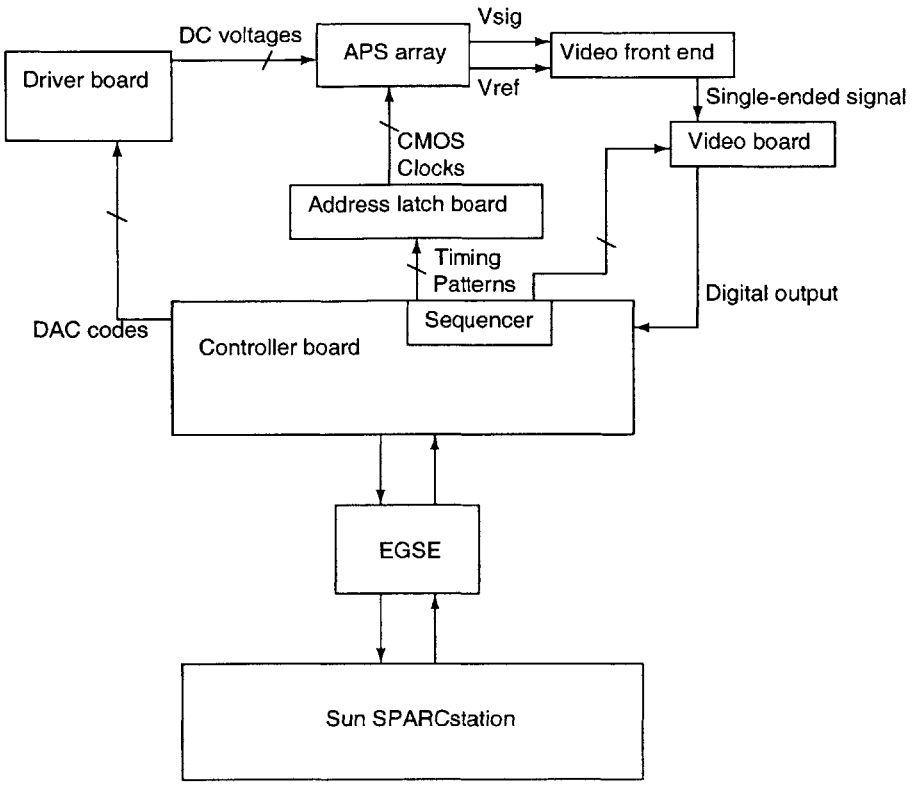


Figure 3-4: Block diagram.

Driver Board

The necessary DC voltage sources were provided by simply mapping several of the DAC channels on the driver board to the appropriate APS-1 lines. The gain applied to the raw DAC outputs was changed in order to provide an output range of 0 to 4 V for most signals.

Current source biasing for I_{CMN} and I_{CMP} was created simply using a voltage source in series with a resistor. By making the voltage on the order of ± 10 V and adding a resistor on the order of 500 kΩ in series, current sources in the range of 20 μA are realized. The double-cascode structure of the current mirrors means that the resistance looking into the mirror from the current source is negligible. The current can be fine-tuned by changing the applied voltage.

Some effort was required to modify current-limiting circuitry. Many of the original APS-1 devices tested had excessively high current consumption; this problem was

addressed by changing the allowable current drive of the regulated voltages.

Sequencer Adaptation

The sequencer contains 16 programmable digital control lines, four of which are reserved for controlling the video board, leaving 12 digital signals to control the 21 required by APS-1. In order to map 12 signals onto 21, a small add-on board, the address-latch board, was designed. The address-latch board uses a 3.3V Xilinx CPLD to create the necessary outputs. One sequencer bit, `B[0]`, was designated as the `Mode` bit. The value of this bit determines the functionality of the others. Given that readouts are usually sequential, the row and column addresses are rarely set to a new value, other than being incremented or decremented. This trend suggested an obvious division between the two modes.

In mode 0, five of the sequencer lines are used to directly control the more-freely varying clock signals *SHS*, *SHR*, *CB*, *PG*, and *RSTG*. The remaining six S-lines are used to initiate frequent row and column operations. For example, it is possible to increment the row address by setting the three bits designated for row operations to 101_b. Opcodes exist for decrementing, setting to 0x00, setting to 0xFF, and using a quick-load feature. Quick-load allows the user to save a desired address and then recall it later instantly. This feature may be used, for example, to store the initial column in a subarray readout. The column address is incremented as the row is read out, but at the end of the row the original column address may be restored via the quick-load feature to begin reading the next row.

In mode 1, eight of the remaining sequencer lines are mapped directly to `ADD[7:0]`, with the value of another bit determining whether `ADD` maps to *COL* or *ROW*. One of the remaining two bits is used as a load signal, telling the CPLD to latch the new value into its row or column address outputs. In mode 1 the other CMOS clocks (*SHS*, *SHR*, *CB*, *PG*, and *RSTG*) are all forced into the unasserted state (high for *PG*, low for the others).

Appendix C contains a complete reference for the new board. Table C.1 shows the sequencer bit reassignments more clearly. Table C.2 shows the possible operations

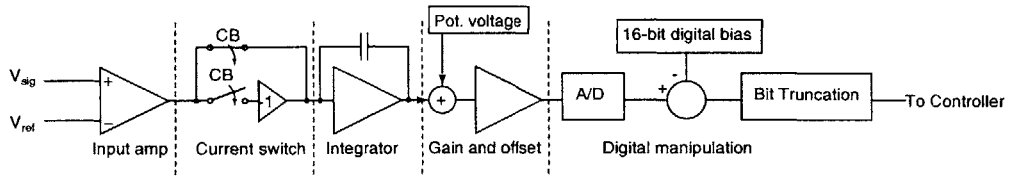


Figure 3-5: Block diagram of modified video chain. The input differential amplifier subtracts V_{ref} from V_{sig}. The difference is integrated onto the capacitor. The crowbar is asserted, and the new values of V_{ref} and V_{sig} are subtracted and then integrated with the opposite polarity because of the current switch. The resulting signal is added to an adjustable offset and sent through a final gain stage to set the overall response near 1 ADU/e^-. After A/D conversion a programmable bias may be subtracted. Finally, four of the 16-bits are removed and the result is sent to the controller board and eventually the EGSE and the SPARCstation.

performed on addresses while in mode 0.

Video Board

A block diagram illustrating the operation of the video board is shown in Figure 3-5.

In order to accommodate the two differential outputs from APS-1, and provide current source biasing for both, a new front end was added to the video chain. The new front end is shown in Figure 3-6. The current sources needed at the output transistors of APS-1 are provided in the form of Q_5 and Q_6, nominally 5 mA each. Q_1 and Q_2 are a differential pair, subtracting V_{ref} from V_{sig}. Q_7 and Q_8 are involved in biasing, and Q_3 and Q_4 simply act as a mirror, flipping the direction of the output current. The gain is set such that for a typical integration time, the video board will produce a response of 1 ADU/e^-.

Since the video board has dual-slope integration capabilities, it may seem unnecessary to perform a subtraction at the front end. However, when operating APS-1 in crowbar mode, there is a second signal to subtract, that of the crowbarred difference. Full operation of the video board involves integrating up the dual-slope integrator while reading the true outputs, then pulsing the crowbar and integrating down.

The video board is capable of subtracting a digital offset from the data after the A/D conversion, but this subtraction does not help if the signal to be sampled is out of the range of the A/D. Since the dynamic range of the A/D is quite small,

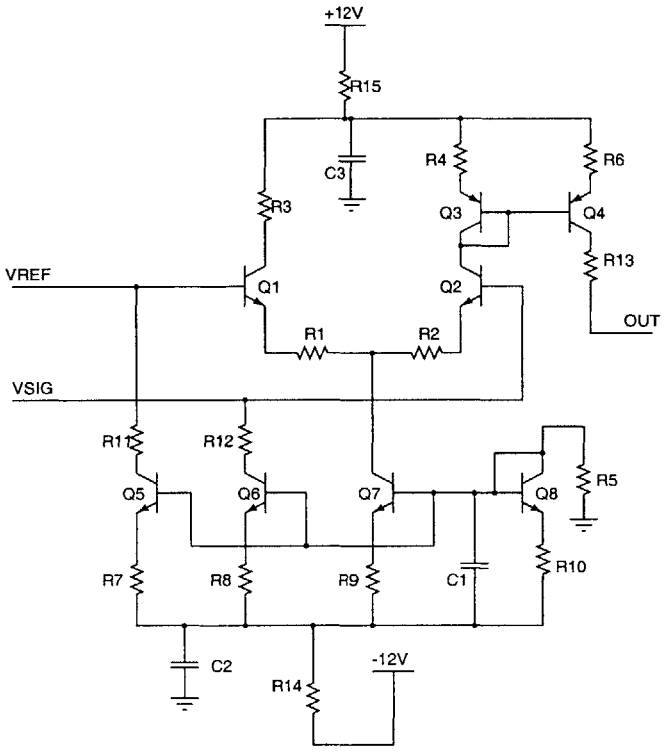


Figure 3-6: New front end for video board. Q_1 and Q_2 are a differential pair which subtract V_{ref} from V_{sig}. Q_5 and Q_6 provide the 5 mA current sources required on the output transistors of APS-1. The collector of Q_4 connects to the rest of the video board, leading into the dual-slope integrator.

approximately 82 mV, a potentiometer was added to provide an adjustable analog offset to the signal before A/D conversion. The pot allows introduction of ± 2 V of offset before the A/D converter.

The operation of the video board was verified using a dummy load consisting of 9.6 Ω resistors from V_{sig} and V_{ref} to ground. The voltage across these resistors provided an easy way to measure the current being drawn by Q_5 and Q_6. In order to simulate a signal, a 4.3 kΩ resistor was connected between the *CB* signal from the address-latch board and V_{sig}.

When *CB* is pulsed high, the voltage at V_{sig} increased by 7.36 mV. Assuming a responsivity of 5 $\mu V/e^{-}$[†], this signal represents 1473 electrons. Running the video

[†]This number was an initial estimate for the responsivity of APS-1. Testing has confirmed that responsivities are on the order of 5 $\mu V/e^{-}$ (see Chapter 4).

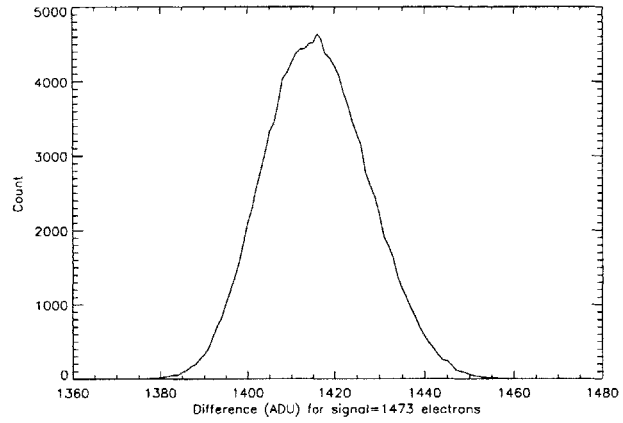


Figure 3-7: Histogram of video gain, as measured using dummy load. The mean is 1415.7 ADU, corresponding to a gain of 1 ADU = 1.04 electrons.

board with the signal present yielded a digital value of 2235.81±0.02 ADU. Without the signal present, the A/D read 820.13±0.02 ADU. The gain was measured to be 1.04 electron/ADU in high-gain mode. Similarly, in low-gain mode the response is 4.16 electron/ADU. Figure 3-7 is a histogram of the digitized difference signal.

RMS noise for an individual measurement is 7.7 electrons, which is insignificant compared to noise from APS-1.

3.2.3 Pixel Readout Sequence

All photodiode pixels were read out with the same sequence. The timing diagram is shown in Figure 3-8. Photodiodes operate in read-then-reset mode, so *SHS* is pulsed first, followed by *RSTG* and then *SHR*.

The signal and reset voltages are applied to the inputs of the differential amplifier, and the difference signal is integrated up. Finally, the crowbar switch is pulsed, shorting the two outputs. The resulting difference signal, due entirely to mismatch, is then integrated down, subtracting it from the original difference, greatly reducing mismatch-related errors.

It should be kept in mind that this sequence does not actually cancel reset noise, since the subtracted reset level is from the following integration. CDS is impossible

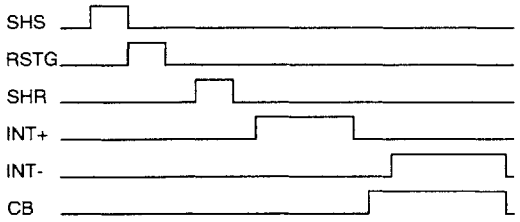


Figure 3-8: Timing diagram for APS-1 PD pixel. Pixels are always run in read-then-reset mode, and the crowbar is thrown for every pixel. Note that *SHS*, *RSTG*, and *SHR* are row-level signals, so they will only be pulsed once per row. For subsequent pixels in the row, only the crowbar needs to be repeated.

with the photodiodes unless readout is limited to a single row. The reason for including the subtraction capabilities is that photogate pixels may be operated with CDS. The photogates have not been tested yet.

3.3 Summary

The electronics from the X-ray Imaging Spectrometer was successfully modified to operate APS-1. Though the system still shows its mission-specific heritage in several ways (fixed sampling rate, data packets fixed at the size of an Astro-E2 CCD), the new electronics operate as desired. The input-referred noise level is 7.7 electrons RMS. Moreover, the system is extremely easy to learn for those familiar with the XIS.

Chapter 4

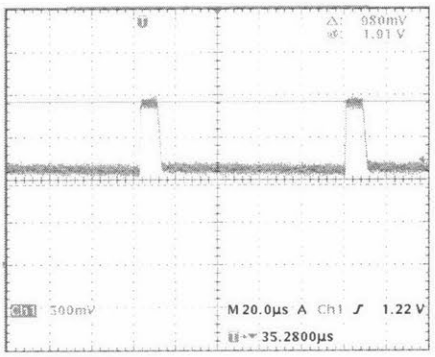
Testing Results

APS-1 was tested using the electronics described in the previous chapter. X-ray sensitivity, responsivity, dark current, and noise were measured.

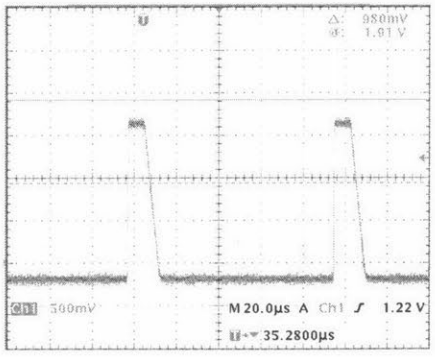
Initial testing of APS-1 at the wafer level indicated that of the twelve photodiode variations (see Table 2.1), three are non-functional. Each photodiode with the SCP implant saturates immediately (see Figure 4-1). The remaining nine photodiode pixel types were tested extensively. Photogates have not been examined yet. Results are presented below. All results are from a single packaged device, CCDCMOS31, wafer 4, row 3, column 10.

4.1 X-ray Sensitivity and Responsivity

In order to obtain accurate measurements in units of input-referred charge, it is first necessary to determine the responsivity, measured in $\mu V/e^-$, of the various APS pixels. This can be accomplished by illuminating the device using an x-ray source. X-rays emitted by ^{55}Fe create 1620 electrons in silicon [9]. Assuming all of the generated charges are captured on the photodiode capacitance, the output voltage generated by an incident x-ray can be used to calculate the responsivity. Additionally, another goal of this project, to determine the x-ray sensitivity of APS-1, is simultaneously accomplished.



(a) Dark response of a pixel from PD2.



(b) Dark response of a pixel from PD3.

Figure 4-1: (a) The response of a pixel from the PD2 subarray in the absence of light. The output level is far above saturation. (b) The response of a PD3 pixel, which contains the SCP implant. The two images are on the same scale, and it is clear that PD3 saturates immediately. The same phenomenon occurs for PD7 and PD11.

4.1.1 Experimental Setup

A copper cover with a 1 cm hole drilled into it is fitted over the packaged APS device. The x-ray source is then placed on top of the hole to illuminate the imager. The iron source used outputs 2.67×10^7 photons per second into 4π steradians. At a distance of approximately 1 cm, the source shines 3.4 photons per second on a single pixel.

As x-ray events are rare, an automatic event finder is used to analyze data. The event finder's job is to determine a background level, subtract this offset, and then look for pixels significantly above the background. The routines currently used are identical to those used for CCDs. This is not an ideal situation; the CCD event finder sums all events detected anywhere on the device, creating a single histogram. As each pixel on a CCD shares a single output amplifier, gain variations are negligible. Offset throughout the device is generally a constant as well. Each APS pixel, on the other hand, has its own amplifier with its own gain and offset. There is no single background level to subtract, and summing the responses of the various pixels would make responsivity measurements impossible. Until an event finder optimized for APS is completed, the simplest way to search for x-rays is by repeatedly reading a single pixel. Measurements take much longer, since the imaging area is only 144 square microns. Nevertheless, it is possible to measure the responses of individual pixels.

Complications

Responsivity measurements proved difficult to obtain. One complicating factor has already been mentioned: time. Collecting enough x-rays to obtain a reasonable histogram takes approximately four hours for a single pixel. Accurate characterization of a pixel type requires knowing more than just a single pixel's response.

Another complication is the copper cover. Although the hole is approximately the same size as the imager, the hole is centered relative to the package, while the imager is not. This misalignment might lead to pixels on the periphery not being illuminated well. It is somewhat difficult to determine whether the cover really is blocking x-rays or, conversely, whether pixel varieties on the edges of the device are simply not sensitive to x-rays. This problem is being addressed, but new measurements are currently unavailable.

A third problem in determining responsivity arises because all measurements were made with APS-1 operating in soft reset, with both signal and reset sampling chains active. First consider the sampling scheme. Since photodiodes operate in read-then-reset mode, the voltage seen by the video board inputs (assuming a crowbarred differential voltage of zero) at time n is

$$\texttt{video}[n] = \texttt{signal}[n] - \texttt{reset}[n+1]. \tag{4.1}$$

By itself, delta-difference sampling would not cause any problems in measuring the signal created by an x-ray. However, because of soft reset, the reset level following a large signal is higher than it would be otherwise. Some of the generated signal that is present in $\texttt{signal}[n]$ is also present in $\texttt{reset}[n+1]$ and therefore subtracted, leading to an underestimation of responsivity.

As an example, consider a case where signal and reset levels are both 0 units in the absence of x-rays, and in a given reset period three quarters of the photoelectrons can be reset. If an x-ray causes the signal level to increase by 1620 units, the following reset level will be 405 units, and the subtracted level will be 1215 units. The responsivity is measured as 1215 units per x-ray, instead of the true value of 1620.

It is possible to get a better idea of responsivity in the presence of soft reset by adding data from several consecutive reads. To see this, continue the previous example. With 405 units still left on the photodiode, the subsequent readout will have 405 units on the signal line and 101.25 on the reset line, for a difference of 303.75. Adding the two differences together gives 1518.75. The pattern here is the familiar geometric series. That the sum of a geometric series has a closed form solution suggests another approach. Two pixels allows determination of the fraction of charge that is lost during each reset. Only two points are then needed to determine the actual responsivity.

The CCD event finder, however, does not presently include the capability to correct event amplitudes automatically for the effects of soft reset. It is capable of adding the signals from two consecutive readouts (in a CCD, these are *split events*, where the charges generated by an x-ray are split between two neighboring pixels), but not more than two. Manual examination of a single event can yield an approximate soft reset correction factor through the method just described.

4.1.2 Results

Examining the measured results for two nearby pixels illustrates the problems with x-ray detection. Pixels r12c12 and r13c13 from within the PD6 (straight-gate, BCCF implant, SOICS implant) subarray were exposed to x-rays. While the first pixel performed extremely well, the second pixel failed to detect x-rays, despite being diagonally adjacent to the first.

PD6 r12c12

The x-ray response of pixel r12c12 is shown in Figure 4-2. The data pictured represents the sum of two consecutive reads. This data provides a lower bound for the responsivity of the pixel at 2.85 $\mu V/e^-$.

Manually examining a single event gives a better approximation. For one event (chosen by opening a randomly selected data file and manually scanning for an event),

the peak value was 404 ADU, with the next read at 334 ADU. Subtracting the mean background of 234 ADU yields 170 ADU for the peak and 100 ADU for the second read. The geometric series method implies a total signal amplitude of 413 ADU. Assuming 413 ADU corresponds to 1620 electrons, the responsivity, as measured by this single event, is 5.1 $\mu V/e^-$. The event finder, however, only adds the first two terms, classifying this event at 270 ADU, corresponding to a responsivity of 3.4 $\mu V/e^-$. Assuming proportionality between these two methods, i.e.

$$\frac{\text{Event finder value of event A}}{\text{Geometric mean value of event A}} = \frac{\text{Event finder value of event B}}{\text{Geometric mean value of event B}}, \tag{4.2}$$

this data implies the peak of the distribution, at 2.85 $\mu V/e^-$, actually represents a responsivity of 4.3 $\mu V/e^-$ for pixel r12c12.

In 740 frames (5920 seconds) of data, 1751 events were detected, for a rate of 0.296 counts per second. The quantum efficiency is therefore 0.087.

An important number obtained from the data plotted in Figure 4-2 is the full width at half-maximum (FWHM) of the x-ray histogram. FWHM is a measure of spectral resolution, one of the most important qualities in a scientific x-ray detector. This pixel shows an FWHM of 1.5 keV when illuminated by 5.9 keV x-rays (assuming a responsivity of 2.85 $\mu V/e^-$). In contrast, CCDs exhibit FWHM on the order of 130 eV for the same x-ray source. The spectral resolution of APS-1 is approximately ten times worse than the best CCDs today.

PD6 r13c13

The x-ray response of r13c13 is shown in Figure 4-3. The data pictured represents the sum of two consecutive reads. This data provides a lower bound for the responsivity of the pixel at 1.71 $\mu V/e^-$. Using the same method as used for PD6 r12c12, a single event was examined manually. This event had an actual magnitude of 321 ADU (implying responsivity of 3.96 $\mu V/e^-$), which the event finder classified as 159 ADU. Assuming Equation 4.2 is valid, the peak responsivity can be estimated as 3.46 $\mu V/e^-$.

In 730 (5840 seconds) frames of data, 1114 events were detected, for a rate of 0.19

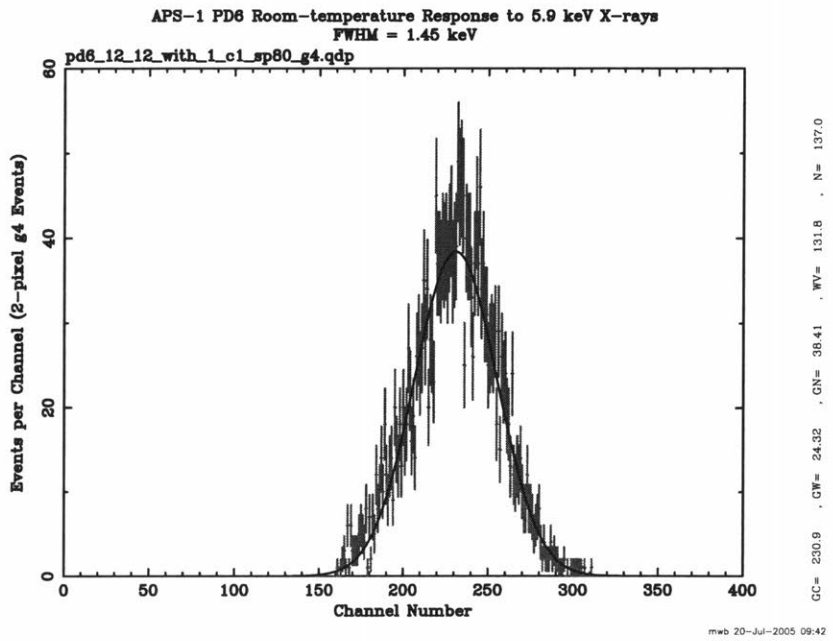


Figure 4-2: Histogram showing x-ray response of pixel r12c12 in PD6. The x-axis represents the amplitude of each event (in ADU) above the background level. 1 ADU represents 20 μV. To compensate for soft reset, each point in this plot is the sum of two successive reads. A gaussian curve is fit to the histogram. The peak of the gaussian is at 230.9 ADU, indicating a responsivity of 2.85 $\mu V/e^-$. Fully accounting for soft reset yields a responsivity of approximately 4.3 $\mu V/e^-$. The full-width half-maximum of the curve is 1.5 keV, about ten times wider than for a CCD. Noise during the readout was 9.8 ADU; since pixels are summed for his histogram, noise should be higher, but by less than a factor of $\sqrt{2}$, since the noises of two consecutive readouts are correlated. The standard deviation of the gaussian is 24.3 ADU, indicating the presence of another noise source.

counts per second. The quantum efficiency is therefore 0.056.

This pixel has a FWHM of 1.8 keV when illuminated by 5.9 keV x-rays (assuming a responsivity of 1.71 $\mu V/e^-$).

PD2 r12c12

The only other pixel for which a solid x-ray response curve was obtained is r12c12 from PD2 (straight gate, BCCF implant), shown in Figure 4-4. The data pictured represents the sum of two consecutive reads. This data provides a lower bound for

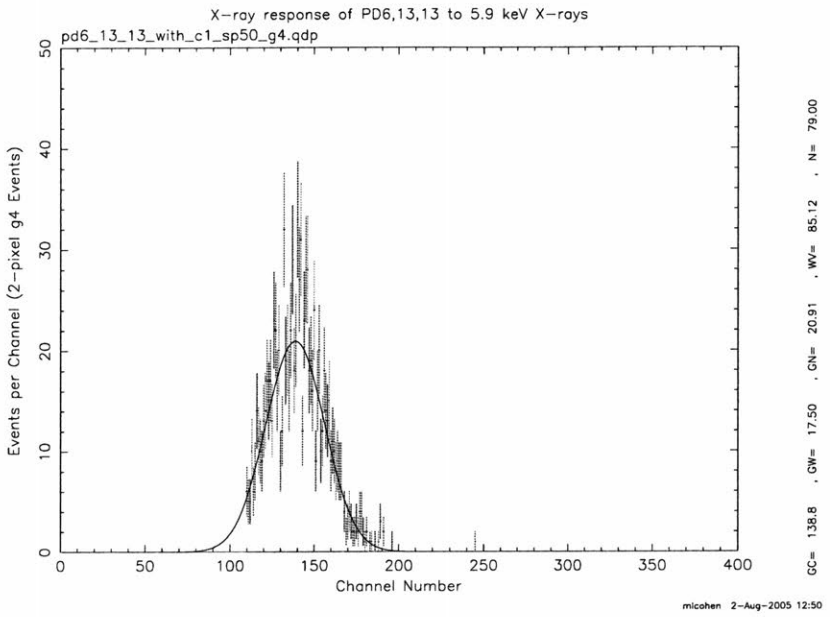


Figure 4-3: Histogram showing x-ray response of pixel r13c13 in PD6. The x-axis represents ADU count above the background level. 1 ADU represents 20 μV. To compensate for soft reset, each point in this plot is the sum of two successive reads. A gaussian curve is fit to the histogram. The peak of the gaussian is at 138.8 ADU, indicating a responsivity of 1.71 $\mu V/e^-$. The full-width half-maximum of the curve is 1.8 keV.

the responsivity of the pixel at 2.49 $\mu V/e^-$. Using the same method as used for PD6 r12c12, a single event was examined manually. This event had an actual magnitude of 183 ADU (implying responsivity of 2.26 $\mu V/e^-$), which the event finder classified as 159 ADU. Assuming Equation 4.2 is valid, the peak responsivity can be estimated as 2.87 $\mu V/e^-$.

In 454 frames (3632 seconds) of data, 293 events were detected, for a rate of 0.08 counts per seconds. The quantum efficiency is therefore 0.024.

This pixel has a FWHM of 1.0 keV when illuminated by 5.9 keV x-rays (assuming a responsivity of 2.49 $\mu V/e^-$).

4.1.3 Conclusions

Results for the three pixels described above are summarized in Table 4.1.

Determining the responsivity of APS-1 has proved difficult with the available

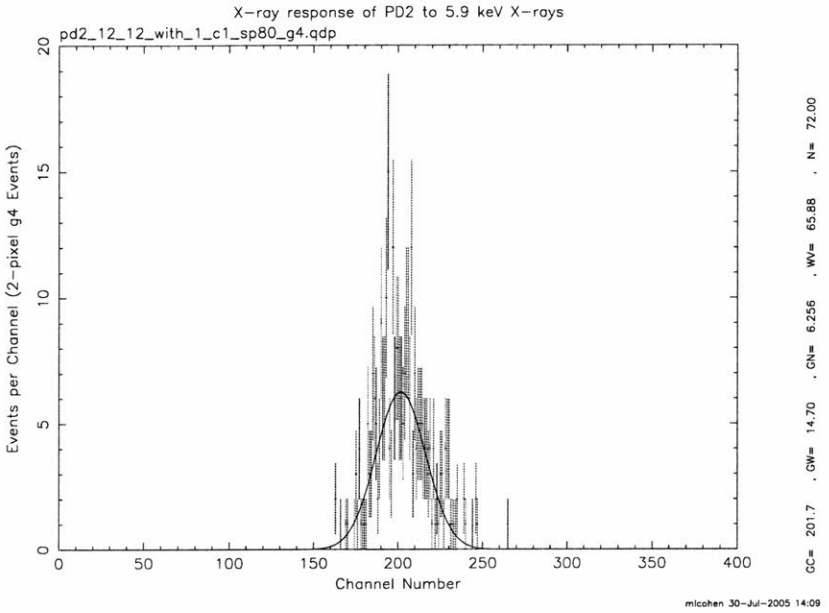


Figure 4-4: Histogram showing x-ray response of pixel r12c12 in PD2. The x-axis represents ADU count above the background level. 1 ADU represents 20 μV. To compensate for soft reset, each point in this plot is the sum of two successive reads. A gaussian curve is fit to the histogram. The peak of the gaussian is at 201.7 ADU, indicating a responsivity of 2.49 $\mu V/e^-$. The full-width half-maximum of the curve is 1.0 keV.

equipment. As the available estimates of responsivity vary from 4.3 to 5.1 $\mu V/e^-$ for a single pixel, with a much wider range when two pixels are considered, a constant responsivity of 5 $\mu V/e^-$ will be assumed for simplicity in the rest of this chapter. The main problem caused by this assumption is not the chosen numerical value (if a different estimate is desired, numbers will scale accordingly). Rather, the assumption that responsivity is constant across all pixels, of all types, is likely a major source of error. Until a brighter X-ray source, which fully illuminates the array, is available, it will not be possible to obtain a full responsivity map for APS-1.

Pixel	Fitted Peak Responsivity ($\mu V/e^-$)	Fitted FWHM (keV)	Extrapolated Peak Responsivity ($\mu V/e^-$)	Quantum Efficiency
PD2r12c12	2.49	1.0	2.87	0.024
PD6r12c12	2.85	1.5	4.3	0.087
PD6r13c13	1.71	1.8	3.46	0.056

Table 4.1: Summary of responsivity measurements. Only three pixels were examined. Note the large spread between two pixels of the same type, implying that a large number should be sampled to accurately characterize a pixel type. For each pixel, a different soft reset correction factor was used. This factor accounts for PD2r12c12 having the lowest extrapolated peak while PD6r13c13 has the lowest fitted peak.

4.2 Dark Current

Dark current is current that flows in a photodetector in the absence of light. Dark current contributes shot noise and nonuniformity to all data. Therefore, it is important to reduce dark current to as small a level as possible. Dark current is highly temperature dependent. A CCD is normally operated cold enough to reduce dark current to less than one electron per pixel per exposure. An imager with low dark current could be operated at higher temperatures, a significant advantage.

4.2.1 Experimental Setup

Dark current measurements were taken on a large number of pixels of each variety. Typically, a 16×16 subarray of pixels was examined, though the exact size used depended on the magnitude of the dark current. By varying the integration time and observing the change in detected signal with time, the average slope of the pixel dark response is obtained. This slope is entirely due to dark current, which can be determined if the responsivity is known. As previously stated, a constant responsivity of 5 $\mu V/e^-$ was assumed. To test temperature variation, the imager was cooled, first to 0 °C and then to −40 °C.

Wafer-level tests suggest that pixels with annular gates (PD9, PD10, PD12) should have significantly lower dark currents than straight-gate devices. The rest of the varieties are unknowns. The various implants were intended to reduce dark current, but success can only be determined by measurement.

The primary complication in obtaining useful dark current data is the wide spread

in DC offset from pixel to pixel compared to the narrow capture range of the A/D converter. The A/D converter has a capture range of approximately 82 mV. During long integration periods, variations in dark current and in offset often combine to push a fraction of the pixels out of range of the A/D. Using the programmable A/D offset capability of the readout electronics, it is possible to change which pixels are captured. Attempts have been made to lose an equal number of pixels on the high and low end of the A/D. There is no guarantee, however, that the resulting data fairly represents the pixel population.

Since dark current magnitudes differ greatly between pixel types, different integration times were used to measure dark current. Pixels with lower dark current require longer integration times to detect a significant change. Since the sampling rate is fixed, larger subarrays were typically read when measuring small dark currents. Mean dark currents greater than 100 nA/cm^2 were measured using integration times of 25, 50, 75, and 100 μs (*short* integration times). Smaller values of dark current were measured with integration times of 6.4, 12.8, 1.92, and 25.6 ms (*moderate* integration times). In both cases, 256 pixels were examined. For pixels with extremely small dark current, 1024 pixels were examined, using integration times of 25, 50, 75, and 100 ms (*long* integration times). Since each of these methods has a different ability to resolve dark current, it is difficult to directly compare data taken by different methods. It is generally possible, however, to say that measurements taken with longer integration times are lower in dark current than those taken with shorter integration times.

4.2.2 Results

Measured values of dark current at 25 °C, 0 °C, and −40 °C are shown in Table 4.2.

Room Temperature

Short integration times were used for PD1, PD2, PD5, PD6, and PD10. Moderate integration times were used for PD4 and PD8, with long integration times used for PD9 and PD12. The data on PD9 is not from a full sample of the population;

approximately 80% of the pixels fell outside the A/D capture range. The sampled pixels might not be representative of the true population. Table 4.2 also includes data on a gaussian fit for each pixel type. These numbers are especially useful for PD1, PD2, PD6, and PD10, where the centroid of the gaussian provides an idea of a typical dark current level.

Figures 4-5 through 4-13 are scatter plots of the dark currents for each pixel type. PD1, PD2, PD5, and PD6 are clearly heavily skewed; it is for their benefit that the gaussian fits were done. PD5 is so heavily skewed that the fit gives a negative mean even though each pixel has a mean greater than zero. For PD5, the fit is not very enlightening.

PD2 shows evidence of fixed-pattern noise; some rows (16 adjacent pixels in the scatter plot) have low dark current while others have higher dark current. PD4, PD8, and PD12 all show very less skewed distributions. The fit numbers more closely agree with the raw data.

Annular-gate pixels (PD9, PD10, PD12) seem to show lower dark current that straight-gate pixels. PD10 seems to have more dark current than some of the straight-gate designs (PD4, PD8). However, these cannot be compared directly, as different integration times were used. PD10 has less dark current than the designs to which it can be directly compared (PD1, PD2, PD5, PD6). To better compare PD10, low-temperature data should be used.

The pixels with LOCOS (PD4, PD8, PD12) seem to have less dark current than similar designs that don't have LOCOS regions. The smaller measurements may actually be due to lower responsivity rather than lower dark current.

Low temperature

Cooling APS-1 clearly reduces dark current. Gaussian fits start to become less useful, as cooling tends to have more of an effect on high-dark current pixels, effectively clustering data points together (scatter plots at -40 °C are shown in Figures 4-14, 4-15, and 4-16). For shorter integration times, dark current measurements begin to be inflated, as there is a minimum dark current that can be measured with a given

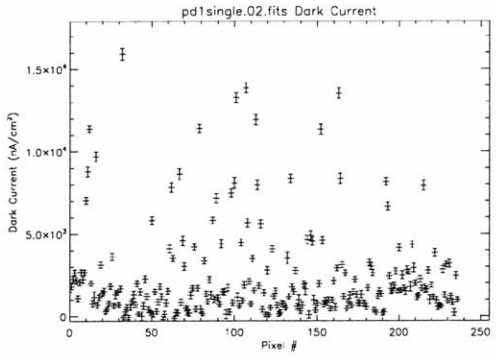


Figure 4-5: Dark current (nA/cm^2) variations at 25 °C in PD1 (straight-gate) pixels.

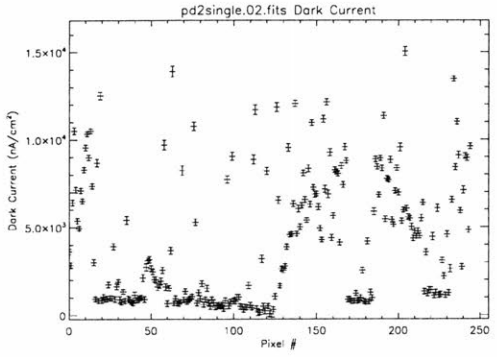


Figure 4-6: Dark current (nA/cm^2) variations at 25 °C in PD2 (BCCF implant, straight-gate) pixels.

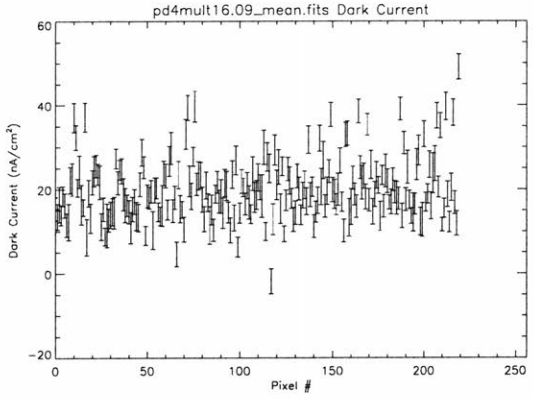


Figure 4-7: Dark current (nA/cm^2) variations at 25 °C in PD4 (LOCOS, straight-gate) pixels.

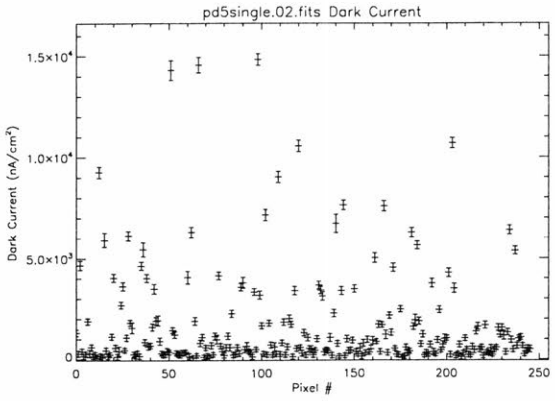


Figure 4-8: Dark current (nA/cm^2) variations at 25 °C in PD5 (SOICS implant, straight-gate) pixels.

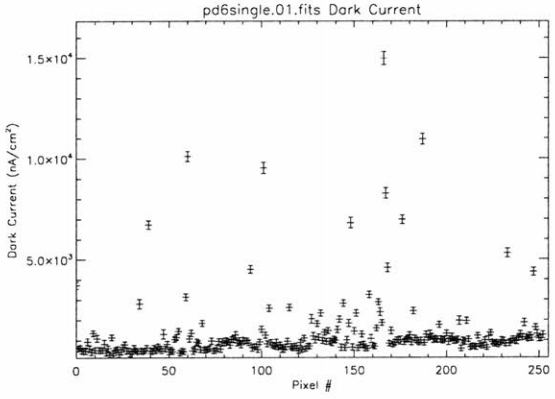


Figure 4-9: Dark current (nA/cm^2) variations at 25 °C in PD6 (SOICS, BCCF implants, straight-gate) pixels.

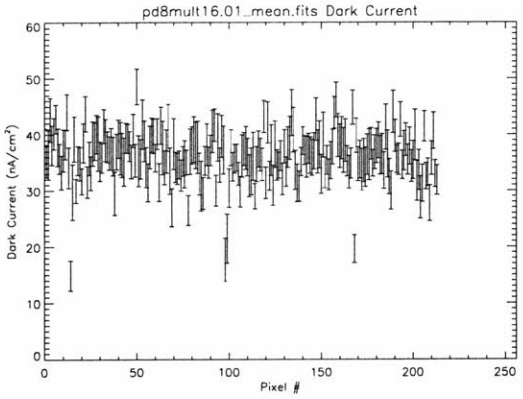


Figure 4-10: Dark current (nA/cm^2) variations at 25 °C in PD8 (SOICS implant, LOCOS, straight-gate) pixels.

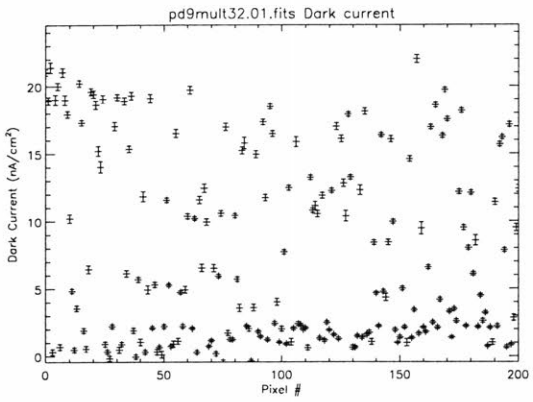


Figure 4-11: Dark current (nA/cm^2) variations at 25 °C in PD9 (SOICS implant, annular-gate) pixels.

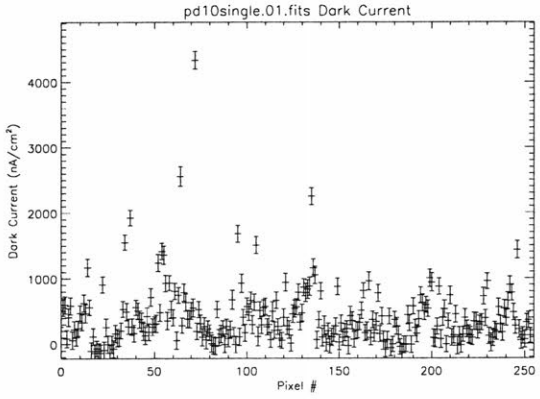


Figure 4-12: Dark current (nA/cm^2) variations at 25 °C in PD10 (SOICS, BCCF implants, annular-gate) pixels.

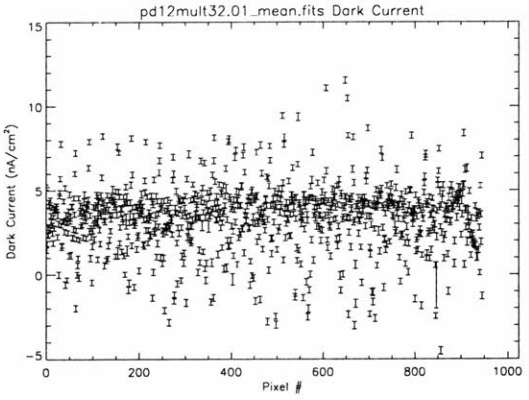


Figure 4-13: Dark current (nA/cm^2) variations at 25 °C in PD12 (SOICS implant, LOCOS, annular-gate) pixels.

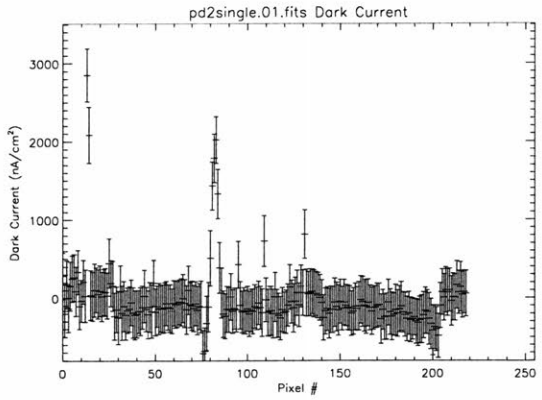


Figure 4-14: Dark current variations at −40 °C in PD2 (BCCF implant, straight-gate) pixels.

integration time.

At 0 °C, dark current in PD4 and PD8 is reduced enough to allow long integration times to be used. PD9 is still underrepresented. At 0 °C, PD10 is calculated using only two points per line instead of four, and the data is still underrepresented. At −40 °C, PD10 has switched to long integration times and PD5 and PD6 have switched to moderate integration times. All pixel types appear to be well-sampled at −40 °C.

Examining the trends in dark current as temperature changes, every pixel type except for PD9 decreases monotonically as temperature decreases. The errors in PD9 are most likely due to partial sampling. At 0 °C, 35% fewer pixels were included than at room temperature, and the mean increased by 45%. Given a wide spread in dark currents, it is certainly possible that this change is due to sampling differences, rather than an increase in dark current with temperature.

Conclusions

Due to the large variances and skewed distributions, it is difficult to accurately compare two varieties of pixels in terms of dark current. Clearly, annular-gate devices have less dark current than straight-gate devices. LOCOS provides a similar benefit. It is possible that with a responsivity map of the array, some of the large variations might disappear. What appears to be high dark current might simply be a pixel with

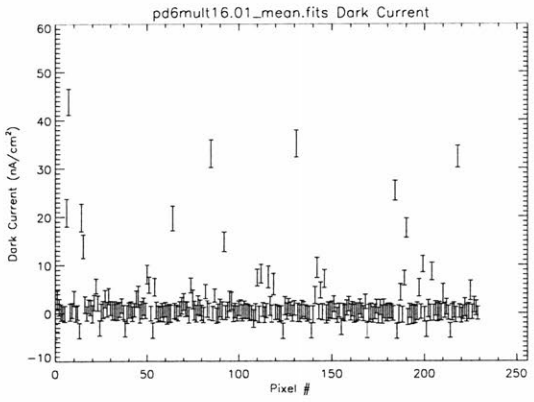


Figure 4-15: Dark current variations at −40 °C in PD6 (SOICS, BCCF implant, straight-gate) pixels.

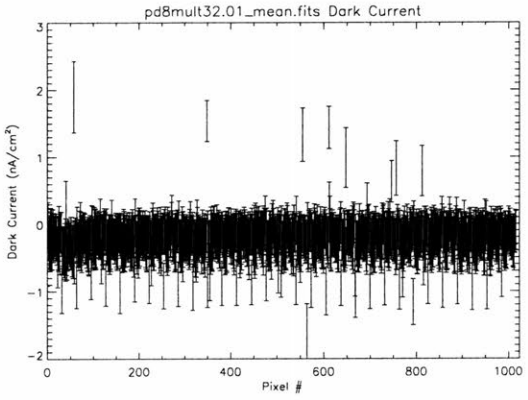
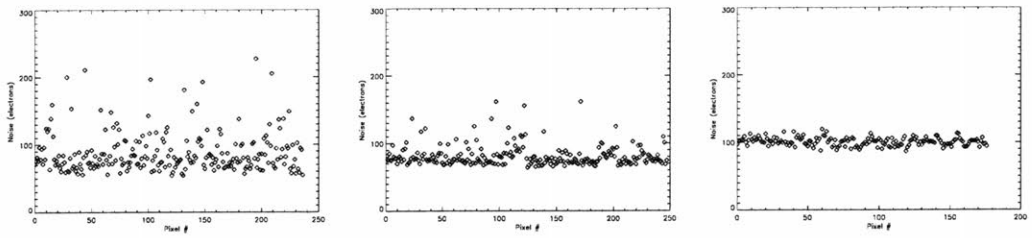


Figure 4-16: Dark current variations at −40 °C in PD8 (LOCOS, straight-gate) pixels.

higher responsivity. Similarly, LOCOS might hurt responsivity, rather than reduce dark current. More thorough responsivity measurements should give some answers.

4.3 Noise

Based on the approximate value of 5 $\mu V/e^-$, it is possible to predict an RMS noise level using the kTC approximation. Assuming a source follower gain of unity, this responsivity corresponds to an input capacitance of 32 fF. If noise from soft reset dominates, the RMS noise of a typical APS-1 pixel is approximately 51 electrons. System noise is 7.7 electrons, an insignificant level compared to reset noise.



(a) 25 °C (b) 0 °C (c) −40 °C

Figure 4-17: Noise in PD1 pixels as temperature varies. Cooling the device tends to lower the noise in the pixels with high dark current, but noise in the typical pixel stays about the same. For unknown reasons, the mean noise actually increases slightly at −40 °C.

4.3.1 Experimental Setup

The data collected for dark current analysis was also used for noise analysis. That is, integration times were varied, with many points being taken at each integration time. Instead of fitting a line to the data, as done for dark current analysis, a line was fit to the variances of each point, and this line was extrapolated to zero signal. This extrapolated variance is the square of the read noise.

Unfortunately, the variances of many of the pixels are not linear with time. Longer integration times led to higher noise measurements, and short integration times often extrapolated to negative variances. A better procedure would be to sample each pixel repeatedly with the shortest possible integration time, and use the obtained noise as an upper bound. Without collecting new data, this procedure was possible for pixels sampled with short integration times, i.e. PD1 and PD2 for all temperatures, PD5 and PD6 at room temperature and 0 °C, and PD10 at room temperature.. These results are presented below.

4.3.2 Results

Figure 4-17 shows scatter plots of the reset noise from 256 PD1 pixels. Cooling tends to decrease noise in pixels with very high dark current. However, pixels with low dark current tend to have slightly higher noise at low temperatures. Similar trends exist in all pixels for which measurements were available.

The mean and standard deviation of all available noises are summarized in Table 4.3. Note that PD10 shows much less spread than other pixel types. This fact suggests gate leakage as an important source of noise. The annular transistors in PD10 should have lower noise, and this appears to be the case.

Read noise is higher than expected with a 32 fF photodiode capacitance. Most likely, this error is due to the assumption of constant responsivity of 5 $\mu V/e^-$ (equivalent to a constant 32 fF capacitance) is wrong.

4.4 Summary

Testing APS-1 has proved difficult. Ideas for implementing better testing procedures have been suggested. Specifically, a responsivity map of the device is necessary. Improvements in capturing data are needed as well. Despite these complications, x-rays have been observed, and differences among pixel types have been explored. One metric that stands out is noise, which in a CCD is as low as 2.5 electrons due to correlated double sampling. Noise reduction mechanisms will be needed to create a useful scientific APS sensor.

25 °C						
Pixel Type	Raw Data			Gaussian Fit		
	n_{pix}	μ_{raw}	σ_{raw}	n_{pix}	μ_{gauss}	σ_{gauss}
PD1	237/256	2342±13	2790	201/237	580±190	1280±160
PD2	245/256	4087±10.	3580	130/245	561±39	390±32
PD4	220/256	20.02±0.21	7.40	219/220	13.14±0.41	5.65±0.36
PD5	246/256	1592±11	2400	230/246	−6400±1400	2270±240
PD6	253/256	1301.5±9.4	1680	241/253	390±110	549±69
PD8	214/256	36.05±0.23	4.39	214/214	31.54±0.32	4.53±0.28
PD9	201/1024	7.576±0.014	6.86	109/201	1.11±0.15	1.25±0.15
PD10	254/256	400.6±8.0	463	249/254	36±63	410±40.
PD12	946/1024	3.4156±0.0059	1.96	946/1024	2.169±0.068	2.034±0.050

0 °C						
Pixel Type	Raw Data			Gaussian Fit		
	n_{pix}	μ_{raw}	σ_{raw}	n_{pix}	μ_{gauss}	σ_{gauss}
PD1	248/256	602±11	1530	233/248	−360.±52	723±47
PD2	251/256	516±12	1180	233/251	−198±28	374±24
PD4	963/1024	3.369±0.023	1.64	963/963	1.453±0.048	1.224±0.041
PD5	249/256	571±10	1140	242/249	−2570±210	1007±55
PD6	254/256	556±12	854	254/254	1115±	1121±
PD8	991/1024	2.360±0.027	1.70	977/991	0.780±0.056	1.548±0.030
PD9	131/1024	11.066±0.054	5.39	131/131	10.5±1.2	8.2±1.7
PD10	94/256	157.84±0.93	23.4	94/94	153.7±3.3	26.1±3.3
PD12	911/1024	0.531±0.012	1.00	879/911	−0.144±0.022	0.644±0.017

−40 °C						
Pixel Type	Raw Data			Gaussian Fit		
	n_{pix}	μ_{raw}	σ_{raw}	n_{pix}	μ_{gauss}	σ_{gauss}
PD1	177/256	−185±15	319	176/177	−2280±400	609±68
PD2	219/256	−26±20	383	218/219	−870±240	590±110
PD4	1018/1024	0.113±0.010	0.42	963/963	−0.374±0.016	0.3639±0.0069
PD5	226/256	4.823±0.096	10.5	212/226	−24.2±3.0	11.3±0.79
PD6	230/256	2.02±0.11	5.98	226/230	−34.2±6.1	10.5±1.0
PD8	1017/1024	−0.223±0.011	0.208	1017/1017	−0.660±0.023	0.3733±0.0095
PD9	880/1024	1.8671±0.0080	3.20	757/880	−0.0627±0.027	0.618±0.016
PD10	1004/1024	2.224±0.010	2.43	931/1004	0.810±0.045	1.123±0.030
PD12	986/1024	−0.045±0.011	1.24	986/986	−2.117±0.084	1.426±0.044

Table 4.2: Dark current (nA/cm^2) at 25, 0, and −40 °C. Due to the limited range of the A/D converter, not all pixels could be captured at once. This problem is most severe for PD9, for which the stated data might not be representative of the true population. The raw data in the table represents the mean and standard deviation of the captured data. The gaussian fits shown in the table are useful due to the skewed nature of many of the dark current distributions, especially at warmer temperatures. Pixels very far from the mean were removed and a gaussian was fit to the histogram, providing a better estimate of a typical dark current. Sometimes this procedure fails, as in PD5 at room temperature, where a negative value was obtained despite all dark currents being positive. See the scatter plots for more information.

Pixel Type	Temperature	Mean	Std. Dev.
PD1	25 °C	88.3	30.2
	0 °C	81.1	15.4
	−40 °C	100.7	6.1
PD2	25 °C	74.9	14.5
	0 °C	97.1	6.9
	−40 °C	151.6	9.2
PD5	25 °C	74.5	30.9
	0 °C	76.8	12.2
PD6	25 °C	70.2	22.0
	0 °C	98.5	11.8
PD10	25 °C	70.0	3.2

Table 4.3: Noise in pixel types as a function of temperature.

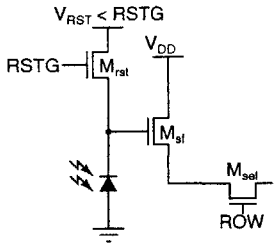
Chapter 5

Review of Pixel Designs

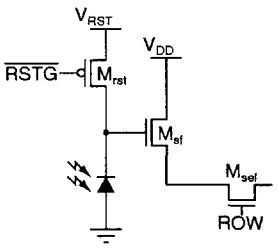
As shown in the previous chapter, noise in APS-1 is rather high. Current trends in fabrication at Lincoln Laboratory are pushing toward 3-D stacked circuitry [16, 17], and although photogates can be operated with lower noise using correlated double sampling, they are typically not available in this 3-D process. The next generation of devices in this program will exclusively use photodiodes as detectors. Low-noise operation of photodiodes can be achieved, however; many approaches to reducing noise have been presented in the literature. This chapter is a review of some of these architectures, with an emphasis on potential application toward x-ray astronomy. Specific attention is paid to *reset noise*, *image lag*, and *pixel size*. Reset noise is mainly the result of thermal noise in the reset transistor, sampled onto the photodetector capacitance, after the reset transistor turns off. Image lag is the persistence of an image onto the subsequent image, due to incomplete reset. Pixel size is important as it affects fill factor, quantum efficiency, and spatial resolution.

5.1 Standard Reset Methods

An important difference among active pixels is the method used to reset the photodetector. The two main variations are called hard reset and soft reset.



(a) Hard reset with NMOS reset



(b) Hard reset with PMOS reset

Figure 5-1: Two methods of achieving hard reset in an APS pixel. In both cases the reset transistor remains in the linear region, resulting in reset without image lag but with high noise. (a) A low value of V_{RST} means that the photodiode will have a lower reset level. (b) Hard reset with a PMOS reset transistor. CMOS pixels typically come at the cost of larger area in bulk processes; an SOI process, on the other hand, can pack PMOS and NMOS transistors close together.

5.1.1 Hard Reset

In *hard reset*, the reset transistor operates in the linear region. It may either be accomplished by lowering the drain voltage below the gate, or by using a PMOS reset transistor (Figure 5-1). This produces a reset noise voltage

$$V_{n,hard}^2 = \frac{kT}{C_{pd}}. \tag{5.1}$$

where C_{pd} is the equivalent capacitance of the photodetector. Measured in electrons, this noise is given by

$$N_e = \frac{\sqrt{kTC_{pd}}}{q}. \tag{5.2}$$

A pixel in hard reset has zero image lag. Lag occurs when a pixel is not reset completely; some fragment of the original image remains. Intuitively, a pixel with hard reset has no lag as long as the pixel is reset for enough time to charge C_{pd} up to V_{RST}, which is easily met in practice. All pixels, no matter the pre-reset value, will reset to V_{RST}, and there will be no trace of a previous image.

In a typical CMOS process, hard reset would be accomplished with an NMOS reset transistor with its drain voltage lower than its gate (Figure 5-1(a)). The dynamic range is subsequently reduced, since V_{RST} is lower than V_{DD}. A higher performance

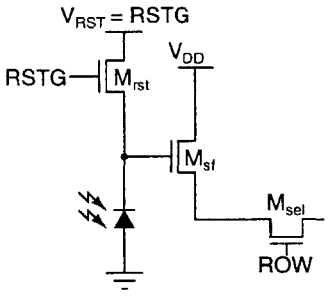


Figure 5-2: An APS pixel using soft reset. As the pixel is reset and the photodiode voltage rises, the NMOS reset transistor, in saturation, begins to enter the subthreshold region, gradually turning off. It cannot fully reset the pixel, causing some image lag, but at the same time reducing noise due to the feedback inherent in the process.

hard reset pixel may be realized with a PMOS reset transistor (Figure 5-1(b)). However, due to restrictions in spacing between n-type and p-type transistors, using both transistor types in a pixel requires a large amount of space, reducing fill factor. In SOI, however, every transistor is constructed on its own island, and PMOS transistors can be close to NMOS transistors. It is quite practical, in this process, to use both transistor types in a single pixel.

5.1.2 Soft Reset

Soft reset is a simple alternative to hard reset, where the reset transistor operates in saturation (Figure 5-2). As in hard reset, the reset transistor is turned on to pull the photodetector back up to a high voltage. The photodetector, at the source of the reset transistor, will rapidly rise to $V_{RST} - V_{th}$, at which point the reset transistor will enter the subthreshold region and begin to turn off. The sense node will continue slowly rising to V_{RST}, but an extremely long reset period would be required to reach this voltage.

Since the photodetector voltage is not pulled all the way to V_{RST}, a pixel in soft reset suffers from a smaller dynamic range. Reduced dynamic range, however, is not important for x-ray detection. X-rays emitted by ^{55}Fe create 1620 electrons in silicon [9]. Assuming a responsivity of 5 μV/e$^-$, as measured on APS-1, such an electron would create an 8 mV signal. X-rays with energies higher by a factor of ten

would still be well within the dynamic range of this pixel.

Since the pixel is not pulled to a fixed voltage, its final voltage after reset depends on where it started; that is, the image will possess some lag. Lag results in reduced linearity in low-light situations, as compared with hard reset [18]. For space-based x-ray detection, lag can cause major performance degradation.

Soft reset does possess a significant advantage over hard reset. Reset noise in soft reset is [19]

$$V_{n,soft}^2 = \frac{kT}{2C_{pd}}.$$

The lower reset noise is due to a feedback mechanism inherent in soft reset. The reset current is partially controlled by the photodetector voltage. A fluctuation on this node in the positive direction, for example, would lower v_{GS}, reducing the reset current, slowing the increase in the photodetector voltage. This negative feedback is responsible for the lower noise level.

5.2 Combining hard and soft reset

Several techniques combine the benefits of both hard reset and soft reset. The basic concept is to do a hard reset, removing lag, followed by a soft reset, which lowers noise. Reset noise is $kT/2C_{pd}$, but without any lag.

5.2.1 Pseudo-flash reset

One simple scheme combining hard and soft resets is *pseudo-flash reset* [19]. Pseudo-flash reset uses an ordinary APS pixel, but with the reset drain voltage, V_{RST}, pulsed low at the start of reset, ensuring a quick hard reset, removing lag. Soft reset is achieved by subsequently returning V_{RST} high. Note that this scheme requires keeping V_{RST} separate from V_{DD}, and thus an additional wire is required for each pixel.

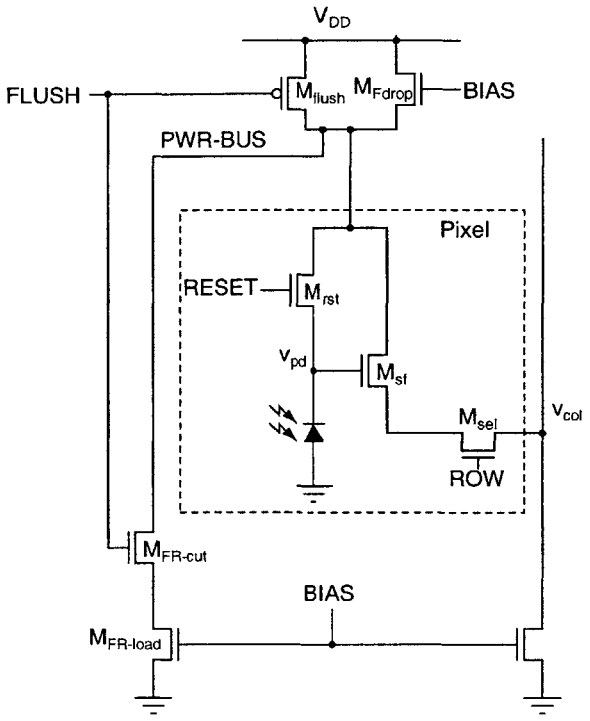


Figure 5-3: An APS circuit using flushed reset [18]. The pixel is shown in the dashed box, while the remaining circuitry is column-level. The effective V_{DD} level of the pixel is lower than V_{DD} due to the column transistor M_{FDROP}.

5.2.2 Flushed reset

A slightly more complicated scheme is *flushed reset* [18]. Flushed reset uses a standard three-transistor pixel, along with a five-transistor *reset-assist* circuit per column (Figure 5-3). Reset begins with a flush phase, where *FLUSH* and *RESET* are high, causing a hard reset. *PWR-BUS* is disconnected from V_{DD} during this phase, and the photodiode is instead reset to a lower level, given by

$$V_{FLUSH} = V_{BIAS} - V_{th} - \sqrt{\frac{2I_{BIAS}}{\mu C_{ox}(W/L)_{Fdrop}}} \tag{5.3}$$

Following this, *PWR-BUS* is returned to V_{DD} by lowering *FLUSH* and ordinary soft reset occurs, resulting in low noise.

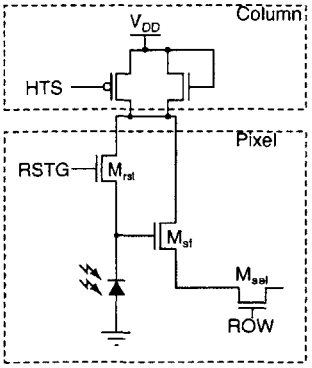


Figure 5-4: HTS reset pixel [20]. Asserting *HTS* at the start of the reset period causes a hard reset. The pixel can then be shifted to soft reset by lowering *HTS*. This results in low lag and low noise.

5.2.3 Hard-to-soft reset

Hard-to-soft (HTS) reset is another scheme to combine hard and soft resets [20]. The pixel is an unaltered, standard APS pixel, with two additional transistors per column (Figure 5-4). During the first phase of reset, *HTS* is high. The drain of the reset transistor is lower than the gate because of the diode connected FET, causing a hard reset. Soft reset is achieved by lowering *HTS*, connecting the reset drain to V_{DD} and putting M_{RST} in the saturation region. Similarly to the flushed reset pixel, the HTS pixel has a lower reset level than an ordinary APS pixel.

5.3 Active Reset

One architecture that allows noise reduction below $kT/2C_{pd}$ is active reset.

5.3.1 Fowler active reset pixel

Active reset, introduced by Fowler *et al.* [21], uses a high gain amplifier to greatly reduce reset noise through capacitive feedback and band-limiting (Figure 5-5). Measurement has shown noise as low as

$$V_{n,active}^2 = \frac{kT}{18C_{pd}}. \tag{5.4}$$

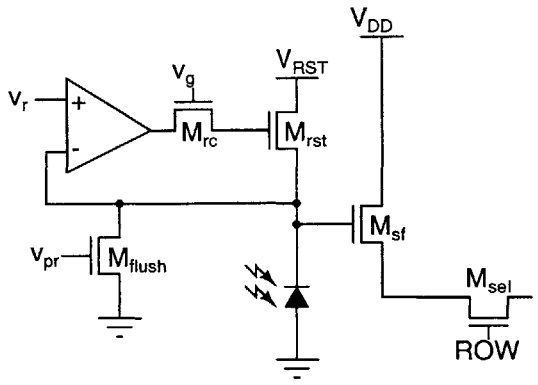


Figure 5-5: Fowler active reset pixel [21]. The op amp's negative feedback controls the reset current, reducing noise. Results have been reported showing noise as low as $kT/18C_{pd}$. Transistor M_{flush} is used to remove lag.

This pixel has a more complicated reset sequence than other designs that have been examined. Initially, v_{pr} is pulsed to remove lag. Transistor M_{rc} then turns on, and v_r begins ramping upwards, gradually resetting the pixel to a high level. Next v_r is lowered, but the photodiode node stays high since there is no pull-down path. Finally v_g drops low, completing reset of the pixel.

The Fowler active reset pixel can be implemented efficiently with six transistors per pixel, and does not introduce any lag.

5.3.2 Pain active reset pixel

A very similar scheme, combining active reset with flushed reset, was introduced by Pain *et al.* [22]. This pixel has shown noise levels similar to the Fowler active reset pixel. This architecture requires four transistors per pixel, with more extensive column-level circuitry, including an op amp (Figure 5-6). Operation is very similar to the Fowler circuit. Reset begins by activating the flush circuit (see Section 5.2.2) to remove lag. Next the transmission gate turns on and v_r rises. The negative feedback provided by the op amp reduces reset noise in exactly the same manner as in the Fowler active reset pixel.

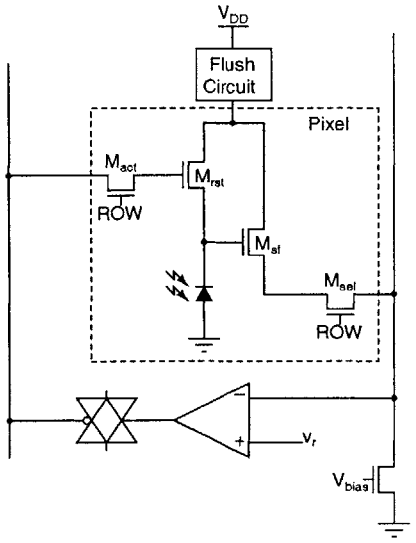


Figure 5-6: Pain active reset pixel [22]. This design uses less transistors per pixel, instead putting supporting circuitry on the column level. The op amp's negative feedback controls the reset current, with reported noise as low as $kT/30C_{pd}$. This pixel uses fewer transistors than Fowler's implementation and can therefore be used to achieve higher fill factor.

5.4 Capacitive Manipulation

Several recent designs reduce noise by manipulating the equivalent capacitance used to calculate kTC noise.

5.4.1 Kleinfelder CDS pixel

Kleinfelder *et al.* demonstrated an imager using 6 transistors and a capacitor in each pixel to lower noise (see Figure 5-7) [23]. Noise voltage is lowered to

$$V_n^2 = \frac{1}{A_{SF1}}\left(\frac{kT}{C_2}\right) \tag{5.5}$$

which, in electrons, is

$$N_e = \sqrt{\frac{kT}{C_2}}\left(\frac{C_{pd}}{qA_{SF1}}\right). \tag{5.6}$$

Here, the noise reduction is limited only by the size of the capacitor C_2 that can fit within each pixel. As suggested by Kleinfelder, the pixel uses NMOS reset transistors,

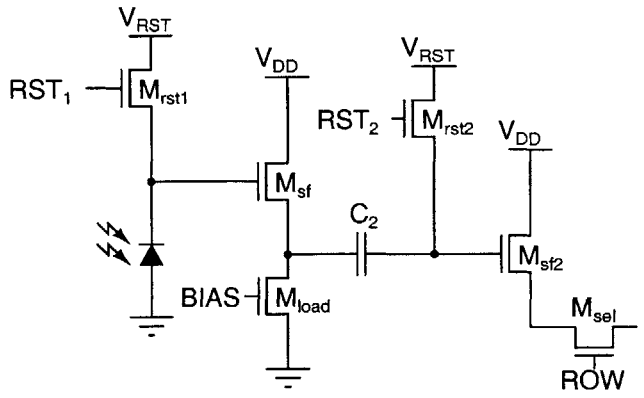


Figure 5-7: Kleinfelder CDS pixel [22]. This design uses a two-phase reset to achieve low noise, limited by the size of C_2 (see Equation 5.5). This design has a relatively large pixel size.

and hence suffers from lag. In an SOI implementation, it should be easy to use PMOS transistors instead, eliminating lag.

The Kleinfelder pixel is operated with a a two-part reset. In the first phase, both RST_1 and RST_2 are held high. Integration begins when RST_1 is lowered. The noise from RST_1 is transferred to C_2, where it is subtracted by the capacitor. Since the initial reset noise is subtracted, this can be considered as a form of correlated double sampling. Lastly, RST_2 is lowered, causing a smaller kT/C_2 noise voltage to be sampled onto the capacitor. Kleinfelder reports noise on the order of $kT/9C_{pd}$.

5.4.2 Takayanagi feedback pixel

Takayanagi *et al.* demonstrated an alternate pixel design using capacitive feedback [24]. This design uses four transistors and two capacitors per pixel, with additional column-level circuitry (Figure 5-8). The circuit is operated by asserting $VDSW$, RST_1, and RST_2. First, RST_1 is dropped, followed by RST_2, followed by $VDSW$. The result is similar to the Kleinfelder circuit, where the order of various reset signals allows a reduction in noise because of the presence of large capacitors. In this pixel, noise is reduced to

$$v_n^2 = kT\left(\frac{C_2}{C_{pd}+C_2}\right)^2\left(C_3+\frac{C_{pd}C_2}{C_{pd}+C_2}\right)^{-1}. \tag{5.7}$$

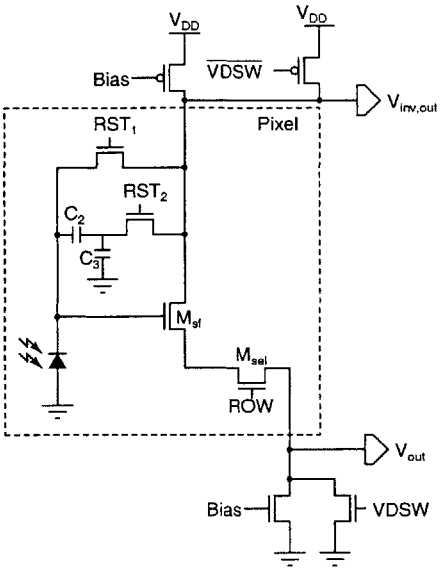


Figure 5-8: Takayanagi capacitive feedback pixel [24]. This has been shown to reduce noise to approximately $kt/7C_{pd}$. It has a relatively large pixel size.

A fabricated imager showed a noise level $V_n^2 \approx kT/7C_{pd}$.

5.4.3 Capacitive Transimpedance Amplifier

Ordinary APS pixels use a source follower in each pixel to convert the integrated charge into a voltage which can be read out. An interesting alternative is to use a *capacitive transimpedance amplifier* (CTIA) in each pixel. A CTIA is a high gain amplifier with a capacitor in the negative feedback path. During reset, the pixel is connected to the large column capacitance, reducing reset noise. After integrating on the small photodiode capacitance, charge is transferred to the smaller feedback capacitor, also reducing readout noise.

A CTIA pixel is illustrated conceptually in Figure 5-9. Assuming a large voltage gain A, all of the generated charge will be transferred to the feedback capacitor. Since the inverting input is a virtual ground, the pixel output voltage is

$$v_{out} \approx \frac{n_e}{C_{fb}} \tag{5.8}$$

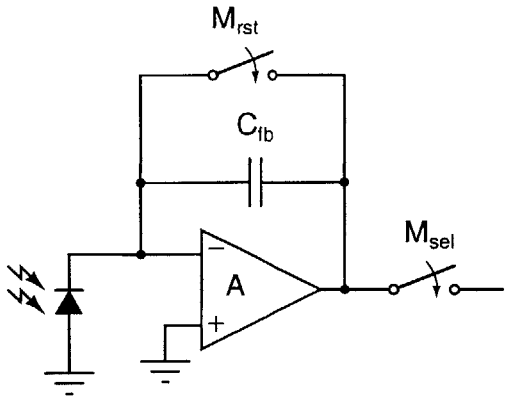


Figure 5-9: CTIA pixel. Charge integrated on the photodiode is transferred to C_{fb}. Reset noise is reduced because of the small value of the feedback capacitance. However, the op amp contributes some additional noise. This design requires a high-gain amplifier in every pixel, something that is not always practical for a conventionally fabricated array [25].

independent of the photodiode capacitance [25]. For $C_{fb} \ll C_{pd}$, the input-referred noise is given approximately by

$$N_e = \frac{\sqrt{kTC_{fb}}}{q}. \tag{5.9}$$

5.5 Summary

The discussion of different pixel types is summarized in Table 5.1. Note that the greatest reported noise reductions come from active reset, as well as the CTIA pixel, where noise reduction depends highly on a specific design and capacitor choice. The Kleinfelder CDS pixel offers great potential if large capacitors can be used. High-performance designs such as these would usually be prohibitive in an ordinary CMOS process because of the large pixel sizes. However, a 3-D fabrication process creates the perfect opportunity to explore such designs.

Pixel type	Reset Noise	Lag	Pixel Contents	Other
Hard	kT/C	No	3 FETs	
Soft	$kT/2C$	Yes	3 FETs	CMOS, or low reset level
Pseudo-flash	$kT/2C$	No	3 FETs	Extra signal per pixel
Flushed	$kT/2C$	No	3 FETs	Lower reset level, column circuitry
HTS	$kT/2C$	No	3 FETs	Lower reset level
Fowler Active	$kT/18C$	No	6 FETs	Op amp per pixel (included in 6)
Pain Active	$kT/30C$	No	4 FETs	Column op amp
Kleinfelder	$kT/9C$	Yes	6 FETs, 1 cap	Big cap $\rightarrow$ lower noise
Takayanagi	$kT/7C$	Yes	4 FETs, 2 caps	
CTIA Pixel	kT/C_{fb}	Yes	2 FETs, 1 cap, 1 op amp	Small cap $\rightarrow$ lower noise

Table 5.1: Summary of different pixel types.

Chapter 6

Detailed Pixel Analysis

Of the pixel designs discussed in the previous chapter, several stand out as offering the strongest potential benefits in a future imager. Specifically, the Pain active reset pixel [22], Kleinfelder CDS pixel [23], and the CTIA pixel [25] all provide high performance. The cost of this high performance typically is low fill factor. With a stacked, three-dimensional fabrication process, however, fill factor can remain high. This chapter presents in-depth analysis of each of these pixel types, giving theoretical predictions as well as simulated results. Flicker noise will not be taken into account, as it is usually much smaller than thermal and shot noise [26]. As the goal is to investigate designs for a future imager in a 3-D integrated process, the equivalent photodiode capacitance in all simulations will be 5 fF, as expected in this process.

6.1 Signal-Chain Noise

Signal-chain noise in APS imagers is insignificant compared to reset noise. To illustrate this, a simple model of a photodiode pixel is shown in Figure 6-1. Also shown are the column bus, the load transistor for the source follower, and the column capacitance. The column capacitance, C_{col}, consists of any parasitic effects because of the large bus, as well as any explicitly added capacitance used as a sample and hold capacitor. This capacitance is typically on the order of 1 pF.

Given the large magnitude of C_{col}, the noise from M_{rst} will dominate. Transistor

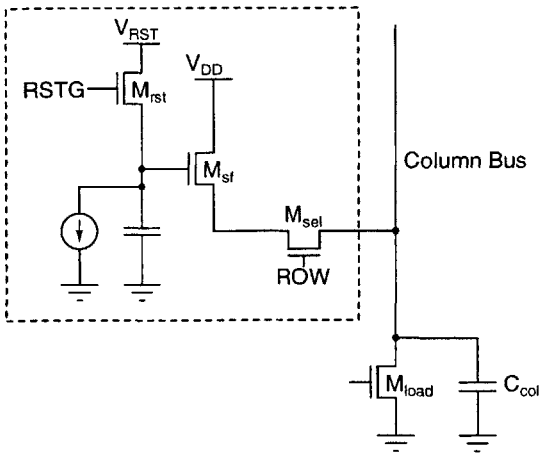


Figure 6-1: Simple model of photodiode pixel. The boxed portion represents the actual pixel contents. The photodiode is modeled by a capacitor, C_{pd}. A current source, I_{photo}, represents incident light. Also shown are the column bus, load transistor for the source follower, and column capacitance. The large column capacitance makes the noise from sources besides M_{rst} insignificant.

M_{sel} can be ignored since its channel resistance (and therefore its noise contribution) is much smaller than the transconductances of the others transistors [25]. Intuitively, M_{sf}, M_{load}, and any other transistors that may be present in more advanced pixel designs are capacitively loaded by C_{col}. The noise from these transistors will be of the form

$$V_n^2 = \alpha \frac{kT}{C_{col}} \ll \frac{kT}{C_{pd}} \tag{6.1}$$

where α is some value determined by the circuit. Referred to the photodiode node, the noise in electrons will take the form

$$N_e = \sqrt{\frac{\beta C_{pd}}{C_{col}}} \left(\frac{\sqrt{kTC_{pd}}}{q} \right) = \left(\sqrt{\frac{\beta C_{pd}}{C_{col}}} \right) \cdot N_{e,RST} \tag{6.2}$$

where β depends on the specifics of the circuit. The large ratio of C_{col} to C_{pd} ensures that M_{rst} dominates the other noise contributions. Signal-chain noise as low as two electrons has been reported with a photodiode capacitance of approximately 5 fF [25]. In comparison, the reset noise for this photodiode is 16.9 electrons under soft reset. Since the noise sources are uncorrelated, the signal-chain and reset noise combine to

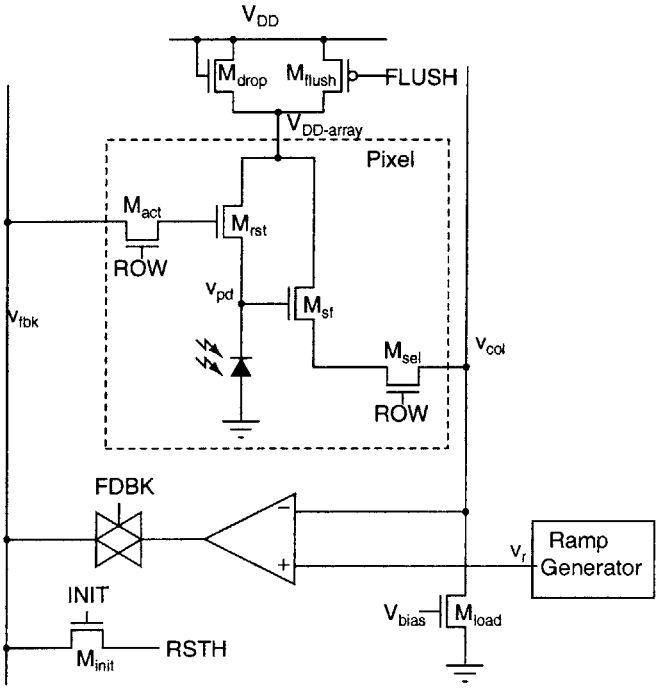


Figure 6-2: Full schematic of APS pixel using active reset. The pixel consists of four transistors, plus associated column-level circuitry. The op amp provides negative feedback which controls the reset current, lowering noise. Pain reports noise as low as $kT/30C_{pd}$ [22].

create 17.0 electrons of noise.

Throughout the rest of this chapter, calculations will ignore signal-chain noise and only regard reset noise. Simulations will, of course, account for all noise sources.

6.2 Active Reset Pixel

A full schematic of the active reset pixel is shown in Figure 6-2, and a timing diagram in Figure 6-3 [22].

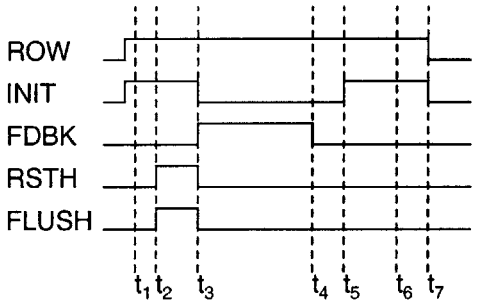


Figure 6-3: Timing diagram for Pain active reset pixel (see Figure 6-2) [22].

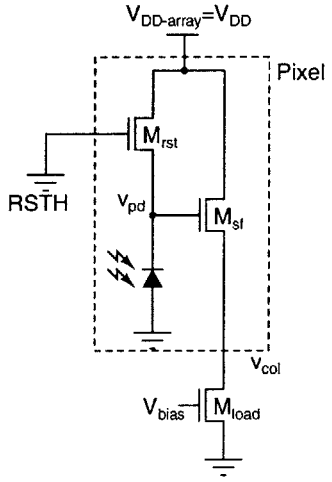


Figure 6-4: Equivalent circuit for active reset pixel at time t_1 (see Figure 6-3). The reset transistor, M_{rst}, is turned off, and the charge that has been integrated on the diode can be read out at v_{col}.

6.2.1 Timing

Signal Level Readout

The active reset pixel operates in a read first, reset later mode. At time t_1, with *INIT* high and the low *RSTH* controlling the gate of M_{rst}, the signal level is sampled. An equivalent circuit, with switches either replaced by wires or open circuits, is shown in Figure 6-4. The pixel looks like an ordinary APS pixel that is not being reset and is ready to be read out.

Initial Hard Reset

Reset begins at t_2 with the rise of $RSTH$ and $FLUSH$. An equivalent circuit is given in Figure 6-5. Since M_{flush} is turned off, the voltage on $V_{DD-array}$ is not pulled all the way up to V_{DD}, but rather to some lower value with an upper bound given by

$$V_{DD-array} < V_{DD} - V_{th}. \tag{6.3}$$

The gate of M_{rst} is controlled by $RSTH$. Transistor M_{rst} will always operate in the linear region if

$$\max |V_{DS}| < V_{GS} - V_{th}. \tag{6.4}$$

Combining Equations 6.3 and 6.4, and eliminating terms on both sides of the inequality yields the condition

$$V_{DD} \leq V_{RSTH}. \tag{6.5}$$

To assure linear region operation, it suffices to keep V_{RSTH} at the same voltage as V_{DD}. The result of keeping M_{rst} in the linear regime is a hard reset, resulting in zero image lag.

Active Reset

The hard reset phase ends at t_3 with the fall of $INIT$, and at the same time the active reset phase begins with the rise of $FDBK$ (see Figure 6-6 for an equivalent circuit). At the same time, v_r begins ramping up from 0 to V_{DD}. The negative feedback provided by the op amp keeps v_{col} very close to v_r. Any changes in v_{col} due to noise in M_{rst} are counteracted by a subsequent opposite change in the op amp output. The op amp output controls the gate of M_{rst}, and therefore is capable of canceling out much of the noise due to M_{rst}. The ramp is necessary because M_{rst} can only pull up; if v_r were held at a constant high level, and noise were to cause v_{col} to overshoot v_r, the op amp would turn off and the reset would immediately end. By slowly increasing v_r, both overshoots and undershoots in the reset process can be compensated for.

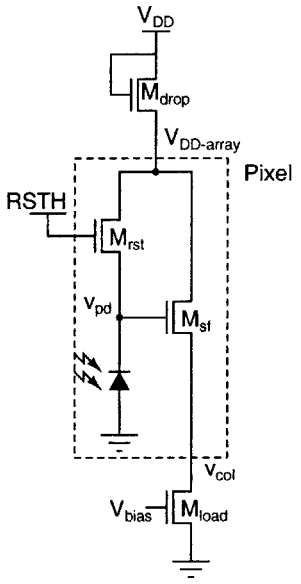


Figure 6-5: Equivalent circuit for active reset pixel between times t_2 and t_3 (see Figure 6-3). The presence of M_{drop} causes $V_{DD-array}$ to be less than V_{DD}. The high voltage $RSTH$ on the gate of M_{rst} causes a hard reset of the pixel, resulting in the complete removal of image lag.

Reset Level Readout

At t_4, the active reset phase ends. The second readout phase begins shortly thereafter, at t_5. At some time following t_5 (shown in the timing diagram as t_6), sampling of the reset level occurs. The equivalent circuit during this period is the same as during t_1 (see Figure 6-4). Finally, at t_7, the reset cycle is concluded, and charge integrates continuously until t_1 is reached again on the next frame.

6.2.2 Analysis and Noise Modeling

To analyze noise in the active reset circuit, an op amp model is first needed. Chen and Kleinfelder suggest a folded-cascode op amp [27]. This type of op amp is modeled as having a single pole response, with gain

$$A(s) = \frac{A_0}{1 + \tau s},$$

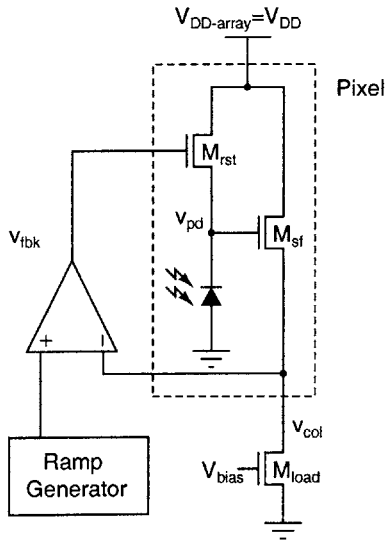


Figure 6-6: Equivalent circuit for active reset pixel between times t_3 and t_4 (see Figure 6-3). The voltage v_{fbk} on the gate of M_{rst} is controlled by the ramping voltage v_r and the output signal from the pixel, v_{col}. A fluctuation on v_{col} causes the opposite change in the reset current because of the negative feedback provided by the op amp.

where τ is the time constant given by the ratio of the op amp capacitive load C_L to its first-stage transconductance g_{ma} [28]. In the active reset pixel, C_L represents the relatively large capacitance of the feedback bus line.

Taking into account just the thermal noise in M_{rst} (with transconductance g_{mr}), modeled as a current noise

$$I_n^2 = 4kTg_{mr}\Delta f$$

gives an input-referred voltage noise of

$$V_{n,M_{rst}}^2 = \frac{kT}{C_{pd}}\frac{1}{A_0+1}\left(1+\frac{A_0\ g_{mr}C_L}{g_{ma}C_{pd}+g_{mr}C_L}\right). \tag{6.6}$$

Rearranging the fraction gives additional insight. Collecting terms into time constants yields

$$V_{n,M_{rst}}^2 = \frac{kT}{C_{pd}}\frac{1}{A_0+1}\left(1+\frac{A_0\ g_{mr}C_L/g_{ma}C_{pd}}{1+g_{mr}C_L/g_{ma}C_{pd}}\right). \tag{6.7}$$

C_{pd} is approximately 5 fF, and a typical column bus capacitance is on the order of 2 pF [25]. Simulations show that g_{mr} is on the order of 10 nA/V (M_{rst} must be

subthreshold for such low transconductance). The transconductance of the op amp, g_{ma} can easily be on the order of 100 μA/V. With these numbers,

$$\frac{g_{mr}}{g_{ma}}\frac{C_L}{C_{pd}} \ll 1. \tag{6.8}$$

This simplification gives

$$V^2_{n,M_{rst}} = \frac{kT}{C_{pd}}\frac{1}{A_0+1}\left(1 + A_0\frac{g_{mr}}{g_{ma}}\frac{C_L}{C_{pd}}\right). \tag{6.9}$$

Since $A_0 \gg 1$, this equation can be rewritten once more as

$$V^2_{n,M_{rst}} = \left(\frac{1}{A_0} + \frac{g_{mr}}{g_{ma}}\frac{C_L}{C_{pd}}\right)\frac{kT}{C_{pd}}. \tag{6.10}$$

Remembering the restriction imposed by Equation 6.8, noise due to M_{rst} is greatly reduced over the standard pixel reset noise of kT/C_{pd}.

There is a major additional noise source present in the active reset pixel that is not found in an ordinary APS design, namely that of the op amp. It is possible to treat the noise of the op amp as one input-referred voltage source with the form

$$V^2_{n,opamp} = 4kT\gamma\Delta f$$

where γ is an equivalent resistance that depends on the op amp design. Analysis similar to that carried out for noise from M_{rst} yields

$$V^2_{n,opamp} = g_{mr}\gamma\left(\frac{1}{A_0} + \frac{g_{mr}}{g_{ma}}\frac{C_L}{C_{pd}}\right)\frac{kT}{C_{pd}} = g_{mr}\gamma \cdot V^2_{n,M_{rst}}. \tag{6.11}$$

Combining these two noise sources yields a final noise voltage of

$$V^2_{active} = (1 + g_{mr}\gamma)\left(\frac{1}{A_0} + \frac{g_{mr}}{g_{ma}}\frac{C_L}{C_{pd}}\right)\frac{kT}{C_{pd}}. \tag{6.12}$$

Another point of view regarding the noise reduction term, shown in Equation 6.8, provides additional insight. This term may be considered the ratio of the sense node

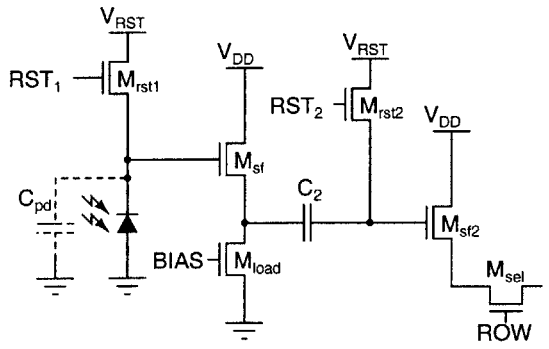


Figure 6-7: Full schematic of APS pixel using CDS [23]. The pixel consists of six transistors and a capacitor. The diode is modeled by the capacitor C_{pd}. The capacitor C_2 causes lower reset noise. Kleinfelder reports noise of approximately $kT/9C_{pd}$.

bandwidth to the op amp bandwidth. If the op amp bandwidth is large, it can respond fast enough to compensate for most of the thermal noise in the M_{rst}. Conversely, a slow op amp cannot cancel out high frequency noise, and the noise reduction term will be smaller.

The preceding analysis was an approximation, assuming that the thermal noise in M_{rst} and the op amp noise are stationary processes. Since the bias point of M_{rst} changes, its noise is non-stationary. Nevertheless, this approximation allows insight into the circuit operation without an overabundance of difficult mathematics. A full analysis of a similar circuit is presented in the literature [27].

6.3 Kleinfelder CDS Pixel

A full schematic of the Kleinfelder CDS pixel is shown in Figure 6-7, and a timing diagram in Figure 6-8 [23].

6.3.1 Timing

Ordinary Reset

Operation of the Kleinfelder pixel begins with an ordinary reset. From t_1 to t_2 both M_{rst1} and M_{rst2} are turned on. With both reset transistors on, both capacitive nodes

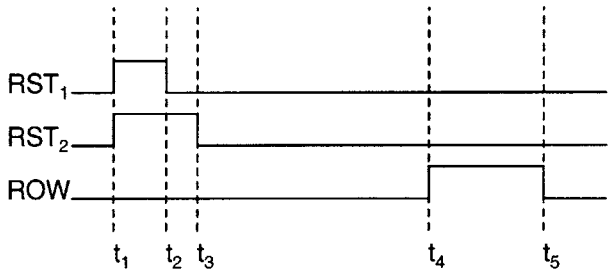


Figure 6-8: Timing diagram for Kleinfelder CDS pixel (see Figure 6-7) [23].

are pulled near the supply V_{RST}. As given by Kleinfelder, the transistors are in the saturation region, causing soft reset at these nodes. In an SOI process, however, p-type reset transistors can be used, allowing a lag-free reset.

Noise Reduction Phase

At t_2, M_{rst1} turns off, capturing a noise voltage kT/C_{pd} on the photodiode node. The source follower M_{sf} causes this noise voltage to appear across C_2 as an offset. At t_3, M_{rst1} turns off, storing the noise from M_{rst1} as a negative charge offset across the capacitor. This noise charge is the reset noise from M_{rst1}, and owing to the sign inversion through the capacitor, it is subtracted from the output signal. Correlated double sampling is effectively performed on the noise from the initial reset. However, reset noise is still present because of M_{rst2}, which creates its own kT/C_2 reset noise. Since $C_2 > C_{pd}$, the result is a reduced amount of noise.

Integration and Readout

From t_3 to t_4 charge integrates as usual on the photodiode node. At t_4 the row select transistor M_{sel} turns on, allowing the integrated signal to be read out.

6.3.2 Analysis and Noise Modeling

With CDS, the noise voltage at C_2 is due entirely to M_{rst2} (ignoring the much smaller thermal noise sources in the source followers, current load, and row select switch),

and is equal to

$$V_{n,C_2}^2 = \frac{kT}{C_2}, \tag{6.13}$$

giving an input referred noise voltage of

$$V_{n,input}^2 = \frac{1}{A_{sf}^2}\left(\frac{kT}{C_2}\right) \tag{6.14}$$

where A_{sf} is the gain of the source follower M_{sf} and is close to unity. Expressed in electrons, the noise charge is

$$N_e = \frac{V_{n,input} \cdot C_{pd}}{q} = \frac{C_{pd}}{q}\sqrt{\frac{1}{A_{sf}^2}\left(\frac{kT}{C_2}\right)} = \frac{C_{pd}}{qA_{sf}}\sqrt{\frac{kT}{C_2}}. \tag{6.15}$$

It is useful to rewrite Equation 6.15 in terms of the usual noise charge, $\sqrt{kTC_{pd}}$, to see the benefit from this design. The result is the following expression:

$$N_e = \left(\frac{\sqrt{kTC_{pd}}}{q}\right)\left(\frac{1}{A_{sf}}\sqrt{\frac{C_{pd}}{C_2}}\right). \tag{6.16}$$

Noise is reduced by a factor depending on the ratio of C_{pd} to C_2. The larger C_2 can be made, the better performance can be achieved.

6.4 CTIA Pixel

A conceptual view of the CTIA pixel is shown in Figure 5-9. A transistor level schematic for a low fixed-pattern noise (FPN) CTIA pixel is shown in Figure 6-9 [26]. This pixel can be operated in a high-gain or low-gain mode. The timing diagrams for these are shown in Figure 6-11.

6.4.1 Fixed Pattern Noise

Most CTIA pixels suffer from high FPN due to capacitor mismatch. Noise is lowered by having a small feedback capacitance. Small capacitances create matching problems, however, as small capacitors are likely to have higher percentage mismatches.

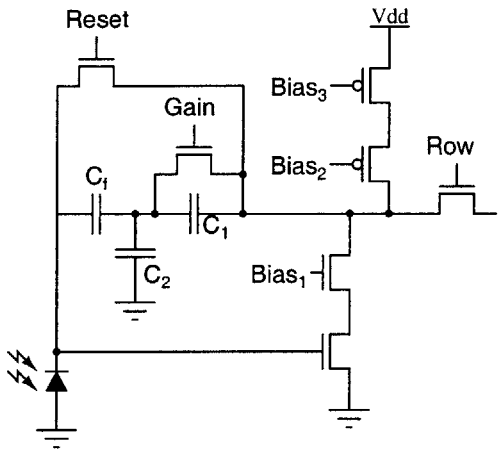


Figure 6-9: Low fixed-pattern noise CTIA pixel [25]. The pixel may be operated in high-gain or low-gain mode. The T-configuration of the capacitors allows realization of a small equivalent capacitance using larger, better-matched capacitors. A cascode common-source amplifier is used as the in-pixel high-gain amplifier.

The low-FPN CTIA circuit solves this problem by using a T-network to realize a small capacitance.

The T-network of capacitors is similar to the familiar resistive T-network. An inverting op amp using a resistive T-network is shown in Figure 6-10. The feedback resistors provide an effective resistance of 10 MΩ without having to use extremely large resistors [29]. Large resistors are undesirable both in discrete and integrated circuits due to larger parasitics, and because of physical size in integrated circuits. The capacitive T-network is very similar, except that it allows the realization of a small capacitance using large capacitors, which are more desirable as they can be matched more precisely.

Simple nodal analysis reveals that the equivalent capacitance here is given by

$$C_{eq} = \frac{C_f}{1 + C_2/C_1} \tag{6.17}$$

where C_f, C_1, and C_2 are as given in Figure 6-9. As an example, this pixel design was originally demonstrated using C_f=22 fF, C_1=20 fF, and C_2=200 fF, for an equivalent capacitance of 2 fF. This particular imager had a photodiode capacitance of 120 fF, so the T-network offered substantial improvement while still allowing the use of large

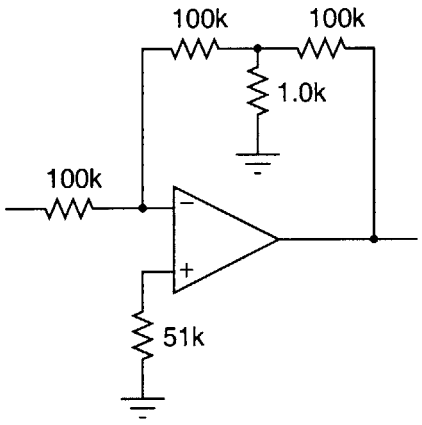
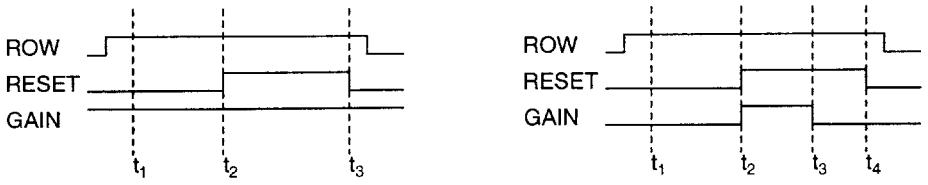


Figure 6-10: Op amp with resistive T-network. This network allows a high effective resistance using lower-valued resistors [29]. The same idea allows the realization of well-matched small capacitors in the low-FPN CTIA pixel.



(a) Low gain

(b) High gain

Figure 6-11: Timing diagrams for CTIA pixel in (a) low-gain and (b) high-gain modes. The differing voltages on *GAIN* during integration cause the effective feedback capacitance to change, resulting in different gains.

capacitors [26].

6.4.2 Timing and Gain Selection

Low-gain Mode

The signal *GAIN* determines whether the low-FPN CTIA pixel operates in low-gain or high-gain mode. Figure 6-11(a) shows the timing digram for the low-gain mode. *GAIN* is held high throughout, effectively shorting out C_1. The result is that the equivalent capacitance is simply C_f, and not the value given by Equation 6.17 for a

T-network. The high gain of the amplifier causes the pixel output voltage to be

$$v_{out} = \frac{n_e}{C_{fb}}, \tag{6.18}$$

so a larger feedback capacitance results in lower gain.

The timing for the CTIA pixel is straightforward. At t_1, the signal level is sampled. At t_2, *RESET* goes high, shorting the feedback capacitor. Since *GAIN* is already high, both capacitors are shorted to their original levels. At t_3, *RESET* falls, and integration begins. A reset level may be taken at this time. Integration continues until the row is accessed again.

High-gain Mode

The timing for high-gain mode is very similar to that of low-gain mode. Figure 6-11(b) shows the timing digram for the high-gain mode. At t_1, the signal level is sampled. At t_2, *RESET* and *GAIN* go high, shorting the feedback capacitors. Since the high-gain mode operates with *GAIN* at a low-voltage, *GAIN* must fall at t_3 before a reset level can be taken. Any changes that may occur due to the lowering of *GAIN* are taken care of by holding *RESET* high for a bit longer. Finally, *RESET* falls at t_4, allowing integration to begin. The reset level may be sampled at this time.

6.4.3 Analysis and Noise Modeling

Calculating the noise in a CTIA pixel is rather complicated. There are two switches present, and three capacitors to be reset, counting the column capacitance. The op amp contributes noise, and there is also a noise correlation to take into account when the pixel is being reset. A full equation for noise in a CTIA, taking into account all of these factors, is given by [25]

$$V_n^2 = \frac{kT}{C_{pd} + C_{SH} + \zeta C_{fb}} \left[2\left(A_{cg} - 1\right)^2 \left(1 + \beta\right) + \zeta \left\{ 1 + \frac{1}{A} \frac{\left(A_{cg} - 1 - \theta A_{cg}\right)^2}{A_{cg} - 1 + \theta A_{cg}} \right\} \right] \tag{6.19}$$

where

$$\zeta = g_m R_{rst}, \qquad \theta = \frac{C_{SH}}{C_{fb}}, \qquad A_{cg} = \frac{C_{fb} + C_{pd}}{C_{fb}},$$

C_{SH} is the column sampling capacitance, g_m is the transconductance of the CTIA, R_{rst} is the on-resistance of the reset switch, and β represents noise contributions from the op amp.

Using Equation 6.18, this voltage can be converted into a noise charge in electrons, given by

$$N_e = \frac{C_{fb}}{q}\sqrt{\frac{kT}{C_{pd} + C_{SH} + \zeta C_{fb}}\left[2\left(A_{cg}-1\right)^2\left(1+\beta\right) + \zeta\left\{1 + \frac{1}{A}\frac{\left(A_{cg}-1-\theta A_{cg}\right)^2}{A_{cg}-1+\theta A_{cg}}\right\}\right]} \tag{6.20}$$

Ignoring the bracketed term, the advantage is obvious. A large effective sampling capacitance is created by the combination of C_{pd}, C_{SH}, and the amplified C_{fb}. However, when referred to the small feedback capacitance, only a very small fraction of this noise remains. The improvement in noise, as compared to that in an ordinary active pixel using a source-follower, is strongly dependent on the ratio of C_{fb} to C_{pd}.

6.5 Simulation

The preceding pixel designs were simulated using a new transient noise analysis feature in Silvaco Smartspice [30]. As this capability is relatively new to SPICE, its performance was first verified on a simple circuit (Appendix A).

Transistors were modeled using BSIM3v3 models (HSPICE level 49) provided by Lincoln Laboratory's Advanced Silicon Technology Group. Though the target process is actually a fully depleted SOI process, the transient noise analysis is not specified to work properly with the SOI model. The bulk transistor models should be similar enough to provide some idea of noise reduction capability.

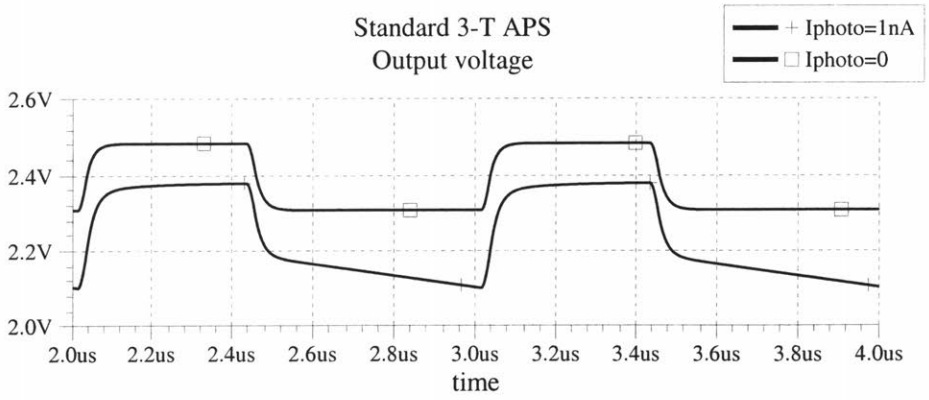


Figure 6-12: Output voltage of 3-T APS pixel. Without the photocurrent, the voltage at the output node stays flat during integration. With signal present, the voltage gradually decreases, except when periodically reset.

6.5.1 Standard APS Pixel

Initially, the standard three-transistor APS pixel was simulated, providing a benchmark by which to measure noise improvement. The circuit simulated is shown in Figure 6-1. In addition to the three transistors in the pixel, a 5 fF capacitor was used to model the photodiode, a current source transistor was used at the output of the pixel, and a 1 pF capacitor was added at the output. The 1 pF capacitor represents the column capacitance, and is very important for accurate simulation results; failure to include this capacitance results in noise from the signal chain dominating reset noise.

Figure 6-12 shows the simulated waveforms of this pixel with and without photocurrent. In the absence of light, the pixel resets to 2.47 V, falling to 2.29 V when the reset pulse falls. With light, simulated by a constant current of 1 nA from the sense node to ground, the pixel is reset to 2.37 V, falling to approximately 2.17 V before beginning its linear descent. Note that due to soft reset, the reset levels are not constant, and would increase with longer reset times, albeit at a logarithmic pace.

Figure 6-13 illustrates saturation in the pixel. If the photocurrent is too high for a given reset frequency, the voltage at the output node will reach a point where the pixel will become non-linear. The limiting factor may come anywhere in the signal chain; here it appears that the column load transistor has left the saturation region of

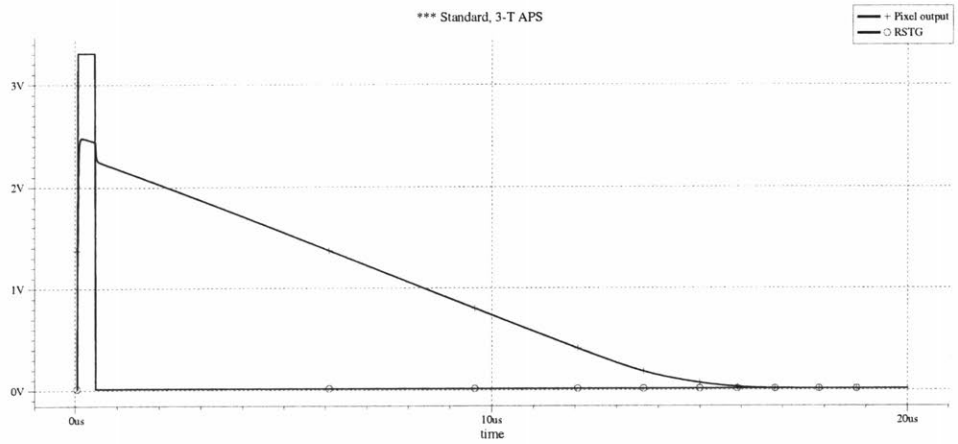


Figure 6-13: Output voltage of 3-T APS pixel without resetting. The voltage decreases due to a constant 1 nA photocurrent source. When the output reaches approximately 0.2 V, non-linearity becomes visibly apparent, with the pixel eventually saturating at 0 V.

operation. Non-linearity becomes noticeable at an output voltage of approximately 0.2 V.

Simulations show a total parasitic capacitance of 5.1 fF at the sense node. The soft reset noise equation, with the capacitance equal to 10.1 fF, gives a predicted sense node noise of 566 μV. The simulated noise at the output node is 561 μV, which can be referred back to the sense node (using the simulated source follower gain of 0.96 V/V) for an input noise of 585 μV, or 18.3 electrons. Given that the soft reset equation is an approximation [19], and tends to slightly underestimate noise (see Appendix A), these results seem to be in good agreement.

6.5.2 Active Reset Pixel

Operational Amplifier

In order to simulate the active reset pixel, the column op amp must first be designed. A folded cascode design was chosen. The key parameters of the op amp are readily observable in Equation 6.10. High DC gain is desirable, but only up to a certain point; for larger values of A_0, there will be less benefit in increasing it as other noise sources will begin to dominate. Equation 6.10 also shows that a high first-stage

transconductance is very important. As the purpose of the op amp is to reduce noise, the op amp must also be low noise. Low power consumption would be useful, as a 256×256 pixel array would have 256 op amps, but power consumption is a less critical parameter; compared to a CCD, an APS array with lots of op amps would still be low power.

Equation 6.10 can be used to produce an estimated value of g_{ma}. The photodiode capacitance C_{pd} is approximately 5 fF, column bus capacitance C_L is approximately 2 pF [25], and reset transistor transconductance g_{mr} is approximately 10 nA/V, with its value decreases as the reset transistor moves further subthreshold. These numbers indicate that in order to reduce the noise from the reset transistor to 1/15 of its original value, g_{ma} should be on the order of 150 μA/V.

The schematic of the folded cascode op amp is shown in Figure 6-14 [28]. M_1 and M_2 are the input transistors, with M_3 and M_4 serving as active loads and M_{11} as the current source for this stage. M_5 and M_6 are cascode transistors, with a wide-swing current mirror consisting of M_7–M_{10}. The remaining transistors are mirror transistors which only need to be included once for an array of op amps. The transistor sizes and biases are listed in Table 6.1. Important performance characteristics are listed in that table as well. The open loop frequency response is shown in Figure 6-15.

Active Reset Pixel Simulation

In order to achieve low-noise performance in the active reset pixel, the ramp waveform must be treated carefully. The rise of the ramp should not be too fast. More importantly, due to limitations in the output range of the op amp, the ramp should not rise too high, or the op amp gain will decrease and the noise will increase. Practically, this behavior sets a limit of about 2.3 V on the level of the reset gate of the photodiode, 1 V lower than in an ordinary soft-reset pixel. The result is that the pixel saturates under lower light conditions. Low saturation levels are irrelevant for x-ray detection, however (see Section 5.1.2). Note that this lower reset level is not inherent in the active reset architecture; rather, it is a deficiency in the op amp, and would be an area to address in future work. One way to address this problem might

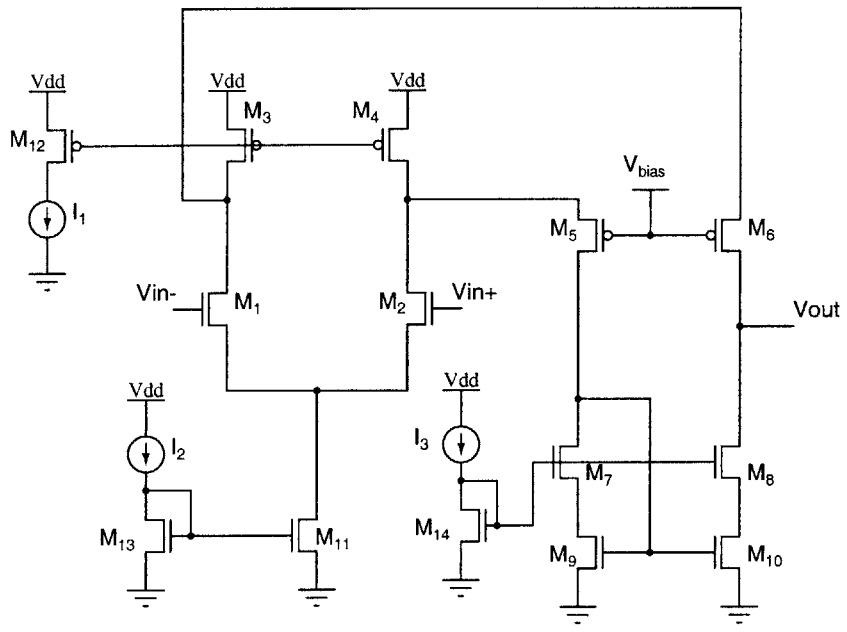


Figure 6-14: Schematic of folded cascode op amp used in active reset feedback circuit. With the exception of the output node, each node in the folded cascode op amp is low-impedance, allowing good high-frequency performance. Transistors M_{13}, M_{14}, and M_{15} are only included once per op amp array.

be adding a second stage, with only one transistor between the rail and the output, to the op amp. One example of such a gain stage is a common-source amplifier. Adding a second stage complicates the frequency response, making stability an issue. It also makes the initial analysis less exact, as it was assumed that the op amp had a single-pole response. Nevertheless, the added gain and output swing make this approach a worthwhile avenue to pursue.

Figure 6-16 shows the active reset pixel integrating with and without photocurrent. Integration begins at approximately 61 μs. The slope during integration, until 67 μs, is a measure of the incident light. Note the complicated waveform. The steep, curvy rise from 67 μs to 69 μs is due to the ramping up of the feedback signal. The pulse between 60 μs and 62 μs is the final pulsing of *INIT*. See Figure 6-3 for the full timing pattern.

Simulation, using feedback bus and column capacitances of 2 pF each, and a photodiode capacitance of 5 fF, yielded an output-referred noise of 383 μV. Using

Device	Width	Length
M_1	10 μm	0.5 μm
M_2	10 μm	0.5 μm
M_3	3 μm	0.5 μm
M_4	3 μm	0.5 μm
M_5	3 μm	0.5 μm
M_6	3 μm	0.5 μm
M_7	2 μm	0.5 μm
M_8	2 μm	0.5 μm
M_9	2 μm	0.5 μm
M_{10}	2 μm	0.5 μm
M_{11}	20 μm	0.5 μm
M_{12}	2 μm	0.5 μm
M_{13}	20 μm	0.5 μm
M_{14}	2 μm	0.5 μm

Source	Bias Level
I_1	50 μA
I_2	80 μA
I_3	30 μA
V_{bias}	2.0 V

Op amp Performance	
DC Gain (V_{out} = 1.5V)	134.5 V/V
Unity gain freq.	26.1 MHz
Phase Margin	89°
Power Dissipation	459 μW
Input referred noise	51 μV
First-stage g_m	423 μA/V

Table 6.1: Sizing of transistors, bias levels, and measured performance of folded cascode op amp.

the simulated source follower gain of 0.96 V/V, this voltage can be referred back to the input as 400 μV, or 12.5 electrons, a 32% improvement over the ordinary active pixel sensor. Efforts to confirm the accuracy of Equation 6.12 failed in that the final noise did not depend much on changing the feedback bus capacitance or reset transistor sizing (and with it the transconductance g_{mr}). This modelling failure is likely due to the $1/A_0$ term in Equation 6.12. As the op amp output begins to rise, its gain decreases sharply, resulting in the $1/A_0$ term dominating the reset noise. The assumption that $A_0 \gg 1$ is false here. An improved op amp could probably do better, as previously suggested.

6.5.3 Kleinfelder CDS Pixel

The Kleinfelder pixel was simulated using a single transistor current source at the output, along with a 1 pF column capacitance. Timing parameters are very important for proper simulation of the Kleinfelder pixel; long reset times, on the order of 100 μs, were used to ensure enough time for the noise to reach its final value. A long reset period is most important for resetting C_2. The large capacitance takes a long time to be fully reset, and an incomplete reset leaves the noise much higher than it could

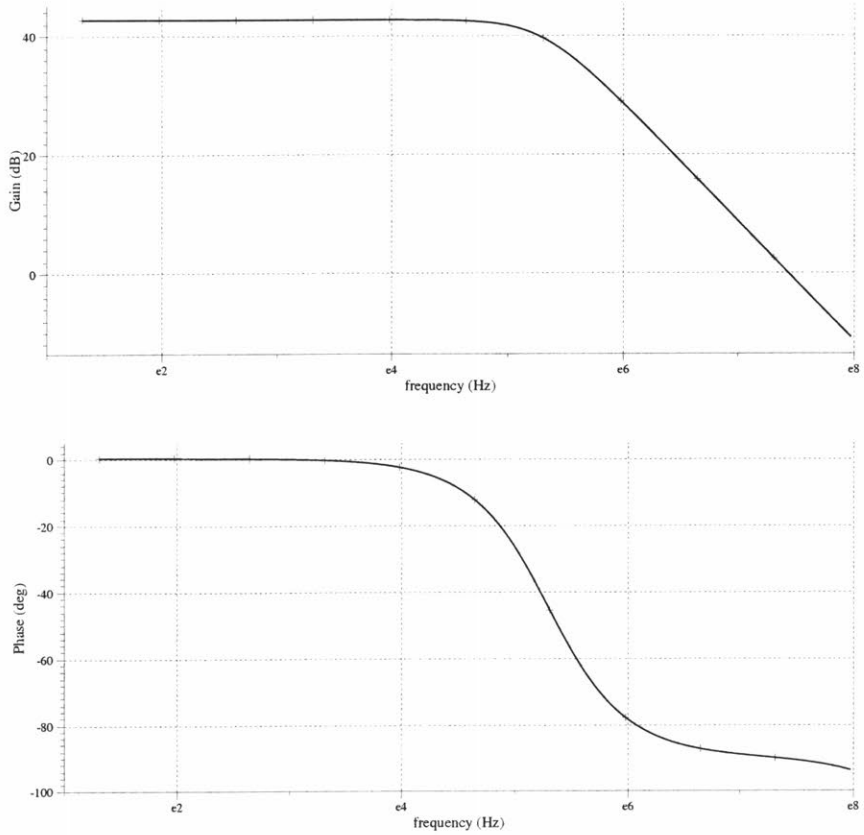


Figure 6-15: Open-loop frequency response of the op amp. The amplifier was loaded with a 2 pF capacitor. A common mode voltage of 1.5 V (approximately $V_{DD}/2$) was applied to the amplifier. The open loop gain of the op amp is 42.6 dB, or 134.5 V/V. The phase margin is 89°.

otherwise be.

Simulation showed quite a significant improvement in noise. Output noise was simulated, and referred to the input using the source follower gain of 0.96. Results are summarized in Table 6.2 and Figure 6-17.

The Kleinfelder pixel design can reduce noise from the 18.3 electrons found in the standard APS pixel down to 4.4 electrons. Results are in very good agreement with those predicted using Equation 6.14 for smaller values of C_2. As the capacitance gets larger, noise sources that had originally been ignored begin to become more important. A rough analysis shows that taking signal chain sources into account can very nearly make up the difference. The Kleinfelder pixel has four transistors

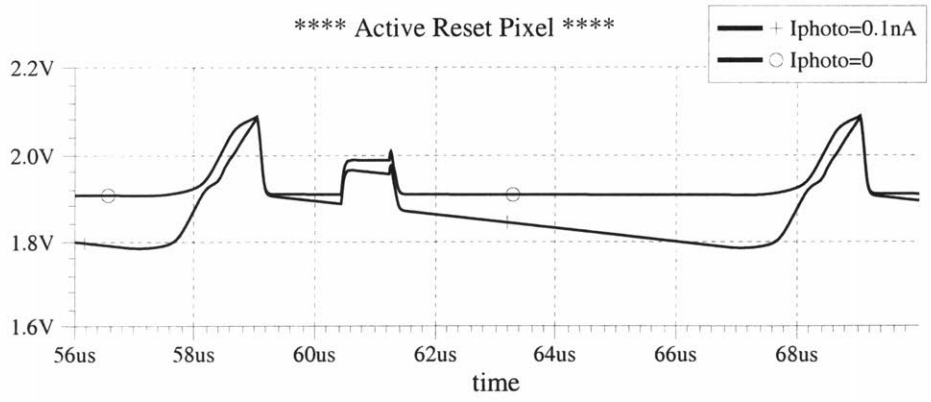


Figure 6-16: Active reset pixel integrating, with and without photocurrent.

operating in the saturation region; two source-followers and their load devices. A saturated mosfet loaded by a capacitance C has a noise given by

$$V_n^2 = \frac{2}{3}\frac{kT}{C}. \tag{6.21}$$

Each of the four saturated transistors has a load of approximately 1 pF. The combined noise of these four transistors, calculated using Equation 6.21, is 3.6 electrons. Adding this noise to the 2.25 electrons expected for a 1000 fF C_2 capacitor gives a noise level of 4.25 electrons, a disagreement of only 3% from the simulated value of 4.4 electrons.

Another noticeable facet of the Kleinfelder pixel simulations is operation in non-CDS mode. Kleinfelder states that the noise in non-CDS mode should be the same as in an ordinary APS pixel, regardless of the size of C_2. Simulations show that increasing the capacitance does reduce the noise in this mode. However, for capacitances smaller than 100 fF, the noise is actually higher than in the ordinary APS case. The extra noise is due to the different load seen by the first source follower. The first stage is not loaded by the column capacitance, but rather by the smaller C_2 capacitance. Above 200 fF, increasing the capacitance has very little effect, and the noise appears to level off at approximately 17.5 electrons. This value is very close to the noise in a standard APS pixel. The difference is due to the additional capacitance present in Kleinfelder's design.

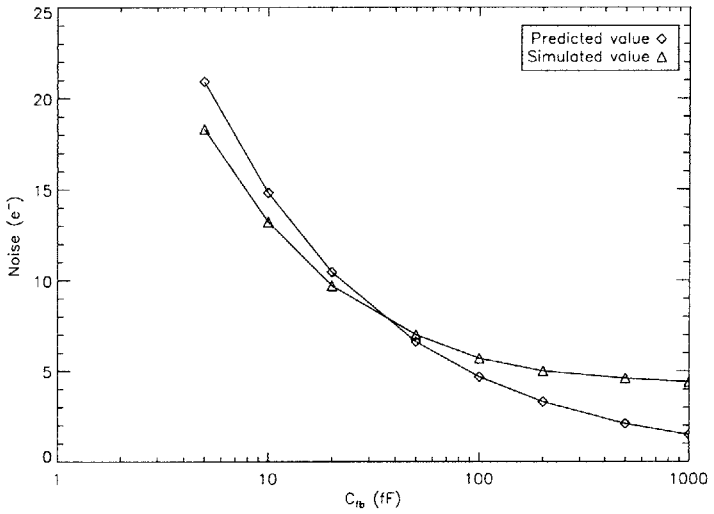


Figure 6-17: Results of noise simulation of Kleinfelder pixel. For small values of C_2, simulation agrees closely with the calculated value (using Equation 6.14). As the capacitance gets larger, simulations show less benefit from the noise reduction than predicted from Kleinfelder's equation. The excess noise is due to other noise sources in the circuit.

6.5.4 CTIA Pixel

The CTIA pixel shown in Figure 6-9 was simulated exactly as in the figure, with the addition of a 2 pF capacitance as an output load. The sizes of the transistors were as given by Fowler [26]: the reset and gain switches were 0.4μm/0.6μm, the row switch 2μm/0.4μm, the cascode NMOS and both PMOS transistors were 5μm/1μm, and the common source amplifier transistor 5μm/0.4μm. An initial goal of reducing noise by a factor of 10 compared to the standard APS meant an equivalent feedback capacitance of 0.5 fF, achieved by setting $C_f = C_1 = 15$ fF and $C_2 = 435$ fF.

Operation of the CTIA pixel was verified first in both high-gain and low-gain modes. Figure 6-18(a) shows the pixel output node, in high-gain mode, in response to three different photocurrents (the input is explicitly shown in Figure 6-18(b)). Note that unlike the previous pixels studied, the CTIA pixel has an increasing output for higher signals. The final output voltage scales linearly with the photocurrent. However, the shape of the waveform is cause for concern; instead of integrating continuously as in the source-follower pixels, the CTIA pixel appears to integrate until

C_2	Calculated noise (e^-) w/CDS	Simulated noise (e^-) w/CDS	Simulated noise (e^-) w/o CDS
5 fF	20.9	18.3	23.9
10 fF	14.8	13.2	22.4
20 fF	10.4	9.7	20.7
50 fF	6.61	7.0	19.0
100 fF	4.68	5.7	18.2
200 fF	3.30	5.0	17.8
500 fF	2.09	4.6	17.5
1000 fF	1.48	4.4	17.5

Table 6.2: Simulated noise for Kleinfelder pixel. The capacitance C_2 is increased, and the pixel is operated in both modes. The predicted noise only takes into account reset noise, using Equation 6.14. Adding noise from the signal chain makes up the difference.

a steady state is reached. This steady state is dependent on the incident light level. Indeed, Figure 6-18(c) confirms that the output voltage of the CTIA pixel responds only to steady light levels, instead of integrating continuously as desired. In Figure 6-18(c), the photocurrent is briefly pulsed to a higher level (the input current is shown in Figure 6-18(d)). The output voltage jumps before quickly returning to its original level.

The CTIA pixel is behaving as a lossy integrator; the capacitor charge is leaking away and the pixel behaves more as if it had resistive feedback than capacitive feedback. A reset leakage current of approximately 1 pA seems to be responsible for this behavior. The inability to properly store charge makes the CTIA pixel unsuitable for use in x-ray astronomy, which relies on seeing only a single particle during an integration cycle. Clearly, the charge generated from an x-ray would quickly be lost due to leakage.

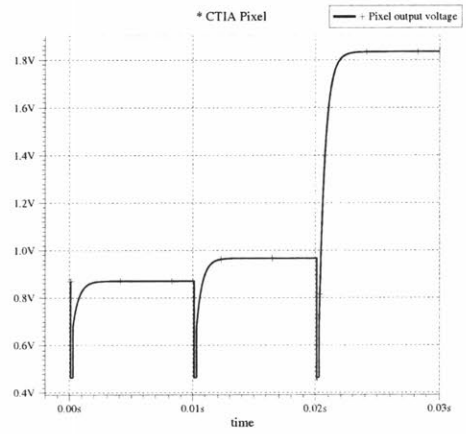
Despite its apparent unsuitability for x-ray detection, the CTIA pixel is still worth exploring. Figure 6-19(a) shows the pixel response for four different photocurrents over a very short time scale, before the pixel can reach steady state. The output voltage is linearly dependent on the photocurrent. Additionally, dividing the photocurrent by the slope gives the input capacitance, 0.5 fF, as predicted from Equation 6.17. Operating in low-gain mode should indicate an input capacitance of $C_f = 15$ fF;

Figure 6-19(b) shows this result.

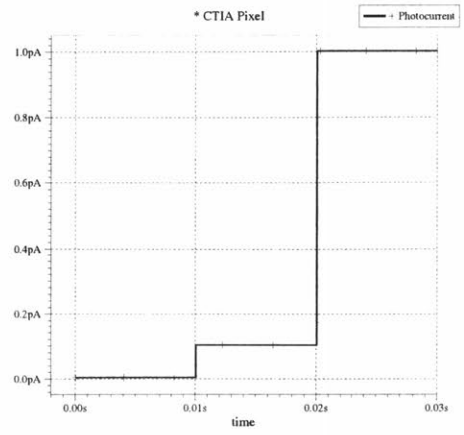
The reset noise in the CTIA pixel should be approximately $\sqrt{kTC_{eq}}$ where C_{eq} is 0.5 fF in high-gain mode and 15 fF in low gain mode. In high-gain mode, the noise at the output of the pixel is measured as 3.31 mV. Referred to the input capacitance of 0.5 fF, the equivalent noise in electrons is 10.4 electrons. The expected value using the kTC approximation is 9.0 electrons. Low-gain mode gives an output noise of 612 μV. Referred to the 15 fF capacitance, this voltage becomes 57.2 electrons. The kTC approximation gives a noise level of 49.2 electrons. Differences between simulation and theory are due to the use of the kTC approximation instead of Equation 6.20.

6.5.5 Simulation Summary

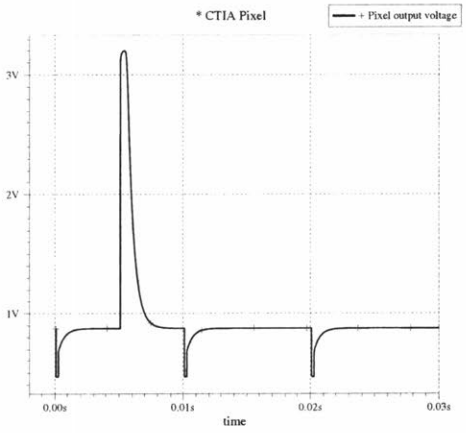
Simulations have confirmed the basic operation of active reset, pixel-level CDS, and CTIA pixel designs. Although noise in the CTIA pixel was reduced to an amount in agreement with basic theory, the pixel operation itself was not good enough for long exposures due to leaky reset transistors. The active reset pixel, while potentially very useful, suffers from an op amp that cannot maintain high gain at high output voltages. The Kleinfelder pixel shows noise reduction in agreement with theory, and, most importantly, is able to achieve very low noise with correct pixel operation. Lincoln Laboratory's Advanced Silicon Technology Group has designed the second-generation imager, APS-2, using the Kleinfelder CDS pixel; these results indicate a good choice on their part. With some more research, the active reset pixel may rival the Kleinfelder pixel in terms of noise performance, and with improved devices the CTIA pixel could be extremely useful.



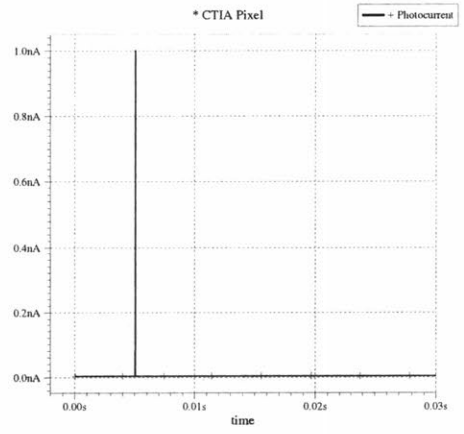
(a) Response due to steady currents



(b) Steady Currents (input to (a))

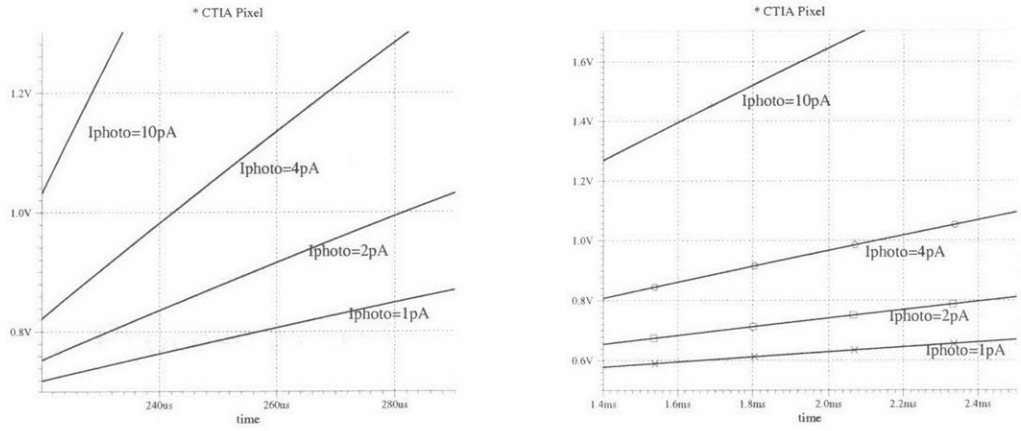


(c) Response due to current pulse



(d) Current pulse (input to (c))

Figure 6-18: Response of CTIA pixel to various inputs. (a) The pixel is exposed initially to no photocurrent, followed by periods of 0.1 pA and 1.0 pA (as seen in (b)). The final levels of the pixel in each of these periods is linear with photocurrent. (c) The response of the pixel to a very narrow pulse of photocurrent (as seen in (d)). Initially, the output jumps up in response to the signal, but due to leakage in the reset transistor this charge is quickly leaked away. This leakiness makes the CTIA pixel unsuitable for x-ray detection.



(a) High gain

(b) Low gain

Figure 6-19: The CTIA pixel operating under shorter time scales. (a) The output of the CTIA pixel in high-gain mode for four different photocurrents. Dividing the applied photocurrent by the slope gives the equivalent input capacitance, which is 0.5 fF here, as predicted. (b) Operation in low-gain mode; here the equivalent capacitance is found to be 15 fF.

Chapter 7

The Future: APS-2

Lincoln Laboratory's Advanced Silicon Technology Group has designed a second generation x-ray active pixel sensor. This device, known as APS-2, is described in this chapter.

7.1 Process overview

APS-2 will be fabricated using a stacked, 3-D process [16, 17]. Two wafers are fabricated independently and later bonded together electrically and mechanically. For APS-2, the bottom tier consists entirely of photodiodes. The photodiodes are formed from p^+ regions on a high-resistivity n-substrate. The upper tier will be manufactured using Lincoln Laboratory's 3.3V FDSOI process and will contain the readout circuitry.

7.2 Imager design

APS-2 is a 256×256 pixel array, with a pixel pitch of 24 μm. The pixels are larger than those in APS-1 to accommodate a large capacitor in each pixel. The APS-2 pixel is a variation of the Kleinfelder CDS design. Figure 7-1 is a schematic of the APS-2 pixel design. The primary difference between the APS-2 pixel and Kleinfelder's design is that the reset transistors in APS-2 are p-type devices. APS-2 thus operates in hard

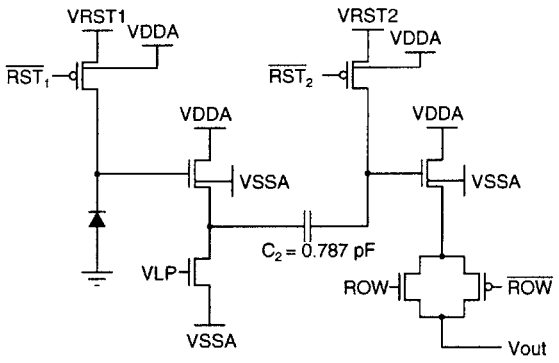


Figure 7-1: APS-2 pixel. The pixel design is based on the Kleinfelder CDS pixel. The reset transistors, however, are p-type devices, allowing lag-free reset. The 787 fF capacitor should allow noise to be reduced tenfold compared to the APS-1 pixel.

reset, improving linearity at the expense of a slight increase in noise. APS-2 should still offer greatly improved noise performance compared to APS-1 due to its CDS capability. Each pixel contains a 787 fF capacitor. Ideally, this capacitor should reduce noise by more than a factor of ten, assuming an equivalent photodiode capacitance of 5 fF.

7.2.1 Layout

Figure 7-2 is a CAD layout view of the APS-2 pixel. The CDS capacitor, C_2, consists of the four large rectangles, occupying most of the pixel space. The resulting fill factor is small when front-illuminated. APS-2 will be back-illuminated, however, giving it nearly 100% fill factor.

The reset and source follower transistors use H-gate layouts. The H-gate transistors, like the annular-gate devices on APS-1, do not suffer from parasitic edge leakage effects. Additionally, H-gate devices allow two sets of body contacts, one on either side of the H. Body contacts are used to further suppress the floating-body effects created by the parasitic BJT inherent in all SOI FETs. Multiple sets of contacts are beneficial, as the resistivity of the substrate can limit the effectiveness of a single body contact [15]. H-gate transistors occupy more area than straight-gate devices. However, the transistor area in each pixel is still much smaller than the capacitor area.

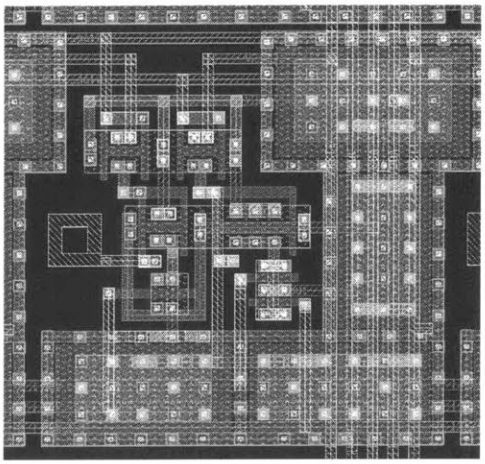


Figure 7-2: APS-2 pixel layout. The four large rectangles make up the CDS capacitor C_2. The reset and source follower transistors use H-gates, while the current source and row-select switches use straight gates.

7.3 Simulation

APS-2 was simulated using the same bulk models used in Section 6.5.

Simulations suggest p-type transistors are leakier than n-type. Simply having zero gate-source voltage does not turn the transistor off enough to allow proper integration. It is possible that the edgeless H-gate designs solve this problem; SPICE does not have an easy way to account for gate shapes. Lowering the reset drain voltage allowed the simulation of the APS-2 pixel operating correctly. All simulations were done with the reset drain at 2.5 V, with the reset gate off voltage at 3.3 V. A 1 pF column capacitor was added to represent bus capacitance.

Basic operation

Despite the negative value of V_{SG} used, simulations still showed the capacitive sense node being pulled up, without any photocurrent present, with a slope of 42 volts per second. This offset resulted in non-linear behavior when applying photocurrents of 100, 200, 500, and 1000 fA (Figure 7-3). Subtracting the offset, however, corrected for this deficiency, allowing linear operation of the APS-2 pixel (see Table 7.1). The gain, measured as output slope divided by input current, varies by 0.6% as photocurrent

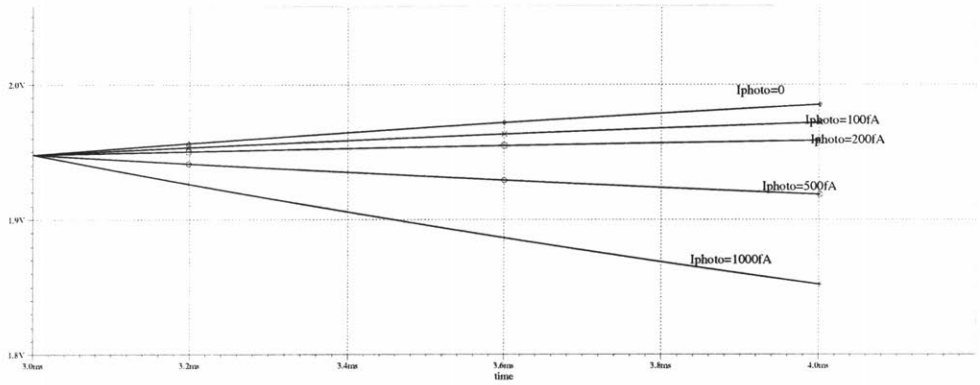


Figure 7-3: Response of APS-2 pixel to steady photocurrents. Applied current varies from 0 to 1000 fA. Comparing the slopes to the photocurrents results in non-linear gain, unless the zero-photocurrent slope is subtracted from every other slope.

Photocurrent (fA)	Slope (V/sec)	Corrected slope (V/sec)	Gain (V/sec / fA)
0	43.1	0	n/A
100	27.6	−15.5	0.155
200	12.2	−30.9	0.155
500	−34.1	−77.2	0.154
1000	−111	−154	0.154

Table 7.1: Measured gain of APS-2. Although a positive output slope is seen for zero photocurrent, this slope can be subtracted to yield linear behavior, for a gain that varies by 0.6% as photocurrent varies by a factor of ten. These gain measurements indicate an input capacitance of 6.5 fF.

varies by a factor of ten. The gain measurements indicate an input capacitance of 6.5 fF.

Noise

The output-referred noise of the APS-2 pixel is measured to be 98.9 μ V, corresponding to an input-referred noise of 4.2 electrons. In comparison, the best CCDs today have approximately 2.5 electrons of noise.

At noise levels this low, signal chain noise becomes very important. As shown in Chapter 6, signal chain noise is low due to the large column capacitance. This fact suggests that increasing column capacitance can lower the noise. Simulations confirm this; increasing the column bus capacitance to 2 pF reduces output-referred noise to 70.1 μ V, or 3.0 electrons.

7.4 Conclusions

APS-2 will deliver low noise performance, almost comparable to a CCD. The actual noise level achieved depends on column capacitance; adding more would improve performance at the expense of increased chip area. APS-2 should benefit from the H-gate designs and perform better in silicon than it does in simulation, potentially as well as a CCD, but with all the benefits of APS that have been discussed. With some work, APS imagers will prove to be a useful technology for scientific imaging.

Chapter 8

Conclusions and Future Work

This thesis has presented a test system designed to operate a new active pixel sensor imager. The imager was tested using this system, and proved capable of detecting x-rays. Because of high noise levels in the imager, noise-reduction schemes have been explored in simulation.

8.1 APS-1 Testing

Contrary to initial expectations, several of the pixels on APS-1 were able to detect x-rays at room temperature. This achievement is a simple demonstration of one advantage that APS devices have over CCDs. True measurements of energy resolution and responsivity were not possible using the data collected, however, due to soft reset operation.

Similarly, dark current and noise were measured for various pixel types. These measurements also suffered from soft reset, as well as the A/D capture problem described earlier. Initial characterization of the pixel types was done, but without more x-ray data the meaning of the dark current data is difficult to determine.

There are still much to explore with APS-1.

- All data collected to this point has been from soft reset. Hard reset will allow more complete measurements, despite higher noise levels.

- A responsivity map should be made since the gain of each pixel is different. This measurements requires improved x-ray analysis. A new event finder, specifically tailored to APS-1, should be written.

- Increased noise at low temperatures is an unusual phenomenon, but it is one that APS-1 exhibits. This behavior should be investigated more experimentally and theoretically.

- The photodetector reverse-bias voltage has been fixed at ground. Increasing this reverse bias should increase the depletion width and improve detection efficiency. A simple modification to the test system is required to control this voltage.

- Only nine of the sixteen pixel types have been tested. The photogates have not been tested at all, and they are expected to have lower noise than the photodiodes. Pixels with the SCP implant appear to be completely non-functional, but it is possible that increasing the reverse bias on these photodiodes will allow these pixels to work.

- All testing has been done with delta-difference sampling. When reading a single pixel (as done in x-ray detection), a single row, or photogates, it is possible to use correlated double sampling, allowing much lower noise.

- Only a single packaged device has been tested. All measurements need to be repeated across different parts, from different wafers. The current setup requires significant user interaction. To effectively characterize many chips, improved data collection scripts are needed.

8.2 Pixel Designs

Several advanced pixel designs were explored in detail. Active reset and in-pixel CDS showed reduced noise in simulation. There is plenty of room for further design work.

- Active reset should be easily improved by using a better op amp. Lincoln Laboratory is interested in building an active reset imager; a full design would be a worthwhile undertaking.
- The CTIA imager is too leaky in simulation; such an imager would not be useful for x-rays. A better design might fix this problem, enabling extremely low noise operation with relatively small gain variations.
- Many other pixel designs have been presented in the literature. More recent and more thorough literature searches could yield more design ideas.

8.3 Summary

The primary goal of this project, to detect x-rays with an active pixel sensor, was accomplished, despite an imperfect sensor and imperfect setup. A low-noise electronics system is available for testing future devices. However, there is still plenty of work to be done, both in testing and in design.

Appendix A

Transient Noise Analysis Tool Verification

All simulations were performed using Silvaco Smartspice [30]. Smartspice possesses a transient noise analysis capability, allowing the simulation of noise under varying bias conditions. As this type of analysis is a new addition to CAD tools, correct operation of the tool was verified using a simple example of time-varying noise. Ordinary linear/AC noise analysis would predict noise of kT/C for both hard and soft reset. It has been shown that under soft reset, due to the changing gate-source voltage of the reset transistor, noise is actually closer to $kT/2C$ [19]. To verify the transient noise analysis, the standard active pixel (see Figure A-1) was simulated with drain voltages of both 3.3 volts and 1 volt, corresponding to soft and hard reset respectively.

The simulation results are shown in Figure A-2. As expected, noise under hard reset is approximately twice the noise under soft reset. Specifically, hard reset gives a total noise of 64.3 μV, while soft reset gives a noise of 51.3 μV. These compare favorably with the theoretical values of 64.3 μV and 45.5 μV given by kT/C and $kT/2C$ respectively. Remembering that $kT/2C$ is merely an approximation, these results are verify the correct operation of the transient noise analysis.

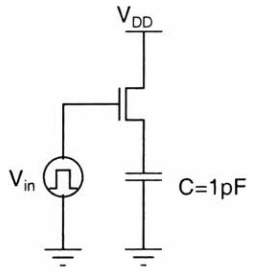


Figure A-1: Model of photodiode pixel used to verify transient noise analysis tool. The gate voltage is pulsed from 0 to 3.3 V, and the drain voltage is either 3.3 or 1 volt, corresponding to soft and hard reset respectively. The capacitor models the photodiode that would normally be present in an APS pixel.

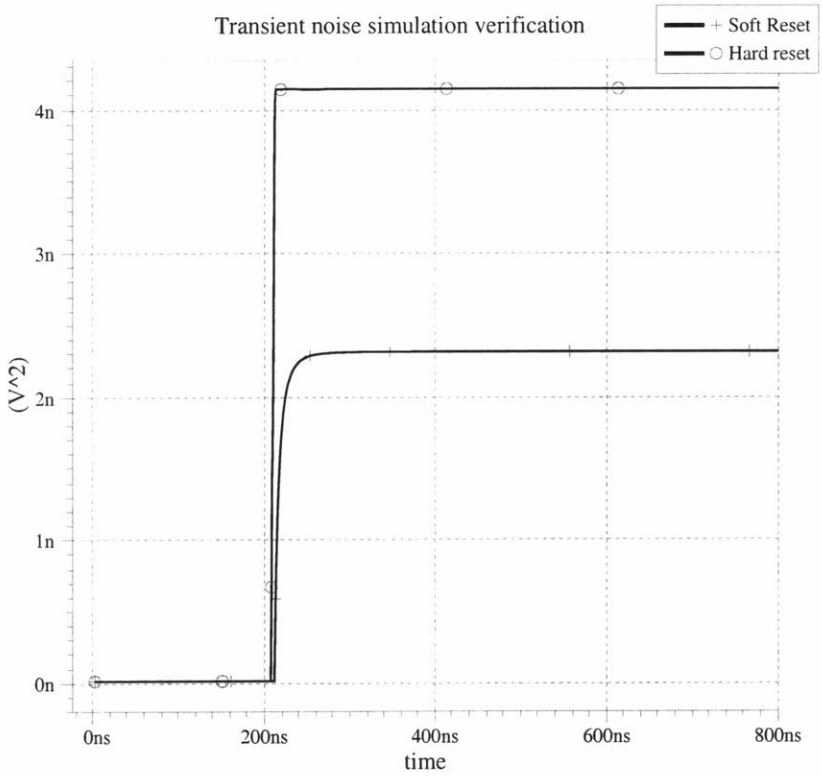


Figure A-2: Results of transient noise analysis performed on the circuit in Figure A-1. At t=0.2μs, the voltage on the transistor gate has gone high, resetting the photodiode. Noise under hard reset is approximately twice the noise under soft reset, and both compare well with the expected values of kT/C and $kT/2C$.

Appendix B

APS Users Guide

This section contains step-by-step guides of how to take certain measurements from APS-1 and analyze the data. A full reference on each timing file, shell script, idl procedure, and hardware is located in Appendix C. All commands listed, unless specified otherwise, should be run from the `mpuwrite` window. In any generated fits files, only quadrant B is relevant; APS-1 only provides a single output node, which is connected to the input of video chain B. Due to some coupling between chains B and D, however, under certain circumstances there may appear to be data in quadrant B; this is not the case.

B.1 Typical Current Draw

The table below lists typical current levels supplied by each of the power supplies. If more is being drawn, something might have been damaged.

-5 V	77 mA
+24 V	72 mA
-12 V	36 mA
+40 V (Bus)	0 mA
+5 V	310 mA
VDDPG	80 mA
VDDD	27 mA

B.2 Starting EGSE

Each of these examples assumes that the EGSE is already active, i.e. the `startEgse` command has been issued and the appropriate programs have been run. The following steps illustrate how to do this.*

1. Certain environment variables must be set, typically by including these lines in the `.cshrc` file (note the difference in `XISMITEGSE` from CCD use):

   - `setenv XISMITEGSE /nfs/min/s1/aps/`
   - `setenv DSP_STREAM /usr/local/dsp/dsp_stream`

2. To start the EGSE, at the prompt type `$XISMITEGSE/bin/startEgse` (or, if `$XISMITEGSE/bin` is in your `$PATH`, just type `startEgse`.

3. The startEgse command creates four windows, the `mpuwrite` window, the `nova2fits` window, the `ppu_read` window, and the `captureLog` window. When each is created, you will have to hit return in it to run the commands mentioned. They should be hit in the following order: captureLog (it will say, `DSP not running, waiting...`), mpuwrite (the captureLog window will now say, `ready`), nova2fits and finally ppu_read. `nova2fits` accepts as a parameter the name of the fits file in which to store captured data. Part of the filename is typically a format specifier such as `%02d` or `%04d` which yield an incrementing 2 or 4 digit number, respectively. `nova2fits` will not run unless there is a file named `fits` in the `testdir` directory. This file contains all of the fits headers that will be used in the generated fits files.

4. When the system is running, you can issue commands in the mpuwrite window. Commands are issued through the `mpu` command and the `mpuf` command. The first takes whatever commands are it's arguments and sends them to the electronics. The second takes a filename argument and sends the contents thereof to the electronics.

*Portions of this section are taken from Michael Vezie's document "Software Control of the EGSE", and are repeated here for convenience.

5. When the system is configured, then you are ready to take data. Make sure that `ppu_read` and `nova2fits` are running. Then either send one or many `S_WRITE_START` commands.

B.3 Turning System Off

The following steps illustrate how to properly power-down an APS device and how to turn off the EGSE.

1. The sequencer should first be stopped. This is done by issuing the command `mpu S_WRITE_STOP`.

2. DACs must now be turned off. This is accomplished easily with the command `mpuf aps_clear_dacs.com`.

3. The last two power supplies must be turned off. These are VDDD and VDDPG, controlled by external power supplies. These supplies may be turned off by simply turning the voltage knob down to 0. It is probably safe to use the power button on the supply to turn the supply off, but this has never been tested. Notice that turning the VDDPG supply all the way down will not bring it to 0 V, but rather closer to 2 V.

4. Open the handle on the socket and remove the device. When the chip is removed, the power on VDDPG will turn down to 0 V. Upon reinsertion, the voltage immediately jumps back up to 2 V. This is an unknown problem, something within the XIS system, as it is only fixed by powering down the XIS box and then turning it back on again. If the user wishes to insert another device, cycling the power is recommended. There is no need to rerun `startEgse` in this case.

5. If the user wishes to shut down the system, he should type `killEgse` at the prompt. The user should `CTRL-C` and exit out of any windows that are still running.

B.4 Dummy Load

The following steps illustrate how to operate the dummy load.

1. With system turned off, remove Analog Cable 1 from J5 on the XIS box and Digital Cable 1 from J3 on the address-latch board.

2. Place dummy load 37-pin solder cup connector on J5 of XIS AE. See Figure B-1

3. Connect dummy load signal wire from J3-18 on address latch board to **F** location on video add-on board (see Figure B-2).

4. Turn on power strip controlling electronics.

5. Type `mpuf powerup.com` to reset the electronics, clear DACs, etc.

6. Type `mpuf dummy.com` to capture a frame of data.

7. For repeated frames type `mpu S_WRITE_START`.

8. The file may be examined in vista or any other program that can analyze fits files. The top half of the B quadrant was sampled with an 8 mV signal applied to the video board. The precise voltage applied may be measured on the 10Ω dummy resistors. The bottom half of the B quadrant was sampled without such a signal present. Again, the precise voltage applied (which, due to component mismatch, will not be 0) may be measured on the 10Ω dummy resistors. By knowing the change in applied voltage during the two halves and the change in A/D readings, it is possible to determine the gain of the video chain. For example, if an 8 mV difference causes the video reading to change by 1600 ADU, the gain is 5 μV/ADU. Using the estimated photodetector gain of 5μV/e^- the gain can be determined as 1 ADU/e^-. Dummy load operation is be done in the high-precision video mode. Therefore, the low-precision video mode, in which all other operations are done, 1 ADU = 4 electrons.

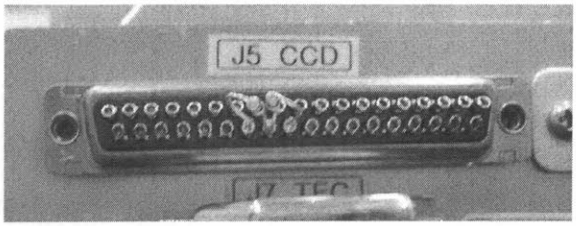
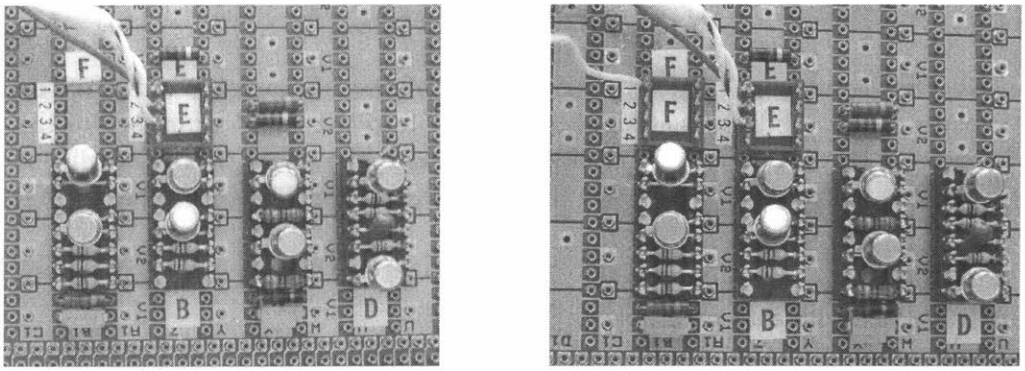


Figure B-1: Solder cup connector with 10 Ω resistors from video inputs to ground. This is one of the components of the dummy load, and fits over J5 on the XIS AE.



(a) Video add-on board without dummy load

(b) Video add-on board with dummy load

Figure B-2: Video add-on board with and without dummy load. The dummy load connects a 4 kΩ resistor from CB on the address latch board to the input of Vsig. When CB is high, an additional signal is created on the video board, which can be measured as a change in video output.

9. If data is out of range, adjust the video board potentiometer (Figure B-3) and try again.

B.5 Single pixel scoping

The following steps illustrate how to observe the output of a single pixel on the oscilloscope.

1. All cables should be connected between the probe card and the electronics box. Turn power strip on.

2. Type `mpuf powerup.com` to reset the electronics, clear DACs, etc.

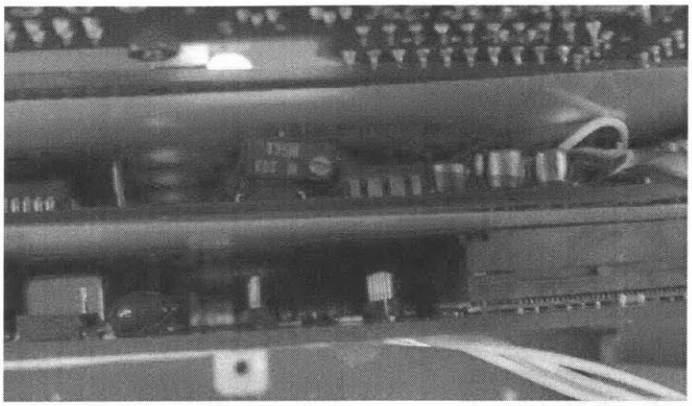


Figure B-3: Overhead view of video board potentiometer (blue object in center). The potentiometer allows the introduction of ±2V offset into the video signal before the A/D converter. Turning the screw clockwise decreases the value, which turning it counterclockwise increases it. Three full turns causes a change of approximately 400 ADU.

3. Insert APS device into probe card. Close handle.

4. Turn the power supplies for both VDDD and VDDPG up to 3.3 V. They should be supplying 27 mA and 80 mA respectively.

5. Type `mpuf aps_test??.com` where `??` is the number of the pixel type to test, ranging from 01–16, e.g. `mpuf aps_test02.com` to choose a pixel of type PD2.

6. Type `mpuf aps_hk_dacs.com` to obtain housekeeping data on all the DACs. These may be examined to ensure correct power-up.

7. Type `mpu S_WRITE_START` to capture a frame of data.

8. Type `mpu S_WRITE_START` to begin operation.

9. Connect the oscilloscope to Vsig or Vref on the video add-on board. This is most conveniently accomplished at the resistors R11 or R12 (see Figure B-4). The waveform seen shows the reset pulse and allows time before another reset to integrate.

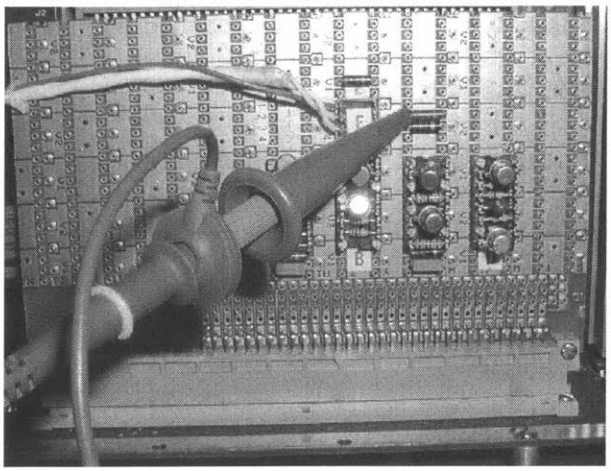


Figure B-4: The scope probe is shown on the video add-on board. R11 is being probed, so that the waveform seen is V_{REF}.

B.6 Single pixel digital readout

The following steps illustrate how to read out a single pixel repeatedly using the video board. Every piece of data sampled refers to the same pixel. This method was used to initially look for x-rays.

1. All cables should be connected between the probe card and the electronics box. Turn power strip on.

2. Type `mpuf powerup.com` to reset the electronics, clear DACs, etc.

3. Insert APS device into probe card. Close handle.

4. Turn the power supplies for both VDDD and VDDPG up to 3.3 V. They should be supplying 27 mA and 80 mA respectively.

5. To determine which pixel will be tested, examine `aps_set_single.sdoc`. Near the beginning of the timing pattern, the address is set. See sequencer documentation for more info, or see Figure B-5 for an example. To choose a pixel from a different subarray, the following steps may be done.

   (a) Type `set_single.tcsh ?` where `?` is the pixel type to choose and may range from 1–16, e.g. `set_single.tcsh 2` will choose a pixel of type PD2.

Alternately, `aps_set_single.sdoc` may be modified manually.

(b) Type `proc_sdoc aps_set_single.sdoc`

(c) Type `proc_seqseg aps_set_single.seqseg`

(d) Type `sram_load single.sym`

(e) Type `pram_compiler pdsingle.pram single.symx`

6. Type `mpuf pdsingle.com`

7. Type `mpuf aps_hk_dacs.com` to obtain housekeeping data on all the DACs. These may be examined to ensure correct power-up.

8. Type `mpu S_WRITE_START` to capture a frame of data.

9. If data is out of range, adjust the video board potentiometer (Figure B-3) and try again.

B.7 Subarray digital readout

The following steps illustrate how to repeatedly read out and analyze a subarray of pixels.

1. All cables should be connected between the probe card and the electronics box. Turn power strip on.

2. Type `mpuf powerup.com` to reset the electronics, clear DACs, etc.

3. Insert APS device into probe card. Close handle.

4. Turn the power supplies for both VDDD and VDDPG up to 3.3 V. They should be supplying 27 mA and 80 mA respectively.

5. To determine what the initial pixel (top left) for the subarray will be, examine `sub_init.sdoc`. Near the beginning of the timing pattern, the address is set. See sequencer documentation for more info, or see Figure B-5 for an example.

```
FileName:    sub_init

Desc:        Sets the APS row and column addresses to address a single pixel
             Sets that pixel as the quickload row and column addresses.
             Row = 64 + 4
             column = 128 + 64 + 4
             Pixel = PD8


Rev       Date      Who   Change
***     ********    ***   ******
A       03/08/05    MLC   Initial Release
B       06/22/05    MLC   Start address modified by set_subarray.tcsh


time:                     00000000001111111111222222222233333333334444444
                          01234567890123456789012345678901234567890123456

b0   MODE       Digital   --------........................................
b1   Cop0/RC~   Digital   .....---........................................
b2   Cop1/Load  Digital   ..-...-.....-...................................
b3   ~VINT-     Video     ------------------------------------------------
b4   ~VINT+     Video     ------------------------------------------------
b5   ~VTRACK    Video     ------------------------------------------------
b6   VRST       Video     ------------------------------------------------
b7   Cop2/A0    Digital   ................................................
b8   Rop0/A1    Digital   ................................................
b9   Rop1/A2    Digital   .-------....-...................................
b10  Rop2/A3    Digital   ................................................
b11  SHS/A4     Digital   ................................................
b12  SHR/A5     Digital   ................................................
b13  RST/A6     Digital   .---.---........................................
b14  PG/A7      Digital   .---............................................
b15  CB/unused  Digital   ................................................
```

Figure B-5: Sample SRAM input for setting an initial address. The example here is used to initialize subarrays, but the file to initialize single pixels is very similar. From time 00 to 07 the address board is in mode 1, allowing addresses to be set directly. From 00 to 04, the low value of B1 means that the column address is selected. At time 02, the load signal on B2 is asserted, latching the value given by bits 14–7; in this case, the column is set to 128+64+4=196. Similarly, at time 06 the row address (64+4=68) is latched. The pixel is selected is in the PD4 subarray. At time 12, both RowOp and ColOp are set to 010_b, storing the current addresses as row and column quick-load addresses. These addresses may be recalled at any time, typically at the end of a row in a subarray readout.

To choose a subarray from a different pixel type, the following steps may be done.

(a) Type `set_subarray.tcsh ?` where ? is the pixel type to choose and may range from 1–16, e.g. `set_subarray.tcsh 2` will choose a pixel of type PD2. Alternately, `sub_init.sdoc` may be modified manually.

(b) Type `proc_sdoc sub_init.sdoc`

(c) Type `proc_seqseg sub_init.seqseg`

(d) Type `sram_load subarray.sym`

(e) Type `pram_compiler subarray?x?.pram subarray.symx`

6. Type `mpuf subarray?x?.com`, e.g. to do an 8x8 subarray readout type `mpuf subarray8x8.com`. Versions currently exist that allow readouts of 4x4, 8x4, 8x8, 8x16, 16x16, 32x16, 32x32, 64x32, and 64x64.

7. Type `mpuf aps_hk_dacs.com` to obtain housekeeping data on all the DACs. These may be examined to ensure correct power-up.

8. Type `mpu S_WRITE_START` to capture a frame of data.

9. If data is out of range, adjust the video board potentiometer (Figure B-3) and try again.

10. The fits file generated by nova2fits will need to be rearranged in order to be understood. This may be accomplished using the IDL `repack?x?` routines. For example, `er = repack8x8('filename.fits')` will analyze the 8x8 subarray data found in `filename.fits`. Since the subarray is read out many times, the repack routine will rearrange the pixels into many 8x8 matrices and write each of these to a separate fits file. The mean, min, max, and standard deviations of each pixel will also be written to separate fits files.

B.8 Single pixel signal current analysis

The following steps illustrate how to take photocurrent data on a single pixel. Integration times are varied from 25 μs to 100 μs in steps of 25 μs. This was originally intended to measure dark current; therefore, the names of many of the files involved contain the word 'dark'. However, this same procedure can be used to measure any signal current, as long as the pixel in question does not saturate in 100 μs.

1. All cables should be connected between the probe card and the electronics box. Turn power strip on.

2. Type `mpuf powerup.com` to reset the electronics, clear DACs, etc.

3. Insert APS device into probe card. Close handle.

4. Turn the power supplies for both VDDD and VDDPG up to 3.3 V. They should be supplying 27 mA and 80 mA respectively.

5. To determine which pixel will be tested, examine `aps_set_single.sdoc`. Near the beginning of the timing pattern, the address is set. See sequencer documentation for more info, or see Figure B-5 for an example. To choose a pixel from a different subarray, the following steps may be done.

   (a) Type `set_single.tcsh ?` where ? is the pixel type to choose, e.g. `set_single.tcsh 2` will choose a pixel of type PD2. Alternately, `aps_set_single.sdoc` may be modified manually.

   (b) Type `make_pdwait8.tcsh` to recompile all of the relevant files.

6. Type `mpuf pdwait8.com`

7. Type `mpuf aps_hk_dacs.com` to obtain housekeeping data on all the DACs. These may be examined to ensure correct power-up.

8. Type `mpu S_WRITE_START` to capture a frame of data. Typically, the first frame of data taken after loading new SRAM/PRAM data is not uniform, so a second should be taken for analysis.

9. If data is out of range, adjust the video board potentiometer (Figure B-3) and try again.

10. In IDL, type `stats = single_dark('filename.fits')` to analyze `filename.fits`. This will create separate 8 fits files, each consisting of pixels with a single integration time. Various summary statistics will be reported and returned.

B.9 Multiple pixel photocurrent analysis—short integration times

The following steps illustrate how to take photocurrent data on 256 pixels. Integration times are varied from 25 μs to 100 μs in steps of 25 μs. This was originally intended to measure dark current; therefore, the names of many of the files involved contain the word 'dark'. However, this same procedure can be used to measure any photocurrent, as long as the pixel in question does not saturate in 100 μs. This is effective for PD1, PD2, PD5, and PD6. PD4 and PD8 tend to have dark current values too low to be effectively measured in this way.

1. All cables should be connected between the probe card and the electronics box. Turn power strip on.

2. Type `mpuf powerup.com` to reset the electronics, clear DACs, etc.

3. Insert APS device into probe card. Close handle.

4. Turn the power supplies for both VDDD and VDDPG up to 3.3 V. They should be supplying 27 mA and 80 mA respectively.

5. Type `set_and_run_single.tcsh 2` to obtain data on 256 pixels of type PD2. Similarly, a different number in the range of 1–16 may be substituted in place of 2 to obtain data on a different pixel type. The initial pixel may be determined by examining `aps_set_single.sdoc`. If a different pixel is desired, it can be chosen before running `set_and_run_single.tcsh`. The script will collect three frames of data. Typically, the first frame of data is not uniform, so a second and third are taken for analysis.

6. If data is out of range, adjust the video board potentiometer (Figure B-3) and try again.

7. In IDL, type `stats = single_dark_256('filename.fits')` to analyze `filename.fits`. The second argument is necessary to provide a title for the

generated plot. This routine will fit each pixel's response to a straight line and generate error bars for them. A scatter plot of dark currents and error bars is created. A two-column matrix is returned, with the first column containing the mean dark current value for each pixel and the second column containing the corresponding standard error bar size, all in nA/cm^2.

B.10 Multiple pixel photocurrent analysis—long integration times

The following steps illustrate how to take photocurrent data on 256 pixels. Integration times are varied from 6.4 ms to 25.6 ms in steps of 25.6 ms. This was originally intended to measure dark current; therefore, the names of many of the files involved contain the word 'dark'. However, this same procedure can be used to measure any photocurrent, as long as the pixel in question does not saturate in 100 μs. This is effective for PD4 and PD8. PD1, PD2, PD5, and PD6 tend to have dark current values too high to be effectively measured in this way.

1. All cables should be connected between the probe card and the electronics box. Turn power strip on.

2. Type `mpuf powerup.com` to reset the electronics, clear DACs, etc.

3. Insert APS device into probe card. Close handle.

4. Turn the power supplies for both VDDD and VDDPG up to 3.3 V. They should be supplying 27 mA and 80 mA respectively.

5. Type `set_subarray.tcsh 4` to choose to examine PD4. Similarly, a different number may be substituted in place of 4 to obtain data on a different pixel type. To examine which pixel precisely is the starting pixel, `sub_init.sdoc` may be examined and modified manually.

6. Type `make_sub16dark.tcsh` to recompile all of the necessary files.

7. Type `run16x16dark.tcsh` to accumulate all of the data. A total of 8 frames are taken, 2 each from 4 different time scales.

8. If data is out of range, adjust the video board potentiometer (Figure B-3) and try again.

9. In IDL, type `stats = subarray16dark('filename.01.fits', 'filename.03.fits','filename.05.fits','filename.07.fits')` to analyze the data from these files. Since two files were taken with each different integration times, and the first file with a given SRAM/PRAM pattern is usually not of good quality, the listed files should always be the second, fourth, sixth, and eighth files captured by `nova2fits`. The final argument is necessary to provide a title for the generated plot. This routine will fit each pixel's response to a straight line and generate error bars for them. A scatter plot is created. A two-column matrix is returned, with the first column containing the mean dark current value for each pixel and the second column containing the corresponding standard error bar size.

Appendix C

APS Test System Reference

This document is intended to provide the user already familiar with operation of the XIS electronics system with enough knowledge to comfortably use the modified electronics to operate an APS device. Throughout this document, if no path is given for a filename, the relevant files are located in `/nfs/min/s1/aps/testdir`

C.1 Background Documentation

Those not familiar with the XIS system should first see the relevant documentation.

- `/nfs/willow/d1/schematics/SEQ_Spec_RevA.txt`—sequencer operation
- `/nfs/willow/d1/schematics/spram.txt`—compiling SRAM/PRAM files

C.2 DAC Channel Assignments

Driver board DAC channels are assigned as follows.

- **Channel 0**—VDDD—Due to current drive problems, VDDD is now controlled by an Agilent power supply. A new set of devices has been received since this change was made; these devices do not demand huge currents from VDDD. It remains to be seen if the connection to DAC0 damaged the old devices in such a way that they began to consume large currents. After testing is complete,

it is worth experimenting with connection VDDD back to DAC0 to see if this causes high current again or not.

- **Channel 1**—unused
- **Channel 2**—unused
- **Channel 3**—VDD—Setting the DAC to 0xEC produces approximately 3.3V.
- **Channel 4**—unused
- **Channel 5**—unused
- **Channel 6**—ICMN—DAC6 controlls the voltage across the resistance R1 + R2 = 940 kΩ on the probe card. 10 V supplies approximately 10 μA. Setting the DAC to 0xC8 produces approximately 10V.
- **Channel 7**—ICMP—DAC7 controlls the voltage across the resistance R3 + R4 = 440 kΩ on the probe card. -10 V draws approximately 20 μA. Setting the DAC to 0xAF produces approximately -10V.
- **Channel 8**—unused
- **Channel 9**—TX
- **Channel 10**—PGBIAS
- **Channel 11**—unused
- **Channel 12**—VDDPG—Due to current drive problems, VDDPG is now controlled by an Agilent power supply. A new set of devices has been received since this change was made; these devices do not demand huge currents from VDDPG. It remains to be seen if the connection to DAC0 damaged the old devices in such a way that they began to consume large currents. After testing is complete, it is worth experimenting with connection VDDPG back to DAC0 to see if this causes high current again or not.

- **Channel 13**—VDDMAXA—Setting the DAC to 0xF3 produces approximately 3.3V.

- **Channel 14**—unused

- **Channel 15**—VRST—Setting the DAC to 0xFC produces approximately 3.3V.

C.3 Sequencer Operation

The modification of the sequencer has been discussed in Section 3.2.2. The sequencer line remapping table and sequencer opcode table are repeated below (Tables C.1 and C.2). XIS users must keep in mind that the sequencer no longer controls driver board clocks; it now generates 3.3V digital signals used by APS-1.

One wrinkle in the operation of the modified sequencer is that data from the address-latch board is delayed by one clock cycle. The actual sequencer, located on the controller board, produces the patterns as specified in the sdoc file. Most of these lines are then sent to the address-latch board where they are processed for one clock cycle. The video board control lines, however, are not processed in this way; the other sequencer lines must therefore be offset by 1 pixel minor cycle in order to realize the proper waveform. This is important to remember when creating sdoc files for APS-1.

C.4 .com files

The following .com files are useful for operating APS-1. Unless otherwise specified, each .com file loads a PRAM file of the same name.

- `aps_clear_dacs.com`—Sets all DACs to 0.

- `aps_hk_*.com`—* may be `dacs`, `power`, or `dump`. The housekeeping channels for either the DAC outputs, XIS power lines, or every channel is requested. In order to make sense of what is reported, the APS version of `commands.h`, located in `/nfs/min/s1/aps/lib/` should be used. Does not use the sequencer at all.

	Mode 0 (Count/Read)	Mode 1 (Address Load)
B[15]	CB	Unused
B[14]	PG	Add[7]
B[13]	RSTG	Add[6]
B[12]	SHR	Add[5]
B[11]	SHS	Add[4]
B[10]	Row Op[2]	Add[3]
B[9]	Row Op[1]	Add[2]
B[8]	Row Op[0]	Add[1]
B[7]	Col Op[2]	Add[0]
B[6]	*Reserved for video board*	
B[5]		
B[4]		
B[3]		
B[2]	Col Op[1]	Load
B[1]	Col Op[0]	Row/$\overline{\text{Column}}$
B[0]	Mode	Mode

Table C.1: Sequencer line mapping for APS-1 operation. A Xilinx CPLD allows 12 signal lines to effectively control 21 lines. The lowest bit, B[0], determines the mode and therefore the function of all the other bits.

- `aps_test??.com`—?? must be in the range 01–16 and represents any pixel type, i.e. `aps_test02.com` tests a pixel of type PD2. One pixel in that subarray is repeatedly reset, and an oscilloscope should be used on output of the device (typically the video board add-on is the best place to do this—see Figure C-1). No data is sampled; SHR and SHS are instead held open. Precisely which pixel in the subarray is determined by `aps_set_p[dg]??.sdoc`. SRAM sources are `aps_test_pd_all.sym` and `aps_test_pg_all.sym`. All source files are located in `/nfs/min/s1/aps/testdir/single_pixel_read/`

- `array.com`—Reads out each working PD subarray in both high and low gain video modes. Most will saturate. Actually calls `pd?array.com` to do this; see that entry for more details.

- `dummy.com`—Operates dummy load, which must be connected for this file's results to be meaningful. The top half of the generated fits file contains data where an input signal simulating an x-ray is present, while the bottom half

Opcode	Function
000	Hold current value
001	Hold current value
010	Store current address as quick-load value
011	Recall quick-load value
100	Set address to 0x00
101	Increment current address
110	Decrement current address
111	Set address to 0xFF

Table C.2: Opcodes for address operations. These operations allow the user to execute common operations such as incrementing the row or column address without leaving changing to Mode 1 and giving up control of the sample/hold clocks, among other. These opcodes are used in the Row Op and Col Op fields found in Table C.1 and affect only the row or column address, depending on in which field the operation is called. Quick-load is a useful feature allowing the user to set an address, typically the initial row and column in an array readout, that may be returned to instantly.

contains data without that signal.

- `pd?array.com`—? may be any number in the range 1-12 and represents that photodiode type. `pd?array.com` repeatedly reads out the entire 64x64 subarray of the specified photodiode. See `subarray?x?.com` for info on analyzing this data.

- `pdsingle.com`—Repeatedly reads out a single pixel, which is set by `aps_set_single.sdoc`. The SRAM source for is `single.sym`.

- `pdwait4.com`—Accumulates dark current data on 256 different pixels by using four different integration times for each pixel. The SRAM source for it is `single.sym`. Data should be analyzed using the IDL routine `single_dark_256`.

- `pdwait8.com`—Accumulates dark current data on 1 pixel by using eight different integration times. Many more points of data for that one pixel are taken than in pdwait4.com. The SRAM source for it is `single.sym`. Data should be analyzed using the IDL routine `single_dark`.

- `powerup.com`—Performs a hardware reset, clears the DACs, and reads them out to make sure they're reset. Should be done on power up.

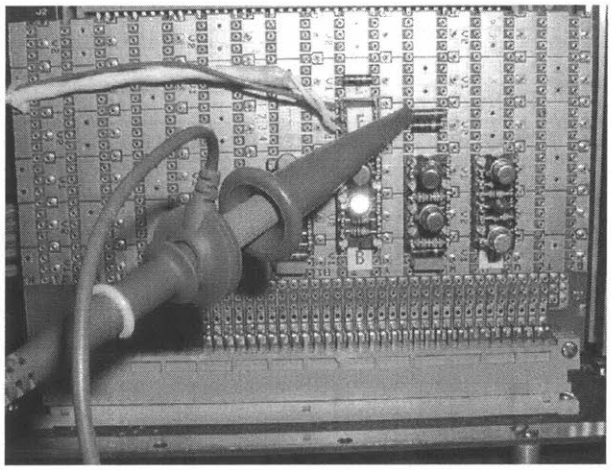


Figure C-1: The scope probe is shown on the video add-on board. R11 is being probed, so that the waveform seen is V_{REF}.

- `subarray?x?.com`—Repeatedly reads out a number of different subarrays. The size of the subarray is determined by the values in place of ?, i.e. `subarray8x8.com` reads out an 8x8 array. Acceptable values are 4x4, 8x4, 8x8, 8x16, 16x16, 32x16, 32x32, 64x32, and 64x64. The initial pixel of the subarray readout is set by `sub_init.sdoc`. SRAM source is subarray.sym. `pd?array.com` is simply a 64x64 subarray readout with the initial point fixed at the corner of a photodiode type. The fits files as generated by nova2fits are not particularly useful; the geometry is off, as the actual array being read is not 272x1024, but rather may vary from 4x4 up to 64x64. IDL routines `repack.pro`, `repack8x4.pro`, `repack8x8.pro`, `repack8x16.pro`, `repack16x16.pro`, `repack32x16.pro`, `repack32x32.pro`, `repack64x32.pro`, or `repack64x64.pro` (depending on the subarray readout size; `repack.pro` is used for a 4x4 array) should be used to break the fits file down into its component subarrays, as well as accumulating some statistics on them, each of which is written to a separate fits file. `subarray16x16.com` is also used to take dark current data for PD4 and PD8, which have very low dark current. See `subarray16x16wait?.com` for more info.

- `subarray16x16wait?.com`—Along with `subarray16x16.com`, these files (where

? is 1, 2, or 3) are used to test 256 pixels at a time for dark current by varying integration times from 25 ms up to 100 ms. Each file reads out the same 16x16 subarray, but with differing integration times. The `wait?` files fill in the gap with garbage data. The results can be analyzed with the IDL routine `subarray16dark`.

- `testpixel.com`—Can be used to operate an APS test pixel. This requires some cable changes, and should probably not be used if the arrays work.

C.5 .sdoc files

The following .sdoc files are useful building blocks for timing patterns for APS-1 operation.

- `aps_readout.sdoc`—Used to view APS output on scope. Holds reset high for a long time, then releases it, and keeps SHS and SHR open the whole time.

- `aps_readout_no_reset.sdoc`—Used to view APS output on scope. Holds reset low and keeps SHS and SHR open the whole time. Is used with `aps_readout.sdoc` to provide longer integration times by adding space between resets.

- `aps_set_single.sdoc`—Sets the pixel used as the starting point for files such as `pdsingle.com`, `pdwait4.com` and `pdwait8.com`

- `dummy.sdoc`—Operates the dummy load, with the x-ray simulation signal present (see `dummy.com`).

- `single_no_reset.sdoc`—Used with files such as `pdsingle.com`, `pdwait4.com` and `pdwait8.com`. Operates the video board as if there were signal present, but the result is meaningless. Nothing has been sampled. Is used as a space filler in these files.

- `single_reset.sdoc`—Used with files such as `pdsingle.com`, `pdwait4.com` and `pdwait8.com`. Reads out a single pixel. The data created from this is genuine, as opposed to that from `single_no_reset.sdoc`.

- `single_reset_increment.sdoc`—Used with `pdwait4.com`. Reads out a single pixel and increments the column address.

- `single_reset_newline.sdoc`—Used with `pdwait4.com`. Reads out a single pixel and increments the row address, while resetting the column address to its original value.

- `sub4x4ap.sdoc`—Used as part of all subarray readouts. Increments the column address and reads out a pixel (active pixel,AP). This was originally used for a 4x4 readout, hence the name.

- `sub4x4fs.sdoc`—Used as part of all subarray readouts. Recalls the original row and column addresses (frame start, FS) and reads out a pixel.

- `sub4x4ls.sdoc`—Used as part of all subarray readouts. Recalls the original column address, and increments the row (line start, LS) and reads out a pixel.

- `sub_init.sdoc`—Used as part of all subarray readouts. Sets the starting address.

- `sub_init_p[dg]?.sdoc`—Used by `pd?array.com` readouts. Sets the address to the corner pixel of a given subarray.

- `zero.sdoc`—Operates the dummy load, without the x-ray simulation signal present (see `dummy.com`).

C.6 Shell Scripts

The following shell scripts are useful for taking measurements of APS-1.

- `make_pdwait?.tcsh`—? may be 4 or 8. After the starting address of the single pixel readout (found in `aps_set_single.sdoc`) has changed, this script will recompile the associated files.

- `make_sub16dark.tcsh`—After the starting address of the subarray readout (found in `sub_init.sdoc`) has changed, this script will recompile the associated files for a 16x16 dark current measurement.

- `run16pdwait8.tcsh`—Runs `pdwait8.com` with 16 different pixels. `nova2fits` should be restarted with a new filename before running this, in order to use the IDL routine `run_single_dark` to analyze the data. In general, `set_and_run_single.tcsh` should be used instead, as it will gather data on 256 pixels much faster.

- `run16x16dark.tcsh`—Runs the `subarray16x16wait?.com` files to gather dark current data on 256 pixels with low dark current, such as PD4 and PD8.

- `set_and_run_single.tcsh`—Takes a single parameter, a number which indicates which pixel type to test. `aps_set_single.sdoc` is subsequently altered, files are recompiled, and three frames of data are taken using `pdwait4.com`.

- `set_pixel.tcsh`—Used by `run16pdwait8.tcsh` to change the initial pixel. Since `run16pdwait8.tcsh` is not recommended for use, `set_pixel.tcsh` is now nearly useless.

- `set_single.tcsh`—Used by several other scripts. Takes a single argument, a number which indicates which pixel type to test. `aps_set_single.sdoc` is subsequently altered and files are recompiled.

- `set_subarray.tcsh`—Used by several other scripts. Takes a single argument, a number which indicates which pixel type to test. `sub_init.sdoc` is subsequently altered and files are recompiled.

C.7 IDL routines

Except for `repack.pro`, these are all currently located in `/nfs/benz/h5/mlcohen/idlpro/`. `repack.pro` was originally created by Beverly Lamarr.

- `dark16x16.pro`—Performs dark current analysis on 256 pixels taken from 16x16 subarray readouts, like those created by `run16x16dark.tcsh`. Is more conveniently called automatically by `subarray16dark.pro`.

- `gfit.pro`—Plots a histogram and does a Gaussian fit on pixel data returned by `subarray16dark.pro` or `single_dark_256.pro`.

- `gfiterror.pro`—Plots a histogram and does a Gaussian fit on pixel error data returned by `subarray16dark.pro` or `single_dark_256.pro`.

- `repack?x?.pro`—Used to analyze subarray readouts. Repacks the data into fits files of the appropriate size, saving up to 100 of them. Simple statistics are done on each pixel, and these are saved to fits files too.

- `repack16x16wait?.pro`—Used to analyze subarray dark current measurements. Repacks the data into fits files of the appropriate size, saving up to 100 of them. These files ignore the dead space between readouts due to the longer integration times. Simple statistics are done on each pixel, and these are saved to fits files too. Is more conveniently called automatically by `subarray16dark.pro`.

- `run_single_dark.pro`—Analyzes data created with `run16pdwait8.tcsh`. The argument should be the name of the series of fits files created, without the `.??.fits` on the filename. As with `run16pdwait8.tcsh`, use of this file is not recommended.

- `single_dark.pro`—Will analyze a file created with `pdwait8.com`. This does dark current analysis of just one pixel, but with many more points that `pdwait4.com`.

- `single_dark_256.pro`—Will analyze a file created with `pdwait4.com`. Dark current is analyzed and a scatter plot is created. The returned value is a two column matrix. The first column contains mean dark current values for each pixel. The second column contains their standard deviations.

- `subarray16dark.pro`—Calls `repack16x16wait?.pro` and `dark16x16.pro` to analyze dark current data for pixel types with low dark current, typically created by `run16x16dark.tcsh`.

C.8 Probe Card

A probe card was designed to hold APS-1 while it is operated. Figre C-3 is a schematic of the probe card. A full list of parts for the probe card is listed below.

U1 = Kyocera PGA100 socket = 3M 2101-6313 series
C1, C3, C5, C7, C9 = 4.7 μF tantalum, 1812 footprint
C2, C4, C6, C8, C10 = 0.1 μF ceramic, 0805 footprint
C11, C12 = 0.27 μF ceramic, 0805 footprint
R1, R2 = 470 kΩ
R3, R4 = 220 kΩ
J1, J2 = Micro-D 25 pin sockets = MDM-25PBR
J3, J4 = 3-pin header

The socket has a keyed location to insure the chip is inserted correctly. The capacitors are solely for bypass. R1+R2 and R3+R4 determine the current through ICMN and ICMP, respectively. J1 serves as the connector for the analog cable. J2 is the connector for the digital cable. The headers connect BLK_GND and CAVITY to ground, but may be used instead to connect them to pins on the analog cable for biasing, if necessary. All device grounds are directly connected on the probe card.

C.9 Dummy Load

A dummy load may be used to test the video system. The dummy load may be created by connection 10 Ω resistors from Vsig to ground and from Vref to ground, and by connecting CB to Vsig through a 4.3 kΩ resistor. The 10 Ω resistors pull the same current as the actual device. 3.3V from CB, through the 4.3 kΩ resistor emulates the arrival of an x-ray by creating an 8 mV signal, which should raise the video level by 1500 adu. `dummy.com` may be used to operate the dummy load.

The physical dummy load consists of two pieces. The 10 Ω resistors are located on a 37-pin solder cup connector that goes in place of the analog cable on the XIS box, at J5. One resistor is connected from pin 29 to 30, and the other from pin 31 to 30. The 4.3 kΩ resistor is connected between a pin and a set of eight connections to the video add-on speedboard. The single pin should be connected to CB, located at J3-18 on the address latch board. The speedboard connector, labelled 'F', fits next to an indentical connected labelled 'E' on the board.

C.10 XIS to APS Conversion List

This section contains a full list of changes made to the XIS electronics boxes in order to produce the APS test system as it currently stands.

C.10.1 Driver Board

Substitutions

R10 = 160k

R20 = 182k

R35 = 100k

R36 = 40.2k

R37 = short

R38 = 100k

R39 = 40.2k

R40 = short

R45 = 33k

R46 = 68k

R47 = 40.2k

R48 = short

R49 = open

R55 = 267k

R56 = 100k

R63 = 267k

R64 = 100k

R95 = 4.02k

R96 = 51

R136 = short

R139 = short

R142 = short

R146 = short

Remove U14, jumper pin 5 to pin 6, pin 9 to pin 1

Remove U18, jumper pin 4 to pin 1, pin 8 to pin 9

Remove U19, jumper pin 16 to pin 3, pin 9 to pin 8

Jumper R118-1 to D4 cathode

Jumper R127-1 to D10 cathode

Additions

26.7k from R12-2 to C9-1

26.7k from R22-2 to C15-1

10Ω and 6.8Ω in parallel with R92

6.8Ω in parallel with R97.

Thermally conductive epoxy around base of Q8, Q10

DAC4 changes

The following changes convert DAC4 into a positive voltage source. They are not necessary since DAC4 is currently unused, and DAC4 has not yet been tested.

Replace Q3 with 2N2219AH

R16 = 160k

Remove R117

Reverse C45A polarity

Connect C14A-2 to C17A-1

Remove R18A

Connect 26.7k from R18-2 to C15-1

Replace R101 with two 82Ω in parallel

Remove D10,D12,D14,Q30,Q32,Q34

Remove U17, jumper pin 5 to pin 8

Jumper from R130-1 to D12 cathode

R137 = short

C.10.2 Video Board

R76B = 24Ω

Remove U1B, Q4B, Q3B, Q5B, Q2B, Q2C, R2B, R3B, R5B, R6B, R4B, R7B, R8B, C2B

Connect a 10 kΩ potentiometer from U3B-7 to U3B-4. The arm of the pot should be connected to U3B-2 through a 10 kΩ resistor. The pot screw should be accessible from the top of the board.

Video Add-On

The Video Add-on board is located on speed board in the J17 slot of the backplane. The schematic for it is shown in Figure C-2. Part values are listed below.

R1 = 200

R2 = 200

R3 = 1k

R4 = 10k

R5 = 10k

R6 = 10k

R7 = 140

R8 =140

R9 =1k

R10 = 1k

R11 = 500

R12 = 500

R13 = 100

R14 = 51

R15 = 160

C1 = 1.0 μF

C2 = 0.1 μF

C3 = 0.1 μF

All NPN = 2N2222A

All PNP = 2N2907A

C.10.3 Controller Board

No changes

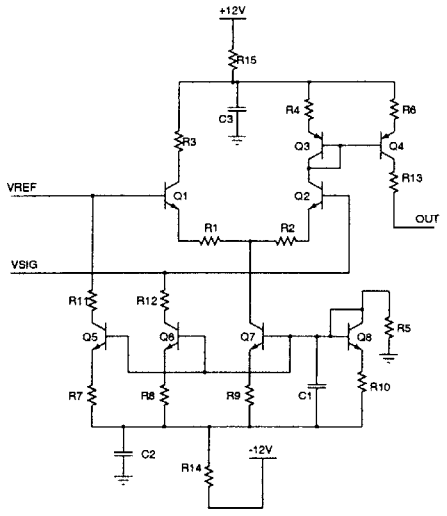


Figure C-2: New front end for video board. Q_1 and Q_2 are a differential pair which subtract V_{ref} from V_{sig}. Q_5 and Q_6 provide the 5 mA current sources required on the output transistors of APS-1. The collector of Q_4 connects to the rest of the video board, leading into the dual-slope integrator.

C.10.4 Address Latch Board

This is a new board created for APS use. The Latch Board occupies the backplane slot originally held by the driver board. With this setup, the driver board goes on top of the latch board, which has a 90 pin connector on both edges of the board that acts as an extender card, providing complete feed-through from the backplane to the driver board. Its general functionality has been described in Section 3.2.2. Schematics are shown in Figures C-4, C-5, and C-6. An equivalent schematic for the internal logic on the Address Latch Board is shown in Figure C-7.

The Latch Board is controlled by a Xilinx XC9500XL series CPLD. Twelve of the sequencer lines are routed from the controller board to inputs of the CPLD. The CPLD uses a scheme described later to convert these 12 digital lines into 21 digital lines that control the APS device. The 21 outputs are routed to J3, a 25-pin D-sub connector, which will connect to the vacuum chamber and then the APS array. Two inputs to the board (clock and S15) are not available on the backplane, and must arrive via J4, a D-sub connector which is currently unused, except for these 2 signals. Note that Xilinx chips are reprogrammable, and the functional-

ity of the board can be almost completely changed by burning a different JEDEC file to the chip (including access to signals on J4). J5 is the mating connector for the Xilinx Parallel Cable IV (currently located in 37-524), which allows the user to program the Xilinx device. The vhdl files for the current version are located at `/nfs/benz/h5/mlcohen/addresscircuit/`.

Programming

To program the latch board, apply 5 V to B5 and ground B1. Connect the Xilinx Parallel IV Cable to J5, and load up Impact from the Xilinx software. Select boundary scan-JTAG mode and follow on-screen instructions.

Design Error on board

There was an error in design of the board. The original schematic had two separate grounds, one for the backplane/driver board connectors, and another that serves as ground for the CPLD circuit. These two must be connected together. *Whenever fabricating a new Latch board, a short wire must be run from pin 2 of the regulator (U2) to pin B1 of J1.*

Parts List

A full list of parts for the Address Latch board is listed below.

C1,C3,C5,C7,C9,C11,C13 = 0.01 μF ceramic = ECJ-2VB1H03K
C2,C4,C6,C8,C10,C12,C14 = 0.10 μF ceramic = C1812C104K1RA
C15 = 10.0 μF tantalum = TAJE106K050R
C16 = 0.10 μF tantalum = T491A104M035AS
J1 = 90 pin (2x45) header = PCN10-90P-2.54DS
J2 = 90 pin (2x45) receptacle = PCN10C-90S-2.54DS
J3 = 25 pin D-sub receptacle
J4 = 37 pin D-sub receptacle
J5 = 14 pin (7x2) JTAG header = Molex 87831-1420, available from Heilind

Electronics

U1 = Xilinx CPLD = XC95144XL-TQFP100

U2 = 3.3V regulator = LM2937/TO263

C.10.5 Board-to-board Jumper Wires

Controller board U11 (AESEQ) pin 25 to Address-Latch board J4 pin 18.

Controller board backplane connector P1 pin B21 to Address-Latch board J4 pin 19.

Twisted, shielded pair: Video board Q2B base to Vsig on video add-on, video board Q2C base to Vref on video add-on

Video board Q2B collector to Vout on video add-on

C.10.6 Cables

Four cables are necessary to run APS-1.

Digital Cable 1

Digital Cable 1 connects J3 on the address latch board to Digital Cable 2. At one end is a 25 pin D-sub header. The other end is a 37 pin D-sub receptacle. Pins are connected numerically.

Digital Cable 2

Digital Cable 2 connects Digital Cable 1 to J2 on the probe card. At one end is a 37 pin D-sub header. The other end is a 25 pin MDM socket. Pins are connected non-numerically, and are listed in Table C.3.

MDM Pin #	D-sub Pin #
1	13
2	25
3	24
4	23
5	22
6	21
7	20
8	19
9	18
10	17
11	16
12	15
13	14
14	n/c
15	n/c
16	n/c
17	n/c
18	5
19	6
20	7
21	8
22	9
23	10
24	11
25	12

Table C.3: Digital Cable 2 Instructions

Analog Cable 1

Analog Cable 1 connects J5 on the XIS box to Analog Cable 2. At one end is a 37 pin D-sub header. The other end is a 37 pin D-sub receptacle. Pins are connected numerically, except that pins 37, 12, and 25 should be removed from the connector at the receptacle end. This is to allow VDDPG and VDDD to be controlled by external Agilent supplies, as opposed to the driver board DACs. In place of pin 37 should be a single wire coming from the ground of the power supplies. In place of pin 12 should be the voltage from the VDDD supply. In place of pin 25 should be the voltage from the VDDPG supply.

Analog Cable 2

Analog Cable 2 connects Analog Cable 1 to J1 on the probe card. At one end is a 37 pin D-sub header. The other end is a 25 pin MDM socket. Pins are connected non-numerically, and are listed in Table C.4.

MDM Pin #	D-sub Pin #
1	29[1]
2	n/c
3	10
4	6
5	n/c
6	5
7	n/c[2]
8	26
9	3
10	1
11	2
12	12
13	25
14	31[1]
15	n/c
16	n/c
17	n/c
18	n/c[2]
19	n/c
20	23
21	28
22	n/c[2]
23	n/c[3]
24	37
25	30

1. These wires should be twisted.

2. These pins are currently not used, buy may be connected to DACs in order bias BLK_GND or CAVITY. See Section C.8.

3. This pin may be grounded, though that is unnecessary as it is tied to ground on the probe card. It can be used as a ground elsewhere if necessary.

Table C.4: Analog Cable 2 Instructions

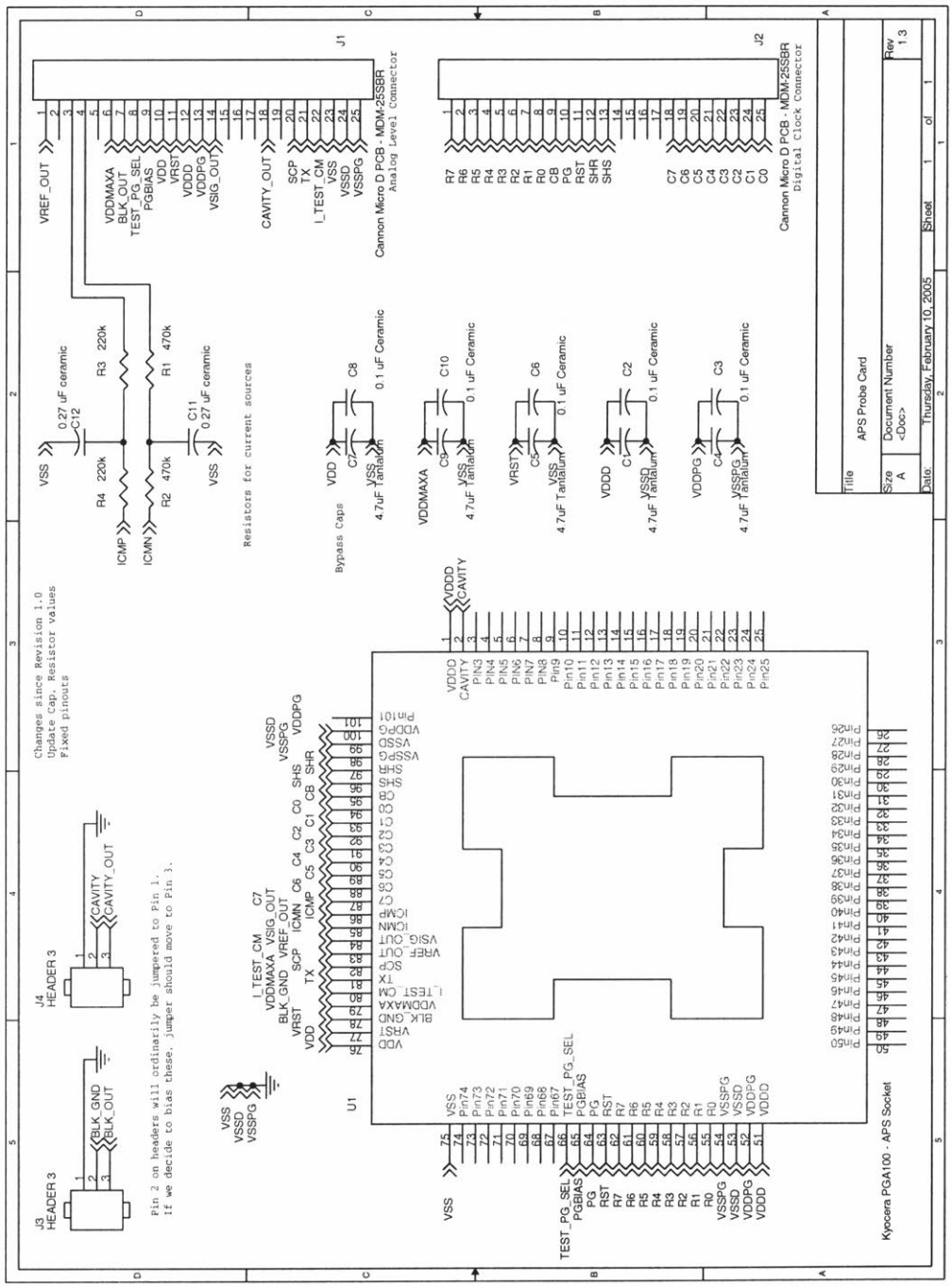


Figure C-3: Schematic of APS-1 probe card.

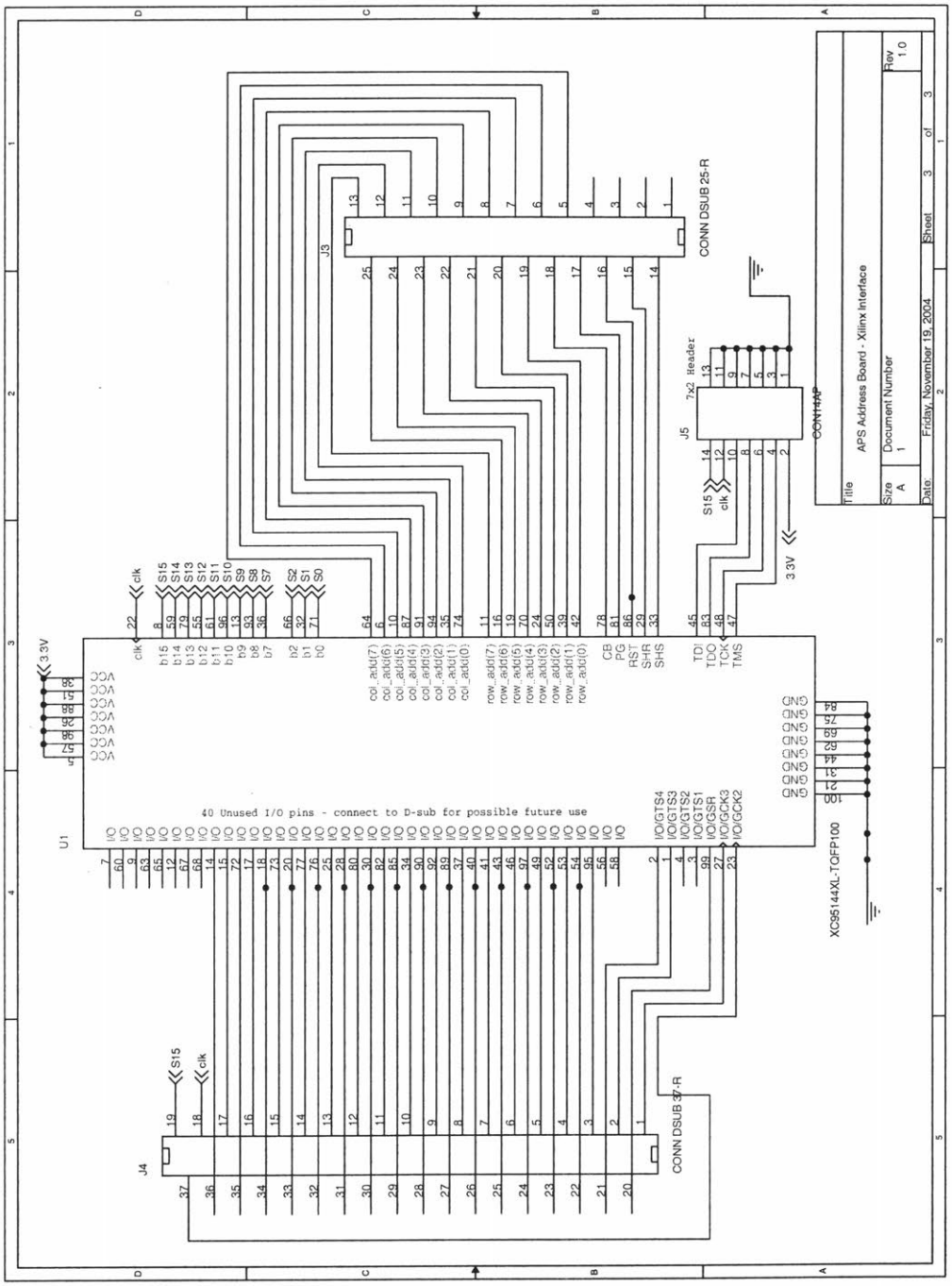


Figure C-4: Address Latch board schematic, page 1/3.

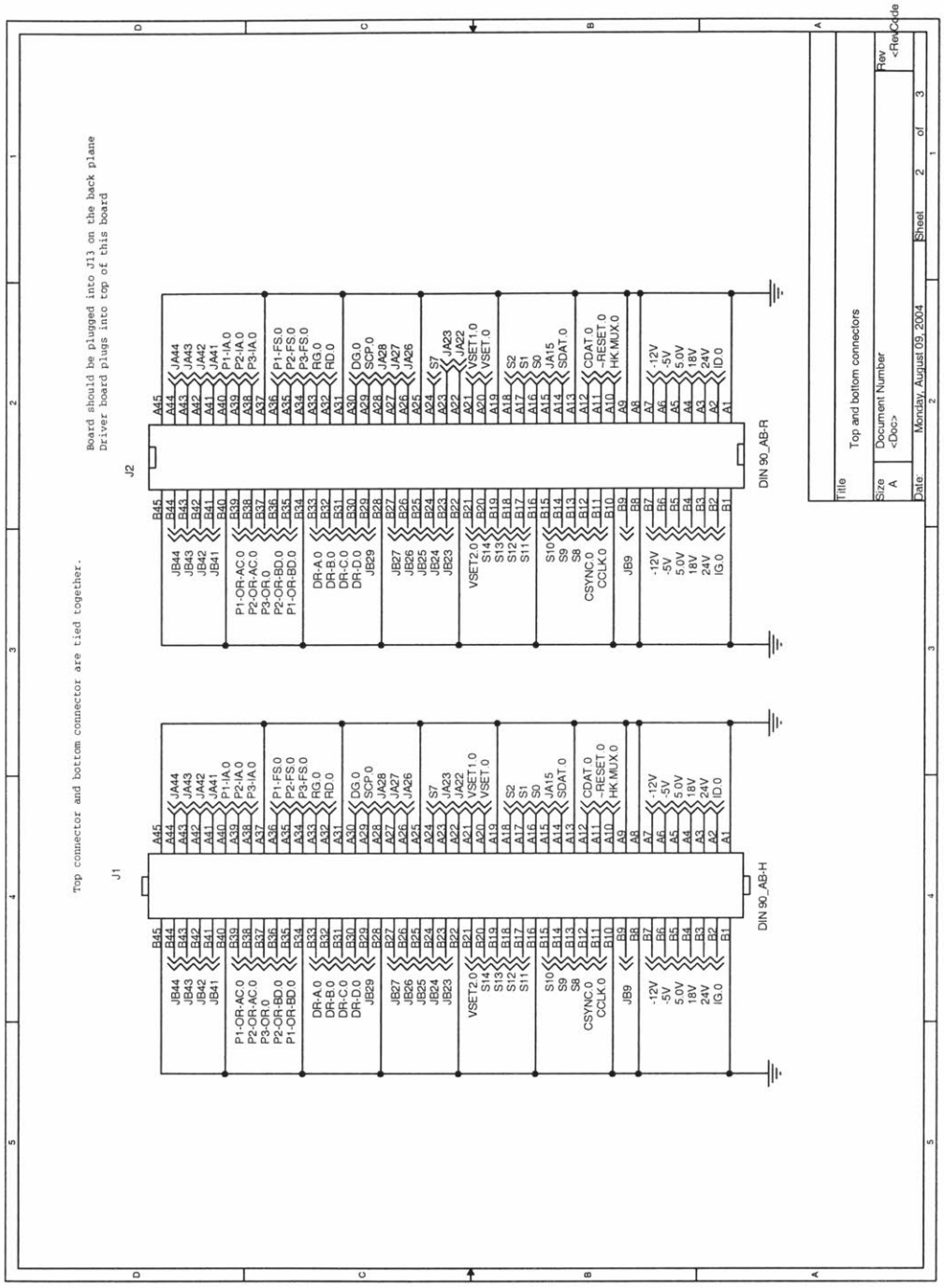


Figure C-5: Address Latch board schematic, page 2/3.

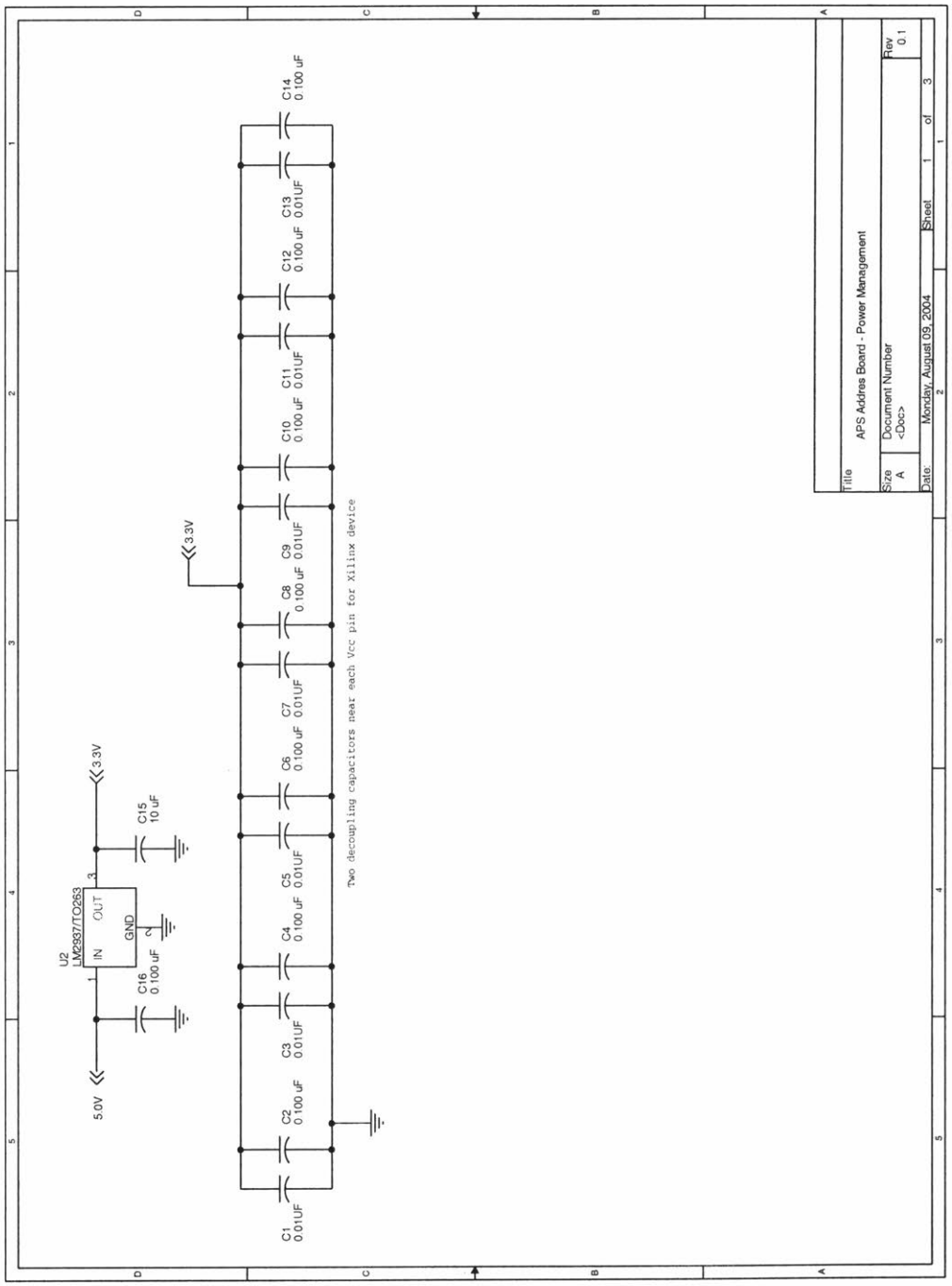


Figure C-6: Address Latch board schematic, page 3/3.

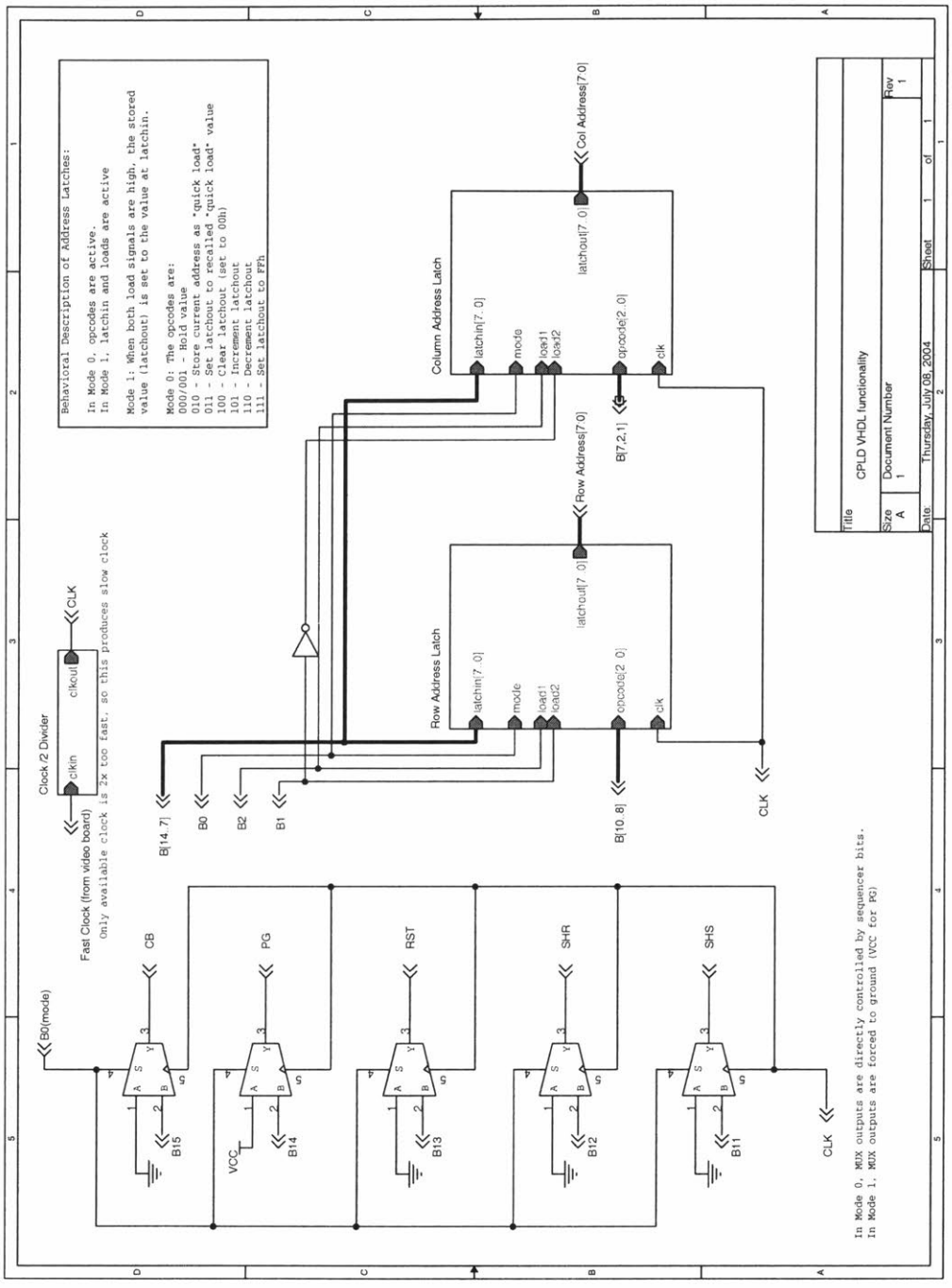


Figure C-7: Equivalent schematic for internal logic of Xilinx CPLD on address latch board. The clock divider has since been removed; CLKIN is now identical to CLK.

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