Recovered Energy Logic: Device Optimization for Circuit Implementation in Silicon and Heterostructure Technologies

by

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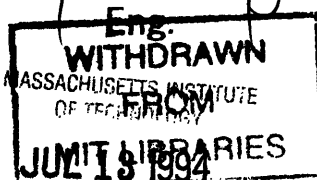
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ABSTRACT

Recovered Energy Logic (REL) is a new family of logic that charges and discharges capacitive logic nodes in an ideally lossless fashion. To accomplish this, REL uses an AC waveform as both the system power supply and a two-phase clock. Unlike mainstream logic circuits, REL circuits require substantial current from all three terminals of a transistor. This makes BJTs and MESFETs a natural choice for implementing these circuits. Device and circuit simulations are performed for REL circuits implemented in MOSFET, MESFET and BJT technologies. The advantages and disadvantages of each technology are examined. REL circuits implemented in a 2 μm CMOS technology function up to 20 MHz. The power-delay product of this circuit is measured at 0.3 pJ for a 3.3 V_{p-p} supply voltage and a 10 fF load capacitance. A comparable 2 μm minimum spacing bipolar process was operational up to 50 MHz, with a power-delay product of 0.8 pJ. The most promising technology implementation for REL circuitry appears to be MESFETs. Circuit simulations predict circuit performance up to 25 MHz for 2 μm channel length devices, with a power-delay product of only 0.05 pJ.

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CHAPTER 1

INTRODUCTION

1.1. MOTIVATION FOR WORK

The trend of device scaling in VLSI technology has resulted in chips so densely packed that power dissipation is becoming a limiting factor to further improvements in circuit speed and performance. This issue has been addressed in existing mainstream logic circuits primarily by reducing the power supply voltage. However, as CMOS technology scales into the deep sub-micron regime, fundamental physical limits are being tested. Further scaling of supply voltages in CMOS must be accompanied by reductions in device threshold voltages. This results in an increase in standby power due to subthreshold leakage currents [22]. It is clear that scaling of existing mainstream technologies will hit fundamental limits of power dissipation and heat extraction for room temperature operation. There has also been research in the area of refrigerated systems, to take advantage of improved device performance and lower dissipation levels at cryogenic temperatures. To date, there has not been significant prospects of developing cost effective, large scale systems for cooling of practical circuits. Finally, the rapid expansion of the portable electronics industry has focused attention on the need for extending the life of battery operated systems. These systems are often limited by a few power intensive functions. Significant power savings in only one aspect of the system performance can often have a profound effect on the dissipation of the entire circuit. For these reasons, it is becoming increasingly important to explore low power circuit innovations. One such circuit innovation is Recovered Energy Logic.

Recovered Energy Logic (REL) is a new family of logic that charges and discharges capacitive logic nodes in an ideally lossless fashion. To accomplish this, REL uses an AC waveform as both the system power supply and a two-phase clock. The projected power

savings compared to functionally equivalent CMOS circuitry is over 80% [1]. That is, REL dissipates less than 1/5 of the energy lost in standard CMOS.

REL circuits rely on charging currents flowing through all three terminals of a transistor. This makes the bipolar transistor or MESFET a natural choice for realizing these circuits, although MOS devices can also be used. This is in marked contrast to current logic circuit trends which use CMOS circuits almost exclusively because there is no gate current. The desire to have very little control terminal current has plagued many promising technologies, such as heterostructures, that have superior material properties, but lack a good native oxide. Rather than trying to force these technologies to behave as insulating gate MOS transistors, REL offers an opportunity to fully exploit the benefits of these technologies without sacrificing low power operation.

In light of the needs of REL devices, a fresh look at bipolar and MESFET technologies is needed, which is the primary goal of this thesis. To do this, it is first necessary to develop an understanding of the principles of energy dissipation in Recovered Energy Logic.

1.2. RECOVERED ENERGY LOGIC PRINCIPLES

The principles of lossless computation are not new. Several adiabatic logic circuits have been previously proposed [12]. The basic premise of lossless computation is that transistors are only turned on when there is zero voltage across them. When current flows, there is no voltage present, and when there is a voltage across the device, no current flows. In this way, the VI power product is always nearly zero. In order to better understand the implications of this principle, an examination of power dissipation in circuits is required.

1.2.1. POWER DISSIPATION MODELS

A CMOS logic inverter is pictured in Fig. 1.1. To analyze the power dissipation in one logic cycle, the transistor switches have been modeled as perfect switches with an associated parasitic resistance.
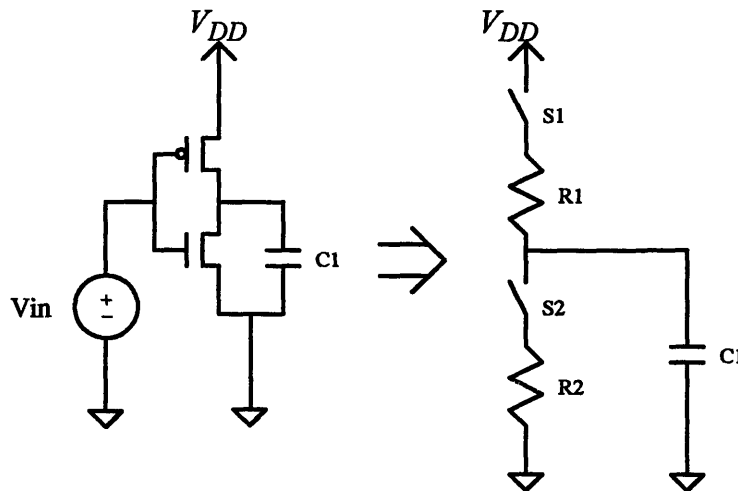
Figure 1.1: CMOS Inverter modeled as a perfect switch with parasitic resistance

Let's start by assuming that the load capacitance has been fully discharged. In order to charge up the load capacitance, the PMOS transistor is turned on. This occurs when the voltage across the transistor is its maximum value of V_{DD}. The total energy supplied by the source in charging the capacitor is given by:

$$E = \int_0^t v \cdot i \, dt = V_{dd} \cdot \int_0^t i \, dt = V_{dd} \cdot Q_C$$

where Q_C is the total charge supplied to the capacitor. However, the capacitor only stores $1/2 \cdot CV_{DD}^2$, so $1/2 \cdot CV_{DD}^2$ is dissipated in this process, assuming the capacitance to be linear with voltage. In order to discharge the capacitor, the NMOS transistor is turned on while a voltage of V_{DD} appears across this transistor. Thus, an additional $1/2 \cdot CV_{DD}^2$ is dissipated in this cycle, for a total of CV_{DD}^2 dissipated energy for a full logic cycle.

In contrast to this, Recovered Energy Logic circuits ideally only turn transistors on when the voltage across them is zero. Fig. 1.2 shows a similar switch model for charging a capacitive load in REL. The V_{AC} source could be an AC waveform with a DC offset voltage. If the capacitor is fully charged, then the switch S1 is only turned on at the peak

of the ac waveform. Similarly, if the capacitor is fully discharged, then S1 is only turned on at the trough of the AC waveform.
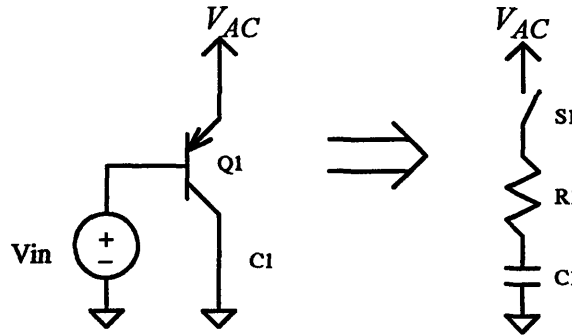
Figure 1.2: A model for charging a capacitance load in REL circuits

If the transistor is driven into saturation, then the voltage across the transistor is only $V_{CE,sat}$. The energy dissipated in this transistor during charging is given by:

$$E = \int_0^t v \cdot i\, dt = V_{CE,sat} \cdot \int_0^t i\, dt = V_{CE,sat} \cdot Q_C$$

Given this principle of circuit operation, this thesis will evaluate REL circuits fabricated in a variety of technologies in order to identify the advantages and disadvantages of each implementation.

1.3. THESIS ORGANIZATION

The second chapter of this thesis will introduce the circuit operation of Recovered Energy Logic, giving a detailed description of how logic nodes are charged and discharged in a nearly lossless fashion. An overview of the issues involved in implementing REL in each technology will be presented, touching on the major points of consideration for each device type. Chapters 3 through 8 will present a more detailed analysis of the advantages

and disadvantages of each implementation, with circuit simulations presented to demonstrate predicted device performances. Finally, Chapter 9 will present the conclusions of this work, indicating which technologies seem most promising for REL circuits.

CHAPTER 2

RECOVERED ENERGY LOGIC

2.1. INTRODUCTION

In order to understand the device requirements of Recovered Energy Logic circuits, it is important to understand how these circuits operate. This chapter will introduce REL circuits by using bipolar junction transistors. As will be seen shortly, these circuits readily lend themselves to BJT devices. However, REL circuits are not restricted to bipolar junction transistors, and explanations with MOSFET and MESFET or JFET devices will also be described. The end of this chapter will be concerned with the implications of circuit operation on the design of each device type. This will serve as a starting point for the in-depth analysis of each device type in the remaining chapters of this thesis.

2.2. RECOVERED ENERGY LOGIC CIRCUIT OPERATION

The REL circuit topology is composed of alternating carrier transport stages, where hole transport devices propagate their output on the rising half-cycle of the AC supply voltage, and electron transport devices propagate their output on the falling half-cycle. In this way, the AC supply voltage will also serve as a non-overlapping, two-phase clock. Circuits can be built in BJT, MOSFET, MESFET or JFET technologies. BJT devices will be used initially to explain the circuit operation, followed by descriptions of MOSFET and MESFET circuit implementations. Circuit operation for JFET devices will be identical to that of the MESFET circuit.

2.2.1. REL BUFFER STAGES

A basic buffer stage in REL circuitry is pictured in Fig. 2.1. As stated previously, the supply voltage, V_{AC}, could be a sinusoidal waveform with a DC offset. Let us assume that the voltage at the base of the second NPN transistor is low at the trough of the sinusoid. As will be shown, this is its pre-charged state. If the input at the base of the PNP transistor Q1 is low, then as the AC voltage rises the base-emitter junction of this transistor will become forward biased and charge up the capacitance at the base node. When the transistor turns on, the capacitance at the collector node will also be charged with a current of βI_B, until the collector voltage becomes higher than the base voltage. The device then enters saturation, and I_C approximately equals I_B. The output voltage of Q1 (which also serves as the base of the NPN transistor Q2) will then charge up to the ac supply voltage. If the voltage at the base input to the PNP transistor had been high instead, the transistor would have been cut off, and the collector voltage of Q1 would have remained low. Thus, a low input to a PNP transistor causes the output voltage to go high, and a high input causes the output to remain low. However, note that regardless of the input voltage at the beginning of the rising half-cycle, its value at the end of the half-cycle was high. This pre-charges the collector voltage of the preceding NPN stage.
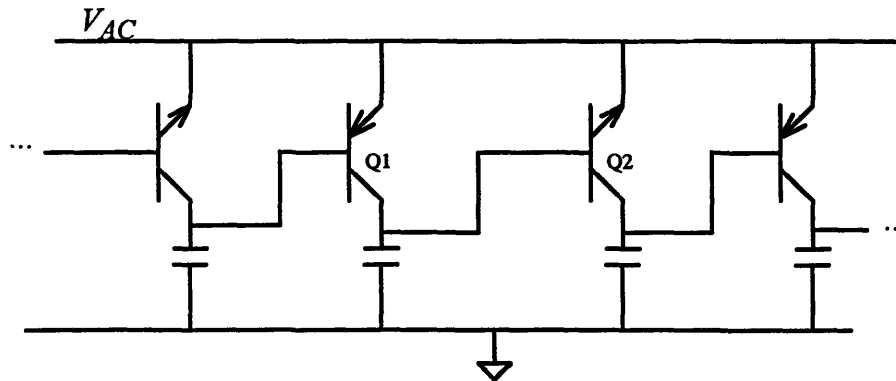
Figure 2.1: REL Bipolar Junction Transistor buffer stages

A similar description can be made of the next NPN stage, which propagates its output on the falling half-cycle of the AC supply voltage. As we saw from the PNP stage description above, in the rising half-cycle the following PNP transistor will pre-charge the output of

the NPN transistor high through the PNP base-emitter junction. If the input to the base of the NPN transistor is high at the peak of the sinusoid, when the supply voltage falls below the base voltage the NPN transistor will turn on, discharging both the collector and base capacitances. Once again, this transistor will quickly saturate due to the current gain, and the collector voltage will closely follow the ac supply. If the input to the NPN base is low, the transistor remains in cut-off and the collector voltage will remain high. Thus, a high input to an NPN transistor causes the output to discharge to a low signal, while a low input allows the output remain high at the end of the half-cycle. Regardless of the initial value of the NPN base voltage, its value at the end of the falling half-cycle will be low. This brings us to our initial assumption that the collector voltage of the PNP transistor was low at the beginning of the rising half-cycle.

2.2.2. REL INVERTER STAGES

In the preceding circuit description, an "active" signal for the PNP devices is a low input voltage; a high voltage input to the PNP transistor leaves the output in its pre-charged state. Similarly, an "active" signal for an NPN stage is a high voltage, and a low input voltage leaves the output unchanged. Considering that the output of each stage represents the input to the next stage of opposite polarity, the circuit description of Section 2.2.1 represents only buffer stages. We will define a logic "1" to be a signal that causes a transition (an active signal) and a logic "0" to be a signal that leaves the output in its pre-charged state. To create inverters out of this two-phased clock system, a high voltage at the input of an NPN stage must produce a high output. That is, an "active" input to the NPN stage must produce an "inactive" input for the following PNP stage in order for the stage to be inverting. Similarly, a low input to a PNP stage must produce a low output for the next NPN stage. This is accomplished by creating a two transistor stage with a pre-charging diode between the transistors.

REL inverting stages are shown in Fig. 2.2. At the beginning of the falling half-cycle, the collector of the output NPN will be pre-charged high from the following base-emitter junction as already explained. The collector of the first NPN transistor will also be pre-charged high through the diode. A high signal at the base of the NPN stage will cause the first NPN transistor to turn on. When this transistor saturates, the collector capacitance of

the first NPN transistor will discharge to the AC supply voltage, leaving the second NPN transistor in cut-off. Thus, the output will remain in its pre-charged high state. For a low input, the first NPN will be cut-off, and the collector of the first NPN will remain high. This high voltage will then turn on the second NPN transistor, discharging the output capacitor as the AC supply voltage falls. The PNP transistor stage works in an analogous fashion.
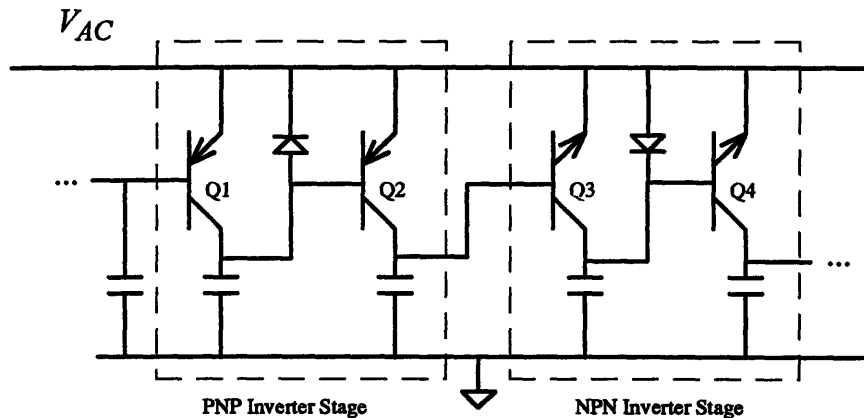
Figure 2.2: REL Bipolar Junction Transistor inverter stages

2.3. MOSFET AND MESFET CIRCUIT OPERATION

REL circuit operation in a MESFET or JFET implementation is essentially the same as that for bipolar junction transistors. The metal-semiconductor or p-n gate junction will function the same as the base-emitter junction in the BJT circuit description. While there is no gain or saturation in the MESFET devices, there will be a current path through which the capacitors may charge or discharge when the devices are on and the gate is forward biased. Other than these slight differences, circuit operation with MESFETs or JFETs is completely analogous to that of bipolar transistors.

MOSFET implementations of REL circuitry are more complex. There is no control terminal current available in MOSFETs to pre-charge the output nodes of each stage. In order to achieve this, an additional transistor must be included wherever pre-charging is required. This transistor will be wired as a diode to provide the pre-charging function.

This circuit is pictured in Fig. 2.3. The MOSFET circuit implementation thus requires two additional transistors over the other circuit implementations. However, as many of these transistors share a common node, and thus can share a common diffusion region, the layout penalty is not severe.
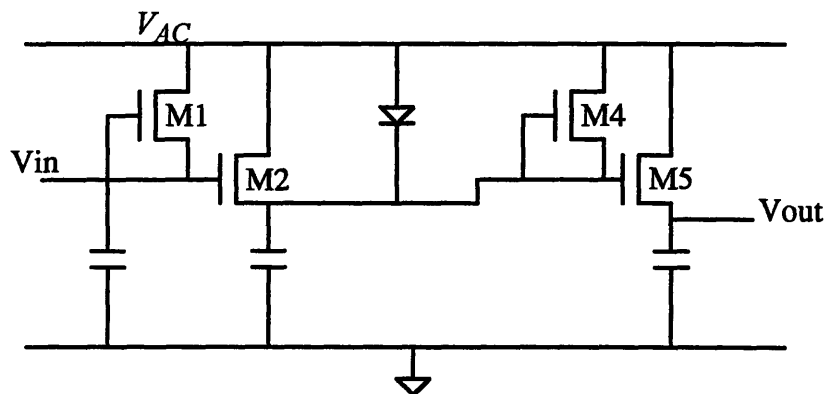
Figure 2.3: REL MOSFET inverter stage

2.4. DEVICE REQUIREMENTS

With this understanding of the circuit operation, it is appropriate to make several observations about the requirements of the devices in each implementation. This section is intended as an overview to highlight the salient features of each implementation. Further exploration of these issues will be undertaken in the appropriate chapters.

2.4.1. BIPOLAR TRANSISTOR DEVICES

The unique operation of REL circuits has its most profound effect on the device requirements of bipolar transistors. The development of Advanced Bipolar device design has focused on reducing the base current and increasing the gain and speed of bipolar devices [23,24]. While decreasing the device transit time is certainly desirable for REL circuits, the first two conditions may not necessarily be beneficial. The regions of operation for bipolar transistors in REL circuits are saturation and cut-off. Therefore,

high gains are not important to circuit operation. In fact, higher gains generally imply an increase in the stored charge in the base during saturation. This base charge must fully recombine at the peak of the AC supply voltage in order to avoid unwanted reverse recovery currents. Therefore, transistors with large gains are not optimum for REL circuits.

Another observation of bipolar device operation in REL circuits is that the cut-off condition sees both junctions reversed biased. This means that the base-emitter junction must be able to withstand a substantial reverse bias without breaking down. Also implied in this observation is that the base region must be able to withstand two reverse biased junctions simultaneously. This will limit how narrow the base region may be. It should be noted that this reverse bias condition occurs when there is very little emitter-to-collector voltage applied across the device. The two space charge regions may actually meet each other without causing conduction from emitter to collector, provided the space charge layer can extend sufficiently laterally before the base contact is encountered.

A third observation can be made about the parasitic capacitances. It was assumed that the conducting currents were mainly charging the load capacitances. The parasitic capacitances between the base-to-emitter and base-to-collector form a capacitive divider with the load capacitor. The parasitic capacitances must be small, probably no more than 1/3 of the load capacitance. This constraint is quite significant. The calculated power savings of REL circuitry over standard CMOS is based on equivalent load capacitances. If it becomes necessary to make the load capacitance large in order to avoid this capacitive divider, REL loses its advantage. For this reason, it is important that the parasitic capacitances of the bipolar devices are kept as small as possible.

Finally, there are two other important factors that are not readily apparent from the circuit description. It is shown in [1] that the power savings in REL circuits is proportional to

$$\frac{E_{REL}}{E_{CMOS}} \propto \frac{V_{BE,on} + V_{CE,sat}}{V_{AC,peak}}$$

where E_{REL} is the energy dissipated in an REL circuit, and E_{CMOS} is the energy dissipated in a comparable standard CMOS circuit. This calculation assumes equal load

capacitances. It is therefore desirable to keep both $V_{BE,on}$ and $V_{CE,sat}$ to a minimum. This fact has important consequences when considering heterojunction bipolar transistors, where the forward voltages are often larger. Another consideration is that the noise margin of the circuit is $\left(V_{BE} - V_{CE,sat}\right)$ [1], so there is a trade-off between power dissipation and noise margin to be considered. These issues, along with those discussed above, are handled in detail in Chapters 4 and 5. Heterostructure bipolar transistors are examined in Chapter 7.

2.4.2. MESFET OR JFET DEVICES

Many of the issues already discussed for the bipolar transistor are also applicable to MESFET or JFET implementations of Recovered Energy Logic circuits. One important observation for MESFET circuits is that the Schottky gate is actually operated in the forward bias regime. This is in contrast with mainstream applications of MESFET devices, where device operation is limited to the relatively small voltage range of V_t to $V_{GS, forward}$. In fact, the lower on-state voltage drops for Schottky diodes may actually be beneficial to REL circuits. In FET operation, the REL power saving is dependent on the ratio:

$$\frac{E_{REL}}{E_{CMOS}} \propto \frac{V_{G,on} + V_{DS,on}}{V_{AC,peak}}$$

where $V_{G,on}$ is the forward bias voltage drop across the Schottky gate diode. However, one must keep in mind that effective noise margin of the circuit is the difference between these two voltages. It will also be shown in Chapter 6 that it is necessary for the threshold voltage for MESFETs to be larger than the on-state voltage drop from source-to-drain in order for the circuits to operate properly.

The parasitic capacitances of the MESFET devices must be kept to a minimum for the same reason as for the bipolar devices. This is much less problematic for MESFET devices, as is shown in Chapter 6. In general, the load capacitances for MESFET devices should be quite comparable to MOSFET devices.

Finally, the need for complementary technology has a significant impact on MESFET implementations of REL circuits, especially when considering heterostructure devices such as AlGaAs/GaAs structures. These devices have traditionally been preferred over silicon MESFET technologies for the insulating properties of the AlGaAs layer, which is not utilized in REL circuits. However, the p-channel devices in III-V semiconductor material systems are actually slower than that of silicon. The implications of this are examined in detail in Chapter 8.

2.4.3. MOSFET DEVICES

Since MOS technology is fully entrenched in the semiconductor industry, REL operation in MOS technology is very important. REL circuitry implemented in MOS technology has very little impact on the design of MOS devices. Since the pre-charging diodes are implemented in diode-connected MOS transistors, it will be desirable to keep the on-state voltages of these diodes small.

$$\frac{E_{REL}}{E_{CMOS}} \propto \frac{V_t + V_{DS,on}}{V_{AC,peak}}$$

One significant observation about REL circuit operation with MOSFETs is that the off-state leakage currents of the transistor are not a significant concern for high frequency operation, since this will only add to the diode current pre-charging the output nodes. Certainly, if the circuits are operated at a low enough frequency, the leakage currents will result in discharging the load capacitance. This leakage current has been a problem in many mainstream MOS logic circuits, where decreasing supply voltages have resulted in the need for lower threshold devices. The scaling of the device thresholds should not be a problem for REL applications. The details of MOSFET operation are covered in the next chapter.

CHAPTER 3

CMOS TRANSISTORS

3.1. INTRODUCTION

As stated in Chapter 2, REL circuits can be fabricated in CMOS technology, despite the lack of gate current to pre-charge the output nodes. This problem is overcome by effectively using diodes to emulate the base-emitter charging action of the bipolar transistor. Two full inverter stages are pictured in Fig. 3.1. We shall consider the detailed operation of the CMOS circuit in order to determine the device requirements of Recovered Energy Logic circuits.

3.2. PRE-CHARGING OF OUTPUT NODES

The purpose of transistors N1 and P1 is to pre-charge the output of the preceding stage of opposite polarity. The purpose of transistors N3 and P3 is to pre-charge the intermediate node of their respective stages. Let us first look at the pre-charging action of the n-channel transistors. If the AC rail is considered the drain of the intermediate transistor N3, then the rising edge of the AC waveform would result in a positive gate-to-source voltage, turning on transistor N3. This pre-charges the output node of transistor N2 high, minus the threshold voltage of the transistor. This is comparable to the diode drop of the intermediate node of a bipolar implementation. This node will be the drain of the input transistor, N2. The pre-charging of the p-channel device output nodes is accomplished through the n-channel transistor N1. If the AC rail is considered to be the source of this transistor, then as the AC voltage falls, the gate-to-source voltage will become positive, turning on transistor N1. The resulting voltage at the input node will be the lowest point of the AC waveform, plus the voltage dropped from source-to-drain for the on-state transistor N1, comparable to the saturation voltage of a bipolar transistor. This ensures that the output of the preceding p-channel stage will be low.

A similar situation exists for the p-channel devices. Let the AC rail be considered the drain and gate of transistor P3. On the falling edge of the AC source, this transistor will turn on when the AC voltage falls below the p-channel stage intermediate node, and this node (the drain of P2) will discharge to a low voltage, plus the threshold voltage of transistor P3. Transistor P1 will have its source at the AC rail. If the voltage at the output of the n-channel stage is low, then the gate-to-source voltage of this transistor will become negative on the rising half-cycle. Transistor P1 will turn on, charging up the output node of the preceding n-channel stage to the AC rail, minus the on-state voltage drop across P1.
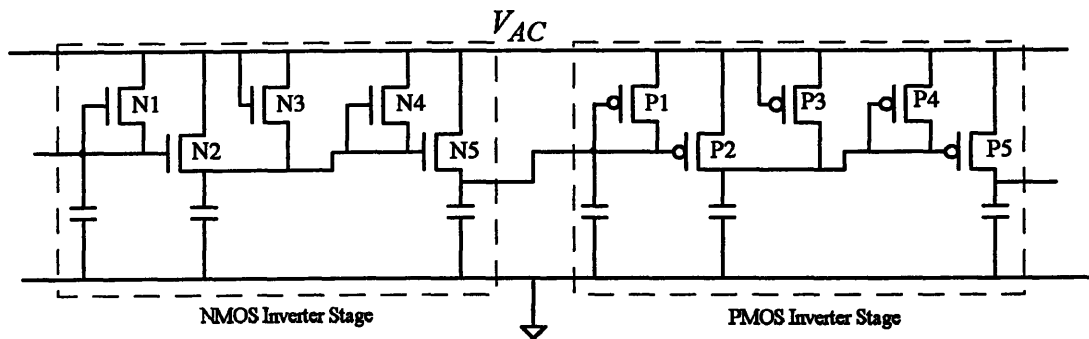
Figure 3.1: REL MOSFET n-channel and p-channel inverter stages

3.3. CIRCUIT OPERATION

With the pre-charging of the nodes established, the circuit operation proceeds essentially the same as that for the bipolar operation of the inverter stages. The n-channel stages propagate their output on the falling half-cycle of the AC waveform. We shall consider the AC rail to be the source of the first n-channel transistor, N1. If the input is high, then as the AC voltage falls below the input V_{GS} will become positive and this transistor will turn on, discharging its output node with the falling waveform. This will keep the gate-to-source voltage of the second n-channel transistor at zero, and the output of the n-channel inverter stage will remain high. Had the input to N1 been low, this transistor would remain off during the rising AC half-cycle, allowing N5 to turn on when the AC voltage

falls below the intermediate node voltage. The output node will then discharge with the AC voltage to a low value, plus the source-to-drain voltage drop of the on-state transistor.

When this cycle is completed, the intermediate node of the inverter stage would remain high in the absence of transistor N4. The purpose of this diode connected transistor is to bring the center node voltage down as the AC waveform falls. This ensures that as the AC waveform begins the rising cycle of the next period, the output transistor M5 does not remain on and charge up its output node to a high voltage again. Considering that this node will be pre-charged high on the rising half-cycle anyway, this may seem unnecessary. This is a subtle but important point to proper operation of the inverter stages. If the output of N5 remains only $V_{DS,on}$ below the AC waveform, the input transistor to the next p-channel stage will never see enough negative V_{GS} voltage to turn on.

The p-channel inverter stage operates in a similar fashion, propagating its output on the rising half-cycle. If the input to P1 is low, the gate-to-source voltage will become negative with the rising source voltage. This will turn P1 on, leaving the second p-channel transistor in cut-off. The output of the p-channel inverter stage will remain at its pre-charged low voltage. If the input to P1 had instead been high, this device would be cut-off, allowing the second p-channel device to turn on and charge up the output node to the AC line voltage, minus the $V_{DS,on}$ of transistor P5. The internal transistor P4 serves the same function as that of transistor N4, namely to ensure that P5 does not remain on during the subsequent falling half-cycle of the AC supply voltage.

3.4. CMOS DEVICE REQUIREMENTS

The presence of transistors N1, N4, P1 and P4 have several unfortunate consequences for circuit operation. First, the CMOS implementation requires twice as many transistors as that of a bipolar or MESFET implementation. Secondly, N4 and P4 result in additional movement of the intermediate node of their respective inverter stages, and thus cause additional power dissipation. This problem was alluded to in the latter part of Section 3.3. When the input to transistor N1 is low this transistor is cutoff, and the pre-charged high intermediate node turns on the output transistor, N5. This node cannot be left high, however, because N5 would remain on and allow the inverter output to follow the AC

voltage source on the rising edge. Thus, the purpose of transistor N4 is to discharge the gate node of N5 (to prevent N5 from remaining on), only to see this node charged up again through transistor N3 on the rising edge of the waveform. The same problem occurs for the PMOS inverter stage, where P4 charges up the center node to prevent P5 from remaining on, while P3 then discharges this same node on the falling edge of the AC waveform.

Finally, these pre-charging transistors (N1, N4, P1 and P4) also keep the gate-to-source voltage of their adjacent transistor from rising much above the threshold voltage. Since MOS devices have only a square law dependence of current on gate voltage, this keeps the device from turning on very hard. The current-voltage relationship of a MOSFET operated in the linear region is given by:

$$I_{DS} = C_{ox} \cdot \mu \left(\frac{W}{L} \right) \cdot \left[(V_G - V_t)V_D - \frac{V_D{}^2}{2} \right]$$

In order for a positive gate-to-source voltage to be maintained for N2 and N5, the drain current for N1 and N4 must be significantly lower than that of N2 and N5 in order to prevent the gate capacitance from discharging faster than the drain capacitance. For a given technology, this is most easily accomplished by appropriately scaling the widths of the device. However, current scaling is also possible by altering the threshold voltage for these transistors.

3.4.1. DEVICE SCALING ISSUES

Although there are no specific design criteria for MOS devices being used in REL circuits other than the sizing restrictions mentioned above, there are several points to be made about device operation. First, since the power efficiency of REL circuits is proportional to $(V_t + V_{DS,on}) / V_{AC,peak}$, REL circuits fit in well with the trend of reducing threshold voltages with reducing power supply voltages. Any gate leakage current will simply add to the existing pre-charging currents, so REL does not suffer ill effects from the increase in off-state leakage currents, provided these leakage currents are not large enough to discharge the output capacitance. This is in contrast to mainstream CMOS logic circuits, which face

an increase in standby power consumption with increases in off-state leakage currents [22].

In addition, the devices see the peak drain-to-source voltage for only a short duration of the propagation cycle. Typical CMOS logic circuits see the full V_{DD} voltage across the device for the entire clock cycle. This should significantly reduce the high field stresses of the devices, improving the long term reliability of the devices from the stand point of hot electron effects, reducing the need for drain engineering techniques such as Lightly Doped Drains (LDD). This becomes increasingly important for short channel devices. Another potential benefit of MOS operation in REL circuits is that the circuit operation does not depend on the absolute value of the threshold voltage. Short channel effects such as Drain Induced Barrier Lowering (DIBL) are less important for REL circuits, provided that the threshold voltage remains greater than the on state drain-to-source voltage drop.

3.5. REL CMOS CIRCUIT SIMULATIONS

Circuit simulations using HSPICE™ have been performed for REL implemented in a 2 μm CMOS process, with a threshold voltage of 0.3 volts. This relatively long channel length was chosen in order to make a reasonable comparison to the non self-aligned bipolar transistors which are presented in Chapter 4. The device parameters are the actual parameters obtained from the 2 μm MOSIS process, except for the threshold voltage [32]. The threshold voltage was reduced to 0.3 volts to allow the circuit to operate at a lower supply voltage of 3.3 V_{p-p}. The circuit simulated is a ring of 4 inverters; 2 n-channel stages and 2 p-channel stages. The internal nodes of the circuit have been set such that each inverter changes its output every other cycle. This circuit is pictured in Fig. 3.2. Representative circuit outputs are shown in Figs. 3.3 and 3.4 for 1 MHz and 20 MHz operation, respectively. The sagging of the voltage is due primarily to the capacitive divider. The load capacitance of CMOS implemented REL circuits is usually the source/drain-to-substrate capacitance. This capacitance is typically about 10 *fF* for 2 μm processes. The parasitic gate-to-source and gate-to-drain capacitances are about 3 *fF*, so this operation is at the edge of the capacitive divider. If necessary, the load capacitance may be increased by increasing the area of the source and drain regions. Higher frequency operation results in more current being drawn due to increases in $C \cdot (\partial V / \partial t)$. This is

apparent in the larger V_{GS} drops across the pre-charging transistors, as shown in Fig. 3.4. The resulting power-delay product for REL circuits implemented in CMOS was 0.3 pJ for 1 MHz operation, and 0.4 pJ for 20 MHz operation. A more state-of-the art technology using 0.6 μm channel length devices were shown to perform up to 150 MHz, with a power-delay product of only 0.04 pJ [32].

It should also be noted that the supply voltage of REL circuits does not scale linearly with frequency, as with standard CMOS circuits. That is, a lower supply voltage does not necessarily reduce the maximum operating frequency through a constant relation. This is because the amount of charge that is delivered to the capacitance will also scale with supply voltage. So, although the currents are reduced, the amount of charge delivered to the capacitors will also be reduced consistent with the relationship

$$i(t) = C(V) \cdot \frac{\partial V}{\partial t} \approx C(V) \cdot \frac{\Delta V}{T/2}$$

where $C(V)$ indicates the voltage dependence of the load capacitance and ΔV the peak-to-peak voltage of the AC waveform.
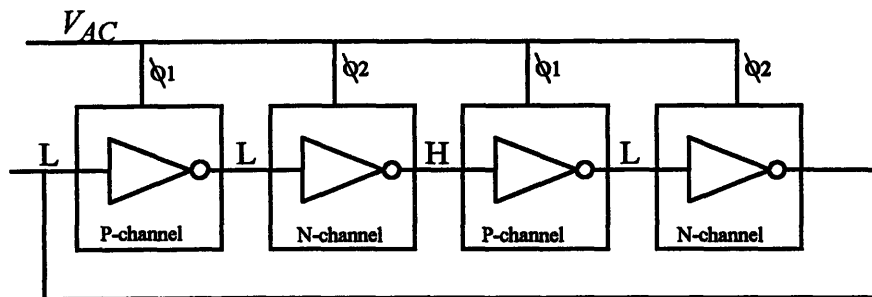
Figure 3.2: Circuit schematic for HSPICE simulations

CMOS Circuit Simulation

1 MHz, Cload = 10 fF
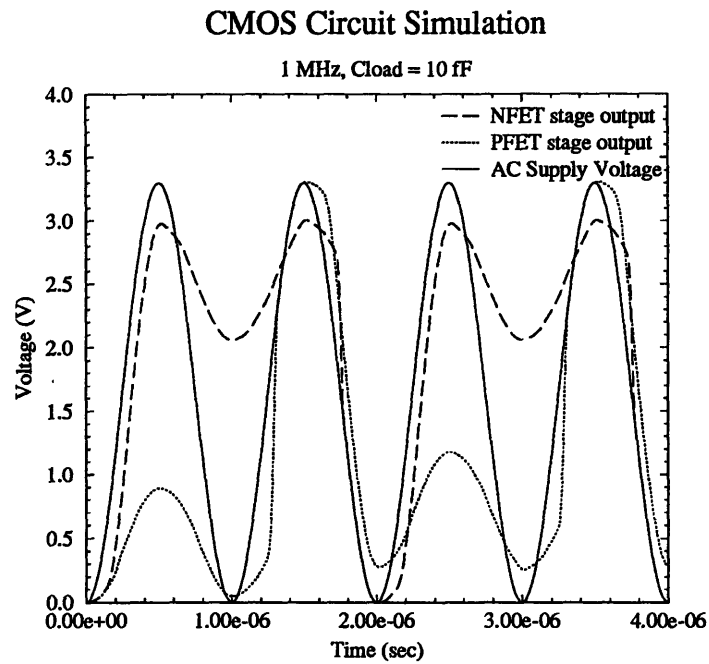
Figure 3.3: CMOS circuit simulation operated at 1 MHz, 10 fF load capacitance.

CMOS Circuit Simulation

20 MHz, Cload = 10 fF
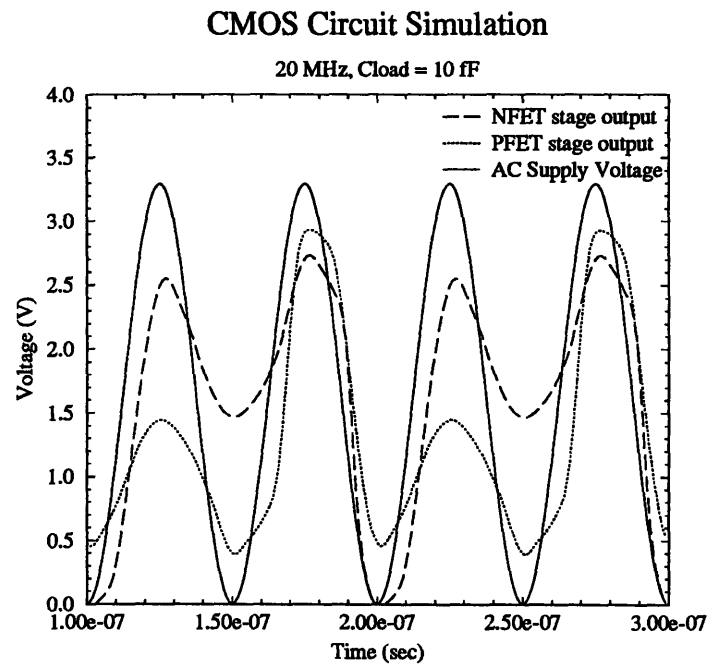
Figure 3.4: CMOS circuit simulation operated at 20 MHz, 10 fF load capacitance.

CHAPTER 4

SILICON BIPOLAR JUNCTION TRANSISTORS

4.1. INTRODUCTION

Bipolar transistors designed for REL circuit applications differ substantially from standard optimized bipolar transistors. This chapter will explore in detail the unique way in which Recovered Energy Logic circuits utilize bipolar transistors. A comparison will be made of implementing REL circuits in standard bipolar technology versus fabricating "inverted" transistors, whose emitters are the buried layer of the standard bipolar process. Finally, a detailed analysis of the device requirements of REL bipolar devices. In keeping with the trend of reducing supply voltages for low power operation, these designs are all done for a $3.3V_{p-p}$ supply voltage.

4.2. INVERTED VERSUS STANDARD BIPOLAR DEVICES

4.2.1. EMITTER-UP BIPOLAR TECHNOLOGY

The standard emitter-up configuration is used in all Advanced Bipolar processes today. Among the advantages of using a standard bipolar process are the well-established fabrication lines, and the excellent transistor characteristics available in silicon bipolar technology. However, REL circuits require that the base-emitter junction be able to withstand a significant reverse bias voltage without reaching breakdown. The typical base dopings of many bipolar processes can reach as high as 1×10^{18} cm^{-3}. For a highly doped emitter, this would result in a reverse breakdown voltage of less than 1 volt. In addition, the base region must be able to withstand two reverse biased junctions simultaneously. Advanced Bipolar processes which have base widths of less than 0.1 μm would not be

able to withstand this condition without punching through. Although the small lateral dimensions achieved in state-of-the-art bipolar processes would be very advantageous to REL circuits, the need for complementary devices in REL circuits will add significant complexity to a self-aligned bipolar technology. Finally, in a standard emitter-up bipolar process, the emitters of REL circuits would have to be connected in metalization, and a collector contact for each device brought to the surface. Individual device isolation is a limiting factor for integration density in this topology.

4.2.2. INVERTED BIPOLAR TRANSISTORS

Because of the complications apparent in realizing REL circuits in a standard bipolar technology process, an alternate process of building inverted bipolar transistor was examined in detail. The proposed cross-sectional diagram in shown in Fig. 4.1. Building the devices in this fashion has many advantages for the REL circuits. The circuit topology has all of the emitters tied together. For inverted bipolar transistors, where the emitter region is the buried layer, the devices become self-isolating. This is similar to Integrated Injection Logic (I^2L)circuits proposed by Hart and Slob in 1972 [4]. It is well known that inverted structures have poor device performance in comparison to emitter-up structures. The reduced gain is not a significant issue, since REL devices are operated in either the saturation or cutoff mode. In fact, a lower gain will help reduce the amount of charge stored in the base and decrease the recovery delay time of the saturated transistor. A gain of at least 2 is required in order to ensure that the transistor goes into saturation, more if fan-out is required. The slower base transit times are more problematic, along with the reduced current drive capabilities. The need for a small saturation voltage makes it desirable to more heavily dope the collector region, which forces more of the collector-base space charge region into the active base. This situation results in a trade-off between heavily doping the base region to reduce the depletion regions within the intrinsic base, and lightly doping the base region, to avoid high parasitic capacitances. Finally, the large area junction of the inverted transistors occurs at the base-emitter junction. This increases the parasitic capacitance of the device, requiring a larger load capacitance to avoid a capacitive divider. All of these issues will be examined in the remainder of this chapter.
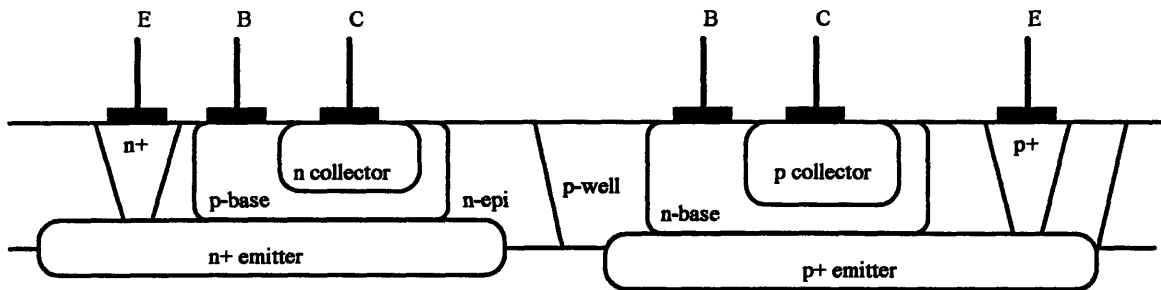
Figure 4.1: Cross section view of complementary REL inverter bipolar devices

4.3. DEVICE REQUIREMENTS

4.3.1. PARASITIC CAPACITANCES

The most difficult of the device requirements to meet in silicon bipolar transistor technology is the need for small parasitic capacitances. A typical load capacitance for a 2 μm CMOS process is about 10 fF. This capacitance is generally the source/drain-to-substrate junction depletion capacitance. The junction capacitances of bipolar processes are generally about 6 to 8 x 10^{-8} F/cm^2. For the inverted bipolar process, the large area junction is at the base-emitter junction. This tends to have a larger capacitance per unit area than the base-collector junction. As will be seen later in the chapter, a representative junction for REL bipolar process is a linear base-emitter junction, where the base is doped at roughly 2 x 10^{17} cm^{-3}, and the emitter is doped at 1 x 10^{18} cm^{-3}. This gives a zero-bias depletion capacitance of 1.6 x 10^{-7} F/cm^2. A total capacitance of 10 fF would be reached for an area of only 2 μm x 2 μm. In order to avoid the capacitive divider created by the parasitic devices and the load capacitance, the load capacitor would have to be at least 3 to 4 times this value. The speed advantages of REL circuits fabricated in bipolar technology versus CMOS must be carefully balanced against the increased $C \cdot V$ losses due to the increased parasitic capacitances.

4.3.2. REVERSE BREAKDOWN VOLTAGE

Although it is desirable to keep the doping in the regions low to reduce parasitic capacitances, there is also a limit on the doping in the more lightly doped base region due to the reverse bias condition at each of the junctions. Assuming both of these junctions to be nearly linear, the peak electric field across the junction is given by:

$$E_{peak} = \frac{q \cdot a}{2\varepsilon_{Si}} \left(\frac{w}{2}\right)^2$$

$$w = \left[\frac{12\varepsilon_{Si}}{qa} \cdot (\phi_{bi} - V_A)\right]^{1/3}$$

$a \equiv$ slope of linear junction, cm^{-4}

$w \equiv$ depletion region width, cm

For the linear junction example given above, the peak electric field for a reverse bias of 3.3V is approximately 3.3×10^5 V/cm. Simulated results given in Section 4.4 show this value to be closer to 2.8×10^5 V/cm.

4.3.3. PUNCHTHROUGH VOLTAGE

There are, however, reasons to keep the doping in the base relatively high. One of these is to avoid punchthrough when both junctions are reverse biased. A higher doping in the base region limits the extent of the depletion region into the base. This would allow a smaller base width for a given reverse bias condition. An important consideration is that the voltage across the base when both junctions are reverse biased is, at most, that of a diode drop. In order for there to be conduction from the emitter-to-collector under reverse bias, it is not sufficient for the depletion regions to simply meet. There still exists a substantial energy barrier from emitter to collector under this condition. For the example junction given previously and a base width of approximately 0.20 μm, a V_{CE} of more than 1.2V is needed in order to get conduction from collector to emitter with both junctions reverse biased at 3.3V. This is in spite of the fact that the depletion regions are clearly overlapping. With this in mind, the more stringent reverse bias condition is that of

the device operating in the forward active region, where the base-collector junction is heavily reverse biased and $V_{CE} \approx 3.3V$.

4.3.4. SATURATION VOLTAGE

Chapter 2 alluded to the fact that the energy efficiency of Recovered Energy Logic is in part dependent on the ratio of the sum of $V_{BE,on} + V_{CE,sat}$ to the peak AC voltage. It is therefore desirable to keep the saturation voltage as low as possible. This implies that the emitter and collector have similar doping levels. This is good news for an inverted bipolar process, since implanting the collector region into the base region assures that the collector must be more heavily doped than the base. This helps reduce the effects of high level injection in the collector region as well. It has the disadvantage of creating larger parasitic capacitances at the base-collector junction. However, this is not the large area junction of the inverted bipolar transistor, where the base-emitter junction capacitance is the limiting parasitic capacitance of the device.

4.3.5. HIGH LEVEL INJECTION

In addition to avoiding punchthrough, it is also desirable to keep the doping in the base relatively high in order to avoid high level injection in the base region. High level injection results in lowering the collector current, and hence the device gain, as well as increasing the stored charge in the base. Since REL relies on having all of the stored base charge recombine before the next clock phase, it is desirable to keep the minority carrier concentration in the base as low as reasonably possible. Because the buried layer emitter region is moderately doped at 1×10^{18} cm^{-3}, high level injection in the emitter region must also be considered in REL devices. This effect is not usually considered in standard bipolar processes, where the emitters are generally degenerately doped However, both effects must be considered in these inverted structures, as will be seen in the circuit simulations in Section 4.5. This effect will limit the maximum frequency that the circuit may operate under. The current drawn by the load capacitor will be determined by:

$$I_{max} = C_{load} \cdot \frac{\partial V}{\partial t} \approx C_{load} \cdot \frac{\Delta V}{T/2}$$

where ΔV is the peak-to-peak voltage of the AC supply, and $T/2$ is half of the AC waveform period. The maximum amount of charge that could be delivered is given by

$$Q_{max} \approx I_{max} \cdot \Delta t \approx C_{load} \cdot \Delta V$$

When this charge approaches the total stored minority carrier charge in the base, the conditions of low level injection will be violated, and the performance of the transistor will degrade. Assuming little recombination in the base region, the total stored charge in the base operated in the forward active region can be approximated as:

$$Q_{diff} \approx \frac{q n_i^2 w_B^*}{2 N_B} \cdot e^{q V_{BE}/kT}$$

where w_B^* is the effective base width, and N_B the doping concentration in the base. The amount of current drawn from the device will be dependent on the frequency of operation, and will in turn force the base-emitter voltage necessary to sustain this current. Thus, high level injection will limit the high frequency performance of these devices.

4.4. DEVICE SIMULATION AND LAYOUT

One possible configuration for the layout of complementary inverted silicon bipolar devices was shown in Fig. 4.1. The two buried n^+ and p^+ regions serve as the respective emitters of each device. These will be connected in metalization through contacts periodically brought to the surface of the wafer. Although only one base region is shown, devices fabricated in this fashion are self-isolating, and multiple base regions can be contained in a single emitter region. Not shown in this figure is the load capacitance contacting the collector. Since there is no parasitic junction capacitance available to implement the load in this configuration, it is necessary to implement the load explicitly on the surface of the wafer.

Based on the design criteria outlined in Section 4.3, idealized devices were simulated using Technology Modeling Associates (TMA) MEDICI™ software. MEDICI is a two dimensional, two carrier semiconductor device modeling program which simulates the electrical behavior of devices under steady state or transient conditions. The program solves Poisson's equation and the continuity equations self consistently for the electrostatic potential and electron and hole concentrations. These equations are discretized on a simulation grid, resulting in a set of coupled, nonlinear algebraic equations, which are then solved by a nonlinear, iterative method. MEDICI was used to identify to best device doping profiles for optimized transistor performance. The device profiles used for these simulations were generated by MEDICI through PROFILE statements. Examples of the input files used to generate these devices appear in Appendix A. The resulting device profiles are shown in Figs. 4.2 and 4.3. The device characteristics are summarized in Table 1.

TABLE 4.1.

Bipolar Device Parameters for MEDICI Simulations

(all dimensions in per unit width)

Device Parameter	NPN Transistor	PNP Transistor
Saturation Current, I_s (A/μm)	3×10^{-17}	1.6×10^{-17}
C_{BE0}(F/μm)	7.3×10^{-15}	7.20×10^{-15}
C_{BC0}(F/μm)	4.1×10^{-15}	4.40×10^{-15}
Base Width (μm)	0.21	0.22
Transit Time (sec)	1.8×10^{-11}	2.6×10^{-10}
Maximum f_t (GHz)	1.9	0.98
Peak β / High Current β (A/A)	55 / 12.9	79 / 3.3
Peak Electric Field (V/cm)	2.8×10^5 @ 3.3 V	2.8×10^5 @ 3.3 V
Punchthrough Voltage (V)	5.2	4.7

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NPN Silicon Device Doping Profile
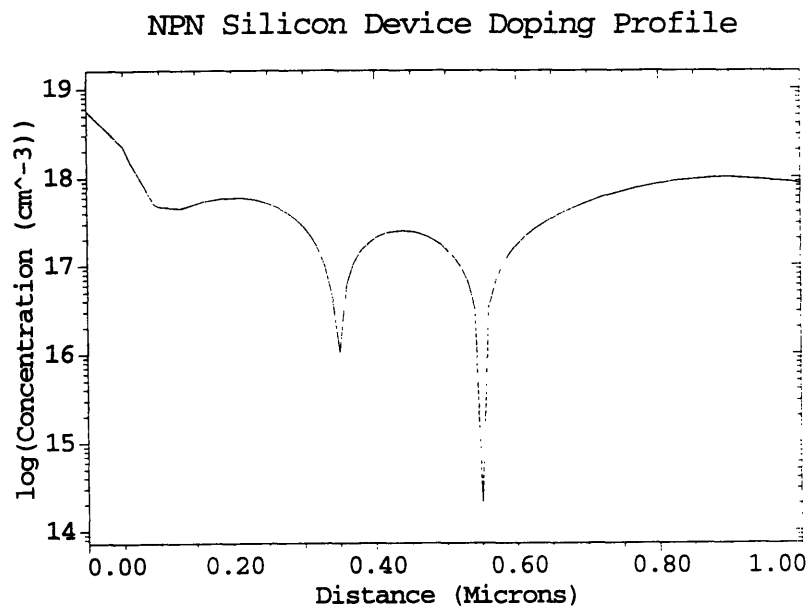
Figure 4.2: NPN MEDICI simulated device doping profile

PNP Silicon Device Doping Profile
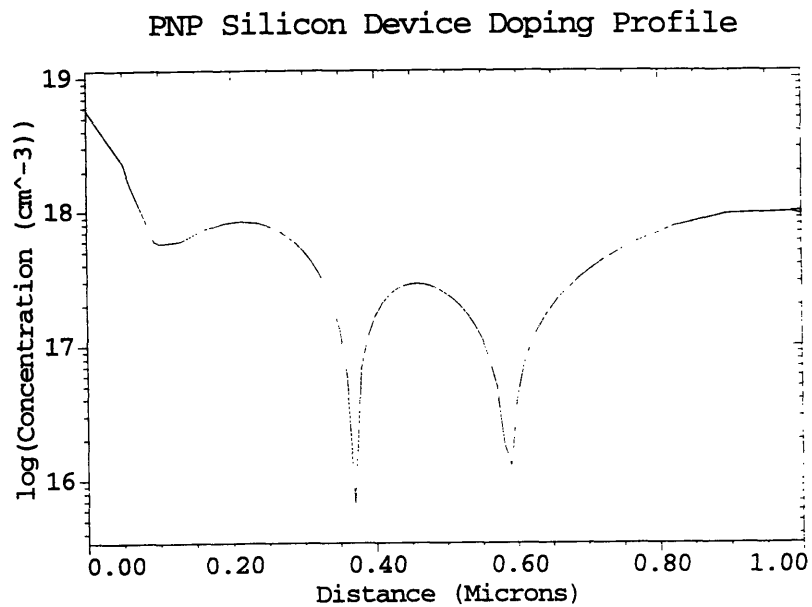
Figure 4.3: PNP MEDICI simulated device doping profile

The Gummel plots for these devices appear in Figs. 4.4 and 4.5. Note that there is a tailing-off of the base current as well as the collector current at high values of base-emitter voltage. This indicates that high level injection in the emitter region is occurring. This is due to the relatively lightly doped buried emitter regions. This region was doped lightly for two reasons. The first is that high gains would result in an increase in the amount of charge stored in the base during device saturation, and thus slow down the operation of the circuits. The second reason is that a highly doped buried p^+ region is very difficult to achieve. The high diffusivity of boron in silicon makes it difficult to maintain a confined buried layer at high doping levels. Therefore, the emitter dopings were intentionally kept light to try to simulate plausible device profiles. These issues are explored in detail in Chapter 5. Also apparent in Fig. 4.5 is the non-ideal behavior of the collector current of the pnp device.
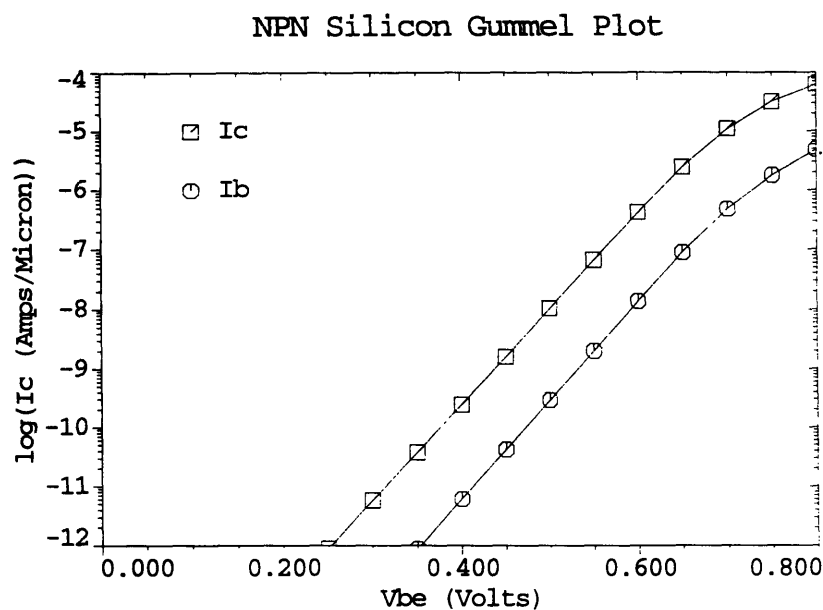
Figure 4.4: NPN MEDICI simulation: $\log(I_C)$ and $\log(I_B)$ vs. V_{BE}

PNP Silicon Gummel Plot
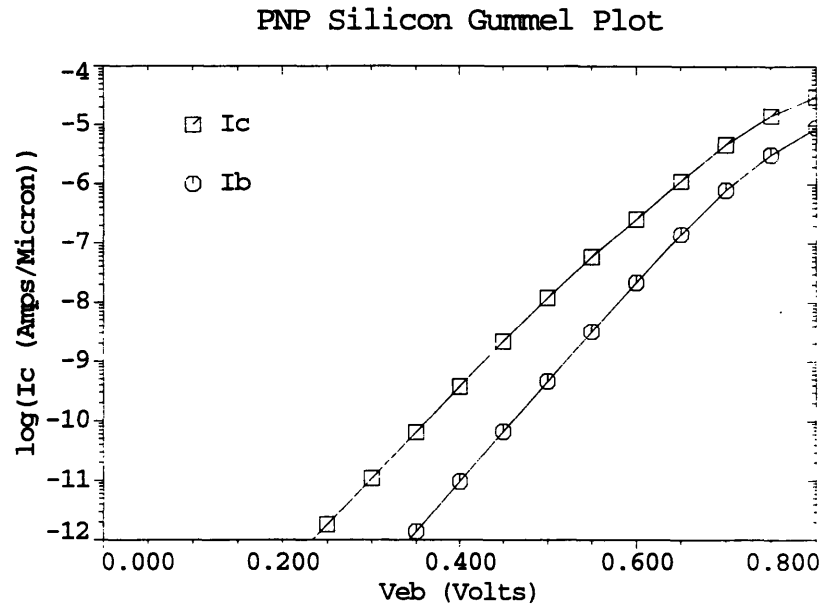
Figure 4.5: PNP MEDICI simulation: $\log(I_C)$ and $\log(I_B)$ vs. V_{EB}

The MEDICI simulations create only two-dimensional device profiles, with all parameters given in per unit width. In order to extract actual device parameters, the layout of the device must be considered. Figure 4.8 shows the top view of a bipolar transistor. The fabrication technology is assumed to be 2 μm x 2 μm contact windows and minimum dimensions, with 0.5 μm registration between mask layers. This results in a base-collector junction area of 3.5 μm x 3 μm, and a base-emitter junction area of 4μm x 7.5μm. Thus, the base-collector capacitance values extracted from MEDICI must be scaled by a factor of 3, and the base-emitter capacitance values must be scaled by a factor of 4 (the lateral dimensions are accounted for in the two dimensional simulation). This gives base-emitter capacitance values of nearly 20 *fF*. In order to avoid the effects of the capacitive divider between the parasitics and the load capacitance, the load capacitor should be at least 80 *fF*. This is in contrast to the 10 *fF* load of the CMOS circuits. This represents a serious limitation to the energy savings of REL circuits implemented in bipolar technology over standard CMOS logic.
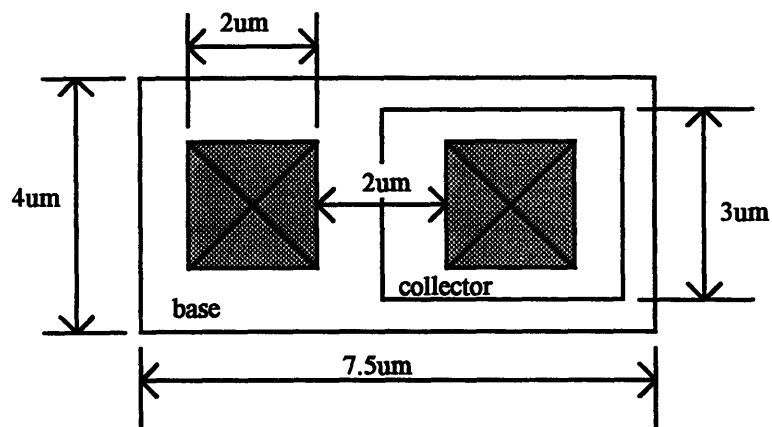
Figure 4.6: Device Layout for REL Inverted Bipolar Transistors

4.5. CIRCUIT SIMULATIONS

Using the devices simulated with the MEDICI software tool, device parameters were extracted for circuit simulation using HSPICE™. The full device models appear in Appendix B. Figures 4.7 and 4.8 show a comparison between the Gummel plots of the MEDICI simulated devices, and the *I-V* characteristics generated from the HSPICE models. There are significant differences in the behavior of the base current between the MEDICI simulations and the HSPICE devices. This is due primarily to the inability to model high level injection in the emitter region with HSPICE. As a result, the high level gain of the npn transistor is significantly less than that of the MEDICI simulated devices. This, however, should not significantly effect the circuit simulations since the gain is still higher than that of the PNP devices. Also noted are the extremely non-ideal characteristics of the pnp devices. The ideality factor of the base-emitter diode for these devices is 1.17. Because of this, it is difficult to assess the accuracy of the HSPICE circuit simulations.

In order to estimate the circuit performance of the bipolar devices, an inverter chain of two n-type and p-type stages was simulated. This is the same circuit that was used for the CMOS simulations. The load capacitance used for these simulations was 80 *fF*. Simulations for the circuit with an AC supply frequency of 20 MHz and 50 MHz are shown in Figs. 4.9 and 4.10. The circuit performance has degraded substantially for the

50 MHz operation. The primary degradation mechanism is due to high level injection in the PNP devices. This causes a reduction in the gain of the transistors, and the PNP devices no longer go into saturation. As seen in Fig. 4.10, the PNP output nodes fail to be pulled all the way to the AC rail. This is one area in which HSPICE may not do a good job in simulating, since HSPICE includes no mechanism for the accompanying reduction in base current due to high level injection in the emitter region as well.

An average power calculation was made by finding the total power for all four stages and dividing by four. This gave power-delay products for the bipolar REL circuits of 0.8 pJ for the 20 MHz simulation, and 0.9 pJ for the 50 MHz simulation. This is in comparison to REL circuits implemented in CMOS technology of 0.3 pJ, which had a load capacitance of only 10 *fF*.
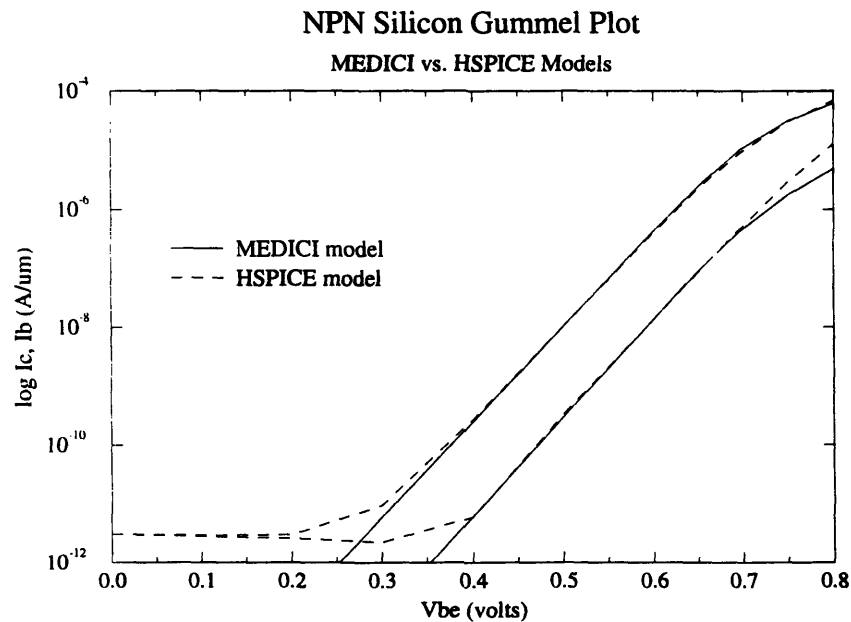
Figure 4.7: NPN Gummel plots for HSPICE and MEDICI models
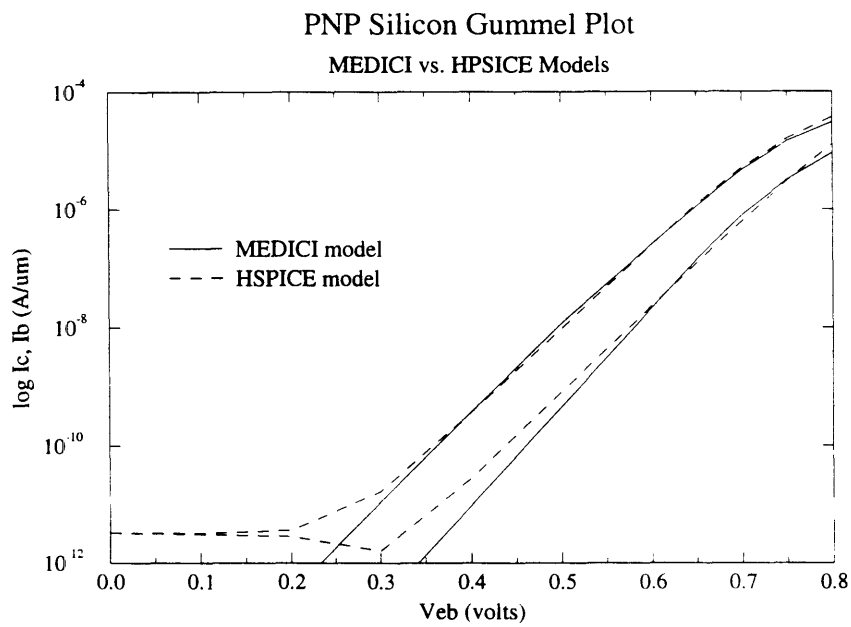
Figure 4.8: PNP Gummel plots for HSPICE and MEDICI models
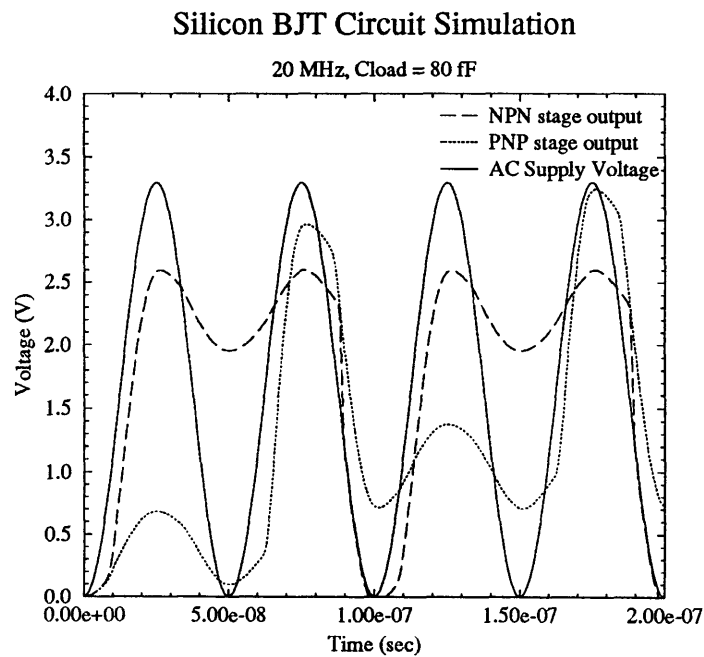
Figure 4.9: BJT circuit simulation operated at 20 MHz, 80 fF load capacitance.

Silicon BJT Circuit Simulation

50 MHz, Cload = 80 fF
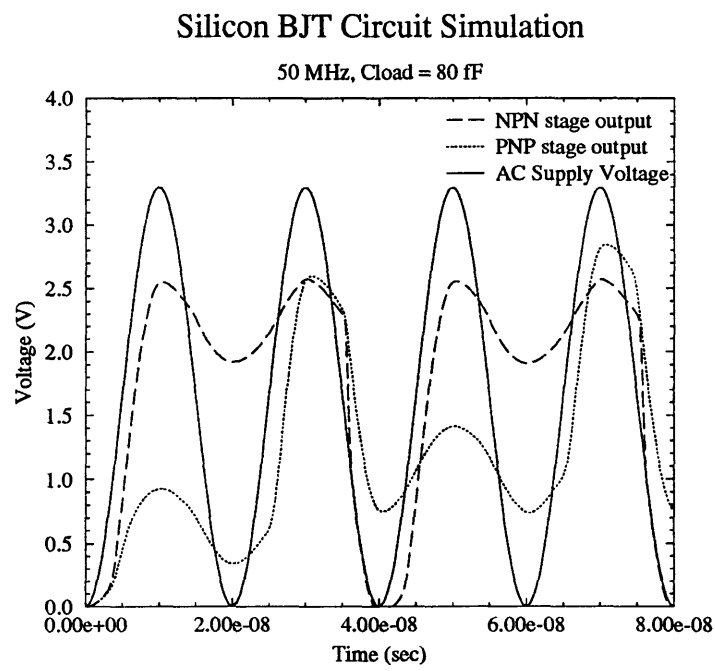
Figure 4.10: BJT circuit simulation operated at 50 MHz, 80 *fF* load capacitance.

CHAPTER 5

SILICON BIPOLAR TRANSISTOR PROCESS DESIGN

5.1. INTRODUCTION

As part of the effort of this thesis, a fabrication process for inverted bipolar transistors was designed. Unlike MOSFET fabrication lines, existing methods of fabricating silicon bipolar transistors are unacceptable for Recovered Energy Logic circuits. This is primarily due to the reverse bias conditions on the base-emitter junction. However, as outlined in the beginning of Chapter 4, there are several issues that make standard bipolar devices poor candidates for REL circuits.

The design process outlined in this chapter is for a non self-aligned process. As seen from the circuit simulations in Chapter 4, the parasitic capacitances of bipolar devices are quite large. It would be extremely helpful from a circuit perspective to fabricate the bipolar transistors in a self-aligned process in order to minimize the size of the devices, and hence the parasitic junction capacitances. Many self-aligned processes for npn transistors have been reported on with great success [23,24]. Devices fabricated in this fashion have achieved base-emitter contact areas as small as 0.35 μm x 1.2 μm, in standard emitter-up devices. The width of the entire device is only 1.6 μm. The reported parasitic capacitances for these devices are less than 2 fF per unit width. However, no literature has been reported on a self-aligned complementary process, although several complementary vertical bipolar processes have been reported [21]. Unfortunately, these processes are all designed for optimum device performance when operated in the forward active regime. Base widths are often 0.1 μm or less in order to achieve f_t's in the tens of GHz range. These extremely small base widths could never withstand two reverse biased junctions. In fact, the base and emitter regions of these devices are so heavily doped that even a small reverse bias causes the junction to breakdown.

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In order to fabricate bipolar devices specifically tailored to the needs of REL circuits, an entirely new fabrication process is proposed. The results of this new design are presented in the remainder of the chapter. Finally, the last section of the chapter explores other approaches to REL device fabrication

5.2. DESIGN METHODOLOGY

5.2.1. EMITTER REGION

It has been established earlier that the buried layer of the bipolar structure shall serve as the emitter region for REL bipolar transistors. Typically, the buried layer is implanted into the starting substrate wafer, and then an epitaxial layer is grown on top of this substrate. This method lends itself especially to n^+ buried layers, because n-type dopants have a relatively slow diffusivity in silicon. There are necessarily several high temperature processing steps that occur after the buried layer implantation which cause this buried layer to diffuse up into the intrinsic region of the device. Creating a p^+ buried layer through this method is less effective. The high diffusivity of boron in silicon causes the buried layer to diffuse substantially into the device region. This junction can easily move more that 1 μm. Considering that the base-emitter junction must be deep enough to include the collector region within the base, along with a collector contact implant, this is a considerable problem. In addition, the profile is often so broad after that much movement that the buried layer is not an effective emitter region.

As an alternative to this fabrication method, the use of high energy implants has also been explored. High energy implantation machines are capable of reaching implant energies of up to 1 or 2 MeV, with doses ranging as high as 1 x 10^{15} cm^{-2}. Most low current machines can only comfortably reach 180 keV, possibly 200 keV energy implantations. This technology adds significant flexibility to the design of PNP devices. The PNP emitter can then be implanted as a high energy implant at the end of the process, providing a relatively narrow peak of acceptors more than 0.6 μm under the silicon surface. A major consideration then becomes annealing out the damage of this high energy implant. A significant portion of the damage sites will be within the active device area.

5.2.2. BASE REGION

Simulated devices using MEDICI show that the base region can be as thin as 0.22 μm without having the device punchthrough under reverse bias conditions of -3.3 V at both junctions. As stated previously, this condition only occurs when the output of the device is left in its pre-charged state, which should be roughly one diode drop below (or above) the peak AC supply voltage. The target base widths for the REL complementary bipolar process were 0.22 μm to 0.25 μm. The location of the base-emitter junction must also be relatively deep when one considers that the base region must contain the collector region and the collector contact implant. It is important that the collector region have a sufficient amount of distance between the base junction and the p^+ implant. Otherwise, the collector region will effectively be the contact implant. This has the undesirable effects of increasing the junction capacitance, forcing the space charge region into the intrinsic base, and increasing the peak electric field when the junction is reverse biased.

The use of high energy implants also allows greater flexibility in the location of the base region for PNP devices. Once again, this is not a problem for NPN devices, since the projected range of boron implantations into silicon is approximately 0.5 μm for 180 keV energy implants. For the NPN devices, the base-emitter junction can easily reach 0.6 μm without the use of high energy implants. Phosphorus has a projected range of only 0.25 μm as implanted into silicon at an energy of 200 keV. This significantly limits the depth of the base-emitter junction, and hence the depth available for the collector region. The use of a high energy implantation in forming the n-base region of the PNP devices greatly eases the constraints of the process design.

5.2.3. COLLECTOR REGION

The purpose of the collector region is simply to collect minority carriers transported across the base. It is generally kept lightly doped to reduce parasitic capacitances and to allow the space charge region to expand into the collector region rather than the base region. The latter effect helps to reduce the base width modulation, or Early effect, of the

transistor operated in the forward active region. Since neither of these is a major concern in REL, there is much more latitude in the design of the collector regions of these devices. It should be pointed out that although it is certainly desirable to keep the parasitic capacitances of these devices small, the large area base-emitter capacitance will dominate in the inverted bipolar structure. The Early effect is not an issue for REL circuit operation since the devices will be driven in either saturation or cutoff. Therefore, the major consideration in design the collector of REL bipolar transistors is to reduce the $V_{CE,sat}$ voltage drop. This suggests that the collector should be doped comparable to the emitter. However, since we would like to be able to drive the transistor into saturation rather easily, the built-in potential of the base-collector junction should not be too large. There is a trade-off between the on-state voltage of the base-collector diode and keeping the $V_{CE,sat}$ drop as small as possible. A good compromise is for the collector doping to be somewhere between the base and emitter doping levels. Considering that the emitter region is not doped extremely highly, this is a relatively narrow range.

5.3. PROCESS DESIGN RESULTS

The resulting process design for fabricating REL inverted bipolar transistor is listed in detail in Appendix C. This section will cover the most important process steps, and go over the differences between the process as designed with and without the use of high energy implantations. These recipes were loosely based on the existing BiCMOS process used in the integrated circuits laboratory at MIT's Microsystems Technology Laboratory [19].

5.3.1. HIGH ENERGY ION IMPLANTATION PROCESS

In the high energy process, only the n^+ buried layer is implanted before the n-epitaxial layer is deposited. The n^+ buried layer for this process is formed with an phosphorus implant of 5×10^{14} cm^{-2} at an energy of 35 keV. Following the emitter drive-in diffusion, the wafer is then stripped and a 1.7 μm n-type epitaxial layer is grown. The p-well implant for the high energy implantation process is slightly different than that of the previous recipe, using two implants to sufficiently cover the device region. After performing the

field implants, a 0.5 μm LOCOS isolation is grown at 950°C for 150 minutes in a wet oxygen ambient, with an additional 180 minutes in an inert ambient. The n-type base of the PNP transistor is then implanted at an energy of 500 keV, with a dose of 3×10^{13} cm^{-2}. Following this implant, the p base of the NPN transistor is implanted at 170 keV with a dose of 2×10^{13} cm^{-2}. Both of these implant include accompanying shallower implant to ensure that the wide extrinsic base regions extend all the way to the surface of the wafer. The base implants are then driven in with a 120 minute diffusion at 950°C in a nitrogen atmosphere.

Next, the collectors for each device are implanted. The NPN collector is first, with a phosphorus implant at a dose of 4×10^{13} cm^{-2} and an energy of 200 keV. This relatively high energy is necessary in order reduce the intrinsic base width of the NPN device. Following this implant, the PNP collector is implanted with boron with a dose of 2.5×10^{13} cm^{-2} at 160 keV. Again, each implant has an accompanying shallow implant to ensure that the collector region reaches the wafer surface. In this process, the collector area would actually be larger than the collector contact area. If the collector area is limited to only the contact region, then the shallow implants would not be necessary. Finally, the entire PNP active device area, including all bases within a single p-type tub, is opened up for the PNP emitter implant. This implant would be done at an energy of 600 keV, with a boron dose of 7×10^{13} cm^{-2}. The subsequent emitter drive and anneal is done at 975°C for 100 minutes. Whether this would be sufficient time to anneal out all of the damage from such a high energy could only be determined experimentally. Finally, the contact implants are performed, along with back-end processing such as BPSG deposition and metalizations. None of these process steps is done at high enough temperatures to significantly affect the device profiles.

5.3.2. LOW ENERGY ION IMPLANTATION PROCESS

The low energy ion implantation process contains no ion implantation steps above 200 keV. This is within the range of the most common low current ion implanters, such as the one available in the Integrated Circuits Laboratory at MIT's Microsystems Technology Lab.

Restricting the process to ion implantations below 200 keV means that both the n^+ and p^+ buried layers must be implanted prior to epitaxial growth. Typically, n^+ buried layers are formed with arsenic or antimony as the implanted species. Since these atoms are relatively slow diffusers in silicon, this keeps the buried layer from significantly diffusing into the active device region. However, we would like the NPN and PNP devices to be well matched. Since the PNP buried layer is restricted to boron, phosphorus was chosen to form the buried layer in the low energy process, since its diffusion constant is better matched to that of boron. The two buried layers were formed in a self-aligned process. First a stress relief oxide is grown, and then a layer of silicon nitride deposited. The nitride and oxide are etched away from the n^+ buried layer region, and the phosphorus is implanted. The n^+ buried layer is implanted with a dose of 5×10^{14} cm^{-2} at an energy of 35 keV. Following this, a second oxide is grown over the exposed p-region. The nitride layer is then stripped to expose the p^+ buried layer area. The p^+ buried layer boron implant dose is 3×10^{14} cm^{-2} at an energy of 30 keV.

Following the buried layer formations, an n-type epitaxial layer is deposited with a doping of 5×10^{15} cm^{-3}. P-wells must be formed over the p^+ buried layer in this n-epi to make the PNP devices self-isolating. The p-well implantation dose is 3×10^{12} cm^{-2} at an energy of 200 keV. Also included are n- and p-field implants. This is to ensure that the areas under the LOCOS isolation do not become inverted due to MOS action from metal lines that may run over the top of the LOCOS [19]. The LOCOS is then grown in a long diffusion cycle of 150 minutes at 950°C in a wet oxygen ambient, with another 180 minutes in an inert nitrogen ambient. The resulting oxide thickness is approximately 0.5µm.

Following the LOCOS diffusion, windows are opened up to form the bases of the devices. The n-base of the PNP transistor is formed first. The base is formed by a phosphorus ion implantation of 5×10^{13} cm^{-2} at an energy of 200 keV. The implantation is done through a thin oxide to prevent tunneling of the implanted species within the silicon. This damage from this implantation is then annealed, and a second oxide is grown for the implantation of the NPN base. The NPN base is formed with a boron implantation of 2×10^{13} cm^{-2} at 170 keV. The base drive-in cycle is 120 minutes at 950 °C in a nitrogen atmosphere. The resulting base-emitter junctions after this drive in are 0.34 µm for the PNP device, and 0.4 µm for the NPN devices.

The collector regions are formed last in the low energy implantation process. The NPN collector is formed with a phosphorus implant of 4×10^{13} cm^{-2} at an energy of 200 keV. The NPN collector drive-in cycle is 100 minutes at 975°C in a nitrogen ambient. The PNP collector region is then implanted with 4.4×10^{13} cm^{-2} boron at an energy of 85 keV. The anneal of the PNP collector will occur with the polysilicon deposition step, which done at 925°C. The final process steps are the contact implants. The p$^+$ contacts are formed with a boron implant of 1×10^{15} cm^{-2} at 30 keV, while the n$^+$ contacts are formed with a phosphorus implant of 1×10^{16} cm^{-2} at 35 keV.

5.4. PROCESS SIMULATION RESULTS

Each of the processes described earlier was simulated using SUPREM III, a one-dimensional process simulation software package developed at Stanford University. SUPREM III has been used to simulate diffusions in both inert and oxidizing ambients, ion implantations, epitaxial growth and etching of various materials. Its use is mainly in determining the resulting carrier profiles of a given process, and thicknesses of material layers if so desired. In this work, it was used solely to predict carrier concentration profiles.

5.4.1. HIGH ENERGY ION IMPLANTATION PROCESS RESULTS

The cross sections of devices simulated using ion implantation energies of up to 600 keV are shown in Figs. 5.1 and 5.2. These devices are quite close to the target device profiles shown in Figs. 4.2 and 4.4. The collector regions for the SUPREM III simulated devices are actually longer than those of the MEDICI simulations. This should only add a small amount a parasitic resistance to the structure, since the collector region is relatively heavily doped. Otherwise, the base and emitter profiles of the two simulations are quite similar.

5.4.2. LOW ENERGY ION IMPLANTATION PROCESS SIMULATIONS

The resulting PNP device doping profile of SUPREM III simulations of the REL inverted bipolar process using only ion implantation energies of 200 keV or below is shown in Fig. 5.3. There is no difference in the NPN device design. In comparison to the target device profiles developed in MEDICI, we can see that the base region is much closer to the wafer surface.

Silicon NPN Device Doping Profile

SUPREM III Simulation
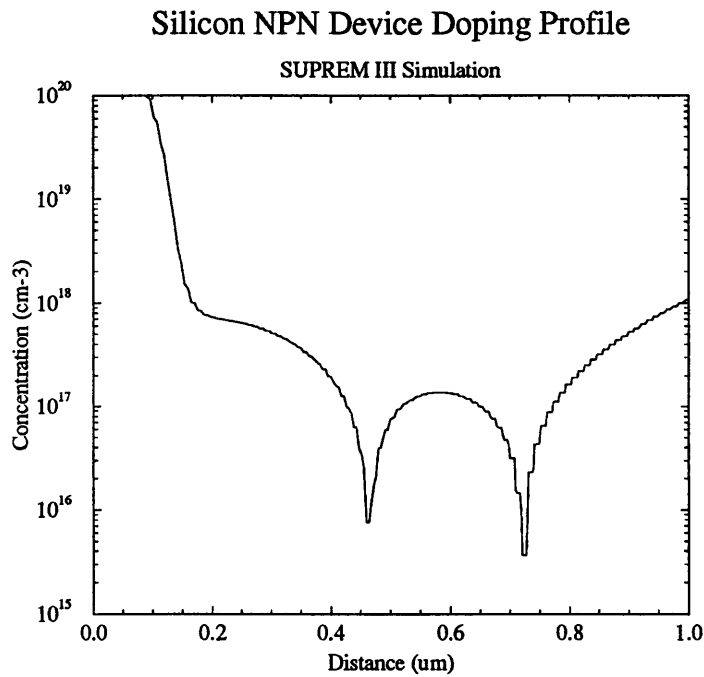
Figure 5.1: NPN device profile for REL inverted bipolar process using high energy ion implantations, SUPREM III simulation

Silicon PNP Device Doping Profile

SUPREM III High Energy Ion Implantation Simulation
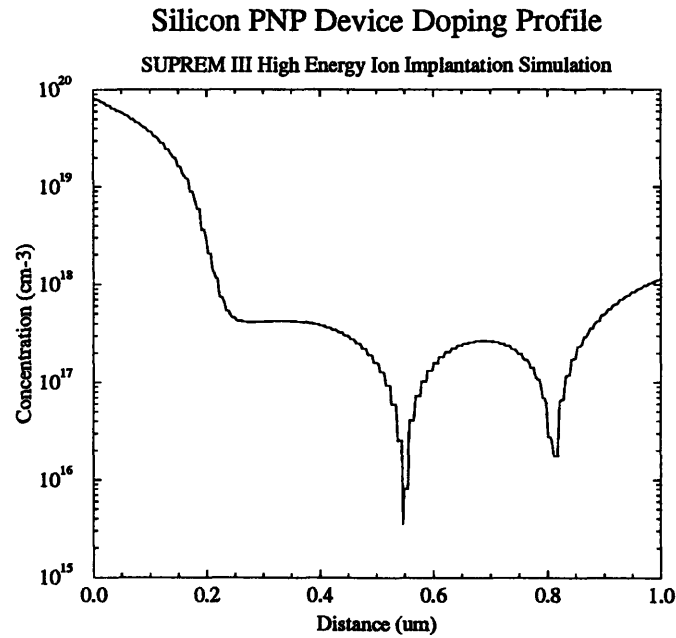
Figure 5.2: PNP device profile for REL inverted bipolar process using high energy ion implantations, SUPREM III simulation

Silicon PNP Device Doping Profile

SUPREM III Low Energy Ion Implantation Simulation
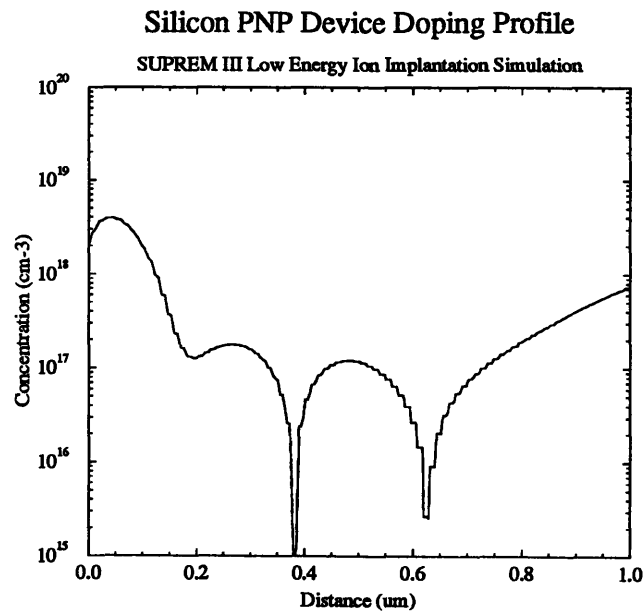
Figure 5.3: PNP device profile for REL inverted bipolar process using low energy ion implantations, SUPREM III simulation

5.5. ALTERNATE FABRICATION TECHNIQUES

Another possible technique for fabricating inverted bipolar transistors is the use of bonded wafer technology [30]. In this technology, the handle wafer could be processed with relatively shallow emitter and base implants. This would allow careful control of the doping profiles and junction depths. Another wafer could then be bonded onto the handle wafer, etched back and planarized to form the collector regions. This would require precise placement of alignment marks so that the location of the base region of each device could be known. Secondly, the bonded region would be within the base of the devices. Problems still exist in the quality of the bonded interface. A poor quality interface within the base region could result in significant increases in carrier recombination within the base. The main effect of this would be a reduction in the base transport factor, and hence a decrease in the overall gain of the device. Depending on the magnitude of the recombination current, this may or may not be a problem for REL devices, since high gains are not necessarily important. It may actually aide in the reverse recovery time of the saturated transistors by providing additional recombination sites. This is not unlike the intentional introduction of recombination sites in transistors designed for high speed switching applications.

CHAPTER 6

SILICON MESFET TRANSISTORS

6.1 INTRODUCTION

The possibility for using silicon MESFETs for implementing Recovered Energy Logic circuits is quite promising. The most common use of MESFET devices is as depletion mode devices, which are normally conducting, and a negative applied voltage is necessary to turn the device off. Silicon MESFETs as enhancement mode devices have gone largely unused, mainly due to the relatively low Schottky barrier gate materials available for contacting n-type silicon. It is even more difficult to find materials which form a suitably high barrier height when contacting p-type silicon. However, previous enhancement mode MESFET applications have focused on trying to operate within the small voltage range between the threshold voltage and the Schottky gate-to-channel forward voltage. Recovered Energy Logic uses enhancement mode devices in an entirely different way. The Schottky gate will actually be forward biased for part of the logic cycle.

6.2. METAL-SEMICONDUCTOR FIELD EFFECT TRANSISTORS

Since Metal-Semiconductor Field Effect Transistors, or MESFETs, are not commonly used, a quick review of the device operation is in order. Qualitatively, MESFET operation is quite similar to the more familiar MOSFET. However, in MOSFETs one applies a voltage to the gate to invert the region under the gate, thereby creating a channel for current conduction between the source and the drain regions. In MESFET devices, the source, drain and channel regions are all of the same type. The device is off when the region under the gate is depleted of carriers. In an enhancement type device, the channel region is fully depleted with no voltage on the gate. In this case, the channel region must

be thin enough that the built-in potential difference between the semiconductor and the metal gate is sufficient to fully deplete the channel. In a depletion mode device, a negative voltage is applied in order to increase the depletion region under the gate, assuming the device to be an n-channel device. A positive voltage would be applied to the gate of a p-channel device in order to deplete the channel.

Quantitatively, the current in a MESFET can be found by neglecting the diffusion component of the current, giving:

$$J_y = q\mu_n n E_y = -q\mu_n n \frac{\partial V}{\partial y}$$

Integrating over the cross sectional area, the current I_D is found to be

$$I_D = 2aW\mu_n n \frac{\partial V}{\partial y}(a - X_{SCR})$$

where a is the width of the channel, and X_{SCR} is the width of the space charge region extending into the channel. The functional dependence of the space charge region width on the applied voltage is simply that of a one-sided p$^+$-n junction:

$$X_{SCR} = \sqrt{\frac{2\varepsilon_{Si}}{qN_D}(\phi_{bi} - V_A)}$$

Integrating the current over the channel length gives the current-voltage relationship of the MESFET as:

$$I_D = 2q\mu N_D a \frac{W}{L}\left\{ V_D - 2/3(\phi_{bi} - V_t)\left[\left(\frac{V_D - \phi_{bi} - V_G}{\phi_{bi} - V_t} \right)^{3/2} - \left(\frac{\phi_{bi} - V_G}{\phi_{bi} - V_t} \right)^{3/2} \right] \right\}$$

operating in the region below the drain saturation voltage. In this equation, V_t is the threshold or pinchoff voltage; the gate voltage necessary to create a channel. When drain voltage reaches the saturation voltage given by

$$V_{D,sat} = V_G - V_t$$

the current has the same square law dependence on the voltage as that of the MOSFET and can be expressed as

$$I_{D,sat} = I_{D0}\left(1 - \frac{V_G}{V_t}\right)^2$$

With the function of MESFET devices understood, the circuit operation will be analyzed to assess the device requirements for REL circuits.

6.3. MESFET CIRCUIT OPERATION

The operation of REL circuits implemented in MESFET technology is quite similar to that of bipolar devices. The n-channel inverter stages will propagate their output on the falling edge of the AC waveform, while the p-channel stages propagate their output on the rising edge of the waveform. An REL circuit implemented with silicon MESFETs is shown in Fig. 6.1.
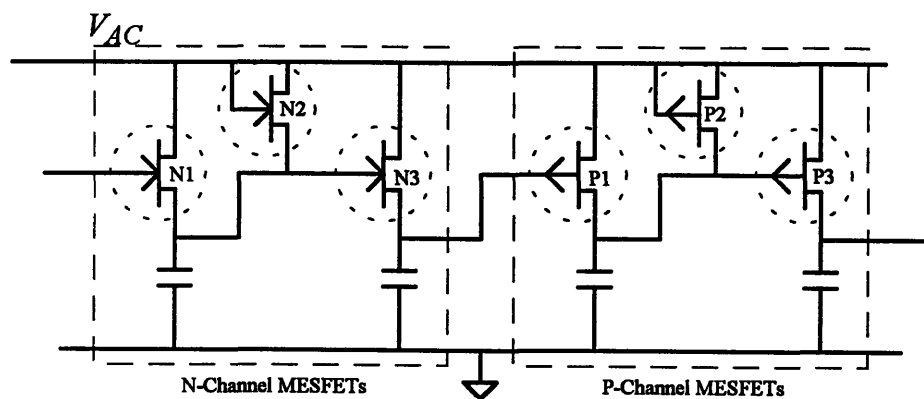
Figure 6.1: REL Inverter stage implemented with MESFETs

6.3.1. MESFET PRE-CHARGING OF OUTPUT NODES

The pre-charging of output nodes in REL MESFET circuits is accomplished through the gate diode. Transistors N1 and P1 will pre-charge the output of the preceding opposite polarity stage. Looking at transistor N1, the rising edge of the AC waveform will cause the Schottky gate diode to become forward biased, discharging the output node of the preceding p-channel stage to the lowest point in the AC waveform plus the diode drop of the Schottky-to-n-type silicon diode. This diode drop could be comparable to that of the silicon base-emitter diode in the bipolar devices, although it may be lower depending on the barrier height of the Schottky contact. This issue will be examined in detail in Section 6.2.1 of this chapter. Had this node been low, no additional pre-charging would have been necessary. Similarly, the Schottky gate of transistor P1 will become forward biased on the rising edge of the AC supply voltage. This will charge up the output of the preceding n-channel stage, minus the drop of the Schottky diode formed by the metal-to-p-type silicon contact.

The intermediate nodes of the inverter stages will be pre-charged by the diode connected transistors N2 and P2. On the rising edge of the AC waveform, the Schottky gate of the diode connected N2 transistor will become forward biased with respect to the intermediate node of the n-channel stage. The diode will charge up this node to the peak AC supply voltage, minus the drop across the forward-biased diode. The pre-charging of the intermediate node of the p-channel stage is accomplished by forward biasing the gate of the diode-connected transistor P2 on the falling edge of the AC source. The p-channel center node will be discharged to the lowest point in the waveform, plus the diode drop across the forward biased Schottky gate diode.

6.3.2. INVERTER OPERATION

On the rising edge of the AC supply voltage, the p-channel inverter stage will be active. We shall consider the AC rail to be the source of transistor P1. If the input to P1 is a low voltage, then this transistor will turn on as soon as the V_{GS} voltage becomes more negative than the threshold voltage (or pinchoff voltage), V_t. This transistor will the charge up the drain capacitor to the AC supply voltage, keeping the gate-to-source

voltage of the second transistor, P3, at zero. The output node will remain at its pre-charged value of the Schottky diode (metal to n-Si junction) forward voltage. Had the input to P1 been high instead, then this transistor would have been cutoff, allowing P3 to turn on. The output would then charge up to the peak AC voltage, minus the voltage dropped across the on-state transistor.

On the falling edge, the n-channel stages will be active. If the input to N1 is a high voltage, then this transistor will turn on as soon as the AC voltage falls below the gate voltage by V_t. This will then turn on transistor N1, discharging its drain capacitance to the AC voltage, plus the drop across the on-state transistor. The gate-to-source voltage of the output transistor N3 will be near zero, keeping this transistor in cutoff. The output of the inverter will remain at its pre-charged value, which is one Schottky diode (metal to p-Si junction) drop below the peak supply voltage. If the input to N1 is a low voltage, then V_{GS} will be negative for the falling edge of the supply, and N1 will be cutoff. This allows N3 to turn on when the AC voltage falls below the center node by V_t. The output of the inverter will then discharge to the AC waveform, plus the drop across the on-state transistor N3.

To summarize the conditions of operation for the inverters, transistor N1 will turn on when

$$\left(V_{AC,peak} - V_{DS,on \ \text{p-channel}}\right) - V_{AC}(t) \geq V_{t, \ \text{n-channel}}$$

Transistor N2 will turn on for the condition

$$\left(V_{AC,peak} - V_{G, \ \text{n-channel}}\right) - V_{AC}(t) \geq V_{t, \ \text{n-channel}}$$

where $V_{G,\text{n-channel}}$ is the metal to n-type silicon diode drop. The turn on condition for P1 will be given by

$$V_{AC}(t) - \left(V_{AC,min} + V_{DS,on \ \text{n-channel}}\right) \geq V_{t, \ \text{p-channel}}$$

where the threshold for the p-channel device has been given as a positive number, representing the source-to-gate voltage. Finally, transistor P2 will turn on for

$$V_{AC}(t) - \left(V_{AC,min} + V_{G,\,p\text{-channel}} \right) \geq V_{t,\,p\text{-channel}}$$

6.4. MESFET DEVICE DESIGN ISSUES

6.4.1. SCHOTTKY GATE FORMATION

The most critical design issue in MESFET technology is the formation of the Schottky gate contacts. The gate contacts control many aspects of MESFET operation. In addition to controlling the forward-biased diode voltage, the barrier between the metal and semiconductor also determines how much electrostatic potential is dropped across the channel region with zero bias on the gate. This, in combination with the channel doping, determines the threshold voltage of the device and its off-state leakage current. The leakage currents for REL are not particularly important, but should be at least two or three orders of magnitude below the conducting current to prevent circuit operation from being impacted. REL circuits will not work with depletion mode devices.

6.4.2. THRESHOLD VOLTAGE AND CHANNEL RESISTANCE

A second issue that should be considered when designing MESFETs for REL operation is that the threshold voltage of the device must be greater than the source-to-drain voltage drop across an on-state transistor. This ensures that the first transistor of the inverter stage turns on before the second transistor for an active input signal. This criteria was not considered when dealing with MOSFET devices, where it is difficult to make this *not* the case. However, the threshold voltages for MESFET devices can be quite low, and are more often than not negative, as is the case for depletion mode devices. In addition, enhancement mode devices must have very narrow channel regions so that they may be completely depleted when the gate voltage is zero. This implies that the sheet resistance of the channel can be very large. Devices should be made as wide as possible to decrease

the channel resistance, thus increasing the device drive current. The combination of these two effects warrants close attention when designing MESFETs.

6.4.3. PARASITIC CAPACITANCES

MESFET devices enjoy benefits over both bipolar and MOSFET devices in lower parasitic capacitances. If the Schottky gate is fabricated such that there is sufficient distance from the source or the drain regions, then there is very little gate-to-source or gate-to-drain capacitance. The self-aligned process cited in [2] resulted in only 1 fF/μm of width in parasitic capacitance. The non self-aligned process simulated for this thesis shows considerably less than this. The primary capacitance in the MESFET structure results from the depletion capacitance under the Schottky gate, which increase only as $1/\sqrt{V_G}$. The metal gate junction has the added advantage of no diffusion capacitance, since there are no minority carriers.

6.5. MESFET DEVICE SIMULATIONS

Simplified MESFET device structures were simulated using MEDICI. No attempt was made to accurately model the physics of the Schottky gate contact. Using the complementary MESFET process reported on by researchers at Stanford University as a guideline, work functions were chosen to give barrier heights of approximately 0.9 eV for both n-channel and p-channel devices [2,25]. These are roughly the barrier heights reported in [2]. No barrier lowering mechanisms were included in the analysis. In addition, no Shannon implants were included in the process simulation, since it would be necessary to properly model the interaction of these implants with the metal gate electrode in order to extract an accurate barrier height. With this in mind, these simulations should be considered only an indication of how MESFET devices would behave in REL circuits.

The input files for generating the MEDICI device simulations appear in Appendix A. The n-channel and p-channel devices were simulated with identical doping profiles. N-channel devices were simulated with a p-type substrate, while p-channel devices were simulated using an n-type substrate. An actual complementary process must include an n-type or p-

type well, depending on the starting substrate. The substrate doping was assumed to be uniform at 5×10^{15} dopants per cm^3. Each channel profile had a peak doping concentration of 5×10^{17} cm^{-3} at the wafer surface. A back channel implant was simulated with a peak of 1×10^{18} cm^{-3} located 0.25 μm below the gate region only. This implant is useful in thinning the channel region so that it will be fully depleted with zero bias on the gate. This implant is pulled away from the source and drain contacts to avoid increased parasitic capacitances at the source/drain-to-substrate junction. The resulting channel profiles are shown in Figs. 6.2 and 6.3.
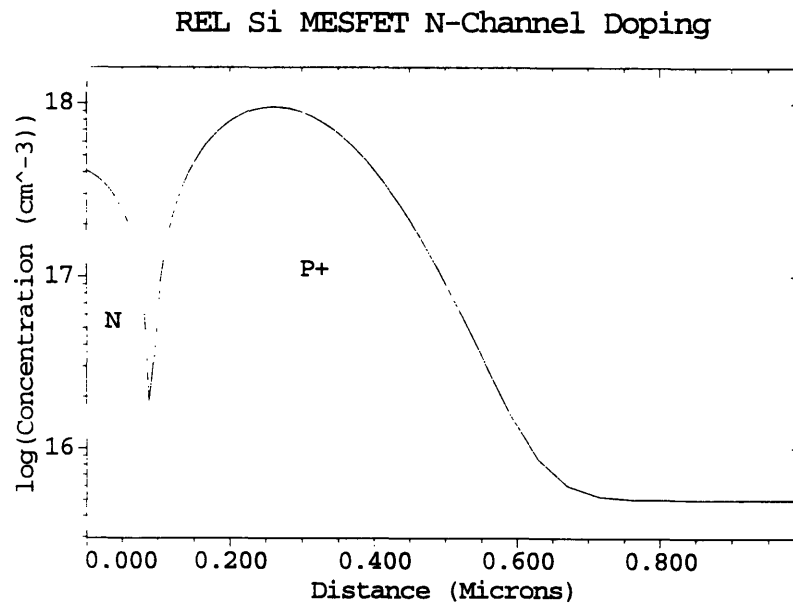
Figure 6.2: MEDICI simulated n-channel MESFET channel doping profile
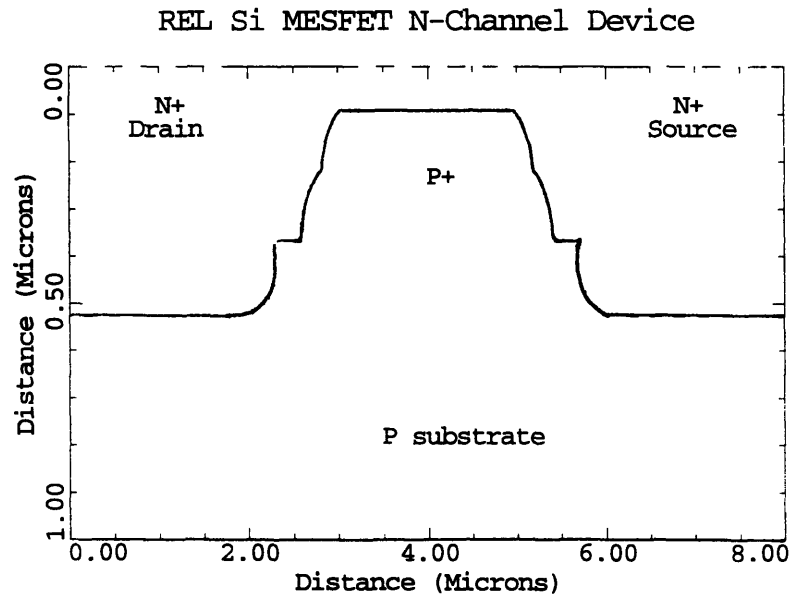
Figure 6.3: MEDICI simulated n-channel MESFET device cross section

The device layout is shown in Fig. 6.4. The gate electrode is 2 μm, with 1 μm spacing on either side to the source and drain regions. The gate region was pulled back from the source and drain regions in order to reduce the parasitic gate-to-source and gate-to-drain capacitances. The workfunction of the gate material contacting n-type silicon was set at 4.95, to give a barrier height of 0.9 eV. As noted previously, no barrier lowering mechanisms were simulated. The workfunction of the material contacting the p-type region was 4.27.
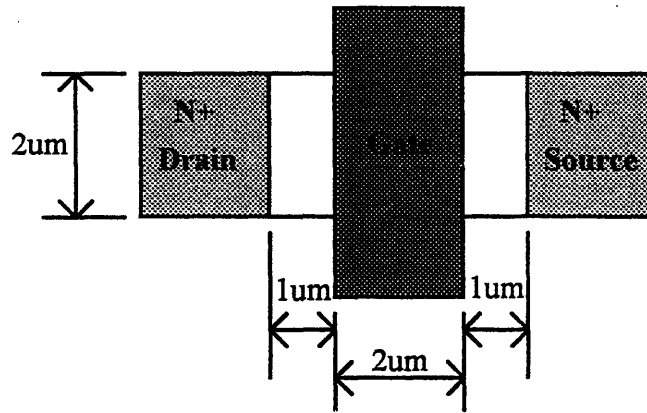
Figure 6.4: MESFET Device Top View

The resulting device parameters were extracted for use in HSPICE models. They are listed in Table 2. These parameters are for level 1 JFET devices, where the transit time across the gate diode has been set to zero, indicating that there is no diffusion capacitance.

TABLE 6.1.

Silicon MESFET Device Parameters for MEDICI Simulations

Device Parameter	N-channel FET	P-channel FET
Beta (A/V^2)	2×10^{-5}	1.5×10^{-5}
C_{GS0} (F/μm)	1×10^{-17}	1×10^{-17}
C_{GD0} (F/μm)	1×10^{-17}	1×10^{-17}
C_{GG} (F/μm)	1×10^{-15}	1×10^{-15}
ϕ_{bi} (V)	0.8	0.8
V_t (V)	0.20	0.32

6.6. MESFET REL CIRCUIT SIMULATIONS

Circuit simulations were performed using HSPICE for 2 μm wide device. The circuit is the same four inverter ring used for MOSFET and bipolar circuit simulations The results for 25 MHz operation are shown in Fig. 6.5. The load capacitance was calculated from the drain-to-substrate depletion capacitance, for an area of 2 μm x 2 μm, giving a load capacitance of 6 fF for a 5 x 10^{15} cm^{-3} substrate doping. Power-delay products were calculated at 0.05 pJ as compared to 0.3 pJ for the 2 μm CMOS implementation. This reflects the smaller device capacitances and smaller load capacitance of only 6 fF. The load capacitance here is considered the parasitic source/drain-to-substrate junction capacitance. Recall in the MOSFET implementation, the inverter transistors N2 and N5 had to be made three times wider than the diode connected transistors in order to ensure proper circuit operation. This extra width results in the increased load capacitance of the MOSFET implemented REL circuit.

Silicon MESFET Circuit Simulation

25 MHz, Cload = 6 fF
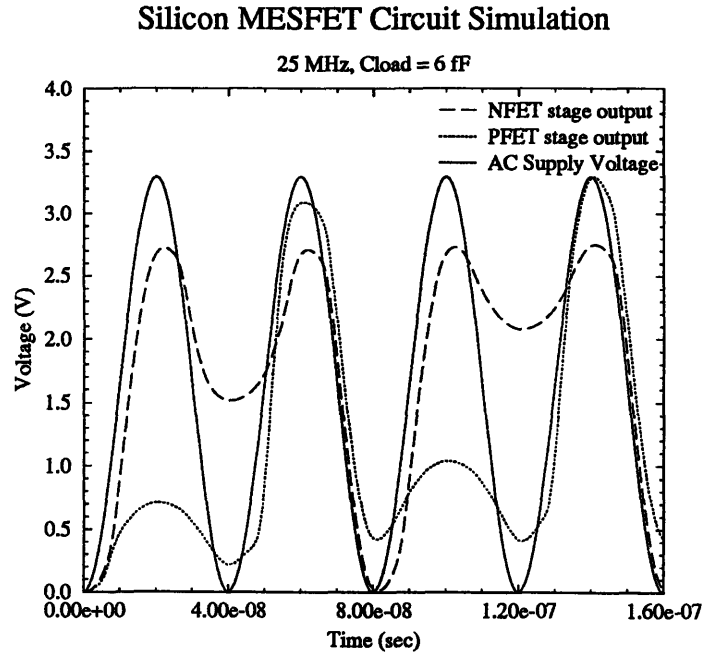
Figure 6.5: Silicon MESFET circuit simulation operated at 25 MHz, 6 fF load capacitance.

CHAPTER 7

HETEROJUNCTION BIPOLAR TRANSISTORS

7.1. INTRODUCTION

Heterojunction bipolar transistors (HBTs) offer several attractive features for fabricating REL circuits. The primary advantage of these devices is their increased emitter injection efficiency due to a wider band-gap emitter region. These devices can be fabricated in many technologies. In most III-V compound semiconductors, the band gap advantage is realized by using a wider band-gap material to form the emitter region. Silicon-Germanium heterostructure devices are fabricated by using $Si_{1-x}Ge_x$ material, which has a smaller band gap than pure silicon, to form the base region. In either case, the band discontinuity serves to limit the base current by presenting an energy barrier to base injection into the emitter, while permitting emitter injected current to travel to the collector unimpeded.

For a homojunction transistor the gain is primarily determined by the doping ratio of the emitter-to-base. Heterojunction bipolar transistors, on the other hand, achieve additional gain due to the band-gap difference. The maximum gain achievable is

$$\beta_{max} = \frac{N_E v_{nB}}{N_B v_{pE}} \cdot e^{\Delta E_g / kT}$$

where N_B and N_E are the emitter and base doping densities, v_{nB} and v_{pE} are the electron velocity in the base and the hole velocity in the emitter, respectively [6]. The base regions can then be very heavily doped, reducing the depletion regions in the base and allowing the base width to shrink. The parasitic capacitance can be kept to a minimum by lightly doping the emitter and collector regions. Because these devices are often grown in an

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MBE process, building inverted structures is not a problem [14]. In addition, speed advantages may be possible through grading the bandgap of the base material. Finally, REL requires only a single line for both the supply voltage and system clock, and thus reduces the need for multi-level metalizations in integrated circuits. This is beneficial to many heterojunction technologies, which rely heavily on mesa structures. These structures can present coverage problem during metalization due to non-planar topologies.

The GaAs/AlGaAs heterojunction is among the most mature of the heterojunction technologies. However, one of the drawbacks of GaAs/AlGaAs heterojunction transistors is the large forward bias voltage drop at the base-emitter junction. The efficiency of REL circuitry depends in part on the ratio of $V_{BE} + V_{CE,sat}$ to the power supply voltage. For a typical forward voltage drop of 1.25 volts, the benefits of REL over CMOS, for equivalent load capacitance, is reduced to just under 50% for a $3.3V_{p-p}$ supply voltage.

A promising alternative is $Si_{1-x}Ge_x$ heterostructures. The increased current gain of $Si_{1-x}Ge_x$ heterojunction transistors is accomplished by the use of a smaller bandgap $Si_{1-x}Ge_x$ base region, so the forward voltage is actually smaller than that of homojunction silicon transistors. This chapter will examine the operation of heterojunction bipolar transistors in REL circuits, focusing on $Si_{1-x}Ge_x$ base HBTs. Data is presented for simulated $Si_{1-x}Ge_x$ HBTs using the MEDICI two-dimensional device simulation software. Finally, circuit simulations indicating probable REL performance with $Si_{1-x}Ge_x$ HBTs are presented in the last section of the chapter.

7.2 HBT DEVICE REQUIREMENTS

The device requirements for heterojunction bipolar transistors do not differ from those of the homojunction silicon BJT. However, the presence of the narrow band-gap material offers several advantages in achieving these criteria.

7.2.1. PARASITIC CAPACITANCE

Low parasitic junction capacitances are one advantage of HBTs. Since the device gain is aided by the exponential dependence on the band-gap difference between the base and emitter, it is possible to reduce the emitter doping. Using a lightly doped emitter region will can greatly reduce the junction depletion capacitance. The increase in gain comes about mainly due to a barrier to injected holes from the base region into the emitter, thereby reducing the amount of base current. This is only true if the band discontinuity lies primarily in the valence base for an NPN device (this would be the conduction band for a PNP device). Any discontinuity at the conduction band edge for the NPN transistor will have the undesirable effect of impeding the flow of electrons injected into the base. Discontinuity in the conduction band can be reduced by grading the mole fraction layer of Ge in the $Si_{1-x}Ge_x$ layer.

7.2.2. PUNCHTHROUGH VOLTAGE

Large doping concentrations in the base region have the added benefit of forcing the space charge region of reverse biased junctions into the more lightly doped emitter and collector regions, rather than the base region. This allows a narrowed base region, and the possibility of faster devices. The actual speed of the device must take into account the minority carrier lifetimes in the base. Heavy doping of the base region can result in significantly reduced carrier lifetimes, increasing the amount of recombination that occurs in the device.

7.2.3. REVERSE BREAKDOWN VOLTAGE

If the method of growth of HBTs is assumed to be Molecular Beam Epitaxy (MBE) or Metal-Organic Chemical Vapor Deposition (MOCVD), then tight control of the doping levels in each region is possible. The junctions of the device will then closely resemble abrupt junctions. The breakdown voltage for an abrupt junction can be calculated as

$$V_{br} = \phi_{bi} - \frac{(N_A + N_D)}{N_A N_D} \cdot \frac{\varepsilon_{Si}}{2q} E_{crit}{}^2$$

The critical electric field for silicon is somewhat dependent on doping level, but a conservative value can be approximated as $E_{crit} \approx 3.5 \times 10^5$ V/cm. For a base doping of 9 x 10^{18} cm^{-3}, the emitter and collector dopings must be less than 1 x 10^{17} cm^{-3} to achieve reasonable breakdown voltages of around 4 volts, 120% over the peak AC voltage of 3.3 volts.

7.2.4. SATURATION VOLTAGE

Single heterojunction HBTs suffer from an offset in the collector-emitter voltage due to the difference in the material interfaces with the base region. If grading of the germanium profile within the base region is employed in order to increase the device speed, then this may also be a problem for SiGe HBTs. In considering the saturation voltage across the device, it is desirable to have identical base-emitter and base-collector junctions, suggesting a uniform distribution of germanium in the base region.

7.3. SILICON-GERMANIUM HBT DEVICE SIMULATIONS

The MEDICI software tool was used to evaluate the one-dimensional device characteristics for silicon germanium base HBTs, with a 20% concentration of germanium (x = 0.2). The full two-dimensional device layout would require a mesa structure in order to isolate the $Si_{1-x}Ge_x$ base region from the emitter region. These non-planar device structures require special grid generation software, which was unavailable for this study. However, comparisons were made between the homojunction simulation results for both one-dimensional and two-dimensional simulations. The results were very similar, indicating that the one-dimensional simulations accurately predict the two-dimensional simulated device parameters. The evaluation of the punchthrough voltage requires a two dimensional analysis which allows the space-charge region to grow into the extrinsic base region. Therefore, the punchthrough voltage could not be determined for the $Si_{1-x}Ge_x$ HBT devices.

The Gummel plots for the simulated $Si_{1-x}Ge_x$ heterojunction bipolar transistors appear in Figs. 7.1 and 7.2. The effects of high level injection on both the NPN and PNP devices are evident in these plots. This is primarily due to the more lightly doped emitter and collector regions, as compared to the homojunction bipolar transistors. It is somewhat less prominent in the PNP devices, where the emitter doping was slightly higher to make up for the ratio of the minority carrier velocities in the n-type $Si_{1-x}Ge_x$ base versus the p-type Si emitter. The f_t plots for these two devices appear in Figs. 7.3 and 7.4. Marked increases in the f_t's are measured. This is primarily a result of the reduced base width and decreased parasitic capacitances of the HBT devices.

NPN SiGe log Ic,Ib vs. Vbe
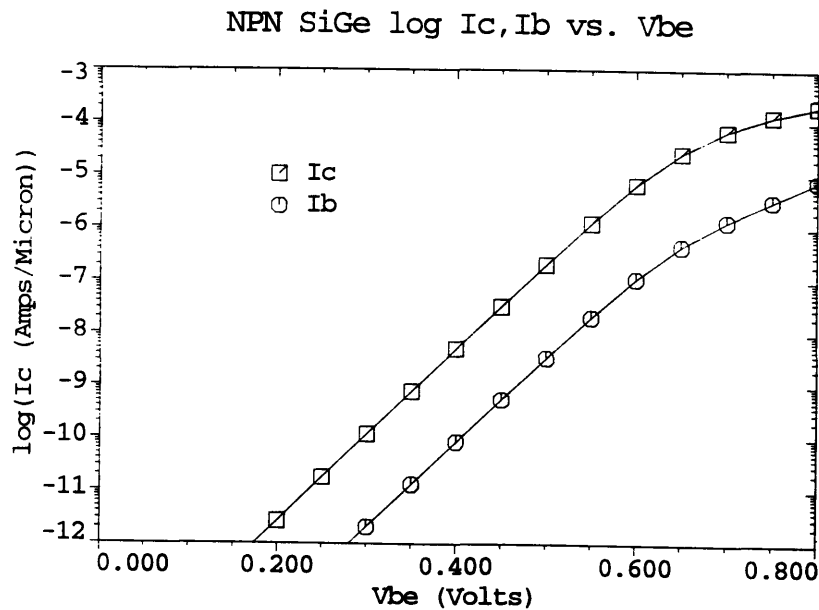
Figure 7.1: Silicon-Germanium NPN HBT $log(I_C)$ and $log(I_B)$ versus V_{BE}

PNP SiGe Ic,Ib vs. Veb
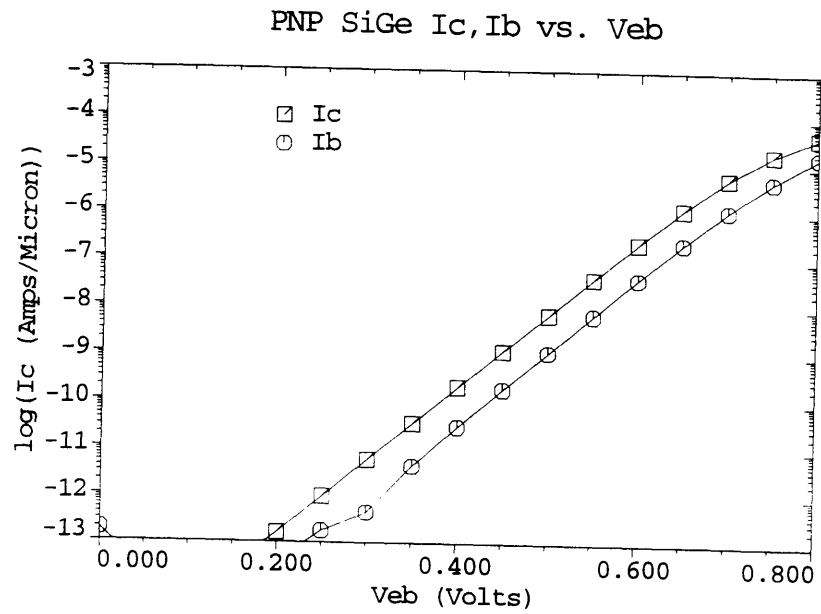
Figure 7.2: Silicon-Germanium PNP HBT log(I_C) and log(I_B) versus V_{EB}

NPN SiGe Ft vs. log(Ic)
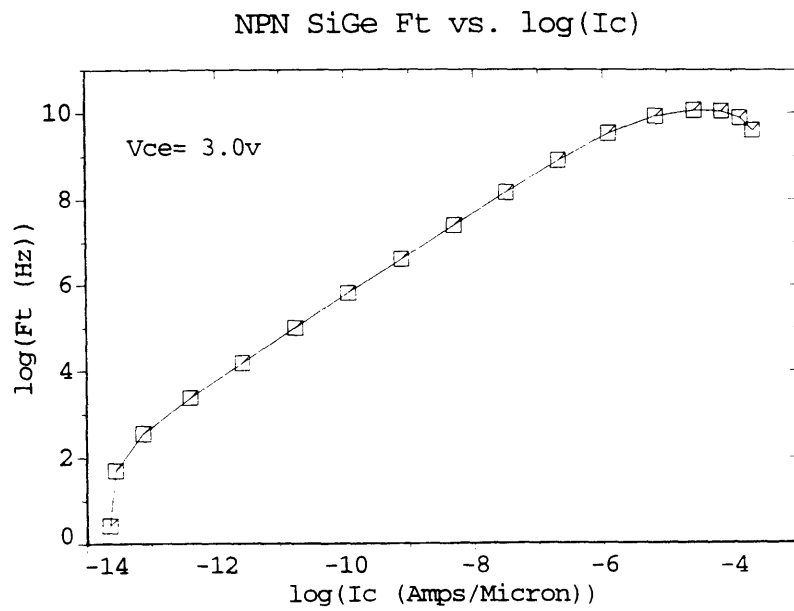
Figure 7.3: Silicon-Germanium NPN HBT f_t versus log(I_C)

PNP SiGe Ft vs. Ic
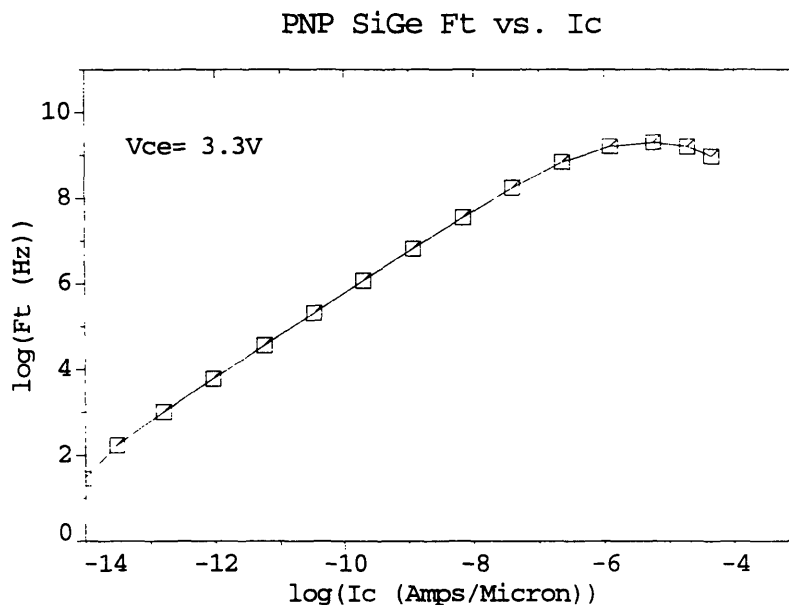
Figure 7.4: Silicon-Germanium PNP HBT f_t versus $\log(I_C)$

7.4. SILICON-GERMANIUM HBT CIRCUIT SIMULATIONS

The device parameters extracted from the one-dimensional MEDICI simulations were used to develop bipolar device models to be used in HSPICE circuit simulations. The circuit simulation was for the same four-stage inverter ring simulated for the other device technologies. Figs. 7.5 and 7.6 show the Gummel plots of the MEDICI devices in comparison to the devices used for the circuit simulations. The rather non-ideal behavior of the $Si_{1-x}Ge_x$ HBTs made it difficult to match the I-V characteristics with great accuracy. Especially noticeable is the discrepancy between the base current for the NPN MEDICI device simulations and that of the HSPICE model. This difference is due to the effects of high level injection in the emitter region, which cannot be modeled with the existing HSPICE equations.

Despite the higher than expected base currents of the NPN devices, the HSPICE circuit simulations show much improved circuit performance for the $Si_{1-x}Ge_x$ devices over the other device technologies. Fig. 7.7 shows the results of a circuit simulation done at 100

MHz, with a load capacitance of 90 *fF*. The sagging in the waveform is a result of the capacitive divider between the parasitic capacitances and the load capacitance, and is independent of frequency. Unlike the homojunction silicon bipolar transistor, both the PNP and NPN devices are well into saturation, even at 100 MHz. The power-delay product for this circuit was calculated to be 0.2 pJ.

Silicon-Germanium NPN Gummel Plot

MEDICI vs. HSPICE Models
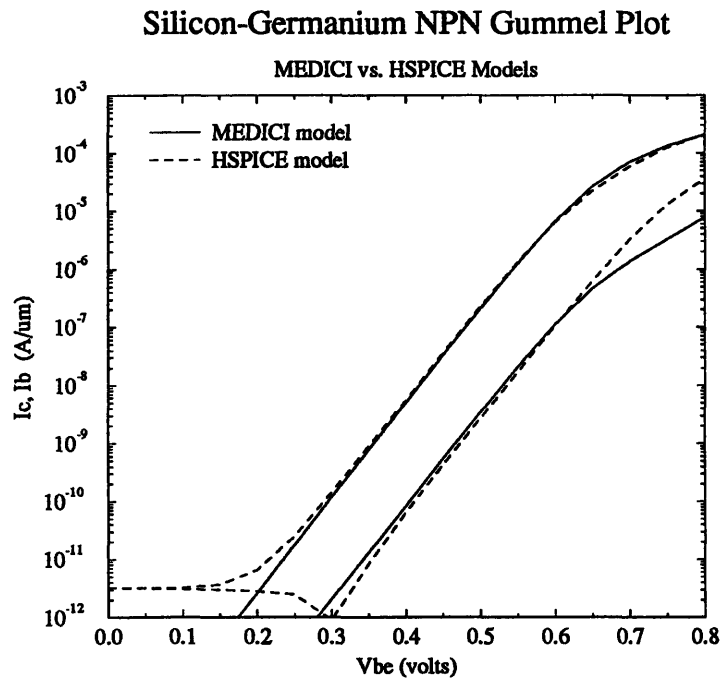
Figure 7.5: Silicon-Germanium NPN HBT Gummel plot: MEDICI versus HSPICE models

Silicon-Germanium PNP Gummel Plot

MEDICI vs. HSPICE Models
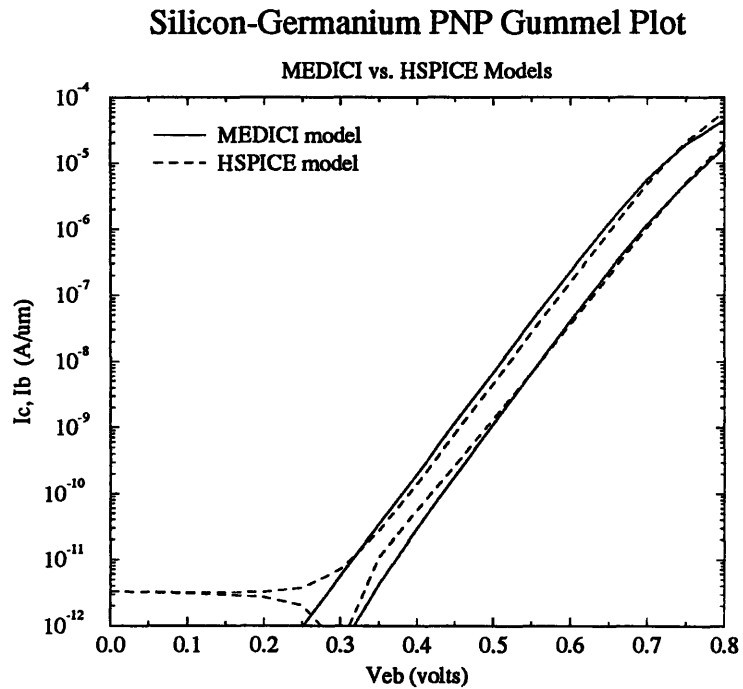
Figure 7.6: Silicon-Germanium PNP HBT Gummel Plot: MEDICI versus HSPICE models

SiGe HBT Circuit Simulation

100 MHz, Cload = 90 fF
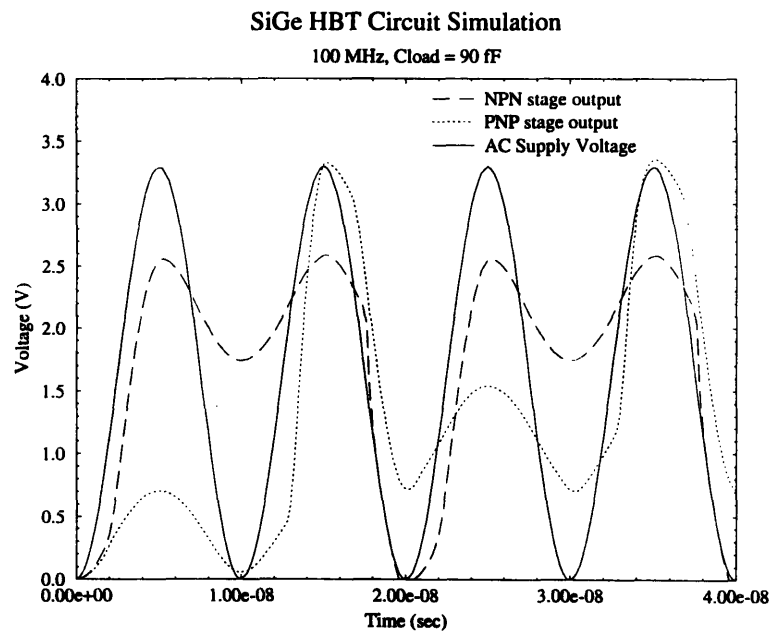
Figure 7.7: $Si_{1-x}Ge_x$ HBT circuit simulation operated at 100 MHz, 90 fF load capacitance.

CHAPTER 8

GALLIUM-ARSENIDE MESFET TRANSISTORS

8.1 INTRODUCTION

The GaAs MESFET has also been investigated, since it is the most mature of the MESFET technologies. However, since REL operation relies on both carrier types, this gives complementary silicon MESFETs a decided advantage over GaAs MESFETs. Although the GaAs material system enjoys higher electron mobilities than silicon, the complementary nature of REL limits the circuit speed to the hole mobility, which is actually lower for GaAs. Given the additional expense of working with GaAs wafers, there seems to be little benefit in GaAs MESFETs over silicon MESFETs for REL applications. Nevertheless, the advances made in fabricating Schottky contacts to both n-type and p-type GaAs may make GaAs FETs attractive for REL circuit fabrication.

The GaAs MESFET was introduced as early as 1980 [20], and has evolved into a rather complex structure of layered materials. The most advanced structure today, often referred to as the HEMT, or High Electron Mobility Transistor, may contain six layers or more. These devices use a lattice matched AlGaAs layer to form an insulating barrier, much like the oxide layer of a MOSFET. The channel layer is often formed out of lattice matched InGaAs, which has higher electron mobilities than GaAs. In order to increase the carrier density in the channel, a thin layer of dopants, usually a monolayer of silicon, may be introduced in the region adjacent to the InGaAs region as well. If the InGaAs channel region is made thin enough, then the density of states in the channel will be confined to only two dimensions, and the electrons will form a two dimensional electron gas (2DEG) [6,7]. This provides additional advantages in electron mobility.

8.2. GAAS MESFET DEVICE REQUIREMENTS

REL circuit operation using GaAs MESFETs is identical to circuits using silicon MESFETs, and therefore the device requirements are quite similar. One of the key parameters is again the Schottky gate contact. The Schottky barrier heights for n-type GaAs are as high as 0.9 eV, and reach just over 0.6 eV for p-type contacts [5], which makes them more attractive than silicon MESFETs for MOS-type circuits. Both of these are also adequate for REL circuit applications. However, it should be stressed that increased barrier heights are not necessarily beneficial to REL. Their main advantage lies in increasing the noise margin of REL circuits. Much of the recent research activity has been in the area of HEMTs. There are several companies currently using or developing complementary HEMT fabrication lines [3,29]. Unfortunately for REL, the trend of developmental work has been to try to increase the insulating properties of the AlGaAs layer. The Schottky barrier height of the AlGaAs to gate electrode contact has recently been increased to nearly 1.6 volts in order to reduce the amount of gate leakage current [3]. This effort is counter productive for REL circuits, since this threshold voltage serves as a logic low in REL circuitry. It is, therefore, more appropriate for REL circuits to examine previous generations of GaAs devices for an indication of GaAs MESFET performance in REL circuits. The more advanced HEMT devices can still be used for REL circuitry by using the circuit topology of the CMOS inverter stage, where an additional transistor is connected as a diode to perform the pre-charging functions required.

8.3. GAAS MESFET CIRCUIT SIMULATIONS

Since the MESFET is inherently a lateral device, using MEDICI for one-dimensional (vertical) simulations of GaAs MESFETs was not possible. The non-planar structure of the GaAs FET made it difficult to create an adequate grid structure for doing two-dimensional simulations. Therefore, the device parameters used for GaAs circuit simulations were taken from reports found in the literature. Since the more advanced structures of recent GaAs MESFETs have increased the threshold voltages of the Schottky gate beyond the usable range of REL circuitry, the main source of information was from older papers on GaAs devices. For consistency, all parameters were taken from

a single source. Kiehl's 1987 work on complementary heterostructure FETs was used as a representative of possible device parameters [17]. The gate-to-channel turn-on voltages were assumed to be 0.8 volts for the p-channel devices and 0.7 volts for the n-channel devices. The threshold voltages were given as 0.2 volts for both devices. The gate length used was 0.7 μm, with a 1 μm spacing between the channel and the source and drain contacts. The parasitic capacitance values were estimated from experimentally determined values at 0.25 fF/μm width for the gate-to-source and gate-to-drain capacitances, and 0.05 fF/μm for the gate-to-ground capacitance.

The GaAs MESFET parameters presented in [17] were used to develop an HSPICE model for circuit simulation. This model is given in Appendix C. Circuit simulations for the four inverter ring appear in Fig. 8.1. This simulation was run with an AC sinusoidal supply voltage running at 100 MHz, with a 6 fF load capacitance. Significant leakage problems were observed in these devices at frequencies below 30 MHz. This is probably due to the relatively low parasitic capacitances and the short channel lengths of these devices.
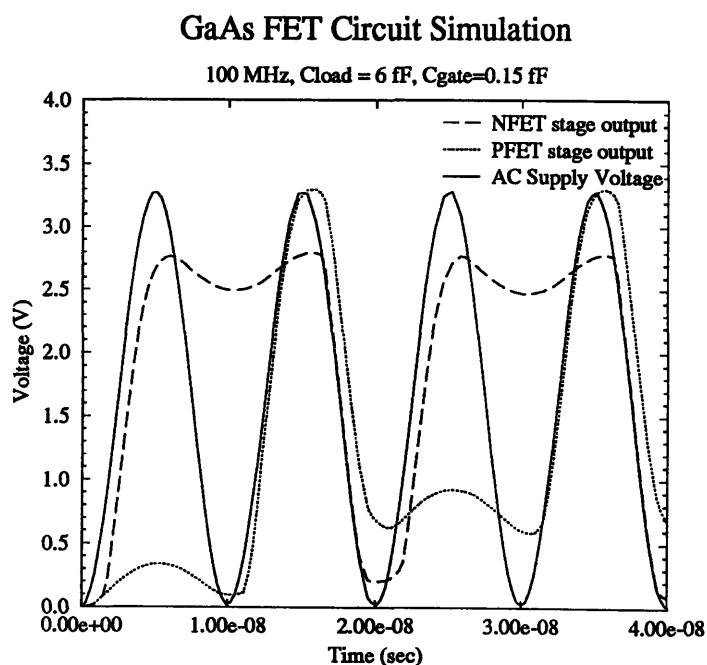
Figure 8.1: GaAs MESFET circuit simulation operated at 100 MHz, 6 fF load capacitance.

The reported gate-to-ground capacitance for these devices was more than one order of magnitude less than that of the simulated silicon MESFET devices. To make a comparison to the silicon MESFET simulations, the device parameters were altered to make the gate-to-ground capacitance the same as that of the silicon MESFET. Fig. 8.2 shows a 20 MHz simulation run for the altered gate-to-ground capacitance. The performance of the GaAs n-channel devices are comparable to the silicon n-channel MESFET stages shown in Fig. 6.5. However, the p-channel stages show significantly degraded performance.

GaAs MESFET Circuit Simulation

20 MHz, Cload = 6 fF, Cgate = 2 fF
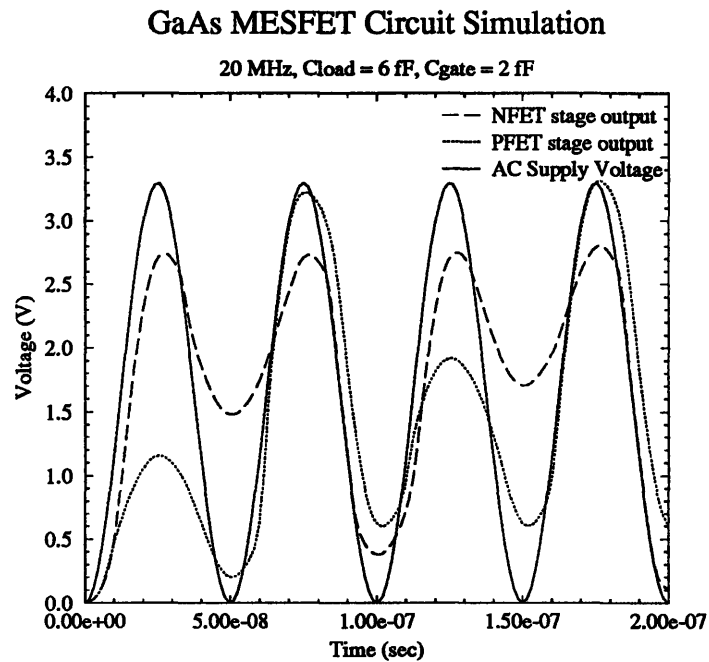
Figure 8.2: GaAs MESFET circuit simulation operated at 20 MHz, 6 fF load capacitance and a gate-to-ground capacitance of 2 fF.

CHAPTER 9

CONCLUSION

9.1. CMOS IMPLEMENTATION

Circuit simulations of REL circuits implemented in MOS 2 μm technology worked up to 20 MHz with a peak-to-peak supply voltage of 3.3 volts. In order to work at this supply voltage, the device threshold voltages had to be lowered to 0.3 volts. Slightly higher frequency operation can be attained if the threshold voltages are reduced further. However, this also reduces the noise margin of the circuit. Performance improvements are also expected for shorter channel length devices. The power-delay products of these simulated circuits was calculated to be 0.3 pJ. Scaling the devices to 0.6 μm channel lengths reduces the device capacitances, allowing the circuit to operate up to 150 MHz, with a power-delay product of only 0.04 pJ.

The main failure mechanism of REL circuits implemented in CMOS is the failure of the transistor to be fully turned on at high frequency operation. This is due to the inability of the device to supply the current demanded by the $C \cdot \partial V / \partial t$ product. This problem is exacerbated by the diode connected transistors necessary for pre-charging the logic nodes. These transistors limit the gate voltage applied to the inverter transistors to little more than the threshold voltage. An area of future work is to examine the effect of using higher threshold devices for the diode connected transistors. This would allow a larger V_{GS} driving voltage for the inverter transistors, improving the current drive and high frequency operation of the transistors.

The benefits of implementing REL in CMOS technology are that the semiconductor industry has invested heavily in CMOS technology, and it is by far the most cost-effective fabrication technology available. REL circuits not only offer lower power dissipation, but

are also less vulnerable to short channel effects. The high field stresses across devices in REL circuits are much less than traditional CMOS logic circuits, and therefore the device reliability due to hot carrier effects should be improved. This reduces the need for expensive drain engineering techniques, such as lightly doped drains.

9.2. BIPOLAR JUNCTION TRANSISTOR IMPLEMENTATION

Simulations of REL circuits implemented in inverted bipolar junction transistors were functional up to 50 MHz. The inverted structures were chosen over the more standard emitter-up transistor because the circuit topology ties all of the emitters together. Thus, the inverted bipolar transistors offer self isolating devices and less wiring. They have the disadvantage of have the large area junction be the base-emitter junction, which has a larger parasitic capacitance per unit area. However, bipolar transistors optimized for use in REL have a relatively highly doped collector region, so the differential in the two junction capacitances is not large.

The main failure mechanism for the REL circuits implemented in silicon bipolar was the failure of the PNP devices to fully saturate, resulting in a loss of noise margin. The PNP devices fail to saturate when driven into high level injection, where the gain of the devices is greatly reduced. Since the inverted PNP devices have very low gains to begin with, even a slight fall off in collector current makes it difficult to saturate the transistor in this circuit configuration. However, the circuit simulations fail to take into account the accompanying reduction in base current due to high level injection in the emitter region as well. This results in lower gain than should be expected.

The power-delay products for these circuits was 0.8 pJ, which is 2.5 to 3 times larger than the CMOS circuits. This increased power dissipation is due to the larger load capacitance of 80 fF for these circuits. The larger load capacitance is necessary to avoid the capacitive divider of the load capacitance with the parasitic junction capacitances, which are much larger than the parasitic capacitances of the MOS devices. There is the possibility of reducing these capacitance through the use of a self-aligned process. Recent reports on self-aligned bipolar processes have achieved total device widths of 1.6 μm. However, the

need for complementary devices will introduce significant complexities to a self-aligned process. An area of future work could be in adapting the existing self-aligned processes to a complementary process. If the devices are to be built inverted, to take advantage of the self-isolating inverted structure and the circuit topology, then this also must be considered for a self-aligned process.

In addition to the silicon bipolar transistors, heterojunction bipolar transistors were also used in REL circuit simulations. Circuit simulations of REL implemented in SiGe HBT technology operated up to 100 MHz, with a power delay product of 0.2 pJ. The load capacitance of these circuits was 90 fF. Despite smaller parasitic capacitances, the larger load capacitances were reflective of the larger device area assumed for an HBT mesa structure.

Heterojunction bipolar transistors offer the advantage of achieving their gain through a difference in the energy bandgap of the emitter and base regions. Among the heterojunction devices examined, the Si/Si_xGe_{1-x}/Si structure seems most promising. The forward voltage of the AlGaAs/GaAs HBT is typically 1.25 volts or more, which is too high to be useful in REL circuits. By taking advantage of the increased gain provided by the lower bandgap base region, the doping in the emitter and collector regions of HBTs can be reduced. The lower dopings in the emitter and collector regions translate into smaller parasitic capacitances. In addition, if the base is highly doped, then the depletion regions at the base-emitter and base-collector junctions will push into the emitter and collector regions respectively. This allows a smaller base width than comparable homojunction devices.

The HBT device simulations performed in this work were only for one-dimensional devices. Extensive work remains in examining the two-dimensional device design.

9.3. MESFET IMPLEMENTATION

REL circuits implemented in a 2 μm silicon MESFET technology showed the best all around performance. Simulated circuits performed up to 25 MHz, with a power-delay

product of only 0.05 pJ. The load capacitance for these simulations was only 6 fF. The smaller load capacitance is representative of the smaller source and drain regions, and hence the smaller junction capacitance. Unlike the MOSFET implementation, no additional diode connected transistors are necessary in a MESFET implementation, because the pre-charging function can be accomplished through the Schottky gate diode. Recall that the inverter transistor of the MOSFET REL circuit had to be three times wider than the diode connected transistor. Further improvements in the frequency response of the circuit can be expect for shorter channel devices.

As with the other technologies, the failure mechanism of the REL circuits implemented in MESFETs is the failure of the p-channel transistors to be fully turned-on. This is due to the lower mobility and transconductance of holes in p-channel devices. The lower frequency limit of operation in REL circuits implemented with MESFETs most likely will be determined be the leakage of the Schottky gate, rather than the off-state leakage of the transistor. For this reason, the formation of the Schottky gate will be critical to device and circuit performance.

With this in mind, the biggest problem facing REL circuits fabricated in silicon MESFET technology is the need for complementary devices. Historically, it has been very difficult to form Schottky contacts to p-type silicon. Recent reports out of Stanford University indicate that this problem can be overcome [2]. Circuits which operate in an MOS-like fashion have had problems with p-channel MESFETs because the Schottky barriers to p-type material were too low. However, low barrier heights are not necessarily a problem for REL circuitry, since the threshold voltage essentially only establishes the noise margin on the logic low state. Provided this threshold voltage is larger than the on-state voltage drop of the transistor, the circuit will be functional. It should also be pointed out that no attempt was made to model the actual Schottky barrier. This remains an area that must be thoroughly examined before an accurate prediction of REL performance in a silicon MESFET technology can be attained.

REL circuit performance for GaAs MESFETs was also examined, although no device simulations were performed. The device parameters were estimated from reports in the literature [17]. These circuit simulations showed operation up to 100 MHz for a 6 fF load capacitance. The power-delay product was measured at 0.01 pJ. The example device had

a channel length of only 0.7 μm, with a gate-to-ground capacitance of only 0.05 fF/μm. This is more than an order of magnitude less than that calculated for the simulated silicon MESFETs. When the gate-to-ground capacitance was increased to that of the silicon MESFET device, the GaAs MESFET circuit simulations showed significantly degraded performance at 20 MHz in comparison to the silicon MESFETs. This due to the reduced mobility of holes in GaAs.

9.4. CONCLUSION AND FUTURE STUDY

Table 9.1 summarizes the performance of REL circuits implemented in CMOS, silicon BJT, silicon MESFET, $Si_{0.8}Ge_{0.2}$ HBT, and GaAs MESFET technologies. Listed are the minimum feature size, load capacitance, power-delay product, and the maximum frequency of operation. It should be noted that simulations were not conducted for frequencies beyond 100 MHz. Presumably, the power supply frequency will become the limiting factor in this frequency regime.

TABLE 9.1.

REL Circuit Simulation Result Summary

Technology	Minimum Feature Size	Load Capacitance	Maximum Frequency	Power-Delay Product
CMOS	2 μm	10 fF	20 MHz	0.3 pJ
CMOS	0.6 μm	10 fF	> 100 MHz	0.04 pJ
Silicon BJT	2 μm	80 fF	50 MHz	0.9 pJ
Silicon MESFET	2 μm	6 fF	25 MHz	0.05 pJ
$Si_{0.8}Ge_{0.2}$ HBT	2 μm	90 fF	> 100 MHz	0.2 pJ
GaAs MESFET	0.7 μm	6 fF	> 100 MHz	0.01 pJ

REL circuits implemented in CMOS are functional, but not optimal. The need for control terminal current makes MESFETs or bipolar junction transistors a more attractive alternative. The simulated performance of REL circuits implemented in bipolar junction transistors show that the large parasitic capacitances of these devices make them un-competitive with FET implementations. The most promising technology for implementing REL circuits is silicon MESFETs. These devices offer higher bulk mobilities and lower interconnect resistances in comparison to MOSFETs, in addition to easier implementation of REL. They are inherently self-isolating with small parasitic capacitances in comparison to bipolar transistors. However, the Schottky contact was not modeled accurately. The issue of leakage currents through the metal-semiconductor contact needs to be carefully addressed. Much work remains in evaluating the practicality of forming reliable Schottky contacts to p-type silicon.

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APPENDIX A

MEDICI SIMULATION INPUT FILES

SILICON BJT MEDICI SIMULATIONS

TITLE	TMA MEDICI - Inverted bipolar transistor File: npn_1.in
comment	for REL applications

COMMENT Grid Generation and Initial Biasing

COMMENT Specify a recatangular grid
MESH
X.MESH   WIDTH=4.0 H1=0.3 H2=0.10
X.MESH   WIDTH=4.0 H1=0.10 H2=0.30
Y.MESH   DEPTH=0.35 H1=0.100 H2=0.02
Y.MESH   DEPTH=1.65 H1=0.050 H2=0.30

ELIMINATE   COLUMNS X.MIN=0 X.MAX=6.0 Y.MIN=0.65
ELIMINATE   COLUMNS X.MIN=0 X.MAX=6.0 Y.MIN=0.65

COMMENT Region definition
REGION   NUM=1 SILICON

COMMENT Electrodes: #1=Base #2=Collector #3=Emitter
ELECTR   NUM=1 X.MIN=1.00 X.MAX=2.50 TOP
ELECTR   NUM=2 X.MIN=4.00 X.MAX=6.00 TOP
ELECTR   NUM=3 BOTTOM

COMMENT Specify impurity profiles
PROFILE   N-TYPE N.PEAK=5E15 UNIFORM OUT.FILE=NPN_DS
PROFILE   P-TYPE N.PEAK=7E17 Y.MIN=.35 Y.CHAR=0.17
+   X.MIN=0.50 WIDTH=6.5 XY.RATIO=.75
PROFILE   P-TYPE N.PEAK=1E19 Y.MIN=0.0 Y.CHAR=0.05
+   X.MIN=1.00 WIDTH=1.5 XY.RATIO=.65
PROFILE   N-TYPE N.PEAK=1E18 Y.MIN=.25 Y.CHAR=0.16
+   X.MIN=3.0 WIDTH=4.0 XY.RATIO=.75
PROFILE   N-TYPE N.PEAK=1E19 Y.MIN=0.0 Y.CHAR=0.05
+   X.MIN=3.75 WIDTH=1.5 XY.RATIO=.65
PROFILE   N-TYPE N.PEAK=1E18 Y.MIN=0.90 Y.CHAR=.25

COMMENT Regrid on doping
REGRID   DOPING LOG RATIO=3 SMOOTH=1
IN.FILE=NPN_DS

```
REGRID                    DOPING LOG RATIO=3  SMOOTH=1
IN.FILE=NPN_DS


COMMENT      Extra regid in emitter-base junction region only

REGRID                           DOPING LOG RATIO=3  SMOOTH=1  IN.FILE=NPN_DS
+                                X.MIN=2.25  X.MAX=4.75  Y.MIN=0.35  Y.MAX=0.65

+                                OUT.FILE=NPN_MS
```

SILICON MESFET MEDICI SIMULATIONS

```
TITLE        REL MESFET Transistor Simulation              File:NFET_1
COMMENT      Simulating a Silicon MESFET enhancement transistor


COMMENT      Specify a rectangular grid
MESH
X.MESH                 WIDTH=4.00  H1=0.500  H2=0.10
X.MESH                 WIDTH=4.00  h1=0.10  h2=0.50
Y.MESH                     DEPTH=0.2  H1=0.008
Y.MESH                     DEPTH=1.3  H1=0.008  H2=0.10


COMMENT      get rid of grid points in s/d regions
eliminate              rows  x.min=0  x.max=2.0  y.max=0.4
eliminate              rows  x.min=0  x.max=2.0  y.max=0.4
eliminate              rows  x.min=6.0 x.max=8.0  y.max=0.4
eliminate              rows  x.min=6.0 x.max=8.0  y.max=0.4


COMMENT      Region definition
REGION                     NUM=1  SILICON


COMMENT      Electrodes:  #1=Gate  #2=Source  #3=Drain #4=Substrate
ELECTR                     NUM=1  X.MIN=3.00  X.MAX=5.00  TOP
ELECTR                     NUM=2  X.MIN=0  X.MAX=2.0  TOP
ELECTR                     NUM=3  X.MIN=6.0  X.MAX=8.0  TOP
ELECTR                     NUM=4  BOTTOM


COMMENT      Doping profiles
COMMENT      Channel doping
PROFILE                P-TYPE  N.PEAK=5E15  UNIFORM  OUT.FILE=NFET_DS
PROFILE                N-TYPE  N.PEAK=5.0E17  Y.MIN=0.0  Y.CHAR=0.17
+                      X.MIN=2.00  WIDTH=4.0
PROFILE                P-TYPE  N.PEAK=1.0E18  Y.MIN=.25 Y.CHAR=.16
+                      X.MIN=3.00  WIDTH=2.0  XY.RAT=.75
COMMENT      Source and drain implants
PROFILE                N-TYPE  N.PEAK=7E19  Y.MIN=0  Y.CHAR=.17
+                      X.MIN=0.0  WIDTH=2.0  XY.RAT=.65
PROFILE                N-TYPE  N.PEAK=7E19  Y.MIN=0  Y.CHAR=.17
```

```
+                          X.MIN=6.00  WIDTH=2.0  XY.RAT=.65
```

COMMENT   Regrid on doping
REGRID   IN.FILE=NFET_DS DOPING LOG RATIO=3
SMOOTH=1
+   y.min=1.0 out.file=NFET_MS

SILICON GERMANIUM HBT MEDICI SIMULATIONS

TITLE   TMA MEDICI - REL SiGe Transistor (Inverted)

COMMENT   Specify a "1D" Mesh Structure
MESH   OUT.FILE=NPN_MS
X.MESH   WIDTH=1.00 N.SPACES=1
Y.MESH   DEPTH=0.5 H2=0.005 RATIO=1.2
Y.MESH   DEPTH=0.5 H1=0.005
Y.MESH   DEPTH=1.0 H1=0.005 H2=0.050

COMMENT   Use a SiGe Base (X.MOLE=0.2) with a graded mole fraction
+   for the emitter-base and base-collector transistions
REGION   NUM=1 SILICON
REGION   NUM=2 SIGE Y.MIN=0.500 Y.MAX=0.520
X.MOLE=0.0
+   X.END=0.1
REGION   NUM=2 SIGE Y.MIN=0.520 Y.MAX=0.700
X.MOLE=0.0
+   X.END=0.2
REGION   NUM=2 SIGE Y.MIN=0.700 Y.MAX=0.720
X.MOLE=0.2
+   X.END=0.0

COMMENT   Electrodes: 1:emitter 2:base 3: collector
+   Use a majority carrier contact for the base
ELECTR   NUM=1 Y.MIN=0.520 Y.MAX=0.520 majority
ELECTR   NUM=2 BOTTOM
ELECTR   NUM=3 TOP

PROFILE   N-TYPE N.PEAK=5E15 UNIFORM
PROFILE   N-TYPE N.PEAK=1E19 Y.MIN=0.00 Y.CHAR=0.17
PROFILE   P-TYPE N.PEAK=1E17 UNIFORM Y.MIN=0.50
DEPTH=0.22
PROFILE   N-TYPE N.PEAK=5E18 Y.MIN=1.80 Y.CHAR=0.25

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APPENDIX B

HSPICE SIMULATION MODELS

```
*
*       hspice transistor models for rel circuits
*
*
*              Silicon Bipolar transistors
*
* transistor models
.model qnpn NPN level=1  subs=1  update=1
+ bf=17                   br=15                   ibc=1e-17
+ ibe=2e-17
+ nf=1.05        nr=1.1          isc=0
+ ise=5e-18      nc=2            ne=1.5
+ vaf=2.6        var=4.4         ikf=1e-4
+ ikr=1e-4       irb=0           rb=500
+ rbm=0                  re=100                  rc=100
+ cjc=1.1e-15    cje=4.0e-15     cjs=0
+ mjc=0.33       mje=0.33                mjs=0.5
+ vjc=.89        vje=.85         vjs=.75
+ itf=1.6e-6     tf=1.8e-11      tr=2e-11
+ vtf=0          xtf=0           nkf=0.5
*
*

.model qpnp PNP level=1  subs=1  update=1
+ bf=4.5                  br=4                    ibc=9e-18
+ ibe=9e-18
+ nf=1.05        nr=1            isc=1e-20
+ ise=3e-20      nc=2            ne=1.5
+ vaf=2.5        var=2.5         ikf=1e-5
+ ikr=1e-5       irb=0           rb=400
+ rbm=400        re=100          rc=100
+ cjc=2.3e-15    cje=4.9e-15     cjs=0
+ mjc=0.33       mje=0.33                mjs=0.5
+ vjc=.89        vje=.85         vjs=.75
+ itf=4.6e-6     tf=2.6e-10      tr=3e-10
+ vtf=0          xtf=0           nkf=0.5
*
*       SILICON BIPOLAR TRANSISTORS: SCALED
*               BASE-COLLECTOR JUNCTION:         3X
*               BASE-EMITTER JUNCTION:      4X
* transistor models
```

```
.model qnpn_s NPN level=1  subs=1  update=1
+ bf=17                 br=15            ibc=3e-17
+ ibe=6e-17
+ nf=1.05       nr=1.1          isc=0
+ ise=15e-18    nc=2            ne=1.5
+ vaf=2.6       var=4.4         ikf=3e-4
+ ikr=3e-4      irb=0           rb=500
+ rbm=0                 re=100           rc=100
+ cjc=3.3e-15   cje=16.0e-15    cjs=0
+ mjc=0.33      mje=0.33                 mjs=0.5
+ vjc=.89       vje=.85         vjs=.75
+ itf=1.6e-6    tf=1.8e-11      tr=2e-11
+ vtf=0         xtf=0           nkf=0.5
*
*
.model qpnp_s PNP level=1  subs=1  update=1
+ bf=4.5                br=4             ibc=27e-18
+ ibe=27e-18
+ nf=1.05       nr=1            isc=3e-18
+ ise=9e-18     nc=2            ne=1.5
+ vaf=2.5       var=2.5         ikf=3e-5
+ ikr=3e-5      irb=0           rb=400
+ rbm=400       re=100          rc=100
+ cjc=6.9e-15   cje=15e-15      cjs=0
+ mjc=0.33      mje=0.33                 mjs=0.5
+ vjc=.89       vje=.85         vjs=.75
+ itf=4.6e-6    tf=2.6e-10      tr=3e-10
+ vtf=0         xtf=0           nkf=0.5
*
*
*       silicon-germanium transistor models
*
* transistor models
.model qnsige NPN level=1  subs=1  update=0
+ bf=85         br=85           ibc=2e-15
+ ibe=2e-15
+ nf=1.05       nr=1.1          isc=7e-18
+ ise=9e-17     nc=2            ne=1.5
+ vaf=100       var=100         ikf=1.5e-5
+ ikr=1.5e-5    irb=0           rb=500
+ rbm=500       re=100          rc=100
+ cjc=1.7e-16   cje=6e-16       cjs=0
+ mjc=0.33      mje=0.33                 mjs=0.5
+ vjc=.87       vje=.84         vjs=.75
+ itf=2e-4      tf=1.4e-11      tr=1.4e-11
+ vtf=0         xtf=0           nkf=0.5
*
*
.model qpsige PNP level=1  subs=1  update=1
+ bf=5          br=5            ibc=1e-16
+ ibe=1e-16
```

```
+ nf=1.105      nr=1.2        isc=0
+ ise=1e-15     nc=2          ne=1.5
+ vaf=50        var=50        ikf=1e-4
+ ikr=1e-4      irb=0         rb=500
+ rbm=500       re=100        rc=100
+ cjc=1.8e-16   cje=7e-16     cjs=0
+ mjc=0.33      mje=0.33              mjs=0.5
+ vjc=.89       vje=.85       vjs=.75
+ itf=2e-5      tf=2.6e-11    tr=3e-11
+ vtf=0         xtf=0         nkf=0.5
*
*
*
*       silicon-germanium transistor models
*               SCALED:
*               base-collector junction: 3um x 3um
*               base-emitter junctin:    9um x 5um
* transistor models
.model qnsige_s NPN level=1  subs=1  update=0
+ bf=85         br=85         ibc=6e-15
+ ibe=6e-15
+ nf=1.05       nr=1.1        isc=21e-18
+ ise=27e-17    nc=2          ne=1.5
+ vaf=100       var=100       ikf=4.5e-5
+ ikr=4.5e-5    irb=0         rb=500
+ rbm=500       re=100        rc=100
+ cjc=1.53e-15  cje=2.7e-14   cjs=0
+ mjc=0.33      mje=0.33              mjs=0.5
+ vjc=.87       vje=.84       vjs=.75
+ itf=2e-4      tf=1.4e-11    tr=1.4e-11
+ vtf=0         xtf=0         nkf=0.5
*
*
.model qpsige_s PNP level=1  subs=1  update=1
+ bf=5          br=5          ibc=3e-16
+ ibe=3e-16
+ nf=1.105      nr=1.2        isc=0
+ ise=3e-15     nc=2          ne=1.5
+ vaf=50        var=50        ikf=3e-4
+ ikr=3e-4      irb=0         rb=500
+ rbm=500       re=100        rc=100
+ cjc=1.62e-15  cje=3.15e-14  cjs=0
+ mjc=0.33      mje=0.33              mjs=0.5
+ vjc=.89       vje=.85       vjs=.75
+ itf=2e-5      tf=2.6e-11    tr=3e-11
+ vtf=0         xtf=0         nkf=0.5
*
*
*
*       silicon mesfet transistor models
*
```

```
.model jpfet pjf level=2
+ acm=0 align=0 hdif=0.5u is=2.7e-18 L=2u
+ ldel=0 ldif=0.5u n=1.1 rd=1300
+ rg=650 rs=1300 rsh=10 rshg=0.5 rshl=10k
+ w=1u wdel=0 capop=0 cgd=1e-17
+ cgs=1e-17 gcap=1e-15 m=0.5 pb=0.9
+ tt=0 beta=1.5e-5 lambda=0 nd=1
+ ng=1 vto=0.32
*
*
.model jnfet njf level=2
+ acm=0 align=0 hdif=0.5u is=2e-14 L=2u
+ ldel=0 ldif=0.5u n=1.1 rd=1300
+ rg=650 rs=1300 rsh=10 rshg=0.5 rshl=10k
+ w=1u wdel=0 capop=0 cgd=1e-17
+ cgs=1e-17 gcap=1e-15 m=0.5 pb=0.9
+ tt=0 beta=2e-5 lambda=0 nd=1
+ ng=1 vto=0.20
*
*
*        SCALED: silicon mesfet transistor models
*
.model jpfet_s pjf level=2
+ acm=0 align=0 hdif=0.5u is=5.4e-18 L=2u
+ ldel=0 ldif=0.5u n=1.1 rd=1300
+ rg=650 rs=1300 rsh=10 rshg=0.5 rshl=10k
+ w=2u wdel=0 capop=0 cgd=2e-17
+ cgs=2e-17 gcap=2e-15 m=0.5 pb=0.9
+ tt=0 beta=1.5e-5 lambda=0 nd=1
+ ng=1 vto=0.32
*
*
.model jnfet_s njf level=2
+ acm=0 align=0 hdif=0.5u is=4e-14 L=2u
+ ldel=0 ldif=0.5u n=1.1 rd=1300
+ rg=650 rs=1300 rsh=10 rshg=0.5 rshl=10k
+ w=2u wdel=0 capop=0 cgd=2e-17
+ cgs=2e-17 gcap=2e-15 m=0.5 pb=0.9
+ tt=0 beta=2e-5 lambda=0 nd=1
+ ng=1 vto=0.20
*
*
*
*        SCALED: silicon mesfet transistor models
*                test devices to see if reducing the
*                barrier affects the circuit operation
*
.model jpfet_test pjf level=2
+ acm=0 align=0 hdif=0.5u is=5.4e-18 L=2u
+ ldel=0 ldif=0.5u n=1.1 rd=1300
+ rg=650 rs=1300 rsh=10 rshg=0.5 rshl=10k
```

```
+ w=2u wdel=0 capop=0 cgd=2e-17
+ cgs=2e-17 gcap=2e-15 m=0.5 pb=0.2
+ tt=0 beta=1.5e-5 lambda=0 nd=1
+ ng=1 vto=0.32
*
*
.model jnfet_test njf level=2
+ acm=0 align=0 hdif=0.5u is=4e-14 L=2u
+ ldel=0 ldif=0.5u n=1.1 rd=1300
+ rg=650 rs=1300 rsh=10 rshg=0.5 rshl=10k
+ w=2u wdel=0 capop=0 cgd=2e-17
+ cgs=2e-17 gcap=2e-15 m=0.5 pb=0.2
+ tt=0 beta=2e-5 lambda=0 nd=1
+ ng=1 vto=0.20
*
*
* N37C  SPICE LEVEL 2 PARAMETERS
*
*  0.3V threshold devices
*
.MODEL N20_vt3 NMOS LEVEL=2 PHI=0.600000 TOX=1.5000E-08 XJ=0.200000U TPG=1
+ VTO=0.3 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08
*
*
.MODEL P20_vt3 PMOS LEVEL=2 PHI=0.600000 TOX=1.5000E-08 XJ=0.200000U TPG=-1
+ VTO=-0.3 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07
*
*
*        GaAs FET Models
*            parameters from "The Potential of Complementary Hetero-
*            structure FET ICs", R. Keihl, IEEE Trans. on Elec. Dev.,
*            ED-34, no. 12, p2412, 1987.
*
*            scaled GaAs FETs width=3u
*
.model jpgaas_s pjf level=2
+ acm=0 align=0 hdif=0.5u is=7.5e-18 L=0.7u
```

```
+ ldel=0  ldif=1.0u  n=1.1  rd=1300
+ rg=650  rs=1300  rsh=10  rshg=0.5  rshl=10k
+ w=1u  wdel=0  capop=1  cgd=.75e-15
+ cgs=.75e-15  gcap=15e-16  m=0.5  pb=0.9
+ tt=0  beta=4.6e-5  lambda=0  nd=1
+ ng=1  vto=0.4
*
*
.model jngaas_s  njf  level=2
+ acm=0  align=0  hdif=0.5u  is=7.5e-18  L=0.7u
+ ldel=0  ldif=1.0u  n=1.1  rd=1300
+ rg=650  rs=1300  rsh=10  rshg=0.5  rshl=10k
+ w=1u  wdel=0  capop=0  cgd=.75e-15
+ cgs=.75e-15  gcap=15e-16  m=0.5  pb=0.9
+ tt=0  beta=2.3e-4  lambda=0  nd=1
+ ng=1  vto=0.40
*
```

APPENDIX C

SUPREM III INVERTED BIPOLAR PROCESS SIMULATION INPUT FILES

Title	Suprem-III REL Bipolar Process
$	High Energy Ion Implantion Process
$	Roxann Russell Blanchard 24 March 1994
$	File: pnp_col.in
Comment	Starting with pepi substrate
Initialize	Structure=psub.structure Thickness=3
Comment	Thin Oxide for implant - Diffusion #1
Comment	RCA Clean
Diffusion	Temperature=950 Time=35 DryO2
Comment	Pattern NPN Emitter
Comment	NPN Emitter Ion Implantation
Comment	Arsenic Dose=1e15 Energy=35
Comment	Resist Ash
$	O2 plasma, 25 min.
Comment	Emitter drive Diffusion #2
Comment	RCA Clean
Diffusion	Temperature=1050 Time=50 Nitrogen
Etch	Oxide
Comment	RCA Clean
Comment	Deposit 1.7um of nepi
Epitaxy	Temperature=1050 Time=4.25 Growth.Rate=.4
+	Phosphorus Gas.Conc=1e15
Comment	Thin oxide for implant - Diffusion #1
Diffusion	temperature=950 time=35 DryO2
Comment	Pattern Pwell
Comment	Implant Boron for Pwell for PNP transistor
Implant	Boron Dose=1e12 Energy=160
Implant	BF2 Dose=5e11 Energy=30

| Comment | Resist Ash |
| $ | OI2 plasma, 25 min. |

| Etch | Oxide |

Comment	Stress Relief Oxide		
Diffusion	Temperature=950	Time=100	DryO2
Diffusion	Temperature=950	Time=30		Nitrogen

Comment	LPCVD Silicon Nitride (150nm)
$	750C, SiH2Cl2 and NH3
Deposit	Nitride Thickness=0.15

Comment	Pattern Active areas
Comment	Nitride plasma (lam etcher)
Etch	Nitride

Comment	P-Field Pattern
Comment	P-field ion implant
Comment	Boron Dose=1e13 Energy=30

| Comment | Resist ash |
| $ | O2 plasma, 25 min. |

Comment	N-field Pattern
Comment	N-field Ion Implant
Comment	Phosphorus Dose=3e12 Energy=40

| Comment | Resist Ash |
| $ | O2 plasma, 25 min. |

Comment	Well Drive-in : LOCOS ~500nm
Diffusion	Temperature=950 Time=30 DryO2
Diffusion	Temperature=950 Time=150 WetO2
Diffusion	Temperature=950 Time=30 DryO2
Diffusion	Temperature=950 Time=180 Nitrogen

| Comment | Nitride plasma etch |
| $ | SF6 + He plasma, 40 sec. |

| Comment | SRO removal |
| Etch | Oxide |

| Comment | Resist Ash |
| $ | O2 pasma, 25 min. |

Comment	Thin oxide for implant - Diffusion #1
Comment	RCA Clean
Diffusion	Temperature=950 Time=35 DryO2

Comment	Pattern PNP Base		
Comment	Implant Phos for PNP Base		
Implant	Phosphorus	Dose=3e13	Energy=500
Implant	Phosphorus	Dose=2e12	Energy=150

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Pattern NPN Base		
Comment	Implant Boron for NPN Base		
Comment	Boron Dose=2e13	Energy=170	
Comment	Boron Dose=5e11	Energy=30	

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Drive in base implants: Diffusion #5
Diffusion	Temperature=950 Time=120 Nitrogen

Comment	Pattern NPN collector		
Comment	Implant NPN collector		
Comment	Phosphorus	Dose=4e13	Energy=200
Comment	Phosphorus	Dose=5e11	Energy=30

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Drive in NPN collector implant: Diffusion #6
Diffusion	Temperature=975 time=100 Nitrogen

Comment	Pattern PNP collector		
Comment	Implant PNP collector		
Implant	Boron Dose=2.5e13	Energy=160	
Implant	Boron Dose=9e12	Energy=30	

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Pattern PNP Emitter	
Comment	Implant PNP Emitter	
Implant	Boron Dose=7e13	Energy=600

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Emitter Drive/ Anneal: Diffusion #6
Comment	RCA clean
Diffusion	Temperature=975 time=100 Nitrogen

Comment	LPCVD polysilicon (500 nm)
Comment	temperature=625, SiH4

Comment	Phosphorus deposition 120nm (POCl3)
Diffusion	temperature=925 time=60 Nitrogen
Diffusion	temperature=925 time=15 DryO2
Diffusion	temperature=925 time=10 Nitrogen
Comment	phosphorus glass wet etch
Comment	Pattern polysilicon
Comment	Plasma etch
Comment	Resist ash
Comment	Pattern N+ Implant
Comment	N+ Ion Implant - Contact
Comment	Arsenic Dose=1e16 Energy=35
Comment	Resist Ash
$	O2 plasma, 25 min.
Comment	Pattern P+ Implant
Comment	P+ Ion Implant - Contact
Implant	BF2 Dose=7e15 Energy=30
Comment	Thin oxide for capacitor
Comment	RCA clean
Diffusion	Temperature=900 time=30 DryO2
Diffusion	Temperature=900 time=15 Nitrogen
Comment	BPSG deposition
$	450C, 100 nm undoped, 500nm doped
Comment	BPSG reflow
Diffusion	temperature=925 time=15 DryO2
Comment	resist coat
$	backside wet etch
$	backside poly plasma etch
$	backside oxide wet etch
$	resit ash
Comment	Contact pattern
Comment	Contact wet clean
Comment	Resist Ash
Comment	RCA clean
Comment	Metal depostion (1um)
Comment	Metal pattern
Comment	Metal plasma etch
Comment	Resist ash
Comment	Sinter (425C, 5 min.)

Stop

Title	Suprem-III REL Bipolar Process
$	Low Energy Ion Implantion Process
$	Roxann Russell Blanchard 24 March 1994
$	File: pnp_lowE.in

Comment   Starting with pepi substrate
Initialize   Structure=psub.structure Thickness=3

Comment   Stress Relief Oxide
Diffusion   Temperature=950   Time=100   DryO2
Diffusion   Temperature=950   Time=30   Nitrogen

Comment   LPCVD Silicon Nitride (150nm)
$ 750C, SiH2Cl2 and NH3
Deposit   Nitride   Thickness=0.15

Comment   Pattern npn emitter area
Comment   Nitride plasma (lam etcher)
Comment   Etch Nitride

Comment   Pattern NPN Emitter
Comment   NPN Emitter Ion Implantation
Comment   Phosphoru dose=5e14 energy=35

Comment   Resist Ash
$ O2 plasma, 25 min.

Comment   Emitter drive   Diffusion #2
Comment   RCA Clean
Diffusion   Temperature=1050 Time=50 Nitrogen

Comment   Thin oxide for implant
Diffusion   temperature=950 time=35 DryO2

Comment   Etch Nitride from pnp emitter area
Comment   Nitride plasma (lam etcher)
etch   oxide
Etch   Nitride

Comment   Pattern PNP Emitter
Comment   Implant PNP Emitter
Implant   Boron   Dose=3e14   Energy=30

Comment   Resist Ash
$ O2 plasma, 25 min.

Comment   pnp Emitter Drive/ Anneal
Comment   RCA clean

Diffusion	Temperature=975 time=100 Nitrogen
etch	oxide
Comment	RCA Clean
Comment	Deposit 1.7um of nepi
Epitaxy	Temperature=1050 Time=4.25 Growth.Rate=.4
+	Phosphorus Gas.Conc=1e15
Comment	Thin oxide for implant
Diffusion	temperature=950 time=35 DryO2
Comment	Pattern Pwell
Comment	Implant Boron for Pwell for PNP transistor
Implant	BF2 Dose=3e11 Energy=30
Implant	Boron Dose=3e12 Energy=200
Comment	Resist Ash
$	O2 plasma, 25 min.
Etch	Oxide
Comment	Stress Relief Oxide
Diffusion	Temperature=950 Time=100 DryO2
Diffusion	Temperature=950 Time=30 Nitrogen
Comment	LPCVD Silicon Nitride (150nm)
$	750C, SiH2Cl2 and NH3
Deposit	Nitride Thickness=0.15
Comment	Pattern Active areas
Comment	Nitride plasma (lam etcher)
Etch	Nitride
Comment	P-Field Pattern
Comment	P-field ion implant
Comment	Boron Dose=1e13 Energy=30
Comment	Resist ash
$	O2 plasma, 25 min.
Comment	N-field Pattern
Comment	N-field Ion Implant
Comment	Phosphorus Dose=3e12 Energy=40
Comment	Nitride plasma etch
$	SF6 + He plasma, 40 sec.
Comment	SRO removal
Etch	Oxide

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Well Drive-in : LOCOS ~500nm
Diffusion	Temperature=950 Time=30 DryO2
Diffusion	Temperature=950 Time=150 WetO2
Diffusion	Temperature=950 Time=30 DryO2
Diffusion	Temperature=950 Time=180 Nitrogen

Comment	Pattern PNP Base
etch	oxide

Comment	Thin oxide for implant - Diffusion #1
Comment	RCA Clean
Diffusion	Temperature=950 Time=35 DryO2

Comment	Implant Phos for PNP Base		
Implant	Phosphorus	Dose=3e13	Energy=200
Implant	Phosphorus	Dose=2e12	Energy=100

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Pattern NPN Base		
Comment	Implant Boron for NPN Base		
Comment	Boron	Dose=2e13	Energy=170
Comment	Boron	Dose=5e11	Energy=30

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Drive in base implants: Diffusion #5
Diffusion	Temperature=950 Time=120 Nitrogen

Comment	Pattern NPN collector		
Comment	Implant NPN collector		
Comment	Phosphorus	Dose=4e13	Energy=200
Comment	Phosphorus	Dose=5e11	Energy=30

Comment	Resist Ash
$	O2 plasma, 25 min.

Comment	Drive in NPN collector implant: Diffusion #6
Diffusion	Temperature=975 time=100 Nitrogen

Comment	Pattern PNP collector		
Comment	Implant PNP collector		
Implant	Boron	Dose=2e13	Energy=60
Implant	BF2	Dose=9e12	Energy=30

| Comment | Resist Ash |
| $ | O2 plasma, 25 min. |

| Comment | LPCVD polysilicon (500 nm) |
| Comment | temperature=625, SiH4 |

Comment	Phosphorus deposition 120nm (POCl3)
Diffusion	temperature=925 time=60 Nitrogen
Diffusion	temperature=925 time=15 DryO2
Diffusion	temperature=925 time=10 Nitrogen

| Comment | phosphorus glass wet etch |

Comment	Pattern polysilicon
Comment	Plasma etch
Comment	Resist ash

Comment	Pattern N+ Implant
Comment	N+ Ion Implant - Contact
Comment	Arsenic Dose=1e16 Energy=35

| Comment | Resist Ash |
| $ | O2 plasma, 25 min. |

| Comment | Thin oxide for implant |
| Diffusion | temperature=950 time=35 DryO2 |

Comment	Pattern P+ Implant
Comment	P+ Ion Implant - Contact
Implant	BF2 Dose=1e15 Energy=30

| etch | oxide |

Comment	Thin oxide for capacitor
Comment	RCA clean
Diffusion	Temperature=900 time=30 DryO2
Diffusion	Temperature=900 time=15 Nitrogen

| Comment | BPSG deposition |
| $ | 450C, 100 nm undoped, 500nm doped |

| Comment | BPSG reflow |
| Diffusion | temperature=925 time=15 DryO2 |

Comment	resist coat
$	backside wet etch
$	backside poly plasma etch
$	backside oxide wet etch
$	resit ash

| Comment | Contact pattern |

Comment   Contact wet clean
Comment   Resist Ash
Comment   RCA clean

Comment   Metal depostion (1um)
Comment   Metal pattern
Comment   Metal plasma etch

Comment   Resist ash
Comment   Sinter (425C, 5 min.)

Stop