A High Bandwidth, Low Distortion, Fully Differential Amplifier

by

David Michael Signoff

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

An amplifier for use in driving an analog to digital converter in an ultra-wideband test system was designed and simulated. The amplifier has differential inputs and outputs and a bandwidth of greater than 500 MHz. According to simulation, the linearity for frequencies above 100 MHz is ten times better than amplifiers currently on the market. The design of this amplifier involved: studying impacts of circuit topology on linearity, creating a schematic design, getting a package model, laying out the die and extracting parasitics, and creating simulation tests.

Thesis Supervisor: William Bowhers
Title: VI-A Company Thesis Supervisor

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Acknowledgments

I gratefully thank William Bowhers and Allan Parks for their guidance and for all that they have taught me. In particular, I would like to thank Bill for giving me the opportunity to work on this project, the time he spent answering my questions about circuit and system design and his aid in searching for help when he did not have the answer. I would like to thank Al for the many hours he spent on the phone instructing me in the ways of analog integrated circuit design.

I appreciate Regan Mills organizing and providing guidance throughout my VI-A experience. I also thank the many other members of Teradyne who contributed to this project and introduced me to the world of automatic test equipment.

I would like to thank Professor Charles Sodini for his advice and the time he spent helping me improve this document.

Special thanks to my parents for their love and inspiration and Susanna Thon for her help, encouragement, and for fixing my many run-on sentences. Finally, I would like to express my gratitude to my family and friends for their support.

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Chapter 1

Introduction

1.1 Overview

This thesis describes the design and simulation of a high bandwidth, low distortion, fully differential amplifier intended for driving an analog to digital converter in a prototype of an Ultra-Wideband test system. Background and motivation are provided in Chapters 1 and 2, along with the target specifications for the amplifier. Chapter 3 provides the current schematic design along with some discussion about how it was chosen. Information about the fabrication process, IBM 5HP, and an explanation of which elements from the process were used is in Chapter 4. The chosen package and the package model used for simulation are discussed in Chapter 5. Chapter 6 shows the layout of the chip and explains how trade-offs were made in its creation. Chapter 7 explains how simulations were performed and their results are stated and discussed in Chapter 8. A summary and suggested future work are in Chapter 9. A block diagram of the chip, which is the subject of this thesis, along with supporting circuitry and the ADC it is intended to drive are shown in Figure 1-1.

1.2 Contributions to This Work

The work described in this thesis was performed at Teradyne Inc. as part of a broad project led by William Bowhers to build a prototype of an Ultra-Wideband test

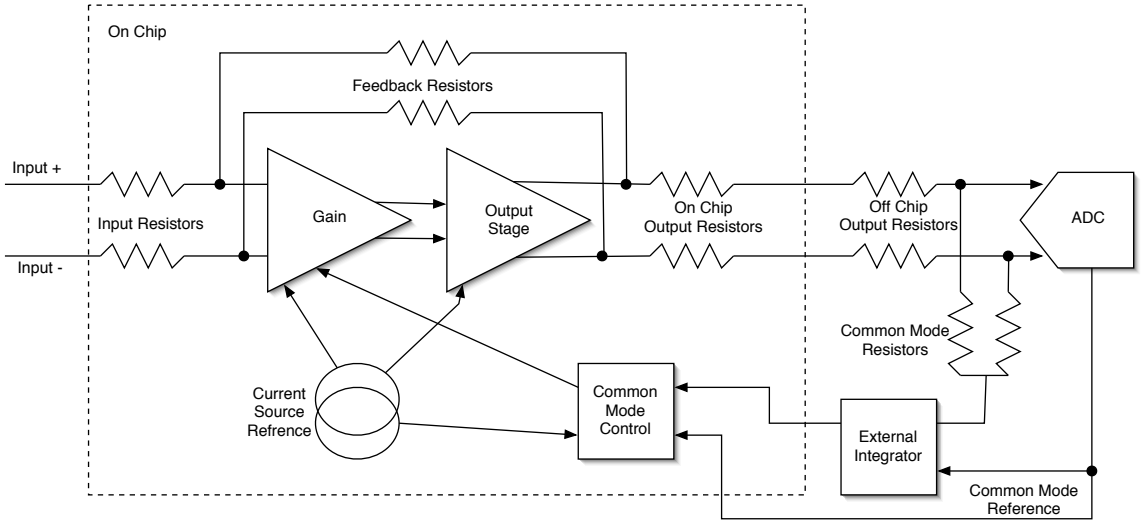

Figure 1-1: Block Diagram of Amplifier and Surrounding Parts

system. Bowhers discovered the need for the project detailed in this thesis and created the most important specifications.

The main contributors to this project were Allan Parks and myself. We worked together on nearly all aspects of this project. Parks took a larger role in creating the architecture and getting package information, while I concentrated more on the schematic design details and layout.

A number of other people also contributed to this project. Yeong-Joo Yoon created the package model. Nathan Altaffer and Earl Shaw set up the Cadence tools and assisted Parks and me in their use. Paul Allen characterized the kickback from the ADCs. Arne Buck and Keith Mullen provided advice on modeling and reducing noise. Alzeem Aziz from Cadence provided advice on improving the accuracy of the harmonic simulations. Grant Kesselring from IBM suggested the ESD protection scheme for the 15 V power supply pin.

1.3 Ultra-Wideband

In 2002 the Federal Communications Commission (FCC) allocated 7.5 GHz of the spectrum, from 3.1 to 10.6 GHz, for unlicensed use of ultra-wideband (UWB) devices, where ultra-wideband is defined as any signal occupying more than 500 MHz in that band [8] [9] [10]. The limit on these signals is power spectral density (PSD) ≤ -40 dBm/MHz.

Shannon's Theorem says $C \leq Wlog_2(1 + S/N)$, where C = maximum number of bits per second, W = bandwidth, and S/N = signal to noise ratio. This means that if a large bandwidth is used, high speed communication can be achieved even if the signal is barely above the noise floor. The maximum power spectral density chosen by the FCC makes UWB a poor choice for long distance communication, but, as shown by Shannon's Theorem, it is a good choice for high speed personal area networks and short range communication such as wireless USB.

The two main methods for using the spectrum are pulsed and orthogonal frequency division multiplexing (OFDM). In the pulsed method, data is sent as an impulse train and uses the entire 7.5 GHz as one channel. This is very different from traditional narrow band communication where the communication band is a small portion of the carrier frequency, so this method requires new circuit blocks and techniques. OFDM splits the 7.5 GHz into 500 MHz channels. The 500 MHz channels are closer to standard narrow band as compared to the pulsed method. Using many channels in parallel is an improvement over standard narrow band. One advantage of this method is that if there is a very strong signal in one particular channel, that channel can just be dropped. Additionally the circuits used for the OFDM method need fairly large bandwidths, but are not radically different from traditional narrow band circuit techniques. Devices using each of these standards will be reaching the market soon.

1.4 Overall System

1.4.1 Automatic Test Equipment

Teradyne designs automatic test equipment (ATE) for the semiconductor industry. Their main challenge is to have enough accuracy and speed to measure signals from state of the art integrated circuits and those that will be made in the near future. They have several advantages that allow them to beat the performance of the integrated circuits, such as power consumption, size, adding circuitry for calibration, and time for multiple runs in order to reduce noise.

The enabling technologies group at Teradyne look at the hard problems Teradyne will face in the future and learns how to solve them. It then passes this knowledge on to the product groups who can more rapidly design a test system. Most of this learning is accomplished by making prototypes of what the product groups will need to build. The goal in building these prototypes is to show how to solve the difficult problems.

As UWB devices appear in the market, Teradyne wants to be ready to provide a testing solution for their present and future components. That means they need a system that meets the bandwidth requirements and has better accuracy than what they expect from these devices over the next several years. In order to test a device, the system needs to provide signals to the device under test (DUT) and measure signals the DUT generates. In general, providing a precision signal is easier than measuring a signal with the same precision, so Teradyne is concentrating on improving the measurement side. The main approach for measuring a signal is to put it through an analog signal chain which drives an analog to digital converter (ADC). Once the signal is digital, it can be stored to memory and then the user can perform whatever processing is desired.

1.4.2 System Overview

In order to learn how to make a system that can measure signals from an OFDM UWB device, an enabling technologies project was started. This project is a circuit board containing the analog signal chain and the digital circuitry necessary to move the signal to a computer. Looking at the analog signal chain from the end, this project requires an ADC with a bandwidth greater than 500 MHz, a sampling rate around 1500 MS/s, and a reasonably large number of bits. Since there are no off-the-shelf parts that meet these specifications, methods of combining ADCs are being investigated. There are several ways of using lower performance ADCs together to make a high performance ADC. Two examples of such combining techniques are interleaving and pipelining.

1.4.3 Analog Signal Chain

There are several reasons why the DUT cannot directly drive the ADCs, and each helps shape the required signal chain. The size of the signal coming from the DUT will vary from device to device, but in order to utilize the full precision of the ADC, the input signal needs to be attenuated or amplified to make the peak voltage as close to the input voltage range of the ADC as possible. In order to accomplish this, an attenuator followed by a selectable gain amplifier is used. The measurement system should not affect the signal from the DUT, so a high impedance or 50 Ω input impedance is required at the beginning of the chain. This signal chain is shown in Figure 1-2.

Since there are multiple amplifiers, the gain needs to be divided along the signal chain. The main concerns in designing the signal chain are bandwidth, noise, and linearity. The bandwidth specification is not very difficult to meet so it does not affect where to put the gain. In order to minimize input referred noise, the gain should be placed as early in the chain as possible. The linearity of each stage gets worse as its output voltage swing increases. The last element in the chain needs to have the full output swing, but if it has gain then the previous stages can have smaller output

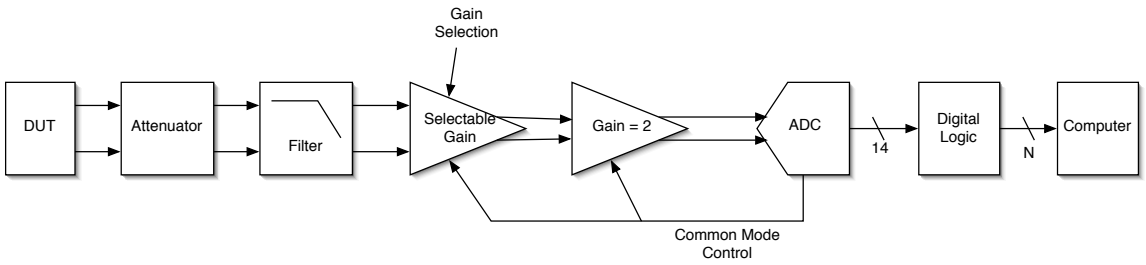

Figure 1-2: Overall System Signal Chain

swings and thus better linearity. Hence, the distribution of gain through the signal chain involves a trade-off between noise and linearity. As will be shown later, linearity is a greater concern in this project. This led to the choice of having a gain of two amplifier directly drive an ADC, which will increase the noise but improve linearity. This ADC driver is the amplifier described in this thesis.

An amplifier directly driving the ADC can be physically placed very close to it, and thus transmission line effects can be ignored for the output of the amplifier. However, due to the requirements of the overall system, the input should be 400 Ω differential.

1.4.4 Analog to Digital Converter

An ADC with high sample rate, bandwidth and linearity is required for the overall system. There are several examples of such ADCs, such as the MAX1430 [11], ADS5500 [1], and AD6645 [12]. The ADS5500 is one of the better ones. Traditionally, the ADC is the performance limiting element in the signal chain. However, recent ADCs, such as the ADS5500, have exceeded the amplifiers that drive them in high frequency linearity. Since amplifiers are now the limiting elements, the goal is to improve their performance enough so that it is at least comparable to that of the ADC. Increasing the performance of the amplifier beyond this point has diminishing returns.

The ADC will be similar to the ADS5500 which is a 14 bit, 125 MS/s ADC with a 750 MHz bandwidth from Texas Instruments [1]. The input has a 2.3 V_{pp} differential

input voltage range. Its input impedance is a 6 kΩ resistance in parallel with a 4 pF capacitance. It supplies a common mode reference voltage; the common mode input needs to match this reference to within 1 mV or else its linearity degrades. See Figure 1-3 for the spurious free dynamic range versus frequency, Table 1.1 for typical harmonics, and Figure 1-4 for the signal to noise ratio versus frequency.

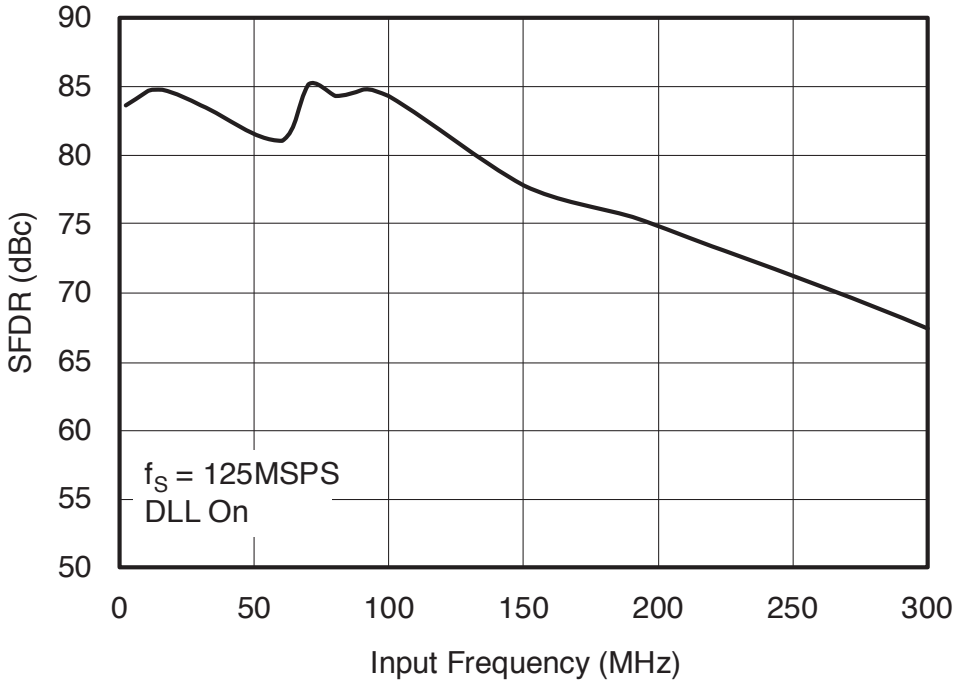

Figure 1-3: ADS5500 Spurious Free Dynamic Range vs. Frequency [1]

Table 1.1: ADS5500 Harmonics [1]

Freq [MHz]	**HD2** [dBc]	**HD3** [dBc]
10	-91	-89
30	-86	-90
55	-84	-79
70	-87	-85
100	-84	-82
150	-78	-80
225	-74	-76

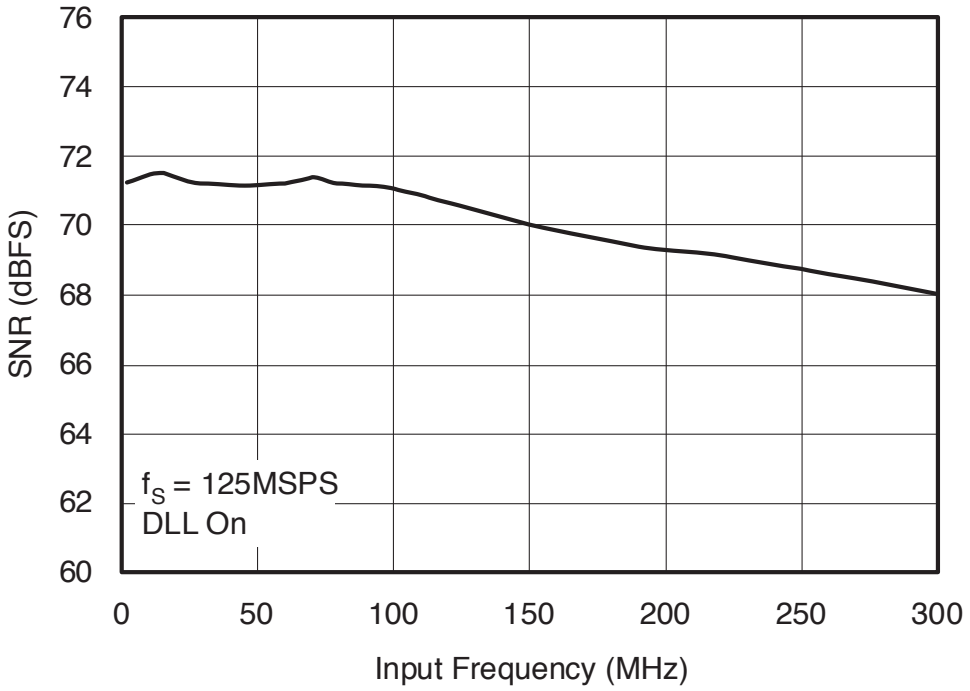

Figure 1-4: ADS5500 Signal to Noise Ratio vs. Frequency [1]

Chapter 2

ADC Driver Specifications

2.1 Desired Specifications

The desired specifications for this amplifier come from several sources. The main source is the overall system's need for a gain of two amplifier that can drive a high performance ADC. This incorporates the specifications of the rest of the system as well as those of the ADC. Additionally, looking at what is on the market gives a range of what is reasonable for specifications other than linearity, bandwidth and gain. For some specifications, such as DC concerns and power dissipation, the requirements for this amplifier are much more lenient than what is on the market. This leniency is due to test systems having different priorities than most electronics systems. The most important specifications are shown in Tables 2.1 and 2.2.

There are many ways to quantify linearity. The three metrics used for this project are the second and third harmonics (HD2 and HD3) and the intermodulation distortion (IMD). The Fourier transform of the output contains a component at the frequency of the input, the fundamental, and components at each integer multiple of that frequency. The second harmonic is measured as the component at twice the fundamental frequency divided by the component at the fundamental. The third harmonic is the same except at three times the fundamental. Further harmonics are not required, because in most systems the higher order even harmonics will be less than HD2 and the odd will be less than HD3. When two tones of nearly equal fre-

Table 2.1: Frequency Dependent Specifications

Freq [MHz]	**HD2** [dBc]	**HD3** [dBc]	**IMD** [dBc]	**Noise** $\left[\frac{nV}{\sqrt{Hz}}\right]$
0.3	-93	-93	-93	n/a
1	-91	-91	-91	5
3	-90	-90	-90	5
10	-88	-88	-88	5
30	-85	-85	-85	5
100	-79	-79	-79	5
300	-65	-65	-65	5
500	-58	-58	-58	5

Table 2.2: Frequency Independent Specifications

Specification	**Value**
Gain	2
Bandwidth [MHz]	750
Power [W]	< 1
Main Loop Phase Margin [^{o}]	> 60
Main Loop Gain Margin [dB]	> 10
Common Mode Loop Phase Margin [^{o}]	> 60
Common Mode Loop Gain Margin [dB]	> 10
Output Common Mode Accuracy [mV]	< 1
Output Common Mode Range [mV]	> 100
Differential Input Impedance [Ω]	400
Power Supply and Common Mode Rejection Ratios [dB]	> 20

quency (f_1 and f_2) are passed through the amplifier, there will be components of the Fourier transform at $2f_1 - f_2$ and $2f_2 - f_1$, due to the third order distortion. These components are compared to the fundamental in the same way the second and third harmonics are to get the IMD value. This value is particularly important if the input is a narrow band signal because the distortion will be in the band. HD2 and HD3 are more important in an UWB system than in a narrow band system because for all but the highest fundamentals these harmonics will be in band. The specifications for these metrics come from trying to match the performance of the available ADCs, which is approximately 20 dB better than amplifiers on the market for signals at 100 MHz.

Since some ADCs have a common mode reference voltage that must be met to within 1 mV, the amplifier must be able to match the reference to that precision over the ADC's specified range.

The outputs of this amplifier can be placed very close to the inputs of the ADC so there is no need to match a transmission line at the output of the amplifier. Because the input of the ADC includes a fairly large capacitance the output impedance of this amplifier has a strong influence on its frequency response. Thus, the output impedance can be used to adjust the bandwidth and amount of peaking in the frequency response. The overall system requires this amplifier to have a 400 Ω differential input impedance. Even if that was not a requirement, this is a good choice of input impedance, since the input and feedback resistors are the most significant contributors of noise in the amplifier. Therefore, they should be as small as possible; however, this amplifier has to drive the feedback resistors so they should not be too small. A 400 Ω differential input impedance is a good compromise between these factors.

The overall system is designed for signals with a 500 MHz bandwidth. In order to meet this bandwidth requirement, each component on the chain must have a bandwidth greater than 500 MHz. Considering the number of components on the chain, this amplifier's bandwidth should be quite a bit larger than 500 MHz. It is tempting to make the bandwidth as large as possible, but there is no filter between this

amplifier and the ADC so excess bandwidth just results in more noise at the output. Thus, the bandwidth needs to be able to be trimmed based on the requirements of the overall system. A good estimate is 750 MHz.

The noise requirements for this amplifier are not particularly strict since it comes after most of the gain of the signal chain, although it should not have an unreasonable amount of noise. From looking at the noise specifications of other amplifiers on the market, 5 $\frac{nV}{\sqrt{Hz}}$ is a reasonable but not cutting edge goal. This also happens to be about one least significant bit of a 2 V_{pp}, 14 bit ADC, assuming a bandwidth of 500 MHz.

As will be shown in Section 2.2, no commercially available amplifiers that meet these specifications were found. Thus, the project which is the subject of this thesis was started. This project is an integrated circuit designed to meet the above specifications. The rest of this thesis describes the design and testing of this amplifier.

2.2 Amplifiers on the Market

Table 2.3 is taken from the ADS5500 datasheet. This table is a good starting point for a search for an amplifier to drive a high performance ADC. Note that most of the amplifiers in this table are single-ended, so a transformer is recommended. Unfortunately, transformers do not work well for low frequency signals and are not very ideal in general. There are, however, circuit configurations that can use two single-ended amplifiers to make one differential amplifier, so it is still worth investigating the performance of single-ended amplifiers.

The THS9001 [13] has a bandwidth from 50 MHz to 350 MHz. This range does not extend to DC and is too small, so it can be eliminated immediately. The THS4503 [14] also does not meet the bandwidth specification as its gain of two bandwidth is 175 MHz.

The THS3201 [15], THS3202 [16] and OPA695 [17] are all single-ended current feedback operational amplifiers. All three have significantly larger harmonics at 100 MHz than the target for this project. Part of the issue is that their second

harmonics are particularly bad, probably because they are not differential.

Table 2.3: Recommended Amplifiers to Drive the Input of the ADS5500 [1]

Frequency	**Recommended Amplifier**	**Type of Amplifier**	**Use With Transformer**
DC to 20 MHz	THS4503	Differential In/Out Amp	No
DC to 50 MHz	OPA847	Operational Amp	Yes
10 MHz to 120 MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
> 100 MHz	THS9001	RF Gain Bock	Yes

2.2.1 KH600

The KH600 [2] is a current feedback amplifier and is the commercial amplifier that comes closest to the desired specifications. It has differential inputs and outputs both of which are matched to 100 Ω differential. The bandwidth with a 2 V_{pp} output is 1 GHz and the gain is 14 dB. Also, it has output common mode control. The input noise is less than 2 $\frac{nV}{\sqrt{Hz}}$. Since the amplifier drives 100 Ω differential, it has to drive a smaller impedance than a 6 pF capacitor for low frequencies. After 265 MHz, the capacitor is a smaller impedance. Additionally, it is easier to avoid oscillations when driving a resistive load. These considerations should be taken into account when comparing harmonics. The KH600's harmonic distortion is shown in Figure 2-1 and is approximately 20 dB worse than what is required for this project at around 100 MHz.

2.2.2 LMH6702

The LMH6702 [3], a current feedback amplifier, has about the same linearity as the KH600. It does not meet the requirement of differential outputs but has impressive input noise and harmonics. The input noise is 1.8 $\frac{nV}{\sqrt{Hz}}$. The harmonics are shown in Figure 2-2. The harmonics are measured with a 2 V_{pp} output across a 100 Ω load. The amplifier and load are single-ended rather than differential, but since the current will

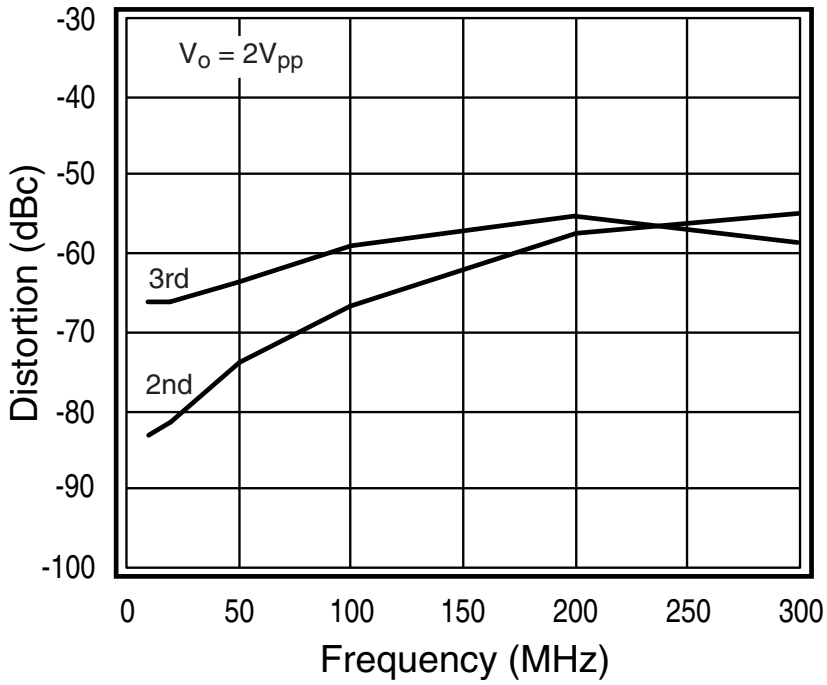

Figure 2-1: KH600's Harmonic Distortion vs Frequency[2]

be the same as in the test conditions for the KH600, this is a reasonable comparison between the two amplifiers. The same differences between the LMH6702's test and the project requirements need to be taken into account as for the KH600. Again, around 100 MHz the harmonics are approximately 20 dB worse than this project's target.

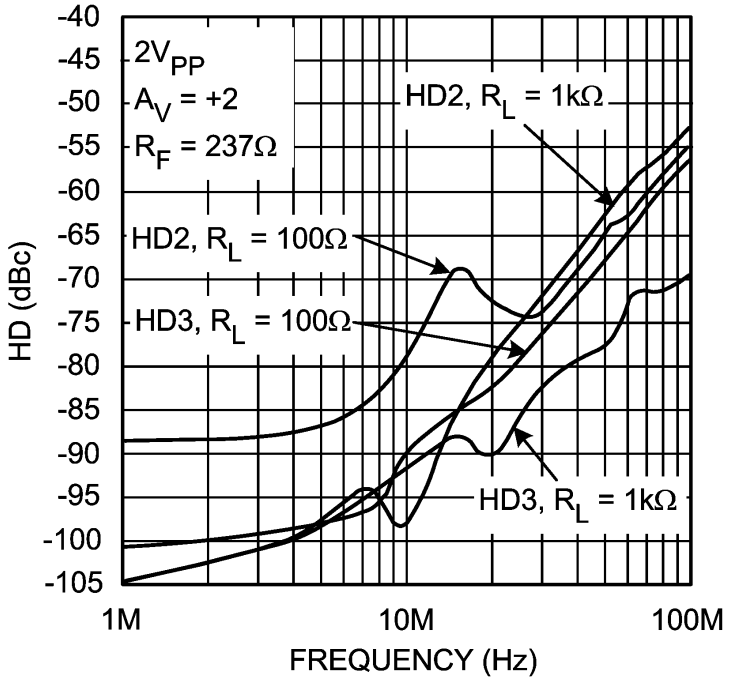

Figure 2-2: LMH6702's Harmonic Distortion vs Load and Frequency [3]

Chapter 3

Schematic Design

The bulk of the work done in this thesis project was designing this amplifier at the schematic level. This design involved simulating a number of individual stages and overall configurations in order to compare their performance and find where improvements could be made. This chapter steps through each section of the amplifier, describes some of the topologies that were tested, and presents the solutions that were used.

3.1 Process

In order to have a large gain bandwidth product, the transistors must have a fairly high f_T. Silicon Germanium (SiGe) bipolar transistors provide a large f_T and are more common and less expensive than alternatives such as Indium Phosphate (InP) and Gallium Arsenic (GaAs). Teradyne has previous experience with IBM's 5HP process so it was used for this chip. 5HP was chosen over faster SiGe processes because of its larger transistor breakdown voltages. Some parameters of the elements available in 5HP are covered in Chapter 4.

3.2 Feedback Style

One of the key factors in deciding how to design an amplifier is which style of feedback to use. There are three basic styles of feedback: no feedback, current feedback, and voltage feedback. Voltage feedback can be split into two categories, large and small open loop DC gain.

Feedback can significantly reduce the distortion from the open loop value [18]. This reduction is a function of the open loop gain divided by the closed loop gain. One important point is distortion is reduced as a function of the open and closed loop gains at the frequency of the distortion. For example the gains that matter for the third harmonic of a 100 MHz signal are the open and closed loop gains at 300 MHz.

Using no feedback allows an amplifier to have variable gain without switching out resistors. However, the signal chain strategy is to put a small amount of gain at the end to ease the distortion requirements on the rest of the chain. Since feedback significantly helps reduce distortion, it is worth pushing back the selectable gain stage to earlier in the chain and concentrating on reducing distortion in this final amp.

Current feedback has large open loop distortion and typically requires PNP devices as well as NPN. Its large open loop distortion comes from the gain's dependence on parameters of active devices, similar to voltage feedback that uses active loads. 5HP does not have any PNP devices, so PFETs could be used. These are much slower, however, and thus it is best to avoid them in the signal chain.

Voltage feedback is often used to reduce the distortion of low frequency or narrow band signals. It is usually designed to have a very large gain at DC, or in the narrow band of interest. For bands that go from DC to high frequencies, the open loop response needs to drop off fairly slowly so that the closed loop will be stable. Otherwise, a more complex compensation scheme must be used. This required drop off is approximately 20 dB/decade. After the first pole, there is approximately a constant gain bandwidth product which is what will determine the open loop gain at higher frequencies. In this design, distortion at high frequencies is of particular concern, so the gain bandwidth product and open loop distortion are much more

important than the DC gain. DC gain is typically achieved by using active loads and no emitter degeneration which are both major sources of non-linearity. The gain bandwidth product, however, is determined by stability and thus is just constrained by the locations of the other poles. Thus, to minimize high frequency distortion, the gain bandwidth product should be maximized and the DC gain should be sacrificed for low open loop distortion by using passive loads and emitter degeneration.

Hence, low gain voltage feedback was chosen as the best way to minimize distortion at high frequencies.

3.3 Overall Topology

There are many circuit techniques that can be used to minimize distortion, such as a number of feedforward techniques or using pre- or post-distortion; however, these are best suited for low frequency or narrow band signals as it is difficult to have them match over a wide range of frequencies. Thus, the amplifier is designed around maximizing the gain bandwidth product while minimizing the open loop distortion. A block diagram of the amplifier and surrounding parts can be seen in Figure 1-1 and the overall schematic of the chip is shown in Figure 3-1. Signals come in through the input resistors to the gain stage and then go to the output stage, which has a low output impedance and enough current to drive the load. The signal then feeds back through the feedback resistors to the input of the gain stage. There is another loop that matches the output common mode voltage to the reference provided by the analog to digital converter. An internal differential amplifier compares the common mode voltage to the reference and then injects some current into the gain stage to control the output common mode voltage. The common mode matching requirement for some high performance ADCs is around 1 mV which requires a much larger loop gain than what was put on the chip. An external integrator can be added to the loop to increase the gain and thus improve the accuracy. This setup is shown in Figure 3-2. This could all be done on chip. However, since this is an enabling technologies project, the primary concern was the main loop, and time was saved by not improving

the internal amplifier. A current source is used as a reference for the current mirrors in the rest of the blocks. The external output resistors can be added to tailor the bandwidth and response of the system. Since there is no filter between this amplifier and the ADC, it is desirable to remove high frequency noise by limiting the bandwidth with external resistors and the internal capacitance of the ADC. In addition, while the amplifier was designed to be stable when driving the ADC directly, adding in a small amount of external resistance can remove peaking from the frequency response.

3.4 Gain Stage

The gain stage is designed to have a large gain bandwidth product, low open loop distortion, reasonable DC gain, and reasonable noise. The gain stage must also control the main loop stability. Several gain stage topologies were tested for these characteristics. Normally, a number of DC and low frequency issues, such as bias currents and DC offsets, would be important in the gain stage, but, since the DC imperfections of this amplifier can be calibrated out in the test system, they were not a concern in this case.

3.4.1 Differential Pair

The simplest gain stage investigated is the differential pair, which can be seen in Figure 3-3. This design's advantage is its simplicity and is thus a good starting point, but it has significantly more distortion than all of the other gain stages tested. The reason for the poor linearity compared to the other stages is the lack of cascode. With just a differential pair, for small changes in base voltage, there is a large change in collector voltage. As the collector voltage changes, the size of the depletion region between it and the base changes and thus the size of the base changes. The size of the base determines β, and thus the gain changes with the input which is a source of distortion. This can also be seen from the equation for the collector current of a bipolar transistor, $I_C = I_S e^{\frac{V_{BE}}{V_{th}}}(1 + \frac{V_{CE}}{V_A})$, where the $\frac{V_{CE}}{V_A}$ term represents the nonlinearity from a changing collector voltage. This term is typically ignored due to the large size

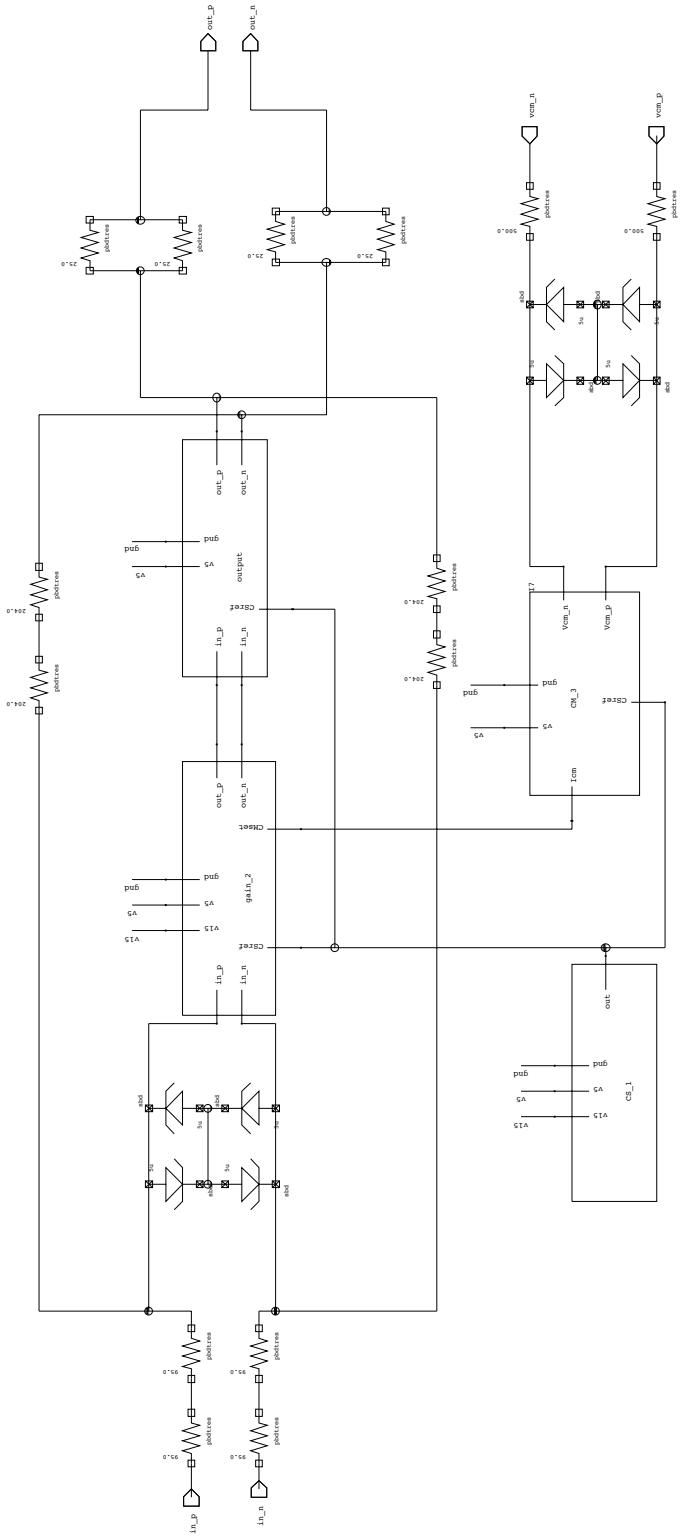

Figure 3-1: Amplifier Topology Schematic

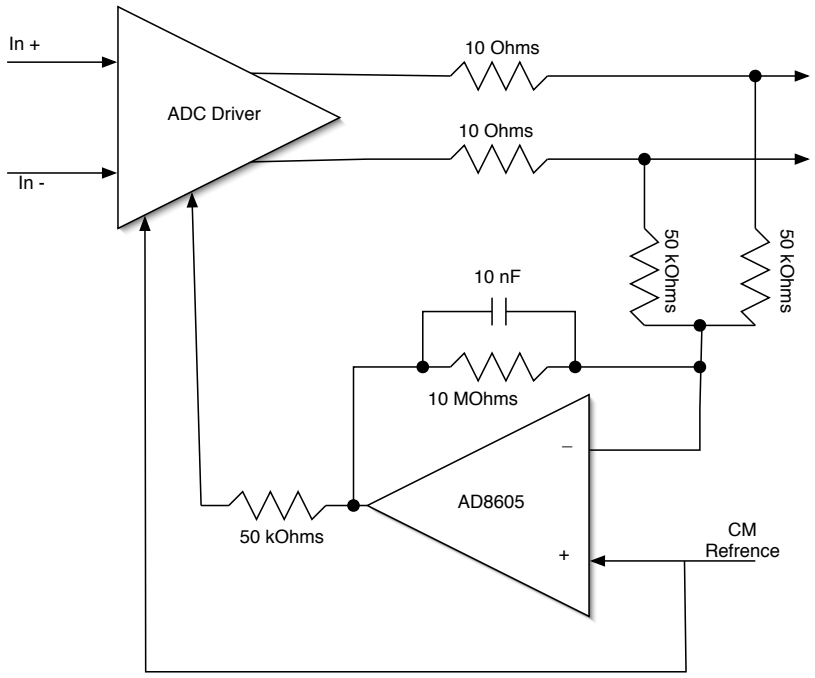

Figure 3-2: Board Level View

of the early voltage, V_A, but in this case simulation shows that it is significant.

3.4.2 Cross-Coupled

The most obvious source of nonlinearity in a differential pair is that the current is exponentially dependent upon V_{BE}. Thus, the cross-coupled [19] [20] and feedforward topologies are attractive, since they linearize this relationship. The cross-coupled circuit shown in Figure 3-4 is a translinear circuit that produces the input voltage across the emitter degeneration resistor. Thus, the collector currents are just the input voltage divided by this resistance which is a completely linear relationship.

The major disadvantages of this circuit are that it uses positive feedback and has negative input impedance. Negative input impedance means that the circuit is conditionally stable. The input impedance can be made positive by putting a small resistor and capacitor in parallel with the input to the gain stage. Putting a small resistor in parallel with a large negative resistance results in an equivalent resistance

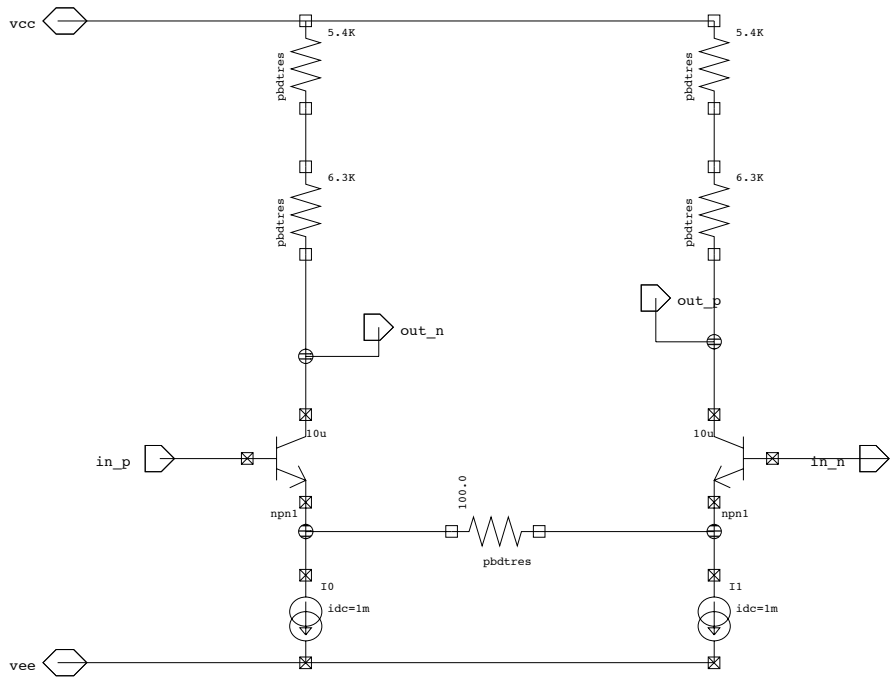

Figure 3-3: Differential Pair

approximately equal to the resistance of the small resistor. Since the magnitude of the input impedance of the gain stage decreases with frequency, the capacitor must be added in parallel with the small resistor in order to keep the combination's impedance much smaller than the input impedance. The disadvantage of this technique is that it reduces the input impedance of the stage and introduces some stability concerns.

As will be discussed in Section 3.4.5, emitter degeneration can improve linearity nearly as well on its own as the cross-coupled configuration can and does not have the stability concerns or the loss of head room due to adding a pair of transistors under the input transistors.

3.4.3 Feedforward

Feedforward [21] [22] [23], like the cross-coupled configuration, is a method for linearizing the relationship between I_C and V_{BE}. An example of a feedforward gain stage is shown in Figure 3-5. In this case an additional pair of transistors takes the

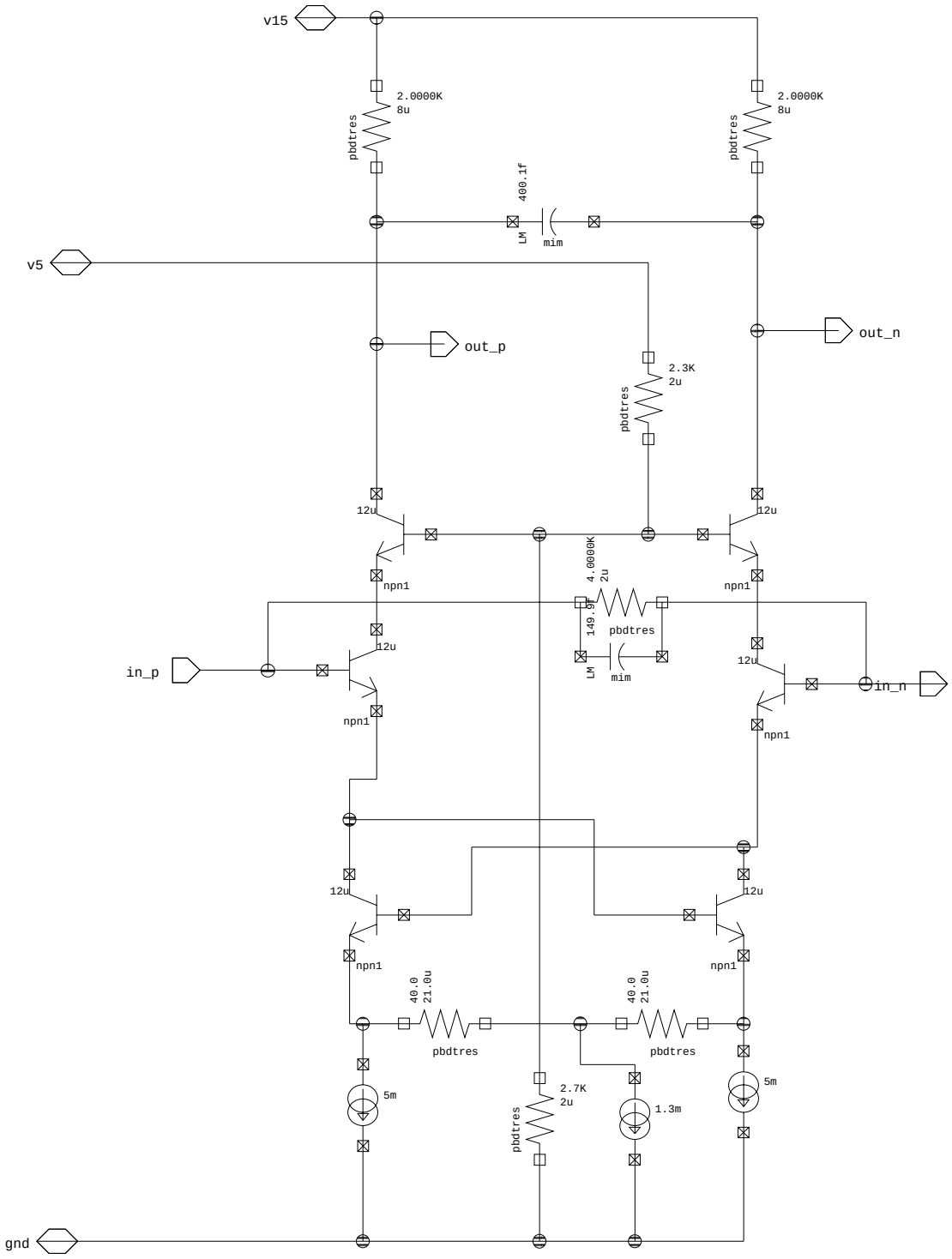

Figure 3-4: Cross-Coupled

emitters of the cascode transistors as inputs and adjusts the current through the load accordingly. Since the bases of the cascode transistors are fixed and the transistors are matched to the input transistors, the movement of their emitter voltages represents the changes in V_{BE} across the input transistors. This difference is the input to the inner differential pair. Unlike in the cross-coupled case, this will have a second order error due to the nonlinear gain of the inner pair. This distortion will be very small since it deals with small inputs. Also, unlike the cross-coupled stage, feedforward has positive input impedance.

The major disadvantage of this method is that it requires additional current for the inner pair of transistors. Feedforward provides minimal advantages in linearity over just a cascode with emitter degeneration. The advantage in this stage lies in linearizing with no or minimal emitter degeneration allowing for large DC gain which is not particularly important in this application. In fact, for a given power dissipation, the cascode can actually out-perform the feedforward setup, since the feedforward setup wastes power in the error correction legs.

3.4.4 Cherry Hooper

The Cherry Hooper [24] configuration is known for its high gain bandwidth product. The configuration that was simulated can be seen in Figure 3-6. The Cherry Hooper amplifier uses local feedback to increase its bandwidth; however, for this amplifier, overall feedback is desired to help improve the linearity of the output stage as well as the gain stage. In order to stabilize the overall feedback, the gain stage is slowed down which contradicts the Cherry Hooper's use of local feedback to increase bandwidth. Thus, the Cherry Hooper configuration is not appropriate for the gain stage of this amplifier.

3.4.5 Cascode

As discussed in the differential pair section, adding a cascode can significantly improve linearity by removing the large swings from the collectors of the input transistors. In

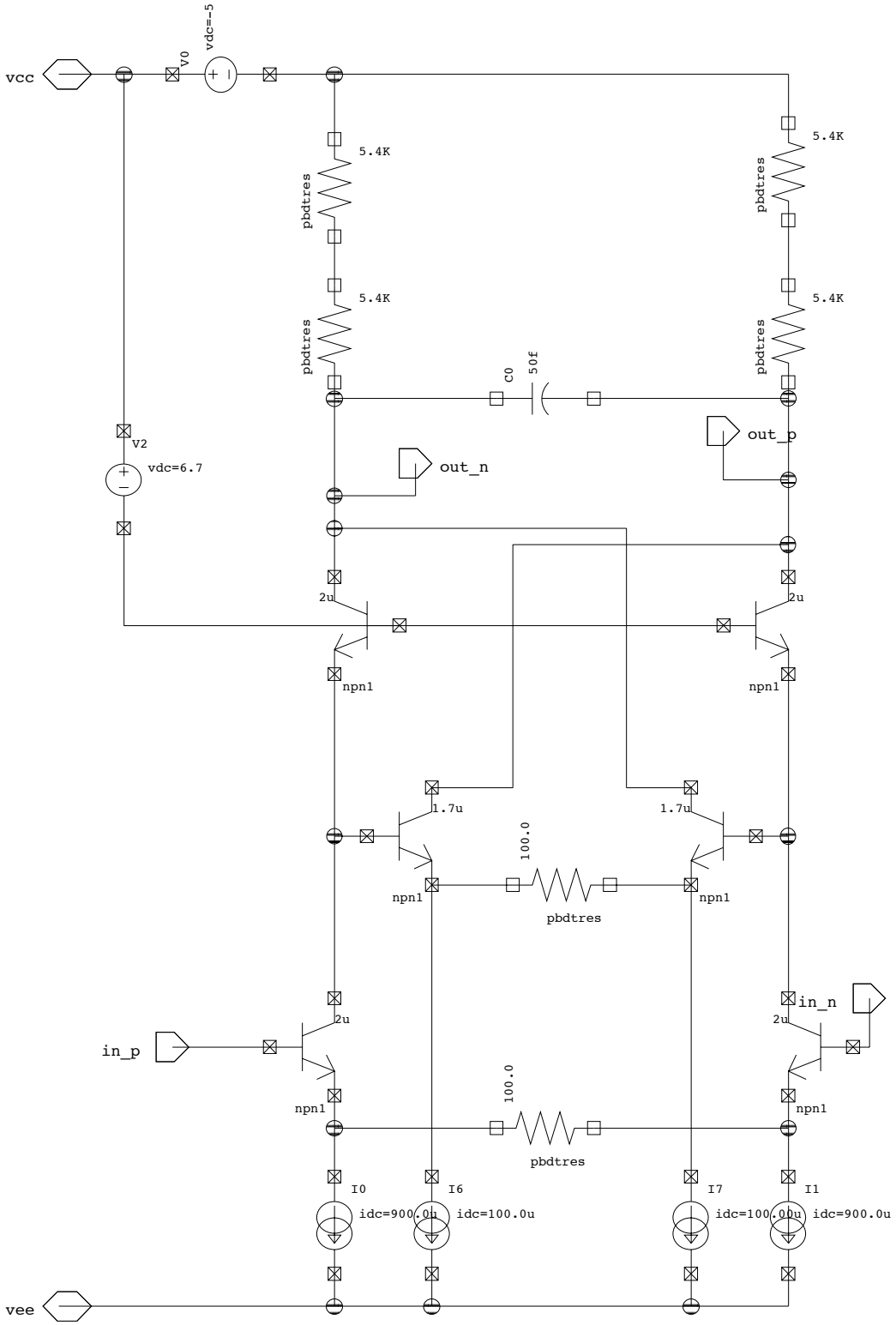

Figure 3-5: Feedforward

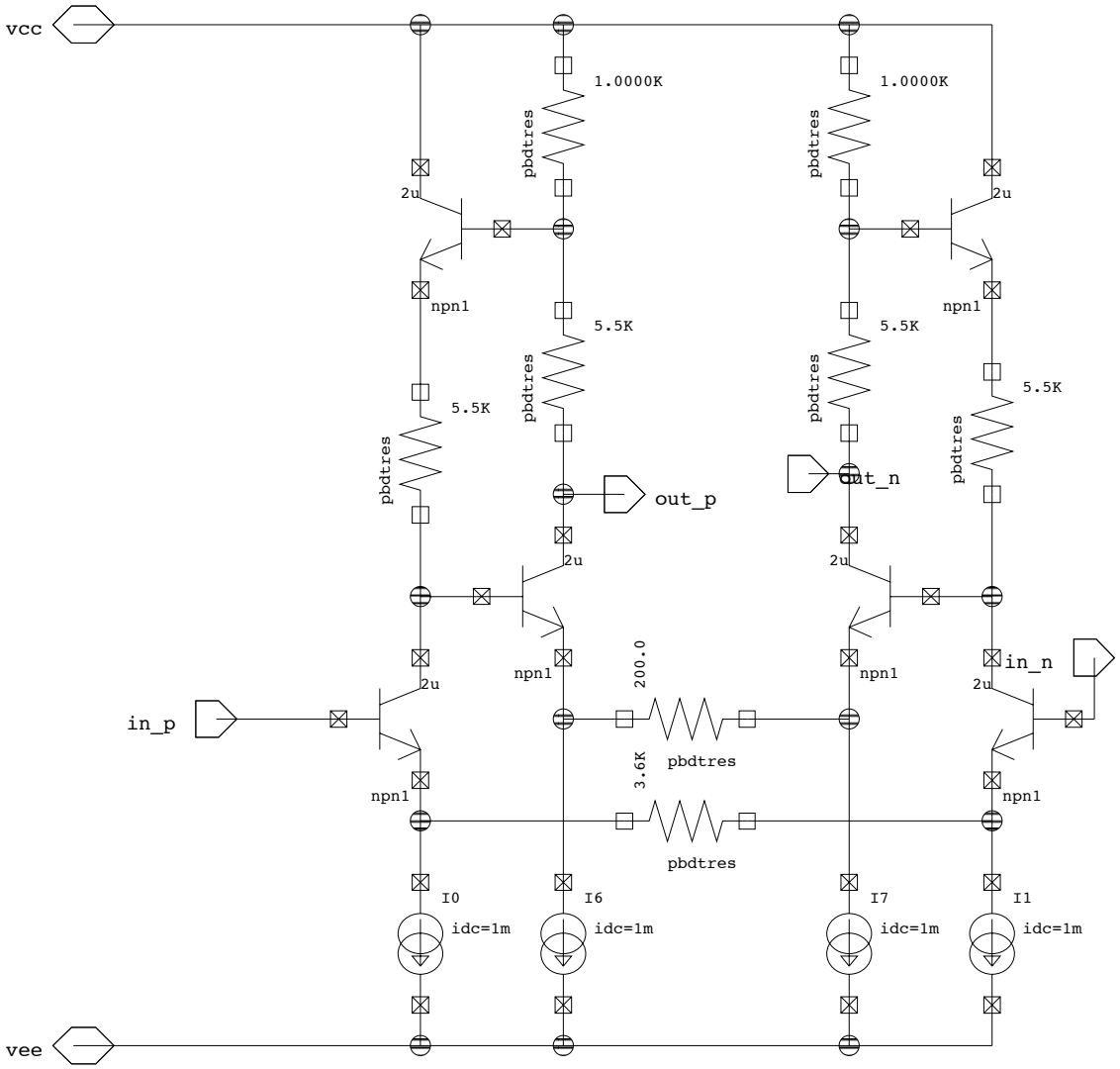

Figure 3-6: Cherry Hooper

addition, using a reasonable amount of emitter degeneration, in this case a total of 70 Ω, makes the cascode have similar linearity as the feedforward and cross-coupled topologies. The gain stage used in this amplifier is a cascode and is shown in Figure 3-7.

The stability of the amplifier is controlled by the capacitor between the loads. This point was chosen for compensation, because it is the highest impedance point in the signal path of the amplifier. In addition, the capacitor is across two differential points, so even if the value of the capacitor varies, it will still be symmetric. If instead the capacitors were placed from the inputs to these points, then mismatches in capacitor values would cause mismatches between the two sides. Also, with the capacitor across the load, it is fairly small, and thus taking advantage of the Miller effect is not particularly important. The above statement about symmetry is not completely true, because the capacitor will have one side closer to the substrate and thus a greater parasitic capacitance to ground. To counter this effect, there are two capacitors with top and bottom attached to the opposite signals. The actual capacitor value was chosen by experimenting with the resulting phase margin. The dominant pole ended up at about 75 MHz. The next pole is from the nodes at the bases of the input transistors. These transistors have $c_\pi \approx 620$ fF and the impedance at that point is approximately 130 Ω. This creates a pole around 2 GHz. There is a direct trade off between noise and gain bandwidth product, since if the transistors were smaller, the dominant pole could be put at a higher frequency. However, larger transistors have smaller base resistance which can be a major factor in the noise.

The common mode adjustment current is injected in the middle of the emitter degeneration resistor. This current feeds directly into the current mirrors and thus reduces the current going into the load resistors. Adjusting the current through the load resistors equally moves the common mode output voltage.

Using two current mirrors rather than one at the center allows for greater head room, since there is no DC voltage drop across the emitter resistors. The current mirrors do not exactly match the 5 mA current source; this was done to tailor the common mode output voltage. While ADCs' reference voltages are typically specified

to a small range, it would be nice to make the amplifier able to accommodate a larger output common mode range. Additionally, there should not be any set of variation of parameters for which the minimum common mode voltage is greater than the reference. A small amount more current was run through the gain stage to extend the bottom of the output common mode range.

The DC gain does not need to be as large as it is in typical voltage feedback amplifiers, but if it is too small, low frequency linearity will not meet the specifications. The gain is approximately $\frac{R_L}{R_E+\frac{1}{g_m}}$ where R_L is the load resistor, R_E is the emitter degeneration resistor and $g_m = \frac{I_C}{V_{th}}$. Linearity is improved by making $R_E > \frac{1}{g_m}$. To maintain constant linearity, $g_m R_E = \frac{R_E I_C}{V_{th}}$ should be held constant. Assuming $R_E I_C >> V_{th}$, the gain is approximately $\frac{R_L}{R_E}$. For a given linearity, $V_{RE} = R_E I_C$ is constant and gain $= \frac{R_L I_C}{V_{RE}}$. $R_L I_C$ is the voltage across the load resistors. Thus, the only way to increase the gain while maintaining linearity is to increase the voltage across the load, which can be done by increasing the power supply voltage. Luckily, in this application, a number of power supply voltages, including +15, are available.

Noise is not as strict of a specification as linearity for this amplifier, but it still needs to be taken into account during design. The major noise sources are the input resistors, feedback resistors and the gain stage. The input resistors are set by the system requirement of 400 Ω differential input impedance. The feedback resistors are determined by choosing a closed loop gain of two. Since these resistors are set, the only place to minimize noise is in the gain stage. The output stage and output resistors are not major noise sources since they are after the gain, and thus their input referred noise is divided by the open loop gain.

The three types of noise of concern are Johnson noise, Shot noise, and Flicker noise. Johnson noise comes from thermal effects in resistors, and its formula is $V_n^2 = 4kTR\Delta f$ where k is Boltzmann's Constant, T is the temperature in Kelvin, R is the resistance and Δf is the width of the band of interest. Shot noise comes from the discrete movement of electrons across potential barriers and thus occurs in transistors. Its formula is $I_n^2 = 2qI\Delta f$ where q is the charge of an electron, I is the current and Δf is the width of the band of interest. Flicker noise is also referred to as 1/f noise

and comes from contamination and defects in crystal. The name 1/f noise is used because it is proportional to the reciprocal of the frequency. All three of these noise sources contribute to the input referred noise, but Flicker noise is only important at low frequencies. In order to meet the noise specification, Flicker noise just needs to be small before 1 MHz, since that is the first frequency for which the noise is specified. Luckily, the Flicker noise corner come out low enough without any effort to optimize it.

The major sources of Johnson noise in the gain stage are the emitter degeneration resistors and the real resistance in the base of the input transistors. The base resistance can be minimized by increasing the size of the input transistors, and so maximum size transistors were chosen for the input transistors. The size of the cascode transistors is not particularly important, so they were chosen to match the size of the input transistors. The load resistors are not a major source of noise, since their noise comes after the gain. The major sources of Shot noise are the input transistors.

The minimum input referred noise is achieved when the noise impedance equals the source impedance [25] [21], where the noise impedance is the input referred noise voltage divided by the input referred noise current. Creating this noise impedance match typically does not correspond to a power match between the source and the amplifier. In this case the input impedance of the amplifier is dictated by the overall system requirements, which is detrimental to the noise performance of this amplifier. Additionally, for this amplifier low distortion is more important than low noise, and maintaining low distortion places additional restrictions on the noise performance. Thus, the amplifier should be designed to come as close as possible to meeting the noise impedance match given the input impedance and low distortion constraints. Given the condition for optimum noise performance and factors contributing to the noise, the simulator can be used to perform the actual optimization.

As discussed above, in order to maintain linearity, $I_C R_E$ must be held constant. To minimize Shot noise, I_C should be decreased, but to minimize Johnson noise, R_E should be decreased. In order to find the minimum noise for a constant $I_C R_E$, the bias current was swept with R_E and R_L changing appropriately to maintain linearity

and gain. A minimum was found near $I_C = 5\ mA$. The values were optimized by repeating this process and tweaking R_E and R_L for linearity and gain.

The bases of the cascode need to be biased. It is possible to do this using transistors; however, a resistor voltage divider is simple and provides sufficiently stiff biasing. This biasing is taken from the 5 V supply to minimize the power dissipated by these resistors. The base voltage is chosen to make sure that the cascode and input transistors' V_{CE} stay above saturation and below their break down voltage.

3.5 Output Stage

There are a number of ways to make an output stage. The two main styles using only NPN transistors are emitter followers and open collectors. In this case, because the load is the ADC input, an open collector configuration would also need resistors to the positive supply. Putting in resistors and then driving the load is equivalent to making a gain stage with very low gain. This type of output stage was investigated, but the emitter follower proved to be a better output stage. To keep the output impedance of an open collector low, the load resistors would have to be small. Therefore, keeping the stage from being an attenuator requires fairly small emitter degeneration and thus poor linearity. The open collector would make sense if the output had to match a transmission line, but since the amplifier is close enough to the ADC, this is unnecessary. In addition, putting some gain in the output stage was considered, which might help linearity, but it would significantly hurt the noise performance and the stability. Hence, an emitter follower was chosen.

A typical ADC along with estimated board parasitics present a differential load of a reasonably large resistance in parallel with a capacitance around 6 pF. A 6 pF capacitance at 500 MHz has an impedance of 53 Ω and requires a peak current of 18.8 mA to drive 2 V_{pp} differential. Thus, the output stage must have an output impedance small enough to drive the 6 pF capacitance at high frequencies and enough current to drive 18.8 mA without adding significant distortion.

The amount of current in the output stage turned out to be one of the major

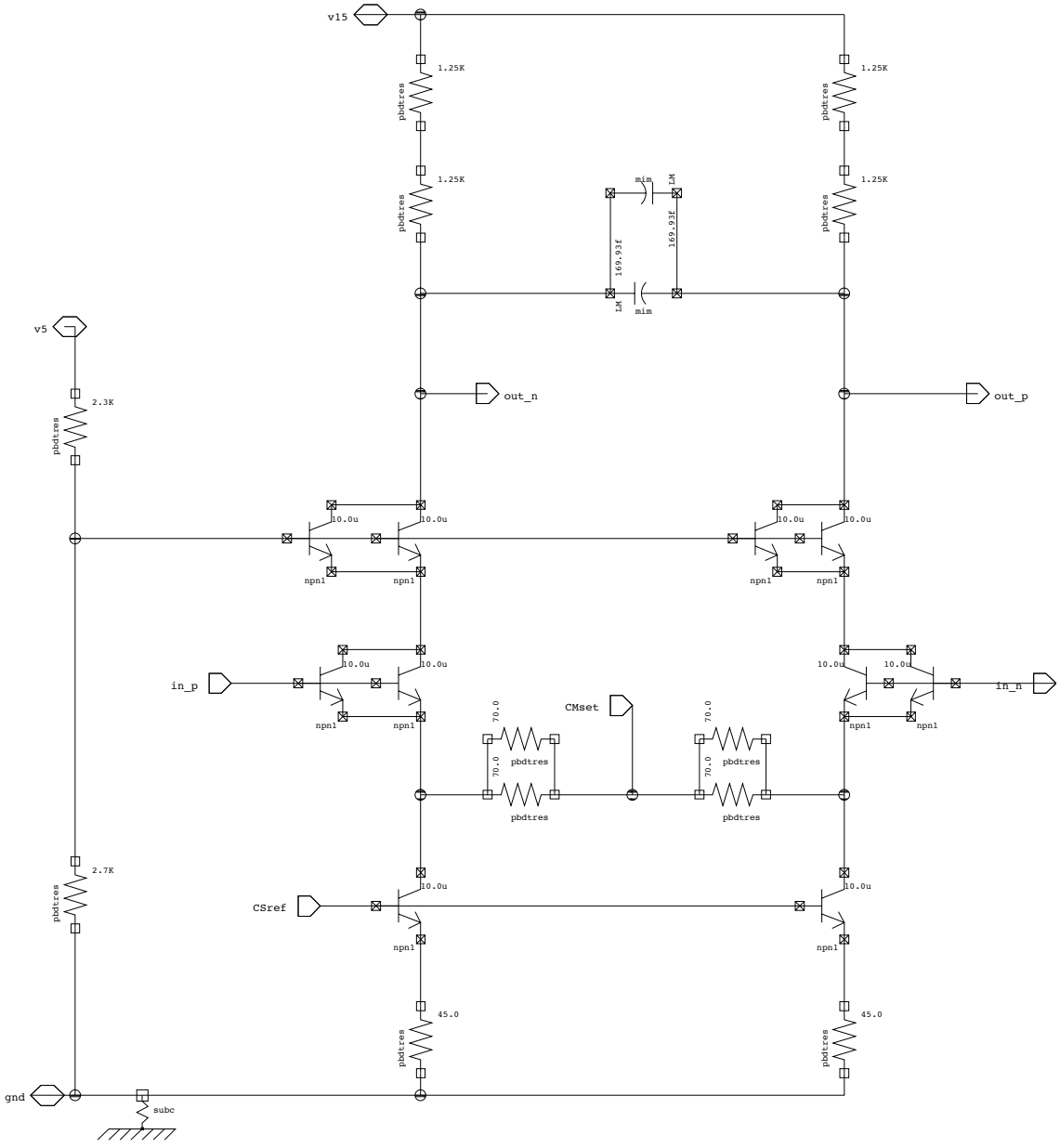

Figure 3-7: Gain Stage

factors in linearity. A Class A output stage is more linear than any other style, but Class A requires the bias current to be greater than the peak required current. In addition, to avoid large changes in V_{BE} which would cause distortion, each side of the output stage was biased with 40 mA so that the deviation in current would be less than half the bias. This consumes a total of 400 mW, which by itself is greater than the total power dissipated by similar amplifiers that are commercially available.

The transistor size required to drive this much current leads to a large capacitance at its input. In addition, due to the large I_C, there is a large bias current. Both of these factors would make connecting the gain stage directly to the output stage very detrimental to performance, especially since some of the capacitance is non-linear. Thus, a buffer is required between the gain stage and the output emitter follower. An obvious choice for this middle stage is a smaller emitter follower, since this stage will present less capacitance and bias current to the gain stage. A small emitter follower will be able to provide the necessary current to the output emitter follower with a fairly small output impedance. The input impedance of this buffer is its r_π plus β times the parallel combination of the input impedance of the next emitter follower stage and the output impedance of the current mirror. The output impedance of the current mirror is $r_\pi||R_E + (1 + g_m(r_\pi||R_E))r_o$. Since $R_E > r_\pi$ and $g_m R_E > 1$ this is approximately $R_E(1 + \frac{V_A}{V_{th}})$. The output impedance of the current mirror is approximately proportional to its emitter degeneration. The emitter degeneration is inversely proportional to the current, so as the current in the first emitter follower stage is decreased, the output impedance of its current mirror increases. This is the dominant factor in the input impedance of the emitter follower, so the key to providing a large input impedance to the gain stage is decreasing the current in the buffer. The benefits of making the buffer small are confirmed in simulation as the low frequency third harmonic is improved by decreasing the size of this stage. This linearity improvement was surprising since the input impedance of this stage is much larger than the output impedance of the gain stage. However, the low frequency distortion is -93 dBc so even small effects can have an impact.

If two emitter followers are better than one, it would seem logical to add yet

another in order to make the load of the gain stage a very large impedance. However, an emitter follower with a resistive source has an output impedance that acts inductive over a certain frequency range [21]. If the emitter follower is driving a capacitor, then the inductance and capacitor can ring and cause the circuit to become unstable. Adding additional emitter followers makes this effect even stronger. In this case, two emitter followers are stable, but adding a third causes the amplifier to oscillate. Even when there are only two emitter followers, with a small amount of inductance in the power supplies to model package parasitics, the output stage oscillated. The resistor and capacitor from +5 to ground at high frequencies provide a low impedance path for the ringing on the power supply to ground. An additional step taken to prevent oscillation and ringing is putting small resistors between the collectors and +5. The resistors are used to damp the LC circuit formed by the capacitance at the collectors and the inductance from the package parasitics. The collectors of the followers from each side are connected as close to the collectors as possible so that the current through the wiring and resistors is constant. Thus, even with resistors in the collectors, the collector voltages are constant. Connecting the differential sides as closely as possible also helps reduce ringing, because the AC currents cancel leaving only a DC component. Even with all of these steps taken, some resistance at the output outside of the feedback loop is required to avoid significant ringing. A 12.5 Ω resistor on each side is placed on chip, so that if the amplifier is connected directly to the ADC, it will not oscillate and have reasonable ringing. However, to completely flatten the frequency response, another 10 Ω on each side is required off chip. With this full setup, even taking into account package parasitics, the frequency response has not peaking.

There are other issues associated with having such large currents move through the output stage. The first is that four transistors are supposed to act in parallel as one large transistor. This works well until thermal effects are taken into account. If the current in one transistor happens to get bigger than in the others, that transistor will get slightly hotter. As the temperature increases, if V_{BE} is forced to be the same as the others, it will conduct even more current. This positive feedback effect causes

run away and would cause one transistor to carry all of the current and eventually burn up. This is corrected by putting a small resistor between each emitter and the transistors connections. This creates a negative feedback effect. If one transistor starts to conduct more than the others, its temperature will still increase, but its V_{BE} will be decreased by the additional voltage drop across the emitter resistor. Even with very small resistors, the change in V_{BE} overcomes the thermal effect and stops run away.

Another thermal effect is if one side is conducting more than the other side, the higher conducting side will get hotter. As one side heats up and the other cools, the V_{BE} of the hot side will decrease, and the V_{BE} of the cool side will increase. This will change the differential signal. This effect is particularly important when looking at slow square waves where the output will settle to some value and then, due to thermal effects, will slowly decrease. Luckily, in a feedback configuration, the feedback mechanism will correct for this kind of change in the output. The correction will not be perfect, and thus this will be a source of distortion. However, thermal effects are rather slow, and thus this would only be a source of low frequency distortion. For a fast signal the current will change must faster than the thermal time constants, and thus the temperature of the transistors will remain fairly constant. Cross-quading the transistors in layout is one technique for reducing this effect and was done to improve matching. However, further techniques were not used because the low frequency linearity specification was easier to meet than the high frequency linearity specification.

The selection of a 5 V supply for this stage came from the trade off of minimizing the power dissipated and having enough head room. Since the output stage uses such a large amount of current, the power dissipation is significantly decreased by decreasing the power supply voltage it uses. At the same time, with the output centered at up to 1.6 V, it can go up to 2.1 V. Therefore, the first emitter follower stage has its emitter at about 2.9 V, since $V_{BE} \approx 800$ mV. A 3.3 V power supply would leave a maximum V_{CE} of 400 mV under this condition, and V_{CE} would be even less when accounting for the drop across the collector resistors which would put the

transistors in saturation. In order to avoid this, the next highest standard power supply value was used.

3.6 Common Mode Control

Many ADCs provide a reference voltage which must be matched by the input common mode to within about 1 mV or else the linearity degrades. If the reference is around 1.55 V, the 1 mV requirement says that the loop needs 1 mV in 1.55 V precision. A loop with that precision requires an open loop gain $\geq$ 1550 which is 63.8 dB. The common mode voltage is detected by putting two large resistors between the outputs and getting the common mode voltage from the point between them. Larger resistors will have less of an effect on the differential signal. Thus, 50 kΩ each seemed appropriate to avoid impacting the differential signal. A bias current through these resistors of 20 nA would cause a 1 mV error. Thus, the bias current through these resistors must be much less than 20 nA. A simple cascoded differential amplifier was implemented on chip which drives the gate of a PFET. The source of the PFET is attached through diodes to the center of the emitter degeneration in the gain stage. The current injected by the PFET reduces the current through the load resistors in the gain stage and the output common mode voltage.

3.6.1 Internal Common Mode Amplifier

The simple on chip amplifier has a gain of approximately 30 dB which is far less than the required 63.8 dB. Also, the bias current of the on chip amplifier is approximately 2 μA which is far too large. Thus, if 1 mV accuracy is desired, an off chip integrator with a large gain and small bias current must be added. This configuration can be seen in Figure 3-2. The internal amplifier is compensated so that it will be stable on its own or with the integrator added to the loop. Making the loop stable with the integrator should have been trivial since the integrator's dominant pole is at a very low frequency. However, if an output resistance and finite gain are added to the ideal operational amplifier model, then it turns out that there is a high frequency

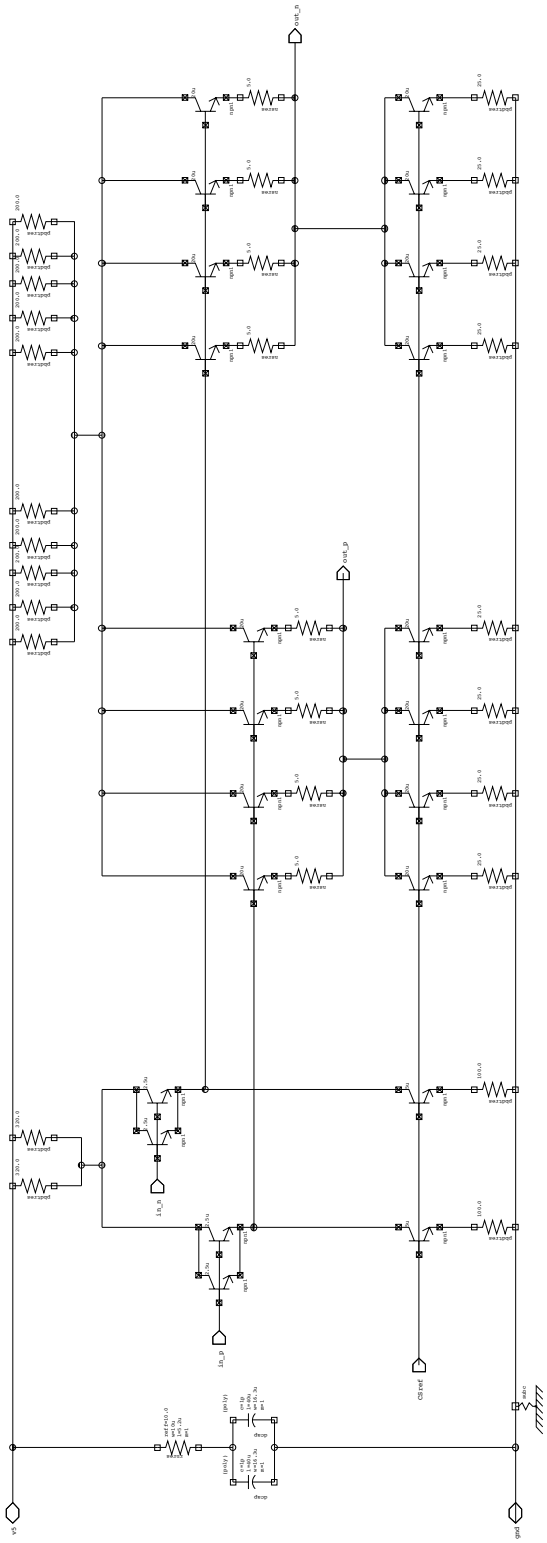

Figure 3-8: Output Stage

right half plane zero in addition to the low frequency pole. This is typically not an issue. However, between the high gain of the integrator and the gain of the internal amplifier, the loop gain would get just under one and then level out because of the zero. Concurrently, the phase would quickly reach -180^o, since the zero is in the right half plane, leading to a very small gain margin. A Bode plot of this situation is shown in Figure 3-9. This problem was fixed by making the pole of the internal amplifier occur at a much lower frequency than it would have been otherwise.

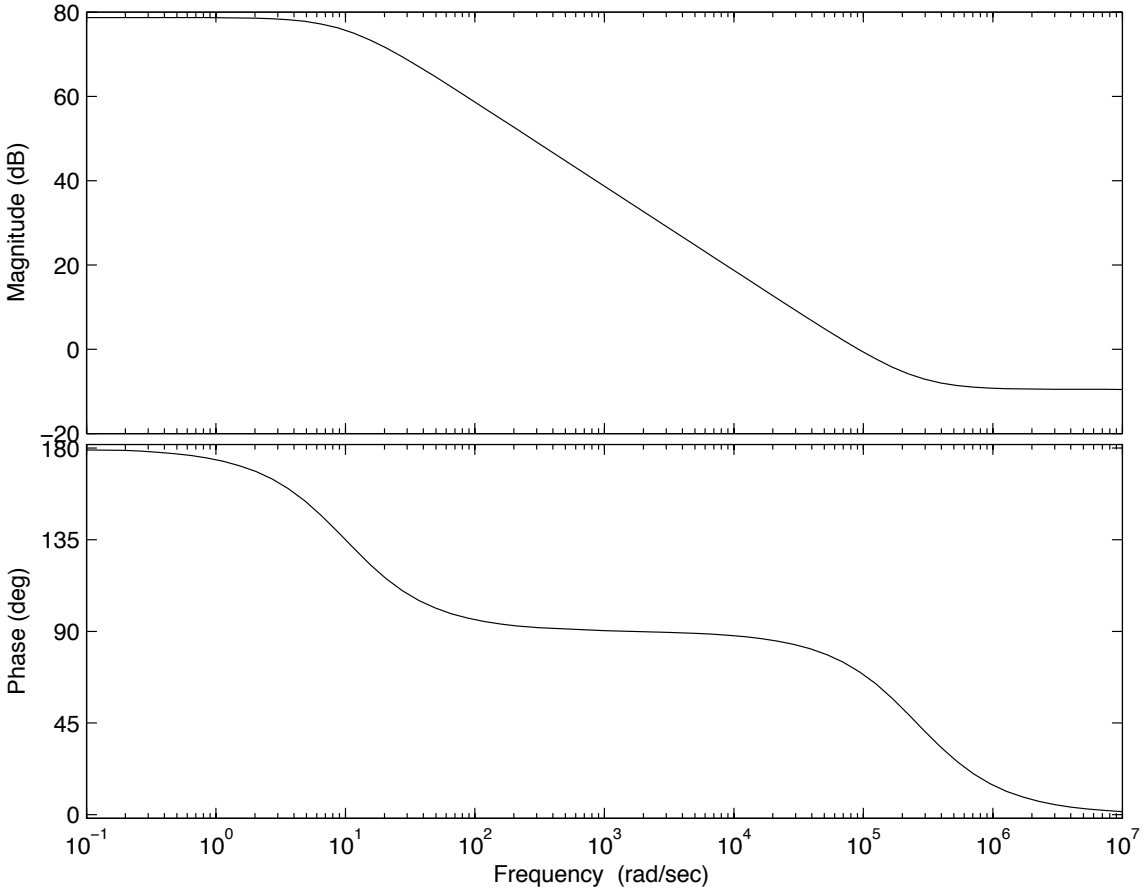

Figure 3-9: Bode Plot of a Pole Followed by a Right Half Plane Zero

There are several differences between this amplifier and the one in the signal path due to the different requirements. The linearity of this amplifier is unimportant, but the DC gain is vital. Thus, there is no emitter degeneration which improves the DC gain. The tail current of this amplifier is 200 μA. In addition to keeping the power

dissipation low, the small current allows for a small input bias current. This amplifier is also cascoded, although not for linearity or speed, but to protect the PFET. V_{SG} of a PFET can only get so large before the PFET will be permanently damaged. The cascode is added to avoid any case where V_{SG} could exceed its limit. Before the gate voltage would get too low, the cascode would saturate. Initially, this amplifier was compensated in the same way as the gain stage, but a power supply rejection issue was discovered. Since the source of the PFET is connected to +5, but the gate is not, signals on +5 change V_{GS} and thus cause the common mode to change. In order to solve this problem, the compensation was changed to the current configuration, in which a large resistor in series with a large capacitor, connected across the gate and source of the PFET, create a pole. The capacitor couples the gate and source, so high frequency signals on +5 go to both the gate and source and thus do not change the current through the PFET. The capacitor was limited in size, and the small resistor between it and +5 was added to avoid ringing caused by having a large capacitor connected to the inductance of the package. A large series resistor was required due to the limit on the capacitor size and low frequency of the pole.

3.6.2 External Integrator

The external integrator requires an op amp with large open loop gain and very low input bias currents. The one odd feature of the integrator is the large resistor between it and the internal amplifier. This resistor only hurts the accuracy of the loop by a small amount since this error occurs after the main source of gain. The resistor improves the stability of the loop. If output resistance is included in the model of the op amp, the output impedance of the integrator is equivalent to a small resistor in parallel with a very large capacitance. In fact, for this case with $R_i = 25$ kΩ, $C = 10\ nF$, $R_o = 30\ \Omega$, $R_F = 10$ MΩ and open loop gain = 300,000, the equivalent circuit for the output impedance is a 40 mΩ resistor in parallel with a 2.5 F capacitor. That is why such a large resistor is required to isolate the capacitance from the inductance of the package.

The amplifier selected for this integrator is the AD8605 [26]. It has a maximum

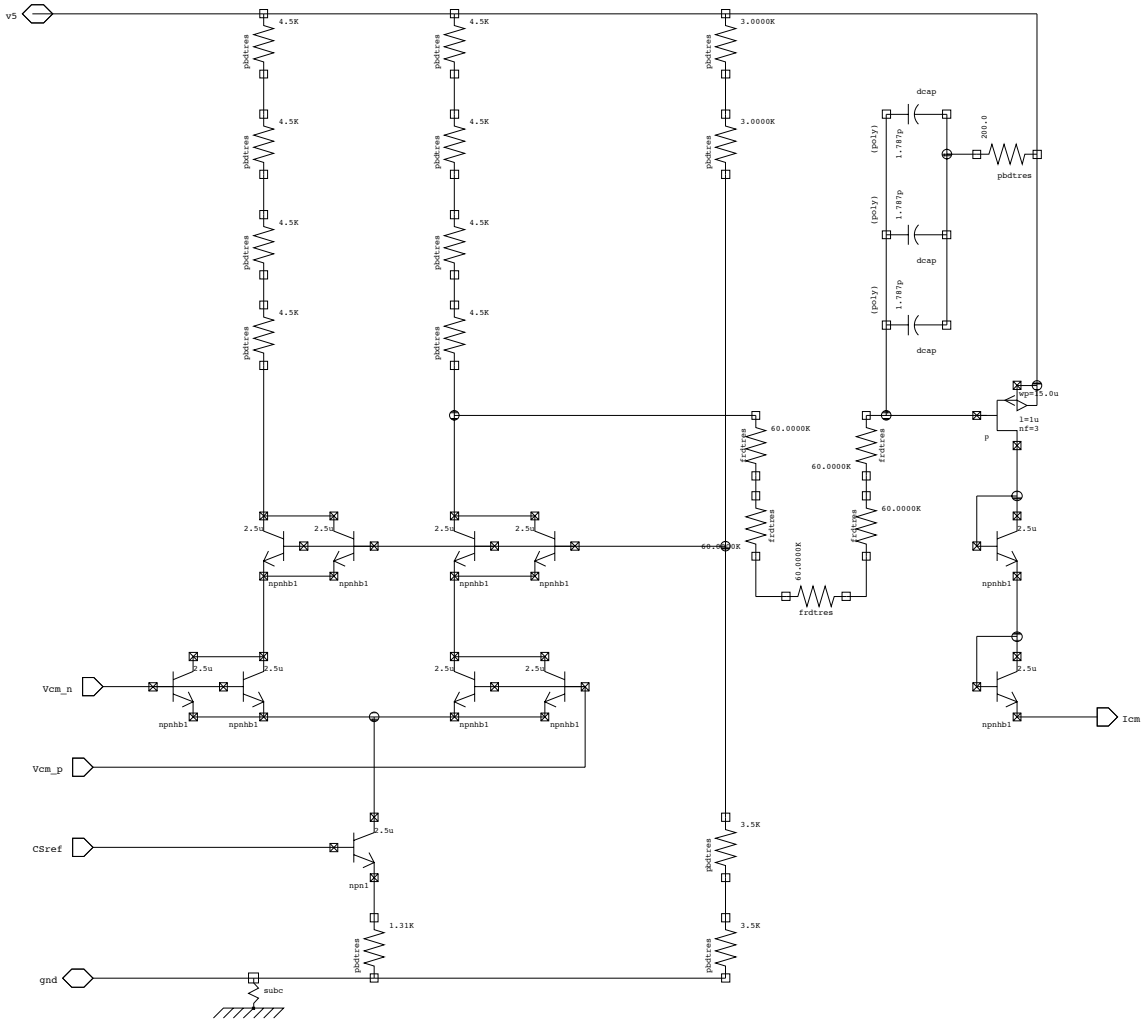

Figure 3-10: Common Mode Control

offset voltage of 300 μV, and a maximum input bias current of 50 pA, both of which are well within the requirements for the integrator. The minimum open loop gain is 110 dB which is well above the closed loop DC gain of 52 dB. The power supplies are +5 and ground and have a worst case output range of 0.04 V to 4.96 V. The supply voltage and output range are part of the reason this amplifier was selected. The range of inputs of the internal common mode amplifier is ground to 5 V, so the external integrator's output should span the whole range but never exceed it.

3.7 Current Reference

The current reference schematic is shown in Figure 3-11. It is a fairly simple current reference, but because of the use of active loads in the gain stage, it actually helps improve the power supply rejection ratio (PSRR). If there is a low frequency signal in the +15 supply, it will alter the current. The current source uses the same resistors as the gain stage loads, so the changes cancel out. The change of current will have some effect on the small signal parameters of the gain stage transistors. The stage was designed so that the gain is very well approximated as $\frac{R_L}{R_E}$, so it will have little effect on the gain. In the output stage, having the currents change is not very detrimental as long as they are still well above the peak output current. Changes in current will affect the common mode amplifier. Luckily, this is not very important, since it comes after the large gain of the integrator.

The helper transistor is needed to provide the current to the bases of the current mirror transistors. Since the current mirrors and source supply a total of approximately 120 mA, and β can go as low as 50, the bases can require up to 2.4 mA. The helper transistor is connected to +5 since the voltage at its collector is not important. This also saves power. The resistor and diode above it are used to ensure that the V_{CE} does not exceed the breakdown voltage. The 1.15 kΩ resistor is used to ensure that there is always at least a small amount of current through the helper transistor, so that its V_{BE} will not vary significantly.

Simple current mirrors with emitter degeneration were chosen over fancier mirrors

to avoid using up too much head room, especially in the gain stage. The emitter degeneration linearizes errors in the base voltage and improves the output impedance. The linearization is very helpful, because it reduces the error due to voltage drops in the wiring between the reference and the mirrors. If these resistors were not included, a drop of 18 mV across a long wire would cause the current mirror to have half the expected current. In this case, the current error would just be 18 mV divided by the emitter degeneration resistor. The size of the emitter resistors were chosen so that the voltage across them is $10V_{th}$.

The variation in current due to temperature could be significant. In a production chip, a bandgap reference would probably be used to eliminate the temperature dependence.

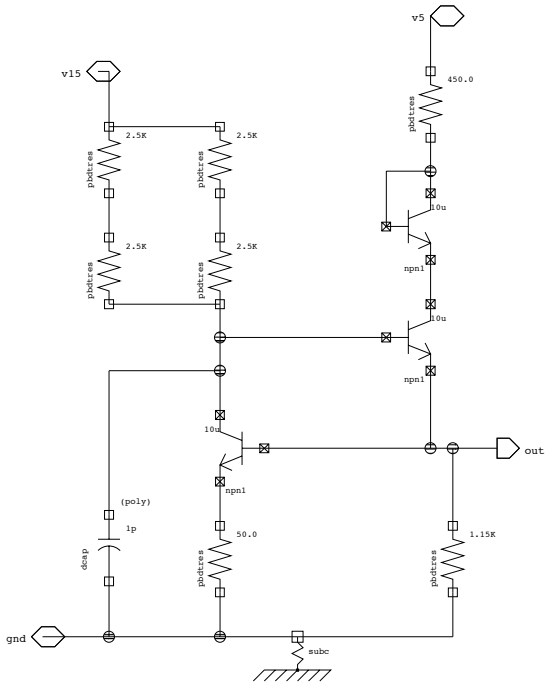

Figure 3-11: Current Reference

3.8 Over Voltage Protection

There are two events that the circuit needs to be protected against: electrostatic discharge (ESD) and improper signal voltages.

Every pin must be protected against a 2 kV human body model ESD event. The main strategy is to provide a low impedance path to ground. The +5 supply has a reverse biased diode to ground so that if the ESD event forces it below ground, the current will flow through the diode to ground. To deal with a large voltage being supplied to +5, there is a clamp, as seen in Figure 3-12, that collapses to provide a low impedance path to ground when the voltage gets too high.

On each signal pin, there is one diode to +5 and one to ground. If the signal goes a diode drop below ground, it is shorted to ground. If it goes well above +5 then it will be shorted to +5, and the clamp will collapse and short it to ground. For the temperature sensor pin, there is a diode to ground and a diode to the top of its own clamp. The temperature sensor gets its own clamp so that it can be used without the power supplies being connected.

The +15 supply pin was a challenge, since clamps are designed to collapse around 5.6 V. While clamps have been extended to around 11 V by stacking them, it seemed unlikely that it could be extended any further. The solution suggested by IBM is a reverse biased diode between +15 and ground. If +15 goes a diode drop below ground, the diode will act as a short circuit to ground. If +15 goes above the reverse break-down voltage of the diode, it will provide a low impedance path to ground. However, it will provide a low impedance path to ground with more than 15 volts across it, so the power dissipation will be much larger than any of the other ESD solutions on this chip. IBM's suggestion for dealing with this large power dissipation is to use a large ns diode. A ns diode is the n sub-collector implant in the p substrate. This is superior to a PIN diode, which is used for all other ESD protection diodes, because the substrate is part of the diode. This allows heat to easily flow away from it. The thermal resistance of a PIN diode is much larger, because it is a p implant in a n sub-collector that is surrounded by a deep trench. Therefore, heat in a PIN diode

has to flow from the n sub-collector through the deep trench to the substrate. The reverse breakdown voltage of the ns diode is unknown, but IBM is confident that it will meet the needs of this application.

If the input signals are pulled too high or too low together, then the ESD diodes and clamps will short the inputs to ground and protect the circuits. However, if they are pulled apart, because of the maximum V_{BE}, they can do damage before triggering the ESD protection. That is why there are Schottky diodes between the inputs. There are two in a row in each direction so that the inputs can only be pulled apart by two diodes drops, 610 mV, in either direction. The center points are connected together to make layout easier. The input to the common mode amplifier is protected in the same way. The amplifier inputs have resistors in series with them, so if a signal that turns on the Schottky diodes is left on for a long time, the current will be limited and not cause the diodes to over heat. Resistors were added to the input of the common mode amplifier to limit this current. It would seem that adding the nonlinear capacitance of all of these diodes would affect linearity, but from simulation, the impact was actually very small. This is due to the symmetry and the resistance at these nodes being small compared to the capacitance of the diodes.

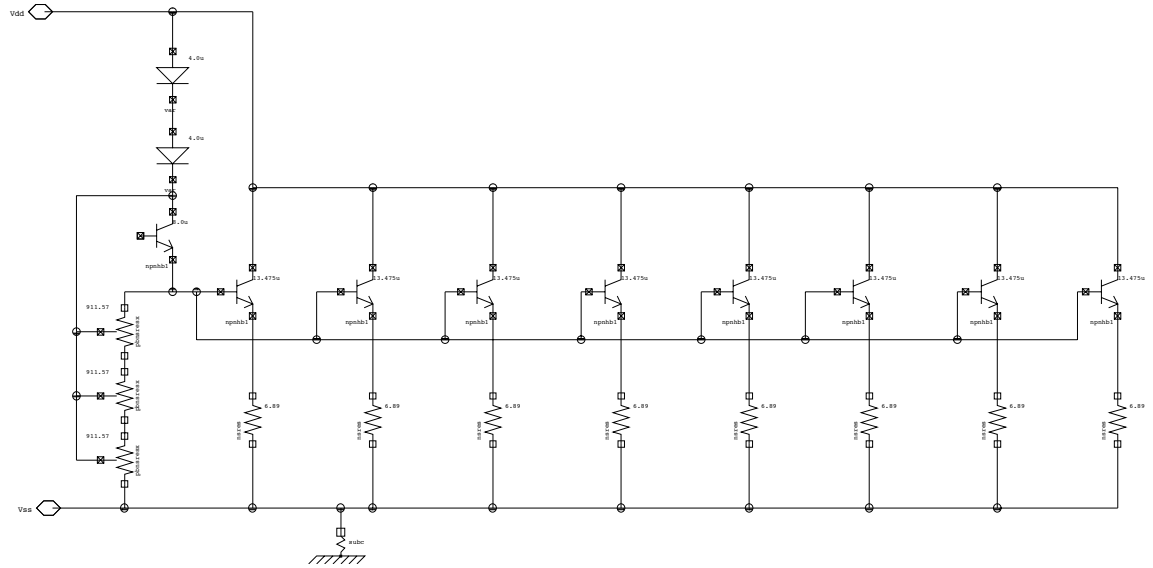

Figure 3-12: Clamp

3.9 Temperature Sensor

It is nice to know the temperature of the amplifier when testing it. With a constant current in a diode connected transistor, $V_{BE} = \frac{kT}{q} ln(\frac{I_C}{I_S})$. Due to the temperature dependence of I_S, V_{BE} has a temperature coefficient of approximately -1.25 $\frac{mV}{^oC}$. With four diode connected transistors in a row driven by a constant current source, the voltage across the temperature sensor will change by approximately -5 $\frac{mV}{^oC}$. The temperature sensor can be driven while power is disconnected from the rest of the chip, so voltage readings can be taken while the temperature on chip is the same as the ambient temperature. This allows the sensor to be characterized. While the chip is powered the temperature can be extrapolated from the characterization data and voltage across the sensor. It is also possible to run these tests using two different currents so that $\Delta V_{BE} = \frac{kT}{q} ln(\frac{I_2}{I_1})$ which is proportional to temperature. This method removes the temperature dependence of I_S but is more difficult to implement due to the need for two current sources. Four diodes in series were chosen, because adding more diodes makes a larger temperature coefficient but also takes up more room. Four is a reasonable compromise.

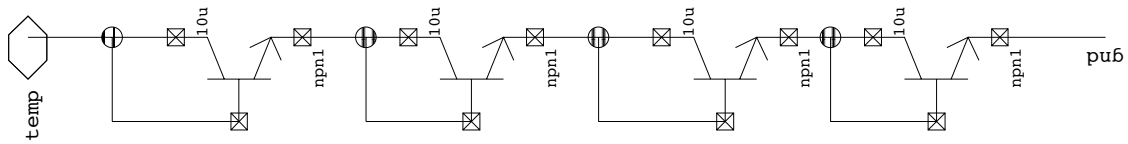

Figure 3-13: Temperature Sensor

Chapter 4

Circuit Elements

IBM 5HP has a number of options to choose from for transistors, resistors, capacitors, and diodes. Choosing which options to use was an important part of the design and was guided by the parameters provided in this chapter.

4.1 Transistors

The parameters for the transistor options in 5HP are shown in Tables 4.1 and 4.2. All poles in the signal path, except for the compensation pole, should be at as high of a frequency as possible to allow for maximum possible gain bandwidth product. In order to achieve this, all transistors in the signal path are high speed bipolar. With a maximum 2 V_{pp} differential output signal, it is reasonably simple to keep all V_{CE}'s between the 3.3 V breakdown voltage and the saturation voltage. The common mode amplifier is limited to low frequencies, since it is used for a DC correction. Thus, there is no need for high speed transistors. High breakdown bipolar transistors are used to eliminate any concern about voltage ranges. If the external amplifier was going to be eliminated, it would probably be best to use MOSFETs on the inputs to this stage in order to reduce the input bias currents. The common mode amplifier uses one PFET, since the output of the internal amplifier is near the +5 supply. A transistor referenced to +5 was needed to make a current source. This requires a p type device, and, since there are no PNPs, a PFET was used.

Table 4.1: NPN Transistor Parameters [6][7]

Type	$\mathbf{BV_{ceo}}$ [V]	**Gain**	$\mathbf{f_t}$ [GHz]	$\mathbf{f_{max}}$ [GHz]	$\mathbf{V_{early}}$ [V]
High Speed	3.3	100	46	65	65
High Voltage	5.5	80	30	55	124

Table 4.2: FET Transistor Parameters [6][7]

Type	$\mathbf{T_{ox}}$ [nm]	$\mathbf{L_{eff}}$ [μm]	$\mathbf{G_{msat}}$ [$\mu S/\mu m$]	$\mathbf{I_{Dsat}}$ [$\mu A/\mu m$]
NFET (10 μm/0.5 μm)	7.8	0.39	195	400
PFET (10 μm/0.5 μm)	7.8	0.39	103	400

4.2 Resistors

There are several types of resistors available in 5HP and their key parameters are shown in Table 4.3. The pbdtres is a polysilicon resistor over a deep trench. It provides a reasonable resistance per square and has very low voltage and temperature coefficients. The deep trench version has lower capacitance than the N+ sub-collector ground plane version, which has less substrate coupling. Many substrate connectors to ground are placed on the die so reducing substrate coupling seemed less important than reducing parasitic capacitance. Thus, the pbdtres is used for all resistors in this design except for very large and very small resistors. The ballast resistors in the output stage are only 5 Ω each, so a pbdtres would have to be excessively wide. The nsres is a N+ sub-collector resistor and is used for the ballast resistors because of its low resistance per square. The resistor used for compensation in the common mode amplifier is 300 kΩ, which would require an extremely long pbdtres. The frdtres was used for these resistors due to its large resistance per square and small parasitic capacitance.

Table 4.3: Resistor Parameters [6][7]

Resistor	$\mathbf{R_{\square}}$ [$\Omega/\square$]	**Tolerance** [%]	**TCR** [ppm/^{o}C]	**Capacitance** [fF/μm^2]
pbdtres	270	10-15	21	0.11
nsres	8	15	1460	0.12
frdtres	1600	25	-1105	0.09

4.3 Capacitors

Table 4.4 gives the parameters for the two capacitor types in 5HP. The MIM cap is a metal insulator metal capacitor. It has a smaller capacitance per area but a much better voltage coefficient than the DCAP which is a metal oxide semiconductor capacitor. The only capacitor in the signal chain is the compensation capacitor in the gain stage, which has fairly small capacitance. The MIM cap is used for the gain stage compensation capacitor to increase linearity. The DCAP was used for all other capacitors in the design to save area.

Table 4.4: Capacitor Parameters [6][7]

Capacitors	**Capacitance** [fF/μm^2]	**Tolerance** [%]	$\mathbf{T_{CC}}$ [ppm/^{o}C]	$\mathbf{V_{CC}}$ [ppm/V]
DCAP	1.5	10	48	1740
MIM Cap	0.7	15	-57	<25

4.4 Diodes

There are three main types of diodes for use in 5HP and a ns diode can also be built for high voltage ESD protection. The forward voltage of these diodes is shown in Table 4.5. The Schottky diode is a guard ring Schottky barrier diode. The PIN diode is an extrinsic collector base diode. The VARactor diode is an intrinsic collector base diode. The PIN diode is used for ESD protection, except for the +15 diode, which is a ns diode, as discussed in Section 3.8. Schottky diodes are used to limit the differential inputs for the gain stage and the common mode amplifier. They were chosen due to

their low capacitance per area.

Table 4.5: Diode Parameters [6][7]

Diode	**Forward Voltage** [mV]	**@ Current** [μA]
Schottky	300	100
PIN	790	100
VARactor	810	100
NS	unknown	

Chapter 5

Package

The package selected for this amplifier is IPAC's QFN20B [4]. This is a 5 mm x 5 mm package with 0.65 lead pitch. The die is only 1.2 mm x 1.2 mm. A smaller package would have plenty of room for the die, but the larger package was chosen for its larger lead pitch and its thermal characteristics. The next smaller package has a 0.5 lead pitch which is more difficult to put on a printed circuit board (PCB). This style of package has a metal bottom which can be attached to the bottom of the die. This connection allows for a better substrate to ground connection as well as a way to dissipate the heat from the die to the PCB. A picture of the package is shown in Figure 5-1.

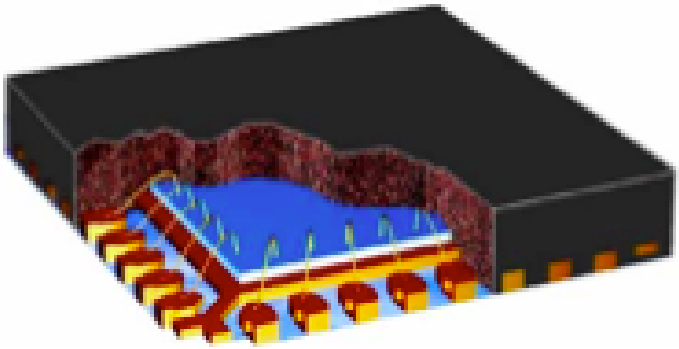

Figure 5-1: Package Picture [4]

5.1 Die Temperature

This package has a thermal resistance of approximately $65^oC/W$. If the temperature around the package is 30^oC and the power dissipated by the amplifier is 700 mW, the average die temperature will be approximately 75^oC.

5.2 Pin Out

The pin out of the amplifier is shown in Figure 5-2. The flow of the main amplifier is from left to right. Ground pins are placed around the inputs and outputs to isolate the differential signals. The common mode inputs come in the top. They are not separated by ground, because they are low frequency signals. There are two +5 supply pins because of the large amount of current coming from that supply. Additionally, using separate +5 supplies for different parts of the circuit was considered. Having two +5 pins allowed for flexibility in the design. +15 comes in from the top to be near the top of the gain stage. The die only has 16 pads, so the four corner package pins are not connected.

5.3 Package Model

The package model from IPAC has inductance and capacitance values that are suspiciously small and does not include mutual inductance or capacitance. Thus, the setup shown in Figure 5-3 was put into a 3-D field solver which gave the S parameters of the pins [5]. The setup only includes three bond wires. This should be sufficient, because on two sides there are only three connected pins. On the other sides, the pins of interest are surrounded by ground pins. Combining the information from the S parameters with the rule of thumb of about 1 nH of inductance per millimeter of bond wire gives the package model shown in Figure 5-4. The package model shown is for a side with three pins; for the five pin sides, it is just extended to have another two pins. The bent arrows between inductors represent mutual inductance. The ground symbols in the figure represent the metal plate on the bottom of the package.

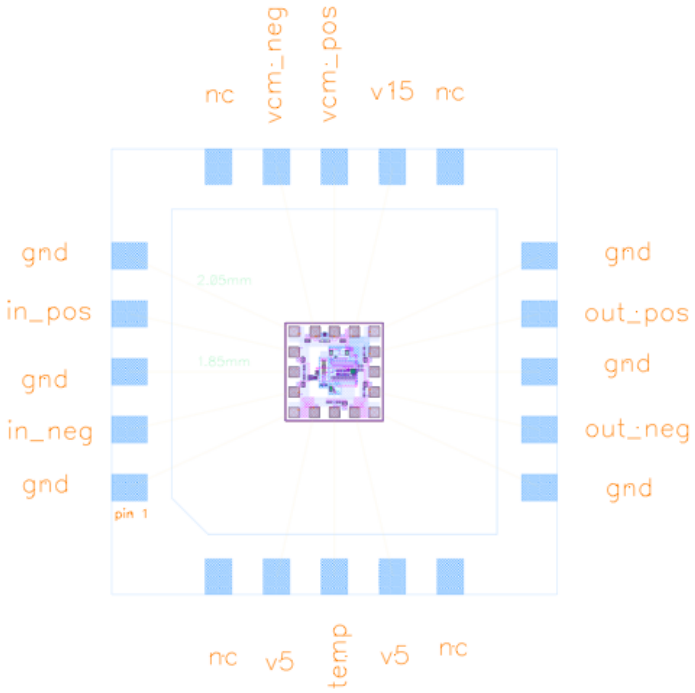

Figure 5-2: Pin Out

The metal plate will be directly connected to ideal ground on the PCB. In addition to simulating with this package model, simpler models involving just inductors of various values were used to check stability. Therefore, even if this package model is inaccurate, the amplifier should still be stable. However, some results, such as the bandwidth and the exact phase margin, will vary if the package model is incorrect.

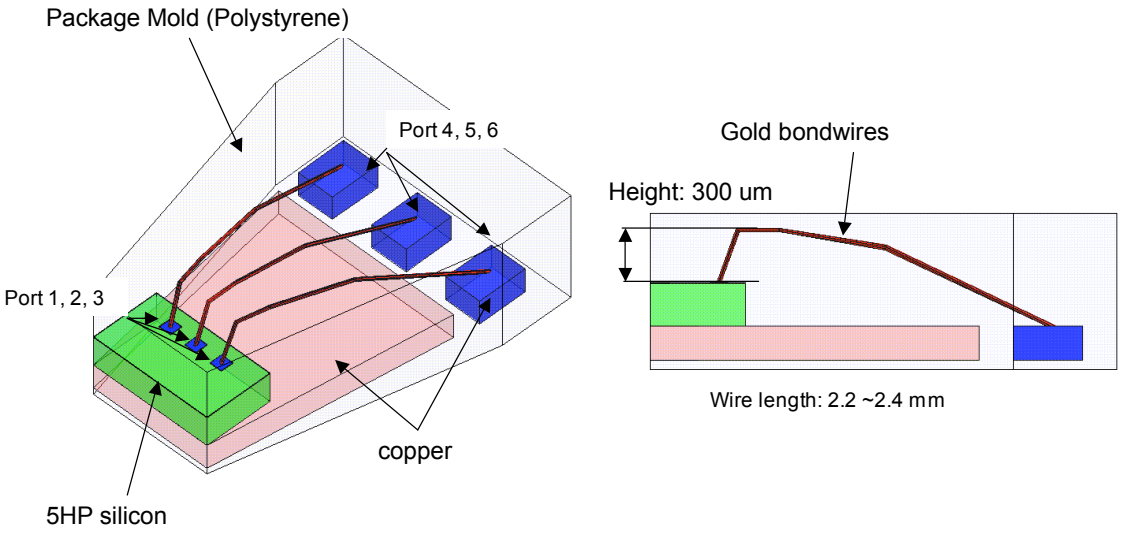

Figure 5-3: 3-D Bond Wire View [5]

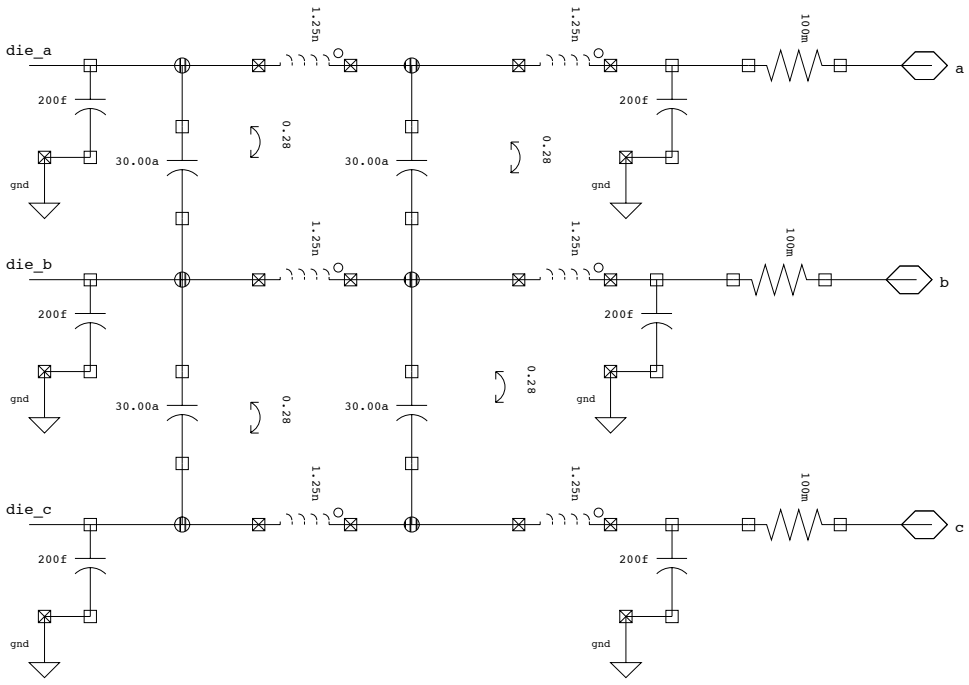

Figure 5-4: Package Model

Chapter 6

Layout

There are a number of considerations that must be taken into account during layout to keep the performance from significantly deviating from the schematic simulation predictions. The main differences between the schematic and the actual chip are temperature gradients, component mismatches, wiring resistance, wiring capacitance, and substrate coupling.

Overall temperature changes and device self-heating are accounted for in the schematic simulations, but temperature changes due to adjacent elements cannot be taken into account without the actual layout. All elements have parameters that vary with temperature, so if one side of the signal path is hot while the other is cool, a mismatch can occur. In order to minimize mismatch, elements on the signal path are cross-quaded. If there is a temperature gradient, with cross-quading, each side will have one cool and one hot device causing the effect to be symmetric. Additionally, the effect of temperature gradients can be minimized by placing elements from both sides close to each other so that the difference in temperature will be small.

Process mismatch is another important deviation from ideal. Wafer to wafer mismatch can be accounted for in schematic simulations by varying parameters such as the sheet resistance. However, mismatches across a die cannot be accounted for without knowing where the elements are on the die. Process changes across a die can be seen as a gradient and thus are minimized by the same techniques used for temperature gradients, cross-quading and keeping elements close to each other. Additionally,

lithography can be affected by the surrounding shapes, so where matching is important, making sure that the surrounding devices are the same for elements on both sides is beneficial. Additionally, making devices wide and long causes lithography variations to be a small portion of device size and thus cause less variation in device parameters. Of course, making devices smaller has advantages, because smaller devices take up less area and minimize parasitic capacitances. A trade off between matching and minimizing parasitics must be made when choosing device sizes.

Wires have parasitic resistance and capacitance. The resistance depends on the particular layer of metal, width, and length. The capacitance depends on the particular layer of metal, area, and the wire's immediate environment. Wire lengths should be minimized, as this reduces both the resistance and capacitance. This is mostly done by putting elements as close together as possible. Minimizing resistance and capacitance is not as important as matching them on both sides, so in a few cases where one wire would be much longer than the other, the shorter one will be extended. This can be seen on the wires coming into the die from the input pads. The selection of the width of a wire involves a trade off between three factors: resistance, capacitance, and maximum current. Most of the wires are fairly short, so wires carrying high frequency signals are made wide enough to handle the maximum current and no wider to minimize capacitance. Wires carrying power are made wide in order to minimize voltage drops across them. In some cases, such as the wires which carry the power to the output stage, the wires cannot be made wide enough, so several layers are used together. The Cadence Assura tools were set up to extract parasitic capacitance but not resistance, so hand calculations were done to check maximum power ratings and approximate resistances. Resistors could have been added to the schematic for simulation. However, all of the resistances were a small portion of the resistance they were connected to so this was unnecessary.

To minimize substrate coupling, substrate to ground connections were made all along the ground rings surrounding each circuit block. These ground rings are used to make sure that there are low impedance paths to ground.

When laying out the ESD devices, it is very important to make sure that the wiring

can handle the large currents involved in an ESD event. In order to accomplish this, a wide ring of ground and one of +5, both on the top metal layer, run around the entire die just inside of the pads. These rings provide power and ground to the entire die and also provide low impedance paths to connect pins, ESD diodes, and clamps. The clamps are on the left and right sides of the die, so that the furthest path an ESD current would have to travel is about one side of the die.

The temperature sensor is very close to its pin, so that it does not get in the way of anything else on the die. It will measure the temperature on the side of the die and will not give any information about the hottest points such as near the output stage. While it would be good to know the maximum temperature, it is not worth sacrificing performance by changing the signal path layout to fit in the temperature sensor.

The feedback wire is an important wire, since it must carry the output signal back to the input. Having capacitance between the input and output creates either a large capacitance through the Miller effect if the signals are out of phase, or, if they are in phase, it creates positive feedback, which can cause oscillation. In this layout, the feedback wire only goes over ground, the current reference going to the common mode amplifier, and the resistors in the gain stage. Going over the resistors in the gain stage is not an issue, because they come after the gain. Going over the common mode amplifier current reference is not ideal, but since the wires are narrow, the mutual capacitance will be small. In addition, the effect is captured by the capacitive extraction, so if there was an issue, the simulator would catch it.

The final layout is shown in Figure 6-1, and a picture of the die is shown in Figure 6-2.

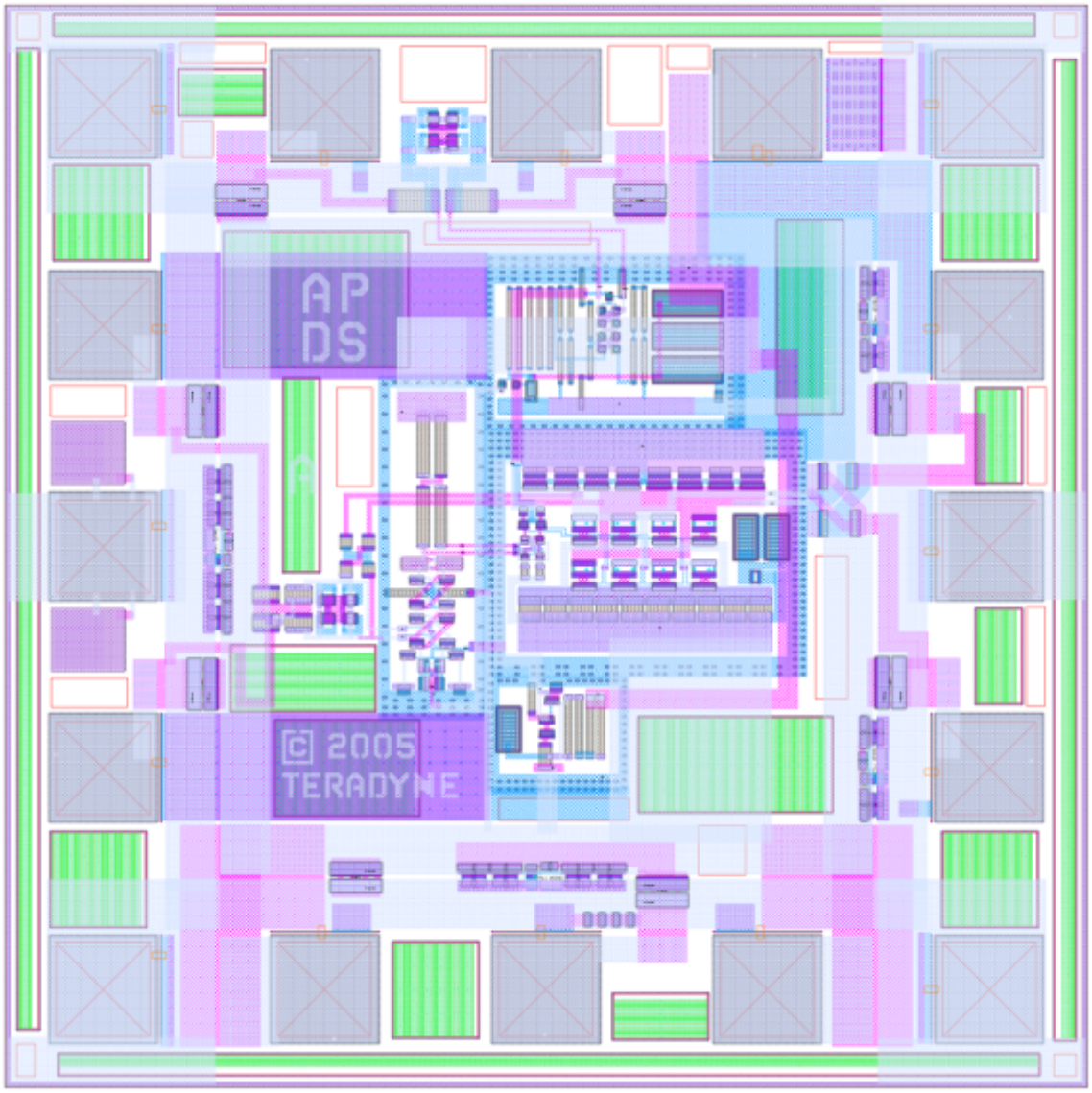

Figure 6-1: Layout

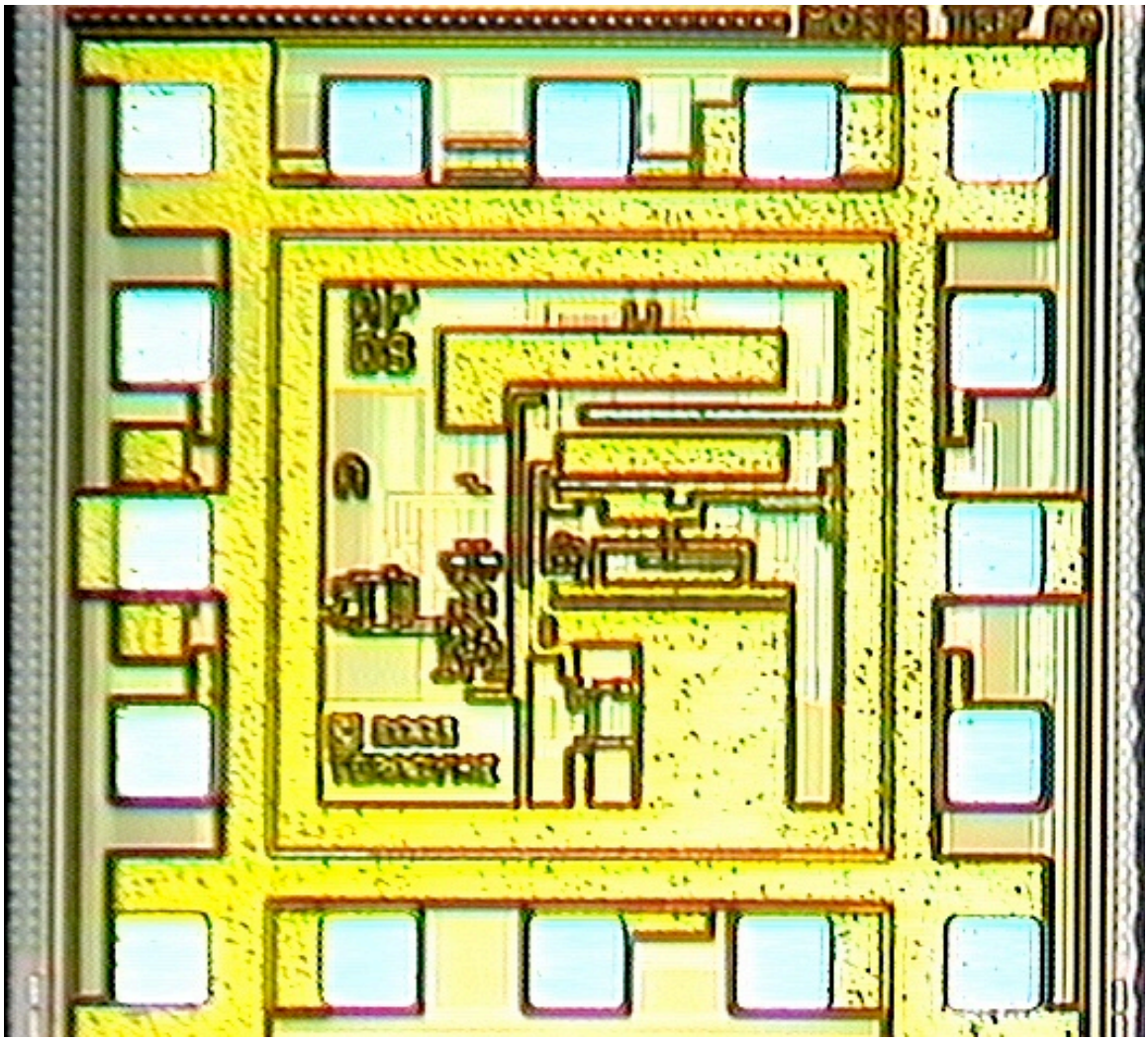

Figure 6-2: Die Picture

Chapter 7

Simulations

7.1 Test Conditions

There are three main variations between amplifiers and their operating conditions that need to be taken into account: process variations, temperature, and power supply voltages. Three tests were run for each parameter. Those three tests are named slow, normal, and fast. Slow and fast cover opposite ends for each variation, and normal has the standard values. The process variations are accounted for by inputting the σ values for bipolar transistors, NFETs, PFETs, and resistors into the simulator. Corners of $\pm$ 1.5σ were used for each, which gives a reasonably large overall variation. The die temperature was tested over a range of 25^{o}C to 125^{o}C. Maximum variations of $\pm$ 200 mV seemed like reasonable requirements to place on the power supplies, so this is the range used for testing. Table 7.1 shows the parameters used for each type of run.

7.2 Mismatching

Several of the characteristics of the amplifier depend heavily on the mismatching of the two halves of the differential signal path. Ideally, Monte Carlo simulations would be used to see the full range of possibilities from the amplifier. However, to get statistically significant information from Monte Carlo simulations requires a fairly

Table 7.1: Test Conditions

Specification	**Slow**	**Normal**	**Fast**
Bipolar corner [σ]	-1.5	0	1.5
NFET corner [σ]	-1.5	0	1.5
PFET corner [σ]	-1.5	0	1.5
Resistor corner [σ]	1.5	0	-1.5
Temperature [^{o}C]	25	75	125
+15 Supply [V]	14.8	15	15.2
+5 Supply [V]	4.8	5	5.2

large number of runs and thus an unacceptably large amount of computation. Instead, the amplifier is mismatched by hand. Rather than mismatching each component in the signal path, just the feedback and input resistors were mismatched, since they have the strongest effect on the overall mismatching of the two sides. The resistors are mismatched significantly more than they would ever be in practice, in order to account for the mismatches of all of the other devices. The input resistors and feedback resistors are mismatched by ± 20%, so one gain is up 50% and the other is down 33%. Since these resistors are mismatched well beyond what would be expected, the results from the mismatched tests should be fairly pessimistic.

7.3 Harmonics

The most important specification for this amplifier is its linearity. The metrics used to measure the linearity of the device are the second and third harmonics and the intermodulation distortion. In order to test the second and third harmonics, the common mode input and common mode reference were set to 1.55 V, and the differential input was a sine wave voltage source set so that the output magnitude was within 0.3 dB of 2 V_{pp} differential. The load was a 6 kΩ resistor in parallel with a 6 pF capacitor across the differential output. SpectreRF's periodic steady state analysis was used to run the simulation. In order to simulate harmonics with the resolution needed, the default simulator parameters were not sufficient. Tightening tolerances and using the gear2only integration method increased the accuracy enough for these

simulations. The second and third harmonics were measured relative to the output fundamental and reported at the frequency of the fundamental. For the second harmonic, the result would be zero distortion at all frequencies if the amplifier was perfectly matched. Thus, the second harmonic was measured with the amplifier mismatched as described in the Section 7.2. The second harmonic on the common mode signal was also measured. It was measured without mismatching and was measured relative to the fundamental on the differential output.

For the intermodulation distortion, two tones of very close frequency are required. In this case, for each frequency tested, the two tones were at ± 5% of that test frequency and had inputs set so that the outputs were -7 dB from 2 V_{pp} differential. With each output set to -7 dBFS, the RMS output is -4 dBFS, so the intermodulation distortion was measured relative to a -4 dBFS output. SpectreRF's quasi periodic steady state analysis was used to run the simulation. Just like the second and third harmonic simulations, the default settings had to be altered to meet the required accuracy. There were two harmonics of interest in this test at ± 15% of the test frequency. The larger of the two distortions was chosen as the result for that frequency.

7.4 Noise

The noise is measured by using the Spectre noise analysis. The models are provided by IBM, so they are as accurate as possible. However, the accuracy of the results is still questionable due to the difficulty of modeling and simulating noise. Since the signal chain is not completely a 50 Ω environment, noise figure is not a good metric. Thus, input referred noise is used to quantify the noise. The noise corner is measured as the frequency where input referred noise is 3 dB greater than the high frequency value. The noise corner is used to indicate where Flicker noise stops being the dominant factor.

7.5 Stability

Phase and gain margin are used to measure the stability of the main and common mode loops. For the main loop, it is inaccurate to only find the open loop bode plot and multiply the magnitude by the feedback factor, since the loading on the output from the ADC is significant but outside the feedback loop. Thus, the Middlebrook method [27] is used to measure stability metrics. This method places a voltage source in the loop at a point where one side has a much larger impedance than the other. The method then looks at the ratio of the signal on one side of the source to the other side. For the main loop, the voltage source is placed between the output and the feedback resistors. Since there are two loops, baluns were used to inject half of the voltage, 180^o out of phase, into each loop. For the common mode loop, the source was placed between the averaging resistors at the output and the input to the external integrator. The Spectre stability analysis was used to run these simulations.

7.6 Other Simulations

The power was measured by multiplying the current through each power supply by the supply voltage while the differential input was set to zero, and the common mode input and reference were set to 1.55 V. The rest of the tests were done by placing AC sources in appropriate places and running Spectre AC analysis. In addition to the tests used to get the reported results, AC sources were placed in various points to watch for any oscillations and to see if any signal had a strong effect on the output differential or common mode signals. Also a square wave differential input was used to make sure that the response had reasonable settling time and peaking.

Chapter 8

Results

The simulation results, obtained through the methods described in the previous chapter, are stated and discussed in this chapter. This amplifier has been fabricated, and second and third harmonic distortion results have been measured. For most of the results it is expected that simulation will closely match reality, except for noise and parameters that depend heavily on how mismatched the amplifier is.

In the tables in this chapter, a star after the description of the parameter being measured indicates that the amplifier was mismatched in order to get that set of specifications.

8.1 Harmonics

The harmonics can be seen in Table 8.1. The second harmonic values shown in the table are split into two categories: the second harmonic on the differential signal, due to mismatching, and the second harmonic on the common mode signal. While the input to the ADC is differential, it will have a finite common mode rejection ratio (CMRR). Since some ADC datasheets do not include their CMRR, it is hard to know which source of second harmonic will dominate. As long as the ADC's CMRR is above 30 dB, the differential signal will be the dominant factor. If this is the case, then the amplifier beats the target by at least 4.7 dB over all frequencies and operating regions.

The third harmonic, which can be seen in Table 8.1 and Figure 8-1, does not have the common mode issue, because it cancels for the common mode like the second harmonic cancels for the differential signal. According to simulation, the only point where the third harmonic does not outperform the target is the slow run at 500 MHz where it misses by 2.3 dB. At low frequencies, it is just barely above target, but for about 10 MHz to 100 MHz, it is significantly better than the target. This is not surprising, since low frequency distortion cancellation techniques were not used. Also, at the other end, the open loop gain has dropped off significantly. Overall, this meets the third harmonic specification.

The IMD simulation exceeds specification except for the slow run at 500 MHz like the third harmonic, which is to be expected, since this IMD results from the third order distortion. Unlike the third harmonic, the IMD exceeds the target by a good margin at low frequencies.

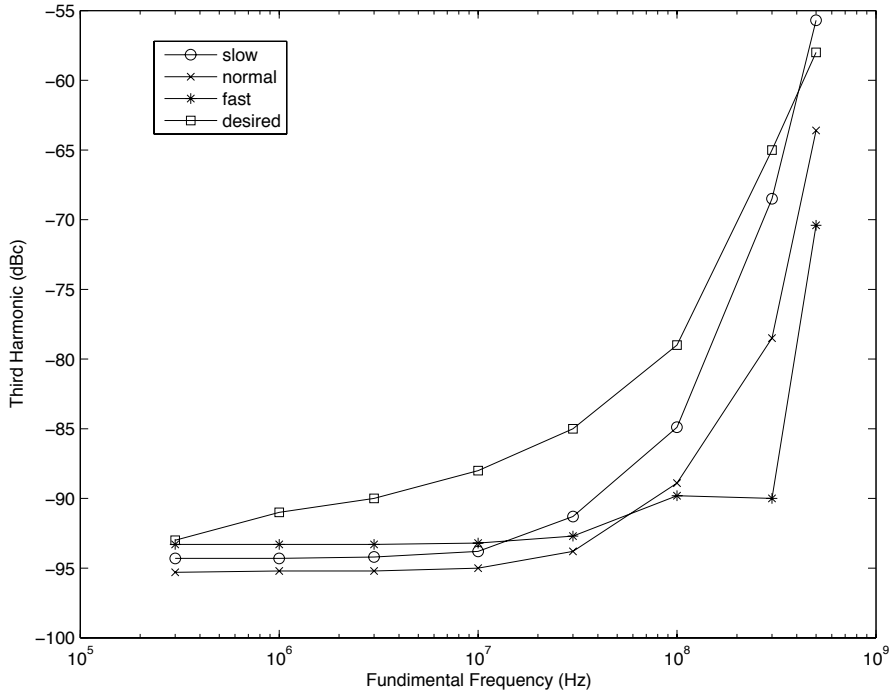

Figure 8-1: Third Harmonic

The second and third harmonics for the fabricated amplifier have been measured. In the lab test, the amplifier drove a 1 kΩ differential resistor and there was ap-

Table 8.1: Harmonics

Freq [MHz]	**Slow**	**Normal**	**Fast**	**Desired**
HD2 (differential only) * [dBc]				
0.3	-99.0	-105	-107	-93.0
1	-99.2	-105	-107	-91.0
3	-99.1	-105	-107	-90.0
10	-97.9	-101	-104	-88.0
30	-93.1	-93.8	-96.1	-85.0
100	-83.7	-83.1	-85.1	-79.0
300	-75.0	-73.0	-74.2	-65.0
500	-72.7	-70.8	-71.4	-58
HD2 (common mode only) [dBc]				
0.3	-71.5	-78	-80.6	n/a
1	-71.6	-78.2	-80.6	n/a
3	-71.6	-77.8	-80.2	n/a
10	-70.6	-74.7	-77.1	n/a
30	-66.1	-67.1	-69.6	n/a
100	-56.2	-56.1	-58.4	n/a
300	-45.3	-44.4	-46.2	n/a
500	-38.7	-38.7	-40.3	n/a
HD3 [dBc]				
0.3	-94.3	-95.3	-93.3	-93.0
1	-94.3	-95.2	-93.3	-91.0
3	-94.2	-95.2	-93.3	-90.0
10	-93.8	-95.0	-93.2	-88.0
30	-91.3	-93.8	-92.7	-85.0
100	-84.9	-88.9	-89.8	-79.0
300	-68.5	-78.5	-90.0	-65.0
500	-55.7	-63.6	-70.4	-58
IMD3 [dBc]				
0.3	102	-104	-101	-93.0
1	-102	-104	-101	-91.0
3	-102	-104	-101	-90.0
10	-102	-104	-101	-88.0
30	-101	-103	-101	-85.0
100	-86.3	-89.1	-90.4	-79.0
300	-75.7	-82.8	-88.5	-65.0
500	-57.7	-66.6	-70.7	-58.0

proximately a capacitance of 10 pF from each output to ground. The capacitance is equivalent to a 5 pF differential load, so the load is slightly different than the load used for simulations. Figure 8-2 shows the measured second and third harmonics, the simulated third harmonic, and the third harmonic of the LMH6702. The data for the LMH6702 comes from Table 2-2. This figure shows that the third harmonic simulation and lab result are in fairly close agreement. The second harmonic is a bit worse than expected, but at high frequencies is still much better than what is available on the market.

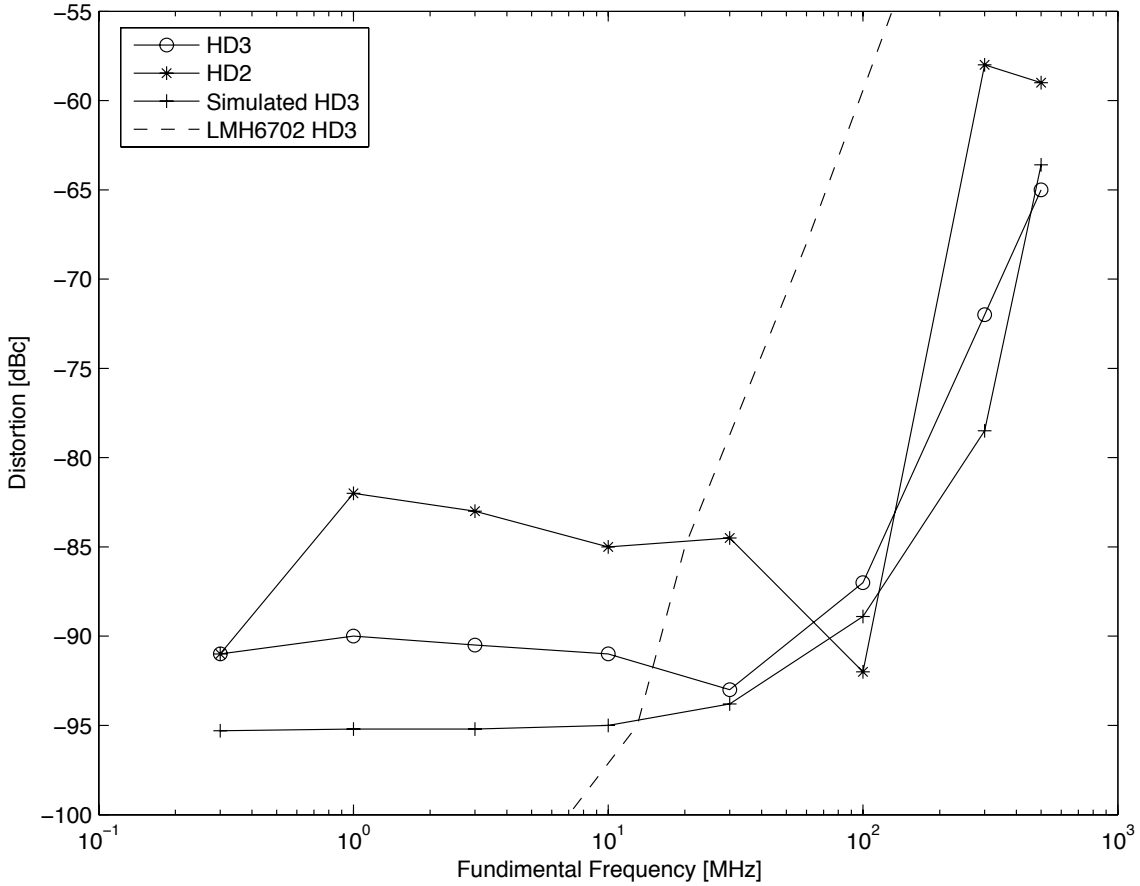

Figure 8-2: Second and Third Harmonics of Fabricated Amplifier, Simulated Third Harmonic, and Third Harmonic of LMH6702

8.2 Noise

The noise results can be seen in Table 8.2. The normal and fast runs meet the target for all frequencies, but the slow run misses by 0.5 to 1 $\frac{nV}{\sqrt{Hz}}$ for all frequencies. There is a large difference in noise between runs. One of the differences between runs is the sheet resistance, and the top noise contributors are the input resistors. From simulation, it looks like some chips will beat and some will miss the target by a small amount. However, noise is difficult to model and simulate, so it is likely that the errors will be large enough to push it well above or below the target for all chips. The top noise contributors can be seen in Table 8.3. This list shows that the majority of the noise comes from the input and feedback resistors. The next two top contributors are the shot noise from the input transistors and the emitter degeneration resistors. These two are fairly close, indicating that the gain stage current was well optimized for noise.

Table 8.2: Noise

Freq [MHz]	**Slow**	**Normal**	**Fast**	**Desired**
Input Referred Noise $[\frac{nV}{\sqrt{Hz}}]$				
0.3	6.01	4.87	4.21	n/a
1	5.70	4.81	4.19	5.00
3	5.61	4.79	4.18	5.00
10	5.58	4.78	4.18	5.00
30	5.57	4.78	4.18	5.00
100	5.56	4.77	4.18	5.00
300	5.54	4.75	4.16	5.00
500	5.49	4.71	4.12	5.00
Noise Corner [kHz]	49.3	12.1	4.76	n/a

8.3 Gain

The gain and its frequency dependence can be seen in Table 8.4. The slow run's bandwidth is a bit lower than desired. However, these results include 10 Ω external resistors in each output, so if more bandwidth is required, then those resistors can

Table 8.3: Top Noise Contributors

Source	**Percent of Total**
Input Resistors, Johnson Noise	29.5
Feedback Resistors, Johnson Noise	13.6
Input Transistors, Shot Noise	11.9
Emitter Degeneration Resistors, Johnson Noise	9.0
Input Transistors, Johnson Noise	7.6
Current Mirrors, Johnson Noise	5.7
Current Mirror Degeneration Resistors, Johnson Noise	3.5

be reduced. The bandwidth is larger than what would be expected from looking at the output impedance and the capacitance of the ADC input. This is due to the inductance of the package model. This inductance also causes peaking in the output if there are no external resistors. Depending on the accuracy of the package model, the external resistance needed to achieve the desired bandwidth may vary.

Table 8.4: Gain

Freq [MHz]	**Slow**	**Normal**	**Fast**	**Desired**
Gain [dB]				
1 Hz	6.01	6.07	6.10	6.000
0.3	6.02	6.07	6.10	n/a
1	6.02	6.07	6.10	n/a
3	6.02	6.07	6.10	n/a
10	6.02	6.07	6.10	n/a
30	6.01	6.07	6.10	n/a
100	5.97	6.05	6.09	n/a
300	5.57	5.82	5.99	n/a
500	4.59	5.16	5.57	n/a
Bandwidth [MHz]	694	800	890	750

8.4 Input and Output Impedance

The low frequency input and output impedances are shown in Table 8.5. The input impedance target is 400 Ω, and the result matches this to within 10.5%. The tolerance results from the variation in sheet resistance. According to the overall system

specifications, this is acceptable.

Table 8.5: Low Frequency Input and Output Impedances

Specification	**Slow**	**Normal**	**Fast**	**Desired**
Input Impedance [Ω]	440	397	358	400
Output Impedance [Ω]	49.4	45.4	42.0	n/a

8.5 Stability

Both the main loop and the common mode loop need to be stable in order for the amplifier to function. Since both have fairly simple open loop transfer functions, phase and gain margin are good metrics for measuring stability. For the main loop, the target is a phase margin of around 60^o and a gain margin of greater than 10 dB. A phase margin of 60^o has the fastest possible settling time and a reasonably small amount of ringing. A gain margin of greater than 10 dB makes the phase margin the dominant factor in the stability. The reported phase margin includes the 10 Ω external resistors. Without those resistors the phase margin is a bit lower, so the phase margin was designed to be greater than 60^o with the external resistors. With this choice, the amplifier will have good stability regardless of choice of external resistors. As can be seen from Table 8.6, the phase margin and gain margin both exceed the targets by a small margin. One note on the main loop DC gain is that the numbers reported are for the gain around the whole loop. The feedback factor is one third, so, to get the open loop forward gain, 9.5 dB should be added to the numbers in the table. The step response from the differential input to differential output is shown in Figure 8-3.

The phase margin occurs where the loop transmission is one. Since the feedback factor is one third, the forward gain bandwidth product is approximately three times the frequency where the phase margin occurs. However, the loop gain at the third harmonic frequency is what helps reduce the third harmonic. Thus, the feedback reduces the third harmonic up to 383 MHz. This correlates well with the location at which the third harmonic starts to have a large slope. Another interesting note is

that the open loop dominate pole is around 75 MHz. The important factor for the third harmonic for signals above 25 MHz is the gain bandwidth product, while for signals below 25 MHz it is the DC gain that matters.

The common mode loop is designed for a DC correction. Its settling time should be reasonable, but there is no need to minimize it. Therefore, being a bit below the 90^o of phase margin from the integrator is perfectly acceptable. Table 8.6 shows that the phase margin is rather high. The gain margin should be greater than 10 dB so that the phase margin is the dominant factor. As can be seen from the results, the gain margin is well above the target. The loop gain needs to be greater than 63.8 dB to achieve 1 part in 1550 precision, and the loop gain from simulation is at least 7 dB greater than this target. The step response from the common mode reference voltage to the common mode output voltage is shown in Figure 8-4.

Table 8.6: Loop Stability

Specification	**Slow**	**Normal**	**Fast**	**Desired**
Main Loop Stability				
Phase Margin [^{o}]	73.8	73.8	74.0	60
@ [GHz]	0.897	1.15	1.45	n/a
Gain Margin [dB]	13.6	14.2	14.5	10
@ [GHz]	3.92	4.77	5.88	n/a
DC Loop Gain [dB]	23.7	24.9	25.7	n/a
Common Mode Loop Stability, with External Integrator				
Phase Margin [^{o}]	85.7	82.0	79.5	60
@ [kHz]	6.70	13.0	14.5	n/a
Gain Margin [dB]	50.6	43.8	40.6	10
@ [kHz]	600	562	571	n/a
DC Loop Gain [dB]	73.0	78.7	81.5	63.8

8.6 Rejection Ratios

Signals from different sources which affect the differential output voltage are the source of some important non-idealities. The common mode signal as well as signals on the power supplies can change the differential output. If the amplifier was per-

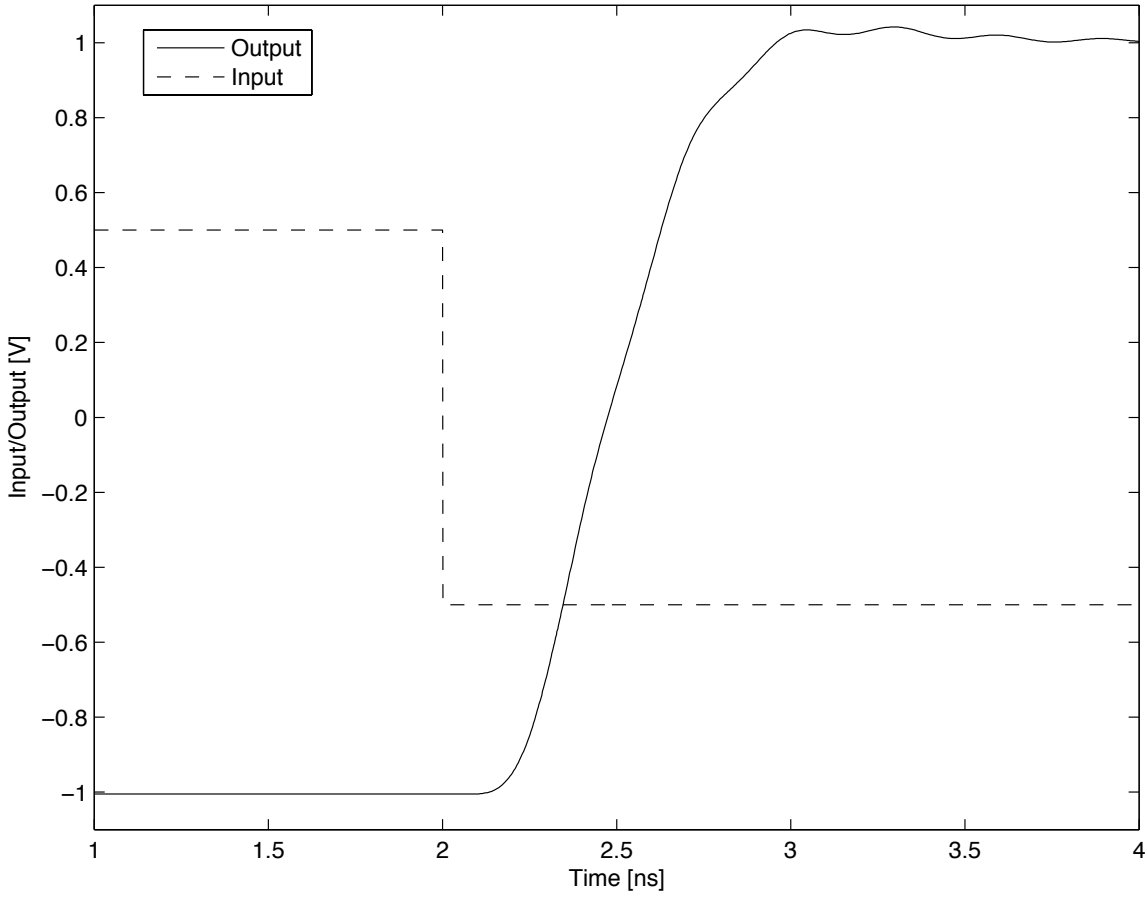

Figure 8-3: Main Loop Differential Step Response

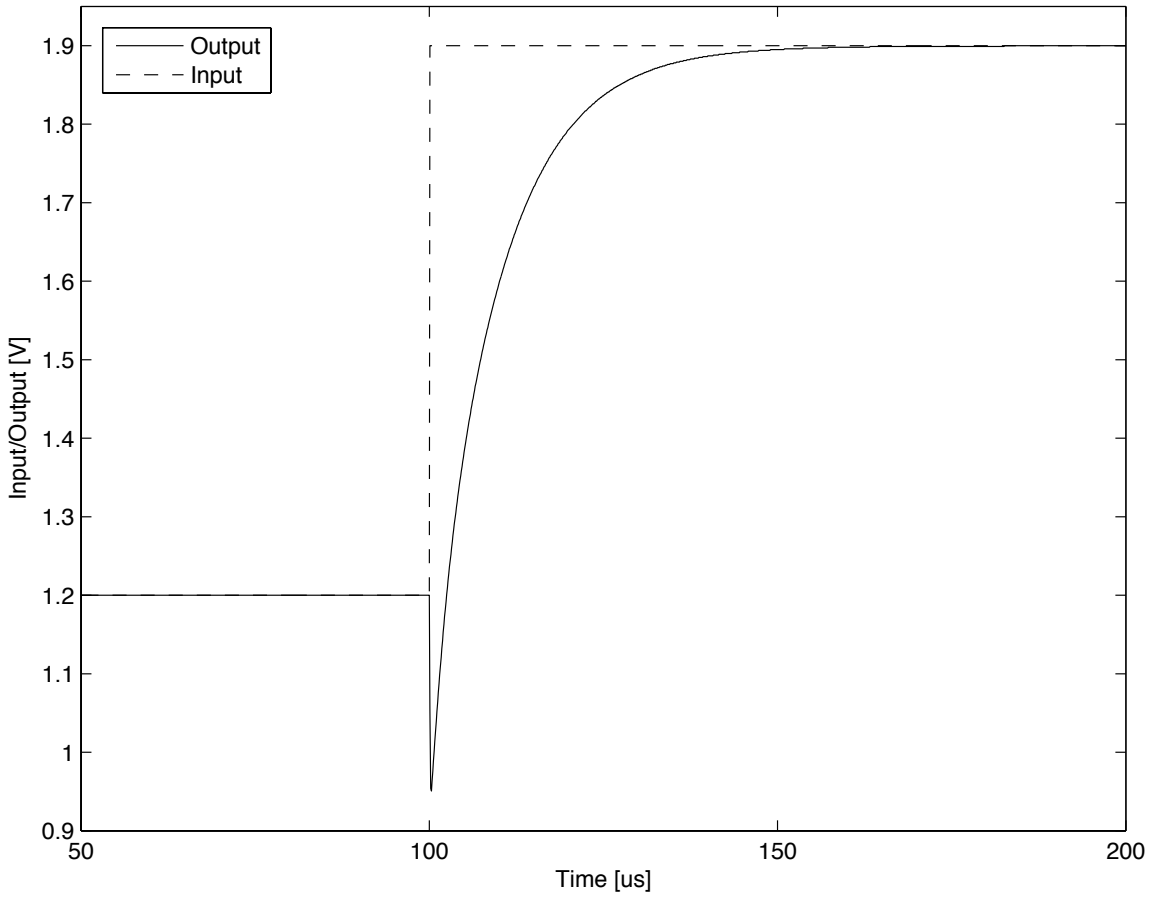

Figure 8-4: Common Mode Loop Step Response

fectly matched, the common mode and both power supply rejection ratios would be extremely large. However, when the sides are mismatched, the rejection ratios are finite. These ratios are shown in Table 8.7. While these ratios do not have target specifications, it is important that they are reasonably large, and definitely not negative. These ratios specify the requirements for the power supplies and the previous stage's common mode signal. The results are not great, but should be fine for this application.

Another interesting non-ideality is the common mode to common mode rejection ratio. Even with the amplifier perfectly matched, some portion of the input common mode signal shows up in the output common mode signal. This is important, because the ADC has a finite CMRR. If the stage previous to this amplifier has a signal on its common mode output, such as the second harmonic, then the amount of that signal which gets to the ADC's common mode input will affect the value the ADC reports as the differential input. It is also important to see that, at very low frequencies, changes in the input common mode signal do not affect the common mode output signal. As can be seen from the results, the common mode to common mode rejection ratio at very low frequencies is very high, and thus this will not be an issue. It is difficult to come up with a target at other frequencies, since for many ADCs the CMRR is unknown.

8.7 Output Common Mode Range

With the input common mode voltage at 1.55 V, the output common mode voltage can match the reference from 0.6 V to 2.6 V. With the input common mode voltage equal to the reference, the output common mode voltage can match the reference from 1.2 V to 2.6 V. The minimum input common mode voltage is limited by the already small V_{CE} of the gain stage current mirrors. With about 250 mV across the current mirror degeneration and V_{BE}'s of about 800 mV, the V_{CE} of the current mirrors is the input common mode voltage minus 1.05 V. Thus, with the input common mode voltage at 1.2 V the current mirrors have $V_{CE} = 150$ mV, so these transistors are

Table 8.7: Rejection Ratios

Freq [MHz]	**Slow**	**Normal**	**Fast**
Common Mode to Differential * [dB]			
1 Hz	26.9	26.8	26.7
0.3	26.3	26.0	25.8
1	26.6	26.4	26.2
3	26.6	26.4	26.3
10	26.6	26.4	26.3
30	26.6	26.4	26.3
100	26.2	26.0	26.0
300	24.6	24.4	24.3
500	24.3	23.7	23.3
+15 Supply to Differential * [dB]			
1 Hz	88.0	93.4	98.0
0.3	53.5	50.6	48.7
1	56.8	51.3	49.1
3	57.3	51.4	49.2
10	57.2	51.3	49.1
30	55.9	51.0	48.9
100	50.2	49.0	47.9
300	42.6	43.3	43.9
500	40.8	41.1	41.6
+5 Supply to Differential * [dB]			
1 Hz	121	128	124
0.300	45.5	44.7	42.6
1	45.1	44.5	42.3
3	45.3	44.8	42.8
10	47.3	47.5	46.3
30	50.5	51.4	46.2
100	48.1	47.8	48.4
300	40.8	40.4	40.9
500	37.7	37.9	37.9
Common Mode to Common Mode [dB]			
1 Hz	82.8	88.2	91.3
0.3	19.2	17.5	16.4
1	26.6	24.5	23.2
3	29.2	26.9	23.7
10	29.2	27.0	26.0
30	26.5	25.3	24.7
100	18.6	18.6	18.8
300	10.9	10.6	10.9
500	8.80	8.05	7.93

well into the saturation regime. It is actually somewhat surprising that the output common mode can track the reference all the way to 2.6 V. The bases of the cascode in the common mode amplifier are biased at 2.3 V, so when an input is $\geq$ 2 V, the input transistor is in saturation. As the reference approaches 2.6 V, the output of the integrator must be much larger than the reference, since the gain of the internal amplifier will be very low. Eventually the difference exceeds 0.6 V, and the input protection diodes turn on. If the reference slightly increases, then the output of the integrator will go all the way to the power rail, since the protection diodes will keep the input to the internal amplifier fairly constant. This occurs around 2.6 V. As the reference continues to increase, the output of the integrator stays fixed at the power rail. However, the negative input of the internal amp increases, so the output common mode voltage decreases. While the common mode can track all the way to 2.6 V, operating in this regime is not recommended. Constant current will flow through the protection diodes, and the loop will be on the edge of not being able to track the reference.

8.8 Power

The power dissipation is rather large compared to commercially available amplifiers intended for similar applications. As stated previously, one of Teradyne's advantages in performance is that test systems can dissipate fairly large amounts of power. Therefore, using 700 mW for an amplifier is not an issue if this value gives the desired performance. The power dissipation under different test conditions can be seen in Table 8.8.

Table 8.8: Power Dissipation

Specification	**Slow**	**Normal**	**Fast**
+15 Current [mA]	13.1	14.5	16.0
+5 Current [mA]	84.2	92.8	102
Power Dissipation [mW]	598	681	775

Chapter 9

Conclusion

Amplifiers on the market fall short of the high frequency linearity performance of ADCs by a factor of 10. This makes the amplifiers that drive the ADCs bottlenecks in the performance of analog signal chains. One case where this performance is particularly important is in UWB devices, since they require high performance over a large bandwidth. Thus, a key element in designing an UWB test system is creating an amplifier with a factor of 10 improvement in high frequency linearity which also maintains impressive low frequency linearity and reasonable noise performance.

This thesis described the design of an amplifier aimed at meeting the above specifications. The key element in improving the high frequency linearity was to make the output stage Class A with a bias current more than double the maximum output current. Trading increased power dissipation for greater linearity is reasonable for a test system, since power dissipation is not as important as performance. The use of voltage feedback with low open loop DC gain but high gain bandwidth product also improved the high frequency linearity. Making the open loop DC gain small compared to most feedback amplifiers allowed for a gain stage with good open loop linearity while still providing the same open loop gain to closed loop gain ratio at high frequencies. This approach worked well for this application because of the availability of a high voltage (15 V) power supply. The key to the high gain bandwidth product was using a process with very high f_T devices and a large enough breakdown voltage to handle the 2 V_{pp} differential signals. Several gain stages were investigated,

but it was found that using a cascode to keep the input transistors' collectors at a constant voltage and emitter degeneration made the only significant improvement in high frequency linearity. The input impedance of the buffer following the gain stage was discovered to be important for achieving very low distortion at low frequencies. The choice of a fully differential amplifier is dictated by the differential inputs of high performance ADCs but is also a key factor in reducing distortion due to the canceling of even harmonics in the differential output signal.

Simulations indicate that a factor of 10 improvement in high frequency linearity, very good low frequency linearity, and reasonable noise performance were achieved. Initial lab tests on the fabricated chips demonstrate functionality and indicate that the resulting harmonics are close to those predicted by simulation.

If simulation results continue to be confirmed in the lab, there are a number of areas for improvement in future versions of this amplifier. The most obvious is trying to make the output stage more efficient while maintaining its linearity. If the power consumption is reduced, the possible applications of the design would greatly increase. Another obvious improvement would be redesigning the internal common mode amplifier so that an external amplifier is not required to meet the common mode reference matching requirements of high performance ADCs. The single-ended even harmonics cancel in the differential output signal but add in the common mode signal. Thus, improving the single-ended even harmonics would allow this design to maintain its low distortion even if the ADC it is driving has a poor CMRR. Additionally, the CMRR, high frequency PSRR, and high frequency common mode input to common mode output rejection ratio of this amplifier are acceptable but not impressive and could use some improvement. Improving the noise performance of this amplifier would expand its possible applications, as it would no longer need to follow a low noise amplifier for the signal chain to have very low input referred noise.

In conclusion, according to simulation the amplifier described in this thesis meets the target specifications, including a factor of 10 improvement in high frequency linearity.

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