The Design of a High Efficiency RF Power Amplifier for an MCM Process

by

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Abstract

In this thesis, I addressed issues arising in the design of a high efficiency RF power amplifier for the Draper Laboratory multi-chip module (MCM) process. A design for a 2.3 GHz PCB amplifier using an enhancement-mode pHEMT device that achieves 68.9% PAE at 30 dBm output power is presented. Analysis of heat management, die connection parasitics, and transmission line structures in the context of the MCM process is performed to show that a similar design could realistically be adapted to the MCM process with possible performance enhancement.

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Last but not least, thanks to my family and friends for your constant support.

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Publication of this thesis does not constitute approval by Draper or the sponsoring agency of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas.

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James Noonan

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Chapter 1

Introduction

Progress in the field of portable communication devices has resulted in a demand for small and efficient electronics. Modern communication devices like cellular phones require electronics for a wide variety of functions, from digital computation to transmission and reception of radio frequency (RF) signals. Such a variety of functions calls for a variety of integrated circuits, fabricated in different processes with different materials. These electronics must all be incorporated with larger elements like a battery and an antenna into a small, hand-held device. Combining separate packaged chips can quickly take up a lot of space. On the other hand, fabricating all of these electronics onto a single integrated circuit using a single process and material will result in sub-optimal performance from components better suited to other processes.

Multi-chip module (MCM) technology provides a solution to the problem of incorporating a variety of electronics into a small volume. In an MCM fabrication process, bare dice are combined onto a common substrate and interconnected, allowing a variety of functional blocks to exist on a single chip. In addition to occupying a smaller area, the parasitic effects associated with the packaging of chips and discrete components are reduced.

Another concern in portable communication devices is power consumption. High power consumption results in large batteries and/or short battery lifetimes. Efficient electronics maximize the performance of a device given the constraints of a battery. The circuit within such a device that typically consumes the most power (sometimes

as much as half of the DC power supplied) is the RF power amplifier, which converts DC power from the battery into the RF signal that is transmitted through an antenna. Maximizing the efficiency of the power amplifier can allow for reduction in battery size, prolonged battery life, increased signal strength, or a combination of the three. Efficient amplifiers also generate less heat, increasing device lifetime and reliability.

The work described in this thesis was completed at Draper Laboratory. Draper is currently doing research into both MCM's and high efficiency power amplifiers. This thesis combines these two research areas by analyzing issues arising in the design of high efficiency RF power amplifiers for an MCM process.

1.1 Multi-Chip Modules

As stated before, the idea behind MCMs is to attach and interconnect multiple bare dice and passive components onto a single substrate, allowing IC's fabricated in different processes to exist on the same compact circuit. For example, in a cellular phone, one must combine digital electronics with high power RF electronics in a small space. Ideally, one might want to use a CMOS process on a silicon substrate for the digital electronics while using a GaAs power FET for RF amplification. Using separate packaged parts for each of these functions quickly takes up precious space inside the device. MCM technology allows these circuits to be combined into a small area while preserving the functional benefits derived from the different fabrication processes.

1.1.1 The Draper MCM-D Process

The specific process this work will look at is Draper Laboratory's MCM-D (Multi-Chip Module-Deposited) process. This process uses a 25 mil thick alumina substrate with multiple Kapton film layers above it. The dice are attached to the substrate and contained within the lowest Kapton layer, which is 6 mils thick. Interconnects are done in the layers above, each of which consists of a 1 mil thick Kapton film and .5 mils of adhesive. The copper metalization is approximately .2 mils thick.

A significant challenge posed by the integration of RF power devices into MCMs is

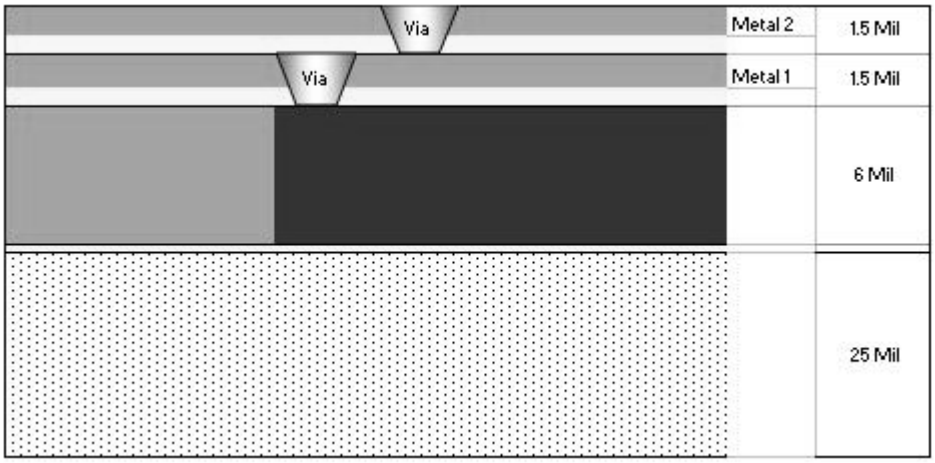

Figure 1-1: MCM-D Cross Section

the management of heat. Incorporating a variety of devices into a small volume makes it difficult to conduct heat away from the devices. Heat can have a significant effect on the electrical performance and operational lifetime of a device. Temperature variations can also cause different materials to physically expand or contract by different amounts. These variations can easily cause structural damage in an MCM, where a variety of materials are housed in close proximity. Chapter 3 of this thesis explores some of the thermal issues that will arise in incorporating RF electronics in an MCM.

One of the main potential benefits of MCM technology is the reduction of the parasitic effects associated with die connections. In packaged devices, the die is typically connected to leads on a package through thin bondwires which can introduce parasitic inductance and resistance. The package and the leads themselves can also introduce capacitive parasitic effects. These parasitic effects can be particularly problematic at RF frequencies. MCM technology offers the potential to bring interconnects close to the bare die for low impedance connections. Chapter 4 of this thesis will use simulations to show the reduction in parasitic effects that can be achieved in an MCM over a surface mount package.

At high frequencies, the behavior of an RF network is largely defined by its physical dimensions and by the dielectric properties of the materials it resides on. When talking about incorporating RF electronics into a process, it is extremely important to

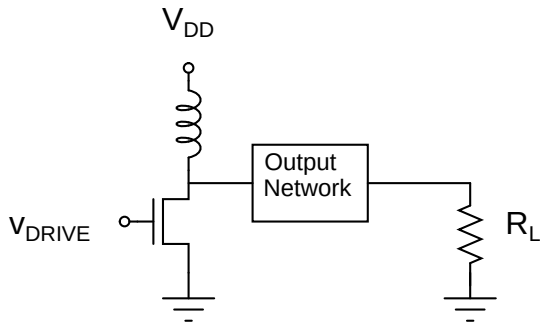

Figure 1-2: General RF Power Amplifier Topology

understand the RF characteristics that transmission lines will have when fabricated in the process. Chapter 5 of this thesis will explore the electrical properties of various transmission line structures achievable in the MCM process.

In chapter 2, we will identify a transistor suitable for use in an MCM high efficiency power amplifier design to provide a realistic framework for the analyses mentioned above. Chapter 6 will detail the design of a PCB high efficiency power amplifier using this transistor in order to demonstrate a design procedure and evaluate this transistor for use in high efficiency amplifiers. Chapter 7 will describe the testing of this design and give analysis of the results. Chapter 8 will conclude the thesis.

1.2 RF Power Amplifiers

We will now take a look at RF power amplifiers and how they can be designed for high efficiency operation.

1.2.1 Topologies

An RF power amplifier is a circuit that converts DC power into RF power. In a transmitter, the PA amplifies the outgoing signal to a level sufficient to drive the transmitting antenna. The most common RF power amplifier topology is given in Figure 1-2. The topology consists of a single active device. The drain of the transistor is coupled to the DC power supply through a large inductor (or RF "choke") that

sets the drain bias but acts as an open circuit at high frequencies. The input signal is connected to the gate through a passive impedance network, which provides an impedance match at the fundamental drive frequency and can also provide harmonic impedance characteristics. The drain of the transistor is connected to the load through an output impedance network.

Most RF power amplifiers fit into one of six common classes: A,B,C,D,E, or F. The distinctions between these classes lie primarily in the biasing conditions of the transistor and the design of the output network that couples the drain to the load. Each class has its own strengths and weaknesses, and choosing a class amounts to compromising between various power amplifier figures of merit, which include gain, linearity, and efficiency. For example, Class A and B power amplifiers offer high gain and a wide linear range, but are inefficient. On the other hand, class E and F power amplifiers can achieve high efficiency but do not provide linear amplification. In this application we are mainly concerned with efficiency, so we will look exclusively at Class E and Class F power amplifiers.

We will use Power Added Efficiency (PAE) as our measure of efficiency. PAE is defined as the ratio between the output power minus the RF drive power and the total DC power dissipated from the supply:

$$PAE = \frac{P_{out} - P_{RF}}{P_{DC}} \tag{1.1}$$

For a fixed power gain, the problem of maximizing PAE amounts to minimizing the amount of power dissipated in the transistor, thereby maximizing the amount of power delivered to the load. The power dissipated in the transistor is primarily given by the product of the drain current I_D and the drain to source voltage V_{DS}. To maximize PAE, we want to minimize the amount of time during which the transistor simultaneously has a non-zero V_{DS} and I_D. We will now look at Class E and Class F power amplifiers to see how this is accomplished.

1.2.2 Class E Power Amplifiers

Class E power amplifiers are members of a class of amplifiers called "switching-mode" power amplifiers. The idea behind switching mode power amplifiers is to drive the transistor hard enough so that it acts like a switch (as opposed to a linear voltage dependent current source). An ideal switch will never simultaneously conduct current and have a voltage across it: while the switch is "on", it conducts current but is a short, so there is no voltage drop, and while the switch is "off", it conducts no current but can support a voltage. If the transistor operates like an ideal switch, the theoretical power dissipation at the drain will be zero.

In reality, transistors do not behave like ideal switches. In operating any transistor, there will be some non-zero switching time associated with charging parasitic capacitances. During these switching times, the transistor simultaneously drops a voltage and conducts current. If the switching time of the transistor is a significant portion of the RF signal period (which it often is at GHz frequencies), then significant power dissipation can occur.

The idea behind Class E amplification is to use an output impedance network at the drain of the transistor to shape the drain voltage and current waveforms to minimize overlap. Theoretical target curves for Class E operation are shown in Figure 1-3. The goal of the Class E design is to achieve a drain voltage waveform that has both zero value and zero slope when the transistor turns on. The zero slope condition assures that the drain voltage will be close to zero around the turn-on time of the transistor, so that even if the voltage and current waveforms overlap, power dissipation will be low. The cost of the increased efficiency encountered in Class E design comes with lowered power gain and increased harmonic distortion.

One possible lumped element topology for a Class E PA is given in Figure 1-4. Analysis and design equations for the Class E PA are given in [12].

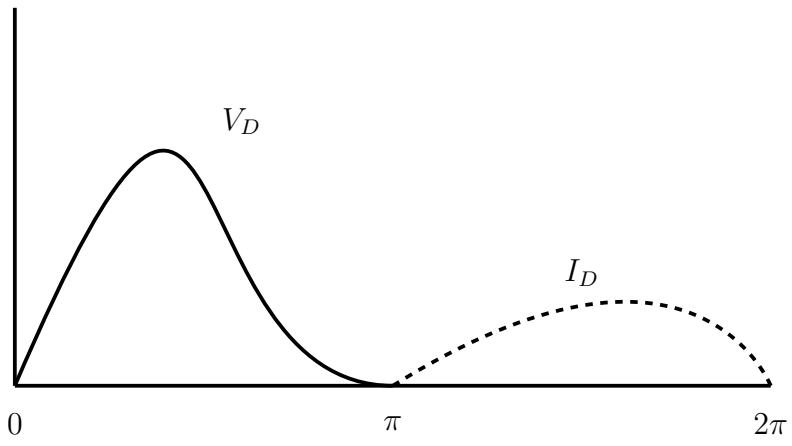

Figure 1-3: Class E Voltage and Current Waveforms

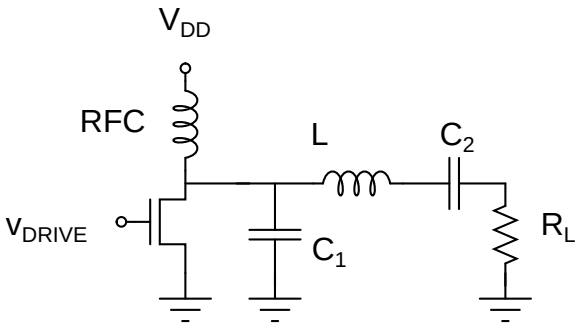

Figure 1-4: Lumped Element Class E Topology

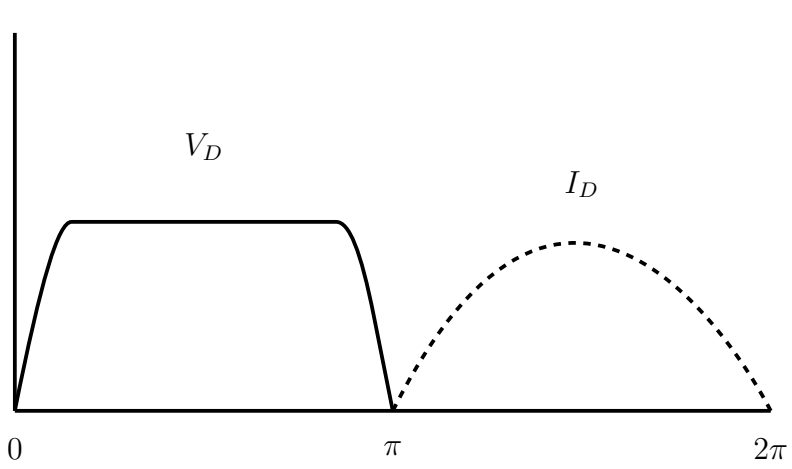

Figure 1-5: Class F Voltage and Current Waveforms

1.2.3 Class F Power Amplifiers

Class F amplifiers are another class of switching-mode amplifiers that use a passive output network to shape the drain voltage waveform. In this case, the goal is a drain voltage waveform that approaches a square wave and a drain current waveform that approaches a half sinusoid. Theoretical Class F waveforms are shown in Figure 1-5. An alternative approach, known as Inverse Class F, uses a square wave in current and a half sinusoid in voltage. Theoretically, these waveforms will not overlap in time, and assuming very large gain, we will approach 100% PAE. In practice, parasitic effects limit our ability to produce ideal waveforms.

A square wave at frequency ω_0 contains the fundamental frequency and all odd harmonics of the fundamental. In order to make the drain voltage approach a square wave, the output impedance network presents a high impedance to all of the odd harmonics and a low impedance to all of the even harmonics. One possible Class F topology is given in Figure 1-6 [7]. In this circuit, the parallel LC tank is tuned to the fundamental frequency ω_0, with a Q large enough to present an effective short at all multiples of ω_0. The key to presenting the proper harmonic terminations for Class F operation lies in the quarter wavelength transmission line connecting the transistor drain to the LC tank. A quarter wavelength transmission line has an input impedance

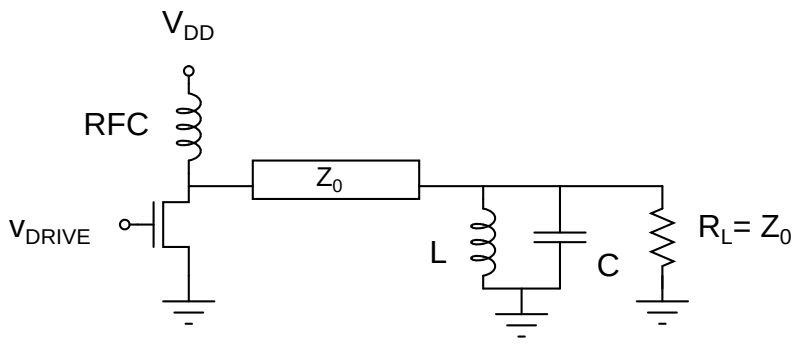

Figure 1-6: Class F Topology Using Resonant Tank and $\lambda/4$ Line

proportional to the reciprocal of its load impedance:

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{1.2}$$

If the transmission line's characteristic impedance is matched to the load impedance, the drain will see the load impedance at the fundamental frequency. At even harmonic frequencies, the transmission line is a multiple of a half wavelength, so the drain will simply see the short circuit presented by the LC tank at the end of the transmission line. At odd harmonic frequencies, the transmission line is an odd multiple of a quarter wavelength, so the drain sees the reciprocal of the short circuit presented by the LC tank, or an open circuit. Thus, we present all odd harmonics with a high impedance and all even harmonics with a low impedance, producing the desired square wave in voltage at the drain of the transistor.

The topology in Figure 1-6 provides an extremely simple and elegant theoretical solution to the Class F problem. Unfortunately parasitic effects make the design impractical at the frequencies of interest. The parasitic inductance at the drain of the transistor will make the length of the quarter wave line look different at different frequencies. Moreover, the design gives no flexibility in tuning the individual harmonic impedances once the impedance at the fundamental is set. In practice, transmission line networks with harmonic traps at some small number of harmonic frequencies are used to get close to a square wave in voltage. Such a design will be described in detail in Chapter 6.

Chapter 2

Transistor Selection

There are currently a wide variety of RF power transistors available that are suitable for use in high efficiency power amplifiers. The choice of transistor for a given design impacts a broad variety of circuit and system level parameters. The electrical properties of the transistor will determine what power amplifier topologies will be possible or effective. The bias conditions required will affect not only the performance of the amplifier, but also what external circuitry is required to provide those bias conditions. Dimensions of the die and placement of the bond pads will dictate how connections can be made to the die and what parasitic effects those connections will have. Thermal properties of the die will affect heat management needs.

In order to provide a realistic framework for looking at the issues stated above, we must first identify a transistor that is suitable for our design.

2.1 RF Power Transistors

Most popular RF power transistors are fabricated using compound semiconductors like GaAs or SiGe. These materials offer higher electron mobility than silicon and hence better high frequency performance. One of the first popular RF power transistors was the GaAs metal-semiconductor field effect transistor (MESFET) [1]. The primary difference between a MESFET and a standard MOSFET is the use of a Schottky gate junction instead of a standard MOS structure. The Schottky junction serves to

lower the input capacitance, making the device easier to drive at high frequencies. An improvement on the MESFET structure came with the pseudomorphic high-electron-mobility transistor (pHEMT). The pHEMT uses an AlGaAs/GaAs heterojunction in the gate to offer better high frequency performance than the MESFET [9]. Both types of devices in their standard forms are "depletion mode" devices, meaning they require a negative gate bias to operate as amplifiers.

The need for a negative gate bias to operate is a serious setback when one is designing for a small battery operated device. There are two main reasons for this. Firstly, in order to provide a negative DC voltage to the gate, one needs to add an additional circuit to the system such as a charge pump or a DC-DC converter, which will take up extra space. The second problem posed by a negative gate bias concerns sequencing the application of bias voltages to the gate and drain. With zero voltage applied to the gate, a depletion mode device is biased in saturation. If the drain power supply is applied before the negative gate supply, the transistor will conduct its saturation current, effectively shorting the power supply to ground. To avoid damaging the transistor or other circuit components, one has to ensure that the negative gate bias will be applied before the drain bias when the device is turned on. Extra circuitry is usually required to accomplish such sequencing.

As a result of the increased circuit area and system complexity imposed by depletion mode devices, there has been much interest in developing RF power transistors that operate with a positive gate bias. Since Draper began looking into high efficiency power amplifier design, a couple of promising new types of transistors have become available as off the shelf parts: enhancement-mode pHEMTs (E-pHEMTs) and heterojunction bipolar transistors (HBTs).

2.1.1 Enhancement-Mode pHEMTs

Enhancement-mode pHEMTs (E-pHEMTS) are pHEMTs that, through careful control of semiconductor layer thickness and composition, do not conduct current with a V_{GS} of zero and thus can be operated with a single positive supply. E-pHEMTs have only recently begun to become available as discrete packaged components. Most E-pHEMT

devices described in the literature operate at low supply voltages, which demand high currents and can make achieving high PAE a challenge. However, some highly efficiency E-pHEMTs have been reported. A 3V E-pHEMT running at 65% PAE at 33 dBm and 1.8 GHz is reported in [14], and a 2.4V E-pHEMT running at 61% PAE at 32 dBm output power and 1.9 GHz is reported in [2].

2.1.2 Heterojunction Bipolar Transistors

Most HBTs are made using GaAs, though more recently some have been made using SiGe. HBTs operate in much the same way as bipolar junction transistors. Instead of using doping to form a standard pn junction, an AlGaAs/GaAs heterojunction is used. This allows for heavy doping in the base, resulting in low base resistance and improved high frequency operation [9]. As with E-pHEMTS, some promising results have been reported for efficient operation of HBTs. A SiGeC HBT running at 72% PAE at .9 GHz with 1W output power is reported in [10], and a GaAs HBT running at 72% PAE at 12 GHz with 1W output is reported in [11].

2.2 Transistor Selection

In the search for a suitable transistor, the following were identified as important criteria:

1. Single supply operation
2. 30 dBm output capability at 2.3 GHz
3. Efficient operation
4. Availability of a large signal model
5. Available as discrete packaged device

One device that was considered was the SGA-9289, a SiGe HBT from Sirenza Microdevices. The device meets the single supply criteria. The data sheet for this part reported a 1dB gain compression point (P1dB) of 28 dBm around the frequencies of

interest. Because switching mode amplifiers are often driven past 1dB of gain compression, it is feasible that this device could achieve the desired 30 dBm output power specification.

Unfortunately there was no non-linear model for the device available at the time this work was completed. Since having devices modeled was beyond the scope of this project, completing a design with this device would have been difficult. Beyond the lack of models, there were other characteristics of the device that made it less than ideal. The power gain reported on the data sheet at 1960 MHz was only 10.8 dB. In our application, we would drive the device hard enough for it to exhibit switching behavior, so we would expect our gain to be lower than this figure. A power gain of 8 or 9 dB would be relatively low and would have a negative effect on PAE. For example, if the amp achieved 8 dB of gain at 30 dBm output power, even if we achieved a drain efficiency (defined as $\eta = P_{out}/P_{DC}$) of 70%, our PAE would only be 59% as a result of our low power gain. The device also has a relatively low supply voltage (3-5V). A low supply voltage requires a high drain current, which will tend to increase power dissipation in the transistor and the output network and lower efficiency. While this device's data sheet does not include data on efficiency, SiGe HBTs are known to be less efficienct than GaAs HBTs [9].

A more promising device found was the ATF511P8, an enhancement-mode pHEMT from Agilent Technologies. Agilent provides a large signal model of the device for use in their Advanced Design System (ADS) software, which is the RF circuit simulator used at Draper. At 2 GHz, the data sheet reports a P1dB of 30 dBm and a gain of 14.8 dB, both of which are high enough for our application. Perhaps most promising of all is the PAE spec of 69%, which is an extremely high figure. All of these criteria made the 511P8 an excellent candidate for the design. Before deciding on this device, however, there were some important issues relating to supply voltage that needed to be addressed.

Agilent offers a similar device, the ATF501P8, which it released as an improvement upon the AFT511P8, claiming the newer die had better thermal properties. In initial simulations, the device model for the 501P8 performed slightly better than the model

for the 511P8. However, the ATF501P8 reports slightly lower PAE and P1dB on its data sheet. Since it was unclear which device would ultimately perform better, both are considered in this work.

2.2.1 Supply Voltage

While the 511P8 is rated to support a maximum DC V_{DS} of 7 volts, the true upper limit on the power supply for use in a Class E or Class F amplifier would be set by the maximum DC V_{DG} tolerated, which is 5 volts. V_{DG} sets the upper bound because our gate bias will have to be near the pinch-off voltage (V_P) to achieve switching-mode operation. V_P is the voltage at which the transistor effectively stops conducting current. Biasing the gate near V_P ensures that the device is truly turned "off" during the negative half cycle of the driving sinusoid and that very little current is conducted. For this device, V_P is around .3V, so our drain supply is limited to being at most 5V above .3V, or around 5.3V.

Another concern when deciding what maximum supply voltage the device can tolerate is the V_{DG} breakdown voltage, or the maximum voltage that can exist across the gate and drain terminals during the RF period. The data sheet does not provide this specification for the device, and Agilent was unable to provide it when contacted. The maximum DC V_{DG} spec of 5V suggests that the drain-gate junction should be able to support at least 10V with RF applied, but it is unclear what maximum voltage the junction can support for safe operation. This is a specification that would have to be watched closely when executing a design.

Beyond the question of what supply voltages the device can tolerate, there are also some system level design requirements imposed by the supply voltage. As stated earlier, one of the goals of Draper's high efficiency amplifier research is to develop efficient technology for use in battery operated communication devices. In such devices, the power amplifier can not be viewed in isolation. Having an efficient power amplifier is all for naught if a DC supply voltage of sufficient power cannot be consistently and efficiently supplied. It was therefore desirable to identify a DC to DC conversion solution that would allow the power amplifier to operate in spite of voltage variations

over the lifetime of a battery. In a case where efficiency is a concern, the most common solutions are "buck" and "boost" switching regulators. Buck converters provide a DC output voltage that is lower than their DC input, requiring that the input voltage always remain higher than the DC output. Boost converters do the opposite, requiring the input to stay below the DC output.

The batteries that Draper has worked with in past high efficiency power amplifier designs have an output voltage ranging from 6.8 down to 3.4 volts over the lifetime of the battery. In all cases a supply of above 6.8 volts was used and generated by a single boost converter. Because we would be limited to a 5V maximum supply in this case, a single boost converter would no longer be an option. The two options that remained were using a single buck converter to generate a supply of around 3V, or using a buck and boost converter in series to generate a voltage between 3 and 5 volts. In order to compare these options, a survey of currently available power converters was done.

The most recent high efficiency power amplifier design executed at Draper used an LM 2731 boost converter to supply 7.1V at 400mA. The data sheet for this part suggests that it would run at about 85% efficiency under these conditions. The best option found for a single 3V buck converter was the LTC 1879 from Linear Technology. The data sheet indicates that this part should run at around 88% efficiency when supplying 3V at around 600mA. For a 3-5 volt output solution, Maxim offers the MAX711, a buck-boost converter that supplies an adjustable output voltage up to 5.5V with an input voltage range from 1.8 to 11V. This part runs at around 83% efficiency at the power level of interest.

Thus, to operate between 3 and 5V we would have to sacrifice around 2% efficiency in the DC-DC converter over the single boost converter case. Operating below 3V would actually result in a 3% gain in converter efficiency. However, such a low voltage supply would require high currents to supply enough output power, making high efficiency more of a challenge. Therefore, the 3-5V solution was viewed more favorably. It was ultimately decided that the 2% sacrifice in converter efficiency resulting from the low drain supply of the ATF511P8 would be worth the system level benefits of using a single supply device, and this device was chosen as the focus of this thesis.

2.2.2 ATF511P8 Device Model

Some initial simulations were performed to see if the device model could achieve as high performance as the specs on the data sheet. The data sheet gave the following data for a bias of $V_D = 4.5$V, $I_D = 200$mA:

Freq (GHz)	**Gamma Source Mag, Ang**	**Gamma Load Mag, Ang**	**Gain (dB)**	**P1dB (dBm)**	**PAE (%)**
2.0	.872, -171	.683, -179	15.06	30.12	66.8%
2.4	.893, -162	.715, -174	14.03	29.90	64.5%

It was attempted to reproduce these results using the device model. The impedances listed were presented to the drain and gate of the transistor with ideal numerical impedances. Bias voltages were applied to the drain and gate using ideal RF chokes. Since no mention of harmonic terminations was made in the data sheet, 2nd-4th harmonic impedances were optimized over PAE. The following results were obtained:

Freq (GHz)	**Gain (dB)**	**P1dB (dBm)**	**PAE (%)**
2.0	14	26	46.9%
2.4	12	26	47.2%

In an attempt to produce better results, the impedances at the fundamental frequencies were then optimized over PAE, yielding:

Freq (GHz)	**Gain (dB)**	**P1dB (dBm)**	**PAE (%)**
2.0	13.7	26	50.7%
2.4	12	26	52.87%

Since the exact details of the test setup that yielded the data sheet results were not known, it is not surprising that the results could not be duplicated exactly. Nevertheless, the transistor model operated with significantly lower P1dB and PAE than was suggested on the data sheet. Agilent was contacted about this, and they said that,

due to the way the model was created, the PAE results on the data sheet may not be achievable in simulation. This would have to be kept in mind when using the model to design a high efficiency amplifier.

Chapter 3

MCM Heat Conduction for RF Circuits

In the design of RF power circuits, heat management is always an important concern. Semiconductor devices like FETs typically have some maximum channel temperature above which the device fails. Even if this temperature is never exceeded, the mean time to failure (MTTF) of a device typically drops exponentially with temperature, so devices are more reliable for longer periods of time at lower temperatures. Heat can also pose structural problems for a circuit. Different materials with different thermal coefficients of expansion (TCE) will swell and shrink by different amounts across different temperatures. High temperatures in a circuit can therefore cause structural deformation resulting in broken connections or short circuits.

Aside from conserving energy from the power source, one of the main benefits of high efficiency power amplifiers is that less power is dissipated as heat in the transistor. But even highly efficient power amplifiers can still generate a significant amount of heat. A 1 Watt power amplifier running at an impressive 70% PAE will still dissipate 430 mW as heat.

When shrinking down electronics into a small volume, heat becomes even more of a challenge. Small power amplifiers still have to dissipate significant amounts of heat, but there is less material to spread the heat into. Heat generation has an increased effect on neighboring components and the system as a whole. Moreover, in the MCM

fabrication process, which has strict design rules, one is limited in the types of materials one can choose and the placement of those materials for the conduction of heat. Even if heat can be conducted away from the device, if the device runs at a high temperature, a large heat sink will be required outside of the module to adequately conduct the heat to the ambient. The heatsink could potentially nullify any volumetric gains from reducing the size of the electronics.

3.1 Heat Flow in an MCM

Before looking at thermal issues in an MCM, we will first look at how heat is managed in a conventional surface mount board to provide a mode of comparison. In the case of the ATF501P8 power transistor, the die sits in the package on top of a piece of metal that acts as both the electrical and thermal ground. Most of the heat is generated in the channel at the top of the die, and it must travel through the die to the metal ground. The metal ground is directly connected to ground on the board, and from here the designer can attach heat sinks with large surface areas to absorb heat. Thus, as soon as the heat has passed out of the bottom of the die, it has a low thermal conductivity path out to the heatsinking structure.

This is not the case in an MCM. Figure 3-1 shows the path that heat takes from the channel in the transistor out to the heatsink. In this case, the GaAs die is attached to a 25 mil thick alumina substrate with a thin layer of eutectic die attach solder. The 25 mils of alumina, which has a relatively low thermal conductivity, adds significant thermal resistance to the heat conduction path. Table 3.1 lists thermal conductivities for some of the materials used in and around MCMs.

We will now look at how much of a problem is posed by the presence of the alumina substrate in the thermal path. In order to do so we will use the thermal properties of the ATF501P8 die. The die is rated for a maximum channel temperature of 150°C. The channel to board thermal resistance (θ_{ch_b}) is 23°C/W, meaning for every Watt dissipated in the transistor there will be a difference of 23°C between the channel temperature and the mounting surface. We will make the assumption that the entire

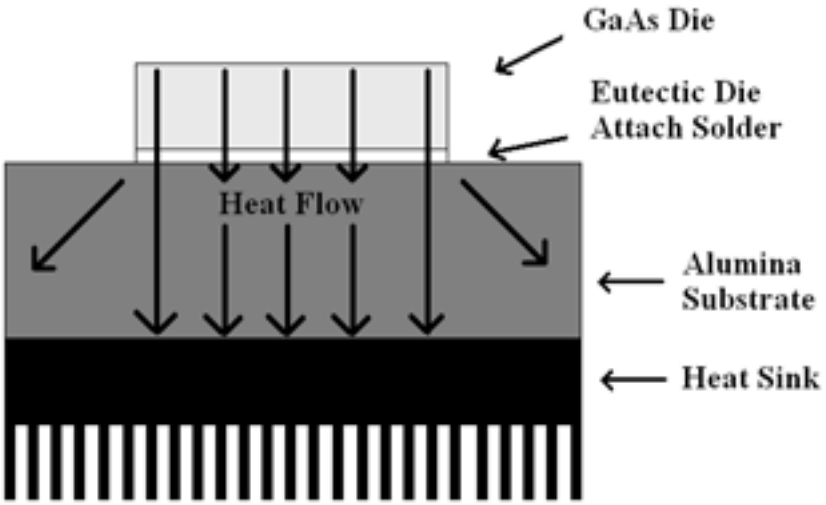

Figure 3-1: Heat Flow in an MCM

Table 3.1: Thermal Conductivities

Material	**Thermal Conductivity (W/in°C)**
Copper	9.9
Silicon	3.8
Eutectic Solder	1.27
GaAs	1.1
Alumina	.7
Air	.007

temperature drop occurs across the die and not the thermally conductive metal connecting the die to the bottom of the package. X-rays revealed the die area to be 36.6 mil x 20.9 mil.

To analyze the change in temperature across the substrate, we will use the following standard relationship:

$$\Delta T = Q\frac{L}{A\kappa} \tag{3.1}$$

Here ΔT is the change in temperature, Q is the heat flow in Watts, L is the length of the conduction path, A is the cross sectional area of the conduction path, and κ is the coefficient of thermal conductivity, with units of W/in°C.

If we assume that we have a 1 Watt amplifier running at 50% efficiency, then the transistor will have to dissipate 1 Watt of power as heat. Assuming heat flow occurs straight downward (ie, the cross sectional area of the conduction path is just the area of the die), we get a change in temperature across the alumina substrate of 46.7°C. Under the same assumptions, the eutectic solder will add about 1°C for a 1 mil layer. At 1 Watt, we get a 23°C temperature difference from the channel to the bottom of the transistor die resulting from θ_{ch_b}. Thus, we have a total temperature difference of just over 70°C from the channel to the outside of the module. If we assume our amplifier is specified to run at a 70°C ambient, as is common in military applications, then our junction temperature will rise to just above 140°C, which is close to the maximum channel temperature for the device. This is assuming a perfect heatsink is placed outside the module, with zero rise above the ambient. In reality, there could be a drop of several degrees across the heatsink, and our channel temperature could be even higher.

Aside from risking exceeding the maximum channel temperature, operating at such a high temperature will dramatically reduce the reliability of the device. Figure 3-2 shows MTTF of the ATF501P8 as a function of temperature. These data were provided in the reliability data sheet for the device. The graph shows an exponential drop in MTTF with increasing temperature. At 140°C, the MTTF is around $3.2 \cdot 10^5$ hours, or 37 years, and we are near the bottom of the curve. With a 10°C drop across the

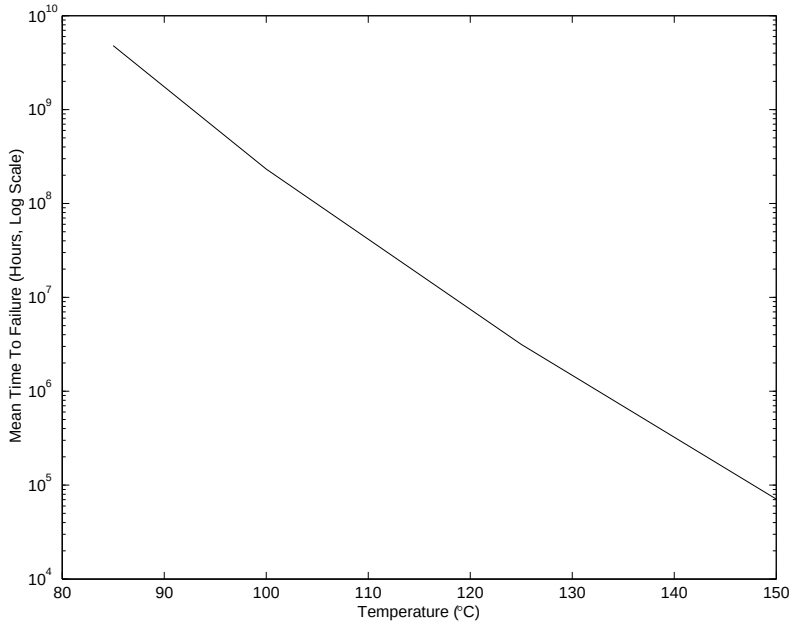

Figure 3-2: Log(Mean Time to Failure) vs. Temperature

heatsink, the channel temperature rises to its maximum allowed value of 150°C, with a MTTF of 71,000 hours, or 8 years. The data suggest that a much longer MTTF is achievable.

In our analysis we have assumed that all of our heat flows straight downward, when in reality some heat will flow laterally outward, effectively reducing the thermal resistance of the substrate. Thus, our assessment of the channel temperature is probably pessimistically high. Nonetheless, our analysis suggests that to operate the device reliably for a long period of time, a more effective heat conduction solution is required.

3.2 Thermal Vias

A common cooling solution for MCMs described in the literature is the use of thermal vias [6], [4] . The idea behind thermal vias is to drill holes in the substrate below the die and fill them with a thermally conductive material in order to reduce the thermal resistance between the die and the ambient. Figure 3-3 shows placement of the vias. Materials used for thermal vias are usually compound metals. In addition to

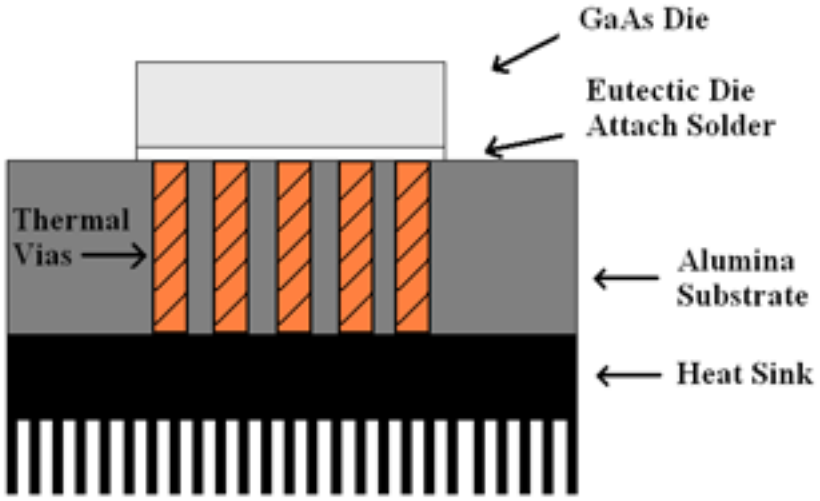

Figure 3-3: Placement of Thermal Vias in an MCM

Table 3.2: Material Properties

Material	**Thermal Conductivity** W/in°C	**TCE** ppm/°C
CuW/15-85	4.57	7.0
CuW/10-90	5.31	6.5
AlSiC	4.57	6.7
CuMo/15-85	4.67	6.6
Silvar-K	2.97	7.0
Alumina	.7	6.9
GaAs	1.1	6.5

high thermal conductivity, it is essential that thermal vias have a similar TCE as the substrate and the transistor. If the TCEs are unmatched, damage could be done to the substrate or device with large swings in temperature. This is especially true with thin microwave devices made out of GaAs, which is very brittle. Some common alloys used in thermal vias, along with thermal conduction coefficients and TCEs are shown in table 3.2.

With a TCE of 7 ppm/°C and a thermal conductivity of 4.57 W/in°C, the 15% copper/85% tungsten alloy provides the best compromise between high thermal conductivity and a match to the thermal coefficients of expansion of alumina (6.9 ppm/°C)

and GaAs (6.5 ppm/°C).

In order to estimate how effective thermal vias would be in lowering the thermal resistance of the conduction path in the MCM, we will use the analysis in [5]. In this work, two methods for modeling the effect of thermal vias in an MCM substrate were compared. The best agreement with experimental results were obtained by modeling the substrate containing the thermal vias as a single material with an adjusted thermal conductivity. The thermal conductivity is adjusted according to the following equation:

$$\lambda_T = \frac{\lambda_1(A - B) + \lambda_2}{A} \tag{3.2}$$

where λ_1 is the substrate thermal conductivity, λ_2 is the via material thermal conductivity, A is the cross sectional area of the substrate below the die, B is the total cross sectional area of the vias, and λ_T is the adjusted thermal conductivity. The equation essentially states that the effective thermal conductivity of the substrate/via combination is equal to the weighted sum of the individual conductivities of the two materials, where the weights are given by the percentage area occupied.

Using the thermal conductivity of Cu-W for λ_2, we can now model the change in temperature across the substrate as a function of the percentage of thermal via area under the die. The results are shown in Figure 3-4.

With a thermal via area of 0%, we see a temperature drop of 46.7°C as expected. The graph clearly shows diminishing returns on via area after around 25%. Indeed, more of a temperature drop is gained with the first 15% of via area than with the final 85%. With 10% via area, the change in temperature across the substrate has dropped from 46.7°C to 30.1°C, a change of 16.6 degrees. Assuming again a 70°C ambient, this places the channel temperature at 124.1°C instead of 140.7°C, a much safer margin for operating the device. The MTTF at 124.1°C is around 3.7x10^6 hours, or 424 years, which is more than a 10-fold increase above the MTTF at 140.7°C.

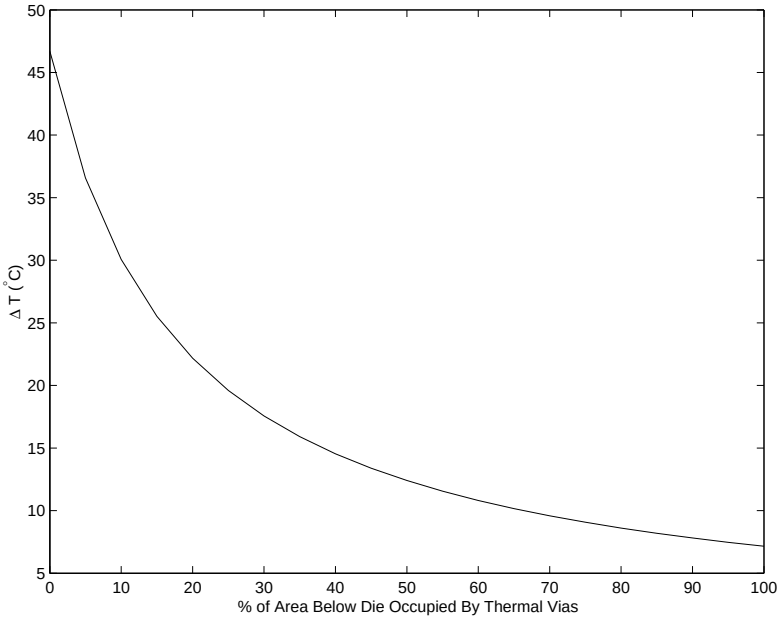

Figure 3-4: Change in Temperature Across Substrate vs. Thermal Via Area

3.2.1 Practical Considerations

The question remains as to what area ratios are achievable given the constraints of practical alumina substrate processing techniques. Current processes place lower limits on how small vias can be and how close to one another they can be placed. These dimensions are usually determined by the thickness of the substrate. A survey of design rules from MCM substrate vendors revealed a typical minimum hole diameter of $.6 \cdot T$, where T is the thickness of the substrate. Spacing between vias is typically on the order of the substrate thickness. At these dimensions, only one via can be placed below a 20.9 by 36.6 mil die. A single via with a diameter equal to the width of the die (which is greater than $.6 \cdot T$) will yield an area ratio of 45%. Applying this figure to the graph in Figure 3-4, we get a temperature drop across the substrate of only 13.4°C, yielding a MTTF of 7,440 years. This is of course only a rough approximation, since we are not modeling several vias below the die as the analysis in [5] assumes.

Another option is to use a non-circular via. In general there is a limitation on how sharp corners can be made when drilling into a substrate, since sharp corners tend to concentrate stresses in the material and cause structural problems. If we assume the

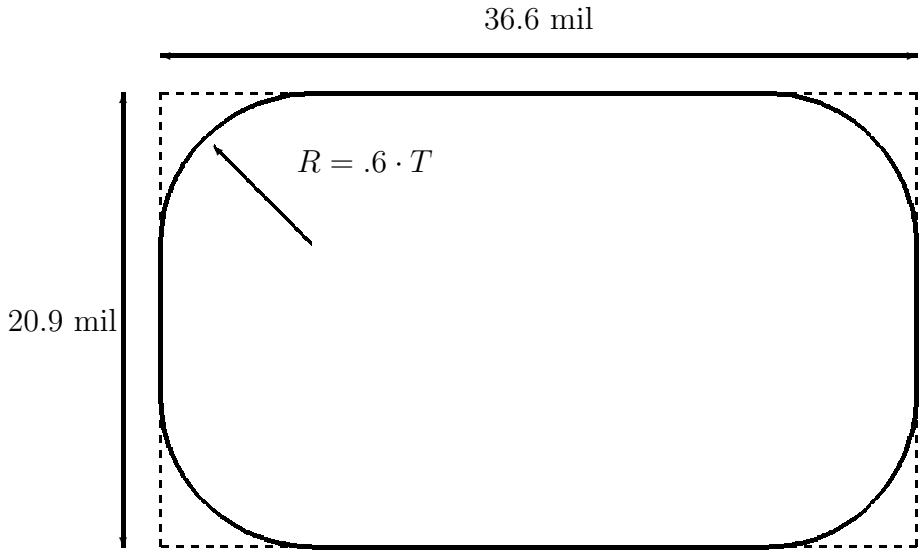

Figure 3-5: Copper Tungsten Area Under Die

minimum radius of a corner is given by the minimum via radius, then the shape in Figure 3-5 should be feasible. Using this shape, the copper tungsten will occupy 86% of the area under the die. According to the above analysis, the temperature across the substrate drops to 8.1°C for a MTTF of 22,000 years.

3.3 Summary

The analysis in this chapter is based upon some simplifying assumptions about how heat flows in an MCM substrate. Nonetheless our analysis suggests that thermal vias can be used to dramatically increase MTTF of the transistor in our amplifier.

Chapter 4

Parasitic Effects of Die Connections

As stated earlier, one of the promising features of MCM technology is the potential to reduce the parasitic effects of making connections to a bare die. In a surface mount package, connections are made between the die and the package leads with long, thin bondwires, which can have significant parasitic inductance and resistance. The package itself can also have capacitive effects. When operating at RF frequencies, these package parasitics can have a significant impact on circuit behavior.

MCM technology offers the potential to make low impedance connections close to the die. There are, however, constraints on how these connections can be made. For a given die and MCM process, the geometry of die connections will be determined by a broad range of parameters, such as location of bond pads on the die, dielectric layer thickness, via dimensions, via pad sizes, inter-layer via spacing, and the location of the ground plane. Thus, the claim that the MCM process allows for reduced parasitics requires justification.

In this chapter we will look at the parasitic effects of connecting to a transistor die, specifically the ATF501P8, using the Draper MCM-D process. This is accomplished using a 3-D electromagnetic (EM) fieldsolver called CST Microwave Studio. We will also look at parasitics in the ATF501P8 surface mount package to show that a reduction in parasitics can be achieved in the MCM.

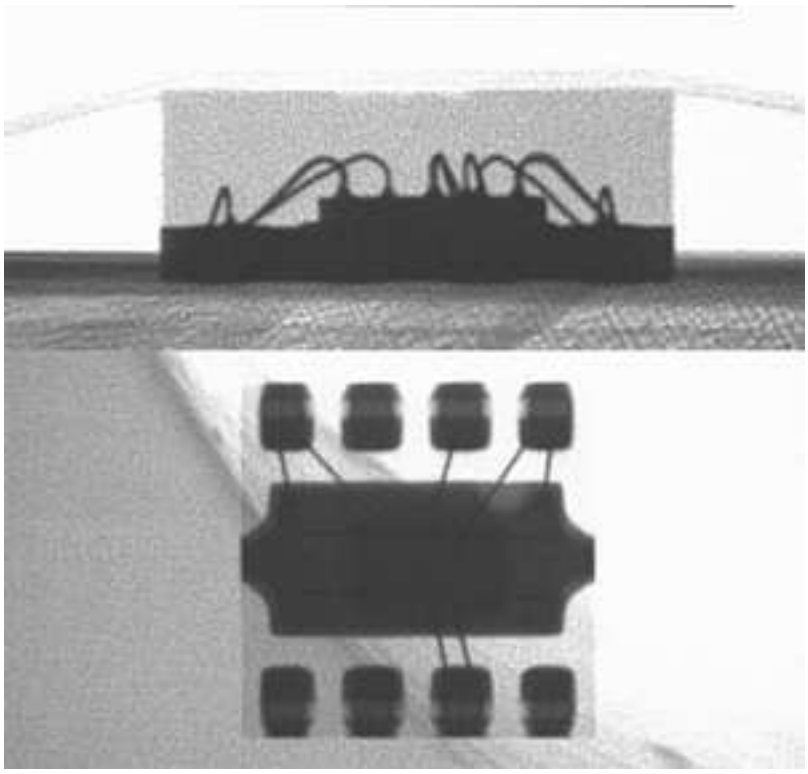

Figure 4-1: X-rays of the ATF501P8 Surface Mount Package

4.1 Parasitics of a Surface Mount Package

The ATF501P8 comes packaged in a 2mm x 2mm leadless plastic chip carrier (LPCC) package. X-rays were taken of the package to determine the internal bondwire geometry (Figure 4-1). The die sits on a metal block that serves as the source connection as well as the thermal ground. The x-rays revealed one bondwire connecting the gate to its external lead, two bondwires connecting the drain, and a total of six bondwires connecting the source to the two source leads on the package and to the thermal ground (some of which are not visible in the figure).

In order to simplify our analysis, we will focus on the gate connection, since it involves a single bondwire. The internal geometry suggests that there will be three main parasitic elements in a model of the gate connection. The bondwire connecting the lead to the die will present a series parasitic resistance and inductance, and a parallel capacitance will exist between the metal lead and the thermal ground. Figure 4-2

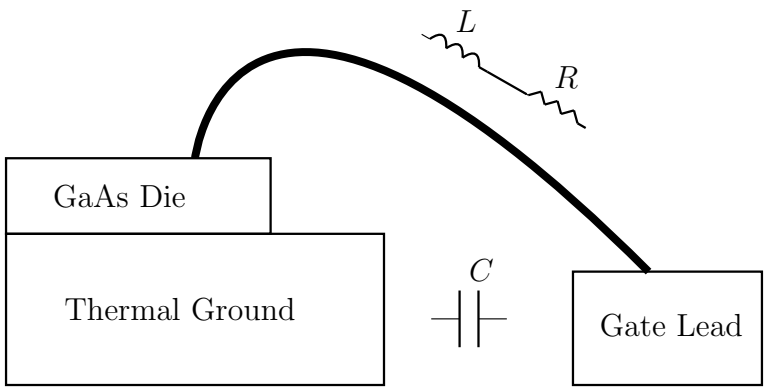

Figure 4-2: Parasitic Elements for a Bondwire Connection

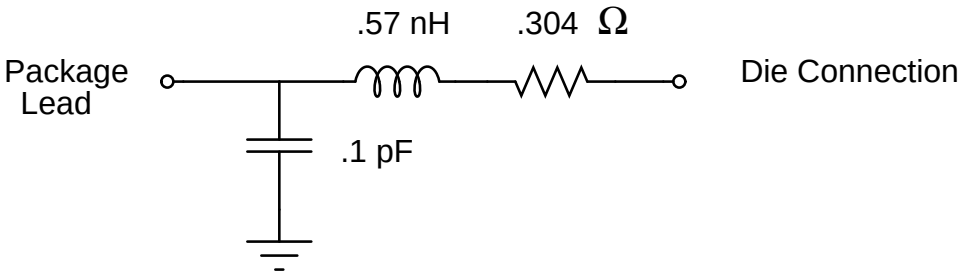

Figure 4-3: Agilent Model for the ATF501P8 Gate Connection

shows the placement of these elements. Agilent provides a lumped element model of the surface mount package with their large signal model of the ATF501P8. Their model of the gate connection, shown in Figure 4-3 agrees with the geometry in Figure 4-2 under the assumption that the thermal ground acts as RF ground, as it will in ours and most applications.

A model of the gate bondwire structure was created in CST Microwave Studio. The purpose of modeling the surface mount structure in the EM simulator was to see how well our simulations would agree with the model provided by Agilent and to provide a consistent mode of comparison within the EM simulator between bondwire structures and MCM structures. The geometry of the connection was constructed as it appeared in the x-rays. A dielectric constant of 3 was estimated for the plastic in the package.

The bondwire was constructed using Microwave Studio's bondwire model.

Two separate S-parameter simulations were performed. First, the impedance from the die to the gate lead was measured to yield the series impedance of the connection. The impedance from the thermal ground to the gate lead was then measured to find the shunt capacitance value. Lumped element models were then fit to these S-parameter measurements using an optimizer in ADS. A summary of the results is shown in the following table:

Model	L_{series}	R_{series}	C_{shunt}
Agilent	.552 nH	.304Ω	.10 pF
EM Simulation	.816 nH	.035Ω	.203 pF

The EM simulation predicted significantly lower series resistance and slightly larger series inductance and shunt capacitance. The results show reasonable agreement considering that the geometry of the structure could only be roughly approximated from the x-rays. In addition, the material properties of the bondwire and package modeled in Microwave Studio may not have perfectly matched those in the physical device.

4.2 Parasitics in the MCM

Now that we have closely analyzed parasitic effects in a surface mount package and demonstrated their measurement in the EM simulator, we will look at parasitics in the MCM process.

4.2.1 The Draper MCM-D Process

In the Draper MCM-D process, the die sits on the substrate in a 6 mil layer of Kapton film. Layers above the die consist of Kapton and adhesive and are 1.5 mils thick. Connections are made to the die with vias through the first Kapton layer. Thus, the shape and sizes of these vias are instrumental in determining parasitic effects of die connections.

However, these vias do not tell the whole story. From here parasitic effects are closely tied to the transmission line structure one is using in the circuit. The structure

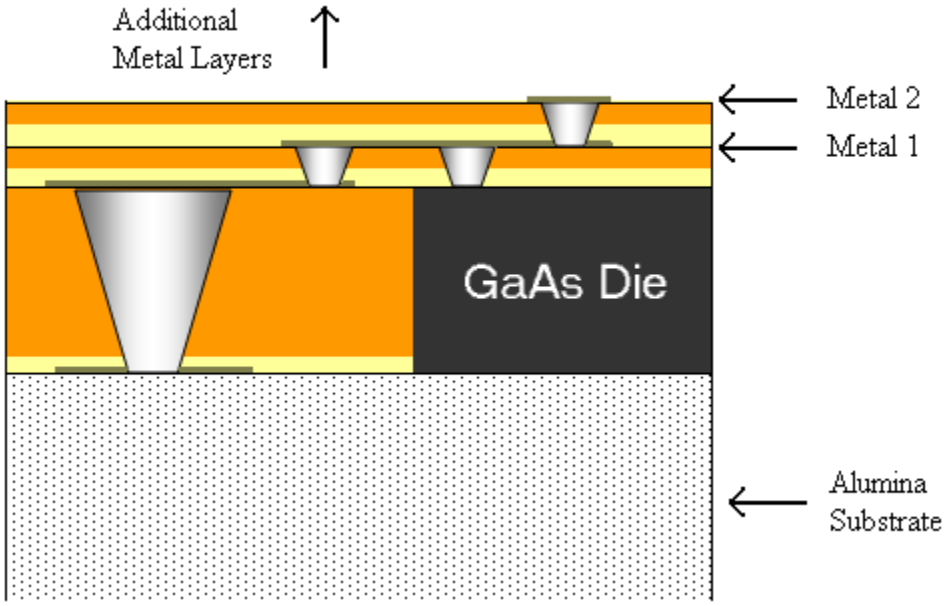

Figure 4-4: MCM Cross Section

determines what metal layer each terminal of the transistor must be connected to. If the transmission lines are going to reside on a metal layer 2 layers above the die, then the parasitic effects will include via connections through 2 layers. Moreover, the placement of these vias will be constrained by the process design rules, which put a lower limit on the distance between vias in adjacent layers. The parasitics will therefore include the metal required to connect the two spaced vias. The choice of structure also determines the placement of the ground plane(s), which affects parasitic capacitance.

Thus, we see that there are many variables in determining the parasitic effects of connecting to the die. In order to provide a broad analysis of the many configurations possible, we will analyze series parasitic elements separately from shunt capacitive elements. This will give a picture of parasitic effects that can be generalized to a broad variety of connection structures.

It should be noted that the current Draper MCM-D process does not currently support metalization on the substrate or filled vias through the 6 mil die layer. Nonetheless, because of the high dielectric constant of alumina, patterning on the substrate holds

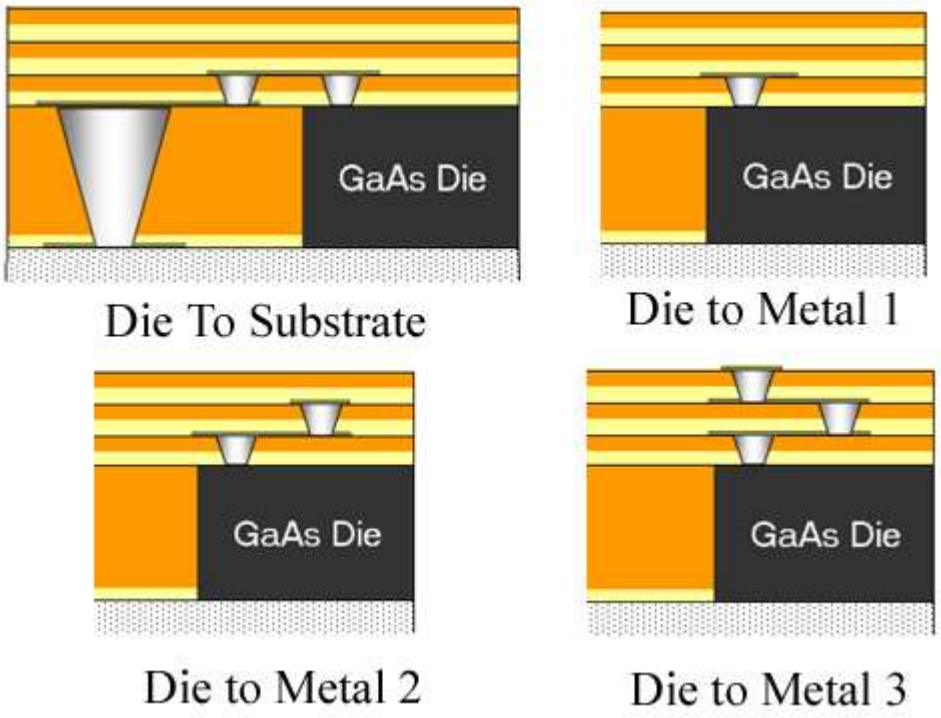

Figure 4-5: Die Connections to Various Layers

the potential for making compact transmission line structures in MCMs (see chapter 5). As a result it may be desirable to work this capability into the process in the future. This work will therefore include analysis of connections made from the die down to the substrate. Vias through the 6 mil layers were assumed to be proportional in aspect ratio to vias through the 1.5 mil layers, as were pad sizes for the vias.

4.2.2 Series Inductance and Resistance

In order to mestimate series parasitics in the MCM, structures were created in Microwave Studio connecting the die to various layers in the MCM, and the impedances of these connections were calculated. The geometries were determined by bond pad placement on the die observed in the x-rays as well as by the design rules of the MCM process. Figure 4-5 shows the different geometries tested. As was done with the bond-wire structures, inductance and resistance values were fit to S-parameter values using ADS. The results are shown in the following table:

Geometry	L_{series}	R_{series}
Die to Substrate	.395 nH	.054Ω
Die to Metal 1	.027 nH	.006Ω
Die to Metal 2	.050 nH	.030Ω
Die to Metal 3	.106 nH	.057Ω

The largest parasitic inductance occurs in connecting the die to the substrate. Even in this case, the series inductance is lower than the inductance in both the Agilent package model and the EM bondwire simulation. In the latter case it is more than 50% lower. When connecting to the metal 1 later, the parasitic inductance is only .027 nH, which is more than a factor of 10 lower than the inductance in either bondwire model.

4.2.3 Parallel Capacitance

The primary source of parallel capacitance in MCM die connections will be the metal pads on the vias (Figure 4-6). We can expect the parasitic capacitances to be roughly proportional to $\epsilon A/d$, where A is the total metal area, d is the the distance to the ground plane, and ϵ is the dielectric constant of the material separating the pad and ground. To provide an estimate of parallel capacitances, die connections were made to the substrate and the first two metal layers. For each structure, ground planes were placed on a variety of different layers. The impedances from the die connection to ground were then simulated and fit to capacitance values.

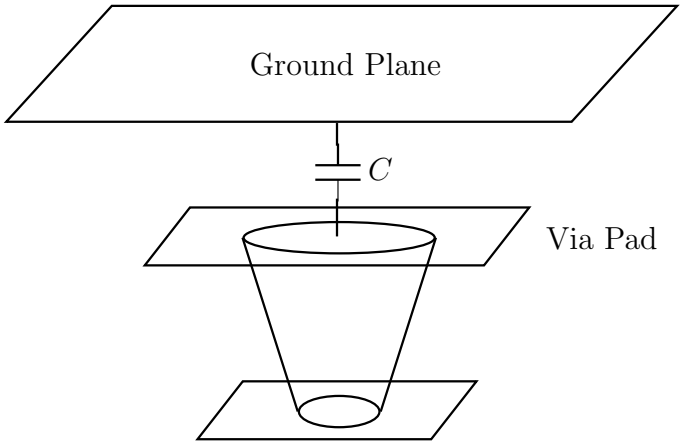

Figure 4-6: Parallel Capacitance Resulting From Via Pads

Connection Type	**Ground Plane Location**	C_{shunt}
Die to Substrate	Below Substrate	.143 pF
Die to Substrate	Metal 2	.156 pF
Die to Substrate	Metal 3	.125 pF
Die to Metal 1	Metal 2	.041 pF
Die to Metal 1	Metal 3	.032 pF
Die to Metal 1	On Substrate	.040 pF
Die to Metal 2	Metal 3	.050 pF

For the case of connecting the die to the substrate, our parasitic capacitances will be on the same order of magnitude as they are in the surface mount package. This is primarily the result of the large via pad required by the via through the 6 mil Kapton layer. Even though the ground plane is far away from the via pad when it is placed below the substrate, we still get a large C_{shunt} because of the high dielectric constant of alumina. If we are dealing with a transmission line structure that uses two ground planes, we have to add the capacitances resulting from each. For example, if we put transmission lines on the substrate and have ground planes below the substrate and on metal 2, our total C_{shunt} would be .156 pF + .143 pF = .299 pF. This C_{shunt} value is higher than that in either model of the surface mount package's gate connection.

In the case of connections to the metal layers above the die, the shunt capacitances are lower than in the bondwire case. Even though the metal connections are close to the ground planes, the smaller via pad areas result in lower capacitances than we see when connecting to the substrate.

4.3 Summary

Our simulations suggest that, when connecting the transistor to the upper metal layers, we can achieve significant reductions in series inductance and resistance and modest reductions in shunt capacitance over a surface mount package. When connecting to the substrate, we can still achieve a reduction in series inductance and resistance, but shunt capacitance remains unchanged and in some cases increased when compared to the surface mount package.

These results are quite positive for our application. Series inductance at the transistor terminals can be problematic, particularly in the source connection of a power amplifier. Inductance from the source to ground can provide a feedback path from output to input and cause instability. We have shown that we can reduce series inductance over a surface mount package regardless of where we put our ground plane, and that we can reduce it by over a factor of 10 if the ground plane is in one of the metal layers above the die.

In addition, the shunt capacitances are not necessarily a big problem. The gate and drain capacitances of an RF power transistor are generally pretty large. In the case of the ATF501P8, the die model gives a C_{gs} of 10.0pF. An additional .1-.3 pF will not have a significant effect. C_{gd} is 1.3 pF, but since the drain would likely be connected to a low impedance (as a result of the low drain supply), a modest increase in shunt capacitance here would be unlikely to impact circuit performance very much.

Chapter 5

Transmission Line Structures

At high frequencies, a circuit's behavior is largely determined by its physical dimensions and by the dielectric properties of the materials it is fabricated on. It is therefore important to understand what the electrical properties of different transmission line structures will be within the constraints of a given process. In this chapter we will use simulations to look at the electrical properties of several transmission line structures as they would be constructed in an MCM.

For each structure, we will try to answer two main questions:

1. What is the line width for a 50Ω line?

2. How long is a $\lambda/4$ line at 2.3 GHz?

Since our amplifier (and, in general, most RF circuits) will require 50Ω lines, the first question is a good indicator of whether a transmission line structure is practical or not. The minimum line width supported by the Draper MCM-D process is 2 mils. If 50Ω lines in a given structure are thinner than 2 mils, then the structure will be problematic for use in RF circuits. Even if the 50Ω line width is slightly larger than 2 mils, the line impedances will still be especially prone to errors resulting from line width tolerances. On the other hand, if line widths grow too large, transmission line behavior can become less predictable.

The second question will give us a feel for how compact we will be able to make transmission line networks. Many transmission line networks will use dimensions on

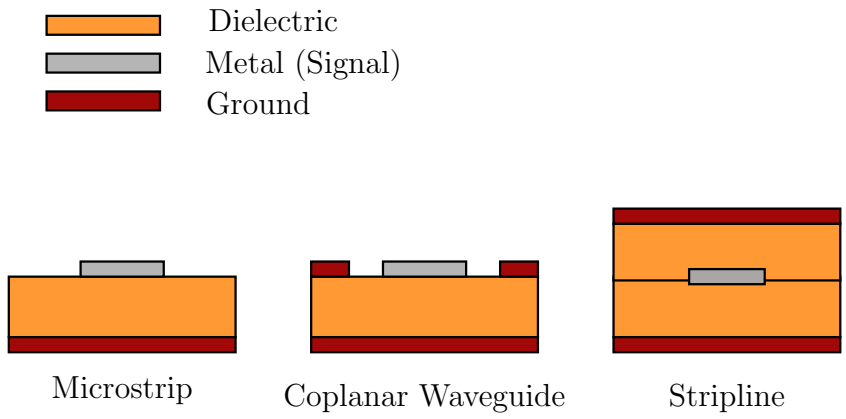

Figure 5-1: Basic Transmission Line Structures

the order of a quarter wavelength at the fundamental in order to achieve impedance transformations. With this metric we will be able to rank transmission line structures in terms of how compact networks are likely to be.

5.1 Transmission Line Structures

The basic transmission line structures considered in this chapter are shown in Figure 5-1. Microstrip consists of a single dielectric layer sandwiched between the transmission line and the ground plane. The coplanar waveguide with ground (CPWG) structure is similar to microstrip, but contains an additional ground in the plane of the transmission line. In a stripline structure, the transmission line lies in a dielectric material symmetrically spaced between two ground planes.

Some variations on these geometries will also be considered. Examples are shown in Figure 5-2. Embedded microstrip is a microstrip structure with a dielectric layer on top. Offset stripline has the transmission line offset from the center of the two ground planes. Unbalanced stripline has two different dielectric materials above and below the conductor.

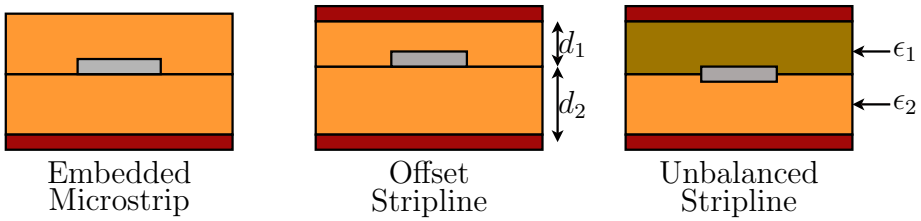

Figure 5-2: Variations on Basic Transmission Line Structures

5.2 Basic Transmission Line Simulations

Basic transmission line structures were analyzed using the ADS LineCalc tool. LineCalc takes substrate material properties and thickness as input and calculates transmission line dimensions given desired electrical lengths and impedances.

5.2.1 Microstrip

The only parameter that can be varied besides line width and length in a straightforward MCM microstrip structure is the thickness of the Kapton dielectric between the transmission line and the ground plane. In the upper layers of the MCM, this parameter can be varied in 1.5 mil increments as more layers are placed above the ground plane. Another possible structure has a ground plane on the substrate and the conductor in the metal 1 layer, for a total dielectric thickness of 7.5 mil. The possible geometries are shown in Figure 5-3. The results of simulations are given here:

Geometry	**Dielectric Thickness (mil)**	$W_{50\Omega}$ (mil)	$L_{\lambda/4}$ (mil)
Microstrip	1.5	3.41	813
Microstrip	3	6.99	808
Microstrip	4.5	10.6	807
Microstrip	7.5	17.8	805

We see that a variety of line impedances are available with microstrip configurations, but that a quarter wavelength line will be more than eight tenths of an inch long. In the interest of compact designs, a shorter line length would be desirable.

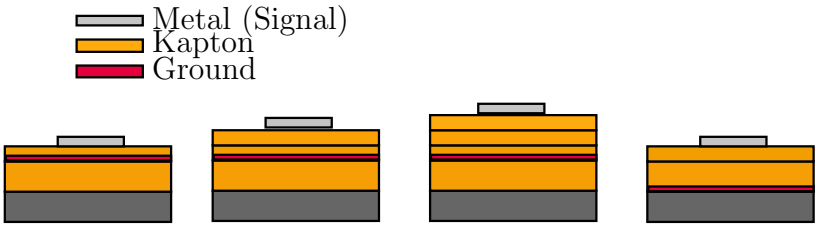

Figure 5-3: Geometries for Microstrip Structures

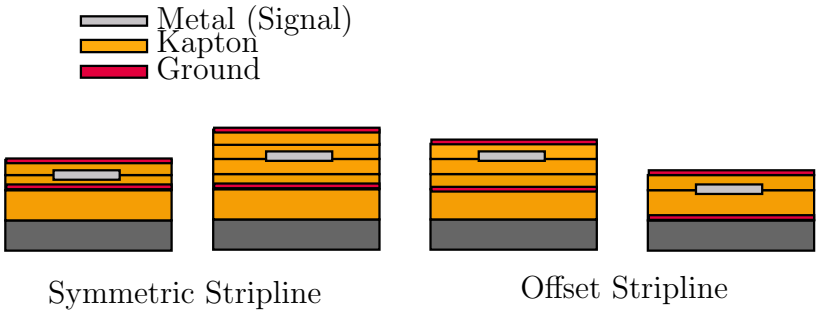

Figure 5-4: Geometries for Stripline Structures

5.2.2 Stripline

Because stripline occupies two layers in the MCM, fewer configurations are possible. We can achieve a total dielectric thickness of either 3 or 6 mils by occupying 3 or 5 metal layers respectively. The geometries are shown on the left in Figure 5-4. The results for stripline are shown here:

Geometry	**Dielectric Thickness (mil)**	$W_{50\Omega}$ (mil)	$L_{\lambda/4}$ (mil)
Stripline	3	1.44	717
Stripline	6	3.24	717

Stripline offers slightly shorter lines than microstrip. With the ground planes spaced 3 mils apart, the 50Ω line width is shorter than the 2 mil minimum line width allowed in the process, so this structure is not practical. Spacing the ground planes 4 layers apart brings the line width above 2 mils, but one might not want the transmission line structure to occupy that many metal layers, so this structure is not very attractive either.

A slight variation on stripline is the offset stripline structure, where the conductor is placed asymmetrically between the two ground planes. One configuration places two

1.5 mil Kapton layers below the conductor and 1 above it. A second configuration considered has the lower ground plane on the substrate, the conductor on metal 1, and the upper ground plane on metal 2. The two geometries are shown on the right in Figure 5-4. Dimensions obtained for these structures are as follows:

Geometry	**Lower Dielectric**	**Upper Dielectric**	$W_{50\Omega}$ (mil)	$L_{\lambda/4}$ (mil)
Offset Stripline	3 mil Kapton	1.5 mil Kapton	2.33	717
Offset Stripline	7.5 mil Kapton	1.5 mil Kapton	4.31	717

The offset stripline structure behaves in a similar fashion as the symmetric stripline structure. By placing more dielectric between the ground planes we are able to increase the 50Ω line width, but the quarter-wave line length stays unchanged.

5.2.3 Coplanar Waveguide With Ground

The coplanar waveguide with ground structure gives another parameter to vary besides dielectric thickness: the distance between the transmission line and the ground metal within the transmission line's plane (here denoted as S). The lower bound for S is 2 mils, given by the minimum metal to metal spacing in the Draper MCM-D process. Results for the CPWG simulations are given here:

Geometry	**Dielectric Thickness (mil)**	S (mil)	$W_{50\Omega}$ (mil)	$L_{\lambda/4}$ (mil)
CPWG	1.5	2	3.32	823
CPWG	1.5	4	3.66	801
CPWG	1.5	6	3.82	791
CPWG	3	2	5.94	841
CPWG	3	4	6.84	817
CPWG	3	6	7.22	805

The simulations show the CPWG structure behaving like the microstrip structure, with similar line widths and lengths.

Ultimately, all three of the structures above yield long quarter wave line lengths at 2.3 GHz as a result of the relatively low dielectric constant of Kapton. Since we are

interested in designing small circuits for hand held devices, it would be nice to identify a structure that could use shorter line lengths for impedance transformations. We will identify two such structures in the following section.

5.3 Variations on Basic Structures

The following two structures employ patterning transmission lines on the alumina substrate to take advantage of its high dielectric constant. It should be noted as it was in the previous chapter that this feature is not currently supported in the Draper MCM-D process. The analysis here serves to point out a potential benefit of pursuing patterning on the substrate in future processes.

The transmission line structures discussed in the following sections are not supported by the ADS LineCalc tool and do not loan themselves to simple analysis. 50Ω line widths and $\lambda/4$ line lengths were identified using an electromagnetic fieldsolver from Agilent called Momentum. Momentum is a "2.5 dimensional" field solver, termed as such because it models the interactions between multiple layers of a planar transmission line structure but does not analyze arbitrary 3-D structures. The following geometries were constructed in Momentum, and line widths and lengths were adjusted until the 50Ω line widths and $\lambda/4$ line lengths were found.

5.3.1 Embedded Microstrip

As stated before, in an embedded microstrip structure, an additional dielectric layer is placed on top of the transmission line. The effective dielectric constant seen by the transmission line is increased, because the line sees the dielectric material instead of free space above it. The three geometries shown in Figure 5-5 were simulated. In the geometry on the left, the line resides on the alumina substrate. The ground plane is placed below the substrate, and the dielectric layer above the line is 7.5 mils thick. In the geometry in the center, the line resides on the metal 1 layer. The ground plane is on top of the substrate, and the upper dielectric is formed with additional Kapton film layers. In the geometry on the right, all of the metal lies in the upper layers. The

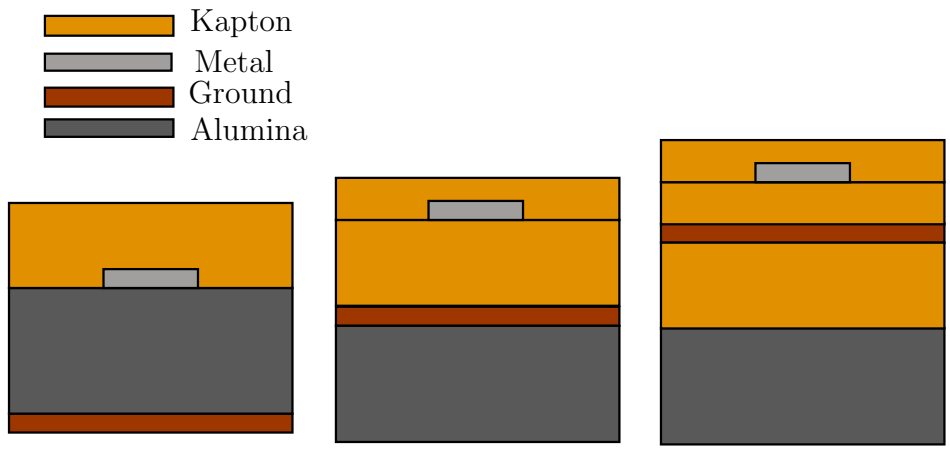

Figure 5-5: Embedded Microstrip Structures

ground plane lies on the metal 1 layer and the transmission line lies in a layer above it. The results of the simulations are summarized here:

Geometry	**Lower Dielectric**	**Upper Dielectric**	$W_{50\Omega}$ (mil)	$L_{\lambda/4}$ (mil)
Embedded Mstrip	25 mil Alumina	7.5 mil Kapton	23.2	492
Embedded Mstrip	7.5 mil Kapton	1.5 mil Kapton	17.5	765
Embedded Mstrip	7.5 mil Kapton	3 mil Kapton	16.9	747
Embedded Mstrip	3 mil Kapton	3 mil Kapton	6.5	736
Embedded Mstrip	3 mil Kapton	1.5 mil Kapton	7	752
Embedded Mstrip	1.5 mil Kapton	1.5 mil Kapton	3.4	721

Patterning the transmission line on the substrate offers a significant reduction in quarter-wave line length. The shortcoming of this structure is its 50Ω line width of 23.2, which will result in very wide low impedance lines. For example, if our circuit needed to transform 4Ω up to 50Ω, a line impedance of around 14Ω would be required. Using an embedded microstrip line on the alumina, a 14Ω line would be approximately 165 mils wide, which, aside from being bulky, would likely exhibit non-ideal transmission line behavior.

One option for reducing the line widths would be to reduce the thickness of the alumina substrate. Some MCM circuits have been fabricated at Draper using a 10 mil

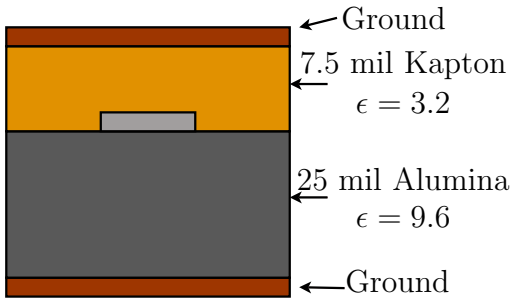

Figure 5-6: Unbalanced Stripline Structure

thick substrate. Simulations showed that the embedded microstrip structure with a 10 mil alumina layer and a 7.5 mil Kapton layer would yield a $W_{50\Omega}$ of 9 mil and an $L_{\lambda/4}$ of 465. While these numbers are quite promising, we will try to find a structure that uses the standard 25 mil alumina substrate.

5.3.2 Unbalanced Stripline

In an unbalanced stripline structure, the thicknesses and dielectric constants of the dielectric material above and below the transmission lines are not necessarily equal. The specific structure simulated here is shown in Figure 5-6. The transmission line is on the substrate, with one ground plane below the substrate and the other on the metal 1 layer.

The results for this structure are shown here:

Geometry	**Lower Dielectric**	**Upper Dielectric**	$W_{50\Omega}$ (mil)	$L_{\lambda/4}$ (mil)
Unbalanced Stripline	1.5 mil Kapton	1.5 mil Kapton	8.0	554

This structure offers a good balance between a moderate 50Ω line width and a short quarter-wave line length.

5.4 Summary

The best structure presented in this chapter for compact designs that used the standard alumina substrate thickness of 25 mils was the unbalanced stripline structure. It offered

a reasonable 50Ω line width of 8 mils and a quarter-wave line length of 554 mils. The structure does have some disadvantages. First of all, it is not currently supported by the Draper MCM-D process, so it could only be used in the event that metalization on the substrate is supported as well as vias through the 6 mil die layer of the MCM. Even if metalization on the substrate is supported, the analysis of chapter 4 reveals that this structure will yield a relatively high parasitic inductance and shunt capacitance on connections to the substrate. Fortunately, the parasitic inductance on the gate and drain connections can be absorbed into input and output transmission line networks. The source connection will be made from the die to the metal 1 layer, so it will have very low series inductance.

The best structure identified that stays within the current MCM-D design rules is the embedded microstrip structure in the upper layers of the MCM. This allows low impedance connections to be made to the gate, drain, and source. The line lengths are reduced from the simple microstrip case, and the line widths are above the minimum allowed for the process while remaining small. A main drawback to this structure is that it can not be analyzed and modeled as easily as microstrip. Testing a prototype using this structure would also be difficult because the networks would have to be probed with vias.

Chapter 6

PCB Power Amplifier Design

In order to learn more about E-pHEMT technology and the high efficiency power amplifier design process, a PCB power amplifier design was executed at Draper Laboratory. The specs for the amplifier were maximal efficiency at 2.3 GHz and 1W output power. A PCB designed at Draper using a depletion mode pHEMT was used as a guideline for the E-pHEMT design. This amplifier achieved approximately 70% PAE at 1 W and 2.3 GHz.

6.1 Design Tools

The primary simulation tool used for the design was Agilent's Advanced Design System (ADS). Within ADS, a harmonic balance simulator was used to simulate large signal circuit performance. The harmonic balance method is a powerful simulation tool for analyzing nonlinear RF circuits. It combines frequency domain analyses of linear elements with time domain analyses of nonlinear elements to iteratively converge on a steady state solution at the fundamental frequency and a pre-determined number of harmonics. In this way the simulator can generate a periodic steady state time domain response of a nonlinear circuit more quickly than a standard time domain simulator would.

In addition to using standard simulation tools in ADS, Momentum, an electromagnetic fieldsolver described in chapter 5, was used to accurately model input and output

transmission line networks.

For the reasons given in chapter 2, the ATF511P8 and ATF501P8 were chosen for this design, and the ADS models for these devices were used in simulations. Since it was unclear which part would ultimately perform better, individual designs were optimized for each part. We will describe the design using the 511P8 here.

6.2 Design Procedure

The overall design procedure consisted of three major steps:

1. **Numerical Impedance Optimization:** The transistor was presented with ideal source and load impedances at the fundamental frequency and the 2nd, 3rd, and 4th harmonics. These impedances, along with the gate and drain bias levels, were optimized for maximum PAE. These results were used to determine the class of operation and topology for the circuit.

2. **Microstrip Network Design in ADS:** The impedances obtained from step 1 were used to design microstrip input and output networks using microstrip models in ADS.

3. **Electromagnetic Modeling of Microstrip Networks:** Momentum was used to model and tune the microstrip networks to obtain the desired impedances.

Progression through the three steps was not strictly sequential. For example, completion of step 2 yielded a realistic set of impedances that could be achieved in microstrip. These impedances were fed back into step 1, and those impedances that could realistically be adjusted further were then reoptimized.

The following three sections give the details of these three steps for the design of the ATF511P8 power amplifier.

Figure 6-1: ATF511P8 Gate Package Parasitics

6.3 Numerical Impedance Optimization

In the first step of the design procedure, numerical impedances were presented to the drain and the gate of the transistor and optimized. At this point, a decision needed to be made as to how package parasitics would be dealt with in the design process. The Agilent device models each came with a model of the bare transistor die and a separate lumped element model of the package. The most significant parasitic effect is the inductance resulting from the bondwire connections from the die to the package. The model also includes a series resistance and a shunt capacitance. The package model for the gate connection of the 511P8 is shown in Figure 6-1.

By presenting the numerical impedances directly to the die of the transistor, one gains a greater intuition for the physical meaning of the optimized impedances since they are not altered to compensate for package parasitics. Therefore, the impedance blocks were connected directly to the die model with the understanding that the gate and drain package parasitics would be lumped in with the input and output networks. On the other hand, because the source package parasitics are connected from the transistor source to ground, they could not be decoupled from the transistor at this stage and were included in these simulations. A schematic of the setup is shown in Figure 6-2.

A gradient based optimizer was used in ADS. This optimization involved a large number of degrees of freedom: four harmonic impedances at the input and output, each with a real and imaginary part, and two bias voltages. In order to avoid finding meaningless local minima in the error surface, intelligent guesses had to be made as to

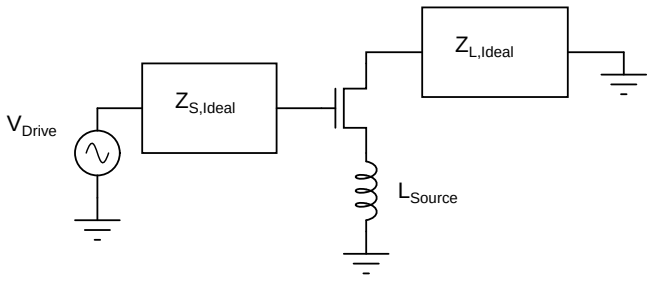

Figure 6-2: Schematic Representation of Numerical Optimization Setup

initial parameter values. These guesses were based upon expected bias conditions and harmonic terminations for Class E and Class F power amplifiers. Since the Class E amplifier is designed using time domain analysis, the harmonic terminations that yield Class E operation are not so easily defined. For the basic Class E topology given in section 1.2.2, the series LC circuit at the output presents an inductive impedance at the fundamental and a rising impedance at the 2nd and 3rd harmonics. Transmission line topologies encountered in the literature generally presented a high impedance above the fundamental [3] [8]. The Class F case is more straightforward: the drain is presented with a match at the fundamental, shorts at even harmonics, and high impedances at odd harmonics. In both cases, we expect the gate bias to be near the pinch-off voltage V_P.

To determine an initial estimate for the fundamental load impedance, the following Class-E design equation was used [12]:

$$R = \frac{8V_{DD}^2}{P_{out}(\pi^2 + 4)} \tag{6.1}$$

For a V_{DD} of 4V this equation yields a resistance of 9.2Ω.

S-parameter simulations showed a capacitive low impedance at the gate of both transistors. The matching fundamental impedance could therefore be expected to be low and inductive. Previous high efficiency PA designs completed at Draper presented the gate with a 2nd harmonic short. A similar approach is used in [13]. The author argues that the nonlinear capacitance C_{GS} at the input of a pHEMT device acts like varactor frequency doubler, introducting a strong 2nd harmonic component to the drive

Table 6.1: ATF511P8 Optimized Numerical Impedances

Harmonic	Gate Impedance	Drain Impedance
1st	3.642 + j3.890	6.789 + j3.380
2nd	0 - j11.80	0 + j7.670
3rd	15.07 - j46.42	850 + j21.60

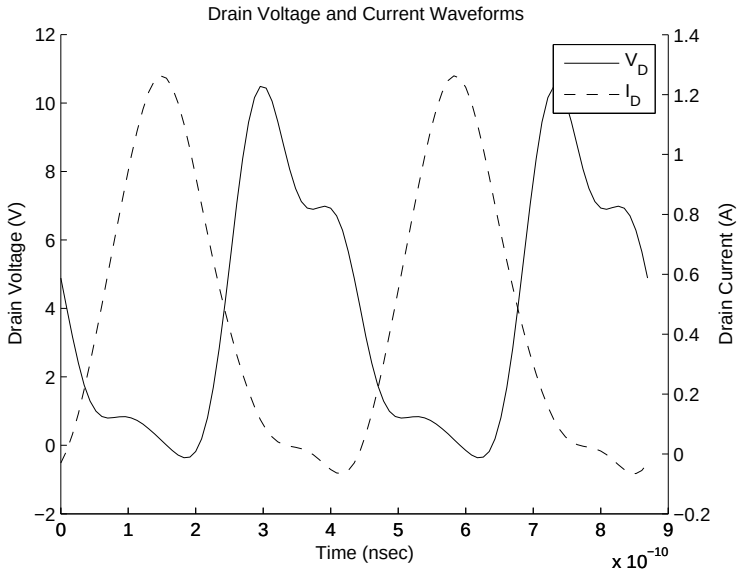

Figure 6-3: Time Domain Drain Voltage and Current Waveforms

waveform. The effect of this second harmonic energy is to alter the duty cycle of the drain waveforms, potentially reducing efficiency. Presenting a 2nd harmonic short at the gate helps restore sinusoidal drive.

Optimizations were run using a variety of initial conditions based on the above guidelines. The 4th harmonic impedances were found to have little effect on efficiency and were omitted as optimization parameters. Table 6.1 shows the optimal impedances obtained, which yielded a PAE of 59.7% at 31.3 dBm output power. Drain voltage and current time domain waveforms are given in Figure 6-3.

The load impedances in table 6.1 are hard to classify as distinctly Class E or Class F. The impedance at the fundamental is slightly inductive, which is indicative of Class E operation. The short at the 2nd harmonic, however, will in theory make the

drain voltage waveform more symmetric, and Class E amplifiers rely on asymmetry to produce the desired drain waveform shape. Both Class E and Class F amplifiers are designed around the assumption that the transistor behaves as an ideal switch. Ultimately, it is difficult to tell whether the impedances we have obtained are serving to place the device in one of the two regimes of operation, or if they are just compensating for non-idealities in the transistor switching behavior. It is likely that the amplifier we have ended up with has both Class E and Class F characteristics.

For the input impedance block, the optimal solution included a second harmonic short as expected. The drain bias for the amplifier was 4V, and the gate bias was near V_P at .3V.

The figure of 59.7% PAE was a slight disappointment at this stage of the design. The data sheet indicated that a PAE of 69% was achievable. One would think this figure could be achieved or even exceeded in a simulation that did not include the effects of drain and gate package parasitics or transmission line losses. One of the main reasons for the low PAE is the relatively low gain of 7.3 dB achieved at the maximally efficient output power. The effect of the low gain can be seen clearly in Figure 6-4. The drain efficency reaches a respectable 73% at the point of maximum PAE and keeps rising even after the PAE has leveled off and begun to drop.

The output power of 31.3 dBm was higher than expected or required, and it was thought that some amount of output power could be traded for increased PAE. In past high efficiency amplifier designs completed at Draper, lower output power translated into lower currents and lower dissipation in the transistor, which increased PAE. This was not the case for the E-pHEMT design. While attempts to decrese the output power by lowering the supply voltage or raising the output impedance did yield small increases in drain efficiency, they also resulted in lower gain. The losses in gain won out over increases in drain efficiency, ultimately lowering PAE.

Before moving on, we will point out one feature of the time domain waveforms shown in Figure 6-3 that was a potential cause for concern. The voltage waveform exhibits a sharp peak on its rising edge that rises above 10V. Such a peak in the voltage waveform poses the potential problem of exceeding the breakdown voltage for the gate to drain

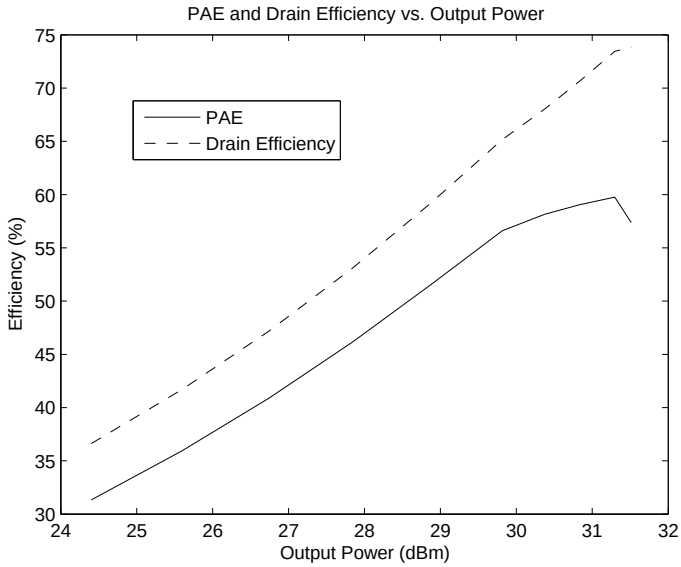

Figure 6-4: Comparison of PAE and Drain Efficiency

junction. Indeed, in the simulation V_{DG} reached a maximum of 11.3V. As discussed in section 2.2.1, the breakdown voltage for this device was unknown, but was thought to be at least 10V based upon the maximum DC V_{DG} spec. It was therefore unclear whether such a drain voltage waveform would be problematic. Since the peak drain voltage was likely to decrease slightly with the introduction of microstrip losses it was decided to proceed with the design. Nonetheless this issue would have to be watched for when testing the actual device.

6.4 Microstrip Network Designs

The numerical impedances obtained from the optimizations were used to construct input and output microstrip networks using linear microstrip models in ADS. These models take into account the material properties of the microstrip substrate like thickness, loss tangent, and dielectric constant to model dispersion and loss as well as impedance and electrical length. We will first analyze the load network design.

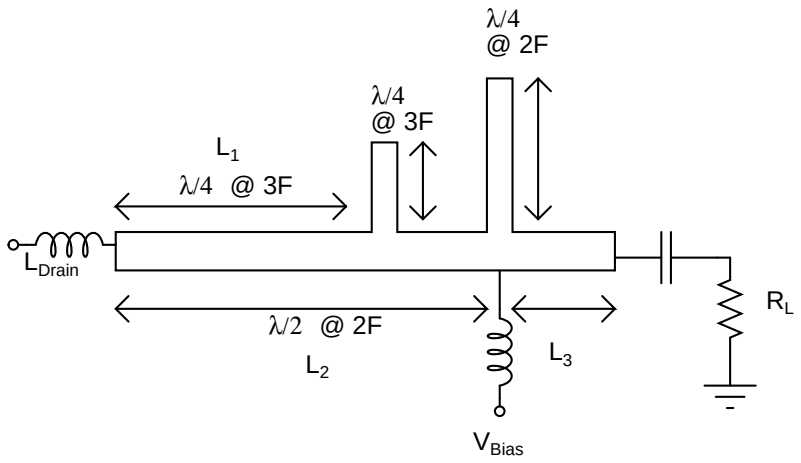

Figure 6-5: Load Network Topology

6.4.1 Load Network Design

Several Class F load network designs had been investigated at Draper in their research on high efficiency amplifiers. In this case, the design needed to meet the following criteria:

1. Transformation the desired output impedance up to 50 Ω.
2. Termination of the 2nd harmonic with a low impedance.
3. Termination of the 3rd harmonic with a high impedance.
4. DC bias network that leaves RF characteristics unaffected.
5. Series transmission line at input to absorb package inductance.

The topology in Figure 6-5 met all of the above criteria. The network consists of a quarter wave transformer with two open circuit stubs, one each for the 2nd and 3rd harmonics. Each stub is a quarter wavelength long at its respective harmonic frequency, so that each open circuit is seen as a short at the transmission line. The distance L_1 between the third harmonic stub and the drain is set to a quarter wavelength at the third harmonic. The impedance seen at the drain is the reciprocal of a short, or an open circuit, which is the desired 3rd harmonic impedance. The distance L_2 between

the second harmonic stub and the drain is a half wavelength at the second harmonic so that it is still seen as a short. The length and width of the entire series line is set to provide the appropriate impedance transformation from the desired fundamental impedance up to 50 Ω.

This load network topology has the nice feature of connecting to the drain through a series transmission line. The parasitic output inductance behaves like a short piece of transmission line whose length varies with frequency. The affect of this inductance can be negated by shortening the series transmission line and adjusting the placement of the two open stubs.

The exact dimensions of the microstrip network were determined using S-parameter simulations in ADS. First, the necessary characteristic impedance of the transmission line was estimated using the equation: $Z_T = \sqrt{Z_S * Z_L}$, where Z_T is the transmission line impedance, Z_S is the impedance we would like the drain to see, and Z_L is 50 Ω. An ADS tool called LineCalc was used to convert line impedances and electrical lengths (given in degrees at a specific frequency) into physical microstrip dimensions. The placement and length of the stubs were also estimated using LineCalc. With these initial dimensions as a starting point, an optimum solution was found through the following iterative procedure:

1. L_1 and the third harmonic stub length were optimized to yield the highest 3rd harmonic impedance possible at the drain.

2. With L_1 fixed, L_2 and the 2nd harmonic stub length were optimized to get as close to the desired 2nd harmonic impedance as possible.

3. With L_1 and L_2 fixed, L_3 and the series line width were optimized to yield the desired impedance at the fundamental.

These three steps were repeated until only negligible improvements were achieved. Finally, the lengths of the stubs were adjusted a final time to fine tune the two minima in the S_{21} forward transmission curve so they fell exactly on the second and third harmonics. This step would help assure spectral purity in the load waveforms of the completed amplifier.

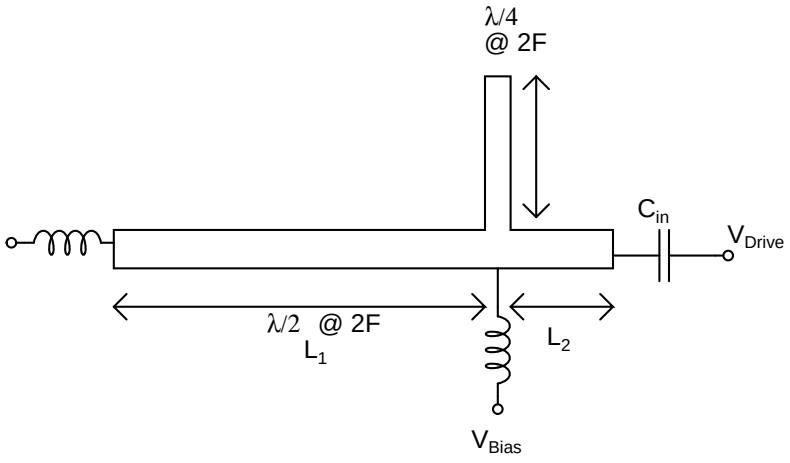

Figure 6-6: Input Network Topology

6.4.2 Input Network Design

The input network design, shown in Figure 6-6 is very similar to the output network design with a couple of important differences. In this case we are only interested in terminating the 2nd harmonic, so no 3rd harmonic termination is included.

One important difference between the input and output networks is the role of C_{in}. In the output network, the capacitor that couples the network to the load is simply a DC blocking capacitor, chosen to have a self resonant frequency around the fundamental to present a low impedance. In the input network, C_{in} is chosen to be small enough to play a role in the RF impedance match. Because the transistor input impedance is low (on the order of 4Ω), a very low impedance transmission line would be required to match the gate to 50 Ω with a simple quarter wave transformer. Simulations revealed that a series line 100 mils wide and 280 mils long would be required. Such a low length to width ratio can be problematic in designing transmission line networks. The series capacitor serves to raise the line impedance required to make the impedance transformation. Figures 6-7 and 6-8 compare the impedance match using a simple quarter wave transformer and a transmission line/series capacitor combination. In the latter case, the transmission line impedance Z_T is moved to the right on the smith chart (to a higher impedance) with the addition of the series capacitance.

Line dimensions were calculated and optimized in an iterative fashion similar to

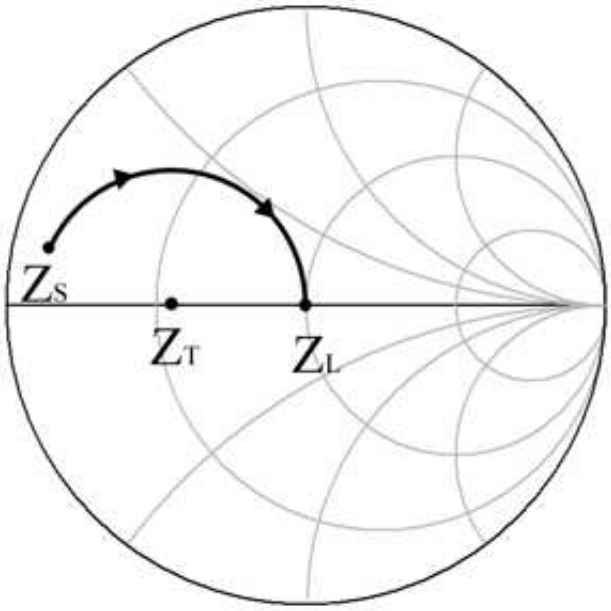

Figure 6-7: Input Match With $\lambda/4$ Transformer

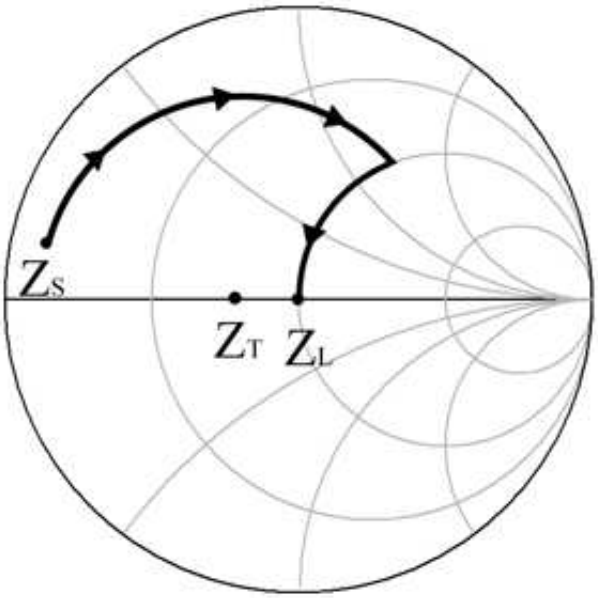

Figure 6-8: Input Match With $\lambda/4$ Transformer and Series Capacitor

that used for the output network.

6.4.3 Bias Network Design

The input and output bias networks used for this design were the same ones used for the previous pHEMT high efficiency amplifier design. Traditionally power amplifiers are biased with a transmission line that is a quarter wavelength long at the fundamental or with a large inductor with a self resonant frequency around the fundamental. Both of these solutions are unattractive when small circuit area is a goal. The bias network in this design uses an inductor choke, but cleverly exploits the capacitance of the 2nd harmonic termination to allow for a reduction in its size. In this case an inductor with a self-resonant frequency of 8.2 GHz is chosen.

One way to reduce the size of the inductor required in a bias network is to put a capacitance in parallel with it. The two elements will resonate at a frequency lower than the self- resonant frequency of the inductor, allowing a high impedance to be seen at this lower frequency. In the bias network for this design, the inductor is placed with its center line directly opposite the 2nd harmonic stub, so that the capacitance of the stub resonates with the inductor at the fundamental and presents a high impedance. This has the effect of both allowing the bias inductor to be smaller and absorbing the 2nd harmonic stub capacitance into the resonant structure so it no longer has a parasitic effect at the fundamental.

At this point, the impedances measured in the input and output microstrip networks were fed back into the numerical impedance optimization step. In both networks, the minimum real part that could be achieved for the 2nd harmonic impedances (ie, the quality of the "short") was around 2Ω. In the second round of optimizations, 2Ω was used as a realistic lower bound for both of these parameters. Additionally the 3rd and 4th harmonic impedances were now fixed in both the input and the output. Those parameters that were still deemed to be adjustable in the input and output networks - the fundamental impedances and the imaginary parts of the 2nd harmonic impedances - were then re-optimized along with the bias voltages. The entire process of feeding back results from the microstrip simulations to the numerical optimizations was repeated

Table 6.2: ATF511P8 Input and Output Network Impedances

Harmonic	**Gate Impedance**	**Drain Impedance**
1st	3.850 + j3.317	7.050 + j2.470
2nd	2.034 - j12.95	2.475 - j8.397
3rd	15.13 - j46.39	786.2 + j20.00

Table 6.3: Comparison Of Amplifier Performances with Ideal and Microstrip Networks

	Ideal Impedance	**Microstrip Network**
P_{in}	.25 W	.25 W
P_{out}	1.35 W	1.17 W
P_{DC}	1.84 W	1.84 W
P_{Drain}	.485 W	.501 W
PAE	57.6%	50.0%

twice, at which point further optimization resulted in negligible improvements in PAE.

The maximum PAE achieved in the final numerical impedance simulations was 57.6%. The drop in efficiency from the 59.7% achieved in the first step was mostly the result of non-ideal shorts at both 2nd harmonic impedances being accounted for. At this point, the four harmonic impedances at the input and output matched the impedances measured in the microstrip networks exactly. The final impedances arrived at are shown in Table 6.2.

With the input and output networks tuned to the proper impedances, the whole amp was simulated. The maximum PAE was 50.0%, achieved with an input power of 24 dBm and an output power of 30.7 dBm. Table 6.3 compares power dissipation figures for the ideal impedance amplifier and the microstrip amplifier. Table 6.4 gives power losses in the microstrip networks. The data clearly show that the large drop in PAE is the result of microstrip losses. Total DC power dissipation and dissipation in the drain of the transistor change very little across the two simulations. Losses of .50 dB and .59 dB are reasonable figures for microstrip losses in an application such as this. The problem in this case is that the gain of the amplifier was so low to begin with, the additional losses in the microstrip had a disastrous effect on PAE.

Table 6.4: Power Loss in Microstrip Networks

	Power Loss (W)	**Power Loss (dB)**
Input Network	.027 W	.51 dB
Output Network	.17 W	.59 dB

6.5 Momentum Simulations

The final step in the design procedure was simulating the input and output networks using Momentum to fine tune dimensions for the final layout. Figure 6-9 shows the layout of the output network in Momentum. Ports were placed at the input and output of the network, as well as at every point that an external lumped element device would interface with the network. In the diagram, ports 1 and 10 are the load and drain connections, respectively. The structure on the left in the diagram is the land pattern for the ATF511P8 transistor. Ports 2 and 3 are connections to the input coupling capacitor. Ports 4 and 5 connect the bias choke, and ports 6-9 connect power supply bypass capacitors. The small squares enclosed in the metal at the top and left sides of the layout represent vias to the ground plane. Simulations in Momentum yielded a 10 port S-parameter model of the microstrip network, which was used in conjunction with device models in ADS to simulate the input and output networks, and eventually the entire amplifier.

The dimensions of the network were adjusted in largely the same fashion as they were using the linear microstrip simulations. Using gradient based optimization to adjust the dimensions was impractical in this case due to the large amount of time it took to generate each model of the transmission line network in Momentum. Instead, adjustments on the order of 1-5 mils at a time were made manually and simulations were repeated until the S_{11} and S_{21} parameters of the network were reasonably close to the target values at the frequencies of interest.

When both networks were satisfactorily tuned, the entire amp was simulated. Using the same bias conditions that were used in the numerical and linear microstrip simulations ($V_D = 4V$, $V_G = .33V$), the amp ran at 44.6% PAE with 29.8 dBm output

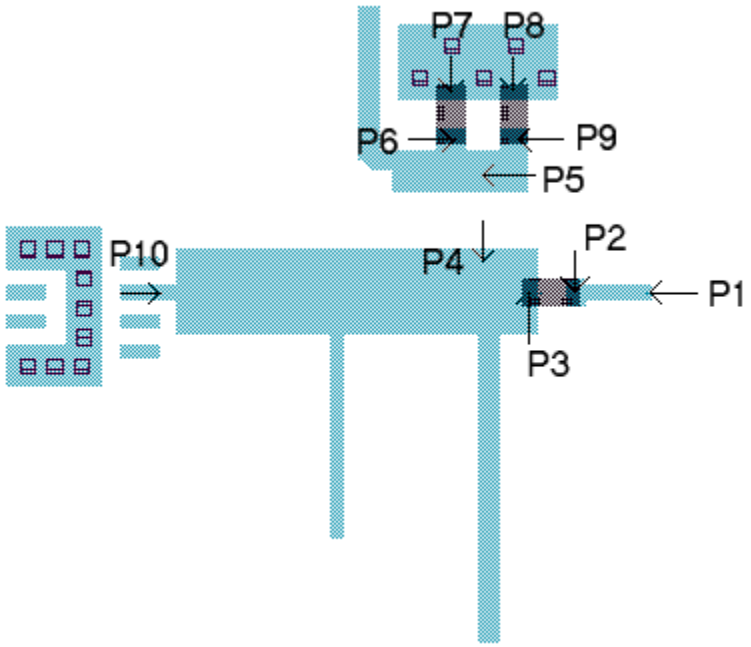

Figure 6-9: Output Network Momentum Layout

power. Optimizing the bias voltages with a 5 volt upper bound on the supply yielded $V_D = 5V$ and $V_G = .46V$, resulting in a PAE of 46.8% at 32.0 dBm output power. These later results should be treated with skepticism because the drain to gate voltage (V_{DG}) reached a potentially dangerous level of 13V at its peak value. Table 6.5 summarizes power dissipation in the amp under the two different bias conditions.

As expected, when operating at the higher supply voltage, power dissipation in the drain increased dramatically. The increase in gain, however, was large enough to boost

Table 6.5: Momentum Simulations of Amps Under Different Bias Conditions

	$V_D = 4V$, $V_G = .33V$	$V_D = 5V$, $V_G = .46V$
P_{in}	.200 W	.244 W
P_{out}	.955 W	1.57 W
P_{DC}	1.67 W	2.82 W
P_{Drain}	.524 W	.911 W
Gain	7.0 dB	8.0 dB
PAE	44.6%	46.8%

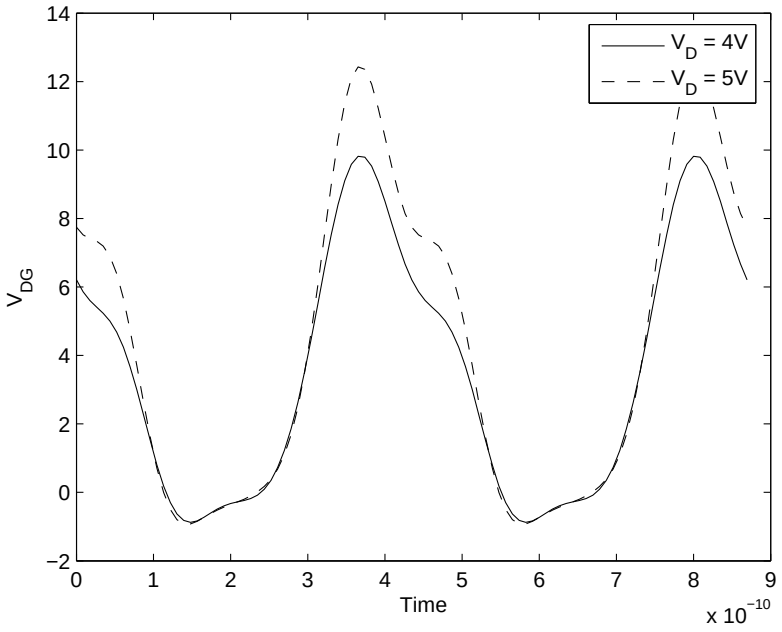

Figure 6-10: V_{DG} Time Domain Waveforms for Two Bias Conditions

Table 6.6: Power Loss in Microstrip Networks: Linear Sim. vs. Momentum

	Linear Simulator μstrip Loss	**Momentum μstrip Loss**
Input Network	.51 dB	1.02 dB
Output Network	.59 dB	.80 dB

PAE by 2.2%. Again, the figures for the higher power case should be treated with some skepticism because of breakdown voltage concerns. Time domain plots of the gate to drain voltage for both bias conditions are given in Figure 6-10.

The main factor contributing to the drop in PAE from the linear simulator models to the Momentum models is increased loss in the Microstrip networks. Table 6.6 compares loss between the two simulation stages. The fact that the Momentum networks exhibited higher loss is not surprising. Momentum is capable of factoring in a wider variety of non-idealities to its analyses that contribute to microstrip losses.

6.6 Summary of Simulation Results

The final PAE figures of 44-46% were quite disappointing. The main problem throughout the design procedure was never power dissipation in the drain, as is often the case with high efficiency designs. It was a combination of low gain and microstrip losses. Indeed, in the final momentum simulations, drain power dissipation only accounted for 31.3% of power drawn from the DC supply. The rest of the loss in PAE resulted from microstrip losses and the large amount of power required to drive the device.

In retrospect, two main device parameters of the ATF511P8 can be identified as contributing to large microstrip losses and low gain. The first is the maximum DC V_{DG} of 5 volts. Limiting the power supply to 5 volts (and possibly lower if the device breakdown voltage proves to be a problem when testing actual devices) forces the amp to run at high current levels, which increases losses in the microstrip. The other device parameter that likely contributed to poor PAE was the input capacitance C_{gs}. The C_{gs} given in the device model was 10.3 pF, which is a relatively high value. In comparison, a depletion mode pHEMT used in a previous high efficiency amplifier design at Draper had a C_{gs} of only 4.44 pF. High C_{gs} results in low power gain in general, but it can be particularly problematic when attempting to drive a transistor hard enough to act as a switch. It is possible that the high C_{gs} of this device made it poorly suited to switching-mode operation.

As stated at the beginning of this chapter, another design was completed using the ATF501P8 from Agilent. This design performed slightly better in simulation, with a PAE ranging from 46% to 48%. The two transistors are very similar, and the design procedure used was identical. Most of the trends in the simulation results were the same, and they offer little insight over what was described here, so the details of this second design are omitted.

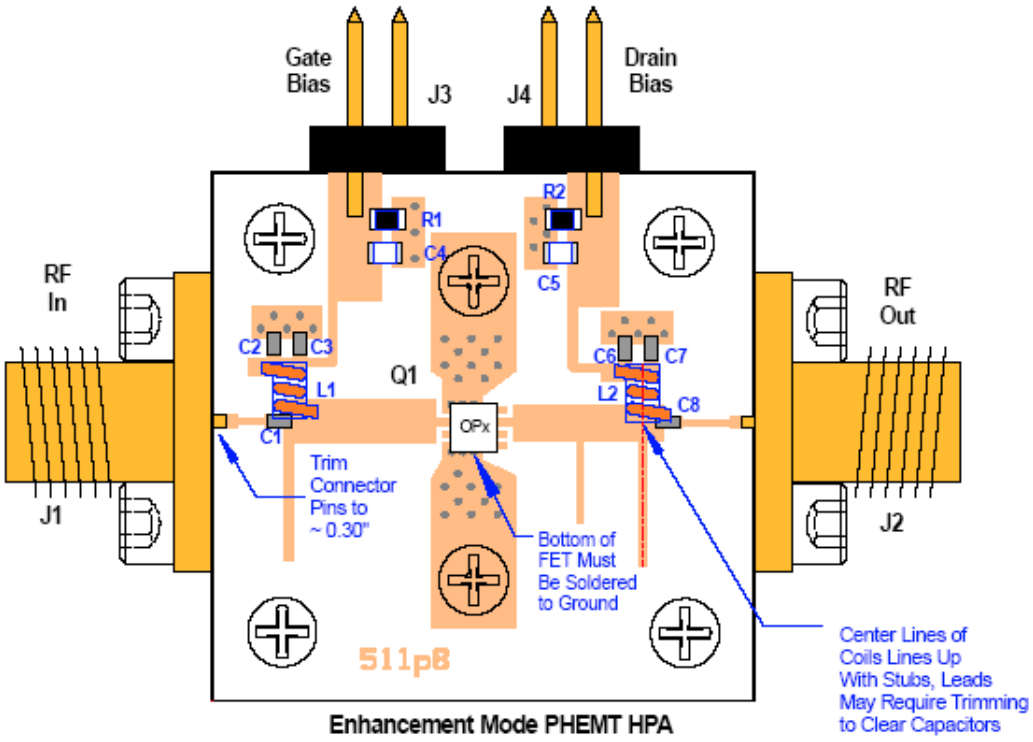

Figure 6-11: Full PCB Amp Layout

6.7 Layout

Despite the disappointing simulation results, at this stage it was decided to complete a layout and fabricate the design to compare actual performance with simulation. As discussed in section 2.2.2, the transistor model had consistently underperformed the PAE specs on the data sheet for the part, so it was thought that a well tuned amplifier might perform better than simulations suggest.

The final layout is shown in Figure 6-11. The board was designed for fabrication on Rogers TMM13i dielectric material, which has a high dielectric constant of 12.8 and resulted in a small, compact layout. The board is about one square inch in size.

Chapter 7

PCB Amplifier Testing

The board design detailed in chapter 6 was fabricated at Microwave Circuit Technologies and the amplifier was assembled at Draper Laboratory, where testing was performed.

7.1 Test Setup

The setup used to test the amplifier is shown in Figure 7-1. A signal generator was connected to a driver amplifier to provide the 2.3 GHz input signal at the appropriate input power range. This was fed into a low pass filter to remove any harmonic energy at the output of the driver amplifier. A coupler was used to feed some of the input power to a power meter for accurate measurement of the input power level. The output of the coupler was connected to the input of the E-pHEMT amplifier.

A coupler was used at the output of the amplifier to pass part of the output power to a spectrum analyzer, so that the spectral content of the output signal could be measured. A broadband coupler was chosen to allow accurate reading of the first four harmonics. The output of the coupler was connected to a 20dB attenuator to bring the output power to an appropriate input level to be read safely by the power meter. The attenuator output was passed to a low pass filter to filter out any harmonic energy and ensure that only power at the fundamental was being measured. The filter output was then connected to a power meter to measure the output power level.

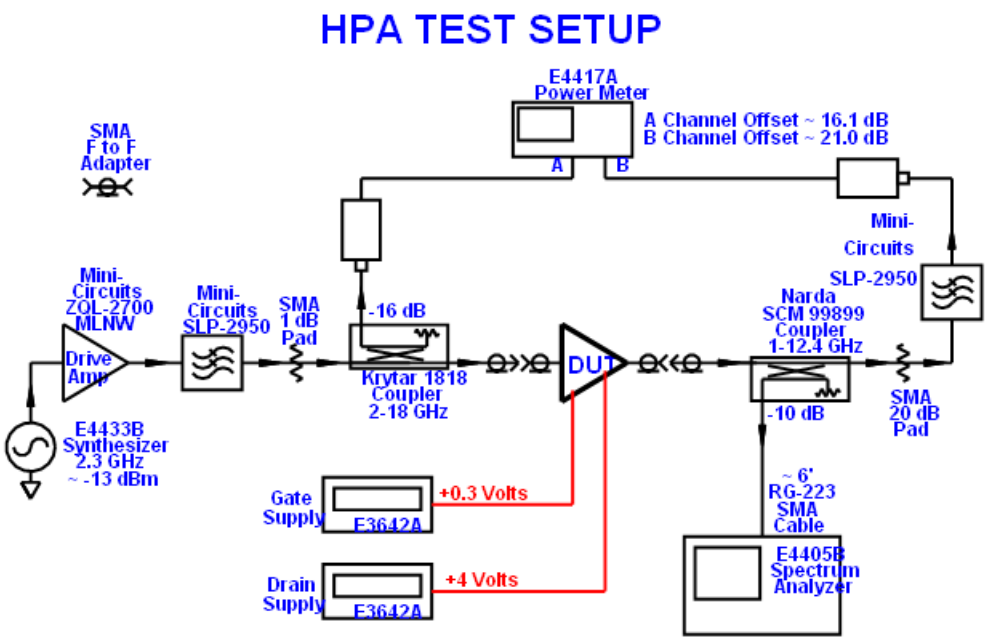

Figure 7-1: E-pHEMT Amplifier Test Setup

Two adjustable DC power supplies were used to provide the gate and drain bias voltages, and the DC currents from each supply were monitored. Before testing began, the power meters were calibrated. Offsets were set in each to accurately reflect the input and output power of the power amplifier. Because the spectrum analyzer would only be used to determine power levels of the harmonics relative to the fundamental, only a rough offset calibration was done.

The entire setup allowed for the accurate measurement of input power, output power, output spectral content, and DC gate and drain voltage and current.

7.2 Device Turn-On

For an enhancement mode device, the sequencing of the application of the gate and drain power supplies should in theory not be an issue. Nevertheless, a strict procedure was adhered to for powering the device on and off:

1. The gate bias was applied and set to zero volts to ensure that the device was pinched off.

2. The drain supply was then applied and slowly ramped up to a value of 4 volts while monitoring the drain current

3. The gate bias was then slowly raised along with RF drive power

During step 3, the amplifier went into oscillations when either 1) the gate voltage was raised above .2 volts, or 2) a drive signal of less than 16 dBm was applied. When oscillating, the transistor drew approximately 330 mA of DC drain current, a value that is high but by no means dangerous. The oscillations stopped once a drive signal of around 16 dBm or higher was applied. The exact value of the drive signal required to stop oscillations varied based on the bias conditions. For higher gate and drain biases, the power needed to stop oscillations was as high as 17 dBm. Once the oscillations had stopped, the power amplifier behaved normally. An pHEMT high efficiency amplifier design completed previously at Draper also oscillated at low drive levels. It is believed that the oscillations are the result of the load impedances presented to the drain at low frequencies by the resonant bias structure, which was a feature common to both amplifier designs.

7.3 Tuning

In order to tune the device, small chips of 25 mil thick alumina were placed on top of the transmission lines at various locations. The effect of the alumina, which has a high dielectric constant of 9.6, is to make the transmission lines appear electrically longer and have a slightly lower impedance. These are the same principles that apply to the embedded microstrip transmission line structure described in section 5.3.1.

This approach was quite effective in adjusting the lengths of the 2nd harmonic stubs on the input and output of the amplifier. It was the experience in past high efficiency amplifier designs at Draper that the stubs came back from fabrication slightly shorter than the optimal length. This was also the case here. When placing the alumina on top of the 2nd harmonic termination on the output, the 2nd harmonic on the spectrum analyzer dropped by around 7 dB. The output current dropped by several milliamps

Table 7.1: Performance for Maximum PAE with Pout > 30dBm

PAE	68.85%
V_{DS}	4.4V
V_{GS}	0V
P_{out}	30.03 dBm
P_{in}	19.50 dBm
Gain	10.53 dB
2nd Harmonic	-36.5 dBc
3rd Harmonic	-28.5 dBc
4th Harmonic	-32.5 dBc

without decreasing output power, resulting in increased efficiency. The alumina also reduced the 3rd harmonic content in the output, suggesting that this stub was also too long, but in this case no efficiency was gained. Tuning the input harmonic stub did not have a dramatic effect on output spectral content, but it did yield an increase in efficiency. The combined effect of tuning the two 2nd harmonic stubs was an increase in PAE of approximately 5%.

7.4 Test Results

Once the amplifier was tuned for maximum PAE above 30 dBm output power, the tuning was fixed and performance data were taken at a variety of bias and drive levels. The performance at maximum PAE while operating above 30 dBm output is shown in table 7.1. The peak PAE achieved was 68.85%.

Figure 7-2 shows PAE and P_{out} while sweeping V_{GS} for a fixed drive power of 19 dBm and a fixed V_{DS} of 4.6V. An interesting feature of this graph is that maximum efficiency is achieved with a bias of zero volts, indicating that the device is truly operating in the switching-mode and being strongly pinched off during the negative half cycle of the driving sinusoid. One potential concern with a low gate bias is an increased risk of exceeding the gate to drain breakdown voltage. At a drain supply of 4.6V this should not be a problem.

Figure 7-3 shows PAE and P_{out} while sweeping V_{DS} for a fixed drive power of 19

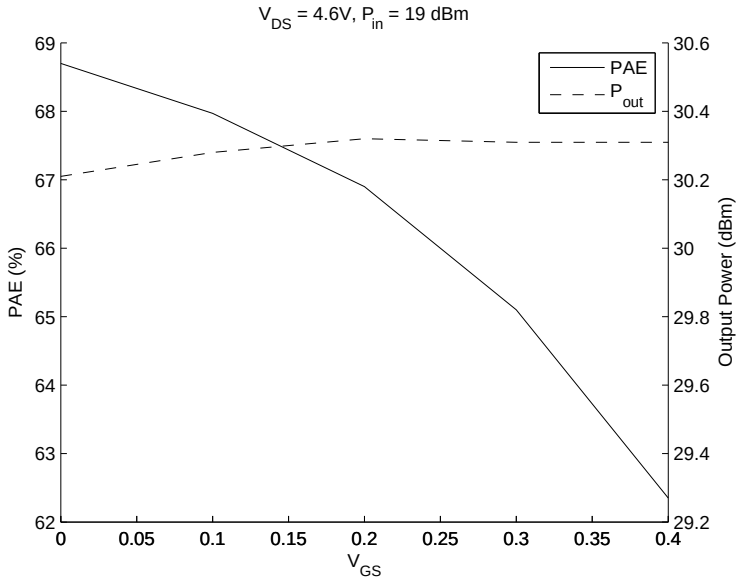

Figure 7-2: PAE and P_{out} vs. V_{GS}

dBm and a fixed V_{GS} of .1V. The results in the graph are as expected: for a fixed output impedance we should expect to see power output rise with increasing V_{DS}, and we should expect higher currents and higher IR dissipation in the transistor, so PAE should fall. This was the opposite of the trends observed with the transistor model.

Figure 7-4 shows PAE and P_{out} while sweeping P_{in} for a fixed V_{DS} of 4.4V and V_{GS} of 0V. As expected, PAE rises to a maximum and then decreases as a result of gain compression in the amplifier.

Figure 7-5 shows the maximum PAE achievable at a variety of V_{DS} values, along with the gain of the amplifier corresponding to each PAE. The graph suggests a tradeoff in gain and PAE up until the maximum PAE point, beyond which both gain and PAE fall. Again, these results are as expected.

7.5 Summary of Results

The performance of the amplifier was a pleasant surprise following the poor performance of the simulations. It was suspected throughout the design process that the device model was inaccurate, and the performance of the amplifier validated that sus-

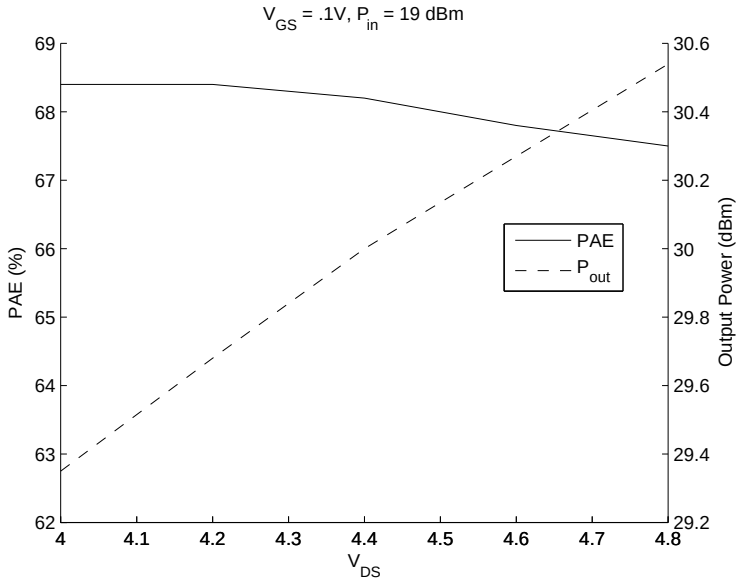

Figure 7-3: PAE and P_{out} vs. V_{DS}

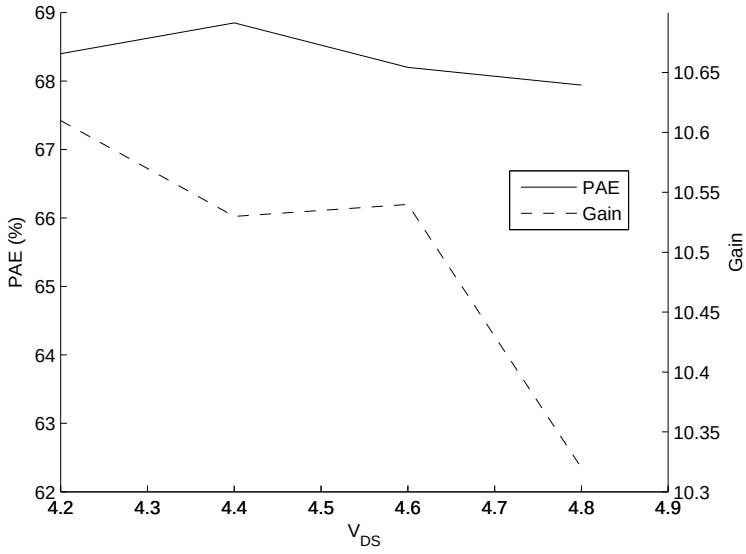

Figure 7-4: PAE and P_{out} vs. P_{in}

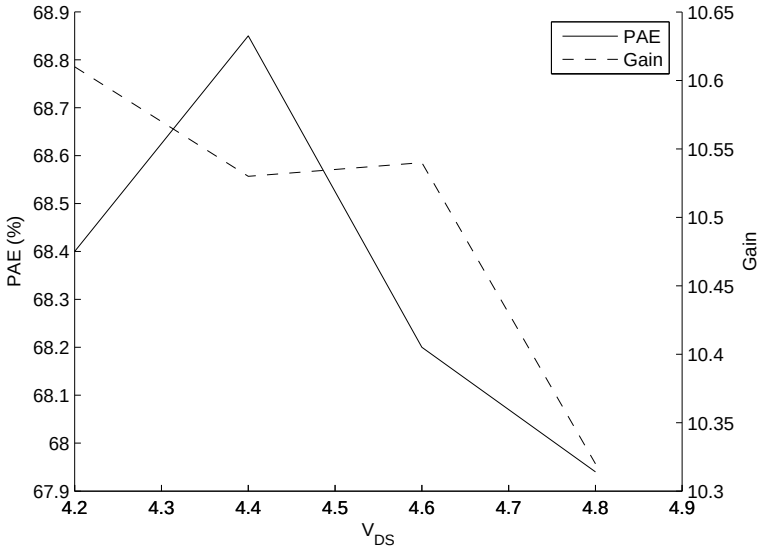

Figure 7-5: PAE and Gain vs. V_{DS}

picion. At 68.85%, the peak PAE achieved by the amplifier was a full 22.15% higher than the PAE of 46.8% achieved in simulation. The margin is really too large for meaningful comparison. Ultimately, it seemed as though the device model sorely underrepresented the gain achievable by the device, which led to very low PAE results. When biased for maximum efficiency, the simulated amplifier only provided 8 dB of power gain, compared to 10.53 dB provided by the actual amplifier. While the gain of 10-11dB achieved by the amplifier was a slight disappointment, it far exceeded the expectations set by the simulations.

The high PAE achieved in the amplifier suggests that the model did provide some meaningful information about what impedances to present the device with for optimal PAE. It is also possible that the design was successful despite the inaccurate model simply because switching mode amplifiers tend to be tolerant of device variations. However, the large gains in PAE achieved through tuning the harmonic stubs suggest that small changes in transmission line dimensions can significantly impact PAE. It stands to reason that an accurate device model could be used to produce an amplifier with very finely tuned input and output networks, and that such an amplifier would achieve even higher PAE and gain than the one described here.

Chapter 8

Conclusion

The ATF511P8 enhancement mode pHEMT from Agilent shows great promise for use in high efficiency RF power amplifiers in MCMs. A PCB design using the device has been presented, demonstrating 68.9% PAE at 30.0 dBm output power. Past pHEMT designs executed at Draper using pHEMT devices achieved 70-75% PAE at 30 dBm. These designs achieved around 15 dB of power gain, which is higher than the 10.5 dB of power gain achieved around maximum PAE for our design. However, the E-pHEMT brings with it the system level benefits of only requiring a single voltage supply. This eliminates the need for power supply sequencing circuitry and DC-DC conversion circuitry for the gate bias, reducing system area and complexity.

Moreover, the PCB E-pHEMT amplifier design was completed without an accurate model of the device. The extent to which the inaccuracies of the model stood in the way of achieving optimal efficiency is unclear. It is likely that a device model yielding accurate gain and PAE data for Class E and Class F operation could be used to design an amplifier achieving better gain and even higher efficiency than the 68.9% achieved here.

Thus, the first step in designing a high efficiency amplifier for an MCM should be having the ATF511P8 accurately modeled for gate bias voltages around V_P. Past Draper designs have employed a company called Modelithics for transistor modeling, and excellent agreement between simulations and experiments has been observed.

If the Draper MCM-D process can be improved to allow metal patterning on the

alumina substrate, then an unbalanced stripline transmission line structure should be used for the amplifier. This geometry will result in short line lengths and reasonable line widths. If a reduction in the substrate thickness from 25 mils to 10 mils is possible, then an embedded microstrip structure should be used. This structure allows further reduction in line length over the unbalanced stripline geometry while maintaining reasonable 50Ω line widths. The result will be a small, compact transmission line structure that will fully take advantage of the reductions in area and volume made possible by the MCM process.

The use of a thermal via under the die will be beneficial to a successful design. GaAs devices have low thermal conductivity in general, and the ATF511P8 is certainly no exception. However, our analysis of the ATF501P8 die in chapter 3 suggests that thermal vias will allow the 511P8 to operate well below its maximum channel temperature in an MCM with a long mean time to failure.

We have also shown that parasitic effects of die connections can be reduced in an MCM. One possible benefit of this reduction might be increased stability. A chief cause of instability in power amplifiers is inductance in the connection from the source to ground, which should be reduced by up to a factor of 10 in the MCM. Indeed, stability was an issue in the PCB amplifier. Beyond possibly reducing instability, it is difficult to tell what effect parasitic reductions will have on amplifier performance and more specifically on PAE. This is another question that could potentially be answered with the help of an accurate model of the transistor.

The demand for small, efficient RF power electronics for communication devices is ever increasing. The analysis in this thesis strongly suggests that multi-chip modules provide a way to meet this demand. A high efficiency PCB power amplifier design has been demonstrated, and analysis has been performed to show that translation of the design onto a multi-chip module is not only possible, but may also yield performance improvements.

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