Copper Wafer Bonding in Three-Dimensional Integration

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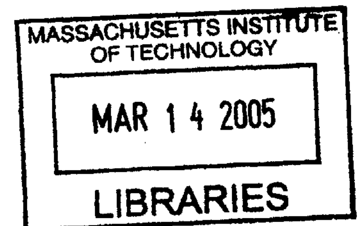

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Abstract

Three-dimensional (3D) integration, in which multiple layers of devices are stacked with high density of interconnects between the layers, offers solutions for problems when the critical dimensions in integrated circuits keep shrinking. Copper wafer bonding has been considered as a strong candidate for fabrication of three-dimensional integrated circuits (3-D IC). This thesis work involves fundamental studies of copper wafer bonding and bonding performance of bonded interconnects.

Copper bonded wafers exhibit good bonding qualities and present no original bonding interfaces when the bonding process occurs at 400°C/4000 mbar for 30 min, followed by nitrogen anneal at 400°C for 30 min. Oxide distribution in the bonded layer is uniform and sparse. Evolution of microstructure morphologies and grain orientations of copper bonded wafers during bonding and annealing were studied. The bonded layer reaches steady state after post-bonding anneal. The microstructure morphologies and bond strengths of copper bonded wafers under different bonding conditions were investigated. A map summarizing these results provides a useful reference on process conditions suitable for three-dimensional integration based on copper wafer bonding.

Similar microstructure morphology of copper bonded interconnects was observed to that of copper bonded wafers. Specific contact resistances of bonded interconnects of approximately 10^{-8} Ω-cm^2 were measured by using a novel test structure which can eliminate the errors from misalignment during bonding. The bonding qualities of different interconnect sizes and densities have been investigated. In addition to increasing the bonding temperature and duration, options such as larger interconnect sizes, total bonding area, or use of dummy pads for bonding in the unused area improve the quality of bonded interconnects.

Process development of silicon layer stacking based on Cu wafer bonding was successfully applied to demonstrate a strong four-layer-stack structure. Bonded Cu layers in this structure become homogeneous layers and do not show original bonding interfaces. This process can be reliably applied in three-dimensional integration applications.

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Chapter 1

Introduction

1.1 Motivation

In order to extend integrated circuit (IC) performance beyond device and interconnect scaling limits, new integration approaches are being explored. Interconnect performance will become more dominant in the system performance of integrated circuits (ICs) as the critical dimension in integrated circuits keeps shrinking [1]. For the purpose of meeting the projected system performance demands, innovative system architecture or new interconnect materials need to be developed. Although new interconnect materials and low-K materials offer improvements in system performance, their contributions are limited. A novel design of system concept, architecture, and fabrication technologies will be required in order to significantly improve and even solve problems such as signal delays [2] by keeping the wire-length short at a high clock speed [3-7]. Three-dimensional (3D) integration, in which multiple layers of devices are stacked with high density of interconnects between the layers, is an attractive candidate for a source of

solutions for these problems [8, 9].

1.2 Three-dimensional (3D) Integration

The concept of three-dimensional integration was first proposed in the 1980s [10-12]. Three-dimensional integration provides more functionalities within a smaller footprint, and may further reduce chip size [8]. This advantage is especially attractive for wireless and military applications. In addition, for integrated circuits, performance such as signal delay and clock skew can be effectively improved with a reduced total interconnect length in three-dimensional integration [13-16]. Thus, the wire length between microprocessor and memory can even be greatly reduced by using three-dimensional integration. Finally, flexibility in device technology and materials selection is also provided through the parallel processing of separate layers or wafers, which are finally stacked together using three-dimensional integration fabrication. Therefore, it becomes possible to stack analog and digital design on different layers together, or optoelectronic and electronic devices on different material substrates together.

Three-dimensional integration can usually be divided into two categories: 3D packaging and 3D IC. 3D packaging is the stack of dies or multi-chip modules (MCM) [17, 18]. In fact, 3D packaging is the idea for decreasing the wire length of chip-to-chip. Some concepts of 3D packaging propose that the total interconnect density can be higher by conducting vertical through-hole vias [19, 20]. Today packaging companies are pushing this concept from R&D to manufacturing. 3D IC, which offers layer-to-layer (level-to-level) interconnect connections, provides even shorter wire-length than 3D packaging. This thesis focuses on the wafer level of three-dimensional integration,

especially possible applications for 3D IC.

For wafer level 3D integration, sequential and parallel approaches have been proposed to fabricate devices [21]. The purpose of these approaches is to build a vertical silicon layer stacking with strong structure and reliable performance. Sequential approaches are that layers with devices are fabricated sequentially [22-23]. The process starts with the first device layer on the substrate, then second layer is formed on the top of first layer and devices are fabricated. This process can be repeated for the sequent layers. Several sequential approaches have been proposed based on recrystallization [9, 24], metal-induced lateral crystallization [25-30], germaniem seeded laterally crystallizated technologies [31-32], and epitaxy growth [33] to form another Si layer on the top of device layer. There are two major drawbacks in sequential approaches. One is the performance of upper device layer may be reduced because of the bad quality of polycrystalline silicon for the upper layer. The other one is the issue of thermal cycling during fabrication may degrade the performance of devices as well. Although the first drawback recently can be improved by seeded laterally crystallizated technologies to form a single grain to avoid the defect problem [31-32], thermal cycling, which may introduce large stresses in the structure, is still a major concern while applying this technology for 3D applications.

While sequential approaches still have concerns to overcome, parallel approaches offer another choice to solve this problem. Parallel approaches to achieve three-dimensional integration are usually based on bonding of separate wafers together combining a process of substrate removal or layer transfer [34]. Therefore, the upper device layers can be fabricated separately. Afterwards, the upper layers can be transferred on the top of bottom layer by bonding. The choice of bonding materials depends on

different fabrication approach. Silicon-to-silicon [35-36], metal-to-metal [37-40], and polymer-to-polymer [41-47] are potential candidates. One big challenge of the approaches with wafer bonding is to achieve a strong bond strength and quality and at the same time the bonding conditions should be compatible to the underlying device layers.

While three-dimensional integration has several significant potential advantages over other monolithic techniques, challenges, such as alignment, process reliability, thermal stress and heat transfer exist [48-50]. Among these challenges, process reliability is one of the most significant. In addition, in order to implement a variety of applications, three-dimensional integration should stack and interconnect more than two layers. Therefore, a reliable process is key to achieve a high number of stacking layer structure in three-dimensional integration.

1.3 MIT Three-Dimensional Integration

The MIT three-dimensional integration is based on direct Cu-Cu wafer bonding at low temperature [40]. Device wafers, with Cu interconnects for electrical connectivity and Cu pads for structural support, are sequentially bonded each other in a face-to-back approach using Cu-to-Cu low temperature thermal compression.

The process flow for fabricating monolithic 3-D ICs is illustrated in Figures 1-1(a) and (b). The significant steps shown in Fig. 1-1(a) are described as followed:

1. Fabrication of device layers on a SOI Si wafer.
2. In order to stack the device layer on the top of another device layer, the substrate of SOI wafer has to be thinned by grinding and etching process. During the grinding process, for the mechanical support reason, a handle wafer is attached to the SOI

wafer under three requirements: (a) the adhesion of handle wafer and SOI is strong enough to withstand the stress during grinding, (b) the adhesion is inert to the solution using in etching SOI substrate process, and (c) the adhesion can be removed by a solution easily, but the solution does attack other materials in the structure.

The handle wafer is prepared by coating silicon nitride on both sides of Si wafer to protect the structure from future etching process. Then Al and Cu films are sequentially deposited on both the handle wafer and SOI wafer. After bonding handle wafer and SOI wafer by Cu-Cu bonding, the handle wafer is attached.

3. The thin back process to remove the Si substrate of SOI wafer is a combination of mechanical grindback and chemical etching, which will stop on the buried oxide of SOI. The chemical etching solution can be either KOH or TMAH [51, 52].
4. Once the completion of the removal of SOI substrate, inter-vias are created by etching the oxide, SOI and ILD.
5. The PECVD oxide sidewall passivation and via filling using damascence are performed.
6. Cu interconnects are deposited on the top of vias for electrical connectivity. In additions, dummy Cu pads can be also patterned to increase the bonding strength of the whole structure. To this step, the device layer attached to the handle wafer is treated as upper wafer for the next bonding process.
7. Fabrication of device layers, including the patterning of Cu interconnects and pads, on a bulk Si wafer. This bulk Si wafer with device layer is treat the bottom wafer. Then the upper wafer and bottom wafer is aligned and bonded at the desired bonding condition. The detailed alignment and bonding process will be described in Chapter 2.
8. Handle wafer release is the final step of the 3-D integration process. By soaking the

bonded wafer in the HCl solution, Al film will be dissolved in HCl but at the same time all other materials are inert to the solution [53]. Therefore, the handle wafer will separate from the bottom wafer. The device layer attached to the handle wafer will be remained bonding to the device layer of the bottom wafer.

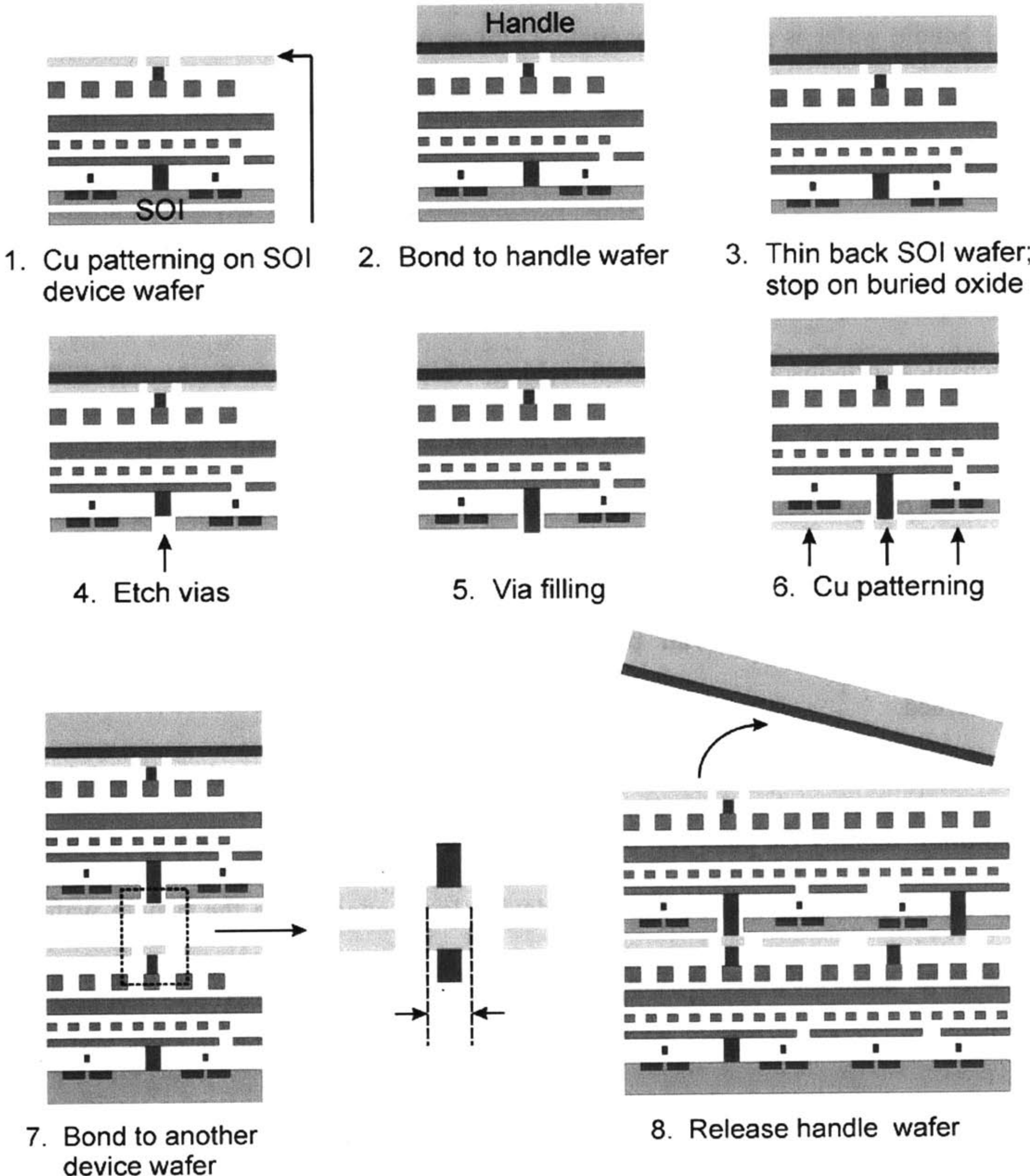
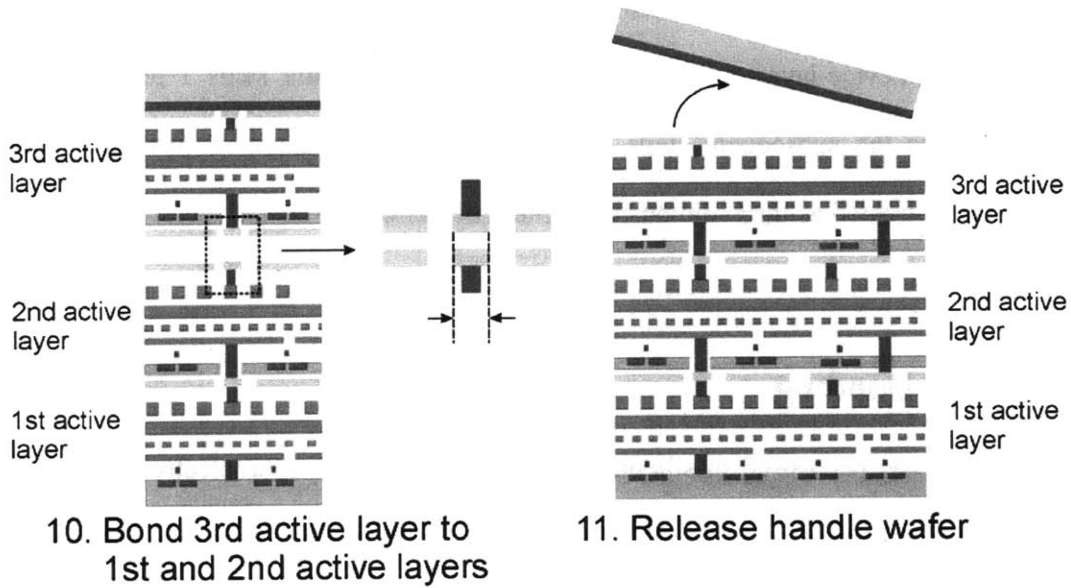


Figure 1-1(a) MIT process flow for fabricating monolithic 3-D ICs

9. Repeat process #1 ~ #6 for 3rd active layer



12. Repeat process #1 ~ #6 for 4th active layer

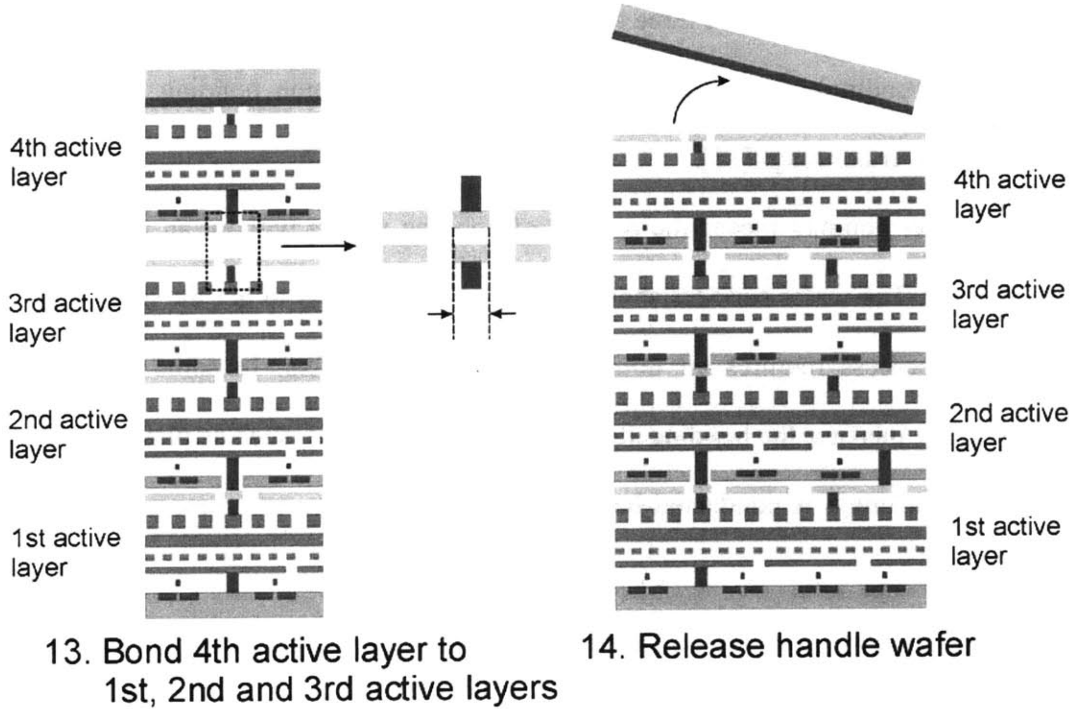


Figure 1-1(b) The subsequent steps for a four-active-layer stacking structure

Two device layers are successfully bonded after step 8. If more than two device layers are required, this two-bonded-device-layer wafer can be treated as the bottom wafer and third-device-layer wafer can be prepared by repeating steps 1 to 6. Figure 1-1(b) illustrates the subsequent steps for a four-active-layer stacking structure. This structure can be treated as three-dimensional integrated circuits.

1.4 Wafer Bonding

Wafer bonding has been used in silicon on insulator (SOI) and microelectromechanical systems (MEMS) applications [34, 39]. In addition, wafer bonding is a key technology for development of three-dimensional integration [39, 40]. The ability of wafer bonding to create a good bonding quality across the wafer enables the possibility of heterogeneous integration of devices. There are three types of wafer bonding: direct wafer bonding (also called fusion bonding), anodic bonding, and thermocompression bonding (also called intermediate-layer bonding) [34].

Direct wafer bonding means the process of bonding wafers without an intermediate adhesion layer. The wafer surfaces should be kept clean and flat to get the best bonding quality. The process requires an initial contact of two wafers. In some cases, heat treatments may increase the bonding strength. Surface treatment, such as plasma etching, and solution cleaning, is conducted before the bonding process to promote the surface attraction.

Anodic bonding involves one silicon wafer and one glass wafer that has alkali metals. This process is completed by the application of an electric field between the two wafers at temperatures ranging up to 500 °C. Attention is paid to ensure the same range

of thermal expansion coefficients of glass and silicon.

Thermal-compression bonding using an intermediate layer such as metal films has been used in packaging level applications [46, 47]. Solder bonding for wiring bonding during the packaging process is the typical example [40]. In addition, eutectic bonding that utilizes the eutectic properties to create a reliable bond during bonding is proposed in Su and Au thin film applications. For wafer level bonding, thermalcompression bonding enables the connections of different wafers via metal line bonding with short distances.

Wafer bonding has attracted a lot of attention for future device applications, especially the potential benefits of high performance, compact size, and low cost. In order to achieve these benefits, improvements of cleanliness, alignment, vacuum and yield of the bonding facility is the first topic. Potential material issues, such as stress and defects, need to be solved as well. These challenges are significant before wafer-bonding technology becomes a production technique.

1.5 Advantages of using Cu as the bonding material

Because integrated circuit interconnect dimensions keep shrinking, copper is a promising candidate of interconnect metallization materials for advanced electronic applications to replace aluminum. Since copper has higher electrical conductivity than aluminum, and the thermal conductivity ratio of copper and aluminum is approximately 2:1, copper can improve the electrical performance, reduced Joule heating, and better heat transfer. The electromigration problem in copper should be less than in aluminum since copper has the higher melting point [54]. Therefore, copper is rapidly developing into the material used in mainstream interconnect technologies.

As mentioned in previous sections, there are several bonding materials for three-dimensional integration. Each bonding material has a different specific bonding approach. For some approaches using silicon or polymer as bonding materials, blank oxide or polymer is deposited on the top of the active layer of each wafer without any patterns. Then after bonding the wafers together, a subsequent etching process to define through-hole vias, which penetrate the whole wafer, is performed. Finally vias are filled with copper. Since the aspect ratio of via is too big, it is difficult to perfectly fill the vias and control the cleanness condition in the bottom of the vias. These two concerns bring issues, such as open circuits and high contact resistance, respectively.

Copper wafer bonding in three-dimensional integration patterns the copper interconnects individually on separate wafers, and then bonds them together. The thickness of Cu layer used in this thesis is 300 nm. Thus the issue of filling the vias with copper due to high aspect ratio in this approach does not exist.

Moreover, compared to oxides or polymers with poor thermal conductivities, copper has an excellent value and thus the copper bonded layer can act as a heat conduit. Besides, the bonded layer can be treated as another metal layer while other approaches do not have this advantage. Finally, copper bonding offers not only the electrical connectivity but also mechanical support. In addition to copper interconnects, an idea to place copper dummy pads in the used areas to increase the mechanical strength is proposed and will be further discussed in Chapter 11.

Based on the above discussions, copper as the bonding material in three-dimensional integration has advantages in different areas and is a promising candidate to fulfill three-dimension integration applications.

1.6 Research Goal and Contribution of Thesis Work

Three-dimensional integration promises to improve circuit performance while device scaling faces fundamental limitations. Since the application of three-dimensional integration has to be based on current semiconductor process technologies, while using copper wafer bonding, compatible process parameters such as the highest process temperature and pressure need to be considered to avoid the destruction of device structure or the degradation of circuit performance. Selection of solutions in subsequent etching processes to avoid the reaction with existing device materials is significant as well.

Since the bonding material is copper, the source of structure strength in three-dimensional integration is based on the result of copper bonding. Copper bonded interconnects are also the media for electrical current to pass through. The electrical performances such as contact resistance may be influenced if copper bonding is not satisfactory.

Moreover, three-dimensional integration is used for the device applications. The expense of the bonding process should be kept as low as possible. A long bonding process, which increases the total process time of a device, is not an acceptable solution for industries.

The research goal, based on the above discussions, is to develop a reliable copper wafer bonding in three-dimensional integration. Copper bonding should have strong bond strength and excellent electrical performance. In the bonding process, temperature should be as low as possible and duration should be as short as possible. Bonding temperature, pressure and any other parameters cannot affect the existing materials or cause a worse

circuit performance.

This thesis work involves fundamental studies of copper wafer bonding and bonding performance of bonded interconnects. In addition, process development of silicon layer stacking based on copper wafer bonding is applied to demonstrate a strong four-layer-stack structure. This process development can be reliably applied in three-dimensional integration applications. Based on the results of research works including bonding quality and bonding parameters, bonding conditions with different considerations are suggested for applications.

1.7 Thesis Organization

The outline of this thesis work is as follows:

Chapter 2 of this thesis describes the detailed bonding process and other experiments that were frequently used. Other experiments for bonding interface observation, material property measurements, and bonding quality investigations are described as well.

Chapter 3 reports the initial results of copper wafer bonding using razor test. The results offer information for initial bonding condition selection in this thesis.

In Chapters 4, 5, and 6, the bonding interfacial morphologies with different bonding conditions are studied. Detailed microstructures, material properties, and evolution of bonded layer are also investigated.

Chapter 7 studies the bonding quality and bonding strength using different techniques. Based on the results in previous chapters, a map summarizing the bonding quality is established.

In Chapter 8, effects of wafer bow on bonding quality are investigated. In the end of the chapter, criteria are provided for future wafer selections.

In Chapters 9, 10, 11, and 12, the research field of copper wafer bonding is moved from blank copper wafer bonding to bonded copper interconnects. In chapter 9, microstructures of copper bonded interconnects are observed.

Chapter 10 and 11 report the contact resistance measurement and bonding quality of copper bonded interconnects, respectively. A novel design of test structure for contact resistance measurement is described. Sizes of interconnect, total bonding area, and the uses of dummy pads are factors to affect the bonding quality.

Chapter 12 describes the process development of silicon layer stacking using copper wafer bonding, grind back, and etch back. Morphology investigation and possible issues are discussed as well.

Chapter 13 summarizes the results of the study including bonding quality and bonding parameters. In the end, suggestions of bonding conditions are made for applications.

Chapter 14 includes the summary of this thesis work and future work.

Chapter 2

Bonding Process and Other Description of Experiments

This chapter describes the detailed bonding process and other experiments that this thesis frequently uses. The description starts with the initial wafer selection and surface cleaning preparation. Procedures of metal deposition, metal surface cleaning prior to bonding, detailed bonding and anneal procedures are described as well. The last section describes different techniques to investigate bonding morphology, materials properties, bonding strength, and electrical performance measurement. Specific experimental procedures for different project will be described separately in each chapter.

2.1 Initial Wafer Preparations

Single crystal, n-type (2-3 Ω-cm) and p-type (8-12 Ω-cm), 4-inch (001)-oriented silicon wafers were used in the present study. Before the next process, surfaces of Si wafers were cleaned to remove native oxides and particles. The cleaning process was carried out with a wet bench. The wafers were first cleaned in a solution A (H_2SO_4 : H_2O_2 = 3 : 1) for 10

min at 120°C to grow a thin layer of SiO_2 which was etched away by immersing the wafers in a dilute HF solution (HF : H_2O = 1 : 50) followed by a de-ionized water rinse. Next the wafers were cleaned by a solution B (NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5) for 10 min. at 75°C and dipped in a dilute HF solution (HF : H_2O = 1:50) followed by a de-ionized water rinse. Then the wafers were cleaned by a solution C (HCl : H_2O_2 : H_2O = 0.25 : 1 : 5) for 10 min at 75℃ and dipped in a dilute HF solution (HF : H_2O = 1 : 50) followed by a de-ionized water rinse. Finally, the wafers were dried in a spinner.

2.2 Thin Metal Films Deposition

The metal films were evaporated with an AIRCO Temescal STIH-270-1 electron gun evaporation system with maximum power about 7 kW. The electron beam, accelerated by a voltage of 8.2 kV, was directed onto the hearth by means of a magnetic field that bent the beam 270° downward. During the evaporation, the top layer of the source in the crucible was melted and evaporated onto substrates by the electron beam. The source crucible was water-cooled to prevent the contamination of the source by crucible materials or other impurities. The thickness and rate of deposition could be read directly from the display of a microprocessor unit connected with a quartz sensor produced by INFICON. The accuracy of the measurement was about 0.1 nm.

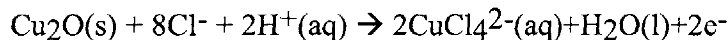
The vacuum system used is an AIRCO Temescal model BJT-1800 system, which is equipped with a 6-inches diffusion pump and a liquid nitrogen cold trap. Optimum vacuum of 1×10^{-7} Torr was attainable. During deposition, the vacuum was maintained to be better than 1×10^{-6} Torr. The deposition rate was about 0.3 nm/sec.

In this experiment, 300 nm Cu and 50 nm Ta films were deposited with an electron

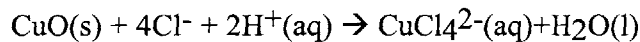
beam deposition. The Ta layer acts as a Cu diffusion barrier up to 550°C [55].

2.3 Copper Surface Cleaning

In previous studies, surface preparation for metal-to-metal bonding is an important factor to achieve a good bond [56]. In this research, metal surfaces of some wafers were cleaned prior to bonding. Wafers needing removal of surface oxides after Cu deposition were dipped in 1:1 (by volume) H_2O:HCl for 30 s followed by a DI water rinse and spin dry. Any native oxide on the Cu surface should be removed through this process. Reactions for HCl and surface oxides are shown as follows [57]:



$$Cu_2O(s) + 8Cl^- + 2H^+(aq) \rightarrow 2CuCl_4^{2-}(aq) + H_2O(l) + 2e^-$$



$$CuO(s) + 4Cl^- + 2H^+(aq) \rightarrow CuCl_4^{2-}(aq) + H_2O(l)$$

In Section 2.1, the cleaning of silicon surfaces ensures high quality and clean surfaces without particles prior to the deposition process, while the cleaning of copper surfaces is to create clean metal surfaces before bonding process.

2.4 Optical Wafer-Wafer Alignment

The bonding targets belonging to separate wafers need to be aligned before bonding in order to acquire the accuracy of circuit placement. This alignment is especially important when the dimension of bonding media is small. Any misalignments will cause the decrease of bonding strength and failure of circuits.

The alignment process was carried out in Electronic Vision EV 620 Aligner. It

started by clamping two wafers together face-to-face, with the wafers separated by three 30-μm metal flaps on the bonding chunk. Afterwards, the chuck with the wafers is ready to bond. Figure 2-1 shows the schematic diagram of alignment procedures [58].

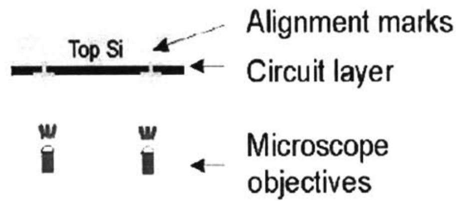
2.5 Bonding Process

The bonding process was carried out in the Electronic Vision AB1-PV bonder. The chuck with the wafers was placed in the EV bonder. The N_2 was purged before the chamber was evacuated to 10^{-3} torr. A 300-mbar force was then applied at the center of the top wafer while the flaps were pulled. When the wafers were in full contact, a 1000-mbar force was applied while both wafers were being heated at a rate of 40°C/min. Once the temperature reached the desired bonding temperature, a 4000-mbar force was applied for the desired bonding duration. Afterward, it required 2 hours to cool the wafers to room temperature.

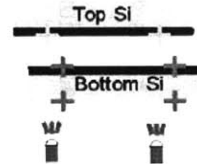
2.6 Anneal

Bonded wafers needing further annealing were placed in a diffusion furnace in N_2 ambient at the desired anneal temperature and duration.

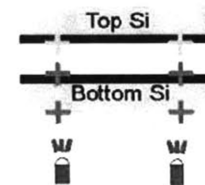
Physical



1. Insert top wafer, circuit-side down

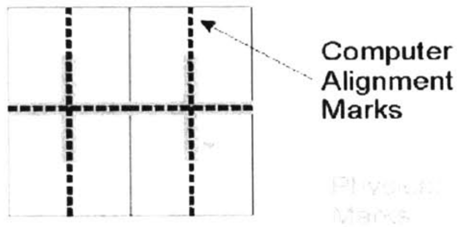


2. Insert bottom wafer, circuit-side up. Wafers are separated by three - 30 μm metal flap

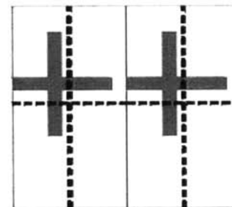


3. Align bottom wafer to computer marks

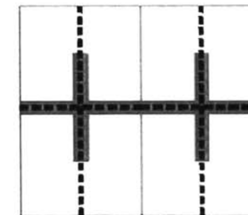
Aligner CRT Display



1. Align computer generated marks to physical marks



2. Bottom wafer mis-aligned



3. Both wafers aligned

Figure 2-1 The schematic diagram of alignment procedures [58]

2.7 Bonding Strength Examinations

2.7.1 Dicing Test

The dicing process is the tool to examine the bonding strength of Cu bonded wafers. Bonded wafers were cut into 5mm x 5mm square dies at a speed of 0.69 mm/sec by a DAD-2H/6T Automatic Dicing Saw. If the bonded piece separates after dicing, the bonding strength is qualitatively decided.

2.7.2 Tape Test

Surviving bonded pieces after the dicing test underwent the tape test. The 3M Scotch 3710 Adhesive Tape was stuck on the bonded pieces. Then force by hands was applied to rip the tape from the piece. If the bonding strength is larger than the adhesion between the adhesive tape and piece, the tape will separate from the piece. If the bonding strength is smaller than the adhesion between the adhesive tape and piece, the piece will break from the bonding interface and the tape will remain stuck to one of the separating pieces.

2.7.3 Pull Test

Surviving bonded pieces after dicing test underwent the pull test by a Guad Group Romulus III Pull Machine. One side of the bonded piece was loaded on the substrate of the machine, while the other side was glued to a pin with Epoxy. During the pull test, the machine pulled the pin until the sample broke. The force at the failure of the sample was recorded.

2.7.4 Shear Test

Surviving bonded pieces after dicing test underwent the shear test by a Dage Series 4000 Shear Machine. The bonded piece was first loaded on the substrate of the machine. Then a board perpendicular to the substrate was raised to a "shear height" of 600 μm. Shear height means the distance between the bottom of the bonded piece to the bottom of the board. During shear test, the board pushed the upper part of the bonded piece until the sample broke. The force at the failure of the sample was recorded.

2.8 Scanning Electron Microscope Observation

The morphologies of copper bonded wafers, which present grain structures, defects, and bonding interface, were observed with a JEOL 6320FV Field-Emission High-Resolution Scanning Electron Microscope (SEM).

2.9 Transmission Electron Microscope Observation

2.9.1 Cross-Sectional Specimen Preparation

XTEM samples were prepared by a modified Sheng's method [59]. The step-by-step procedures are described as follows:

1. The samples were cut into 3 mm x 2 mm rectangular pieces.
2. The pieces were lapped from the back surface to a thickness less than 60 μm.
3. The samples were stacked face to back and bonded together with epoxy. A special

holder was used to squeeze out the epoxy so that only a thin layer of epoxy, about 0.1 mm in thickness, was left between the samples. Two protective silicon wafers were also cut into 3 mm x 2 mm rectangular pieces and bonded together with the samples.

4. Stack was then mounted on a blank silicon piece.
5. Sample assembly was polished sideways sequentially by 1200-grit abrasive paper, 15 μm and 3 μm diamond pastes.
6. The polished surface of the stack was then mounted with a thin layer of CRYSTAL BOND on a glass piece.
7. The new specimen assembly was then lapped from silicon side to less than 10 μm thick using, in succession, 400-, 800-, 1200-grit abrasive papers and 3 μm diamond paste.
8. A copper mesh, 3 mm in diameter, was bonded by epoxy to the sample stack.
9. The silicon material and wax outside the boundary of copper mesh were removed with tweezers.
10. The CRYSTAL BOND was dissolved with ACE. Sample stack with copper ring was then detached from the glass piece. Finally, the exposed side of the sample was bonded by epoxy to another copper mesh.
11. Both surfaces of the sample stack were milled by argon ions until a hole developed near the center of the sample. The argon ion energy, milling angle and ion current were 5-6 keV, 12-15° and 50-200 μA, respectively. It should be noted that during the ion milling process, the samples were kept below 120 °C to avoid grain growth [60].

2.9.2 Transmission Electron Microscope Observations

A JEOL-200CX scanning transmission electron microscope (STEM) and JEOL-2010 transmission electron microscope operating at 200 kV were used for conventional TEM examination. Most of the micrographs were taken under two beam diffraction conditions with deviation parameter S_g slightly positive. Most of the XTEM micrographs were taken along [110] zone axis of the Si substrate.

2.10 Energy Dispersion Spectrometer (EDS) Analysis

Energy Dispersion Spectrometer (EDS) Analysis, a Link ISIS energy dispersive analysis of the X-ray instrument attached to the JEOL-2010 TEM, was used to determine the compositional distribution of oxidation in local areas of samples in the Cu bonded layers [59]. Various beam sizes and a process time of 100 sec were chosen for EDS analysis for the samples.

2.11 Atomic Force Microscope (AFM) Observation

The surface morphologies and surface roughness of Cu films with or without any surface treatment before bonding were examined with an Autoprobe CP atomic force microscope (AFM).

2.12 X-ray Diffraction (XRD) Analysis

The crystallography, which is also grain orientation, of the Cu bonded layer after different bonding condition was analyzed by X-ray diffraction (XRD) [Rigagu D/Max] with Cu Kα radiation.

2.13 Wafer Bow Measurement

Wafer bow is obtained from the measurement of the overall magnitude of wafer curvature, and usually means the height deviation between the center of the wafer and the edge of the wafer. Wafer bows were measured using a KLA-Tencor thin film stress measurement. This equipment can be operated at different temperature.

2.14 Electrical Properties Measurement

A four-point probe station was used to stress current and measure the voltage drop of the testing samples. An HP 4156 Semiconductor Parameters Analyzer was used to ramp a current between 1 mA and 100 mA on the test structures.

Chapter 3

Initial Results of Copper Wafer Bonding

In order to successfully fabricate three-dimensional integration applications using copper wafer bonding, the quality of copper bonded wafers should be strong and able to support the structure during subsequent processes. In addition, the bonding process should not affect any existing devices in the wafers. Therefore, developing a reliable copper wafer bonding is the key role in three-dimensional integration. To achieve a reliable copper wafer bonding, the bonding quality and other properties such as material and electrical performances under different bonding parameters must be investigated. The razor test is used to examine the copper wafer bonding quality and offers the initial results for the rest of this thesis.

3.1 Razor Test

Before studying the bonding quality and bonded layer properties, initial results of copper wafer bonding were examined. Razor test is a good candidate for qualitative study. In the razor test, the strong bonding means the razor cannot penetrate the bonding interface [61]. Razor test for copper wafer bonding was developed by A. Fan in MIT to examine the bonding qualitatively [62]. The bond strengths can be categorized as follows: A good bond means the wafers are inseparable and the razor does not penetrate the bonding interface. In general, the wafer fractures are small fragments and located in the edge area. This good quality is comparable with that of silicon-silicon wafers bonded at high bonding temperature. Partial bond means the bonded wafers separate from the bonding interface completely or in large area when a large force is applied to the razor. Poor bond means the bonded wafers could separate from the bonding interface easily with a small force applied to the razor or the wafers did not bond at all [62].

3.2 Initial Test Results

According to the results reported in ref. [62], detailed bonding parameters were carefully selected for razor test. Based on the operating parameters of Electronic Vision AB1-PV bonder, the bonding temperature was from 300°C to 600°C; the bonding pressure was at 4000 mbar; and the bonding duration was 30 min. Optional nitrogen anneal after bonding was performed at the temperature of bonding for 30 min.

Table 3-1 shows results of razor test for bonded wafers with different bonding conditions. The experiment was based on the previous results of razor test on copper

bonded wafers [62]. Three or four wafers of each bonding condition were investigated.

Table 3-1 Results of razor test for bonded with different bonding conditions.

	Number of Test Wafers	Bonding Temperature (°C)	Bonding Duration (min)	Anneal Temperature (°C)	Anneal Duration (min)	Bonding Quality
A	3	300	30	N/A	N/A	Partial
B	4	300	30	300	30	Partial
C	4	400	30	N/A	N/A	Partial
D	4	400	30	400	30	Good
E	4	450	30	450	30	Good
F	3	500	30	N/A	N/A	Good
G	3	500	30	500	30	Good
H	3	600	30	N/A	N/A	Good
I	3	600	30	600	30	Good

Results of razor test show that the bonding quality increases with the increase of bonding temperature, the increase of bonding duration, and the use of nitrogen anneal after bonding. Reliable good bonding quality of copper bonded wafers can be found in the bonded wafers that were bonded at 400°C for 30 min followed by nitrogen anneal at 400°C for 30 min. The bonding quality remained as the bonding temperature was higher than 400°C. Because of the preference for low process temperature in industry, the bonding condition: "400°C bonding for 30 min at 4000 mbar plus 400°C nitrogen anneal for 30 min", with the good bonding quality at the lowest temperature in Table 3-1, was chosen for the fundamental studies in this thesis such as interfacial morphology

investigation of copper wafer bonding.

Chapter 4

Microstructures of Copper Bonded Layer

In previous section, the preliminary result of the quality for bonded wafers has been testes by the razor test. Although it shows that copper wafers can be bonded reliably as low as 400°C at 4000 mbar for 30 min and followed by a 30 min N_2 anneal at 400°C for 30 min with the test, detailed interfacial microstructure observation of the bonded layer to support this result. If the interfacial morphology shows the two copper layers are bonded, the evidence of good quality bonding is more solid. In this chapter, the microstructure morphologies and oxide distribution of copper bonded wafers at this bonding condition were examined by means of transmission electron microscopy (TEM) and energy dispersion spectrometer (EDS).

4.1 Sample Preparation and Experimental Procedures

(100) Si wafers were deposited 300 nm Cu and 50 nm Ta films were deposited with an electron beam deposition. After dipping in HCl for 30 sec, the wafers were bonded at 400°C with a 4000-mbar force for 30 min followed by annealed in diffusion furnace in N_2 ambient for 30 min at 400°C. Detailed experiments of theses processes are described in Chapter 2. The morphologies of the Cu-Cu bonded wafer interface were examined with a JEOL-200CX scanning transmission electron microscope (STEM) and JEOL-2010 transmission electron microscope. Energy Dispersion Spectrometer (EDS) Analysis, a Link ISIS energy dispersive analysis of the X-ray instrument attached to the JEOL-2010 TEM, was used to determine the compositional distribution of oxidation in local areas of samples in the Cu bonded layers. Various beam sizes and a process time of 100 sec were chosen for EDS analysis for the samples.

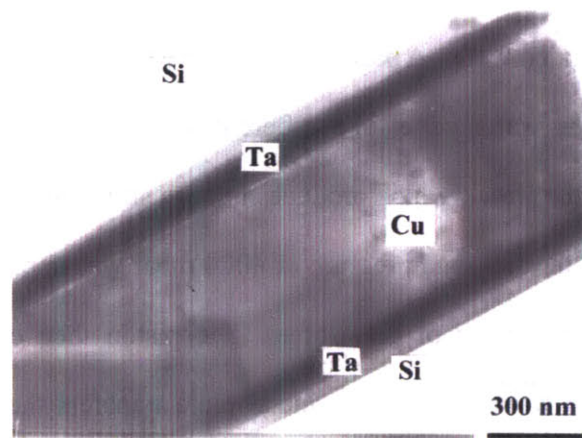
4.2 Interfacial Morphologies

4.2.1 TEM Observation

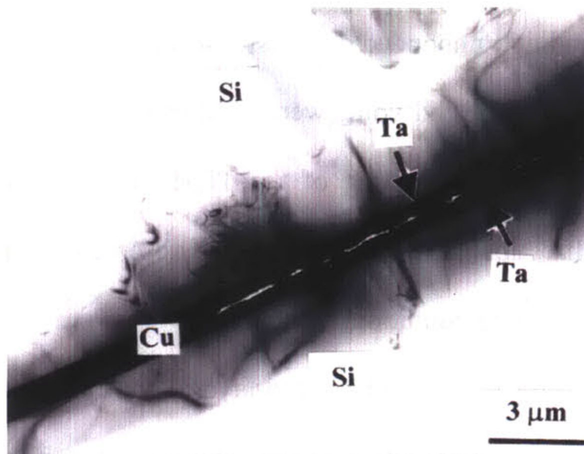
Figures 4-1 and 4-2 show the cross sectional transmission electron (TEM) images of the Cu-Cu bonded layer. This wafer was bonded at 400°C and 4000 mbar for 30 min. and then annealed at 400°C for 30 min in N_2 ambient atmosphere. In Figure 4-1, the TEM sample was taken from the center of the wafer, which shows a well-bonded layer. Random interfaces, grains, and defects are observed but no voids or vacancies are found. In Figure 4-2, however, the TEM sample was taken from near the edge of the wafer. A

mixture of good bond and unbonded areas is observed in this Cu-Cu region. The actual sizes of the voids and unbonded voids were smaller since enlargement of vacancy sites were probably caused by ion-milling of the TEM sample during sample thinning. It should be noted that this morphology is only observed once in ten TEM sample observations at this bonding condition.

The microstructures of the well-bonded layer were examined by TEM, as shown in Figures 4-3(a) and (b). The condition of the samples is the same as that in Figure 4-1. Different kinds of defects were observed: stacking faults, twins and dislocations were formed in the bonded layer with different directions. Two groups of defects with different directions are observed in Figure 4-3(b). One group is parallel to the metal layer formed along the Cu-Cu interface. The other group is continuous twins with 75 degrees respect to Si substrate that penetrates the bonded layer.



Figures 4-1 XTEM image of the Cu-Cu bonded layer. This wafer was bonded at 400°C and 4000 mbar for 30 min. and then annealed at 400°C for 30 min in N_2 ambient atmosphere. Image was taken from the center of the wafer.

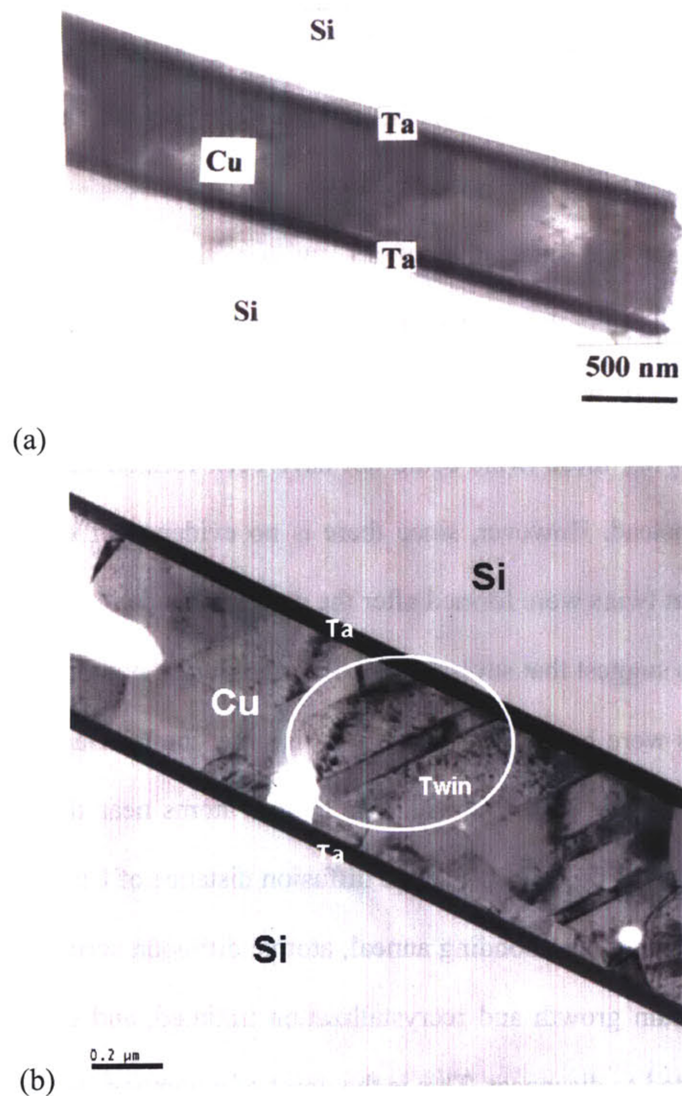


Figures 4-2 XTEM image of the Cu-Cu bonded layer. This wafer was bonded at 400°C and 4000 mbar for 30 min. and then annealed at 400°C for 30 min in N_2 ambient atmosphere. Image was taken from near the edge of the wafer.

4.2.2 Discussion

Comparing Figures 4-1 and 4-2, a good bond area with no vacancies could be obtained at the center of the bonded wafer. A partial bond area, where vacancies and good bond areas mix, occurs near the wafer edge. The different results come from the pressure profile distribution across the wafer, which produces uneven stress points during bonding. In our bonding apparatus, the full load pressure of 4000 mbar was applied to a metal plate by a piston located at the center of the wafers. The piston then creates a pressure wave emanating from the wafer center. The metal plate transfers the pressure profile to the wafers, and wafer- to-wafer contact occurs. It is reasonable to assume that the pressure applied on the edge of the wafer was less than the 4000 mbar applied at the center. Under the lower pressure, this area does not receive enough pressure to bond. Therefore, the Cu-Cu area of the edge of the wafer only could form a partial bond. Razor test results of

bonded wafers with bonding pressures less than 4000 mbar (1000, 2000, and 3000 mbar) provide the support of this assumption. Three pairs of bonded wafers were tested for each bonding pressure. From these razor test results, bonding qualities in bonded wafers with bonding pressures less than 4000 mbar were weaker than that with the bonding pressure of 4000 mbar.



Figures 4-3(a) and (b) XTEM images of the microstructures of the well-bonded layer

Figures 4-3(a) and 4-3(b) show a good bond area in the bonded wafer. Unlike the partial bond, no vacancies are observed. On the other hand, random interfaces and grains are still observed in some areas. Also, some defects, stacking faults, twins and dislocations are seen in the layer.

No bonding interface was observed in Figures 4-3(a) and 4-3(b). Interatomic bonds formed at the interface between two surface layers is speculated to be similar to the bond in the bulk in this bonding condition. This suggested that, after bonding there is no contrast visible in the TEM, which means the interface is clean and the grains have the same orientation or the interface is disappeared.

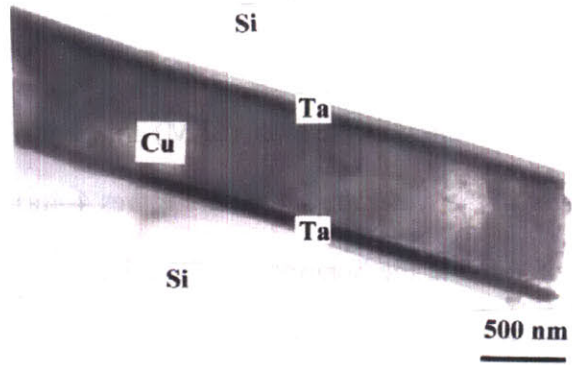
Most important and interesting of all, twins with 75 degree with respect to Si substrate were observed in the bonded layer. These twins are continuous and penetrate the bonded layer. If there were still a distinct interface or defect areas between the two original copper layers, these twins could not have been formed and would have stopped at the interface instead. However, since there is no evidence of truncated twins in this area, it implies that twins were formed after the uniform bonded layer was formed.

These results suggest that several steps occurred during bonding and annealing. First, two copper layers were bonded at 400°C. At this time, the interface between two layers should still exist but not quite defined. The copper atoms near the surface of different layers may have interdiffused because the diffusion distance of Cu atoms at 400 C for 30 min is 0.02 cm. During post-bonding anneal, atomic diffusion across the Cu-Cu interface was enhanced. Grain growth and recrystallization initiated, and the Cu-Cu interface in some regions started to disappear. This is the onset of a homogeneous Cu-Cu bond. After a homogeneous layer was formed, continuous twins could form and then penetrate the bond layer.

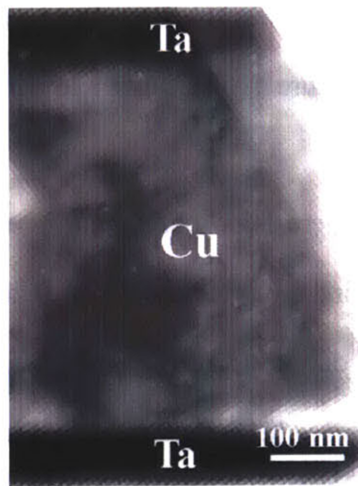
4.2.3 Types of Morphologies

Cross sectional transmission electron (TEM) images of the Cu-Cu bonded layer taken from the center of the wafer are shown in Figures 4-4(a)-(f). These pictures show a "good" bond layer formed at the bonding condition. A variety of interfaces, grains, and defects are observed, but no voids are found in the bonded layer. It is important to note that all of the morphologies shown in Figs. 4-4(a)-(f) can be repeatedly and randomly observed in any locations of bonded wafers after 30 min bonding at 400°C and 30 min nitrogen anneal at 400°C. Figure 4-4(a) shows a low magnification TEM image of Cu-Cu bonded layer.

Figure 4-4(b) shows there is no observable interface between two Cu layers after bonding. We also do not find any grain boundaries in this region. On the other hand, in Fig. 4-4(c), another kind of interface is observed: a zigzag interface with an average fluctuation depth (i.e., distance between the original interface and the grain boundary) of 30 nm. The dimension of the fluctuation depth could change drastically, up to 75 nm, as shown in Fig. 4-4(d). As shown in Fig. 4-4(c), a zigzag interface between two original Cu layers as well as grain structures in the films are observed. The intersection point of grain boundaries of the two original films at the interface is the turning point of the zigzag fluctuation. This morphology was also observed in Pt bonded layer in the paper of Shimatsu et al. [63]. A smooth interface with a smaller fluctuation depth of 5 nm is observed in Fig. 4-4(e), and no grain boundaries are observed. We also found continuous twins, oriented 75 degrees with respect to the Si substrate, penetrate the bonded layer, as shown in Fig. 4-4(f). It should be noted that no voids are observed in the interface region in these five images.



(a)



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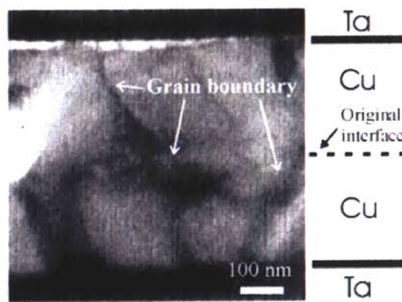
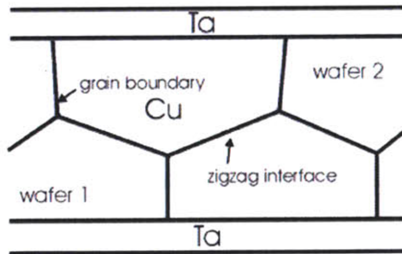
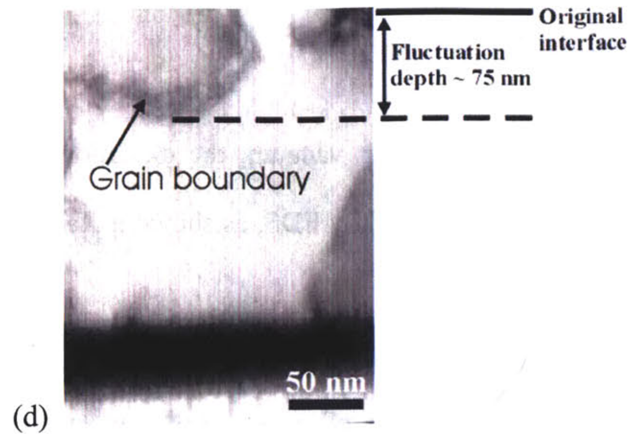
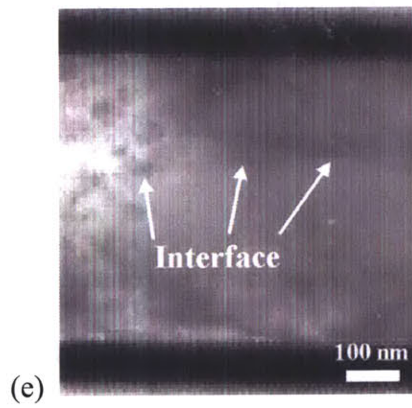




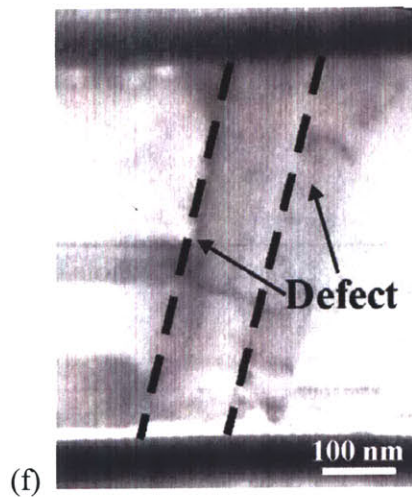
(c)



(d)



(e)



(f)

Figures 4-4(a)-(f) XTEM images of the Cu-Cu bonded layer: (a) low magnitude image, (b) no observable interface, (c) zigzag interface, (d) drastically changing fluctuation depth, (e) the smooth interface with a smaller fluctuation depth, and (f) continuous twins.

4.3 Oxide Content Examination

After HCl treatment and bonding under vacuum, the oxidation distribution in various areas of the bonded wafer was examined by EDS, as shown in Table 4-1. The tested areas are shown in Figure 4-5.

In the "good bond" layer, the quantity of oxygen in the layer is lower than 3 wt% when the beam size of X-ray is 500 nm. Furthermore, the local oxygen quantity, both in the middle of the bonded layer and near the edge of the Ta layer, is also lower than 3 wt% when the beam size of X-ray is 5 or 25 nm. In the partially bonded areas, the oxygen content at the surface, interfaces, and bonded regions were all below the detection threshold of EDS.

Any oxide in the metal line would raise the resistance and decrease the performance of the line. Since copper is easily oxidized in atmosphere at elevated temperatures, preventing oxides on the surfaces of copper layers is an important issue.

Table 4-1 EDS examination for oxygen in different areas of the bonded copper layer

	Beam Size (nm)	Oxygen (wt %)	Location Description
A	500	2.67	whole bonded layer
B	25	2.13	near Ta layer
	5	2.22	
C	25	2.53	near bonded interface
	5	2.78	
D	25	2.98	near Ta layer
	5	2.89	

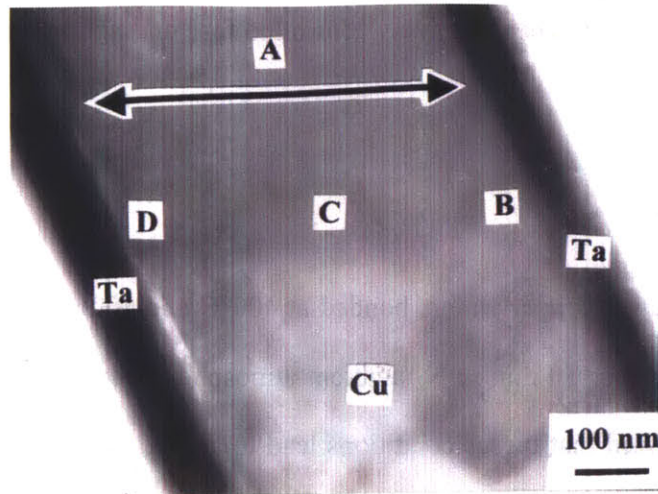


Figure 4-5 XTEM image for EDS tested areas

From the results in Table 4-1, the bonded wafer exhibits a low level of oxygen (less than 3% wt), and its concentration is uniform across the wafer. Therefore, successful bonding persists despite the presence of copper oxide; these results imply two possibilities. First: Oxides on the original copper layer were effectively removed through HCl treatment, and the remaining amount of oxides may be considered negligible during bonding. Second: Although the oxides on the original copper layer were only partially removed through HCl treatment (or new oxides formed between the HCl treatment and bonding), the oxygen atoms diffused into the layer easily and quickly and then distributed everywhere in the bonded layer under this high temperature and pressure. The diffusion distance of O atoms at 400 °C for 30 min is 0.02 cm [54]. This distance is much larger than the average Cu grain size (300 nm) before bonding and the total bonded layer thickness (600 nm). Therefore, the oxide atoms near the surface of different layers may have interdiffused because the diffusion distance of Cu atoms at 400 C for 30 min is very large. The result shows that under this condition and HCl treatment, the quantity of oxide

in the bonded layer could be effectively controlled for bonding to proceed.

4.4 Summary

The morphologies of copper wafers bonded at 400°C and 400 mbar for 30 min and then annealed at 400°C for 30 min in N_2 ambient atmosphere were examined by TEM. TEM observations showed that theses conditions lead to a good bond area in the center of the wafer. A partial bond area was formed in the edge of the wafer, probably due to a reduction of the pressure applied. Moreover, microstructures in the good bond area were studied. Different types of defects formed along the interface of the two original copper layers. Continuous twins penetrating the whole bonded layer showed that the layers became homogeneous and the bonding interface disappeared under these bonding conditions. EDS examination shows few oxidized regions in the bonded layer which are distributed uniformly.

Chapter 5

Evolution of Microstructure and Grain Growth During Bonding Process

Evolution of microstructure morphologies and grain orientations of Cu-Cu bonded wafers during bonding and annealing were studied by means of transmission electron microscopy, electron diffraction and X-ray diffraction. The bonded Cu grain structure reaches steady state after post-bonding anneal. An abnormal (220) grain growth was observed during the initial bonding process. Upon annealing, the preferred grain orientation of the whole film shifts from (111) to (220). The effects of yielding and energy minimization may are possible reasons for the evolution of the preferred grain orientation.

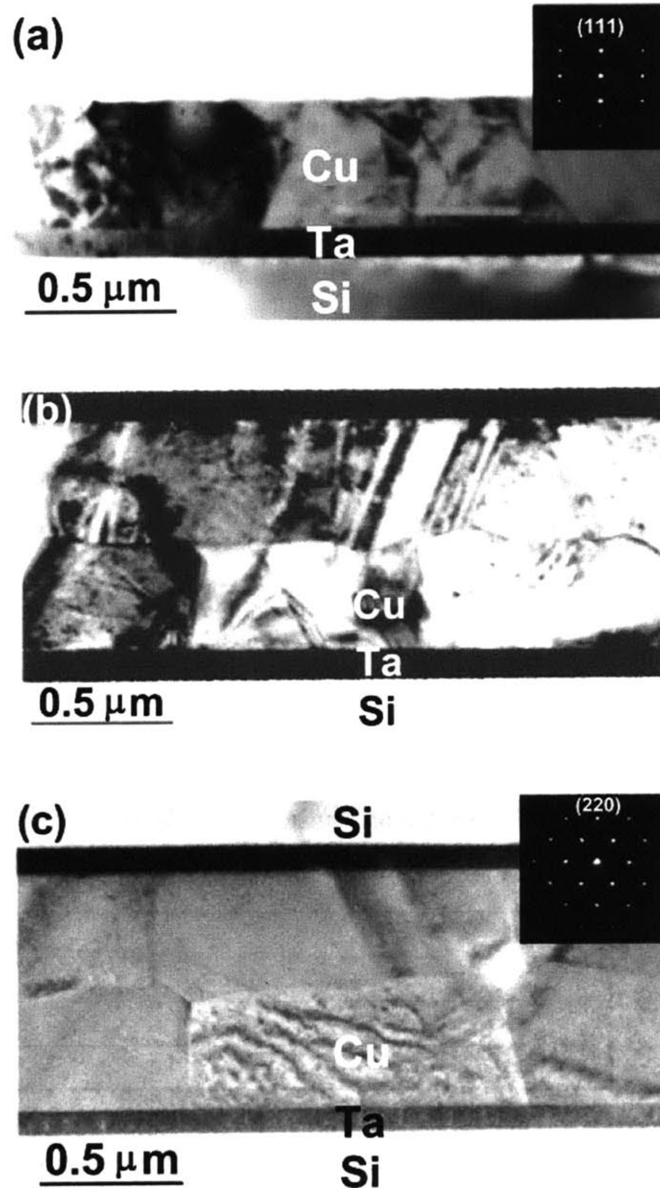
5.1 Sample Preparation and Experimental Procedures

50 nm of Ta and 300 nm of Cu layers were successively deposited on N-type (100) 4" Si wafers. The wafers were bonded under a pressure of 4000 mbar for 30 min at 400°C. After bonding, some bonded wafers were annealed at 400°C in N_2 ambient for 30 and 60 min. The morphology, diffraction pattern and grain size of bonded Cu-Cu layer were examined using a JEOL-2010 transmission electron microscope (TEM). During the TEM sample preparation, the samples were kept below 120 °C to avoid grain growth. The crystallography of the Cu film was analyzed by X-ray diffraction (XRD) [Rigagu D/Max].

5.2 Interfacial Morphologies Evolution Observation

Figures 5-1 (a)-(c) show the XTEM images of the bonded Cu-Cu layer and the major diffraction pattern of single grains from selected area: (a) before bonding, (b) after 30 min bonding, and (c) after 30 min bonding and 30 min annealing. As shown in Fig. 5-1(a), the Cu grains have an average size of 300 nm, and most grains show an (111) orientation which is similar to the results from other research [64-71]. In Fig. 5-1(b), the bonded interface is clearly observed but it is not straight. Different kinds of morphologies such as twins are present in the bonded Cu film. The distribution of grain size ranges from 300 nm to 700 nm. In addition, no major grain orientation but (111), (200) and (222) grain orientations are observed. However, after further annealing, Fig. 5-1(c) shows a well-developed grain texture with an 800 nm grain size profile and a major (220) orientation. In some area, there are even only single (220) grains existing in the bonded

layer. For each condition, five wafers were used for investigation. It should be noted that these morphologies were observed in different wafers under the same bonding condition.



Figures 5-1(a)-(c) XEM images of the Cu-Cu bonded layer and the major diffraction pattern of single grains for selective area: (a) before bonding (b) after 30 min bonding (c) after 30 min bonding and annealing

5.3 Effects of Bonding and Anneal on Microstructure Evolution

From these TEM images, it is evident that there is strong grain growth during bonding and annealing. The jagged Cu-Cu interface shows that interdiffusion between two Cu layers takes place during bonding. However, the grain growth is incomplete and the bonded layer still contains defects such as twins in the individual layer, as shown in Fig. 5-1(b). The two original Cu layers can still be distinguished. During the post-bonding annealing, the bonded layer was provided enough energy to complete the grain growth and thus achieved a stable microstructure. As a result, the two Cu layers can no longer be distinguished in Fig. 5-1(c). Figure 5-2 shows the distribution of average grain size from five wafers of each condition estimated from TEM images under different bonding conditions. There is a large distribution of grain sizes after 30 min bonding due to the incomplete grain growth. The grain growth then accelerated during the first 30 minutes of post-bond annealing. However, the grain size did not increase significantly beyond 30 minutes of annealing. This indicates that a certain amount of annealing time is required to complete the grain growth and to obtain an "intimate" Cu layer.

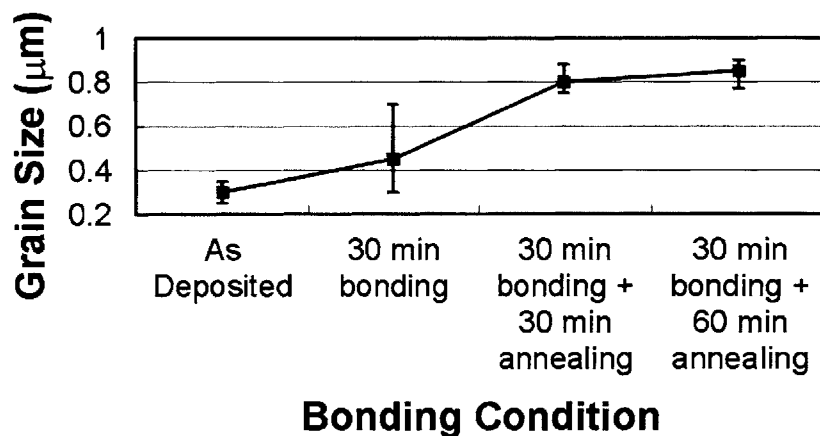
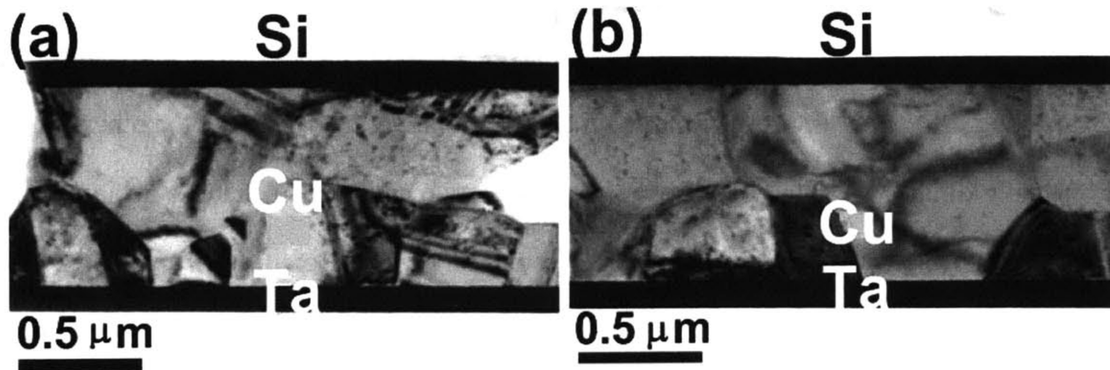


Figure 5-2 Average grain sizes as a function of different bonding conditions. Five wafers were investigated for each condition. Bar represents range of data.



Figures 5-3(a) and (b) Various of XEM images of the Cu-Cu bonded layer after 30 min bonding

It is interesting to compare the morphologies of the annealed sample (Fig. 5-1(c)) and the non-annealed ones (Figs. 5-1(b), 5-3(a) and 5-3(b)). In Fig. 5-1(b), a clear bonding interface can be observed and each layer seems to retain the similar morphologies before bonding, as shown in Fig. 5-1(a). In another sample, grains with different sizes, twins and defects are shown in Fig. 5-3(a). Both Fig. 5-1(b) and Fig. 5-3(a) show that the effects of bonding and heating are not very significant in these two areas. However, in Fig. 5-3(b), a whole grain formed in the bonded layer. This suggests that the local grain growth in Fig. 5-3(b) was much stronger than those in Fig. 5-1(b) and Fig. 5-3(a). These three types of microstructures were observed randomly across the whole wafer and on different wafers.

These three images indicate that after 30 min of bonding, grain growth saturation for the whole bonded layer is not reached yet. At this stage, non-homogeneous bonding exists throughout the wafer, possibly due to local heating non-uniformity. To achieve grain growth saturation in the whole bonded layer, more energy is required. This explains the result that post-bonding annealing improves the bond strength in Ref [62] that this

incomplete grain growth area has weaker bond strength due to the existing interface. When a razor applies a force in the bonded layer, the crack would have the chance to grow along the "poor" (non-saturated grain growth) bonding interface. On the other hand, even with a huge force, the bonded layer cannot be delaminated if there is no interface existing in the layer. Therefore, through the second time grain growth from annealing, the microstructure of the whole bonded layer can be further arranged and then reaches a steady state with increased bond strength.

5.4 Grain Orientation Evolution Observation

From the TEM diffraction patterns in Figs. 5-1(a) and (c), it is clear that there is a grain orientation transformation from (111) to (220). In order to make sure that this is not a local phenomenon, bonded samples with one side substrate removed by grinding were analyzed by XRD. Grain orientations under different bonding conditions are shown in Fig. 5-4. It is evident that the (220) intensity increases while (111) and (200) intensities decrease after bonding and annealing. In addition, Table 5-1 shows the average fraction of grain orientations under different bonding conditions. The fraction of (220) increases upon bonding and further annealing, but does not increase significantly after 60 min annealing. The trend here is similar to the distribution of average grain size under different bonding conditions.

5.5 Mechanism of Abnormal Grain Growth during Bonding

During the bonding and annealing processes, the intensity of (220) grains increases but

that of (111) grains decreases. A preferred grain orientation (220) after bonding and annealing is observed while (111) is the preferred orientation before bonding. Since this is also identical to the results from TEM diffraction patterns, this phenomenon appears both in the local and the whole bonded layer.

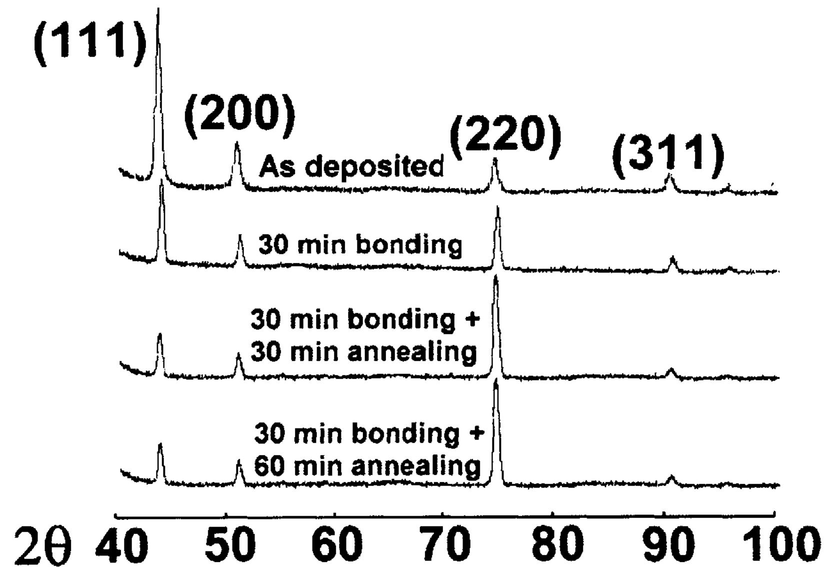


Figure 5-4 XRD patterns for different bonding conditions

Table 5-1 The average fraction of grain orientations under different bonding conditions

	(111)	(220)	Other orientations
As deposited	0.62	0.13	0.25
30 min bonding	0.42	0.33	0.25
30 min bonding +30 min annealing	0.23	0.57	0.20
30 min bonding +60 min annealing	0.23	0.60	0.17

The effect of yielding in grains is proposed to explain the (220) preferred orientation during bonding [72]. The Cu bonded layer is in a state of biaxial strain due to their attachment on both sides of the much thicker Si substrates. Since the in-plane stress in a grain is the product of the biaxial strain and biaxial modulus, which is a function of grain orientation factor C_{ijk}, the yield stress of the grain also varies depending on its orientation. It is reported that the orientation factor C_{ijk} of (111) has the largest value of 3.46 while that of (220) has the smallest one of 1.42 [73]. This means that the yield stress of (220) is much smaller than that of (111). Therefore, for grains of equal initial sizes, (220) grains will yield before (111) grains, thus the (220) grains have an energetic advantage for further growth [72]. This yielding process also leads to strain energy minimization [72, 74]. For further annealing process, the bonded wafer is heated again from room temperature to high temperature, so the in-plane strain also increases. Then, at high temperature, the secondary grain growth occurs; and at this time, (220) grains yield first and take this energetic advantage to minimize the strain energy in the bonded layer. This may explain why (220) grains grow faster than other grains and becomes the final preferred orientation. When the grain growth saturation is reached after 60 min annealing, the yielding process also stops.

It is reported that Cu with preferred (111) orientation has longer electromigration lifetime than that with preferred (220) orientation [75]. Therefore, the abnormal (220) grain growth during Cu wafer bonding is certainly not desirable in IC fabrication. It is imperative that methods to suppress (111) to (220) transformation while maintaining reasonable bonding strength during Cu wafer bonding should be developed.

5.6 Summary

An abnormal Cu (220) grain growth during bonding and annealing was observed by TEM, electron diffraction and XRD. It is suggested that the growth of (220) grains is easier than that of (111) and (002) grains since (220) grains have a lower yield stress and the growth has minimized the surface or strain energy. The preferred orientation becomes (220) after further annealing. Both grain sizes and (220) grain intensity reach a saturated state after 30 min of annealing. In addition, the grain structure becomes saturated after further annealing.

Chapter 6

Interfacial Morphology of Bonded Layer under Different Bonding Conditions

Interfacial morphologies of copper bonded wafers at bonding temperatures from 150°C to 400°C for 30 min followed by an optional 30 or 60 min nitrogen anneal were investigated by means of transmission electron microscopy. Results showed that increased bonding temperature or increased annealing duration improved the bonding quality. Wafers bonded at 400°C for 30 min followed by nitrogen annealing at 400°C for 30 min, and wafers bonded at 350°C for 30 min followed by nitrogen annealing at 350°C for 60 min achieved the same excellent bonding quality.

6.1 Sample Preparation and Experimental Procedures

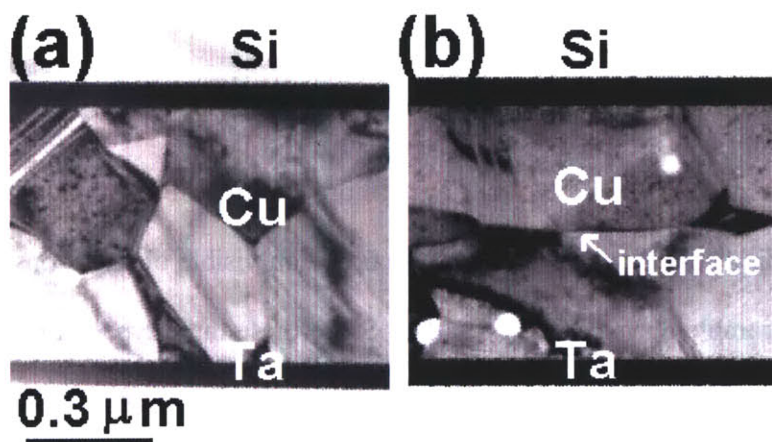
Layers of Ta and Cu, 50-nm and 300-nm of Cu thick respectively, were successively deposited on N-type (100) 4" Si wafers. The detailed bonding procedure is described in Chapter 2. The bonding pressure was kept at 4000 mbar. The bonding temperature ranged from 150°C to 400°C, and the bonding time was 30 min. A subsequent optional nitrogen annealing was performed at the same bonding temperature for 30 or 60 min. The morphology of the bonded Cu-Cu layer was examined using a JEOL-2010 transmission electron microscope (TEM). During the TEM sample preparation, the samples were kept below 120 °C to avoid grain growth.

6.2 Categories of Morphologies

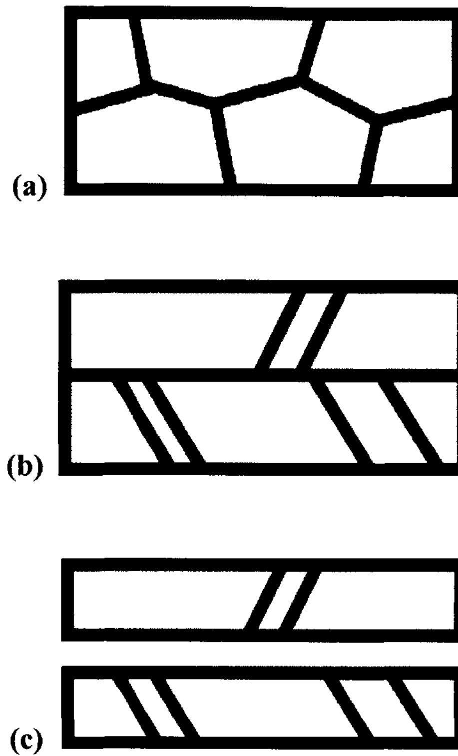
According to previous results in Chapters 4 and 5, two major bonding morphologies have been observed in the bonded layer. In one, the original bonding interface still exists after bonding. In the other one, the bonding interface disappears and a whole grain structure appears after bonding. Examples of TEM morphologies for types (1) and (2) are shown in Figs. 6-1(a) and (b), respectively. Therefore, TEM morphologies can be sorted into three categories: (1) No interface but grain structure (identified as "Grain" in following discussion and tables), (2) Interface structure (identified as "Interface" in following discussion and tables), and (3) Failure of TEM sample (identified as "TEM failed" in following discussion and tables). Figures 6-2(a), (b), and (c) show the corresponding schematic diagrams. The bonded morphology showing a whole grain structure without the original bonding interface is expected to exhibit a high bonding strength. In the case

where the bonding interface still exists in the layer, however, its persistence suggests that the structure has acquired sufficient but not maximum bonding strength. In other words, the grain structures of the two bonded layers did not have enough energy to completely remove the bonding interface. Finally, if the TEM sample fails during preparation, it is treated here as an indication of poor bonding strength.

For each bonding condition, several bonded wafer pairs were prepared in order to access the reliability/reproducibility of these results. Samples cut from different areas of each bonded wafer pair were used for TEM observation. Results gathered from different areas of different wafers are qualitatively classified into three categories: 1. "Most" means more than 66% of observed bonded area belongs to this morphology, 2. "Some" means 33%-66% of observed bonded area belongs to this morphology, 3. "Few" means less than 33% of observed bonded area belongs to this morphology. Not only can this method easily distinguish the bonding quality of an individual bonding condition, but also show the bonding quality trend as a function of temperature and process duration.



Figures 6-1(a) and (b) TEM morphologies of (a) "Grain" (bonded at 350C for 30 min followed by N_2 annealing for 60 min), and (b) "Interface" (bonded at 350C for 30 min)



Figures 6-2 Schematic diagrams of three catalogues for possible TEM observation results of Cu bonded layer (a) No interface but grain structure (identified as "Grain"), (b) Interface structure (identified as "Interface"), and (c) Failure of TEM sample (identified as "TEM failed")

6.3 Observation Results

Table 6-1 summarizes the TEM interfacial morphologies of Cu bonded wafers under different bonding conditions. The results are based on visible observations along the full length of the sample during TEM operation. Since these three types of morphologies all appear in each TEM sample, it is difficult to decide quantitative results. In general, observation shows that the proportion of interface morphologies exhibiting "Grain" structure increases when the bonding/annealing temperature or annealing duration

increases, while the proportion with "TEM failed" structure decreases. This suggests that better bonding strength can be achieved at higher bonding/annealing temperature or longer annealing duration since the "Grain" structure represents an excellent bonding quality, whereas the "TEM Failed" structure represents a poor bonding quality.

Table 6-1 TEM results of the interfacial morphologies on Cu bonded wafers under different bonding conditions.

Bonding Duration / Bonding Temperature	30 min bonding	30 min bonding + 30 min annealing	30 min bonding + 60 min annealing
400°C	Grain: Few Interface: Most TEM failed: Few	Grain: Most Interface: Some TEM failed: Few	Grain: Most Interface: Some TEM failed: Few
350°C	Grain: Few Interface: Some TEM failed: Some	Grain: Some Interface: Some TEM failed: Few	Grain: Most Interface: Some TEM failed: Few
300°C	Grain: Few Interface: Some TEM failed: Some	Grain: Few Interface: Some TEM failed: Some	Grain: Some Interface: Some TEM failed: Some
250° C	Interface: Some TEM failed: Some	Interface: Some TEM failed: Some	Interface: Some TEM failed: Some
200° C	Interface: Some TEM failed: Some	TEM failed	TEM failed
150° C	TEM failed	TEM failed	TEM failed

As indicated in Table 6-1, the bonding interface still exists in the wafer pair bonded at 400°C for 30 min. Whole grain structure morphology and TEM sample failure are rare. After 30 min annealing, however, the major morphology in the bonded layer becomes that of a whole grain structure and most of the original interface has disappeared. In

addition, there are only very few failed TEM samples during sample preparation. This suggests that the bonding quality is strong and relatively uniform under this condition, which is consistent with previous observations. When the annealing time is increased to 60 min, the morphology composition is almost the same as that corresponding to 30 min annealing. This suggests that the bonding strength does not increase further.

When the bonding temperature is decreased to 350°C and 300°C, the number of failed TEM samples increases for all bonding conditions. At the same time, the possibility of a whole grain structure in the bonded layer is low. For example, at 300°C, the morphology of the bonded layer corresponding to 30 min bonding followed by 30 min annealing shows only a relatively small fraction of the no-interface "grain" structure, while this is the major morphology at 400°C under the same bonding condition. These results suggest that the bonding strength decreases when the bonding temperature decreases.

Furthermore, when bonding temperatures are above 300°C, after post-bonding anneal in nitrogen, the fraction of no-interface "grain" structure morphology increases, and that of TEM samples failure decreases. This suggests that post-bonding anneals are important for successful bonding, consistent with the previous results at 400°C. At 300°C and 350°C, increasing annealing duration also showed improvements in bond strength.

It is interesting to note that the interfacial morphologies at 350°C and 300°C, unlike those at 400°C, still changed with annealing time up to 60 min. This suggests that the bonding strength at 300°C and 350°C can still be improved by increasing the annealing duration further.

When the bonding temperature is 250°C, approximately half of the morphologies can be classified as "Interface" structure, while the other half are "TEM failed." On the

other hand, almost all wafers bonded below 200°C failed during TEM preparation. In addition, further annealing at bonding temperatures at or below 250°C does not improve the bonding quality, while further annealing does improve it at bonding temperatures of 300°C and higher.

6.4 Discussion

Several important observations can be made from Table 6-1. At 400°C, diffusion and grain growth during bonding are enhanced. Strong inter-diffusion of the atoms from two originally distinct Cu layers probably increases the bonding strength. Further grain growth also helps remove the bonding interface, thus creating a whole grain structure. Finally, the bonding quality becomes excellent.

Further anneals after bonding also improve the bonding quality. After bonding at a temperature higher than room temperature, the bonded wafer cools down to room temperature. When the bonded wafer is undergoing annealing, the temperature of the microstructure in the bonded layer is increased again. Consequently, the grains grow again during annealing, and this will further remove the bonding interface. This explains the no-interface "grain" structure observed as the main morphology in wafers further annealed at 400°C for 30 min. The microstructure appears to be a stable state and most of the grains seem to have stopped growing. Therefore, further annealing will not change the major morphology, which is why the interfacial morphology corresponding to 60 min annealing is the same as that corresponding to 30 min annealing.

At lower temperatures such as 300°C and 350°C, annealing still improves the bonding quality, but it takes longer to reach a stable state. It is interesting that, unlike at

400°C, the major morphologies still change when the annealing time is increased from 30 min to 60 min at 300°C and 350°C. This is also understandable. Compared with 400°C, in the 300°C and 350°C samples, the bonded layers may not have enough energy to allow grains growth to the stable state after 30 min of annealing. The major morphologies will continue to change with anneal time until the stable state is reached (i.e., until the interface is removed).

It has been shown that wafers bonded at 400°C for 30 min followed by nitrogen annealing at 400°C for 30 min will reach a strong bond quality. From the manufacturing viewpoint, the bonding and annealing temperature should be kept as low as possible, but it is also desirable to reduce bonding and annealing time. One advantage of lower bonding temperature is cost savings. Another advantage is to avoid destroying device components. An alternative bonding condition that achieves the same bonding quality is 350°C for 30 min followed by nitrogen annealing at 350°C for 60 min.

In general, in order to obtain a "Grain" structure, wafer bonding conditions of 400°C for 30 min followed by nitrogen annealing at 400°C for 30 min, or 350°C for 30 min followed by nitrogen annealing at 350°C for 60 min, are required. Under the conditions investigated here, the minimum bonding temperature must be at or above 300°C to obtain a better "bonded" layer (i.e., a "Grain" morphology).

The morphology observations summarized shown in Table I represent the quality of the bonded layer. The "Grain" structure represents an excellent bonded layer. The "Interface" structure represents that the two layers are not fully bonded and exhibit a bonding interface, but can withstand the TEM sample preparation. These are the two major morphologies observed at higher temperatures. At lower bonding temperatures, part of the bonded layer cannot withstand the TEM sample preparation process. Therefore,

another approach to characterize the bonding quality such as bonding strength at low temperatures is necessary. Different testing techniques for bonding strength are described in the next chapter.

6.5 Summary

Copper bonded morphologies were investigated by means of transmission electron microscope at different bonding conditions. The bonding time was kept at 30 min and some wafers were annealed in nitrogen for 30 min or 60 min. The results show that the bonding quality improves when either bonding temperature increases or post-bonding annealing is used. The increase of the annealing time beyond 30 min improved the bonding quality when the wafers were bonded at 300°C or 350°C. Wafers bonded at 400°C for 30 min, followed by nitrogen annealing at 400°C for 30 min, and wafers bonded at 350°C for 30 min, followed by nitrogen annealing at 350°C for 60 min, achieved the same excellent bonding quality.

Chapter 7

A Map of Bonding Quality and Bonding Strength Investigation Using Different Test Techniques

The bond strength of copper-bonded wafer pairs prepared under different bonding/annealing temperatures and durations are presented. The bond strength was examined from dicing test. Physical mechanisms explaining the different roles of post-bonding anneals at temperatures above and below 300°C are discussed. A map summarizing the transmission electron microscopy morphology results in previous chapter and bonding strength from the dicing test provides a useful reference on process conditions suitable for actual microelectronics fabrication and three-dimensional integrated circuits based on Cu wafer bonding. In addition to dicing test, tape test, pull test, and push test are used to investigate the bonding strength qualitatively and quantitatively.

7.1 Test Bonded Sample Preparation

Layers of Ta and Cu, 50-nm and 300-nm of Cu thick respectively, were successively deposited on N-type (100) 4" Si wafers. The detailed bonding procedure is described in Chapter 2. The bonding pressure is kept at 4000 mbar. The bonding temperature ranged from 150°C to 400°C, and the bonding time was 30 min. A subsequent optional nitrogen annealing was performed for 30 or 60 min.

7.2 Dicing Test

Bonded wafers of different bonding conditions were cut into 262 square pieces (5mm x 5mm) at a speed of 0.69 mm/sec by a DAD-2H/6T Automatic Dicing Saw. When the bonded wafer is sawed into 5mm x 5mm pieces, the two bonded pieces bond may stay bonded or the two pieces may separate due to the applied stress during sawing. The later case is defined here as a "failed piece". This approach allows characterizing the bonding quality when the wafers are bonded at lower temperatures. At the same time, it offers some interesting data relevant to subsequent packaging.

Table 7-1 shows the percentage of failed pieces at different bonding conditions after sawing. For each data entry, the results are the average of failed pieces from three wafers under the same bonding condition. As Table 7-1 indicates less than three pieces bonded at 350°C and 400°C failed of three wafers. The percentages of failed pieces stay below 25% for the bonding temperatures of 250°C and 300°C. However, when the temperature is 200°C or lower, the percentage of failed pieces is much higher. For wafers bonded below 200°C followed by nitrogen anneal, the pieces almost always failed.

Table 7-1 Number and percentage of failed pieces at different bonding conditions after dicing process

Bonding Temperature \ Bonding Duration		Number and percentage of failed pieces (One wafer: 262 pieces)		
		30 min bonding	30 min bonding + 30 min annealing	30 min bonding + 60 min annealing
400 C	Wafer 1	2	1	0
	Wafer 2	0	0	0
	Wafer 3	1	1	1
	Total #	3	2	1
	Percentage	0.4 %	0.3%	0.1%
350 C	Wafer 1	0	2	1
	Wafer 2	1	0	1
	Wafer 3	2	0	0
	Total #	3	2	2
	Percentage	0.4 %	0.3 %	0.3 %
300 C	Wafer 1	3	9	13
	Wafer 2	0	21	10
	Wafer 3	0	12	11
	Total #	3	42	34
	Percentage	0.4 %	5.3 %	4.3 %
250 C	Wafer 1	2	48	61
	Wafer 2	4	64	60
	Wafer 3	4	53	52
	Total #	10	165	173
	Percentage	1.3 %	21.0 %	22.0 %
200 C	Wafer 1	43	198	229
	Wafer 2	38	248	193
	Wafer 3	60	227	170
	Total #	141	673	592
	Percentage	17.9 %	85.6 %	75.3 %
150 C	Wafer 1	97	250	260
	Wafer 2	101	219	257
	Wafer 3	96	231	237
	Total #	294	704	754
	Percentage	37.4 %	89.6 %	95.9 %

Table 7-1 suggests that the bonding quality is better at higher bonding/annealing temperature and that it deteriorates below 250°C. When the two layers are bonded below 250°C, the thermal energy is not high enough for grain growth development during the bonding process. Therefore, as shown previous chapters, the bonded layer has not had sufficient time to develop a grain structure. In order to achieve a good bonded interface, the required bonding duration will be very long at lower temperature, and it would not be practical in manufacturing. On the other hand, when the temperature is higher, the layers will have more energy to reach a stable structure, thereby improving the bonding quality.

7.3 The Effect of Anneal Temperature on Bonding Quality

The data in both dicing test and morphology observation results in Chapter 6 show an interesting behavior for wafers bonded below 250°C followed by nitrogen anneal. In morphology observation results shown in Table 6-1 of Chapter 6, for example, wafers bonded at 200°C for 30min without further anneal exhibit a mixed "Interface" and "TEM failed" structures while those that underwent further anneal all failed during TEM sample preparation. On the other hand, wafers bonded higher than 300°C tend improve their bonding quality after further anneal. Similarly, dicing test shows that at low bonding/annealing temperatures, the percentage of failed dies increases if the wafer undergoes nitrogen anneal. This behavior is more striking when the temperature is below 200°C.

To explain this apparent discrepancy, the state of the bonding interface between two layers at "high" and "low" temperatures must be analyzed. As shown in previous chapters,

after bonding at high temperature, the two layers bond together though the original interface remains. At this stage, since the bonding temperature was high, both interdiffusion between the two layers and preliminary grain growth may have already occurred. Therefore, defects, impurities and voids in the bonding interface area have been effectively removed through this process. Consequently, during the further anneal, the grains will grow further until the whole structure reaches a stable stage.

However, when bonding occurs at "low" temperature for a relatively short time, the wafers do not achieve sufficient energy. Therefore, after bonding, although the two wafers are bonded together and can withstand the sawing process, the bonding strength may be insufficient, while defects, impurities, and voids may still remain at the bonding interface area. When these wafers undergo further nitrogen anneal, the weakly bonded interface with defects is subjected to thermal stress. If the bonding strength cannot tolerate the thermal stress and the stress field induced by the vacancies and defects, the bonded area may separate. This qualitatively explains why the bonding quality and interfacial morphology become worse when further nitrogen anneal is carried out for wafers bonded at "low" bonding/annealing temperature.

7.4 A Map of Bonding Quality

A morphology and strength map summarizing the results of morphology observation and dicing test for copper wafer bonding under the conditions examined here is shown in Fig. 7-1. Three lines are plotted. The first line distinguishes "Grain" structure and "Interface" structure regions. The second line represents "Low failure percentage region", and the third line represents "High failure percentage region". The region above the first line

yields a "Grain" structure as a major interfacial morphology with excellent bonding quality. The region between the first and second lines yields mostly an "Interface" structure that has sufficient bonding quality and that shows the original bonding interface. The region below "High failure percentage region" represents a major result of "dicing failure".

The map in Fig. 7-1 offers helpful information for future applications based on Cu wafer bonding. For example, for excellent bonding quality, the bonding condition can be either 400°C for 30min followed by annealing at 400°C for 30min or bonded at 350°C for 30min followed by annealing at 350°C for 60min. For sufficient bonding quality with an interface, bonding temperature above 300°C is necessary.

7.5 Tape Test

After the dicing test, surviving bonded pieces underwent the tape test. The 3M Scotch 3710 Adhesive Tape was stuck on the bonded pieces. Then force was applied to rip the tape from the piece by hands. If the bonding strength is larger than the adhesion between the adhesive tape and piece, the tape will separate from the piece. However, if the bonding strength is smaller than the adhesion between the adhesive tape and piece, the piece will break from the bonding interface and the tape will remain stuck to one of the separating pieces. The later case is defined as "failed piece".

Table 7-2 lists the number and percentage of failed pieces at different bonding conditions after dicing process and tape test. Three wafers were investigated for each bonding condition. In general, the percentages and numbers of failed pieces increase after tape test. This means that some bonded pieces can stand the stress during the dicing but

not during the tape test. Also the increased failed pieces and percentages before and after tape test are not large, which implies that the stress during dicing and tape test should be in a similar range.

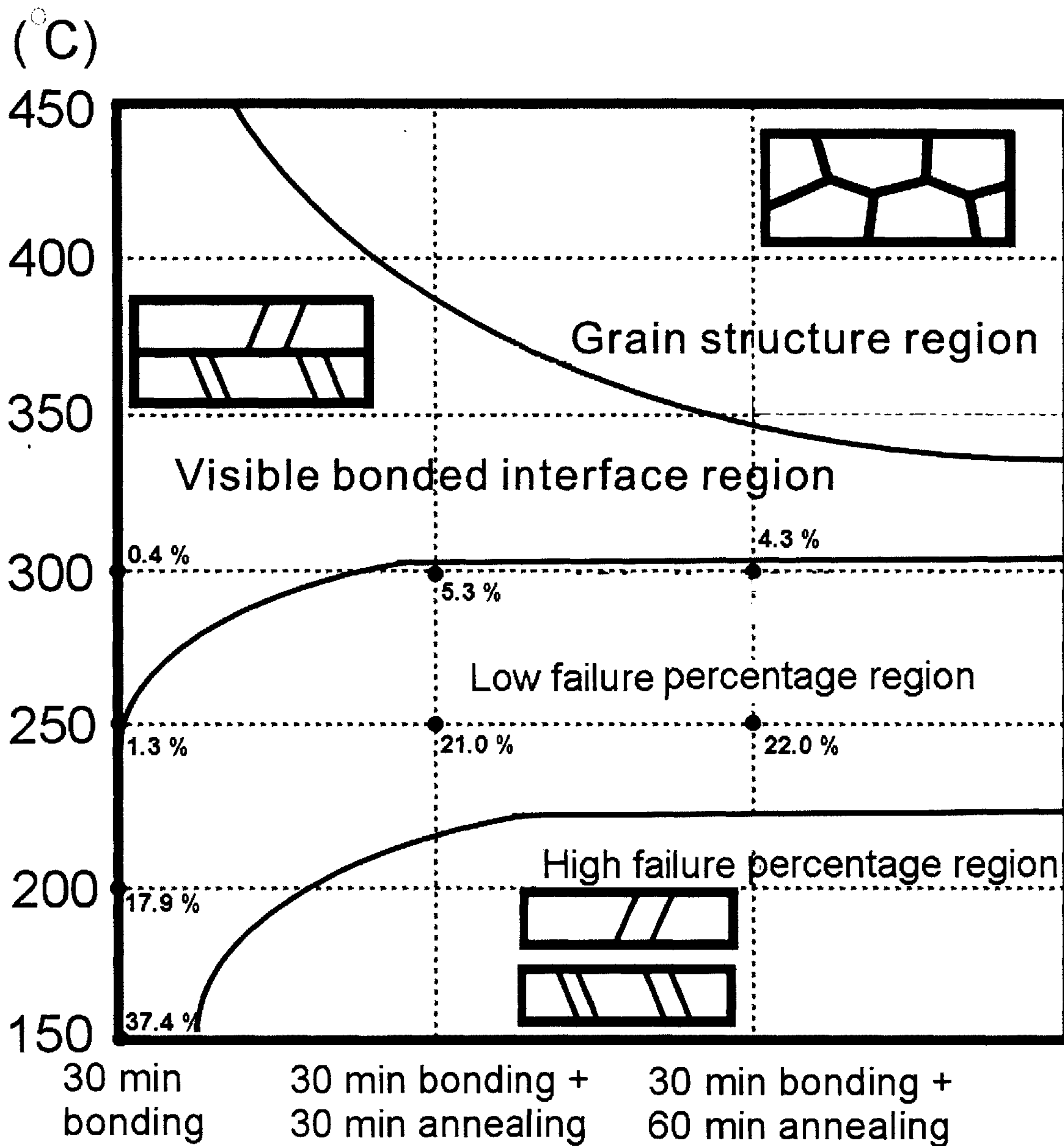


Figure 7-1 Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions. Some dicing failure percentages of bonding conditions are marked in the map.

Table 7-2 Number and percentage of total failed pieces at different bonding conditions after dicing process and tape test

Bonding Temperature \ Bonding Duration		Number and percentage of failed pieces (One wafer: 262 pieces)		
		30 min bonding	30 min bonding + 30 min annealing	30 min bonding + 60 min annealing
400 C	Wafer 1	2	1	0
	Wafer 2	0	1	0
	Wafer 3	1	1	1
	Total #	3	3	1
	Percentage	0.4 %	0.4%	0.1%
350 C	Wafer 1	0	2	1
	Wafer 2	1	0	2
	Wafer 3	2	1	0
	Total #	3	3	3
	Percentage	0.4 %	0.4 %	0.4 %
300 C	Wafer 1	3	17	23
	Wafer 2	0	22	19
	Wafer 3	0	21	21
	Total #	3	60	63
	Percentage	0.4 %	7.6 %	8.0 %
250 C	Wafer 1	5	54	64
	Wafer 2	6	68	62
	Wafer 3	8	58	55
	Total #	19	180	181
	Percentage	2.4 %	22.9 %	23.0 %
200 C	Wafer 1	47	201	229
	Wafer 2	48	252	195
	Wafer 3	62	228	178
	Total #	157	681	602
	Percentage	20.0 %	86.6 %	76.6 %
150 C	Wafer 1	103	250	260
	Wafer 2	106	234	258
	Wafer 3	105	245	244
	Total #	314	729	762
	Percentage	39.9 %	92.7 %	96.9 %

It should be noted that the percentages of total failed pieces remain zero for bonding temperature above 300°C. These results show that the bonding strengths at these conditions are excellent. The bonded pieces under these bonding conditions not only can stand the stress during the dicing but also during the tape test.

7.6 Pull Test

The previous approaches to investigate the bonding strength, including TEM image examinations, dicing test and tape test, offer an overall image of bonding quality under different bonding conditions. However, these approaches are all qualitative methods. If the specific number of bonding strength at one bonding condition is desirable, quantitative methods should be applied. Pull test is the quantitative method used in this thesis to investigate the bonding strength.

After dicing test, surviving bonded pieces underwent the pull test by a Guad Group Romulus III Pull Machine. One side of the bonded piece was loaded on the substrate of the machine, while the other side glued to a pin with Epoxy. During the pull test, the machine pulled the pin until the sample broke. The force at the failure of the sample was recorded.

Figure 7-2 shows the results of bonding strength under different bonding conditions by pull test. It should be noted that each value is the average of bonding strengths at different locations from different wafers at the specific bonding condition. Four or five bonded pieces were investigated for each bonding condition. The bar associated each data point in the figure represents the full range of strength values. Since each bonding strength is the average value of samples, this value depends on the uniformity of bonding

results across each wafer, and the stability of bonding process parameter control. The bonding strengths range from 0 to 80 MPa when bonding temperatures are from 150°C to 400°C. It is obvious that the bonding strength increases with the increase of bonding temperature. The trend is identical to those observed in TEM observation, dicing test, and tape test.

Similar to the trend observed in the dicing test, at the high temperature regime (above 300°C), the bonding strength increases if the nitrogen anneal is applied after bonding. At the low temperature regime (below 300°C), the bonding strength decreases if the nitrogen anneal is applied after bonding. The possible mechanism for the anneal effect has been proposed in Section 7.3.

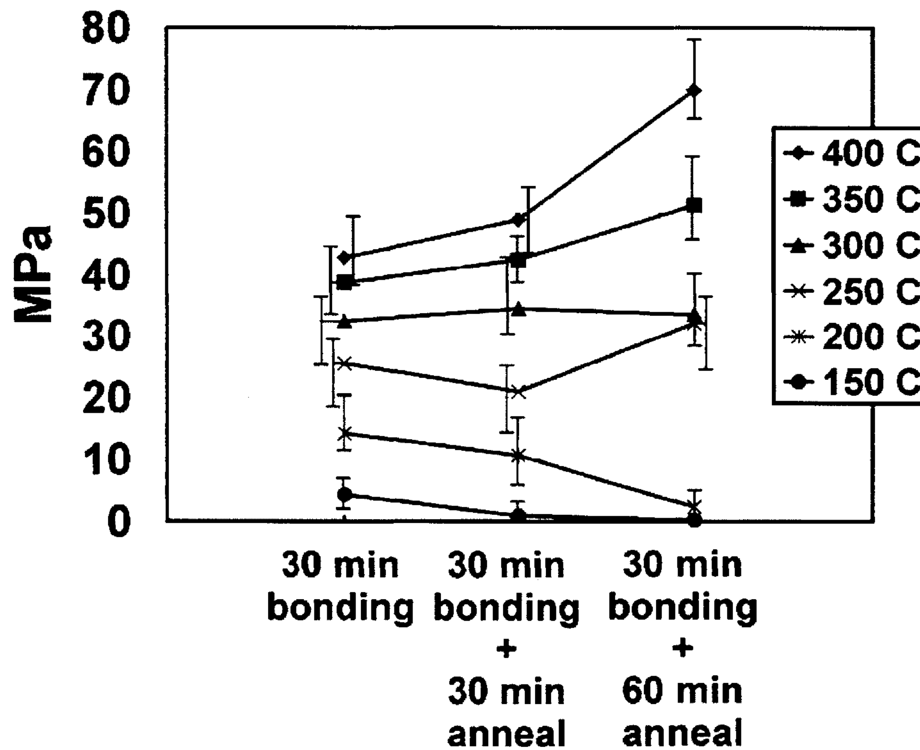


Figure 7-2 Results of bonding strength under different bonding conditions by pull test. Some of bonded samples above 300°C did not break along the bonding interface but along other thin film interfaces. Bars represent range of data, and offset from the average point for visual conveniences.

When the wafers bonded at 150°C, the bonding strengths were weak and close to zero under different bonding conditions. Compared to the results of dicing test, which shows almost most of the pieces failed during the test, these two results are identical.

The bonding strength of bonded pieces at 150°C for 30 min bonding is smaller than that of bonded pieces at 200°C for 30 min bonding followed by 30 min nitrogen anneal, and approximately the same as that of bonded pieces at 200°C bonding for 30 min followed by 60 min nitrogen anneal. However, the results are different in dicing and tape tests, in which the bonded pieces at 150°C for 30 min show better bonding strengths than those at 200°C for 30 min bonding followed by 30 or 60 min nitrogen anneal. Similar discrepancies are found in the comparison of 200°C for 30 min bonding and 250°C for 30 min bonding followed by 30 or 60 min nitrogen anneal. The reason is that dicing and tape test are based on the stress applied on the bonded pieces. The result only reflects if the bonded pieces can or cannot stand the stress during test. On the other side, the pull test reports the absolute value directly. Therefore, it is reasonable to expect different trend among these tests.

The difference between pull test and dicing or tape test becomes clear when the bonded pieces are bonded at 350 or 400°C. In dicing or tape test, the results for bonded pieces at 350 and 400°C show zero failed dicing pieces. Based on these results, we still cannot tell the differences of bonding strengths among these conditions. However, in Fig. 7-2, bonding strengths at 350 and 400°C under different bonding conditions are different. The higher bonding temperature and the longer anneal duration introduce the higher bonding strength. The highest average value of bonding is around 70 MPa for bonded pieces that were bonded at 400°C for 30 min followed by nitrogen anneal at 400°C for 60 min.

It should be noted that during the pull test, some of the bonded pieces, which were bonded above 300°C, broke along the interfaces between Si and Ta or other locations but not the original Cu and Cu bonding interface. This phenomenon also increases with the increase of bonding temperature and anneal duration. For these bonded pieces, their strengths of bonding interfaces are already larger than the adhesive force of other thin films. According to the previous TEM results, the original bonding interface may disappear after 400°C or 350°C 30 min bonding followed by nitrogen anneal. If the bonding interface has already disappeared, it is reasonable to expect that the bonded piece should break along other thin film interfaces.

7.7 Shear Test

In addition to pull test, shear test is another quantitative method used in this thesis to investigate the bonding strength.

After dicing test, surviving bonded pieces underwent the shear test by a Dage Series 4000 Shear Machine. Figure 7-3 shows the schematic diagram of the shear test. The bonded piece was first loaded on the substrate of the machine. Then a board perpendicular to the substrate was raised to a "shear height" of 600 μm. Shear height means the distance between the bottom of the bonded piece to the bottom of the board. During shear test, the board pushed the upper part of the bonded piece until the sample broke. The force at the failure of the sample was recorded.

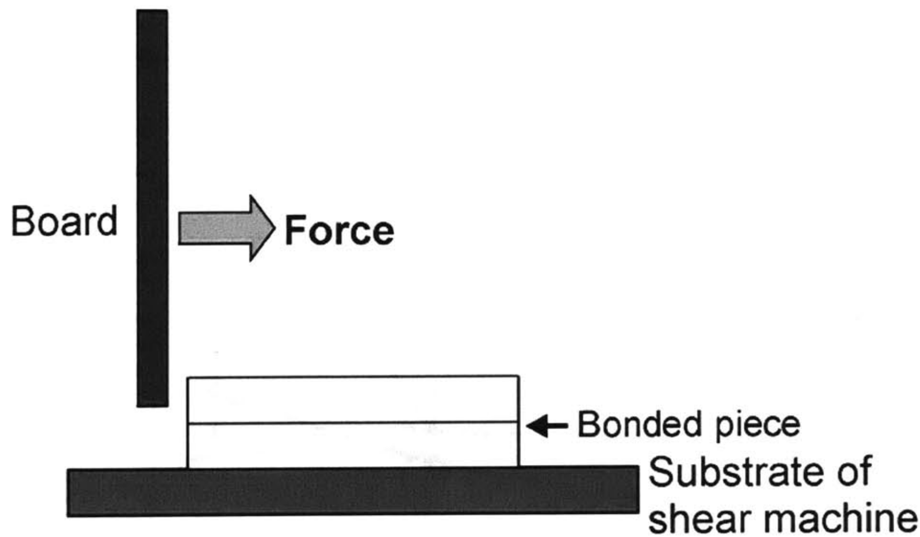


Figure 7-3 The schematic diagram of the shear test

Figure 7-4 shows results of bonding strength under different bonding conditions by shear test. Each value is the average of bonding strengths at different locations from different wafers at the specific bonding condition. Four or five bonded pieces were investigated for each bonding condition. The bar associated each data point in the figure represents the full range of strength values. The trend of bonding strength corresponding to the different bonding conditions in this figure is similar to that in Fig. 7-2 by pull test. Bonding strength by shear test increases as the bonding temperature or anneal duration increases. As shown in other tests, the anneal effect in high and low temperature regimes also shows different result. Some of the bonded samples above 300°C did not break along the bonding interface but along other thin film interfaces.

Fig. 7-4 shows that the bonding strength at 400°C for 30 min bonding followed by nitrogen anneal at 400°C for 60 min by shear test is much higher than others. Although the bonding strength should increase with the increase of bonding temperature and anneal duration, the reason for this abrupt increase is still under investigation.

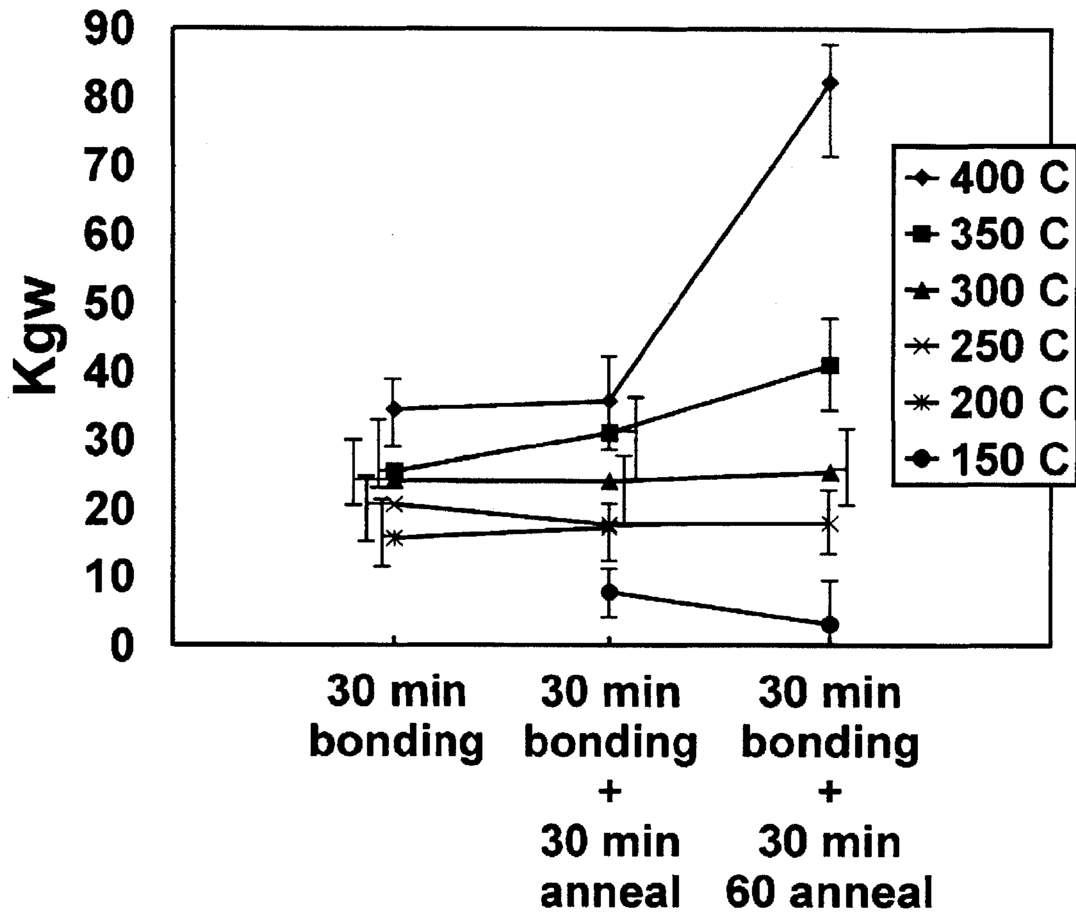


Figure 7-4 Results of bonding strength under different bonding conditions by shear test. Some of bonded samples above 300°C did not break along the bonding interface but other thin film interfaces. Bars represent range of data, and offset from the average point for visual conveniences.

In general, pull and shear tests offer quantitative data of bonding strengths. Thus these results should be more reliable than other qualitative ones. However, since these results were based on the average of bonded pieces on different locations from different wafers, any process reliability issues such as the non-uniformity of bonding qualities may generate a different result. Therefore, it is necessary to examine more wafers to achieve

more reliable average values.

7.8 Summary

The bond strength of copper-bonded wafer pairs prepared under different bonding/annealing temperatures and durations are examined. The approaches to investigate the bond strength include dicing test, tape test, pull test, and shear test. Dicing and tape tests belong to the qualitative tests, while pull and shear tests belong to quantitative tests. These tests observed the phenomenon that bond strength increases with the increase of bonding temperature or the increase of anneal duration at high temperature.

Both qualitative and quantitative tests show that post-bonding anneal does not improve the bond strength when the process temperature is below 300°C. Physical mechanisms explaining the different roles of post-bonding anneals at temperatures above and below 300°C are discussed.

By summarizing the results from transmission electron microscopy morphologies in previous chapter and bond strength from the dicing test, a map is established to indicate good areas for further process evaluation in three-dimensional integrated circuits based on Cu wafer bonding.

Chapter 8

Effect of Wafer Bow on Copper Wafer Bonding Quality

Research on the behavior of thin metal films on substrates have been widely investigated because of their applications in microelectronics [76-82]. Some of these studies on Cu thin films used substrate curvature methods [77-80], which corresponds to the measurement of wafer bow. Wafer bow is obtained from the measurement of the overall magnitude of wafer curvature, and usually means the height deviation between the center of the wafer and the edge of the wafer. Wafer bow may result from the wafer manufacturing process or thin film stress on the wafer substrate. Since wafer bonding relies on the surface flatness of the two wafers [83-88], wafer bow may play an important role in the bonding quality. Understanding the effect of wafer bow is also helpful to accurately study other bonding parameters. This chapter reports the effect of wafer bow on bonding quality under different bonding temperatures, and a criterion to minimize the effect of wafer bow during bonding process.

8.1 Sample Preparation and Experimental Procedures

Wafer bows of unprocessed bare 4" (100) prime silicon wafers within the range between –20 μm and 20 μm were investigated in this study. Wafer bows of each silicon wafer before and after depositing 50 nm Ta and 300 nm Cu by electron beam deposition were measured using a KLA-Tencor thin film stress measurement. Wafer bow of unprocessed wafers before metal thin film deposition will be referred to as "initial wafer bow" in the following discussion for convenience. Two wafers with similar initial wafer bows were chosen as the bonding pair. These two wafers with similar initial wafer bows after Ta and Cu deposition were bonded face to face in the Electronic Vision EV 450 Aligner and AB1-PV under a pressure of 4000 mbar for 30 min at 200°C, 300°C and 400°C in the ambient of 10^{-3} torr. A DAD-2H/6T Automatic Dicing Saw cut bonded wafers into 5mm x 5mm square pieces at a speed of 0.69 mm/sec. After the bonded wafer is sawed into pieces, one bonded piece may stay bonded or separate due to the applied force during sawing. The later case is defined here as "dicing failure". This approach allows us to characterize the bonding quality with different initial wafer bows. In order to simulate the *in situ* wafer bow at the bonding temperature, some wafers with different initial wafer bows were subjected to thermal heating from room temperature to 400°C with a ramp up at 0.4°C/s to measure the evolution of wafer bow. The surface of the Cu film during heating and measurement is capped to avoid oxidation. The ramp rate is similar to the heating rate of the bonding process. In each case, *in situ* wafer bow measurements were taken at a 10°C interval to monitor the change of wafer curvature.

8.2 Wafer Bow Evolution During the Heating Process

Figure 8-1 shows an example of wafer bow evolution during the heating process from room temperature to 400°C. Y-axis represents the change of wafer bow at each step of measurement relative to the initial wafer bow, which is set at zero. Right after depositing Ta and Cu films, the change of wafer bow is -3 μm due to the difference of thermal expansion coefficient between Si and metals. For other wafers with the same deposition conditions, the change of wafer bow right after deposition usually varies from –2 to -5μm. Then the change in the wafer bow becomes less negative with the heating process. However, a more negative change in the wafer bow is observed from 150 to 200°C. This is because of the microstructure evolution, which includes the grain growth of the Cu film [82, 89]. Afterwards, the change of wafer bow becomes less negative again with the temperature until zero and goes into the positive regime.

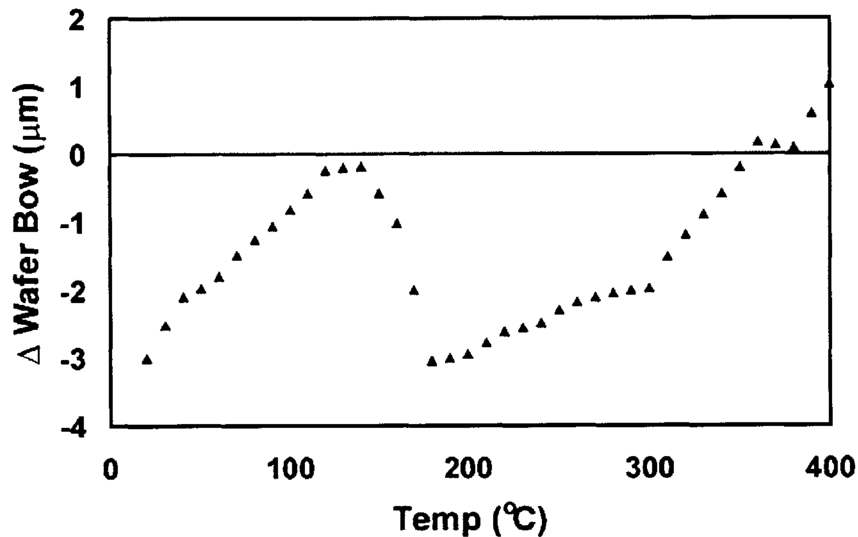


Figure 8-1 An example of wafer bow evolution during the heating process from room temperature to 400°C. The value of " Δ Wafer Bow" means the difference of wafer bow relative to initial wafer bow.

Table 8-1 Average change of wafer bow at different temperature relative to the wafer bow after Ta and Cu film deposition.

	200°C	300°C	400°C
Average changes of wafer bow from room temperature to heating temperature	+0.3 μm	+ 1.1 μm	+ 4.2 μm

Table 8-1 lists the average values of wafer bow change at different temperatures relative to the wafer bow after Ta and Cu films deposition. These values are the average values of measurements from different wafers. The reason to use the wafer bow after metal film deposition as the reference point is that wafer bows vary from one wafer to another. By applying the information in the table, it is possible to estimate the wafer bow value at the bonding temperature and to understand the relation of wafer bow, bonding temperature and bonding quality.

8.3 Wafer Bow and Bonding Quality at Different Bonding Temperatures

8.3.1 At 200°C

Table 8-2 shows relative dicing failure percentages of bonded wafers with different initial wafer bows when these wafers were bonded at 200°C. Six pairs of wafers with initial wafer bows ranged from –20 μm to +20 μm were investigated. Two wafers to be bonded had the similar initial wafer bow. Each pair included one top wafer and one bottom wafer. Wafer bows of each silicon wafer before and after metal film deposition were measured.

The possible wafer bows at 200°C are also estimated based on the information from Table 8-1. In order to clearly show the effect of wafer bow on bonding quality, in addition to list the absolute values of failure pieces during dicing, the relative values are shown. The value of the least dicing failure percentage of the bonded wafer is set as zero. Bonded wafer with the least dicing failure percentage can be treated as the strongest bonded wafer in the group. For other wafers, their values of dicing failure percentage are the differences from the least dicing failure percentage. By using the method, it is easy to decide the strongest bonded wafer and understand the effects of the wafer bow on the bond strength.

Among the six bonded wafers in Table 8-2, the bonded wafer pair D with the flattest initial wafer bows (-0.49 and 1.05 μm) has the least dicing failure percentage. At the same time, wafer pair D is also the flattest pair of wafers at 200°C. When wafer bows of wafers to be bonded increase either positively (A, B, and C) or negatively (E and F), the dicing failure percentage also increases. The increase of the dicing failure percentage can reach 19% when the negative wafer bows at 200°C are more than –15 μm. In addition, similar phenomena can also be observed when wafer bows are in the positive value regime. However, comparing the dicing failure percentages of C, D and E, their value differences are within 3% and can be regarded as in the range of error tolerance. Generally speaking, the wafer bow effect is not obvious when the wafer bow at 200°C is smaller than +- 5 μm.

Table 8-2 Relative dicing failure percentages of bonded wafers with different initial wafer bows when these wafers were bonded at 200°C (One wafer: 262 pieces).

		Wafer bow (μm)			Number of dicing failure	Absolute dicing failure percentage	Relative dicing failure percentage
		Initial	After Ta and Cu deposition	At 200°C (based on Table 8-1)			
A	Top Wafer	-13.51	-16.48	-16.18	94	36%	+19%
	Bottom Wafer	-15.24	-18.42	-18.12			
B	Top Wafer	-7.24	-10.49	-10.19	73	28%	+11%
	Bottom Wafer	-7.42	-10.47	-10.17			
C	Top Wafer	-2.73	-5.80	-5.50	52	20%	+3%
	Bottom Wafer	-1.24	-5.03	-4.73			
D	Top Wafer	-0.49	-2.84	-2.54	44	17%	0%
	Bottom Wafer	1.05	-1.86	-1.56			
E	Top Wafer	5.24	3.01	3.31	50	19%	+2%
	Bottom Wafer	4.14	2.09	2.39			
F	Top Wafer	16.77	13.10	13.40	89	34%	+17%
	Bottom Wafer	14.99	12.21	12.51			

8.3.2 At 300°C

When the bonding temperature is increased to 300°C, the relation of wafer bows and relative dicing failure percentages are showed in Table 8-3. Six pairs of wafers were investigated. Results in Table 8-3 also show similar trend as that in Table 8-2: the dicing failure percentage increases with the increase of wafer bows of wafers to be bonded, both for larger positive or negative values. However, the effect of wafer bows for bonding at 300°C is less than that at 200°C. The increase of the dicing failure percentage only reaches 11% when the negative wafer bows at 300°C are more than –15 μm, while with the similar wafer bow at 200°C it can reach 19%. In addition, the wafer bow effect is not obvious when the wafer bow at 300°C is smaller than +- 8 μm.

Pair K, with the smallest wafer bows at 300°C, shows the strongest wafer bonding quality. However, it should be noted that pair K does not have the flattest initial wafer bows. While pair J have the flattest wafer bow, a 2% increase of dicing failure is observed. From the strongest wafer bonding pairs at 200 and 300°C, it is suggested that the factor that determines a better bonding quality is the wafer bow at the bonding temperature and not the initial wafer bow.

Table 8-3 Relative dicing failure percentages of bonded wafers with different initial wafer bows when these wafers were bonded at 300°C (One wafer: 262 pieces).

		Wafer bow (μm)			Number of dicing failure	Absolute dicing failure percentage	Relative dicing failure percentage
		Initial	After Ta and Cu deposition	At 300°C (based on Table 8-1)			
G	Top Wafer	-13.53	-16.77	-15.67	34	13%	+11%
	Bottom Wafer	-13.26	-16.89	-15.79			
H	Top Wafer	-8.70	-11.80	-10.70	26	10%	+8%
	Bottom Wafer	-8.52	-11.67	-10.57			
I	Top Wafer	-4.43	-6.77	-5.67	16	6%	+4%
	Bottom Wafer	-5.36	-7.05	-5.95			
J	Top Wafer	-0.40	-4.14	-3.04	10	4%	+2%
	Bottom Wafer	0.10	-4.20	-3.10			
K	Top Wafer	4.79	-0.20	0.90	5	2%	0%
	Bottom Wafer	5.03	0.50	1.60			
L	Top Wafer	10.28	6.89	7.99	16	6%	+4%
	Bottom Wafer	9.99	6.25	7.35			

8.3.3 At 400°C

Table 8-4 shows the relative dicing failure percentages of bonded wafers when these wafers were bonded at 400°C. It can be seen that the relative dicing failure percentages are generally less then those at 300 and 200°C. Pairs P and Q, the wafer pairs with the flattest surfaces, have the strongest bonding quality among these six pairs of bonded wafers. In fact, during the dicing experiments, these two pairs did not experience any dicing failure. The result is identical to the results in previous chapter. The increase in the relative dicing failure percentage only reaches 8% when the negative wafer bows are more than −15 μm at 400°C. This performance is better than those at 200 and 300°C bonding. On the other hand, for all of the other pairs, the relative dicing failure percentages are small. Even pair N, with wafer bows of 10 μm, has only 5% of relative dicing failure. Generally speaking, the wafer bow effect is not obvious when the wafer bow at 400°C is smaller than +- 10 μm.

Table 8-4 Relative dicing failure percentages of bonded wafers with different initial wafer bows when these wafers were bonded at 400°C (One wafer: 262 pieces).

		Wafer bow (μm)			Number of dicing failure	Absolute dicing failure percentage	Relative dicing failure percentage
		Initial	After Ta and Cu deposition	At 400°C (based on Table 8-1)			
M	Top Wafer	-18.23	-21.34	-17.14	21	8%	+8%
	Bottom Wafer	-17.17	-20.29	-16.09			
N	Top Wafer	-10.42	-13.71	-9.51	13	5%	+5%
	Bottom Wafer	-10.52	-13.99	-9.79			
O	Top Wafer	-8.13	-10.77	-6.57	8	3%	+3%
	Bottom Wafer	-9.25	-12.05	-7.85			
P	Top Wafer	-3.04	-5.14	-0.94	0	0%	0%
	Bottom Wafer	-2.10	-4.24	-0.04			
Q	Top Wafer	1.09	-2.45	1.75	0	0%	0%
	Bottom Wafer	1.13	-2.71	1.49			
R	Top Wafer	6.82	3.98	8.18	8	3%	+3%
	Bottom Wafer	6.34	4.12	8.32			

8.4 Summary

Figure 8-2 summarizes the relation of wafer bow and bonding quality at different bonding temperatures. Since the wafers of each pair have similar wafer bows, average values of two wafer bows from each wafer pair are used in the figure. Comparing the results in Fig. 8-2 from Tables 8-2, 8-3 and 8-4 (200, 300 and 400 °C, respectively), it is clear that larger wafer bows introduce higher relative dicing failure percentages. The reason is that larger wafer bow creates a longer initial local distance between two surfaces at the beginning of the bonding. The bonding pressure and the interdiffusion process during bonding can decrease and eliminate a small distance between two surfaces. However, when the distance is large, there are still some areas that are not close enough and therefore cannot be bonded well. That also explains that the failure percentage does not change much when the wafer bow is small, but it increases dramatically when wafer bow is large.

In addition, the effect of wafer bow on bonding quality decreases when increasing bonding temperature. At a higher bonding temperature, a higher thermal energy during bonding strengthens the diffusion process within the bonded layer and the bonding quality is further improved. At any wafer bow condition, the effect of the wafer bow can be balanced by higher bonding temperature to improve the bonding quality.

Since Cu wafer bonding is becoming an attractive choice for future three-dimensional integration, the results from this wafer bow investigation offer an important reference for initial wafer selection. In order to achieve high quality bonding, the wafer bow should be considered. By applying the criterion of wafer bow described here, the effect of wafer bow on the bonding quality can be effectively avoided.

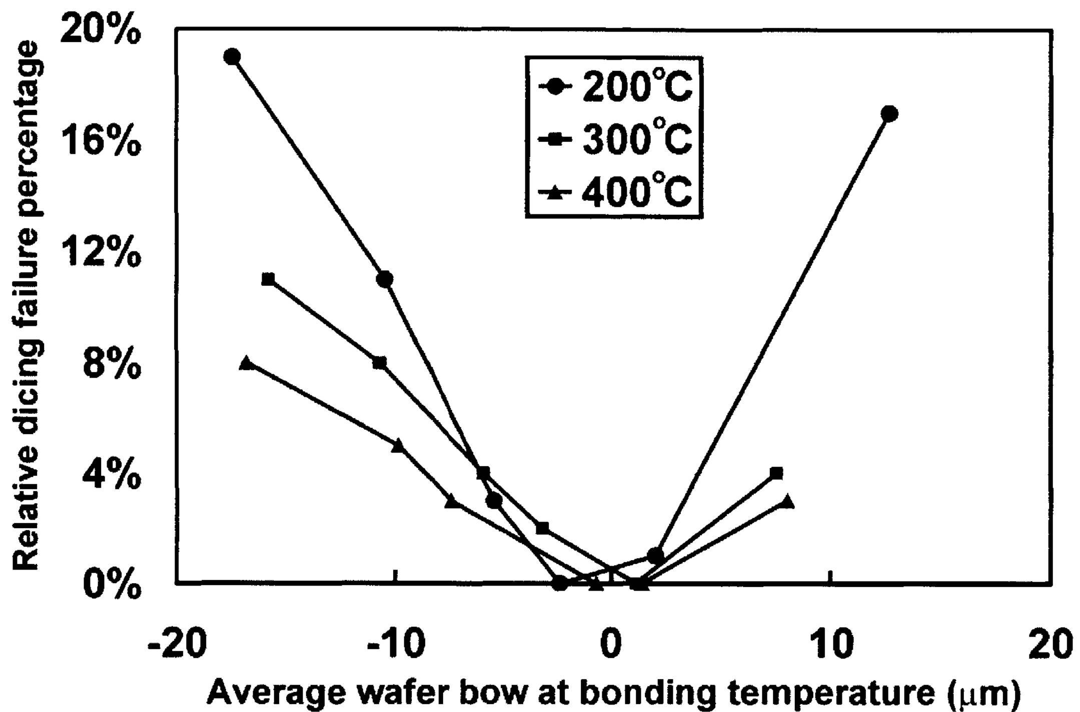


Figure 8-2 The relation of wafer bow and bonding quality at different bonding temperatures. Average wafer bow means the average wafer bow of two wafers to be bonded.

In conclusion, the effects of wafer bow on bonding quality were investigated. The bonding quality degrades with a high wafer bow during bonding. In addition, the effect of the wafer bow is significant at low bonding temperature. When the wafer bow is small, it does not significantly affect the bonding quality. The effect of wafer bow on bonding quality at different bonding temperatures were explored. This criterion can be applied in the future device applications.

Chapter 9

Microstructures of Copper Bonded Interconnects

Chapters 2 to 8 describe research on Cu wafer bonding, which studied the fundamental issues and properties when two Cu blank films, without any patterns, are bonded together. These efforts are quite helpful to understand Cu wafer bonding mechanisms and applications in future technologies. However, if Cu wafer bonding is to be the candidate for future applications, such as 3D ICs, the bonding structures will be small interconnects and not blank films. Therefore, although the bonding parameters of blank Cu films have been developed, it is necessary to study these properties when the bonding structures move from blank films to interconnects. This chapter reports the investigation of morphologies of Cu bonded interconnects. The results show that interconnects as small as 5 μm can be bonded well and that their morphologies were similar to those observed in blank Cu bonded films.

9.1 Sample Preparation and Experimental Procedures

4-inch (100) Si wafers were used in this study. Detailed wafer selection for both sides and the alignment marks process are described in Chapter 2. A series of lithography processes defined the desired interconnects before depositing 50 nm Ta and 300 nm Cu by electron beam deposition. The interconnect sizes ranged from 5 μm to a few hundred μms. Afterwards, Cu interconnects were formed by using the lift-off process by soaking the wafers in Acetone for 4 hrs. Wafers with Cu interconnects then were bonded at 400°C for 30 min followed by nitrogen anneal at 400°C for 30 min. Detailed bonding and anneal experimental process are described in Chapter 2. The morphologies of the Cu-Cu bonded interconnects were examined with a JEOL-200CX scanning transmission electron microscope (STEM), JEOL-2010 transmission electron microscope, and scanning electron microscope (SEM).

9.2 Morphology Observation

Figure 9-1 shows the cross sectional scanning electron microscope (SEM) image of 10 μm-wide bonded interconnects. This image shows that the white area in the middle, which represents copper materials, looks like a layer. In fact, it is the Cu bonded interconnects, which were bonded from two Cu interconnects. Based on the SEM image result, the two interconnects were bonded together and did not separate after the bonding process. The bonded interconnect does not show any obvious original bonding interface in the layer.

A transmission electron microscope (TEM) was used to investigate the detailed

morphologies of bonded interconnects. Figure 9-2 shows the cross sectional TEM image of 5 μm-wide bonded interconnects. Since the purpose of TEM observation is to investigate the interfacial microstructure of bonded interconnects, the width of this bonded interconnect (5 μm) is too large, and only part of the bonded interconnect was shown in the TEM image. From the morphology observation in Figure 9-2, there is no distinguishable bonding interface in the bonded layer after bonding. Instead, a whole layer, with defects and grain structures penetrating the layer, is observed. This morphology is similar to that observed in bonded wafers. It should be noted that the 5 μm-wide bonded interconnects are the smallest feature of bonded interconnects which can be obtained in this research currently. Larger interconnects also have the same SEM and TEM observation results.

9.3 Summary

From the results of Figures 9-1 and 9-2, the bonded interconnects have the similar microstructures and morphologies as those observed in Cu blank films bonding. This means that at the scale of microns the sizes of interconnects do not affect the bonding morphology within the same bonding condition until they are as low as 5 μm. Other performances and properties such as contact resistance and bonding strength will be discussed in the following chapters.

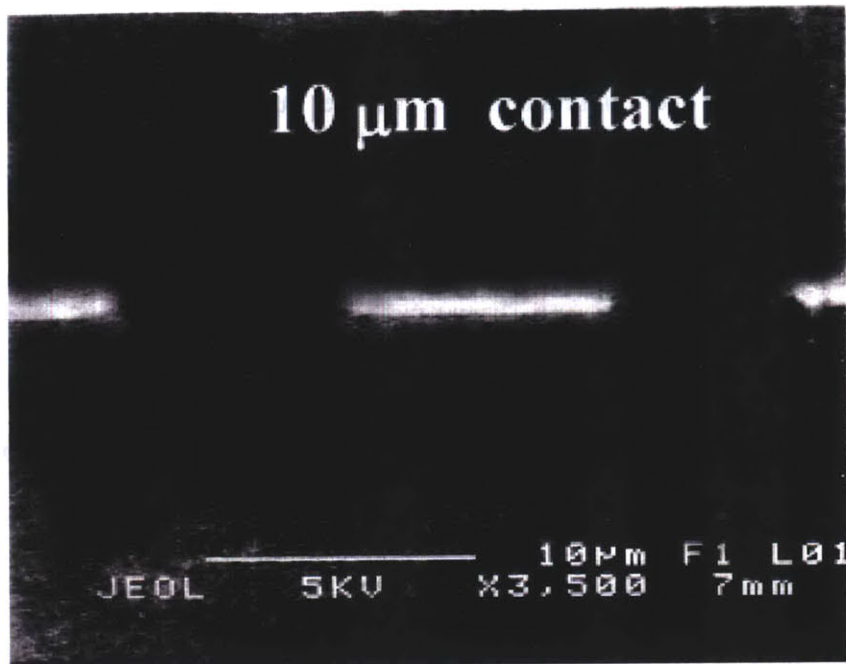


Figure 9-1 SEM image of 10 μm-wide Cu bonded interconnects

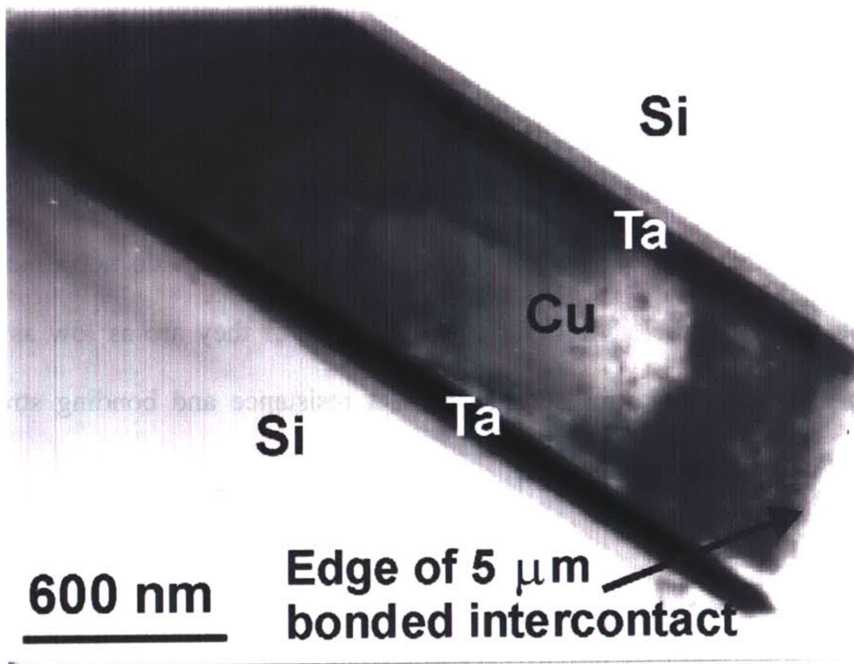


Figure 9-2 TEM image of 5 μm-wide Cu bonded interconnect

Chapter 10

Contact Resistance Measurement of Copper Bonded Interconnects

A novel test structure for contact resistance measurement of bonded copper interconnects in three-dimensional (3-D) integration technology is proposed and fabricated. This test structure requires a simple fabrication process and eliminates the possibility of measurement errors due to misalignment during bonding. Specific contact resistances of bonding interfaces with different interconnect sizes of approximately 10^{-8} Ω-cm^2 are measured. A reduction in specific contact resistance is obtained by longer anneal time. The specific contact resistance of bonded interconnects with longer anneal time does not change with interconnect sizes.

For bonded copper interconnects without a pre-bonding HCl clean, the corresponding specific contact resistance did not change while increasing the stress current. However, for some interconnects with the pre-bonding HCl clean, an abnormal contact resistance reduction was observed during the increase of the stress current. The

rise of temperature at the bonding interface area due to Joule heating under high current density may have caused the decrease of contact resistance.

10.1 A Novel Test Structure for Bonded Interconnect Contact Resistance Measurement

10.1.1 Concept of Design

The schematic diagrams for the contact resistance measurement test structure are shown in Figures 10-1(a), 10-1(b) and 10-2(a). This test structure is similar to a Kelvin contact resistance test structure [90]. The contact resistance can be obtained from:

$$R_C = \frac{V_{MH} - V_{ML}}{I} \qquad (1)$$

where V_{MH} (pad 1) and V_{ML} (pad 2) are measured while a constant current from 1 mA to 100 mA is stressed from pad 3 to pad 4. The specific contact resistance ρ_c can be obtained from:

$$\rho_C = R_C \times A_C \qquad (2)$$

where A_C is the bonded area. Note that the upper and lower metal layers belong to different wafers and the bonded area is constant as designed. In Figure 10-2(b) for the Kelvin test structure, two L-shape metal lines, one belonging to the upper wafer and one to the bottom wafer, would only be contacted in the center area. The resistance of the contact area could be calculated from stressing the current between contact pads 1 and 2 and measuring voltage between pads 3 and 4. However, because of possible misalignment during the bonding process, the contact area A_C may give rise to measurement errors [91], and a reasonably accurate value of specific contact resistance

may be difficult to obtain. Although contact resistance measurements have been developed for years, these measurements are related to conventional devices and cannot solve this misalignment issue [92-99]. In our test structure, the bonding (contact) area does not change with the bonding misalignment. Consequently, a more accurate specific contact resistance can be expected. Figures 10-3(a) and (b) show schematic diagrams of (a) the conventional Kelvin structure with misalignment, and (b) the test structure used in this work.

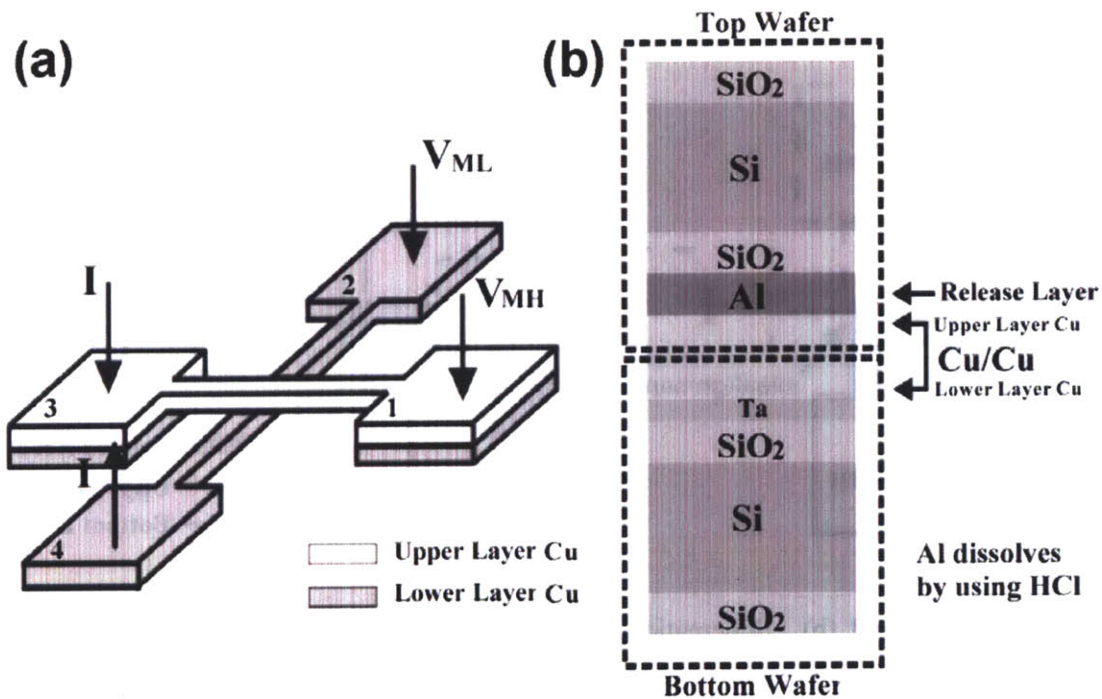
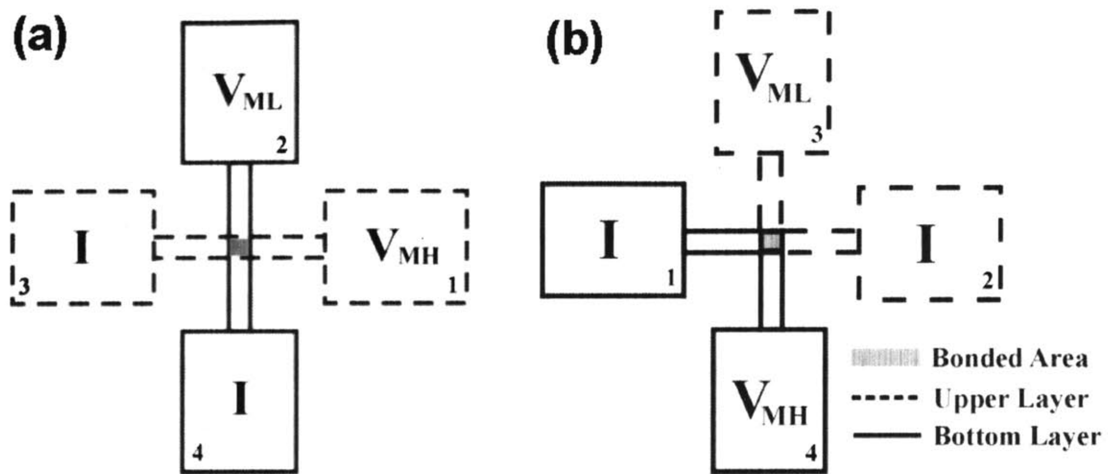
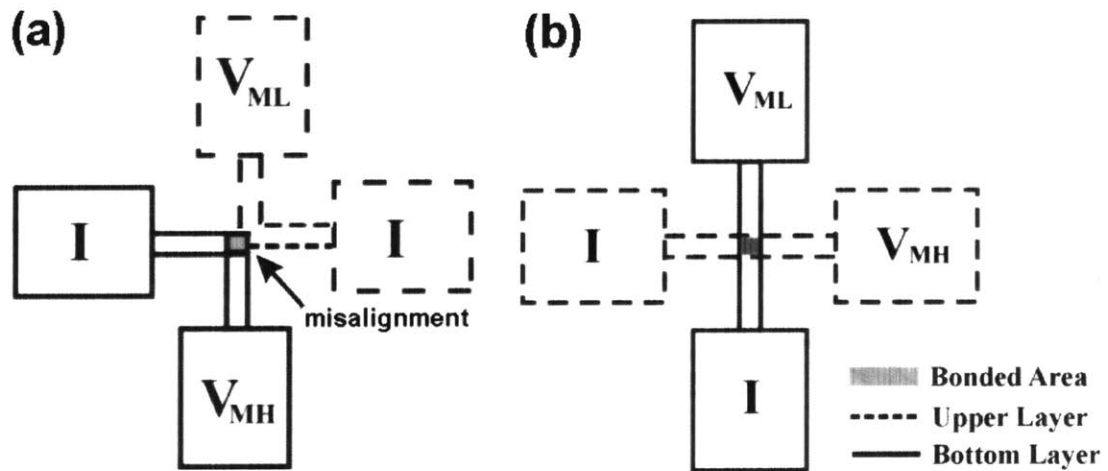


Figure 10-1 Schematic diagram of the contact resistance test structure



Figures 10-2(a) and (b) Top view of (a) our contact resistance and (b) Kelvin test structure.



Figures 10-3(a) and (b) Schematic diagrams of (a) the conventional Kelvin structure with misalignment, and (b) the test structure used in this work.

10.1.2 Fabrication Flow

Figure 10-4 shows the fabrication flow of the test structure for contact resistance measurement. The bottom wafer was covered with 300 nm of thermal oxide, 50 nm of Ta

and 300 nm of Cu. The upper wafer preparation was essentially the same as that of the bottom wafer, except that there was no Ta layer and a 1 μm Al layer was inserted between the thermal oxide and Cu layers. Prior to bonding, half of the wafers were cleaned by dipping in 1:1 (by volume) H_2O:HCl solution for 30 sec followed by a DI water rinse and spin dry. The upper and bottom wafers were bonded face-to-face at 400 °C for 30 min followed by 30 or 60 min of N_2 annealing. Then the substrate of the upper wafer was released to reveal the test structure by soaking the bonded wafer in HCl for 2 hours. Since HCl dissolves Al preferentially over Cu, Ta and SiO_2 [100], the substrate of the upper wafer separated from the bonded wafer pair due to the undercut in the Al layer created by the HCl solution. After releasing the upper substrate, the bonded test structures remained on the bottom substrate and were ready for measurement. For the case of 60 min of N_2 annealing, line widths of 5, 7, 10 and 15 μm were patterned on the upper and bottom wafers. The corresponding bonded areas are 25, 49, 100 and 225 μm^2, respectively. For the case of 30 min of N_2 annealing, line widths of 7, 10 and 15 μm were patterned on the upper and bottom wafers. The total bonded area was 30% of the whole wafer area and the remaining area was air. Surface morphologies of wafers with and without HCl clean process before bonding process were investigated by an Autoprobe CP atomic force microscope (AFM). An HP 4156 Semiconductor Parameters Analyzer was used to ramp a current between 1 mA and 100 mA on the test structures. Figure 10-5 shows top view and dimensions of the test structure.

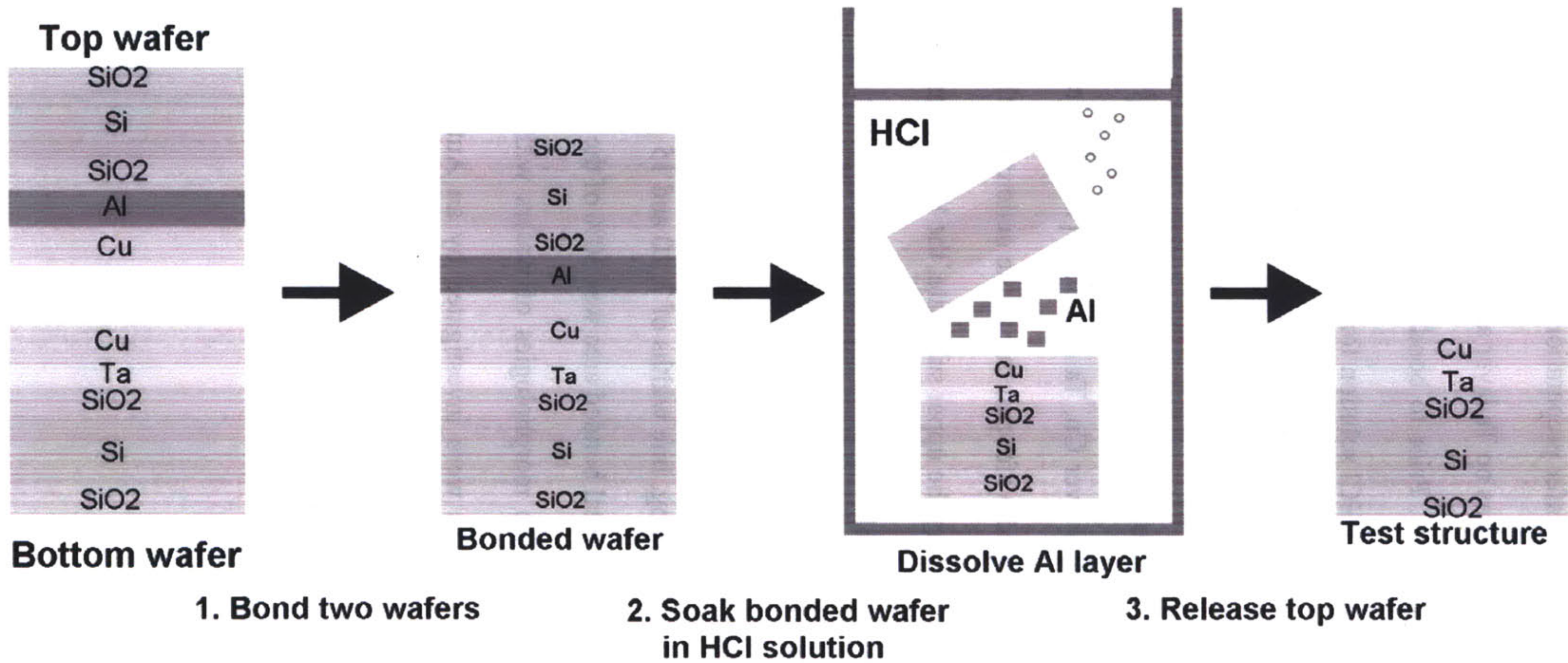


Figure 10-4 The process flow of the test structure for contact resistance measurement

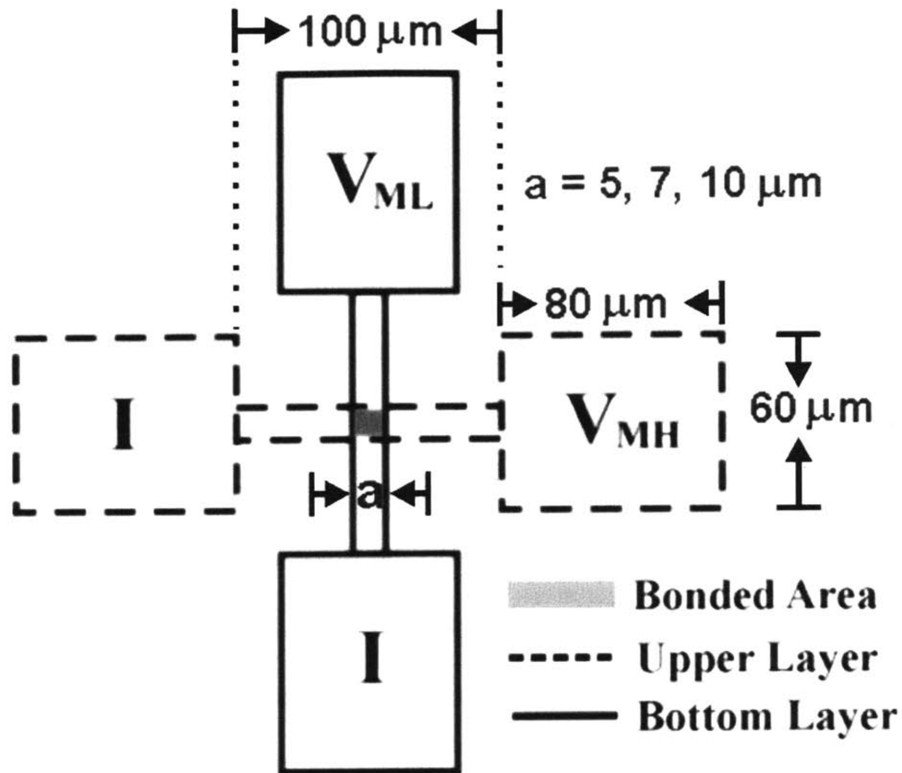


Figure 10-5 Top view and dimensions of the test structure.

10.2 Measurement Results

10.2.1 Different Bonding Conditions

Figure 10-6 shows the measured specific contact resistances of bonded interconnects under two bonding conditions: (1) 400 °C bonding for 30 min followed by 400 °C N_2 anneal for 30 min, and (2) 400 °C bonding for 30 min followed by 400 °C N_2 anneal for 60 min. Table 10-1 shows our measured data for Cu-Cu contacts bonded at 400 °C for 30 min followed by 400 °C N_2 anneal for 60 min, and data from the literature for metal-metal

and metal-Si contact resistances and specific contact resistances [101, 102]. By comparing these three systems, the specific contact resistance of Cu-Cu bonding is smaller than that of the Metal-Si system and is one order of magnitude smaller than that of the Metal-Metal system. A higher value of specific contact resistance in the Metal-Si system is due to the higher barrier height between metal and Si.

For bonded Cu interconnects annealed for 30 min, and for contact areas of 100 μm^2 or larger, the specific contact resistance is approximately 10^{-8} Ω-cm^2. Bonded Cu interconnects with a width of 7 μm shows a higher specific contact resistance. It may be due to an incomplete bonding process and/or due to the presence of a thicker bonded interface with porosities and impurities at the interface. Both of them represent a poorer bonding quality. When the N_2 anneal duration is increased to 60 min, the specific contact resistance decreases significantly. In addition, the contact resistance is independent of contact area after 60 min anneal, while it increases for interconnects smaller than 100 μm^2 after 30 min anneal. This trend is identical to that of the bonding morphology evolution mentioned in Chapter 5.

Previous microstructure examination of Cu wafer bonding showed that the disappearance of Cu-Cu interface after bonding indicated excellent bonding. The existence of the bonding interface results in higher contact resistance. Thus, the low specific contact resistance of the bonded interconnects after 60 min anneal is the result of a better bond quality. This is because the longer heat cycle provides the energy required for the bonded interconnect to refine their interfacial structure.

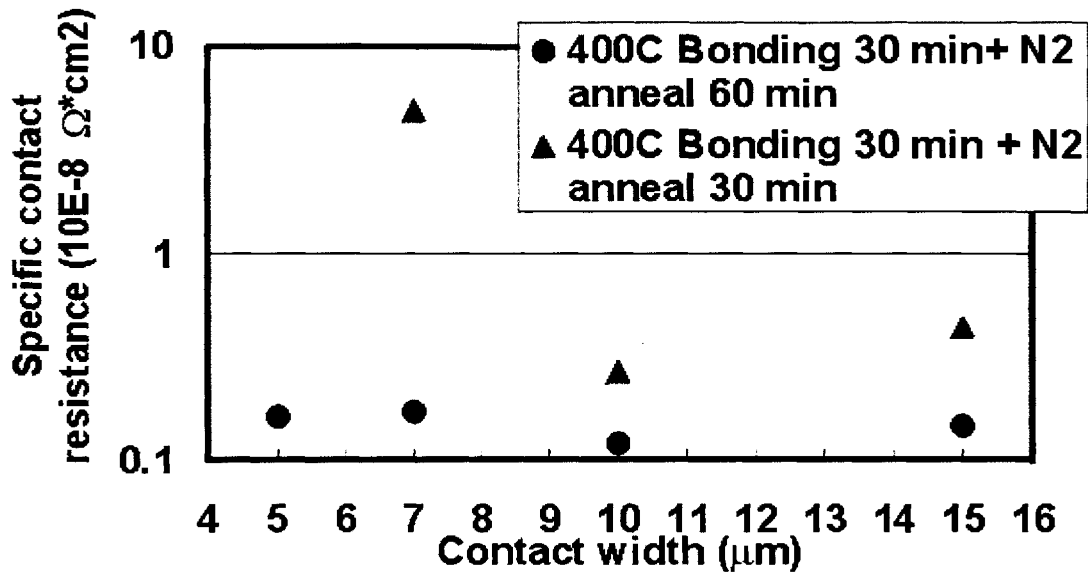


Figure 10-6 Average Cu-Cu bonded specific contact resistances as a function of interconnect size for different bonding conditions

Table 10-1 Comparison of contact resistance and specific contact resistance for Cu-Cu bonding at 400 °C bonding for 30 min followed by 400 °C N_2 anneal for 60 min (this work), metal-metal and metal-Si interconnects [101, 102].

	Interconnect size (μm)	**Specific contact resistance** ρ_c (Ω-cm^2)	Average measured contact resistance R_C (Ω)
Metal-Si	1	$1\text{-}3*10^{-7}$	10-30
Cu-Cu	5	$0.16*10^{-8}$	$6.40*10^{-3}$
	7	$0.17*10^{-8}$	$3.47*10^{-3}$
	10	$0.12*10^{-8}$	$1.20*10^{-3}$
	15	$0.15*10^{-8}$	$6.67*10^{-4}$
Metal-Metal	1	$2*10^{-8}$	2

10.2.2 Stability

Figure 10-7 shows the specific contact resistances of the bonded interconnects without pre-bonding HCl treatment when stress current was applied. The interconnects were bonded at 400 °C for 30 min followed by nitrogen anneal for 60 min, and their sizes are 5 μm. The stress current was ramped gradually from 1 mA to 100 mA at a rate of 1 mA/s then decreased gradually at the same rate. The measurement results show that the specific contact resistance is stable regardless of the applied current, both when the current was increased and decreased. In addition, it suggests that the microstructure of bonded interconnects does not change after stressing current and that the microstructure has already reached a final stable state prior to the current test. This behavior was also observed in the 7 and 10-μm-wide interconnects.

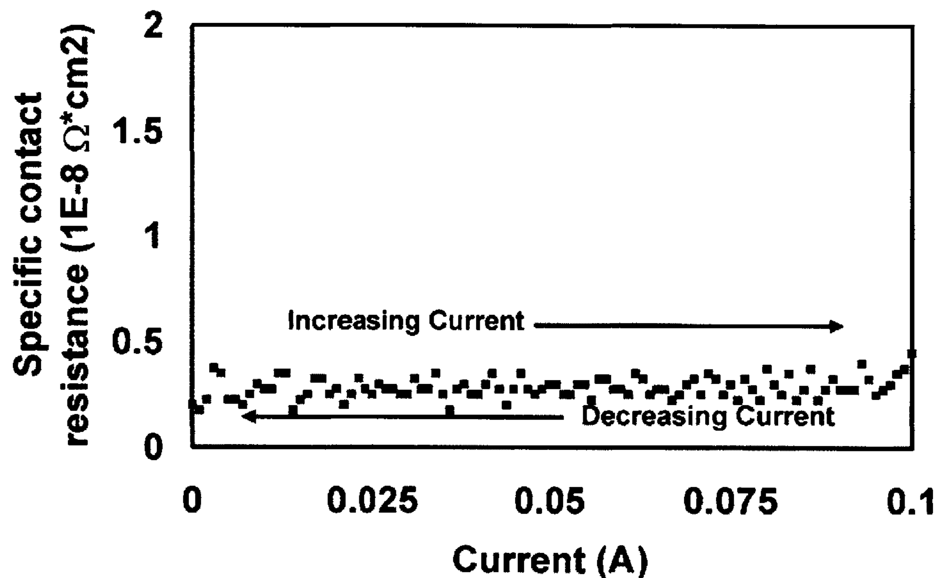


Figure 10-7 The corresponding specific contact resistance of bonded 5-μm-wide interconnects without pre-bonding HCl treatment when stressing current was ramped gradually from 1 mA to 100 mA at the rate of 1mA/s. The interconnects were bonded at 400 °C for 30 min followed by 400 °C N_2 anneal for 60 min.

10.2.3 Electrical Yield

Table 10-2 lists the number of test structures, the number of open-circuit structures, and electrical yield of different interconnect sizes of test structures. Bonding condition was 30 min bonding at 400°C followed by 30 or 60 min nitrogen anneal at 400°C. Samples of each condition were collected from three wafers. Total bonding area was 31.67%. If the test structures did not bond, the test structure became an open circuit during stressing. Electrical yield is defined as the ratio of non-open-circuit test structures to total test structures.

Table 10-2 Electrical yield of different interconnect sizes of test structures. Bonding condition was 30min bonding at 400°C followed by 30 or 60 min nitrogen anneal at 400°C. Samples of each condition were collected from three wafers. Total bonding area was 31.67%.

Interconnect size (μm)	5	7	7	10	10	15	15
Anneal Duration (min)	60	30	60	30	60	30	60
Total samples before testing	98	97	102	99	103	95	101
Working samples during testing	30	31	33	41	44	40	46
Electrical yield	30.6%	32.0%	32.3%	40.4%	42.7%	42.1%	45.5%

Figure 10-8 shows the electrical yield as a function of interconnect sizes for different bonding conditions. The electrical yields are between 30% and 50% and increase with the interconnect sizes. For interconnect bonding, since the local bonding area is isolated

within the interconnect size and total bonding area is smaller than that of the blank copper wafer, the bonding quality of interconnects is not as good as that of the blank copper bonded wafers. A detailed description will be discussed in the next chapter.

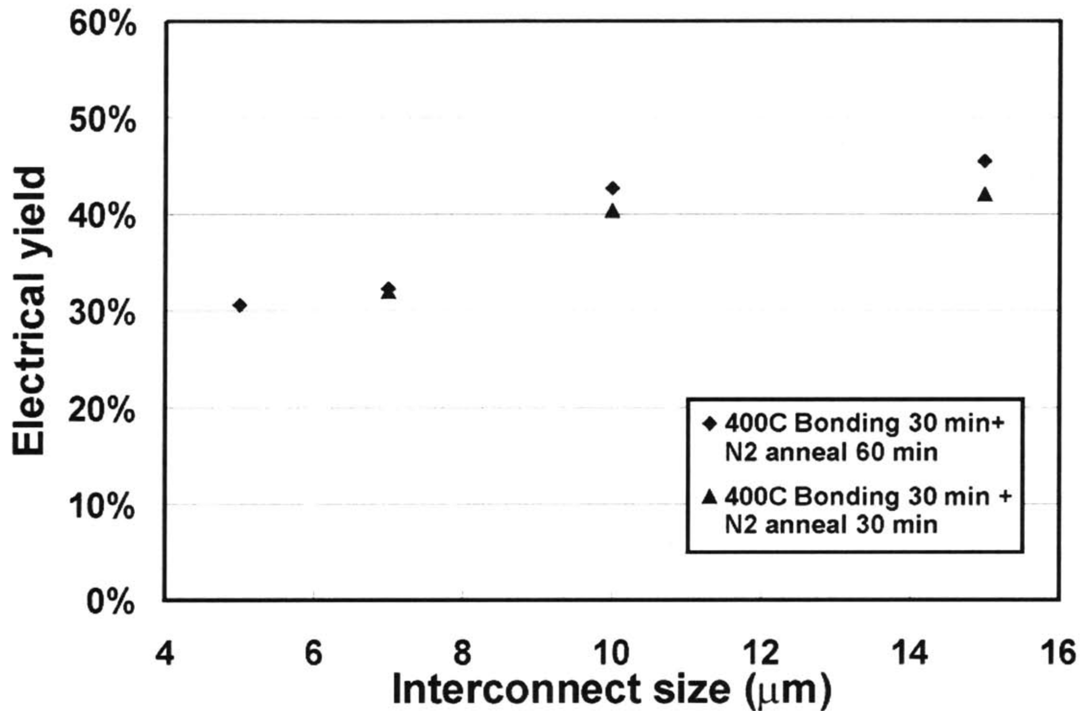


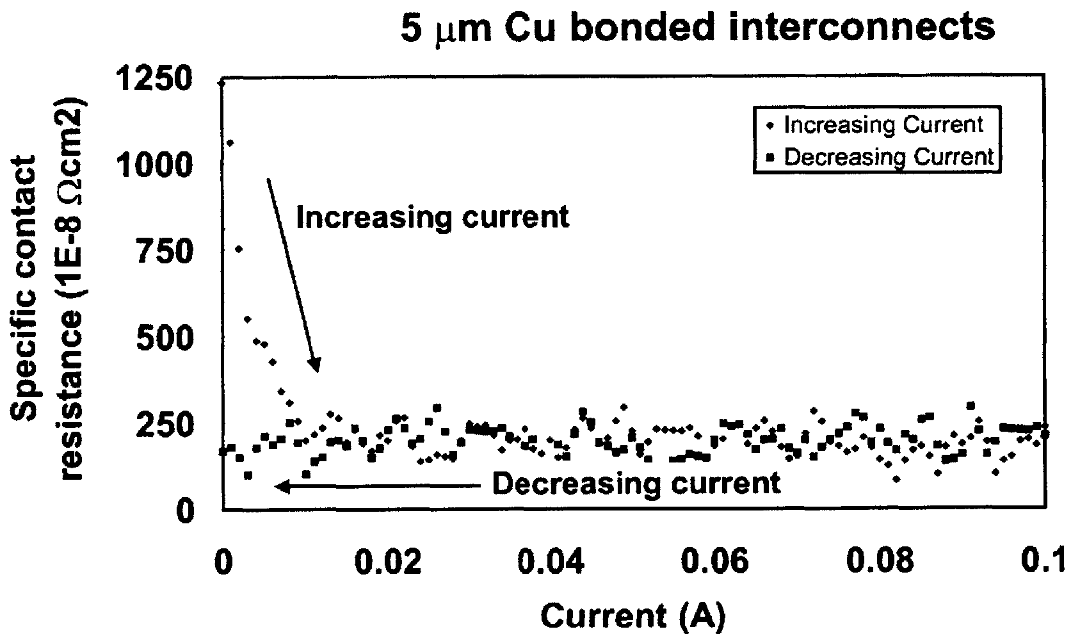
Figure 10-8 The electrical yield as a function of interconnect sizes for different bonding conditions.

10.3 Abnormal Contact Resistance Reduction for During Current Stressing

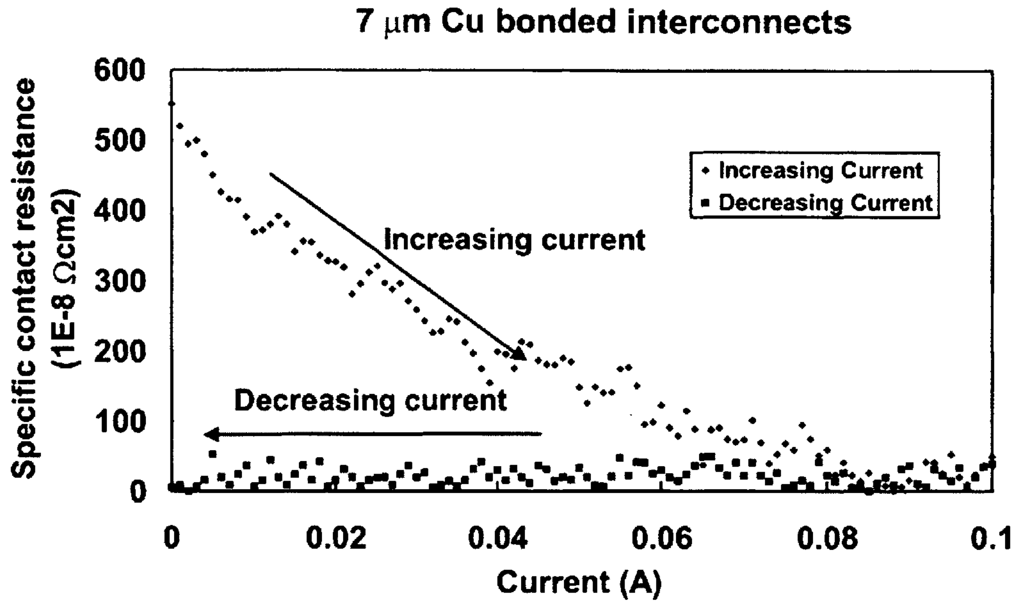
10.3.1 Contact Resistance Reduction

Figures 10-9 (a), (b) and (c) show the corresponding specific contact resistance of bonded

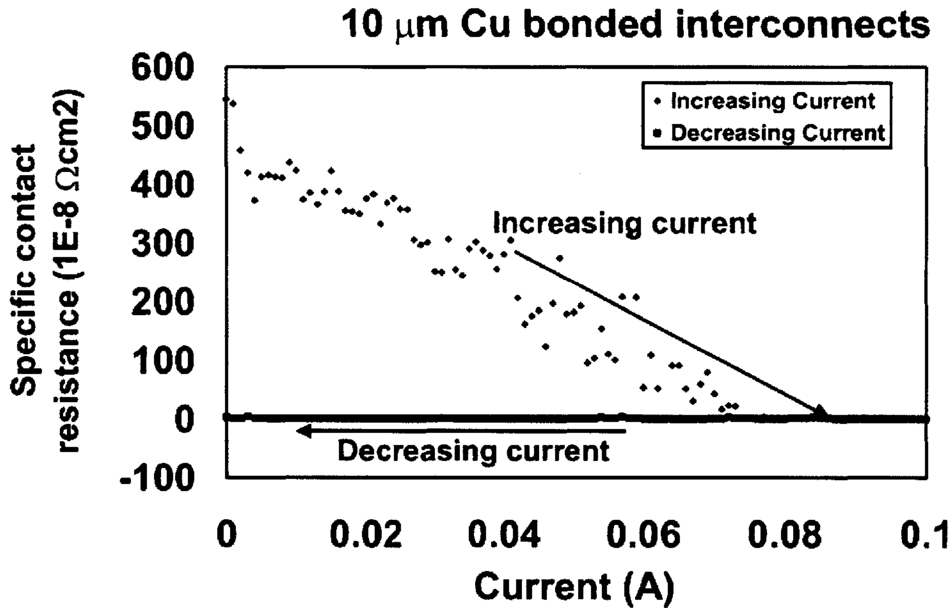
interconnects at the same ramping rate for wafers with 5, 7 and 10-μm-wide interconnects bonded at 400 °C for 30 min followed by 400 °C N_2 anneal for 60 min, respectively. These interconnects were cleaned by HCl prior to bonding. An abnormal gradual contact resistance reduction was observed when the current was ramped from 1 mA to 100 mA. It is also observed that the contact resistance decreases and converges to a constant value at high stress current. After reaching 100 mA, the stress current was decreased gradually back to 1mA. During the decrease of the stressing current, the specific contact resistance remained in the same range and did not change significantly. This phenomenon was observed in some of the three different sizes of interconnects under test. About thirty percent of test samples in each interconnect sizes exhibit this behavior. For the remaining of the bonded interconnects, their contact resistance values stayed stable and in the same range as shown in Figure 10-7.



Figures 10-9(a)

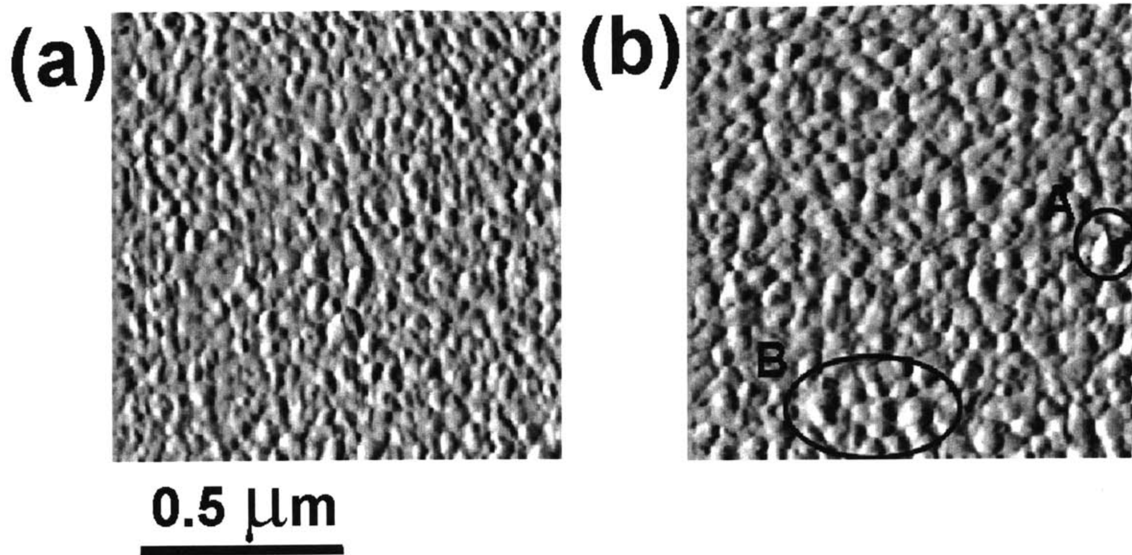


(b)



(c)

Figures 10-9(a)-(c) The corresponding specific contact resistance of some bonded interconnects with pre-bonding HCl clean at the rate of 1mA/s for wafers with (a) 5, (b) 7 and (c) 10 μm-width interconnects bonded at 400 °C for 30 min followed by 400 °C N_2 anneal for 60 min.



Figures 10-10 (a) and (b) AFM surface morphologies of Cu interconnects (a) without and (b) with HCl clean before bonding. "A" area shows an abrupt peak and "B" area represents a generally rough area

10.3.2 Surface Morphology and Roughness Investigation

In order to explain the abnormal contact resistance reduction, the surface morphologies and roughness of Cu interconnects were investigated prior to bonding. Figures 10-10(a) and (b) show the surface morphology of Cu interconnects without and with HCl clean before bonding, respectively. A smooth and flat surface was observed in interconnects without HCl cleaning as shown in Fig. 10-10(a). However, figure 10-10(b) shows that a rough surface with peaks and valleys was observed in interconnects with HCl cleaning. For instance, "A" area shows an abrupt peak and "B" area represents a generally rough area in Fig. 10-10(b). AFM investigation also estimated that the surface RMS roughness of Cu interconnects without HCl clean was 1.15 nm while that with HCl clean was 1.55 nm. Therefore, from both the surface morphology observation and surface roughness estimation, Cu interconnects with HCl clean show the rougher surface. This is because

oxides formed on the copper surface depend on the original surface morphology. It is reasonable to believe that the oxides on the surface may not be uniform and some oxides may even form along the grain boundaries and defect areas. Therefore, during the HCl clean, when the oxides were removed, rough morphologies in some areas was created.

10.3.3 Possible Mechanism

A contact resistance smaller than 10^{-8} Ω-cm^2 was measured for interconnects without HCl clean at this bonding condition as shown in Fig. 10-7. In addition, it is also suggested that the bonding morphology at the interface has already reached a steady state. Therefore, the specific contact resistance remained in the same range of value while stressing current was being applied. However, for the bonded interconnect with HCl clean, the surface roughness is higher than that without HCl clean and especially there are high rough shapes such as peaks in some areas, which may hinder the bonding process. Therefore, it is reasonable to assume that under this condition there are still defects after bonding and voids remain in the interface for some of the bonded interconnects, and these defects introduce a high value of the contact resistance.

When the bonded interconnects are stressed with electric current, Joule heating takes place. Since the amount of heat generation is proportional to the resistance, a high value of heat is generated in the region of the bonded interface area that has a high value of contact resistance. Therefore, when the bonded interconnects were stressed with current gradually, the generated heat increased and the temperature near the bonded interface became high. At this stage, atoms including copper and other defects around the bonded interface will all have relatively high diffusivities. In order to relieve this high

temperature and reach low system energy, the structures near the interface rearranged thus contributing to the decrease in resistance. This rearrangement process continued and the contact resistance keeps decreasing while the stressing current increases gradually. This phenomenon can also be observed in some welding systems for large species joint [103-107]. However, when the resistance reaches a value that is small enough and the heat generated around the interface cannot support further atomistic rearrangement, the contact resistance would stop decreasing and stay in a stable value. After a stable value of contact resistance was reached, the interface achieved a stable state. Therefore, the contact resistance did not change after further decreasing stress current.

10.3.4 Interconnect Sizes

From Figs. 10-9(a), (b) and (c), it is observed that the stressing current needed to reach a stable state increases when the size of bonded interconnects increases. Since larger bonded interconnect sizes have smaller current density under the same stress current, a higher stress current is necessary to complete the rearrangement process. In addition, it is found that the final value of stable specific contact resistance decreases with increasing the interconnect sizes. This is because under the same bonding condition, some interconnects with HCl clean may not complete the bonding process and may still have defects in the interface area. It has been shown that smaller bonded interconnects have higher specific contact resistance if the bonding state is not complete prior to the current test.

10.4 Summary

A novel and simple test structure for contact resistance measurements of Cu interconnect bonding interface was developed. This approach eliminates the measurement error due to misalignment during wafer bonding. Contact resistances under different bonding conditions were investigated. A reduction of contact resistance is obtained by longer anneal time since the bonded interconnects have more energy to refine the interfacial structure. In addition, the specific contact resistances of bonded interconnects with longer anneal time do not change with interconnect sizes.

Stable contact resistance results were found in interconnects without pre-bonding HCl clean when stressing current is ramped. Abnormal contact resistance reductions were found in some bonded interconnects with pre-bonding HCl clean while the stressing current was ramped up gradually. Afterwards, the contact resistance of these interconnects stayed at a stable value even the stressing current was increased further. The contact resistance reduction may be resulted from the high temperature heating of interface due to the high electrical current.

Since a lower processing temperature is an important consideration for future device and materials processing [108, 109], this improvement of electrical performance (contact resistance reduction) by stressing high current may be one option for quality enhancement of 3-D integration process at low temperature.

Chapter 11

Bonding Quality of Copper Bonded Interconnects

The results in previous chapters show that bonding quality depends on actual bonding strength, which comes from the contact of bonding areas between two layers. Two factors of bonding area can be considered: one is local bonding area, which is decided by interconnects size; the other one is total bonding area, which is the total Cu area on the wafer, which is decided by interconnects size and numbers. In order to investigate the relation of the quality of Cu bonded interconnects and these two factors, sizes of Cu interconnects and total bonding area were considered separately. One case is that total bonding area was fixed to study different sizes of Cu interconnects, while the other is to keep the size of interconnect the same and study the bonding quality of different total bonding area.

In addition, in three-dimensional integrated circuits, copper bonding has two major contributions: one is electrical connectivity, which is known as the use of interconnects;

and the other is mechanical support, which can be obtained from the use of interconnects and dummy pads. A comparison of the bonding quality between the same interconnects placement with and without Cu dummy pads was carried out in this study.

11.1 Different Sizes of Copper Interconnects

11.1.1 Parameter Choice and Experimental Procedures

To study the effects of Cu interconnect size on bonding quality, total bonding area were 25% and 66% of the wafer size. For the case of 25% of the total bonding area, 5-μm, 10-μm, 60-μm, and 150-μm-wide Cu interconnects were patterned on different wafers. The corresponding air space between two interconnects were 5, 10, 60, and 150 μm wide. For the case of 66% of the total bonding area, 60-μm, 150-μm, and 8-mm-wide Cu interconnects were chosen. The corresponding air space between two interconnects were 14 μm, 34 μm, and 1.8 mm wide. Thus, a regular square array pattern was formed on each wafer.

Four-inch (100) Si wafers were used in this study. Detailed wafer selections for both sides and the alignment mark process are described in Chapter 2. A series of lithography process defined the desired patterns before depositing 50 nm Ta and 300 nm Cu by the electron beam deposition. Afterwards, Cu interconnects were formed by using the lift-off process to soak the wafers in Acetone for 4 hrs. Wafers with Cu interconnects were then bonded at 400°C for 30 min followed by nitrogen anneal at 400°C for 30 min. The detailed bonding and anneal experimental processes are described in Chapter 2. A dicing

test was performed on the bonded wafers to investigate the bonding quality. Dicing process and method of describing bonding quality are described in Chapter 7. The experimental procedures will also be applied in the other sections in the current chapter.

11.1.2 Bonding Quality Examination

Figure 11-1 shows the bonding percentage of different Cu bonded interconnect sizes. Both 25% and 66% of the total bonding area cases are included. For the 5- and 10-μm-wide Cu interconnects with an area of 25% of total bonding area, the average bonding percentages are 38% and 42%, respectively. For areas of 25% and 66% of total bonding area, both of average bonding percentages reach values between 60% and 80% for the 60- and 150-μm-wide Cu bonded interconnects. When the Cu interconnects size is 8 mm with an area of 66% of total bonding area, the average bonding percentage has a good result of 95%.

These results show that the bonding percentage increases with interconnect size. When two interconnects approach bonding, the larger local area (interconnect size) has the advantage of acquiring the larger amounts of the initial bonds. In addition, it is found that the larger interconnect size, the better the bonding support within the local area. Therefore, wafers with larger interconnect sizes tend to acquire better bonding percentages when the total bonding area is kept at the same value.

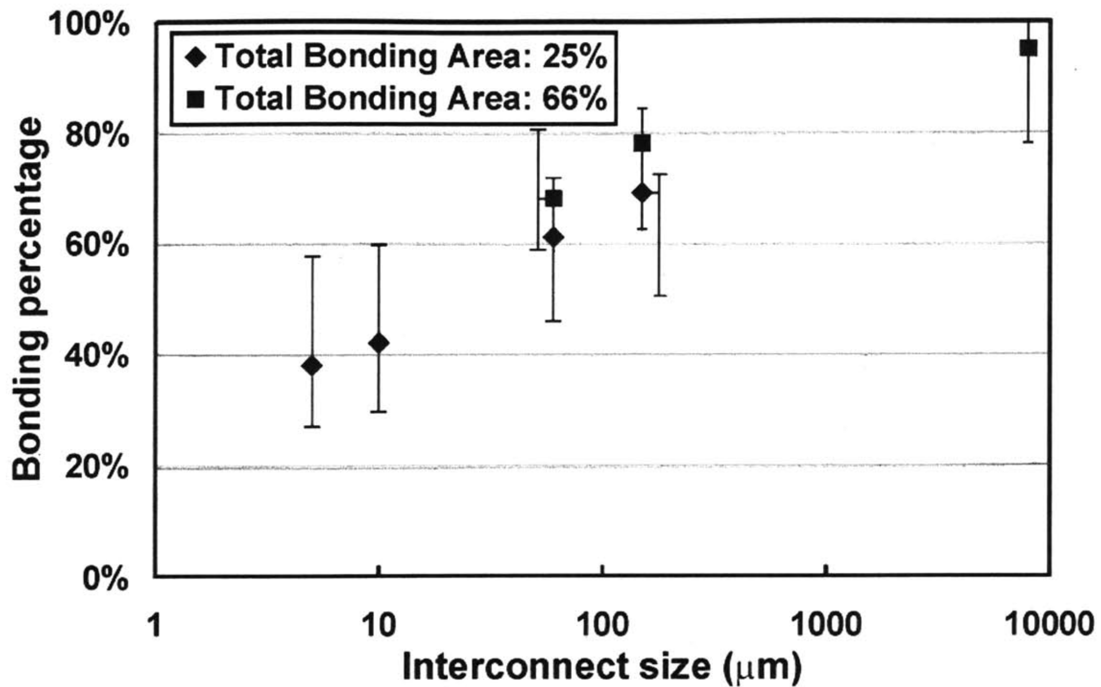


Figure 11-1 The relation of bonding percentages and interconnect sizes under different total bonding areas. Bars represent range of data, and offset from the average point for visual conveniences.

It should be noted that for the 5- and 10-μm-wide Cu interconnects the variations of the bonding percentage are larger than those for other sizes. The reason is possibly due to the wafer bow and the surface condition. For smaller interconnects, since the initial contacts within the local bonding area are limited, other factors such as the wafer bow and the surface roughness, which also can affect the initial contacts, becomes significant for the bonding quality. Therefore, any large wafer bow and bad local surface roughness during bonding will decrease the number of initial bonding contacts and further hinder the bonding evolution. A large variation in bonding percentage can be seen for small interconnects.

In addition, for the same interconnect sizes (60 μm and 150 μm), the higher total

bonding area (66%) shows a better bonding percentage than that of the lower total bonding area (25%). A detailed discussion is in the next section.

11.2 Different Bonding Areas

11.2.1 Choice of Parameters

To study the effects of total bonding area, areas of 25% and 44% of total bonding areas were designed for bonding quality examination. Three interconnect sizes (10 μm, 60μm, and 150 μm) of Cu interconnects were chosen for the bonding. The corresponding air space between two interconnects for 25% of total bonding area were 10, 60, and 150 μm, respectively. The corresponding air space between two interconnects for 44% of total bonding area were 5, 30, and 75 μm, respectively.

11.2.2 Bonding Quality Examination

Figure 11-2 shows the bonding percentage of different total bonding areas. 10 μm, 60μm and 150-μm-wide Cu interconnect cases are included. For the 10-μm-wide Cu interconnects, the average bonding percentage with a 25% of total bonding area is 42%, while that with a 44% of total bonding area becomes 50%. The average bonding percentages reach between 61% and 63% for the 25% and 44% of total bonding area with 60-μm-wide Cu interconnects. When the Cu interconnect size is 150 μm, with a 66% of total bonding area, the average bonding percentages with a 25% and 44% of total

bonding area are 60% and 62%, respectively.

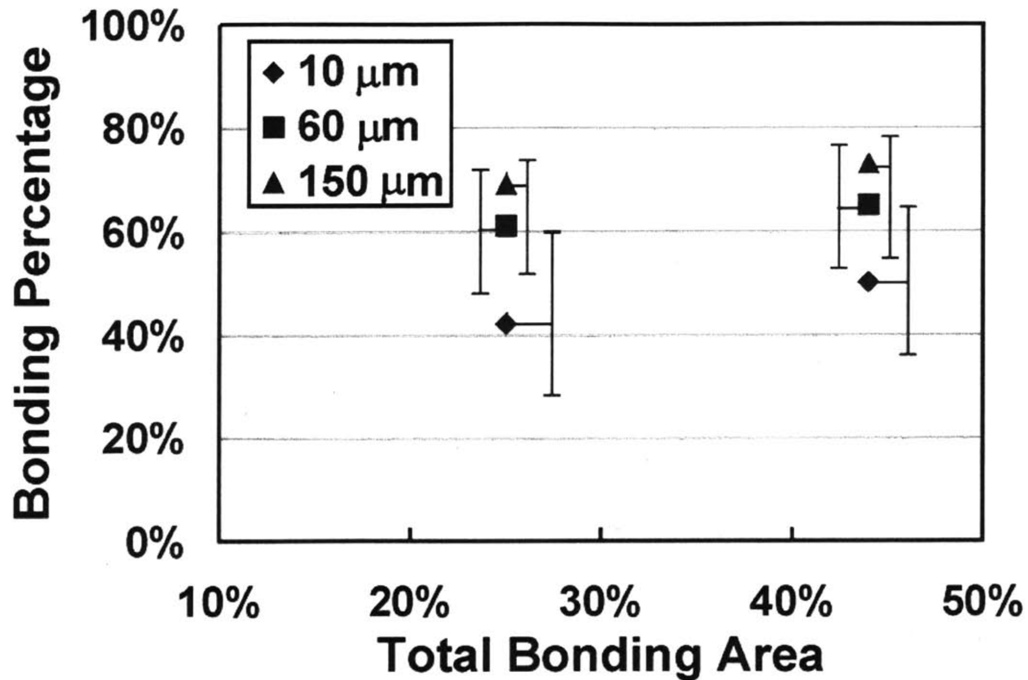


Figure 11-2 The relation of bonding percentages and total bonding areas under different interconnect sizes. Bars represent range of data, and offset from the average point for visual conveniences.

These results show that the bonding percentage increases with total bonding area, but the percentage is not as large as that caused by interconnect size. For wafers with a higher percentage of total bonding area, there is more area available for bonding. This means that the total support through the wafer is larger. Therefore, wafers with higher total bonding area can lead to higher bonding percentages when the Cu interconnect size is kept at the same value.

A comparison of the enhancement of bonding quality by changing the total bonding areas and interconnect sizes appears to show that increasing the interconnect size increases the bonding percentage more effectively than increasing the total bonding area.

However, it should also be noted that the total bonding area is only increased from 25% to 44% (1.7 times), while the interconnect size is increased from 5 μm to 60 μm (12 times) and eventually reaches 8 mm (1600 times). Therefore, the size factor is perhaps the reason that the effects of increasing the total bonding area are not as obvious as those of increasing the interconnect size. Hence, for smaller interconnect sizes the bonding quality enhancement is made greater by increasing the total bonding area from 25% to 44%.

The results in 11.1 and 11.2 show that both interconnect size and total bonding area influence the bonding percentage. Interconnect size seems to have a stronger effect than total bonding area on the bonding percentage. When processing interconnects bonding, the best strategy is to increase the interconnect size and total bonding area at the same time. In addition, in order to get the best bonding quality, the interconnect size should be as large as possible. Detailed studies will be necessary to examine the effects of interconnect size and total bonding area quantitatively in the future..

11.3 Bond Quality Enhancement by Adding Dummy Pads

11.3.1 Placement Design and Parameter Choice

In 3-D ICs design, the bonded interconnects, which connect two different active silicon layers, do not occupy the whole area of the wafer. After subtracting the area of interconnects and their corresponding air gaps, how to effectively use the remaining area becomes significant. Since Cu wafer bonding not only offers electrical connectivity but also mechanical strength of structure, placing dummy pads in these remaining area seems

a good option.

Figure 11-3 shows the schematic diagrams of normal design for placement of electrical interconnects only and a new design for placement of electrical interconnects and dummy pads at the same wafer. The new design with dummy pads has a larger bonding size and a larger total bonding area. According to previous results, larger bonding sizes and larger total bonding areas introduce better bonding quality.

Two cases were considered to investigate the bonding percentage for different designs. Case 1 has Designs A and B, which both have 5-μm-wide interconnects for electrical connectively. Design A only has 5-μm-wide interconnects with a 6.25% total bonding area. Design B not only has the same interconnect placements as Design A, but also has the dummy pads in the remaining area. The size of the dummy pads is larger than the interconnect size. The total bonding area of Design B is 50.00%.

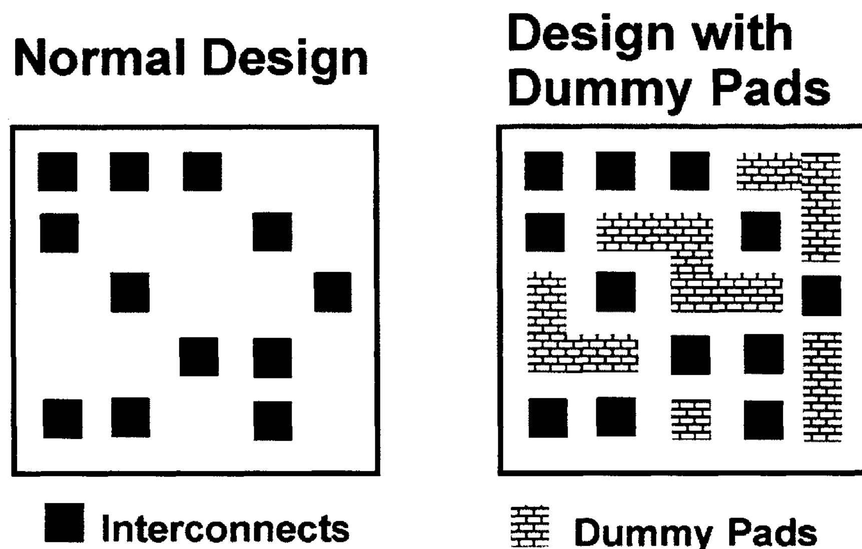


Figure 11-3 Schematic diagrams of normal design for placement of electrical interconnects only and a new design for placement of electrical interconnects and dummy pads on the same wafer.

Case 2 has Designs C and D, which both have 10-μm-wide interconnects for electrical connectively. Design C only has 10-μm-wide interconnects with an area of 11.11% of total bonding area. Design D not only has the same interconnects placement as Design A, but also has the dummy pads in the used area. The size of dummy pads is larger than the interconnect size. The total bonding area of Design B is 66.66%.

It should be noted that the purpose to choose low total bonding areas in these two cases is to identify the effect of the new design. After bonding, dicing test was performed on the bonded wafers to investigate the bonding quality.

11.3.2 Bonding Quality Examination

Figure 11-4 shows the bonding percentage using different designs under different total bonding areas. Interconnects in Case 1 and Case 2 are 5 μm and 10 μm, respectively. Designs A and C are normal designs with interconnects only, while Designs B and D are new designs with interconnects and dummy pads on the same wafers.

From the results in Figure 11-4, it is obvious that Designs B and D (new design) have better bonding percentage than Designs A and C (normal design). The improvement of bonding percentage may be from larger dummy size, or larger total bonding area, or both. By using the dummy pads, the bonding percentage of 5 μm and 10 μm interconnects can be effectively increased to more than 50%.

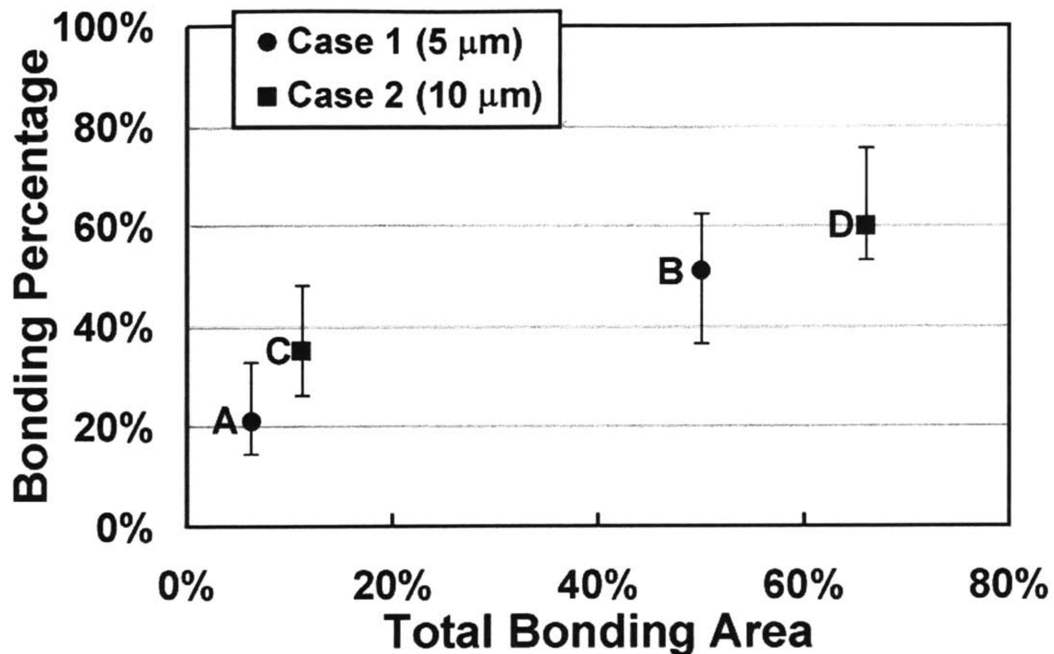


Figure 11-4 The relation of bonding percentages and different designs of interconnects and dummy pads using different interconnect sizes. Bars represent range of data, and offset from the average point for visual conveniences.

Although the improved bonding percentages are not 100%, there are several approaches to reach a better performance. As previously discussed in this chapter, small interconnects are sensitive to wafer bow and surface condition during wafer bonding. It is important that wafers are flat and clean. In addition, increasing the bonding temperature and duration can also enhance the bonding strength. If bonding parameters cannot be increased because of the requirements of the process, proper interconnect placement design combining the dummy pads may improve the bonding quality.

11.4 Summary

From the results of studies of different interconnect sizes and total areas for bonding, it is

founded that the bonding quality improves with the increase of the interconnect sizes or total bonding area. The effect of interconnect sizes is larger than that of total bonding area. When the requirement of interconnect size is not stringent, the interconnect size can be increased to improve the bonding quality. At the same time, increase of the total bonding area is another option to enhance the bonding strength. In addition, the results in previous chapters about flat and clean surface prior to bonding are also significant.

In summary, the criteria to obtain an excellent interconnect bonding qualities are flat and clean wafer selections, long bonding duration or high bonding temperature if possible, larger interconnect sizes or total bonding area, and use of dummy pads for bonding in the unused area.

Chapter 12

Process Development of Silicon Layer Stacking Based on Copper Wafer Bonding

This chapter reports that the process development of silicon layer stacking based on Cu wafer bonding, SOI grind back, and etch back was successfully applied to demonstrate a strong four-layer-stack structure. Bonded Cu layers in this structure became homogeneous layers and did not show original bonding interfaces. This process can be used in three-dimensional integrated circuit applications.

12.1 Fabrication Flow and Other Experimental Procedures

N-type 100 mm Si (100) wafers were used in this experiment. The thickness of these wafers were in the range of 500 – 550 μm. Figure 12-1 describes the fabrication flow:

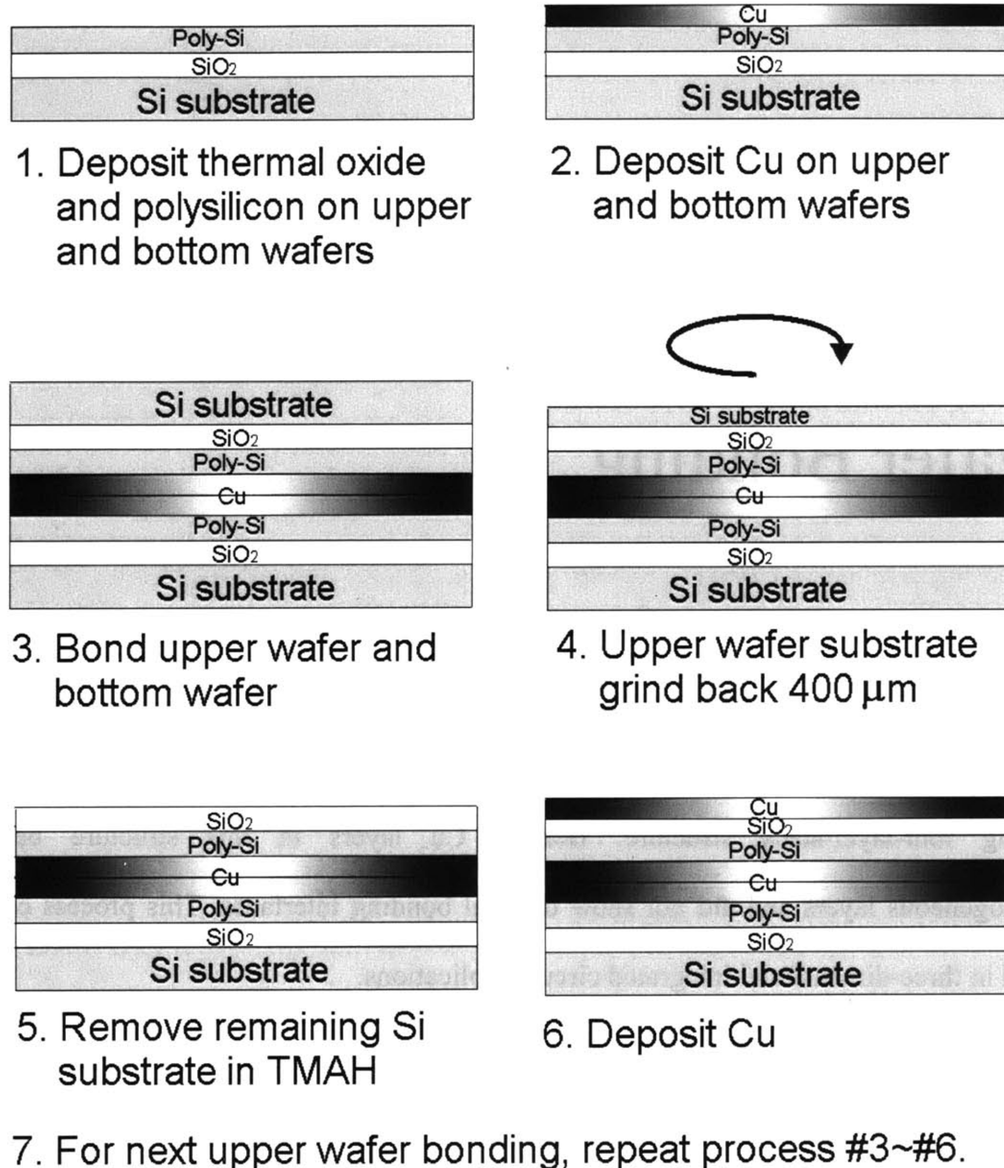


Figure 12-1 Schematic diagram of fabrication flow for the bonded structure

1. SOI dummy structures were prepared by growing 500 nm of thermal oxide as buried oxide (BOX) followed by deposition of 400 nm of polysilicon at 620°C using silane source low-pressure-chemical-vapor-deposition (LPCVD). The purpose of choosing SOIs in the process is to use buried oxide as etch stop during chemical etching[110].
2. 50 nm Ta and 300 nm Cu were then deposited on SOI dummy structure by electron beam evaporation. The Ta layer is the diffusion barrier for Cu. The vacuum during depositions was maintained to be better than 2×10^{-6} Torr. The deposition rate was about 0.3 nm/sec.
3. Two identical wafers with SOI dummy structure and Cu/Ta layers were chosen for bonding process. One wafer was denoted as upper wafer and the other one was denoted as bottom wafer. Prior to bonding, the wafers were dipped in 1:1 (by volume) H_2O:HCl for 30 s followed by a DI water rinse and spin dry to remove the native oxide on the Cu surface. The two wafers were bonded face to face in an Electronic Vision EV 620 Aligner and AB1-PV under a pressure of 4000 mbar for 60 min at 400°C in the ambient of 10^{-3} torr. The bonded wafer pair was then annealed at 400°C in a diffusion furnace in N_2 ambient for 60 min. Detailed bonding and anneal process are described in Chapter 2.
4. The substrate of the upper SOI dummy wafer was then mechanically grinded back. The remaining Si substrate thickness of the upper wafer was around 100 – 150 μm. Therefore, the mechanical grind back did not destroy the buried oxide (BOX) and other structures.
5. Wet silicon etchants such as KOH and TMAH (tetramethylammonium hydroxide) are known to have excellent selectivity towards thermal oxide [51-52]. In this process, the remaining Si substrate of the upper wafer was removed by soaking the bonded wafer

in a 12.5% TMAH solution at 85°C. The etching stopped at the buried oxide

6. The bonded wafer was again deposited with 50 nm Ta and 300 nm Cu thin films above the buried oxide of the upper wafer. Afterwards, this bonded wafer can be used as the "bottom" wafer as described in step 2 and ready to be bonded with another upper wafer.
7. Repeat the fabrication flow steps 3 to 6 for next wafer bonding, grind back and etch back.

The morphologies of the whole bonded wafer structure were examined with a JEOL-2010 transmission electron microscope.

12.2 Two-Layer-Stack Structure

12.2.1 TEM Observation

Figure 12-2 shows the cross sectional transmission electron microscopy (TEM) image of the two-wafer-bonded structure after grind back, etch back and Cu/Ta deposition process. This figure is the result of step 6 in the fabrication flow. The substrate of the second wafer (upper wafer) has been removed. In addition, Cu/Ta metal films have been deposited as the second metal layer. A 200-nm-Si film was deposited by electron beam evaporation prior to Cu/Ta metal film depositions. This Si film is optional. The Cu bonded layer in Fig. 12-2 shows the two Cu films have became a single layer without the original bonding interface. The strong bonding of the two Cu films and the excellent adhesion of each layer make the whole structure appear as a single wafer after sequential thin film depositions.

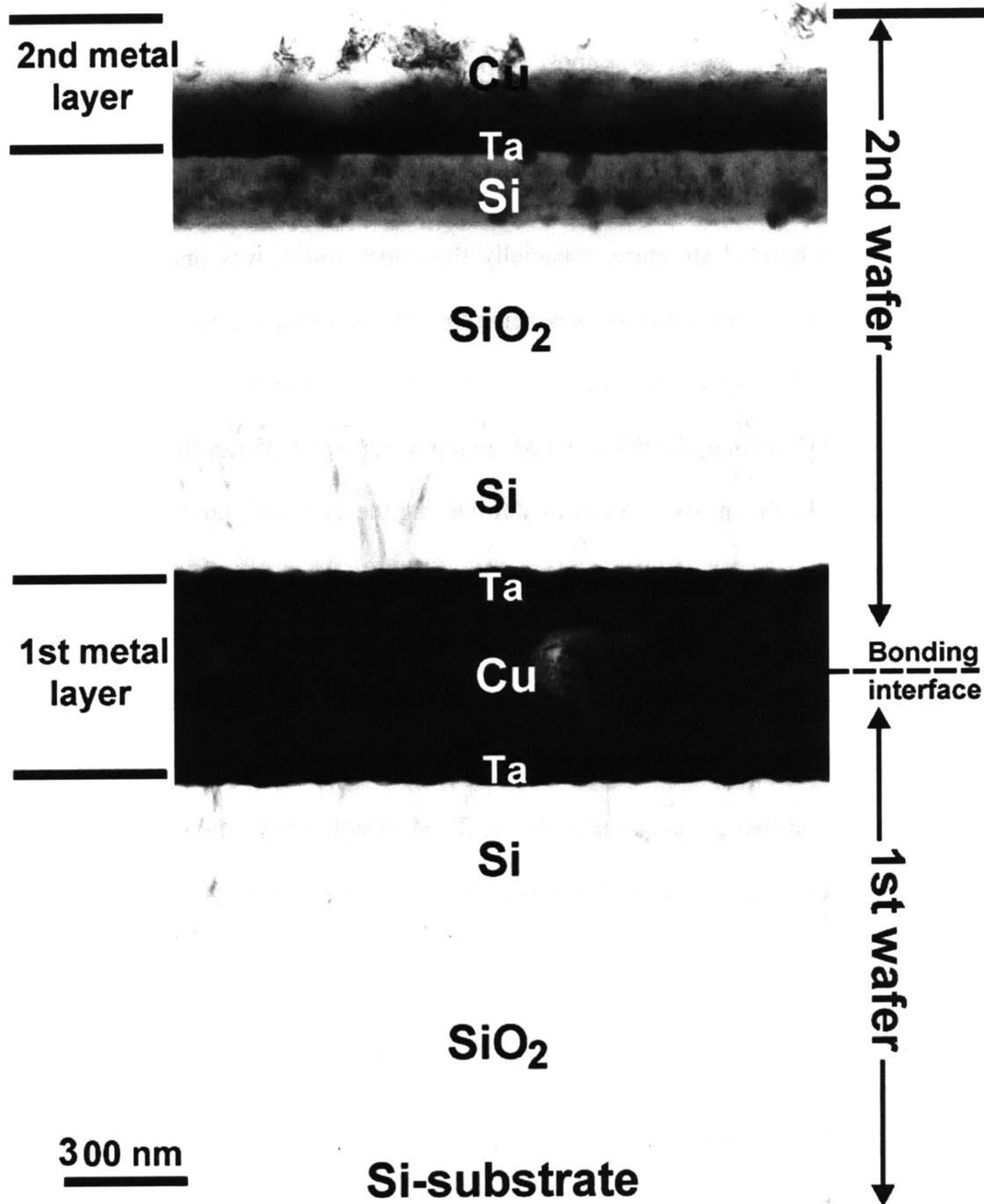


Figure 12-2 TEM image of a two-wafer-bonded structure after grind back, etch back and Cu/Ta deposition.

12.2.2 Discussion

In previous results, we have shown that a good Cu wafer bonding pair not showing the original interface can be achieved at 400°C followed by a nitrogen anneal. However, the previous bonded structure was achieved without grind back and etch back, while the bonded structure in this research were subjected to both of these processes. In the grind back process, the bonded structure, especially the upper wafer, was under continuous mechanical stress while the substrate was being thinned. Afterwards, before the aqueous chemical etching, the upper wafer became a 100-μm-thick film bonded to the bottom wafer. After TMAH etching, the thickness of the top wafer was 1.25 μm (0.3 μm Cu, 0.05 μm Ta, 0.4 μm polysilicon, and 0.5 μm oxide). During the etch back process, if the bond quality was not strong enough, the upper wafer would separate from the bottom wafer and led to the failure of the structure. Therefore, excellent Cu bonding quality is essential for the wafer stack to withstand these steps. Using the bonding conditions in this process, our bonded structure did not fail after the grind back and etch back. Furthermore, it is common knowledge that stress induced during TEM sample preparation may destroy a weakly bonded structure. However, our bonded structure was strong enough to withstand the severe TEM sample preparation steps.

12.3 Four-Layer-Stack Structure

12.3.1 TEM Observation

As mentioned in the fabrication flow, it is possible to repeat the steps 3 – 6 to stack

additional layers onto our original substrate. We repeated these steps and were able to stack four layers on the substrate, as shown in Figure 12-3. The TEM image in Figure 12-3 shows three Cu bonded layers in the structure while the fourth Cu layer is ready to be deposited on top of the structure. Because of the non-uniform thickness distribution across the large scale TEM sample, these three Cu bonded layers could not be focused simultaneously to show all clear images at the same time. Consequently, Figure 12-3 ahows a clear image of only the first (bottom) Cu bonded layer displaying a homogenous layer without the original bonding interface, similar to that shown in Fig. 12-2. Figures 12-4 (a) and (b) show magnified TEM images of the second and third (middle and upper in Fig. 12-3) Cu bonded layers, respectively. Both of these Cu bonded layers also show continuous and strong bonded layer, similar to the first bonded layer. The morphology observations of these Cu bonded layers suggests that this four-layer structure has a robust integrity.

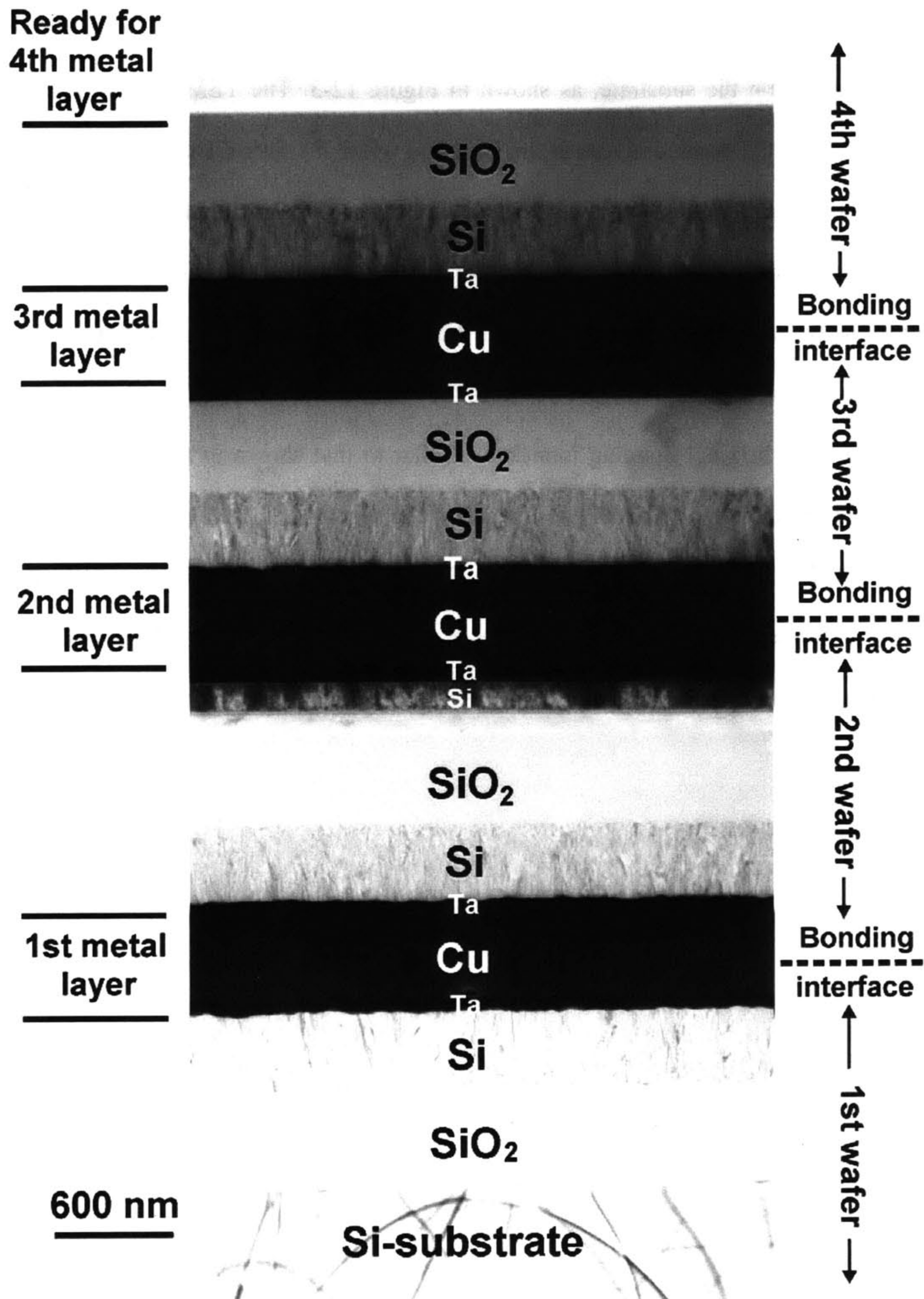
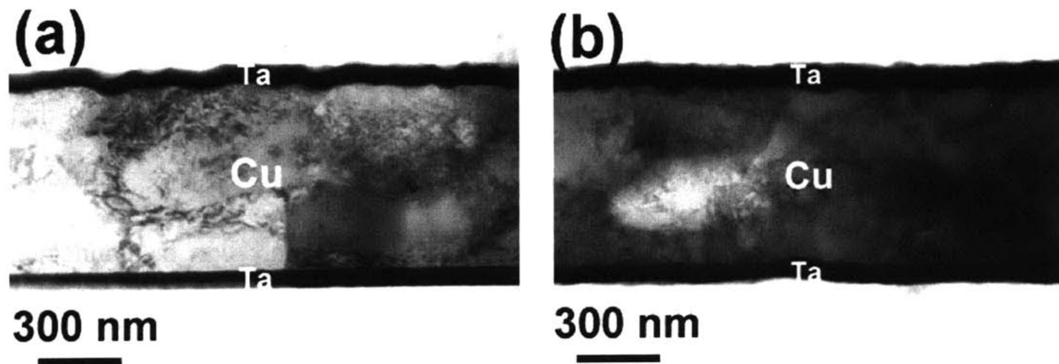


Figure 12-3 TEM image of a four-wafer-bonded structure after grind back, etch back and Cu/Ta deposition.



Figures 12-4 (a) and (b) Magnified TEM images of the (a) second and (b) third (middle and upper in Fig. 12-3) Cu bonded layers, respectively.

12.3.2 Discussion

Figure 12-3 shows the morphology of the bonded strucutre after three cycles of bonding, anneal, grind back and etch back processes. It is interesting to compare the Cu bonded layer in Fig. 12-2 to that of the first (bottom) Cu bonded layer in Fig. 12-3. The morphology of bonded layer in Fig. 12-2 suggests a strong bond even though it was subjected to stress from grind back and etch back. The first Cu bonded layer in Fig. 12-3 has undergone three cycles of bonding -> anneal -> grind back -> etch back, which means this bonded layer was under the mechanical stresses from grind back and etch back three times plus two additional thermal stresses from the heating and cooling during bonding and anneal processes. Thus, this bonded layer was subjected to a larger stress environment compared to that of the bonded layer in Fig. 12-2. However, from Fig. 12-3, the first Cu bonded layer shows a morphology similar to that in Fig. 12-2. This means that the bonded structure is strong enough to withstand additional grind back and etch back after the first cycle of layer stacking.

12.4 For Three-Dimensional Integration Applications

The successful development of multi silicon layer stacking suggests that three-dimensional integration applications using copper wafer bonding is feasible. When the devices are processed in individual silicon layers, these layers can be connected through copper interconnects. Copper interconnects belonging to different silicon layers can be bonded using the bonding parameters we developed. This is the concept behind the fabrication of three-dimensional integration using copper wafer bonding.

12.5 Possible Issues

Large wafer bows have been shown to decrease the bonding quality of two wafers, especially at low bonding temperature in Chapter 8. Since one silicon layer stacking requires one bonding process, when the bows of wafers are too large, it is difficult to achieve excellent bonding quality after repeated bonding steps. In this chapter, the wafer bow of two-layer-stacking structure shown in Fig. 12-2 increased from 2.6 μm to 16.7 μm, while the wafer bow of four-layer-stacking structure shown in Fig. 12-3 increased from 3.9 μm to 26.3 μm. In addition, until now, we have not successfully demonstrated a five-layer-stacking since films failed after fifth layer bonding and etch back. These facts indicate that wafer bow may be an important factor to decide the final number of layer stacking.

In addition, an accumulated stress from thin film stacking on the silicon substrate is expected. As the numbers of silicon layer increase, stress may play a role in the failure of the bonded structure. Finally, uniform bond quality across the wafer in each bonding

process directly determines the total bond strength of the structure. The contributions of these factors need to be investigated before the interconnected stacking of unlimited numbers of silicon layers becomes feasible.

12.4 Summary

In summary, we have developed a process for silicon layer stacking using copper wafer bonding, SOI grind back and etch back. This process can be used to fabricate a strong four-layer-stacking while each pair of bonded copper layers became a homogenous layer without the original bonding interface. With this process, it becomes possible to fabricate three-dimensional integrated circuits using copper wafer bonding.

Chapter 13

Application of Copper Wafer Bonding in Three-Dimensional Integration

Chapters 3 to 12 investigated copper wafer and interconnect bonding in different areas of properties and performances. Integration of these results for further three-dimensional application is important. For example, IC industries intend to use more and more polymer products because of the low dielectric constant requirement to reduce RC delay. It can be seen that in the future the temperature requirement for bonding will have to be decreased due to the low melting point of these polymers. The chapter summarizes the results of bonding quality, bonding parameters, and application suggestions. Based on the process requirements of different applications, people can choose suitable bonding conditions to achieve a reliable and robust bonding quality.

13.1 Summary of Bonding Parameters for Three-Dimensional Integration

There are many parameters related to the bonding quality, including the wafer preparations and bonding parameters. Some of them can be changed freely. However, some of them have limitations due to facility or design constraints. In order to achieve the best bonding results and further apply them in 3D integration applications, studies of relations between these parameters and bonding results have been carried out from Chapter 3 to Chapter 12. Based on the commercial bonder facility "Electronic Vision AB1-PV bonder" used in this research and the current semiconductor technologies, the following are the summary of bonding parameters and their effects on bonding quality:

1. Anneal: Further anneal after bonding has been considered as an important step to improve the bonding quality. Anneal temperature and bonding temperature are usually the same and the highest temperature can be used in the process. It has been shown that the original bonding interface can be removed through the nitrogen anneal. However, it should be noted that nitrogen anneal does not improve but might even destroy the bonding quality if the strength after bonding is not strong. In general, in the case of 30 min bonding, anneal is encouraged when the bonding temperature is above 300°C.
2. Temperature: Higher bonding temperature gives Cu atoms in two bonded layers more energy to diffuse, and more energy for grain growth. Therefore, high bonding temperature improves the bonding quality. However, in order not to destroy other materials in the device, the bonding temperature cannot be increased without limitation. In general, based on the bonding condition of 30 min bonding with an

optional 30 or 60 min nitrogen anneal, 300°C is necessary to achieve a reliable bonding quality, but with distinguishable bonding interface. 400°C or 350°C with a longer anneal duration is necessary to achieve a strong bonding quality without the original bonding interface.

3. Duration: Bonding duration is another key to the completeness of the bonding process. It is especially important when the bonding temperature is not high enough. Long duration of bonding offers enough time for Cu atoms and grains to complete the bonding even though their energies are low. In general, in the regime of this research, 30 min bonding is enough for bonding temperatures higher than 300°C.
4. Bonding Pressure: Sufficient bonding pressure can bring the two surfaces close enough to be bonded; letting the atoms from different layers interdiffuse in the initial stage of bonding process. Therefore, sufficient bonding pressure is a necessary parameter for the success of bonding. The highest pressure of the Electronic Vision AB1-PV bonder is 4000 mbar (4000N on 4" wafer) and offers enough contact for two wafers to initiate bonding.
5. Chamber Ambient: The chamber ambient should be kept in a vacuum environment as low pressure as possible. A vacuum can effectively preventing the particles in the atmosphere reacting with Cu atoms on the surface and hinder the bonding process. Electronic Vision AB1-PV bonder used in this research can reach 10^{-3} torr. In order to get the best quality of bonding, a nitrogen purge to remove the oxygen in the chamber prior to vacuum is suggested.
6. Surface Condition: Surface cleanness prior to bonding is crucial. Particles on the surface become barriers for two surfaces to contact and the Cu atoms to diffuse. The system (two layers) may need higher pressure and longer time to reach the starting

point of the bonding process. Therefore, under the same bonding condition, if the wafer surface is not clean, it is difficult to reach an excellent bonding quality. In this circumstance, a standard cleaning process is required prior to bonding.

7. Oxide removal: Oxides form on copper surfaces quickly in atmosphere after deposition. Thick oxides hinder the process of bonding and decrease bonding quality. HCl has been used to remove the oxides on the surface before bonding. Although oxides may still form between the HCl clean and the start of the bonding process, analysis showed that the small amount of oxides diffused across the bonded layer during bonding and did not affect the bonding strength. In fact, if the bonding process can be started right after the Cu deposition, HCl cleaning is not necessary at high temperature bonding.
8. Wafer Bow: A flat surface is important during bonding. It ensures all points of the two surfaces are on the same level and can contact each other. If the surface is not flat due to a large wafer bow, extra pressure, higher temperature, or longer bonding duration may be necessary to assist the bonding process. It should be noted that the wafer bow here is not the initial wafer bow of Si wafers but that with Cu films at the desired bonding temperature.
9. Interconnect Size: The bonding quality improves when the interconnect size increases. This factor becomes significant when the interconnect size is small. In addition, when the interconnect size is small, the corresponding bonding quality is sensitive to the wafer bow and surface condition as well.
10. Total Bonding Area: Increase of the total bonding area benefits the strength of the bonded wafer. To increase the total bonding area, increase of the number or size of interconnects, or adding dummy pads in the unused area, are useful options.

11. Use of dummy pads: Since the use of dummy pads increases the total bonding area, the bonding strength is enhanced. This design is especially helpful when the interconnect size is small and other process parameters are strictly confined.

In summary, a perfect Cu bonding for the whole wafer is the goal of 3D integration. Criteria for excellent Cu bonding can be categorized into the following three groups:

1. Blank Cu wafer bonding: Clean and flat wafers should be chosen for process. Cu oxide content on the surface should be kept as low as possible. High temperature, high pressure, and long duration are favorable to good bonding quality. Among these three parameters, adjusting two factors can compensate the third one. Nitrogen anneal should be applied if the bonding temperature is above 300°C. Excellent bonding without original interface can be obtained for wafers bonding at 400°C for 30 min followed by a 400°C 30 min nitrogen anneal, or at 350°C for 30 min followed by a 350°C 60 min nitrogen anneal.
2. Large Cu interconnect bonding: The bonding quality is not as good as blank Cu wafer bonding due to a smaller total bonding area. Increasing the total bonding area or adjusting the bonding parameters can balance this effect.
3. Small Cu interconnect bonding: The bonding quality is not as good as blank Cu wafer bonding due to a smaller total bonding area. Also, since the local bonding area is small as well, more efforts are needed to make a 100% bonding percentage possible. These efforts include increasing the total bonding area, adjusting the bonding parameters, or using the dummy Cu pads in the unused area.

The criteria for excellent bonding are based on the operation of the commercial bonder facility "Electronic Vision AB1-PV bonder" in this research. Several constraints of this facility can hinder the pursuit of room temperature bonding or very small

interconnects bonding. This will be discussed further in the next section. However, based on these results, the criteria can be applied in 3D integration applications.

13.2 An Alternative Bonding Approach and Its Bonding Facility Design

According to the results of this copper wafer bonding study, it has been found that once interconnect size becomes very small, or the required bonding temperature is low and close to room temperature, it is difficult to reach excellent bonding quality throughout the whole wafer. Both the surface oxide and the required energy for bonding are factors that hinder a perfect wafer bonding.

"Electronic Vision AB1-PV bonder" is the facility used in this research. Today it is also quite commonly used in both industry and universities, especially for the MEMS applications. This machine has good control of temperature and pressure during bonding, and its vacuum can reach 10^{-3} torr, which should be enough for Cu bonding. However, since Cu oxide easily forms on surfaces, it is reasonable to assume that the Cu surface has a thin layer of oxides shortly after unloading the wafer from the deposition chamber. This thin layer of oxides forms again after HCl cleaning and before loading the wafer into the bonding chamber. Although it has been shown that the oxides do not affect the bonding quality when the bonding temperature is high, they do at low bonding temperature.

In addition, at low temperature, the Cu atoms on the surface do not have enough energy and mobility for growth and interdifusion since the diffusivity of Cu atoms exponentially decay with the decrease of temperature. This lack is also harmful for the bonding quality when the bonding area is small.

A new idea using surface activated method was proposed recently for room temperature bonding [111]. This method can be applied on any species bonding. The idea is to set an Ar ion beam instrument in a bonding chamber coupling with a high vacuum system (at least 10^{-7} Torr). Without the pre-cleaning process, after loading the wafers and pumping the chamber to high vacuum, Ar ion beam is used to activate both Cu surfaces prior to bonding. Since the surface oxides can be removed and surfaces have been activated in a high vacuum environment after the ion beam activated process, the two activated surfaces can be bonded at room temperature. Because the mechanism of this approach is to bond activated atoms of two surfaces, once the surface is flat, the bonding process does not require the assistance of high bonding temperature and larger area.

Although the design of this bonder machine complicated and the machine is expensive and complicated, using the surface activate approach may effectively solve the limitations of Electronic Vision AB1-PV bonder in the future.

Chapter 14

Conclusion

14.1 Summary

In this thesis work, fundamental studies and bonding performances of copper wafer and interconnect bonding were investigated. The parameters of copper bonding were developed for applications in three-dimensional integration. For copper wafer bonding, the razor test was first applied to decide the initial bonding results. The interfacial morphology was observed by TEM and it was shown that original bonding interface can be removed by using the bonding parameters developed in this thesis. Different types of microstructures have been found in the bonded layer. Evolutions of microstructures, grain sizes, and grain orientations during the bonding were studied as well. The saturations of grain growth and (220) grain orientations mean a stable state of the bonded layer. The morphologies of bonded layer under different bonding conditions have been examined. Bonding strengths under different bonding conditions were analyzed by several methods as well. A map of bonding quality based on the morphologies and bond strengths was

established. Finally the effects of wafer bow on bonding quality were investigated.

Morphologies of copper bonded interconnect showed similar results in the blank copper films under the same bonding conditions. The size of successful copper bonded interconnects can be as small as 5 μm. A novel test structure to measure the contact resistance of copper bonded interconnect was designed. This test structure can effectively remove the effects of errors from misalignment during bonding. Specific contact resistances of bonded interconnects approximately 10^{-8} $\Omega\text{-cm}^2$ were measured. An abnormal contact resistance drop was observed in some bonded interconnects with pre-HCl cleaning when stressing current. A possible mechanism for this phenomenon was proposed. The bonding qualities of different interconnect sizes and densities were investigated. In addition to increasing the bonding temperature and duration, larger interconnect sizes, larger total bonding area, or the use of dummy pads for bonding in the unused area are options to improve the quality of bonded interconnects.

Process development for silicon layer stacking using copper wafer bonding, SOI grind back and etch back was studied. This process can fabricate a strong four-layer stacking while each copper bonded copper layer becomes a homogenous layer without the original bonding interface. With this process, it becomes possible to fabricate the real three-dimensional integrated circuits using copper wafer bonding.

14.2 Future Work

"Copper wafer bonding in three-dimensional integration" is a broad topic. In order to develop the best bonding conditions and quality for three-dimensional integration, there are so many parameters that one can easily feel directionless along the line of research. In

order to maximize the payoff from future research, research efforts have to be first focused on topics that are fundamental to development of copper wafer bonding.

On the fundamental study side, the method to establish the bonding quality map in Chapter 7 can be a reference in the future when the bonding condition is different. One may explore the necessary bonding and anneal duration for a reliable bonding if the desired operating temperature is low such as 100°C. This will be significant when the dielectric materials become polymer in the future. In addition, the relation of wafer location and bonding quality can be an interesting topic.

For practical application, it has been proved that using copper dummy pads can effectively improve the bonding quality. It will offer more practical information if one can use a real interconnect placement with an optional dummy pad design to investigate the bonding quality. Also, once copper interconnects and polymers are integrated in the integrated circuits in the future, it is important to understand if the polymer can survive at the bonding pressure and temperature.

As mentioned in Chapter 13, one can develop a bonding facility with a novel approach such as surface activated method to improve the bonding quality and decrease the bonding temperature. Efforts to decrease the high expense and simplify complicated design of the bonder machine will be necessary in the future before the room-temperature-bonding machine becomes commercial.

A strong four-layer-stack structure has been demonstrated in this thesis work. However, some factors will be significant before the realization of unlimited silicon layers of stacking. To decrease the effects of wafer bow on bonding quality for multi layer stacking is the first issue people can work on in the future. In addition, an accumulated stress from the thin film stacking cannot be neglected when the number of

stacking silicon layers keep increasing. How to keep the uniform bond quality across the wafer in each bonding process will be another topic. Afterwards, real three-dimensional integrated circuits using copper wafer bonding can be demonstrated in the future.

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