# Effects of Applied Loads, Effective Contact Area and Surface Roughness on the Dicing Yield of 3D Cu Bonded Interconnects

H.L. LEONG<sup>1, 2</sup>, C.L. GAN<sup>2</sup>, K.L. PEY<sup>2</sup>, C.V. THOMPSON<sup>3</sup>, Hongyu LI<sup>4</sup>

<sup>1</sup> Singapore-MIT Alliance (AMMNS)
<sup>2</sup> Nanyang Technological University
<sup>3</sup> Massachusetts Institute of Technology
<sup>4</sup> Institute of Microelectronics

### Abstract

Bonded copper interconnects were created using thermo-compression bonding and the dicing yield was used as an indication of the bond quality. SEM images indicated that the Cu was plastically deformed. Our experimental and modeling results indicate that the effective contact area is directly proportional to the applied load. Furthermore, for the first time, results have been obtained that indicate that the dicing yield is proportional to the effective contact area. It is also shown that films with rougher surfaces (and corresponding lower effective bonding areas) have lower dicing yields. A quantitative model for the relationship between measured surface roughness and the corresponding dicing yield has been developed. An appropriate surface-roughness data acquisition methodology has also been developed. The maximum possible applied load and the minimum possible surface roughness are required to obtain the maximum effective contact area, and hence to achieve optimum yields (both mechanically and electrically).

*Keywords* : Cu-Cu thermo-compression bonding, wafer-wafer bonding

## 1. Introduction

In recent years, there has been an increasing amount of interest in three-dimensional (3D) integration technology for integrated circuits and other semiconductor devices. Besides potentially able to dramatically reduce metal interconnect lengths, which reduces signal propagation delays and power consumption, it also allows different type of devices (III-V, SiGe, analog, digital, etc) to be stacked on top of one another to form a 3D system-on-chip (SoC), something which conventional 2D SoC might not be able to achieve.

3D integration can be achieved through either thermocompression chip-wafer or wafer-wafer bonding. While (commercially) there are some successes in chip-wafer and wafer-wafer bonding, literature on the physical aspects of bonding are few. Although there were some investigations into the effects of bonding temperature, metal stack thickness and pre-bond cleaning <sup>1,2</sup>, they are by no means exhaustive. Other factors that could affect either chip-wafer or waferwafer bonding include wafer topology, pattern density, applied piston load, wafer bow and surface roughness.

This report's primarily aim is to investigate the impact of pattern density, applied piston load and surface roughness on Copper (Cu) wafer-wafer bonding, though no doubt that some of the results would be applicable to chip-wafer bonding as well. Blanket and patterned Cu wafers were bonded at a temperature of 300°C and subsequently diced. The dicing yield was then taken as a measure of the bond quality.

### 2. Experiment and Fabrication of Test Structures

200 mm blanket and patterned Cu wafers were bonded in the experiments. The film stack consists of 2000 Å PECVD SiO<sub>2</sub>, a 250 Å-thick sputtered Ta barrier and a 1  $\mu$ m-thick Cu, deposited using the Electro-Copper-Plating (ECP) method. The wafers were subsequently annealed and the Cu film was chemical-mechanical polished until approximately 4000Å-thick of Cu remained. Bonding was performed on blanket-blanket, blanket-patterned and patterned-patterned Cu wafers, as shown in Figure 1.

For the patterned wafers, the Cu lines were made protruded by recessing (plasma etch) of the oxide. This is to ensure that the Cu lines would be able to make full contact with blanket/patterned wafer. However the oxide recess step increases the surface roughness of the Cu lines and this effect would be dealt with in the proposed model which predicts the contact area of various bonding configurations.

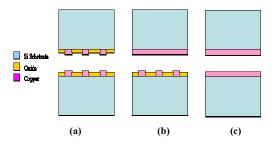


Figure 1: Schematic cross section of (a) line-line bonding, (b) line-blanket bonding and (c) blanket-blanket bonding.

For the patterned wafers, it consists of rectangular strips of Cu lines with a width of 50  $\mu$ m. The pattern density was varied by changing the spacing between the Cu lines. There are three different spacing of 50, 175 and 310  $\mu$ m. A pre-bond clean process using acetic acid (at 35 °C for 10 minutes) was used to remove the native oxide on the Cu surface and the samples were subsequently blown dry with N<sub>2</sub>. However, there was an interval of about four to five minutes between the pre-bond cleaning and loading of the wafers into the bonding chamber when the wafers were exposed to the cleanroom ambient. Hence some re-growth of Cu oxide was inevitable<sup>3</sup>.

For bonding of patterned-patterned wafers, they were aligned front-to-front using the Electronic Vision Aligner whereas for line-blanket and blanket-blanket bonding, the alignment was performed manually with respect to the notch. The wafers were subsequently clamped together in a bond chuck, but separated by three 30 µm-thick metal flaps. The aligned wafers were then transferred to the bond chamber. Prior to contacting the wafers, the chamber was subjected to three N<sub>2</sub> pump-purge cycles to reduce the ambient oxygen content. After the pump-purge cycles, the preprogrammed piston load was applied and the chamber was ramped up to the desired bonding temperature. The bonded wafers were subsequently held for 30 minutes under a vacuum condition of less than 0.5 mTorr.

The force per bonded area applied during the bonding process ranges from 0.145 MPa to 2.7 MPa, depending on the pattern density and piston load applied. The wafers were bonded at 300°C and subsequently annealed (piston load off) in vacuum condition for another 30 minutes. Lastly, dicing was performed on the bonded sample into strips of 5.85 x 30.4 mm<sup>2</sup> area.

# 3. Model

The Cu film surface roughness was measured using Atomic Force Microscopy (AFM). Digitized raw data from the AFM scans were being fed into a code (MATLAB) where the asperities' density (number per area) and radius of curvature were approximated. SEM images taken after a bonded sample was delaminated, as in Figure 2, suggested that when the Cu wafers come into contact, there were plastic deformations. Working on that basis, a quantitative model for the relationship between the contact area, taking into account of the surface roughness, and the corresponding dicing yield has been developed.

### 4. Results and Discussion

Using the model mentioned in the previous section, we obtained a quantitative estimate of the contact area, of bonded wafers with different nominal contact area, surface roughness. This model provides an estimate of the contact area when two wafers are brought into contact with each other, taking into account the applied

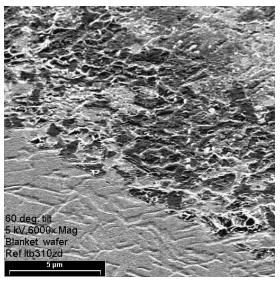


Figure 2: SEM images of a Cu blanket wafer. Bottom left is area which has not been in contact with the Cu line (from opposite wafer). Top right area has been in contact with the opposite Cu line. The morphology is dramatically different between these two regions, suggesting plastic deformations involved.

piston loads and surface roughness of each wafer. First, an increase or decrease in the applied load would bring about a corresponding increase or decrease in the estimated area by a similar factor. Secondly, for surface roughness, this paper adopts the simulation results of [6] that when the surface roughness parameter,  $\psi = (\sigma_R)^{\frac{1}{2}4,6}$  (where  $\sigma$  is the standard deviation of the asperity heights and *R* is the average radius of curvature of the asperities) increase or decreases by a certain factor, the contact area would approximately decrease or increase by the inverse of that factor.

Figure 3 shows the plot of different estimated contact area (different wafer bonding configurations) from the model and their corresponding dicing yield while Table 1 shows most of the results in a tabulated form. Although we are unable to verify the accuracy of this estimate compared to the actual contact area, our results obtained are largely in agreement with what is generally accepted that the contact area is proportional to the applied load, regardless whether the deformations are elastic<sup>4</sup> or plastic<sup>5,6</sup>.

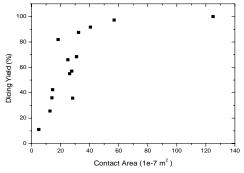


Figure 3: Dicing yield vs Contact area.

·	Load (N)	C. Area (1e-7 m2)	D. Yield (%)
Blanket-Blanket	400	5.01	11.1
	2000	25	66
	4550	56.9	97.2
	10000	125	100
Blanket-Blanket (Etched)	4550	18.32	81.9
	10000	40.56	91.7
Blanket-Patterned (50 µm)	4550	14.53	42.4
	10000	32.39	87.5
Blanket-Patterned (175 µm)	4550	14.04	36
	10000	30.98	68.4
Blanket-Patterned (310 µm)	4550	12.72	25.6
	10000	27.69	57

Table 1: Different types of bonding configurations: blanketblanket, blanket-blanket (etched), blanket-patterned of 50, 175 and 310  $\mu$ m spacing.

Results suggested that the dicing yield seems to be proportional to the contact area, until a 100% yield is reached. As we have mentioned earlier that the contact area is proportional to the applied load, we can then infer that the dicing yield could be proportional to the applied load as well.

Figure 4a and 4b shows the variation of  $\sigma$  and *R* for different types of wafers. Regardless of nominal contact area, samples which have been etched displayed little difference in *R*. However the nominal contact area does have an impact on  $\sigma$ : the smaller the nominal area, the larger is the standard deviation. This could be due to a smaller nominal area would result in a larger concentration of the ions bombardment during the etching process.

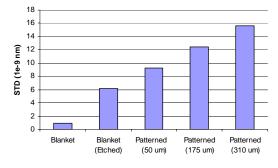


Figure 4a: Variations of standard deviation,  $\sigma$ , for different types of wafers

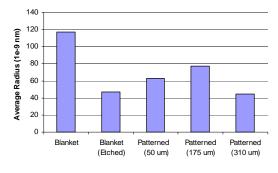


Figure 4b: Variations of average asperities radius, *R*, for different types of wafers

## 5. Conclusion

We have developed both a surface-roughness data acquisition methodology as well as a quantitative model for the relationship between the measured surface roughness, applied bonding load and the corresponding dicing yield of bonded Cu wafers. Results indicate that the dicing yield could be proportional to the contact area, which in turn is dependent on the applied load and surface roughness of the wafers. It is then not difficult to foresee that for optimal yields (both mechanically and electrically), we need to obtain the maximum contact area by applying the maximum applied load with minimum wafer surface roughness.

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