Commercial Applications of Nanostructures Created with Ordered Porous Alumina

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Abstract

In the drive from microfabrication to nanofabrication, porous alumina templates may play a key role in technological evolution. Under the right processing conditions, ordered pores can grow in anodic aluminum oxide, which is a high strength, thermally and electrically insulating material. There are many potential applications for porous alumina templates, ranging from the simple fabrication of nanostructure arrays to the more complex processing of components for end-user products such as nano-integrated circuits and gas sensors.

Porous alumina templates can also be processed to have long-range pore ordering on an entire twelve-inch silicon wafer, which may be of unique benefit to processes requiring such pore precision, such as parallel electron beam lithography. The high aspect ratios which can be attained through porous alumina template technology may also offer unique advantages in applications such as field-emission-based devices. As a durable high strength material, porous alumina templates are not limited by extreme process conditions, further extending the reach of their application.

The vast array of applications allows the technology to be financially attractive inside business models ranging from sustaining to disruptive innovation. Porous alumina template technology has the necessary multitude and diversity of attributes to play a crucial role in the future of nanotechnology.

Thesis Advisor: Carl V. Thompson II
Title: Stavros Salapatas Professor of Materials Science and Engineering

Acknowledgments

I've studied electronic materials for the better part of my collegiate career and have only studied nanotechnology on one other occasion outside of my M. Eng. Project: a case study in a senior level materials engineering class back at Virginia Tech. That was my first exposure to nanotechnology, but it was by no means an all-encompassing course. There was much about the nano-world that I had not been introduced to until I started working on my M. Eng. project these past two semesters at MIT. I actually feel quite fortunate to be working with graduate students who have dedicated the last 4 years of their lives working on nanotechnology. I have learned so much just talking to them and listening to their presentations at meetings that even if I did not have to do an M. Eng. project myself, I still would have considered my time with them to be both educational and invaluable.

I paint this background because the work which I am about to present is in no way all from my own head. Those I have worked with have taught me everything I have learned and have provided me the basis from which the following document grew. I am specifically thankful to Professor Carl V. Thompson for his advising as well as his hospitality which was apparent from the beginning of the project. He graciously took me under his wing and I felt from the start as a part of his group. I couldn't imagine working with a better professor. Ramkumar Krishnan has been the vehicle by which I have learned all I've had to learn in order for this project to be a success. His constant commitment to me and this project has helped me get as far as I have. I've relied on both of these men as I pushed towards the final thesis, and they have been an immense help.

Additional support has come from the following people: Mom, Dad, Kevin, John, Andrew - I love you all; Sean, John, Adam - Apt. 245 forever; Katie - So this is what Boston is like; and finally, my alma mater - Virginia Polytechnic Institute & State University where my fascination for materials science first began.

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1.0 Introduction

Nanotechnology is perhaps the buzzword of all buzzwords. There is something intrinsically interesting about the study of phenomena at a scale so small that lengths, diameters, and circumferences can be measured in terms of a relatively small number of atoms. Not only does this *science of small* make for interesting research, but it may hold many of the world's future technologies as well.

Because many see nanotechnology as the future course of technology, there is an overabundance of research in nearly all conceivable nanoscience areas - from drug delivery to magnetic storage media to nanoelectrical mechanical systems. At the heart of these various nanotechnologies are nanostructures which serve as the building blocks of these applications. As the integral and fundamental part of nanosystems, nanostructures must be developed with the same quality, reliability, and efficiency that current microstructures and microdevices are produced.

There has been and continues to be a driving force in scientific research to "grow" nanowires, nanodots, nanotubes, and other nanostructures conveniently with controlled spacing, diameter, and location. This document serves as an evaluation of one specific way in which nanostructures are grown, through the use of ordered porous alumina templates. Of fundamental concern here is an understanding of their production, application, and benefit over current and future competing technologies.

Whereas microelectronic devices and other structures of "micro" scale have been categorically understood for well over fifty years, the field of nanotechnology and nanoscience is young. Therefore, any study into specific nano-endeavors must be prefaced with an understanding that the nanotechnology market has not been fully predicted nor can it be until a plethora of nanotechnologies make it to market. This will take time, and we are currently only at the beginning of a long journey that will take us to the realm of the miniscule, or better yet nanoscule.

2.0 Porous Alumina Template Technology

Many advances in porous alumina template technology (PATT) have occurred over the last ten years, beginning with the work of Masuda et. al.[15], of Nippon Telephone and Telegraph in Japan, on double anodization in the mid 1990's. His group noted porous alumina's affinity to grow pores under certain process conditions, and upon further study, they developed a double anodization process that produced pores with short range ordering. Another of the group's major contribution to PATT was their development and patenting of a stamping technique to allow for long range pore ordering.[8] This work was followed by other groups who noted the interesting aspects and potential applications of porous alumina. Aiba et al., of Canon Corporation in Japan, studied alternative methods to fabricate a long range ordered porous template. Specifically, they developed and patented the use of charged particle beams on aluminum surface for this purpose.[5]

Nielsch et al., at the Max Planck Institute (MPI) in Germany, repeated Masuda et al.'s work by demonstrating ordered porous alumina templates processed through a stamping technique.[58] He also successfully worked on ordered magnetic nanowire growth using porous alumina templates.[59] Nielsch teamed up with Krishnan, Ross, and Thompson at the Massachusetts Institute of Technology (MIT) to develop a technique to produce long range ordered porous alumina through the use of a pre-patterned silicon substrate.[60] The group noted their success in incorporating inverted pyramids and interference lithography to produce ordered templates. Ohkura et al. independently studied an identical technique at Canon, and patented the approach.[57]

When Krishnan began concentrating more heavily on porous alumina templates, he again collaborated with Nielsch, Ross, and Thompson in developing pore doubling, a technique to reach beyond lithographic limits for pore spacing. Further work done by the group included the successful fabrication of ordered copper and gold nanowire growth in long-range ordered porous alumina templates processed by the silicon pre-patterning technique.[61]

In recent years, Krishnan and Thompson have focused on other template fabrication techniques allowing high aspect ratio pore growth on 30 nm diameter pores.

They have also successfully fabricated ordered arrays of carbon nanotubes using porous alumina templates[62], as well as worked on various applications, including parallel electron beam lithography. A collaboration of Thompson, Ross, and Stellacci at MIT has also resulted in new-found proprietary applications which take advantage of the unique features of porous alumina templates.

It is from these and other past developments which have allowed PATT to be where it is today, a continually thriving research topic and an interesting and marketable idea. What follows is a full description of the most pertinent processing developments and scientific modeling that details the unique benefits of PATT.

2.1 Anodization Process

The method of fabricating porous alumina templates is accomplished through the anodization of an aluminum layer. The purpose of the anodization process is two-fold: to convert the aluminum layer into the much more versatile material alumina; and to grow ordered nanopores in the alumina for use as templates for nanomaterial growth and other applications. Metals form an oxide layer in air, and aluminum, Al, forms alumina, Al_2O_3. This layer is typically only a few nanometers thick and is nonporous. For industrial applications, often a thicker layer of alumina is desired because of the welcome materials properties of alumina which are not present in aluminum, most notably corrosion resistance. The oxide that forms on aluminum does not flake off, but instead is held strongly in place on the aluminum. One key aspect to alumina is its growth from aluminum under certain processing conditions results in an inherent porosity. This feature is at the heart of porous alumina template technology.

When aluminum is immersed and electrically connected in an electrolytic cell in the presence of an electrolyte, two forms of anodic alumina can form. If the electrolyte has a pH > 5.0, a nonporous barrier alumina forms. However, in the presence of an acid with much lower pH, porous alumina can form with pore diameters less than 100 nm and lengths on the order of microns. Pore diameter is a function of the electrolytic cell voltage, the acid used and its pH. Typically one of three acids is used in aluminum

anodization: phosphoric, oxalic, and sulfuric, with relative diameters, D, given below in increasing size (all other variable unchanged).

$$D_{phosphoric} > D_{oxalic} > D_{sulfuric}$$

A layer of barrier alumina constantly separates the aluminum from the electrolyte, and serves as the area of interest for the chemistry of pore growth reactions. Specifically, at the bottom of the pores, where the pore maintains a significant curvature, the barrier alumina plays the central role in pore development and growth throughout the anodization process. Figure 2.1 shows the anodization process in detail[2].

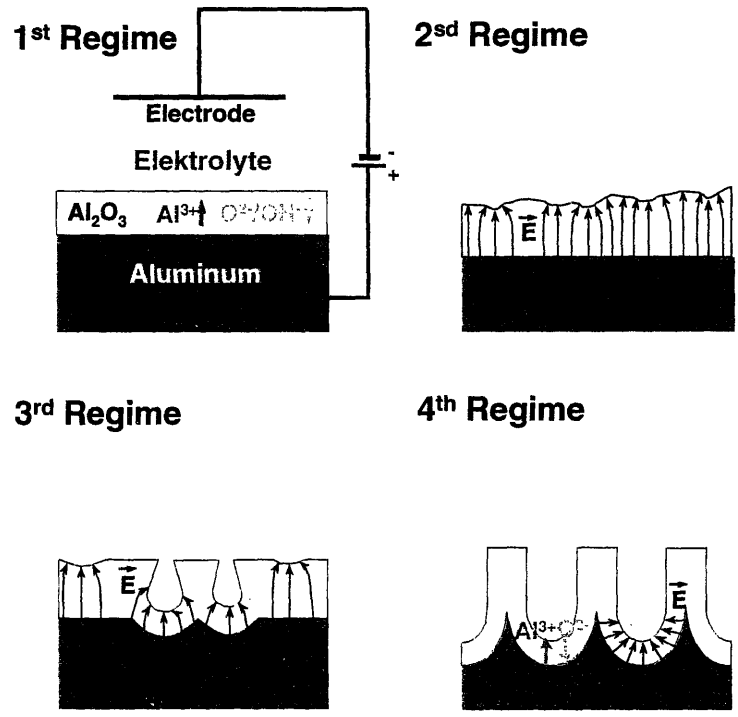


Figure 2.1: Pictorial description of aluminum anodization and nanopore nucleation.[2]

The aluminum film is cleaned and electropolished prior to anodization to reduce surface roughness, which would otherwise affect pore formation and ordering processes. The polished surface is immediately covered by a native nonporous oxide in air. Because this oxide is of higher atomic volume than aluminum, very small stress cracks appear on the surface where the native oxide forms. While the exact pore growth mechanism is debated by scientists, many believe that imperfections or cracks present on the surface of the native oxide, which create areas of higher electric field beneath them, are the initial causes of pore nucleation. This can be seen in the 2nd regime of Figure 2.1. The higher electric field at the bottom of the pore/crack causes a faster dissolution of oxide into the electrolytic solution than at other surface points, resulting in pore generation and preferential growth, as shown in the 3rd regime. The oxide dissolution rate is controlled by the electric field at the base of the pores, where the curvature is highest (4th regime), and the rate of aluminum conversion to alumina is controlled by the average electric field across the barrier oxide/aluminum metal interface.

There are, thus, two chemical processes occurring simultaneously. Aluminum loses electrons, becomes an ion and converts into alumina at the barrier region (1st regime) or else continues through the barrier region into solution. Secondly, alumina, which had gained the lost Al^{3+} ions from aluminum is dissolving into solution. Whether the aluminum ions which reach the solution are delivered directly by the dissolution of alumina or instead by diffusion from the aluminum through the alumina, or both, the net effect is conversion of aluminum to alumina, and dissolution of alumina concurrently. The dissolution of alumina happens much faster at surface areas that have higher electric fields; i.e. where there is higher curvature, and therefore higher electric flux density. Oxide ions from the electrolyte in solution provide oxygen in the alumina formation. The voltage applied over the electrolytic cell drives Al^{3+} and O^{2-} ions in opposite directions, allowing aluminum to alumina conversion, and barrier alumina dissolution. Pore diameters are kept constant by two limiting phenomena. If pore curvature decreases (creating a larger pore diameter), the flux density at the base of the pores is decreased, and the rate of alumina dissolution slows and the pores would partially fill. If, on the other hand, pore curvature increases (creating a smaller pore diameter), the flux density would increase, hastening alumina dissolution and pore growth.[55]

After one anodization process, an array of twisted unordered pores exists at the top of the alumina region, while at the bottom (i.e. the alumina/aluminum interface), the pores are ordered, as shown in Figure 2.2.

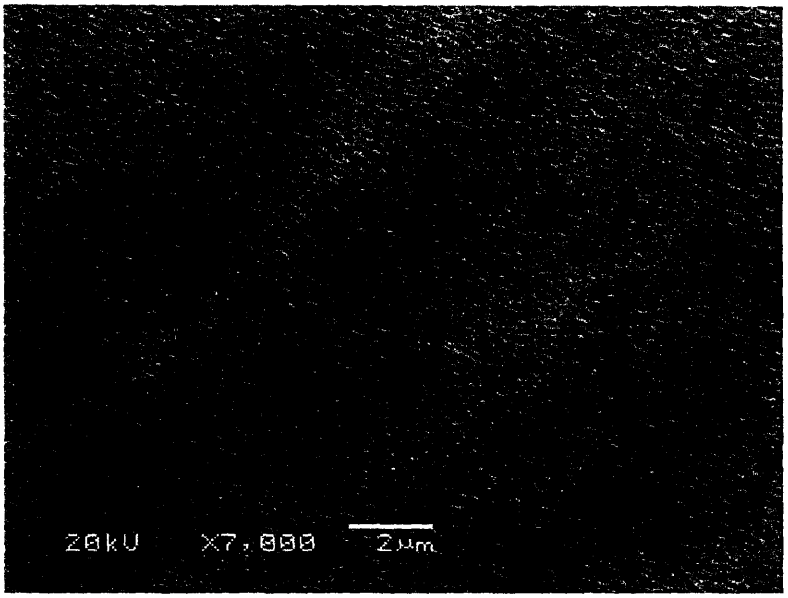


Figure 2.2: SEM image of alumina surface after single anodization.[2]

In order to generate ordered porous alumina, one must control the topography of the aluminum metal prior to anodization. As described above, it is at areas of higher curvature that the barrier alumina (formed natively) dissolves most rapidly, leading to pore growth. While pores are not ordered on the surface of the once-anodized alumina region, they do order at the base of the pores. The 4th regime of Figure 2.1 shows that the aluminum underneath the barrier alumina layer maintains the topography given to it by the base of the porous alumina. One way to control the aluminum topography, introduced by Masuda et al. in the mid 1990s, is by stripping the alumina off of a sample after anodizing one time. That is, by anodizing a sample of aluminum through a given thickness of material, and then stripping off the top layer of porous alumina which was created, one is left with an aluminum layer with an ordered topography. After an alumina strip, the aluminum sample will again grow a native oxide in air, covering the new

topography. A second anodization reconstitutes the chemical reactions described above, but now the pores are ordered at the top of the alumina surface, and proceed to grow as described above. Thus, through double anodization, one can grow locally ordered arrays of porous alumina.

Figure 2.3-4 shows the result of a double anodization.

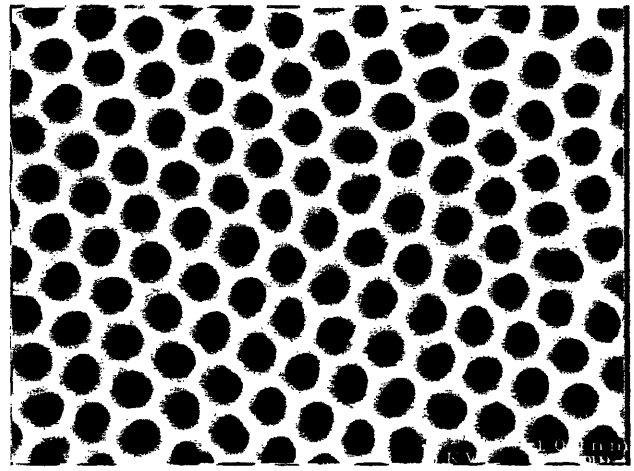


Figure 2.3: Locally ordered pore structure in double anodized alumina.[2]

Note that at the base of the pores in Figure 2.4, the aluminum/alumina is curved. One could conceivably remove the alumina and anodize yet again, maintaining the same ordered array that is transferred from the base of the original alumina pores

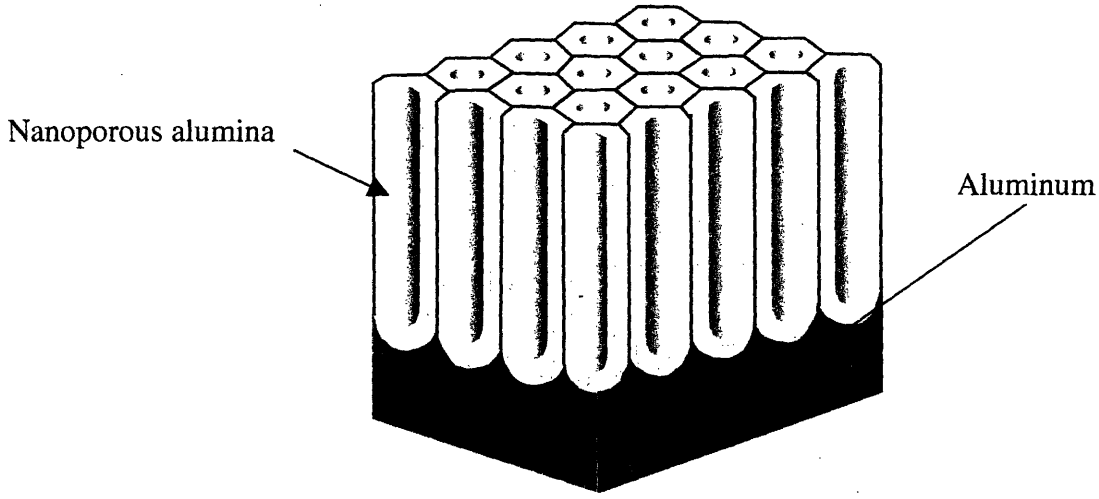


Figure 2.4: Pore structure in alumina on virgin aluminum.[2]

The first anodization process and subsequent alumina strip define a locally ordered topography with hexagonal geometry which, upon a second anodization, results in a locally ordered porous alumina template with the same geometry. While local hexagonal ordering is evident in bulk aluminum anodization, long range ordering is not present, as shown in Figure 2.2.

Porous alumina template fabrication is not the only application of aluminum anodization processing. Alumina has long been understood to contain porosity when grown under the right conditions. Because alumina does not flake off, as do other metal oxides such as iron oxide, it has corrosion protection characteristics that are attractive to a host of industries. Therefore aluminum anodization was developed to grow thicker films for protecting aluminum components in various products. In these instances, process conditions prevent porous alumina from growing (which would be susceptible to corrosion). Instead, solely the barrier oxide is grown. Other metals whose oxide is protective, but are often too thin when grown naturally include titanium, tantalum, and niobium.

In some applications, porous alumina films are specifically sought. Porosity allows alumina to be dyed relatively easily, lending to applications in the art world as well as the cosmetics industry. Anomatic is one company whose sole production capability is the anodization and finishing of aluminum packages for a variety of

products, from lip gloss to flashlights. Figure 2.5 shows a processed example of the latter.

Figure 2.5: Anodized flashlight cases created by Anomatic.[49]

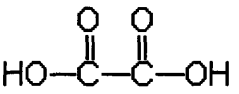
The flashlights' brightness and color are controlled during the anodization processing of the package material.

2.2 Process Chemistry

The nanopore shape and size can be constrained by process chemistry and electrochemical potential. The following section describes how these two elements affect pore growth.

Though the process design itself involves several clever ideas in the fabrication of porous alumina, there have been few attempts at studying the underlying relationships between applied voltage, acid molarity, and the quality of pores produced. Up to this point, the research literature only reports on the results obtained using specific setups. There have been a few empirical relationships that have been reported, but for the most part the focus has been on perfecting the anodization process by a "guess and test" scheme. Of the many variables in the anodization process, there are two aspects that have been analyzed: control of the chemistry and control of the voltage.

First, the chemistry involved is an oxidation reaction whereby the aluminum will readily form an ion by losing three electrons from its 2p orbital so that it can ionically bond with oxygen. The oxygen exists as an ion because it is in solution as an acid. Assuming oxalic acid, $C_2H_2O_4$, is the chosen electrolyte in the anodization reaction, then there are two hydroxide ions, OH-, per molecule, as shown in Figure 2.6.



OXALIC ACID

Figure 2.6: Atomic description of oxalic acid.[3]

The hydroxide ions float around in the acid under no other constraints. However, when they are subjected to a voltage, they will be drawn to the positive terminal, at which sits the aluminum, and will therefore bond to the aluminum to form alumina. Alumina forms from 3 hydroxide ions, leaving 3 hydrogen ions to return to the solution and float towards the negative terminal. As the aluminum is attacked by the electrolyte, aluminum converts to its own ion Al^{3+}. At first Al^{3+} is attracted to the negative terminal, but upon combination with incoming O^{2-} ions, becomes alumina. The oxidation reaction proceeds as follows:

$$2Al^{3+} + 3O^{2-} \rightarrow Al_2O_3 \qquad \text{(Eq. 2.1)}$$

The overall reaction is as follows:

$$8/3Al + 2C_2H_2O_4 \rightarrow 4/3Al_2O_3 + 2C_2O_2^{-2} + 4H^+ \qquad \text{(Eq. 2.2)}$$

For safety and practical purposes, oxalic acid is typically used at 0.3 molar solution. The electrolyte concentration has a direct impact on the potential at the electrode/electrolyte interface, according to the Nernst Equation:

$$E = E^0 - (RT/zF) * \ln([\text{Reduction}]/[\text{Oxidation}]) \qquad \text{(Eq. 2.3)}$$

Where E = actual potential of the electrode, E^0 = standard potential of electrode couple, R = gas constant, T = absolute temperature, F = Faraday's constant, z = number of moles of electrons exchanged in reaction, and [Reduction] & [Oxidation] represent the activities (or concentrations for aqueous solutions) of all species on the reduction & oxidation side of the reaction equation, respectively. Therefore, changing the concentration of the electrolyte does have an effect on the actual potential at each electrode, which by extension affects the potential applied across the cell (potential across cell = difference in potentials at each electrode).[16]

The second important variable in this process is the applied voltage. There have only been empirical equations drawn from research in this area. "Anodization at low potentials (30-60 V) in 0.3 M oxalic acid at 20 C leads to pore distances of 50-150 nm. Potentials of 100-195 V can be applied using 10wt% phosphoric acid as electrolyte at 3 C and lead to interpore distances of 300-420 nm."[4] Natural ordering is observed at cell potentials of 25, 40, and 195 V in sulfuric, oxalic, and phosphoric acid solutions, respectively.

Other relationships relating pore spacing to voltage exist as well. A classically held empirical relationship between interpore distances and applied voltage is noted in Equation 2.4,

$$2R=10+2V_a \qquad \text{(Eq. 2.4)}$$

where 2R equals the pore spacing in nanometers and V_a is the applied voltage. Experimental results show that pore diameters scale at about 30% of the pore spacing.

The final product of the anodization process is a block of alumina with pore spacings on the order of 100 nm and pore diameters on the order of 4 -100 nanometers. There are, however, several other important features in the anodization process which control these pore dimensions.

2.3 Controlling Pore Uniformity

The crucial criterion for creating a uniform template requires that the pores be equispaced, contain vertical sidewalls, and have nearly equal diameters. Typically, locally ordered pore growth, such as that described above and by other competing technologies discussed in Chapter 4, result in pore domains. Pores are perfectly ordered in a hexagonal geometry inside these domains (which look like grains), but along domain boundaries, there are regions of non-uniformity, where two pores may be nearly touching, or else have completely combined. Figure 2.7 shows this pictorially.

Pore domain boundaries

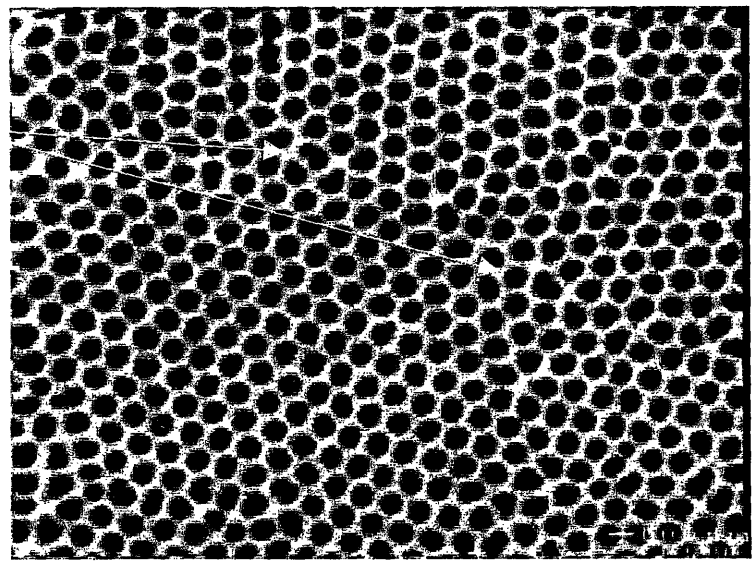


Figure 2.7: Ordered pores separated into domains as a result of double anodization.[55]

While pore uniformity is attempted for most porous alumina template technologies, many applications simply require short range order. Accomplishing long range ordering, on the other hand, requires alternate processes to double anodization. Chapter 4 details several competing technologies which attempt short and long range ordering. Many of these ideas are theoretically possible for pore ordering across a rather sizable area, but are technically unfeasible or simply impractical. Attaining ordered pores and pore spacing across an entire twelve-inch wafer, for example, has many benefits and some unique applications, however it requires variations on the processing steps used by double anodization. There are two predominant methods employed by the MIT group to attain long range order: substrate pre-patterning; and a heretofore undisclosed procedure resulting in high aspect ratio porous alumina production.

The first method involves a silicon substrate, or other preparation layer, and was independently innovated by Nielsch et. al of MIT and Ohkura et al. of Canon Corporation, the latter of whom owns a patent on the process[57]. Though the anodization process requires only aluminum, a silicon substrate allows added versatility and a unique pore structure control mechanism. The substrate layer is patterned using interference lithography and wet etched so that an array of inverted pyramid-shaped structures cover the surface of the silicon. Figure 2.8 shows a scanning electron micrograph of the patterned silicon topography.

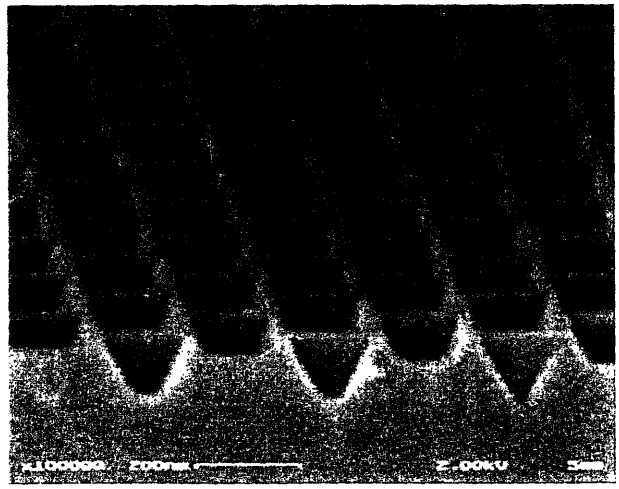


Figure 2.8: Inverted pyramid structures etched into a silicon substrate.[2]

Aluminum is then deposited over the silicon substrate, and conformally coats the Si surface, as shown in Figure 2.9.

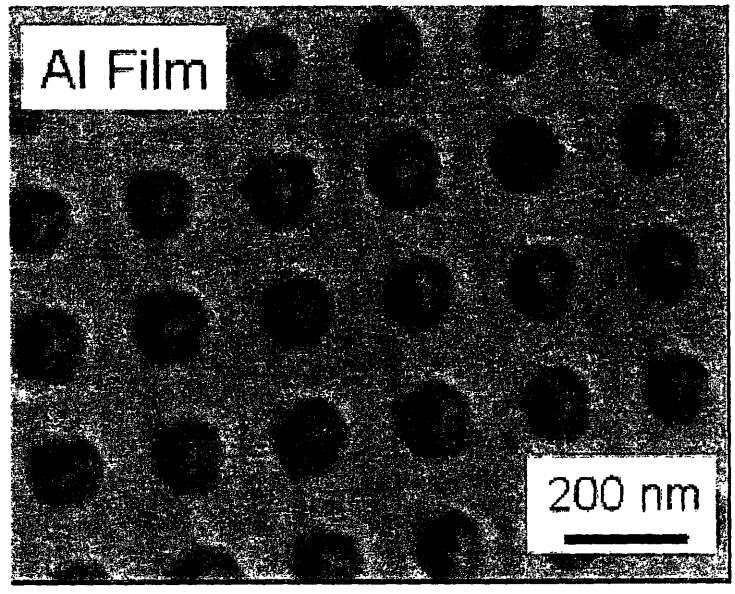


Figure 2.9: Al film conformally deposited on pre-patterned silicon.[2]

A topography is created on the top of the aluminum which identically matches the pre-patterned silicon substrate. A very small native aluminum oxide then forms immediately in air over the deposited aluminum, and the anodization process continues as described previously. In this technique, however, because an ordered topography has already been established, there is no need for a second anodization. The first anodization causes pore growth at points of high curvature in the alumina barrier layer (which has been transferred through the virgin aluminum, from the pre-patterned silicon substrate). Figure 2.10 shows a cross-sectional view of anodized alumina on a pre-patterned silicon substrate.

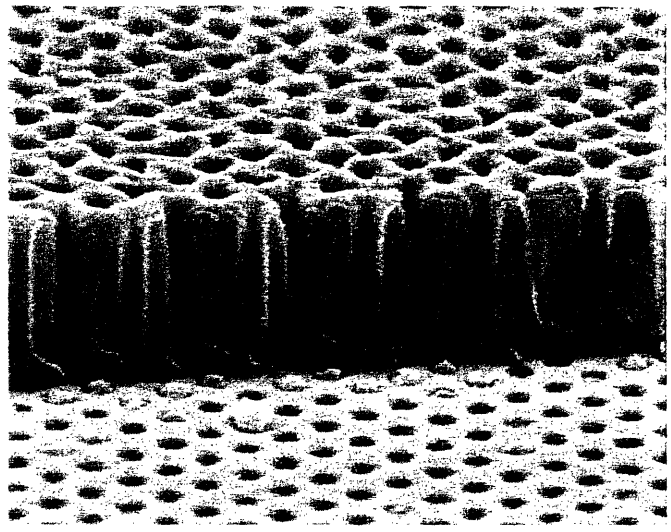


Figure 2.10: Cross-sectional view of ordered porous alumina on pre-patterned Si.[2]

Figure 2.11 shows a top-down view of an anodized template first deposited on a hexagonally arranged Si topography.

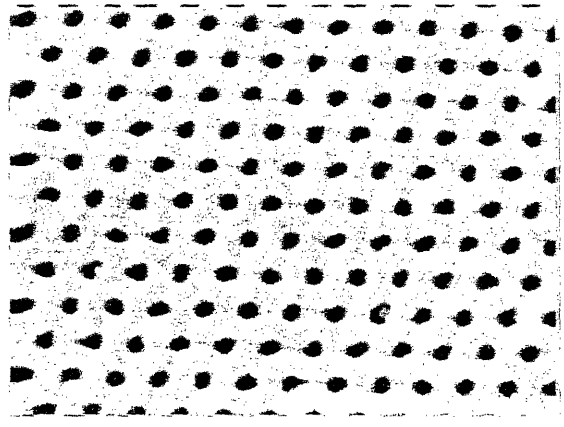


Figure 2.11: Hexagonally ordered array of porous alumina grown on topographic Si.[2]

Figure 2.12 shows a cross sectional cartoon of the result of anodization on pre-patterned silicon.

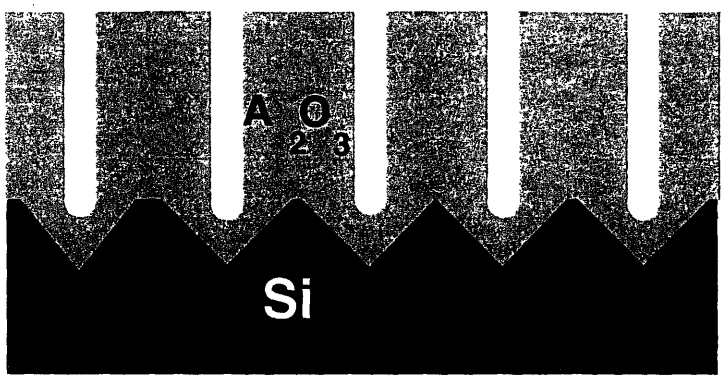


Figure 2.12: Alumina nanopores grown on a patterned silicon substrate.[2]

The physical limit of the pores' length is the thickness up to which a silicon pattern can be transferred to the aluminum film. At a critical thickness, on the order of 1 micron, the pattern is no longer distinguishable from surface roughness. This limit still allows for very good aspect ratio structures to be created using PATT.

One other advantage of this technique is that it allows periodic and identical pore structures to be developed over large areas. Pores are not separated into domains, as in the case of double anodization. Instead, depressions in the aluminum are equispaced due to the silicon's pre-patterning. It has been demonstrated by Heilmann et al., whose results are shown in Figure 2.13, that interference lithography can be used to successfully pattern equispaced features across an entire wafer.[56] Therefore, pre-patterning a silicon wafer, followed by aluminum deposition and anodization could produce an entire wafer of ordered pores.

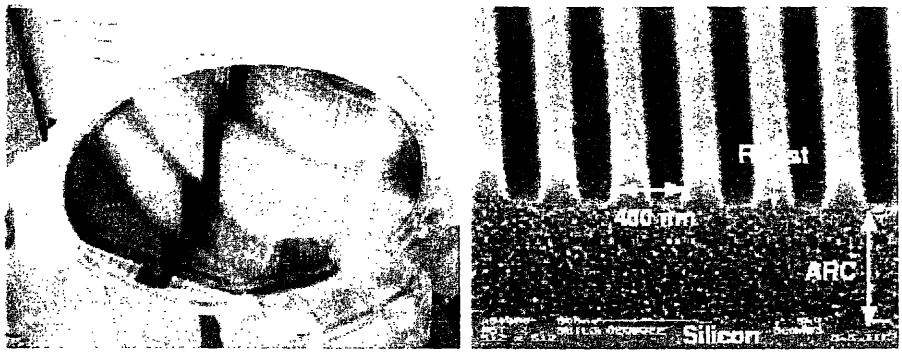


Figure 2.13: 300 mm wafer, uniformly patterned by interference lithography.[55]

Filling an entire wafer with ordered pores requires careful selection of pore location geometries. Using the topography-transfer technique described above, the geometry of pore growth at the surface of the aluminum layer is controlled by the topography of the silicon substrate. Square, rectangular, triangular, or hexagonal geometries guarantee that an entire surface will be uniformly covered by equispaced nanopores. One advantage of this approach in porous alumina fabrication is that the geometry can be controlled. In double anodization of bulk alumina, only the most stable hexagonal arrays will grow. However, square and other geometry arrays can be grown stably on patterned substrates up to specific alumina thicknesses. Most research has concentrated on hexagonal arrays of nanopores because the majority of studies on the subject are geared towards short-range ordering. A square array of aluminum, deposited on pre-patterned silicon prior to anodization, is shown in Figure 2.9. A hexagonal array of ordered pores is shown in Figure 2.11.

Another unique advantage of pre-patterning Si to grow ordered arrays of pores in alumina is that the pore size and spacing can be independently controlled. Whereas Eq. 2.4 and other empirical evidence describe the relationship between applied cell voltage and subsequent pore features and spacings, pre-patterning results in the forced growth of pores at specific locations due to a patterned topography. Figures 2.14-15 show the relative ease of pore diameter control using the pre-patterning technique.

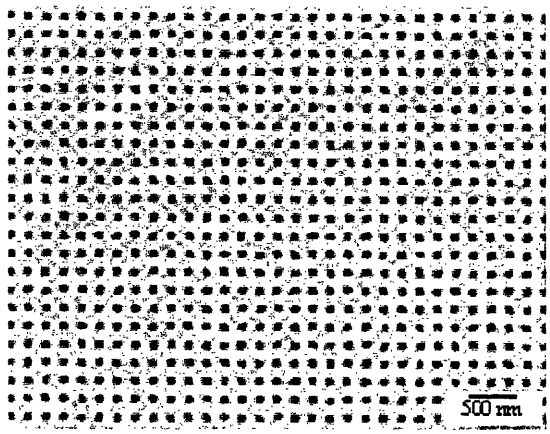


Figure 2.14: Square array of 80 nm dia. pores, processed in phosphoric acid at 86 V.[2]

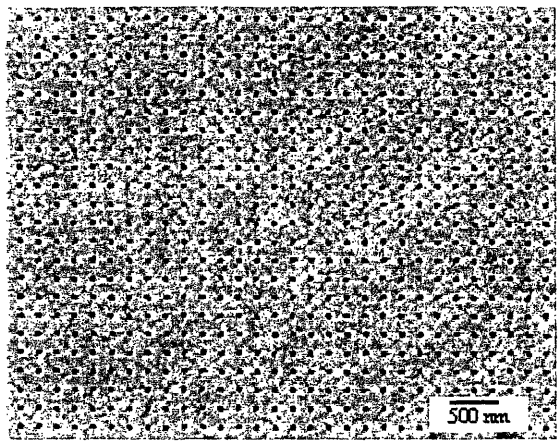


Figure 2.15: Square array of 30 nm diameter pores, processed in oxalic acid at 89 V.[2]

Not only does the silicon substrate allow control over the placement of pores in the alumina, but it also allows the template to be integrated into current silicon technologies in the microelectronics industry. Because silicon is so widespread and is the most common link between devices and components, growing templates on silicon allows for this added benefit.

The second, and perhaps most promising, technique researched by the MIT group follows some of the same principles and techniques as described above, but allows for both very high aspect ratio structures and long range pore ordering. Patents are currently pending.

2.4 Reaching Beyond Lithographic Limits

The more pores that fit on a surface, the more useful the template becomes. Approaching and surpassing lithographic limits using porous alumina may be possible by way of a technique called pore doubling. Occurring at processing conditions which include lower electrolytic cell voltages than that given by empirical relationships, such as Eq. 2.4, pore doubling reduces the distance between pores by growing a second array of pores offset from a first array. Thus far, however, there have been no successful attempts at creating uniform pores using this technique. The added pores are smaller and

deformed. More development is required before this technique can be implemented commercially. Figure 2.16 shows results of the technique.

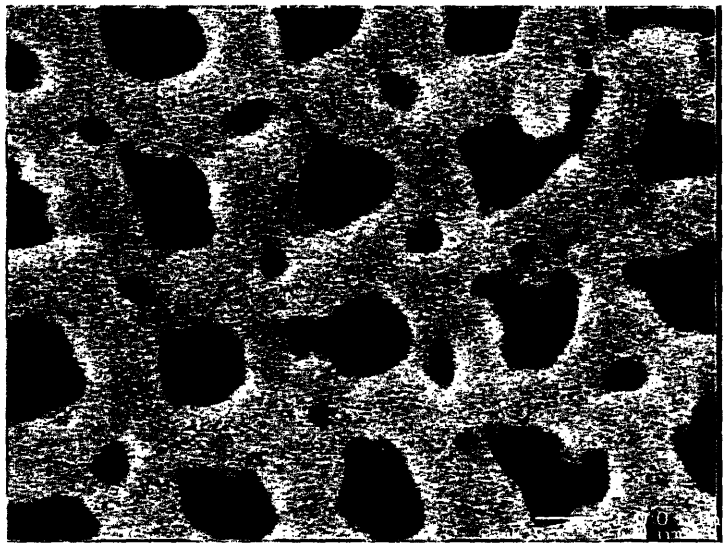


Figure 2.16: Effect of pore doubling.[2]

2.5 Nanostructure Fabrication

Fabrication of the porous alumina template constitutes the primary and most unique step in this process of fabricating nanodevices, however there is much more flexibility in the second process: fabricating nanostructures in the template. At this point, there are several fabrication options, including nanodots[6], nanorods, nanowires, and nanotubes. It has been shown[2] thus far that each of these structures can be fabricated successfully, and in a relatively straightforward manner. In fact, upon the first successful fabrication of a porous alumina template with long-range order, the MIT group's first attempt at depositing nanostructures was successful as well. Because the template serves as a mold for nanostructure growth, simply depositing (generally done by electrodeposition) the desired metal (nickel, copper, etc) will yield a metal nanostructure. In the case of nanotube and semiconductor wire growth, catalyst-assisted vapor phase

deposition is the process of choice. Figure 2.17 shows an array of locally-ordered porous alumina after copper electrodeposition.

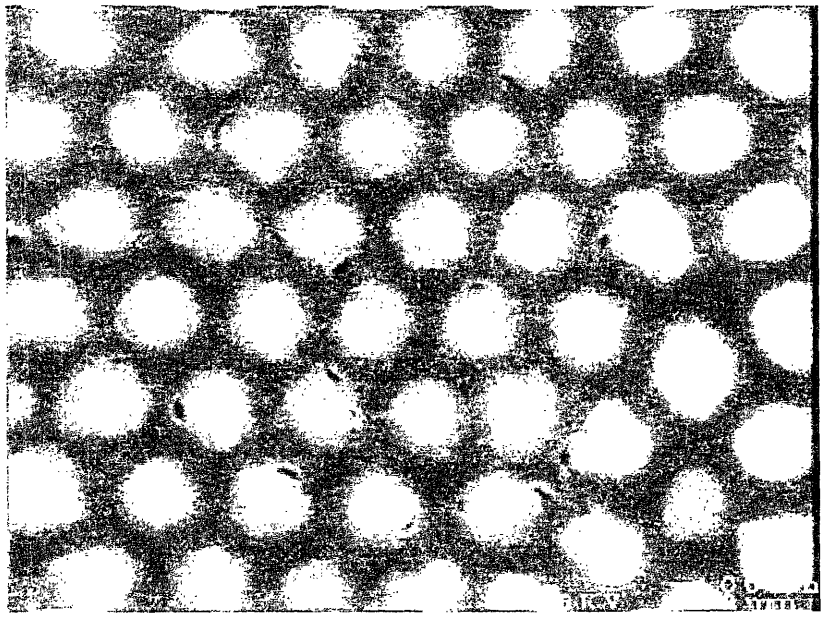


Figure 2.17: Electrodeposited copper in porous alumina.[2]

One way to tailor the dimensions of the nanoparticle is to control the film thickness of the anodized aluminum. Nanopores will only grow through the oxidized metal until they reach the silicon barrier layer (or more commonly until the reaction is stopped in the experiment). Thus, pits or long pores can be fabricated and then filled with metal to allow for nanodots or nanorods and nanowires. Additionally, carbon and other types of nanotubes can be grown as has been suggested in the literature[2, 7]. Figure 2.18-19 show SEM micrographs of a cobalt nanotube, and an ordered array of carbon nanotubes, both grown in porous alumina, respectively.

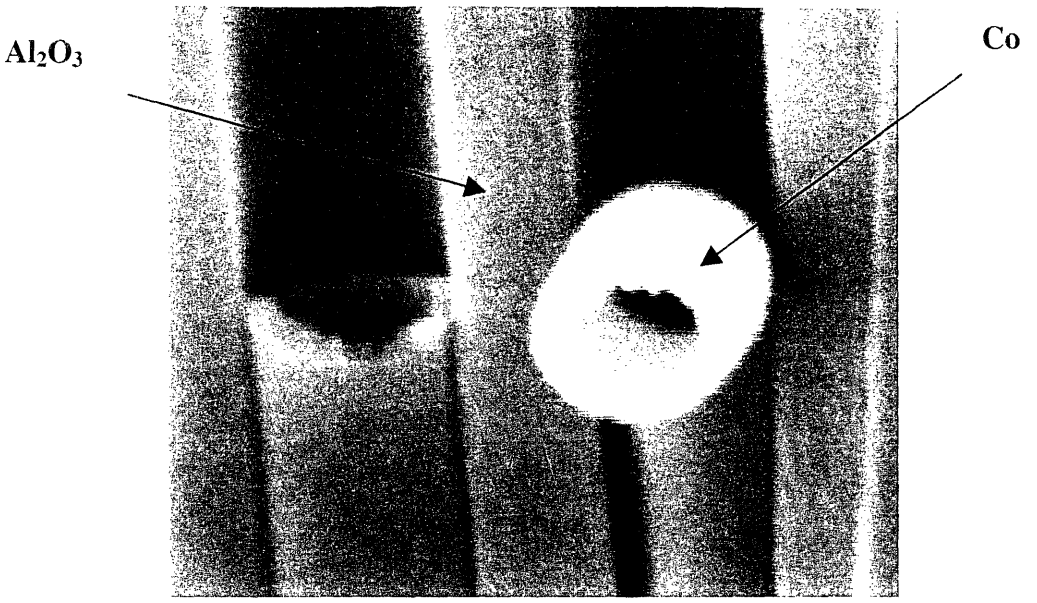


Figure 2.18: Cobalt nanotube in a porous alumina template.[2]

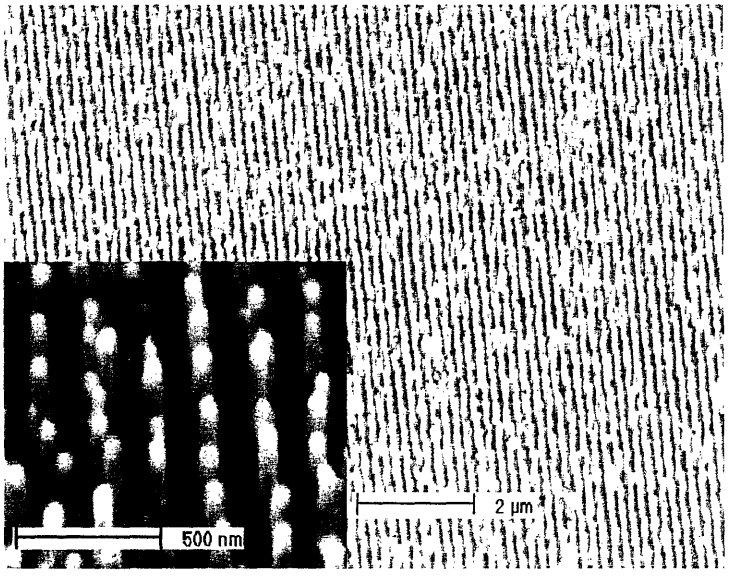


Figure 2.19: Ordered array of carbon nanotubes.[2]

Two powerful techniques, one of which is already patented, but the other of which may prove to be more valuable to template processing, have been employed throughout the MIT group's work on PATT. Both allow long range ordering and

variability of nanostructure growth. The proprietary techniques developed at MIT also offer other added benefits, such as high aspect ratio attributes.

3.0 Intellectual Property

The intellectual property landscape for PATT is scattered, at best, with most patents covering specific ways to fabricate templates and structures. There are many patents on various template processing ideas, fewer on nanostructures, and an extreme few on devices. There may only be one patent that prohibits commercialization of the techniques employed by the MIT group without licensing.

Porous alumina template technology patents are stratified in three layers. First, there are patents pertaining to the various techniques to grow alumina templates. There are many such patents, all resulting in the same final product: a porous alumina template. These template patents protect various processes derived to fabricate locally and long range ordered templates.

The second layer of patents include nanostructure growth using porous alumina templates. Groups have grown nanodots, nanowires, nanorods, and nanotubes using a variety of template processing techniques and subsequent nanostructure growth techniques. Because of the large amount of variability in the processing of various structures on templates that have been grown in various ways, there is a good bit of leeway in porous alumina template intellectual property. As there has been much more work on template fabrication than nanostructure fabrication, there are far fewer nanostructure patents currently published.

The final layer of patents include devices fabricated with nanostructures grown using porous alumina templates. There are very few patents for devices, most notably simple electron emitters[7], because most of the current research in the area has concentrated on perfecting template processing and nanostructure fabrication. Research is progressing, but will probably not focus heavily on device fabrication for another several years, as consistent reliable nanostructure growth has yet to be mastered using porous alumina templates.

The majority of patents having to do with PATT specifically detail various processes to fabricate the physical template itself. The pioneers of porous alumina template technology were Masuda et al[8]. at Nippon Telephone & Telegraph who, in 1996 first published a description of how to anodize aluminum to grow nanopores. The

technique involved the creation of topography on the aluminum surface and allowed for full pore formation and short range order through double anodization, as described in Chapter 2. Later, they showed that instead of a double anodization, stamping the aluminum could also be used to generate topography on the aluminum surface which, upon anodization grew ordered pores. The curved starter points had higher curvature, and under an electric potential, a higher flux density would exist at these higher curvature areas leading alumina generation and pore growth. A patent was issued in 2000 for the stamping technique, and the following appears as an abstract in patent # 6,139,713 :

A plurality of recesses having the same interval and array as those of pores of an alumina film, which are to be formed in anodizing, are formed on a smooth surface of an aluminum plate in advance, and then, the aluminum plate is anodized. With this process, the roundness of the pores of the porous anodized alumina film and the uniformity of pore size are improved, and the pores are regularly arrayed at a predetermined interval. The recesses are formed by pressing a substrate having a plurality of projections on its surface against the aluminum plate surface to be anodized.[8]

Masuda et al. recognized that the pores would locally order in a hexagonal array, and that this configuration was the most stable geometry, noting in the patent's second claim:

A method of forming a porous anodized alumina film according to claim 1, characterized in that the plurality of recesses are arrayed such that recesses around each recess are arrayed in a regular hexagon in the aluminum plate, and the step of anodizing the aluminum plate comprises anodizing the aluminum plate at an anode oxidation voltage obtained by dividing the interval of the recesses by 2.5 nm/V, thereby forming a hexagonal close-packed array of the plurality of pores corresponding to the plurality of recesses.[8]

Figure 3.1 shows pictorially the initial hexagonal geometry with which Masuda's group prefaced their anodization process. These starter points were generated to alter the topography of an aluminum sample before anodization. Upon anodization, pores form in the same pattern as the pretreated aluminum surface.

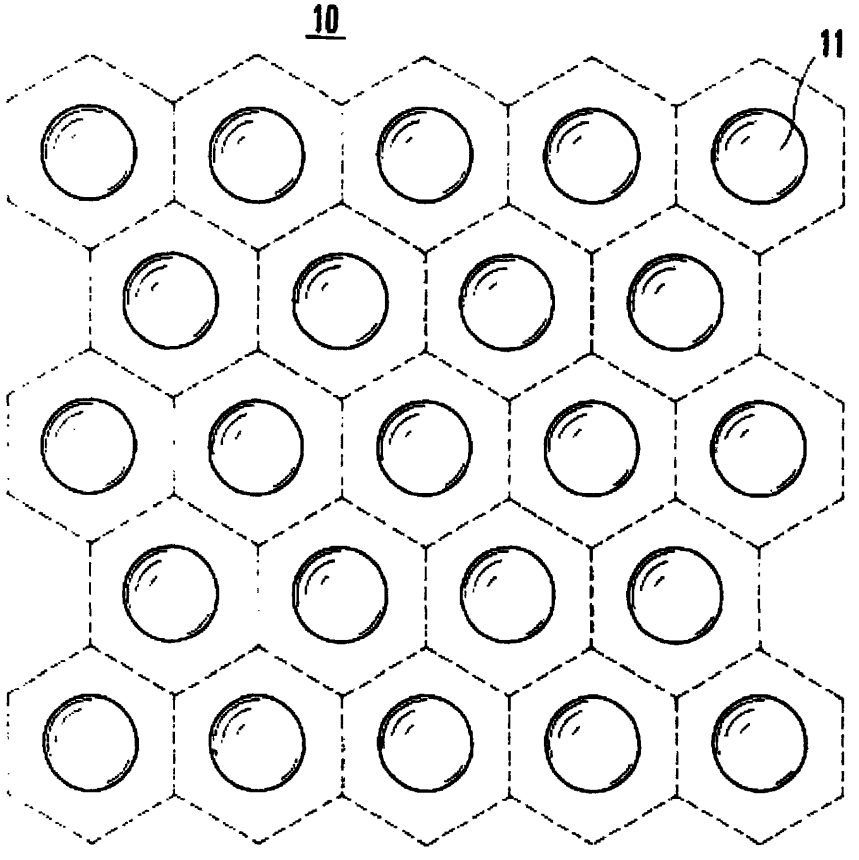


Figure 3.1: Hexagonal starting point arrangement.[8]

Masuda et al. also discuss in their patent alternative techniques to stamping. Specifically, Masuda's group mentions the idea of pre-patterning an aluminum surface through photolithography or electron beam lithography, to fabricate starter holes. Masuda et al. describe that using electron beam or x-ray lithography to create nanometer-sized pore diameters and spacings is economically unfeasible.

In the present invention, to form and array the plurality of recesses in the surface of the aluminum plate to have the predetermined interval, a resist pattern may be formed on the aluminum plate surface by, e.g., photolithography or electron beam lithography, and then, the aluminum plate may be etched. However, especially, when a porous anodized alumina film having pores at a very small interval of about 0.1 microns is to be formed, a high-resolution micropatterning technique using electron beam lithography or X-ray lithography must be used to artificially and regularly form the fine recesses in the

aluminum plate surface. It is not economical to apply such micropatterning technique every time a porous anodized alumina film is formed.[8]

Figure 3.2 from the patents shows the photolithographic patterning method pictorially.

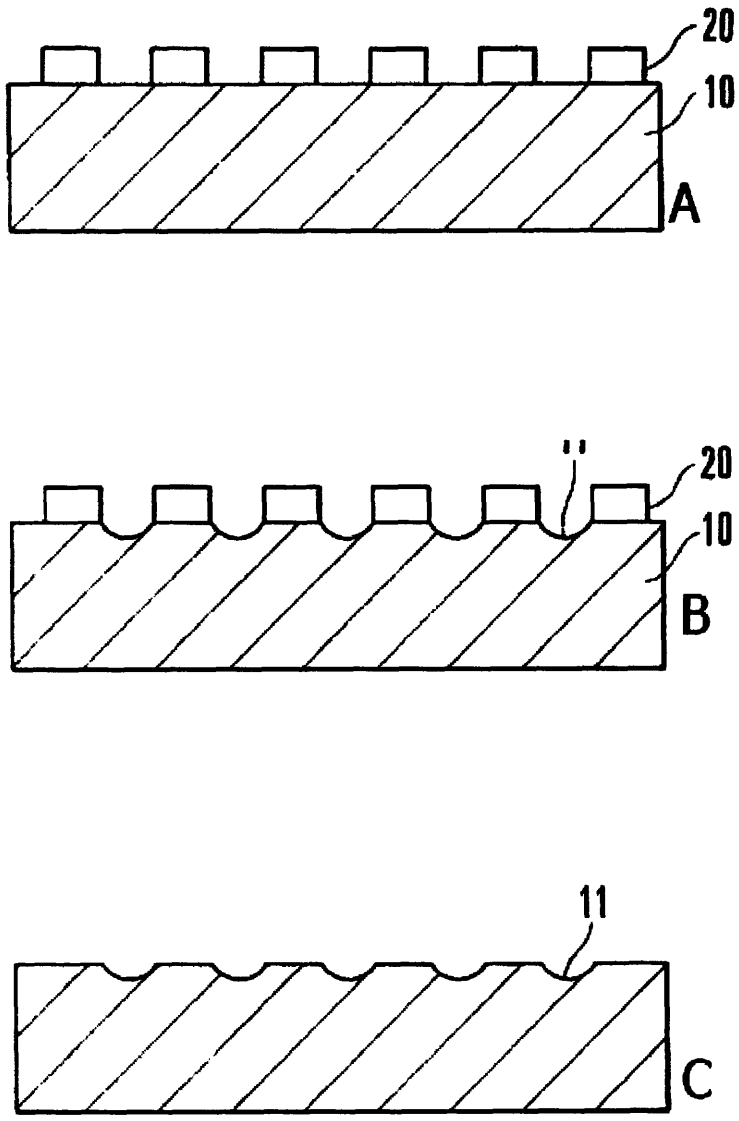


Figure 3.2: Lithographic pre-patterning of aluminum film.[8]

The use of electron beams to pattern the surface of the aluminum was not explicitly claimed in the patent. Instead, it was merely mentioned in the discussion. Of legal interest is what is technically covered in their first claim:

A method of forming a porous anodized alumina film, characterized by comprising the steps of: forming a plurality of recesses in a surface of a smooth aluminum plate in a predetermined array at a predetermined interval; and anodizing the aluminum plate to form a porous anodized alumina film having pores having a predetermined shape and the same interval and array as those of the plurality of recesses.[8]

Specifically, the line, "Forming a plurality of recesses in a surface of a smooth aluminum plate in a predetermined array at a predetermined interval," would seem to preclude electron beam patterning of an aluminum sample. However, as is shown below, other interpretations must have been considered, because another specifically claimed electron beam patterning. This is an interesting legal example of how often a very general statement can be intended to cover a broad array of ideas, but simply cannot be stretched to include all that the inventor may have hoped.

Developing and fabricating precise stamping processes and materials over a large surface area to constantly and consistently transfer a pattern through a stamping process to aluminum films is technically unfeasible. Surface roughness as well as inherent wafer and stamp curvatures would prevent such stamping mechanisms for large areas.

Another approach in making starter points was patented by Aiba et al. in 2001[5]. Instead of stamping the aluminum, they used either an electron or ion beam on the surface, similar to what Masuda et al. referenced in their 2000 patent. The first claim in Aiba et al.'s patent is as follows:

A method for producing a structure with pores, said method comprising: a step of preparing a workpiece containing Al; a step of irradiating a particle beam onto said workpiece; a step of anodizing the workpiece to form pores in the workpiece; and a step of enlarging a diameter of the pores formed by the anodizing step. [5]

The details of the anodization process remain largely unchanged between this and almost all other porous alumina template growing techniques described in various intellectual property outlets. It is the creation of starter points which varies between groups or researchers. In later claims, Aiba et al. list the particle beams which fall under the patent's coverage, including "electron, ion, or a charged particle beam."[5] Figure 3.3 shows pictorially the general idea.

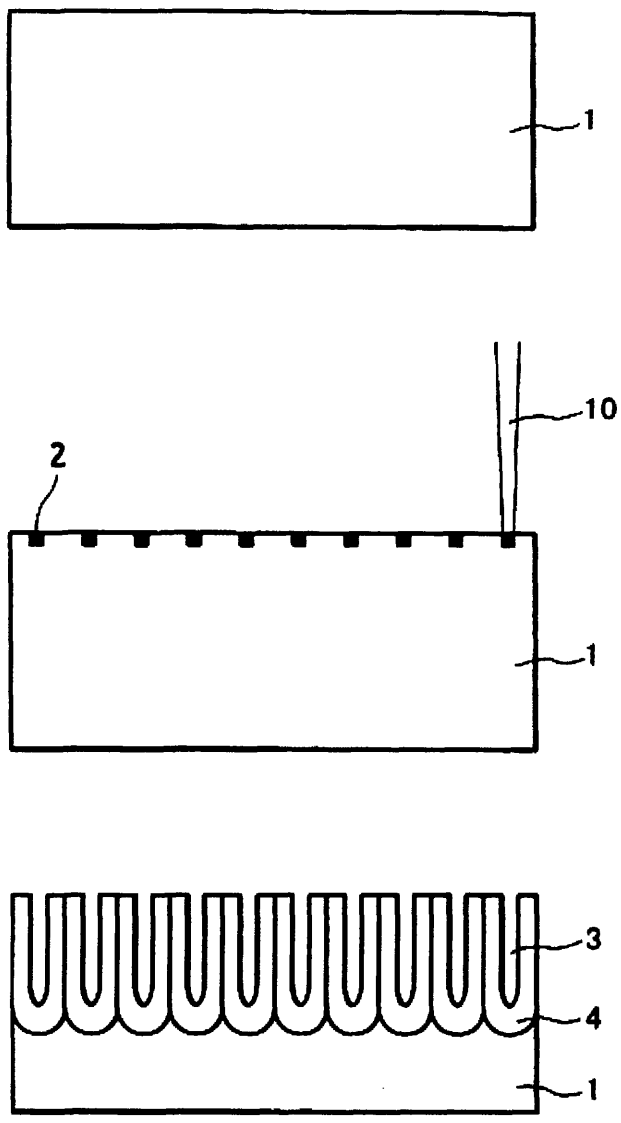


Figure 3.3: Particle beam technique for fabricating porous alumina templates.[5]

As Masuda et al. noted, mass production of templates or components based on templates created in the manner described in Aiba et al.'s patent is unwieldy and inefficient. Because electron beam processing is serially performed, it is a very slow process. This technique may be of use for small areas or ordered pores. Additionally, this piece of intellectual property may become important for low-volume specialty template applications in which just a few templates are produced with ultra-small pore diameters and inter-pore distances. Particle beam technology, though powerful, seems destined for niche applications and one-of-a-kind products.

Ohkura et al. were recently granted a patent protecting the pre-patterning of silicon prior to aluminum deposition and anodization, as described fully in Chapter 2. The group at MIT and still a third group all independently developed the same idea. Unfortunately, it appears that Ohkura et al. have the intellectual property upper-hand, holding the important patent on the process. While this is a setback for the MIT group, it is not an insurmountable barrier. Of the two techniques employed by the MIT group for long range ordering, the more powerful technique is not what Ohkura et al. have patented. Instead, it is a heretofore undisclosed process that results in high aspect ratios. The multitude of template processing techniques is important to the MIT group as it allows them additional avenues to avoid intellectual property infringement. In fact, the group's undisclosed template processing approach may well result in significant intellectual property.

Only if the MIT group started a company that commercially produced and sold templates, nanostructures or devices fabricated by the technique of silicon pre-patterning claimed by Ohkura et al. would there be any legal issues. As for research purposes, intellectual property is open to the public. Therefore, while a company that uniquely infringes on Ohkura et al.'s technique would constitute legal action, its use in research would be allowed. This means that the MIT group can continue on their current research paths without worrying about infringement until (and if) they commercialize an application which directly uses Ohkura et al.'s technique. Since there is an alternative technique used by the MIT group, which is in the process of legal activity, the MIT group has an avenue around the Ohkura et al. patent. Nonetheless, the patent is very powerful,

as it now allows them to freely commercialize products that rely on the technology or are processed similarly.

One key difference between what the group at MIT focuses on and what many other groups (outside of Ohkura et al.) have focused on previously is the goal of long range ordering. The majority of intellectual property on PATT deals with various template structures and fabrication techniques which result simply in short-range order. Concentrating intellectual property on the less densely populate long-range order idea may prove to be a key ingredient in developing a strong intellectual property portfolio.

There are other patents for various template processing techniques, but none appear to infringe on the techniques employed at MIT. As far as template processing, therefore, while there is one potential barrier, it does not seem insurmountable, and should not stop continued pursuit of PATT.

The second category of intellectual property for PATT entails developments of nanostructures grown using PATT. There do not seem to be any problems for the MIT group based on current intellectual property claims. One technique for growing nanostructures in pores is patented by another independent research group at MIT, involving a pressurized deposition of metal into a nanopore template (similar to an injection), by Ying et al., granted in 1998.[9] The patent abstract details what is protected, specifically "a technique for melting a material under vacuum and followed by pressure injection of the molten material into the pores of a porous substrate produces continuous nanowires"[9]. This technique is unlike the technique utilized by the PATT group who employ electrodeposition for metal nanostructure fabrication, and vapor phase deposition for nanotube and semiconductor nanostructures.

Additionally, Iwasaki et al., patented a technique whereby a metallic interlayer, containing some fraction of titanium, is deposited adjacent to the template. After anodization and pore growth, the template is thermally processed to allow the metal to seep into the template, resulting in nanostructure-filled pores.[10] They describe the process specifically as, "(i) providing a structure comprising a substrate having a titanium-containing surface and a porous layer containing narrow pores extending towards the surface; and (ii) forming narrow titanium-containing wires in the respective narrow pores by heat treatment of the structure obtained in the step (i)"[10]. There are

many individual claims, all of which detail similar ideas, including the use of various titanium-based materials, as well as the direction in which the nanostructures will be oriented with respect to the porous alumina (i.e. perpendicular to the titanium-containing layer). This is an interesting technique, one not previously considered by the MIT group, but one which is already protected. The techniques employed at MIT must avoid infringement on this piece of intellectual property as new nanostructure growth processes are studied.

A third patent relating to nanostructure growth was granted to Miller et al. at the University of Notre Dame du Lac in 1996 regarding the electrochemical deposition of metal to grow nanodots[6]. There is a chance that this patent could interfere with commercialization of some of the techniques being pursued at MIT and elsewhere. Specifically, the MIT group is looking at electrodeposition of metals to fabricate metal nanostructures. The major difference is that the templates manufactured at MIT offer long range order whereas the group at Notre Dame used their templates for the fabrication of nanodots on quasi-periodic templates. They electropolish single-crystal aluminum samples to form starter points, but do not mention any long range ordering assurance. In fact, they claim "semi-periodic" arrays. Long range order requires the use of a different techniques. Therefore, there is a good chance that the MIT group can avoid infringing on this intellectual property. If, on the outside chance the MIT group was limited in their capacity to fabricate nanodots similar to the way Miller et al. did, this would not be too large of an economic setback. The group could either study an improved way of fabricating them or at worst pay a licensing fee to use the technology, if the technique is employed in a commercial product. However, based on the long range order exception, it appears that the Miller et al. patent is no real barrier.

It is interesting to note that Miller et al.'s patent claims the use of substrates in their process. While using substrates is a central role in the MIT group's approaches, there would not be infringement. This is because the Miller group does not pre-pattern their substrates, or use them for the purpose of generating long range order. One claim in which substrates are noted is claim 16 which protects:

A method of fabricating nanostructures, comprising the steps of: selecting a semiconducting substrate; depositing a layer of metal on said substrate; electropolishing said layer of metal so as to form pits therein; anodizing said metal layer so as to convert substantially all of said metal layer to an oxide layer containing pores; and depositing material in said pores.[6]

It appears that the substrate simply serves as a route of integration into semiconductor devices and does not serve to allow for long range pore order.

The final layer of intellectual property involves devices made from nanostructures, which are, in turn, fabricated in porous alumina templates. There are fewer nanostructure-related patents than there are template patents, and as one would assume, there are far fewer device-related patents than either of the other two categories. Porous alumina template technology has not yet matured into a science of applications quite yet, which gives reason why the available intellectual property is focused primarily on templates and nanostructures. Simple device patents in PATT include Reed et. al's patent for conductive polymers as interconnects[11] for various electronics. Additionally, a few single electron device ideas have been patented. Specifically, Ahn et al. protected developments in manufacturing a single electron memory device, using porous materials[12]. This patent would only affect the MIT group if they commercialized a product that performs the same functions as Ahn et al.'s device. A final device patent that has been studied is attributed single-handedly to Li[13], who has patented various manufacturing methods for thin film single electron devices. As long as the MIT group avoids fabricating the same single electron device using the same processes as Li or other similar patents, this intellectual property is non-threatening as well. While single electron devices seem like one interesting application for PATT, they are not deeply considered in this document as they do not take advantage of the uniqueness of PATT. See Chapter 5 for a review of potential applications which may rely of long range ordering and other properties central to the MIT approach.

Aside from the various academic and corporate research groups (and individual patentees), there is one company that is developing manufacturing capabilities for devices based on nanoporous template technology: Nanomaterials Research Corporation (NRC). They have several processes and devices currently under development, including gas sensors, microheaters, nanowire arrays[14], and carbon nanotube field emission display

projects. The majority of their intellectual property comes from 18 patents on topics which include composite and polymer materials, micro-machining techniques, and powder technologies. A few of their patents are on how their sensors work, specifically by enhancing oxygen ion conductivity in a nanopowdered ceramic. Additionally, they have published reports[7] on how carbon nanotubes may be combined with PATT to create field emission displays (FEDs). Details of this application are discussed in Chapter 5, but from an intellectual property standpoint, the idea is already out. Commercializing FEDs could still be a possibility if the application matched up well enough with what PATT has to offer. Again, it doesn't seem that their intellectual property will be a large barrier to what the group at MIT is doing, even though they are working on similar technology. From a business strategy point of view, NRC has already launched a company and has first-mover advantage for commercializing products. While many of their devices are currently under development, their status as an independent company is quite an advantage.

While there seems to be many groups working on nanotechnology using templates, it doesn't seem that the group at MIT has too many uncontrollable issues regarding what they can and cannot pursue from an application standpoint. It seems that there is a lot of room for future intellectual property.

The onus is on the MIT group to quickly and broadly claim all of the ideas they have developed. The key to intellectual property is in claiming the most fundamental ideas possible. While some of the fundamental aspects of what the MIT group is doing remain unpatentable (because of publication or previous intellectual property), there are still many good ideas percolating in laboratories which could be of interest and value to existing or new companies. Protecting these ideas is paramount to earning financial dividends from scientific discovery.

Overall, porous alumina template technology has many scattered patents with no one group holding on to many major patents that would influence others. In the absence of template patents, however, nanostructure growth and device fabrication patents may prove to be equally powerful if a market is developed requiring their use in an application. The difficulty with these top two layers is that one must predict the future. The more fundamental the patent, the less accurate the prediction must be since one

patent may cover ideas that have yet to be developed. The idea of disruptive technologies, as described by Professor Christensen[1,50] in The Innovator's Dilemma and The Innovator's Solution, underscores the point that true market disruption results from applications which are initially unbeknownst to the inventor, but which later prove to be important. So it may be with PATT. The applications of tomorrow may not be foreseen today. Therefore, claiming as much intellectual property as possible, regardless of the importance of the idea, is the most important step to securing a place in the future of PATT marketability.

4.0 Competing Technologies

In order for porous alumina template technology (PATT) to effectively create or infiltrate a market or application, there must be at least one differentiating property which grants PATT a competitive advantage. It is simply not sufficient for PATT to replace another technology just because it is newer, it must prove to be better in at least one critical area for it to be a part of a device or application. Porous alumina template technology has already been described in detail in previous sections, and in order to provide evidence of superiority in a certain application, it is necessary to analyze competing technologies which offer similar avenues to accomplishing what PATT aims to accomplish, namely nanotechnology fabrication.

One notable benefit of PATT is its ability to allow the fabrication of nanostructures which border on current lithographic limits. In the processing of integrated circuits (ICs) and memory devices, Moore's Law predicts the progression of device geometries to smaller and smaller sizes, as described earlier. At present, there are lithographic limits which prevent processing of structures past around 70 nm. This so-called "0.07 μm" technology is still under development by leading research and development companies such as IBM. Using lithographic tricks and new techniques, researchers have found ways to shrink geometries to unprecedented sizes. Lithography, therefore, is a competing technology for PATT.

Lithography in its truest sense is simply a technique to transfer a pattern from one medium to another. Early lithography was used to make engravings, drawings, and designs on paper or other substrates. It is used by the microelectronics industry to transfer circuitry patterns from a mask to a silicon wafer. Layers of circuitry are patterned on top of each other in this way until a completed wafer can be broken into dies and inserted into electronic packages for sale as microprocessors or memory devices. This is a simplified description of wafer processing, used solely to identify the importance of lithography.

There are many types of lithography, and by far the most common process used currently in wafer fabs and research laboratories is photolithography. Photolithography entails four major steps: spinning resist onto a substrate; patterning the resist with a mask;

removing the desired area of resist; etching the desired area of substrate. If the resist is "positive", the pattern is exactly transferred, and if "negative", the inverse image of the pattern is transferred.

Figure 4.1 shows a typical photolithographic process pictorially.

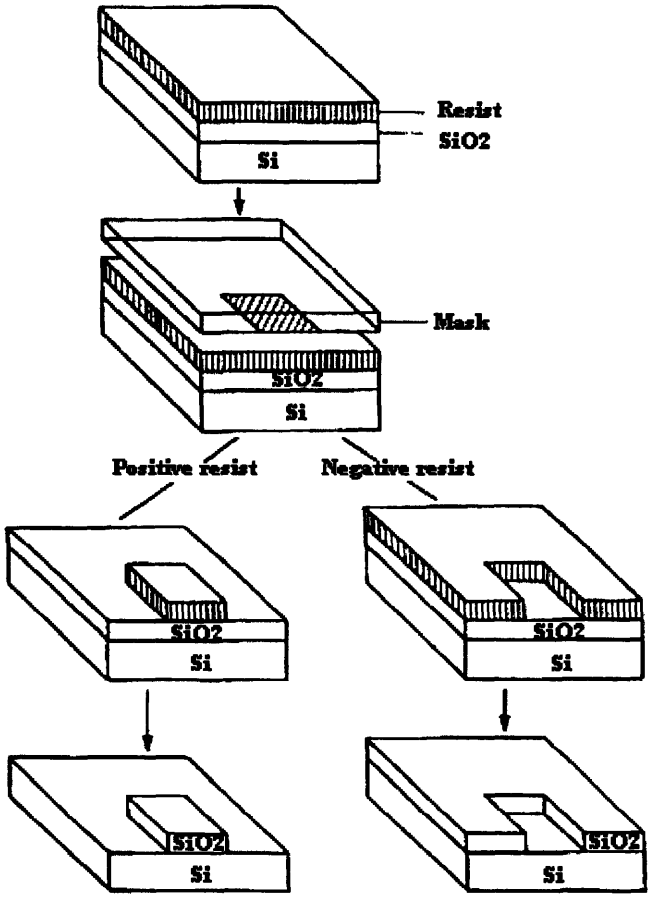


Figure 4.1: Four major steps in photolithography.[17]

Figure 4.1 shows how to create an SiO_2 pattern onto a Si substrate, perhaps for use as a gate oxide. The Si substrate is first covered with a thin film of SiO_2, and a layer of photoresist is then spun on. Photoresist is typically deposited by spin-coating, a

process in which the substrate wafer is adhered to a vacuum chuck, and spun at high speeds (between 1500-8000 rpm). A few drops of the polymer-based photoresist are deposited into the middle of the spinning wafer and centrifugal forces send the resist radially outward to the edges of the wafer, covering its entire surface area. Photoresist can be continually added while the wafer spins to attain a desired thickness. Figure 4.2 shows the spin-coating process pictorially.

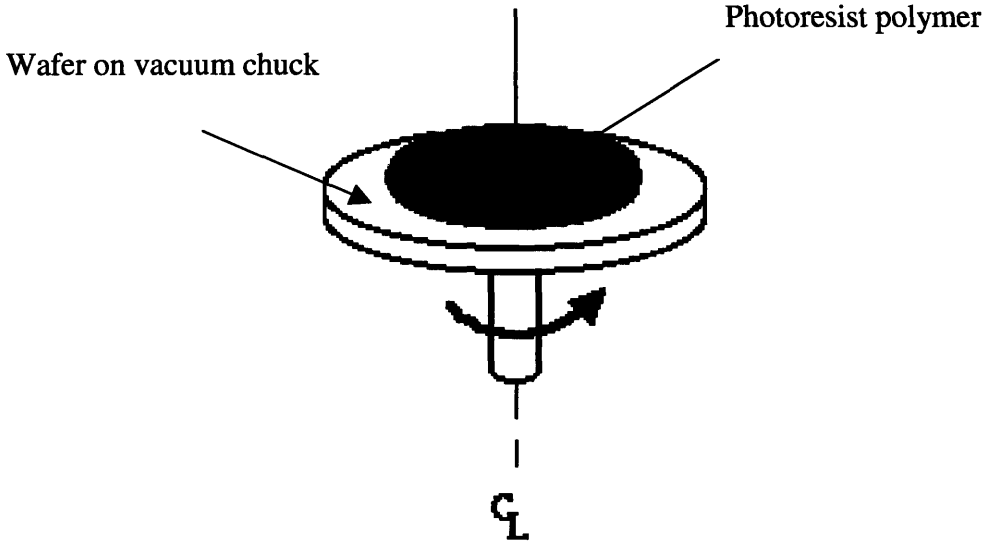


Figure 4.2: Spin-coating of a substrate with photoresist.[18]

One important empirical relationship used to determine the thickness, T, of a photoresist layer is shown in Equation 4.1,

$$T = \frac{KC^{\beta}\eta^{\gamma}}{\omega^{\alpha}} \qquad \text{Eq. 4.1}$$

where K = a calibration constant, C = polymer concentration of photoresist (in units of g/100 mL), η = intrinsic viscosity of the photoresist, ω = rotational velocity (in units of rotations per minute), and α, β, γ are experimentally determined exponents.[19] Calculating photoresist thickness in real-time allows the deposition tool to maintain consistent precision over thousands of process cycles. Device features with high aspect ratios are difficult to attain under current photoresist technology, and the average photoresist layers are nearly 1 μm with a tolerance of roughly +/- 1 nm. These typical industry standards for modern devices (with feature sizes nearly 0.07 μm) are approaching current photoresist technology limits. As photoresist thicknesses get thicker and thicker for high aspect ratio devices, it is more difficult to maintain a low surface roughness across an entire wafer of 200-300 mm diameter.

The next step in photolithography, as shown in Figure 4.1, is pattern transfer from a previously fabricated photomask to the surface of the photoresist. The photomask is typically made of an optically transparent (up to and including ultraviolet frequencies of light) glass with an opaque pattern etched into the mask. It is this pattern that is transferred to the photoresist upon the application of ultraviolet light. The fabrication of photomasks is typically done through electron beam lithography, a different type of pattern transfer process described later. The opaque regions of the mask absorb rather than transmit light, and often include thin metal films such as chromium films on the order of 80 nm.[19]

Three types of photomasks are generally used: contact masks, where the mask is in direct contact with its complementary photoresist film; proximity masks, where the mask is slightly raised above the surface of the substrate; and projection masks, where the mask is farther away and the masked pattern is projected through a lens system onto the substrate. The substrate is then exposed, chemically changing unmasked areas of the substrate so that they can later be developed. After exposure, the photoresist is developed (removed) by the application of an acidic species which will preferably attack either the masked or unmasked portion of the substrate surface, depending on whether a positive or negative mask is used. Once a positive or negative pattern has been transferred from the photomask (through a lens system, if applicable) onto the photoresist, the next step in photolithography, as shown in Figure 4.1, is to etch through the substrate so as to transfer

the photoresist pattern onto the substrate below it. The final amount of residual photoresist that was removed during development can now be removed, resulting in a given feature. In commercial semiconductor fabrication operations, dozens of photolithographic steps are performed to build a final intricate multi-layered array of chips.

The two most important quantitative relationships for gauging photolithography technology are the resolution and depth-of-focus (DOF) resulting from projection printing. The resolution, R, is a function of the ultraviolet light's wavelength, and can be written as follows:

$$R = \frac{k_1 \lambda}{NA} \qquad \text{(Eq. 4.2)}$$

where k is experimentally determined and depends on the photoresist, certain process parameters, and the optics used in mask alignment; λ is the wavelength of light used in the process; and NA is the numerical aperture of the lens system.[19] It has been found that typical values of k can go no lower than 0.4, while NA ranges between 0.16 and 0.60. The numerical aperture is a rating of the amount of light that a lens system allows through. According to Madou, "The numerical aperture in a medium of refractive index, n, defines the angle of acceptance, $2\theta_{max}$, of the cone of diffracted light from the photomask that the lens can accept"[19]. Therefore, when NA = 0, the lens does not procure any of the light, whereas NA = 1 describes the state where the lens procures the entirety of light that strikes it. Equation 4.3 relates these details to lens geometry:

$$NA = n \sin\theta_{max} = \frac{D}{2F} \qquad \text{(Eq. 4.3)}$$

where D is the lens diameter and F is the focal length normalized by D.

Depth-of-focus is an extremely important quantity that measures how consistent a feature's dimensions remain through the thickness of the photoresist. The higher the DOF, the larger a feature's aspect-ratio can be fabricated within specified tolerances. Specifically, DOF is a measure of the defocus tolerance of an imaging system and can be written as:

$$DOF = +/- \frac{k_2 \lambda}{(NA)^2} \qquad \text{(Eq. 4.4)}$$

where k_2 is again a constant depending on various process parameters which generally takes on a value of around 0.5. From Eq. 4.2, it is apparent that to attain good resolution requires a decrease in λ, or high frequency ultraviolet light, as well as a large numerical aperture. However, as Eq. 4.4 details, these same constraints work against the subsequent DOF. Therefore, while the resolution may allow for smaller and smaller line widths on an integrated circuit, for example, the DOF will be much lower forcing the design to include very small resist layers. Ultimately, this prevents small features with good resolution from even being fabricated because the feature defocuses outside tolerance limits while being transferred through the thickness of the photoresist. Additionally, this can have an effect on a photolithographic tool's ability to process devices with high aspect-ratios which may require thick photoresist films.

There is a constant battle between feature size, quantified by photolithographic resolution, and fabrication capabilities, quantified by DOF. As inversely proportional quantities, each plays the role of limiting agent on the other during device designs. There are many commercial techniques, such as variable NA tools, which can help to balance resolution and DOF during processing. These techniques give more leeway to device designs and allow for smaller and smaller feature sizes.

Photolithography has long been used as the pattern transfer technology of choice in semiconductor fabrication operations, both industrial and academic. This is largely due to the immense amount of research and pervasive knowledge there has been on the

subject over the last thirty years. However, as device features continue to shrink, lithographic alternatives are being sought. Many MEMS devices seek structures and devices with high aspect ratios. Traditional photolithography does not satisfy the MEMS criterion, nor will it continue to sustain IC technology at the current Moore's Law pace. For nanotechnology endeavors, photolithography may fall short of its hopes. Recent research has allowed for photolithography of feature sizes near 70 nm. Overexposing and overdeveloping photoresist layers is one technique that is currently under study[21]. However, one major drawback is that these techniques have not yet been proven successful at creating anything but the simplest shapes. They may have a niche application in fabricating isolated transistor gates. Interference lithography is performed by interfering laser beams at the surface of a wafer, and has been used to fabricate gratings with 200 nm period[22]. It has been shown that trim and blockout masks may be incorporated into the process to allow for the fabrication of simple devices.[23] Again, complex circuits have yet to be proven effectively producible with photolithography.

Recent developments in photoresist technology have been targeted at the development of high aspect-ratio devices and systems, most notably in field of MEMS. An IBM-developed material with the trade name SU-8 was first used for high aspect-ratio fabrication. The epoxy-based negative photoresist has many interesting materials properties which allow it to trump conventional photoresists in its ability to print high aspect-ratio features with sufficient resolution. First, it is sensitive to near ultraviolet radiation (~400 nm) and maintains very low optical absorption in this regime. This means that the UV light which strikes the SU-8 photoresist during exposure is consistent all the way through the SU-8 film, allowing high aspect ratio structures to be processed. Some structures having aspect ratios as high as 14:1 with 300 nm lateral dimensions and nearly vertical sidewalls have been obtained[24]. Additionally, the molecular structure of SU-8 allows for good thermal (up to 200 C) and chemical stability. There is a significant amount of cross-linkage upon exposure of SU-8. Its chemical composition, shown in Figure 4.3, presents another important quality of SU-8: low molecular weight (~7000 amu).

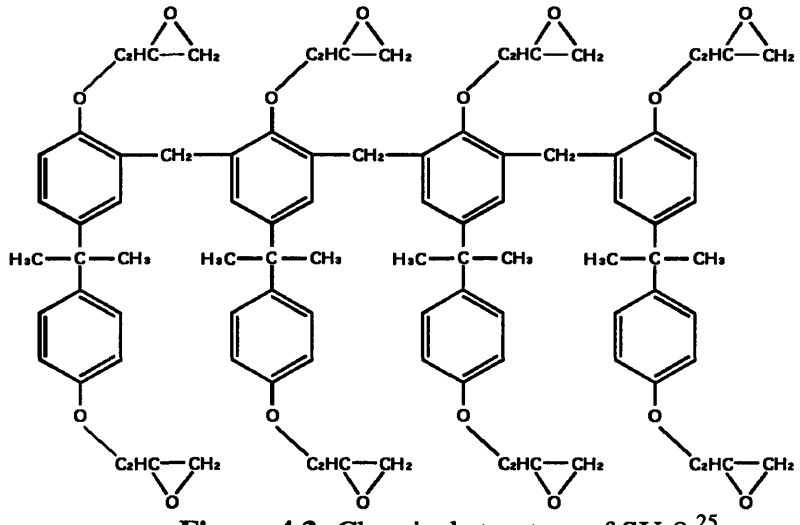


Figure 4.3: Chemical structure of SU-8.[25]

A low molecular weight means SU-8 can be dissolved by a host of organic solvents, including propylene glycol methyl ether acetate (PGMEA), gamma-butyrolactone (GBL), and methyl iso-butyl ketone (MIBK)[24].

Many SU-8 applications include 3-D MEMS structures which can be fabricated without the typical layer-by-layer processing required for ICs. While SU-8 has many benefits, its drawbacks as well as other competing technologies have limited its applications commercially. Its chemical inertness makes it difficult to strip cured SU-8 when necessary. Additionally, while it allows marginally high aspect ratio structures, other techniques such as LIGA and deep reactive ion etching (DRIE) allow for much higher aspect ratios (> 30:1). One important advantage of SU-8 is its low cost in comparison to other competing technologies, and there may be a market in MEMS applications, such as micro-fluidics, ink jets, and optical waveguides[26], in the future. At this point, however, most research has concentrated on the aforementioned technologies and on PATT as well.

One way in which resolution can be increased in conventional lithography is through the use of phase-shifting masks (PSM). Diffraction patterns of light can often cause areas of photoresist that are supposed to be masked to be exposed instead. The theory behind PSM is that when incorporated into the photolithography process, they can

invert the phase of some of the light that hits a wafer. The subsequent destructive interference around the frontier of exposed/unexposed edges is crisper and sharper.

Conventional photolithography uses light with $\lambda = 193$ nm, and with resolution enhancing techniques, including the use of PSMs, industries have been able to manufacture critical feature dimensions approaching 70 nm. A natural extension for future technologies is the use of extreme ultraviolet (EUV) photolithography. Instead of conventional wavelengths of light, so-called "soft x-ray lithography" is employed using wavelengths ranging between 10 and 14 nm. One drawback to this technique is that most materials absorb EUV radiation, so not only does the processing have to be done under vacuum conditions, but the masks must be reflective, as opposed to refractive in conventional lithography.

Recent advances in materials science have allowed for some development in this area. Multilayer Bragg reflectors, incorporating varying reflective capabilities are being studied. The most notable reflective coating is Mo/Si, which has a peak reflectivity of 70% at $\lambda = 13.4$ nm. However, cost concerns would be likely in industry since EUV systems would have to be under vacuum. Additionally, fabricating reflective coating with low defect densities has been a consistent problem and is another reason why EUV technologies have not yet proven to be the answer to nanolithography.

Another competing technology under development for nanofabrication applications is x-ray lithography. X-ray lithography has many advantages over traditional photolithography. Exceptional DOF and resolution can be attained with minimal light divergence through a proximity mask due to the wavelength of x-rays, ~ 1 nm. This allows for the fabrication very high aspect-ratio structures. In fact, x-ray lithography has been shown capable of reaching aspect ratios near 100:1 (for dimensions on the order of 1 micron in LIGA processing, described below). There is not the same problem with light absorption of x-rays as there is with EUV, and because photons are the main conduit of patterning a substrate, vacuum processing is not a prerequisite. X-ray tools do not use optics to transfer patterns as conventional photolithography does, therefore expensive optics equipment is not needed. However, this, in turn, vastly increases the cost of mask manufacturing, which has kept many companies away from

investing in the technology. As a result, there are few groups working on x-ray lithography development[19].

In the same vein as x-ray lithography resides LIGA, a German acronym for Lithographie, Galvanoformung, Abformtechnik, or lithography, electrodeposition, and molding. Incorporated in LIGA is the use of high energy x-ray radiation with the express purpose of fabricating trenches in polymer masks[54]. Poly-methyl methacrylate (PMMA) is typically used in LIGA applications, giving trench stability. Finally, metal is electrodeposited onto the PMMA resist and into the trenches to form high aspect ratio structures with vertical side walls. These structures are of great use in MEMS applications.

Processing with LIGA requires that the substrate be electrically conductive (for the electrodeposition), and it must adhere well to PMMA or whichever resist is being used. Stainless steel or copper plates are often used after first being electroplated with Ni, Au, or Ti. When silicon wafers serve as substrate, a thin film of Ti or Ag/Cr is typically deposited for conductivity. For Si substrates, adhesion chemistry is of particular importance as PMMA does not readily bond with silicon. Polymer substrates can even be used in processing, provided a requisite conductive coating is first deposited before LIGA processing.

The resist requirements include a high x-ray sensitivity for ease in chemically alteration upon lithographic processing. The resist must also withstand electrodeposition parameters, and therefore must be thermally and chemically stable. While PMMA is used predominantly in industry and research, it is prone to cracking under certain process conditions (including temperature changes). Controlling resist deposition and LIGA processing is crucial to sidestep these issues.

There are three major types of resist fabrication for LIGA. The conventional lithography technique of spin-coating is often employed, but is only practical for thin resist layers. Commercial PMMA layers can be purchased and used for larger film thicknesses where high aspect ratio features are important. Finally, in-situ polymerization can be performed under high pressures to mold very precise thicknesses of resist, as shown in Figure 4.4.

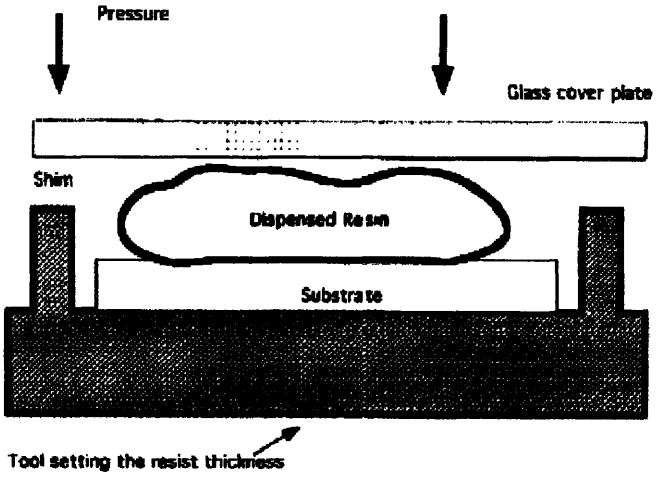


Figure 4.4: In-situ polymerization of PMMA resist.[19]

The advantage to this approach is that the thickness can be controlled during the process, whereas purchasing commercial PMMA sheets does not allow mid-process design changes. A drawback to in-situ polymerization is residual stress and cracking, which one generally does not have to worry about with commercial grade layers.

In x-ray lithography, the x-rays themselves are typically generated through the use of a synchrotron, which accelerates electrons in a circular motion. This generates centripetal acceleration of electrons and subsequent x-radiation as the electrons approach the speed of light, as shown in Figure 4.5.

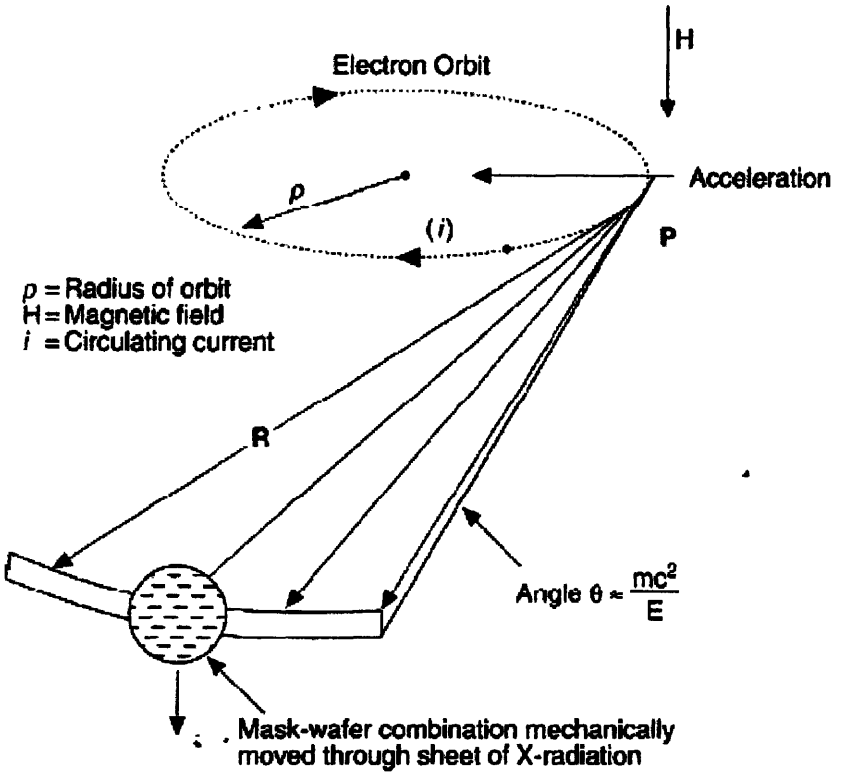


Figure 4.5: Schematic of x-ray generation by electron acceleration.[19]

Although the wafer is not under vacuum, the x-rays are under vacuum during travel from the synchrotron to an area near the wafer. A beryllium glass transparent to x-rays separates the two compartments, and the wafer atmosphere is generally helium-rich to avoid losses that would occur in plain air. Areas of resist exposed to x-rays suffer a decrease in molecular weight as covalent bonds are broken in PMMA. The lower molecular weight allows for solubility in the development solvent.

When metal is electrodeposited onto the developed wafer, the substrate serves as the cathode in an electrolytic cell. The maximum deposition rate, r, is given by:

$$r = \eta \frac{iM}{Fz} \qquad \text{(Eq. 4.5)}$$

where M is the molecular weight of the deposited species, i is the current, z is the valence of the ions in the cell, and η is an efficiency parameter.[19] Process growth rates are typically no more than 10 μm/min and resulting materials properties of the deposited species can vary greatly with small changes in process conditions. Residual stress, hardness, and surface roughness are all affected deposition rate, resist surface roughness, and temperature.

LIGA allows for reproducible high aspect ratio structures with good surfaces and adequate pattern transferability. However, the main drawbacks to LIGA processes are two-fold. First, the extremely high cost of the process is driven by the requirement of a synchrotron and support equipment. Secondly, with advances in SU-8, DRIE, and other technologies, LIGA is currently considered to be a "middle-ground" type process, uniquely capable for only limited applications. One potential application for LIGA processing is electromagnetic actuators, and there are several groups, predominantly in academia, that are heavily focused on LIGA process development and cost reduction.

Several other more advanced lithographic alternatives serve as competing technologies to PATT as well. Charged-particle-beam lithography encompasses both electron and ion beam lithography and has many unique advantages over conventional photolithography. Electron-beam lithography (EBL) allows for very good resolution through the use of a high energy focused electron beam to directly write a pattern onto a photoresist. Whereas photolithography is limited by diffraction of light, EBL, like x-ray lithography, is characterized by quantum waves which have extremely small wavelengths as high energy electrons. Figure 4.6 shows a typical EBL tool setup.

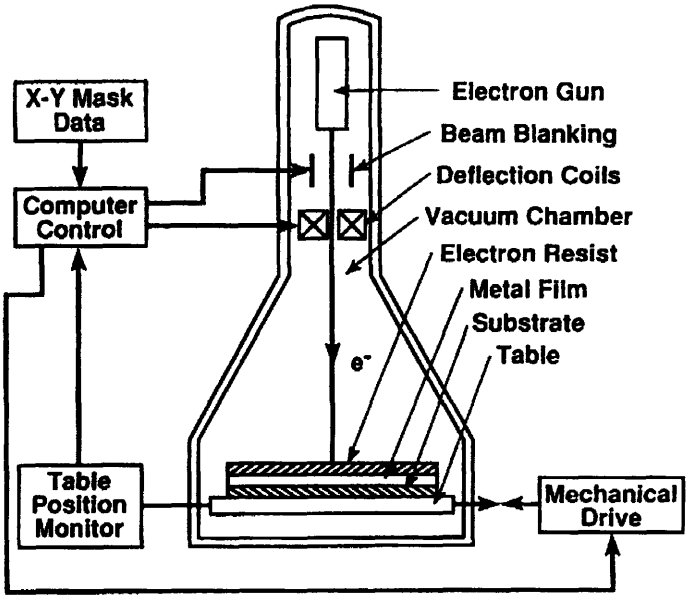


Figure 4.6: EBL setup.[27]

One important advantage to EBL is that no physical masks are required, saving the high cost of having to manufacture or purchase masks for EBL fabrication. The electron beam is focused and driven across a wafer through the use of electric and magnetic fields in order to form a proper pattern on the resist. Software masks replace physical masks and are incorporated into the computer control in Figure 4.6. It is much easier to install new masks or edit existing masks because of this virtual character.

There are two types of direct-writing techniques for EBL, shown in Figure 4.7 as raster and vector scans. Raster scanning entails a pre-defined side-to-side path for the beam, much like in a television. The shutter is controlled by the mask software to open and close at specific times to generate a pattern. The beam, therefore, can remain on throughout the entire process. Controlling a shutter is more cost-effective than controlling the beam itself in terms of tool costs. However, a consistently running electron beam would incur higher energy and other variable costs throughout its lifetime.

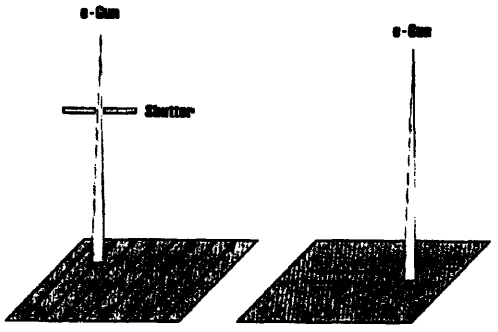


Figure 4.7: EBL direct-writing techniques.[27]

The second type of direct-writing technique is vector scanning. In this scenario, the electron beam itself is controlled and driven by the mask software to create a given pattern on the resist. Both positive and negative resists are available for EBL, and Table 4.1 lists several of the most common resists along with their minimum resolutions.

Table 4.1: Various resists used in EBL.[27]

	Tone	*Resolution nm*
PMMA	Positive	10
EBR-9	Positive	200
PBS	Positive	250
ZEP	Positive	10
AZ5206	Positive	250
COP	Negative	1000
SAL-606	Negative	100

There are many advantages to EBL. The user can control electron energies and dosages as well as focus a beam spot to < 10 nm, as opposed to the 500 nm spot typically generated by light. This allows for the fabrication of very small features. Additionally, the DOF is very good because the beam can be refocused as the topography of the wafer changes. Some of the drawbacks to this approach include electron scattering, which occurs readily in solids and limits resolution to no smaller than 10 nm, though limits on current EBL systems are generally around 60 nm. These proximity effects can be marginally controlled through the use of proximity effect algorithms, but this requires more investment in time and money for the manufacturer. Because electrons are charged particles, they must be kept in a vacuum, raising the cost of developing or purchasing an EBL system. The final, and perhaps most important, drawback to EBL is the immense investment of time required to process a single wafer. Because a beam of electrons must physically write each feature, it often takes up to an hour to write one complex pattern onto a 4-inch wafer, which is only a third of current commercial wafer diameters[19]. This process is unfeasible for mass production of nanoscale devices or ICs. However, EBL is powerful nonetheless and has appeal for niche market and small volume nanodevice manufacturing as well as, more commonly, physical mask making for photolithography. Electron-beam lithography is best used in circumstances where precision and small feature size is a priority while process time is not.

Some current areas where it is being used is for the fabrication of GaAs ICs and optical waveguides.[28] As is noted in the Handbook of Microlithography, Micromachining, and Microfabrication, "both the flexibility and the resolution of electron beam lithography are used to make devices that are perhaps one or two generations ahead of mainstream optical lithography techniques".[23] IBM has been extensively researching the use of EBL for device fabrication, and has produced many devices through the technique, one of which is shown in Figure 4.8. Note the ability of EBL to produce feature sizes of 70 nm, as the active gate structure appears in the figure. Other research endeavors incorporating EBL have included the study of various quantum effects, such as the Aharanov-Bohm effect which studies the interference of electrons traveling in different paths under an applied magnetic field.[29-31] Finally, single electron transistors

have been fabricated using EBL and may serve as a future step along the path of Moore's Law.

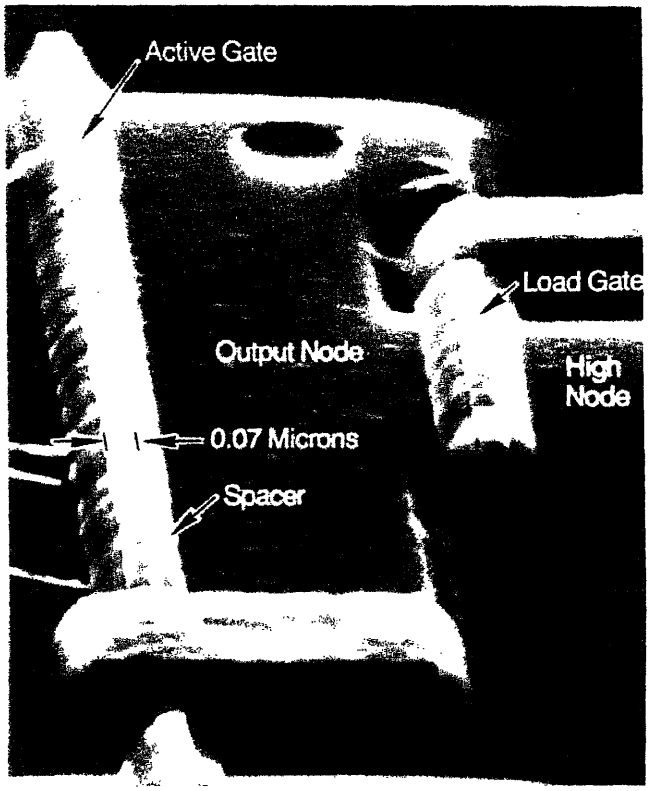


Figure 4.8: IBM IC produced with EBL. Note gate dimensions < 100 nm.[23]

Scanning probe lithography (SPL) is yet another alternative technology for realizing nanosized features. It only differs from EBL in that it utilized lower-energy electrons (< 50 eV) than does EBL to avoid the detrimental effects of backscattering from which EBL suffers. Additionally, SPL tips are positioned much closer to the wafer than in EBL systems, and therefore smaller beam spots are attained. A major drawback to SPL, however, is that it takes an even higher dose of electrons to pattern a substrate than for EBL, which is already a time-intensive process[19]. Both SPL and EBL continue to be reviewed and studied by many academic research groups.

Similar in some ways to EBL and SPL is ion-beam lithography (IBL). Liquid metal sources are predominantly used to generate the ion beam. These sources consist of either liquid Ga, In, or Au on a beam tip and exposed to a high electric field which breaks atomic bonds and creates the ions. This technique allows for high current densities (up to 8 A/cm^2) with a beam diameter of 50 nm or less. The ions are accelerated towards the resist-covered wafer in much the same way as in EBL, however the reaction of the ions at the surface allows for a greater variety of surface modifications, including patterned doping. This would be useful in processes where a very small area needs to be doped with a certain metal. When a focused ion beam (FIB) is utilized, resolution approaching that of EBL can be attained (beamspot sizes of ~6 nm). As with EBL, there are several groups working on IBL, including one group that has been able to produce an array of nanodots with dimensions of 10-20 nm in 60 nm thick PMMA resist[32]. So-called deep ion-beam lithography (DIBL) has been used by another group to fabricate 300 nm walls at an aspect ratio of 100:1[33]. These niche processes are typical of IBL and other advanced alternatives, as the technology has not yet proven to have stronger advantages than disadvantages. A group at the University of California, Berkeley is sending low energy ion beams through micron-sized holes in a mask. The holes can be controlled to be open or closed to allow or block ion beams passing through, much like the shutter in an EBL system. This allows the group to change masks very easily by simply programming a different pattern of holes to be opened and closed[34].

Drawbacks to IBL are similar to EBL in that the beam must be serially scanned over a wafer to write a pattern onto the resist. This results in a time-intensive process. Additionally, the process must be done under vacuum which raises the cost of the technique.

Another interesting technique currently being researched for application in nanofabrication is dip pen lithography (DPL). As shown in Figure 4.9, DPL is a completely different process than the previously described lithographic techniques. In DPL, an atomic force microscope (AFM) tip is used to physically write molecules onto a substrate surface through chemisorption. The tip is generally silicon nitride, and one deposition material of choice for researches is 1-octadecanethiol (ODT)[35-40] because of its chemical affinity for many substrates, including Au. As the AFM tip comes close enough

to the substrate to form a water meniscus, molecular transport commences and the ODT on the tip then is attracted to and travels towards the substrate. The meniscus is controlled predominantly by the relative humidity of the atmosphere in which it is being used, and in turn controls the rate of mass transport from tip to substrate, DPL resolution, and the area of contact of the tip to the substrate.

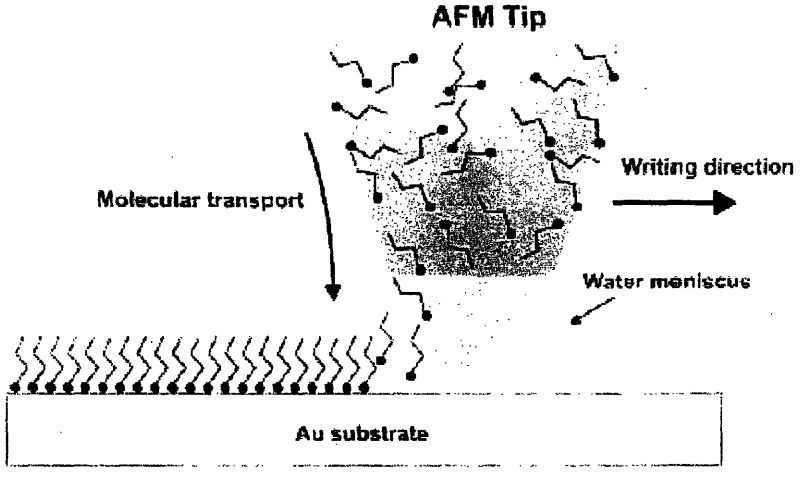


Figure 4.9: Dip pen lithography through molecular transport.[35]

Humidity control therefore is crucial to successful operation. As a result, it is also a drawback to the technique, as much care must be given to ensure that the humidity of the environment is constant and at an appropriate level for desired results. Another major drawback is that, like EBL and IBL, DPL is a serial writing technique, requiring a lot of process time. Nevertheless, there are still many groups, most notably at Northwestern University where DPL was first developed, working on improving the technique. One group is accomplishing DPL through the use of aqueous Au nanocrystal dispersions which they try to deposit onto a substrate, and which upon drying result in Au nanocrystals patterned onto an Au substrate[41].

While it may seem that there are innumerable alternatives to PATT for nanofabrication applications, there are many groups using scaffolds for nanofabrication. A group at the University of Massachusetts is using a liquid interface as a scaffold for

nanoparticles by surrounding water droplets with an oil solution that has nanoparticles. The nanoparticles, it's been found, will encapsulate and support the water droplet at the liquid-liquid interface. The process for controlling the placement of nanoparticles allows for the creation of 3-dimensional structures made of nanoparticles[42, 43] and a liquefied alternative to PATT. This research is nascent, however, and is not overly widespread at this point.

Reaching further to the bounds of nanotechnology, there is a self-assembly technique being researched at Northwestern University, which uses the same alumina scaffold feature as that which has been presented in this document. Similar to PATT, the group is synthesizing gold and polymer segments in porous alumina template to create nanorods of varying composition of polymer and gold. The team then dissolves the template leaving an array of parallel rods. The polymer ends of the rods interact with each other causing stresses to form in the rods and subsequent bending. This ultimately produced nanostructures with curves and shapes. The leader of the group underscored the importance of PATT as a central technology to the fabrication of ultra small features, as the previous lithographic technologies aim to become as well, "The research clearly shows that some unnatural building blocks, such as the gold-polymer rods, need assistance in order to form higher-ordered structures. This means that when we work with building blocks that are larger than molecules but smaller than macroscopic objects, we should consider building materials in a completely new way - by using templates to help guide the assembly process and reduce the large number of assembly pathways potentially available to the building blocks[44]".

One final competing technology which seeks to accomplish similar goals as PATT, namely high aspect ratio features, is deep reactive ion etching (DRIE). The process is an extension of reactive ion etching (RIE) which combines the etching capabilities of plasmas with the directionality of ion bombardment to anisotropically dry etch a material. Reactive ion etching only allows for moderately high aspect ratios and is limited by etch rate and the inability of current mask technology to protect trench and other high aspect ratio features' sidewalls. The breakthrough for transition from RIE to DRIE came with the development of new and improved plasma sources which allowed for high aspect ratio structures and higher etch rates. One of these sources is inductively

couple plasmas, which "create high-density, low pressure, low-energy plasmas by coupling ion-production electrons to the magnetic field arising from the RF voltage,"[19] supplied by a power source. This technique has produced etch rates in silicon which are six times faster than comparable RIE etch rates. Deep reactive ion etching has also been found to produce aspect ratios on the order of 30:1 with feature sizes as small as 1 micron. One drawback to DRIE is that as the etching process proceeds, the sidewalls of the trench (or other high aspect ratio feature) must be continually passivated to avoid sidewall roughening. To alleviate this problem, time multiplexed deep etching (TMDE) has been developed, which uses one of two approaches to reduce sidewall etching. There are generally two separate gaseous species used in this process, the first is an etchant (often SF_6), and the second is passivating (typically C_4F_8). One can either mix these two gases and proceed with DRIE, or else one can cycle the gases consecutively for greater control. The latter approach is most often used because of the many parameters, such as cycle time, gas flow rate, etc, which can be controlled. Figure 4.10 details the idea behind alternating between etch and passivation cycles.

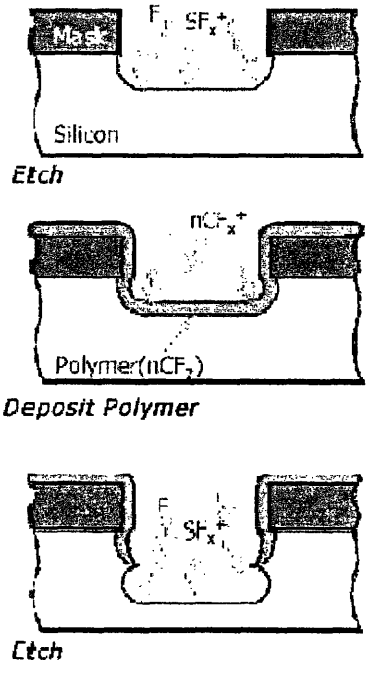


Figure 4.10: Alternating etch and passivation cycles to protect sidewalls.[53]

As shown in the figure, the polymer is deposited on all surfaces, but since the etchant is directed vertically downward, the polymer material at the bottom of the trench will etch quicker than what is deposited on the sidewalls. Therefore, one can continue to etch through the substrate until again the newly developed sidewalls must be passivated. Controlling the cycle time is of critical importance to ensure sidewalls with as low a surface roughness as possible. Figure 4.11 shows a relative flow rate cycle change and the accompanying sample cross-sectional view resulting from each cycle.

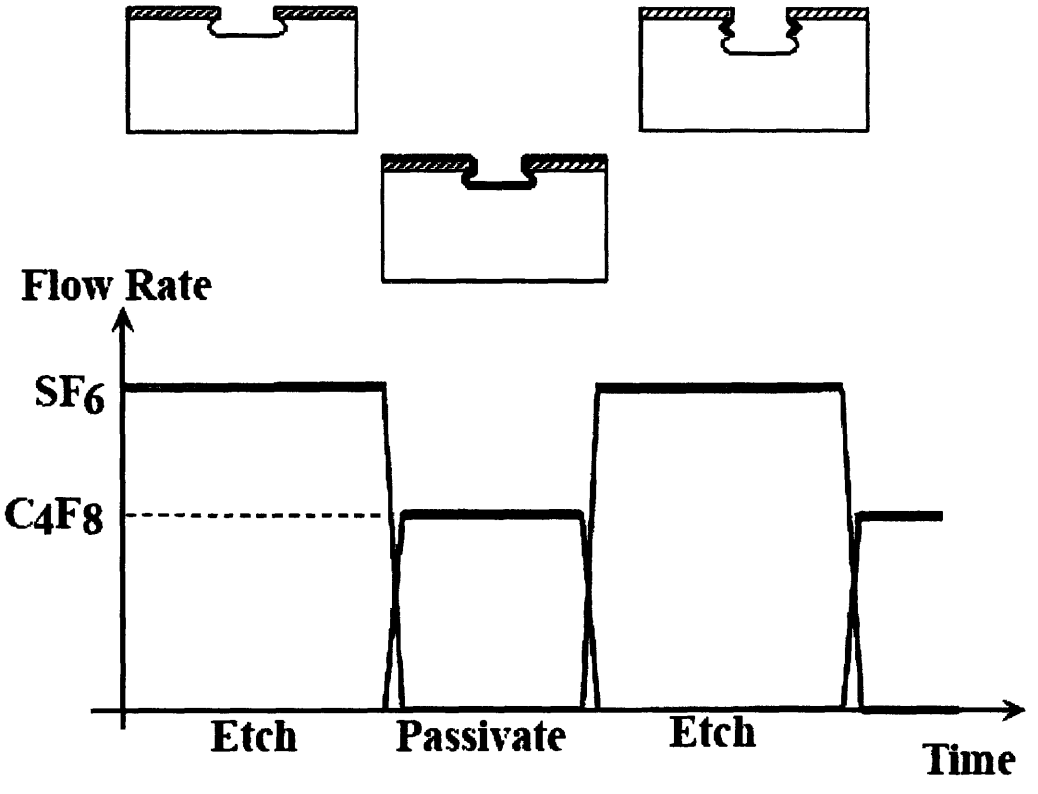


Figure 4.11: Typical time multiplexing gas flow scheme for DRIE.[52]

Note the overlap of gas flow in the figure. This is another critical parameter to the proper fabrication of vertical sidewalls, as it allows for decreased process time. Figures 4.12-13 shows a scanning electron micrograph of the silicon sidewall of a trench

processed by DRIE. Note the extremely fine sidewall roughness relative to trench depth and thickness.

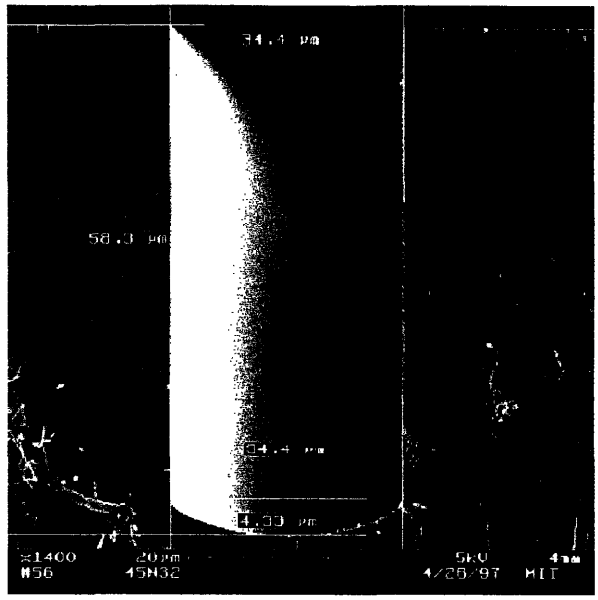


Figure 4.12: Trench in silicon fabricated by DRIE.[52]

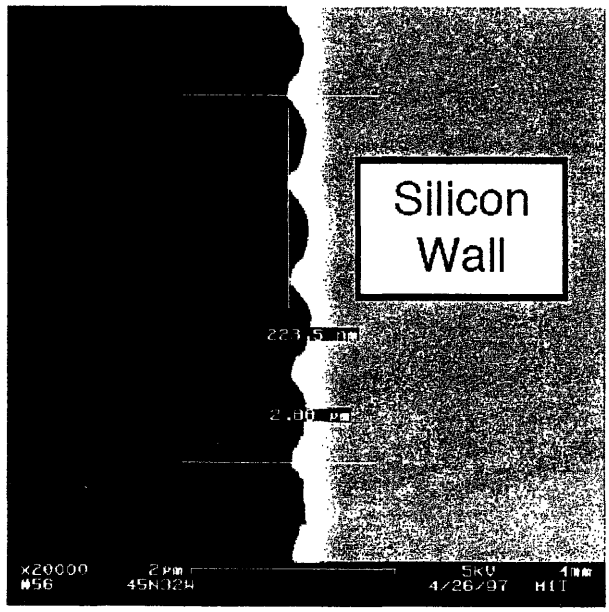


Figure 4.13: Sidewall of trench fabricated by DRIE.[52]

Some of the drawbacks of DRIE include the lack of a suitable etch stop. Typically, the process must be time-controlled for a desired trench depth. Additionally, DRIE is less selective than wet etches and the process may be too time intensive for commercial applications. Finally, the cost of DRIE equipment and plasma sources is very high.

The landscape of competing technologies for nanofabrication of high aspect ratio features is quite crowded. All of the technologies discussed herein have advantages and disadvantages of their own accord, but when compared with PATT for certain applications, the competing technologies fall short. Specifically what PATT offers is high aspect ratio pores, ordered over the entire surface of an alumina template. It has been shown that PATT can quite easily allow for nanostructure growth (dots, wires, tubes), and the templates are not limited by the time constraints that many of the preceding processes are. Additional unique properties and advantages of PATT is that the template is made of a ceramic oxide, which is very stable, both thermally and chemically. Alumina also has a tunable dielectric constant, it is electrically insulating, and mechanically rigid, lending itself to IC integration applications. Aspect ratios on the order of 50:1 at 30 nm dimensions have been demonstrated at MIT without physical limit. Still larger aspect ratios can be similarly demonstrated. Because PATT is not a serial process, like many competing technologies, it does not suffer large-scale manufacturing impracticalities. Pore diameters as small as 20 nm have been demonstrated at MIT, as have spacings of 90 nm: both of which are unattainable by conventional photolithography. Finally, PATT can have a variety of substrates. Aside from silicon and other electronic materials such as gallium arsenide, porous alumina templates on plastic substrates would allow for flexible applications like flexible displays.

Applications that would benefit exclusively from PATT over these competing technologies are discussed in Chapter 5. The table presented in the Appendix gives a summary of all of the previously discussed competing technologies as well as their advantages and disadvantages.

5.0 PATT Applications

Porous alumina template technology is only as useful as its applications prove to be. That is why there is a large push in both experimental study and intellectual property to discover and claim as many potential uses of PATT as possible. As was described earlier, the intellectual property of PATT developments to this point are organized into three major clusters: technology and process patents, PATT-based nanostructure fabrication patents, and PATT-based device patents. The vast majority of IP on the subject deals with technology and process patents relating to porous alumina. As progress continues in studying PATT, it is clear that technical developments will migrate more heavily towards nanostructure fabrication using PATT and device applications. It is to the latter end that this chapter focuses. While much of the future of PATT and its impact on nanotechnology is ambiguous at best, it is a worthwhile exercise nonetheless to consider the potential applications this technology currently holds and may hold in the future.

To understand how PATT would be useful to a certain product or industry or how it would replace a current technology, it is necessary to understand and identify the properties of the technology which make it unique. Combining any number of the properties discussed previously, including alumina's stable materials properties, long range order, and high aspect ratio, would promote PATT as a unique technology for applications which seek such attributes.

The variety of nanostructures that can be grown on the templates allows for a myriad of devices to be fabricated. There has not been as much work in this area as there has been in the growth of nanoporous templates and nanostructures. This is predominantly due to the bottom-up approach of the technology, where the template is fabricated, followed by nanostructure development, followed by device fabrication. The top level is the most complex, but perhaps the most interesting.

There have been many ideas for nanodevices using templates cited in the literature, including Peltier cooling devices, gas sensors, random-access memory devices, field-emission-based components[2]. These devices share many of the same features,

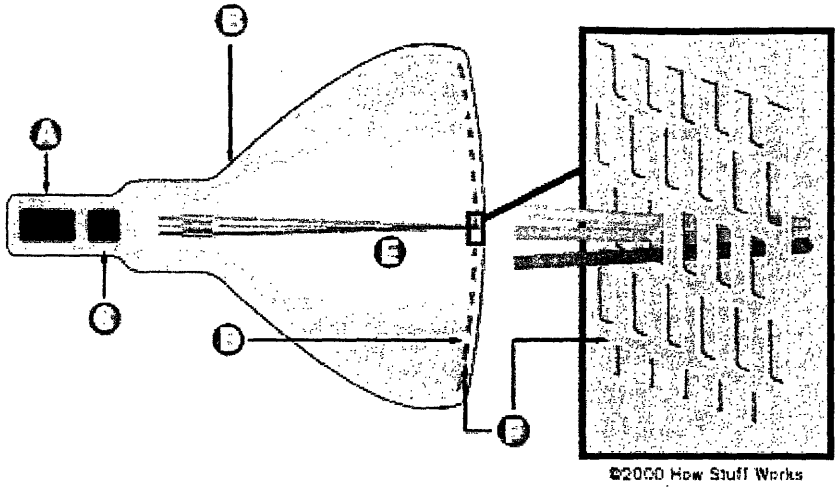


Figure 5.1: Cartoon of standard cathode ray tube in a television.[45]

In the diagram, A is the cathode, B is a conductive coating lining the televisions inside, C is the anode, D is a phosphor-coated screen, E is the electron beam, and F is a shadow mask. The cathode is a heated filament that emits electrons under vacuum. These electrons are focused into a beam by the anode and accelerated towards the phosphor-coated screen. The shadow mask helps to separate individual pieces of light which have been irradiated from the phosphors by the electron beam. The conductive coating along the inside of the television collects the electrons and prevents electrostatic buildup. In color televisions, there are three electron beams, one for red, green, and blue, and these beams are rastered across the screen based on an incoming television signal. Copper windings create the magnetic fields which control the horizontal and vertical positions of the electron beams. Figure 5.2 shows the inside of a television where these copper windings are evident.

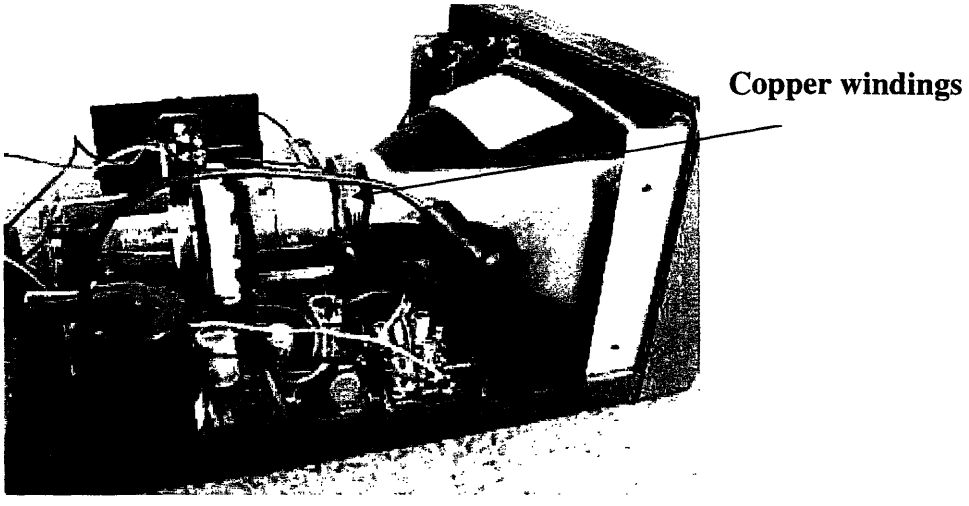


Figure 5.2: View of the inside of a television.[45]

The primary drawback to CRTs is their bulkiness. Because electrons must be generated, focused, and shipped to a screen, CRTs have longer depth dimensions than they do diagonal screen dimensions. They are also extremely heavy, especially when screen sizes are large. Additionally, CRTs draw a lot of power to generate their electron beams, and much of it is wasted off as heat.

Flat panel displays have recently become popular because of their high quality resolution and incredibly small depth dimension. They also draw much less power than do CRTs. Of all the flat panel technologies, liquid crystal displays are currently the most widely used, and are quite different from CRTs. Figure 5.3 shows how they work.

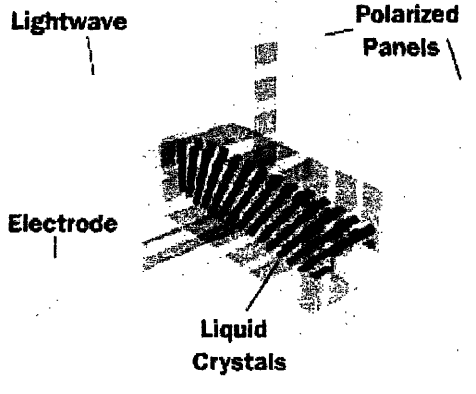


Figure 5.3: Liquid crystal controlling light.[46]

including nanostructure growth and electrical connection with other pores or CMOS components integrated into a silicon substrate.

Of greatest interest may turn out to be field-emission-based device applications. Carbon nanotubes are intrinsically difficult to process and integrate into devices because they are not structurally supported or insulated from other tubes. Mechanically rigid insulating templates allow for structural support and electrical insulation, while promoting unidirectional nanotube growth. This property of porous alumina templates could serve to "aim" the electron emission of nanotubes at a screen to create a field emission display (FED), which may allow for an attractive inlet into FED markets (tiny displays, for example) as a sustaining technology.

While FEDs are still generally considered to be several years away from widespread commercial use, their eventual inclusion in the display market would cause a great bit of competition among current display technologies, which include cathode-ray tubes (CRTs) and liquid crystal displays (LCDs).

To fully understand the potential that lies in FEDs, it is of value to note the current and future needs of display devices. Cathode ray tubes are still the overwhelming favorite of most consumers when they face a decision to buy a new computer monitor or television. The most critical criterion for the average customer is price, and CRTs have been nearly commoditized, with average 27" television sets costing in the neighborhood of $150. This price target simply cannot be met by current generation FEDs.

The technology behind CRTs is somewhat similar to what was later developed for FEDs, and is described pictorially as a television in Figure 5.1.

Instead of electrons radiating phosphors to produce visible light, a liquid crystal is controlled by an electric current to allow or disallow visible light to pass through. Under an electric field, a liquid crystal can twist or untwist, and can be aligned parallel or perpendicular to a polarizing glass. When parallel, light passes through, and when perpendicular the light is blocked. A liquid crystal display consists of a light source, several polarizers, filters, and other optics. All of this equipment reduces brightness and luminous efficiency. Additionally, the viewing angle of a LCD is quite small, meaning that one must be looking almost perfectly perpendicular to the display screen in order to view images properly. Liquid crystals exist in very narrow temperature ranges, and therefore LCDs can malfunction when temperatures increase or decrease. This limits LCD use in overly cold or hot environments. Finally, LCDs currently cost much more than comparable CRTs in many display devices because of the commoditization of most CRT applications, most notably televisions and computer monitors.

Liquid crystal displays are used in a large variety of products. They are very thin and because they work by allowing or blocking light, they are very useful to simple devices such as watches and alarm clocks which only require the display of basic shapes and patterns.

While CRTs and LCDs have demonstrated functionality in past and current applications, the future of display technologies may lie in field emission. Field emission displays have many of the benefits of CRTs and LCDs without the same drawbacks. In much the same way as CRTs, FED technology consists of the acceleration of electrons through a vacuum, striking a phosphor-coated screen to produce light. However, the main difference between FEDs and CRTs is the way in which electrons are generated. Whereas CRTs rely on thermally generated currents, FEDs utilize field emission. Figure 5.4 shows part of a FED schematically.

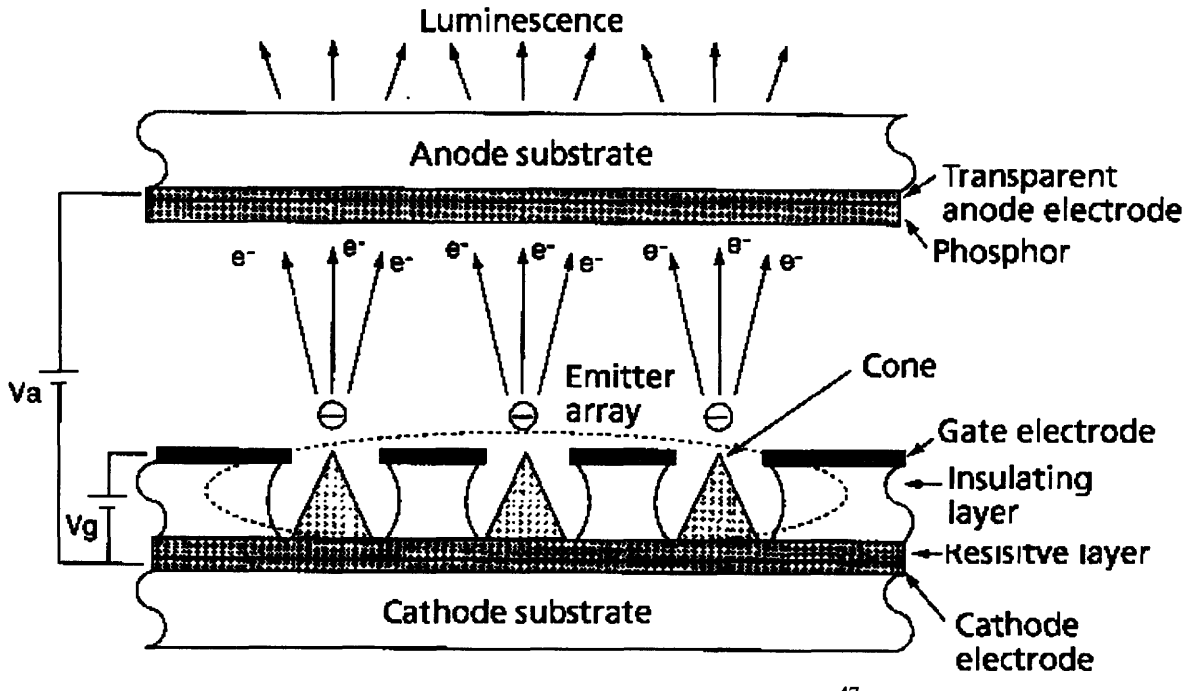


Figure 5.4: Inside a field emission display.[47]

A cathodic substrate serves as ground while a voltage is applied at the tip of the cone emitters, for electron emission, and at the anode, for electron acceleration. Extremely high electric fields are required for electrons to tunnel out of the cones and accelerate towards the phosphor-coated screen. In order to generate these high electric fields at safe low voltages, cones with extremely narrow tip diameters are used. One of the leading drawbacks to current FED technologies is the high voltages that are required for sufficient emission. Lithographic and other processing constraints have limited the allowable tip diameters, requiring very high voltages be used in order to emit electrons. These high voltages translate to high power consumption and low power efficiency. This type of materials drawback has long been one of the major reasons attributed to FEDs failure in overcoming CRTs and LCDs as the dominant display technology.

Recent developments have begun to find alternatives to lithographically patterned or machined tips which would allow field emission at much lower voltage. Specifically, the use of carbon nanotubes (CNTs) have been shown to be very good electron emitters at low voltages because of their tip diameters on the order of nanometers. It is here where PATT may serve to better FED technology. Carbon nanotubes can be grown in

the pores of ordered porous alumina to create an array of ordered nanotubes supported by the walls of the pores. These CNTs will all be naturally facing the same direction, and can be addressed to form pixels. While color televisions may have three electron beams, FEDs have thousands of electron emitters *per pixel*.[46] These extra emitters serve to increase current density as well as act as redundancies for the device in instances when an emitter fails. Aside from the requirement that all CNTs be supported and facing the same direction, another important constraint for FEDs is a high aspect ratio for the electron emitters. As shown in Figure 5.4, electrons are emitted from the tips at a small range of angles. If the tips are too close in proximity to the grounded substrate, some will be directed to ground instead of the phosphor-coated screen, resulting in a loss of power and brightness. Additionally, the tips need to limit the amount of electrons that are sent at large angles which may interfere with adjacent pixels. This can cause two pixels to light up when only one is addressed. Porous alumina template technology may provide a solution to these issues. The aspect ratio of porous alumina can be controlled, allowing high aspect ratio pores to be fabricated, which in turn allow for CNTs to grow and remain supported up to a desired height. This would prevent electrons from circling around from the CNT tips through vacuum and returning to ground. Another approach would be to stop CNT growth before it reaches the top of the pores so that electrons which are not emitted vertically out of the pores would reach the phosphor-coated screen, but instead would hit the pore walls. A high aspect ratio also allows for a lower voltage requirement at the anode to attract the electrons because the driving force for them to return to ground has been reduced.

While PATT seems like a good fit to FED development, it remains to be seen whether or not long range order in PATT, that which sets the MIT group's work apart from others', is of any benefit. One possible benefit which has yet to be researched for long range order is that it may make addressing individual pixels easier. While it would certain allow addressing individual *pores* much easier than non-ordered PATT, it may also do the same for actual pixels. This may serve to be important for very large scale FEDs, though no work has yet been done on it to prove this is the case.

A second and potentially even more useful application where ordered PATT may be of value is in parallel electron beam lithography (PEBL). As discussed in Chapter 4,

electron beam lithography allows for very good resolution and small feature sizes. However, its primary drawback is that the process is serial, taking far too much time to complete than is worthwhile for industrial use. Aside from mask making, there are few direct applications to EBL. However, combining the long range ordering of PATT with the power of EBL may solve this issue. If the pores were fitted with electron emitters, such as CNTs, they could be used to generate the same circuit pattern many times at once. While a nanotube may not have the same writing capabilities of an electron gun, growing multiple tubes into a pore or else using several adjacent pores (if spacing is very small) to write a feature could allow for parallel processing of small features. Parallel electron beam lithography would require that the pores be individually addressed, which is a unique capability to ordered porous alumina templates. A silicon substrate could also be fitted with microelectronics features to control word and bit line addressing so that off-device circuitry could be minimized.

Potential PEBL equipment might be very similar to EBL equipment, aside from the addition of an ordered porous alumina template filled with CNTs, and a movable sample stage. The idea could be extended further to allow parallel processing of features on a chip, or chips on a wafer, or with a large enough template, the parallel processing of features on a chips on different wafers. While the latter application may be years away from fruition, the parallel patterning of features on a chip is certainly within the realm of possibility. If the porous alumina template is grown on silicon, this would allow for CMOS pore-addressing circuitry to be integrated into the template. All of the electron emission and electronic components could feasibly be built on one template, with the only other requirements being mechanical equipment to interface with a sample to be patterned.

Another application of ordered PATT which takes advantage of the unique properties of the technology is the use of a porous alumina templates as a mask for DRIE applications. Combining very small, ordered pores in a chemically and thermally stable mask could allow for DRIE processes on silicon, gallium arsenide, or other semiconductor materials. Unlike many DRIE mask materials which wear down in the presence of etching gases, alumina may be more capable to handle rough processing

conditions. Development of high aspect ratio trenches with low wall-to-wall dimensions is a specific application of PATT combined with DRIE usefulness.

There truly are a myriad of potential applications for PATT. Porous alumina templates can be used in sensors, FEDs, as previously described, CMOS circuitry, and even for simply fabricating and separating nanoparticles and structures. Applications where the unique properties of ordered PATT are utilized offer the greatest potential for marketability. There does seem to be great promise in PEBL systems. By combining the feature size advantages of EBL and the speed of parallel processing in manufacturing, this application has significant promise. Ordered porous alumina templates have many unique capabilities, and the potential benefits of their continued development are worth the time and effort invested in seeking new breakthroughs.

6.0 Business Plan

In discussing the marketability of various template nanotechnology applications in order to form a business strategy, it is important to concentrate on whether an application has the capability of being a sustaining of disruptive force in a given market.

Figure 6.1 shows a graph of the technological barriers versus perceived value of a technology as a function of time. The progression and current state of PATT, and even its personification as a microcosm of nanotechnology in general, is noted on the figure.

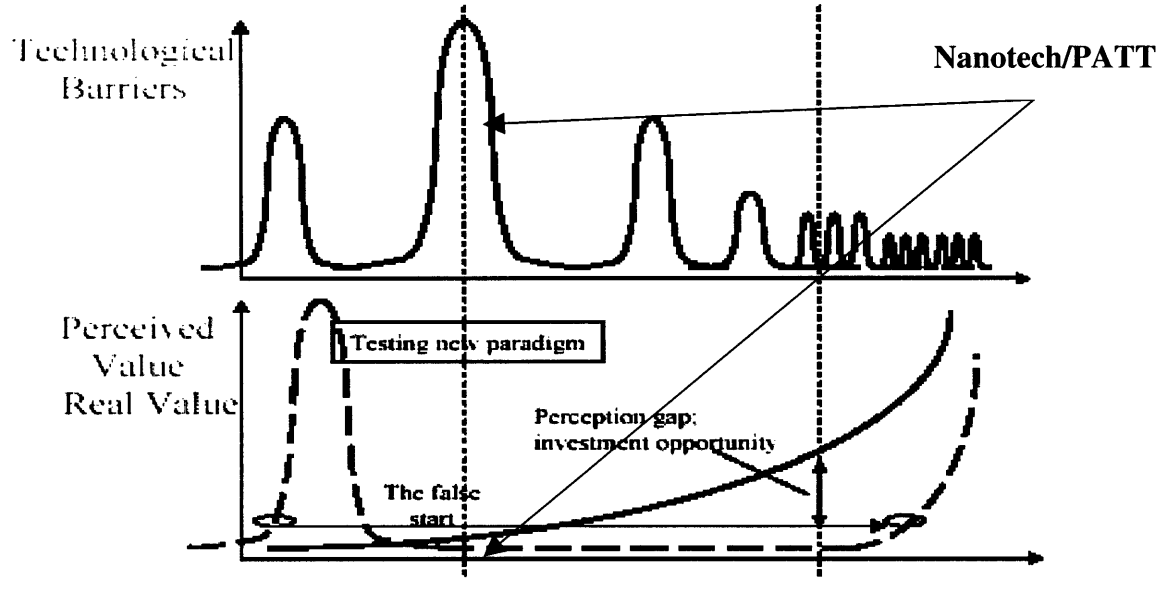


Figure 6.1: Technological barriers and value of a new technology over time.[48]

The initial buzz for PATT has passed and there has yet to be enough large breakthroughs in research to allow for the profitability of much of what the technology is capable of right now.. The same can be said for nanotechnology in general. Microtechnology still rules most applications, and the only talk of nanoscience and technology is focused on the future. That is, based on what our needs (computing, or otherwise) are today, and where they've been in recent years, scientists and business officials are predicting what our needs may be tomorrow. It is a very difficult task,

indeed. Noting physical limits on feature sizes due to photolithography, scientists are studying many of the competing technologies noted in this document. Business officials are constantly evaluating potential technologies based on their uniqueness and application potential to current or future products. There must be clear evidence, both scientifically and economically, that a technology is capable of success in a given market for it to truly have potential. As fabricated by the MIT group, PATT has many unique features, among which are long range order, high aspect ratios, and nanometer-scale feature details approaching the furthest possibilities of current photolithography. According to Figure 6.1, the current state of development is mired in solving large challenges. While there are many ideas for applications of PATT, more experimental work is required to prove that these applications are feasible. Porous alumina template technology has come a long way, but still requires persistence.

Among the applications that have been mentioned in this document, there are many that fit the category of a sustaining technology. What marks a product as sustaining is its inability to compete against low-end or non-consumption. The competition is either non-existent or very sparse in low end markets and non-consumption. Many large companies are happy to rid themselves of low-end market products because their average bottom line increases, with a higher percentage of revenues coming from large-market, premium profit products. As Christensen points out in his book The Innovator's Dilemma, it is very difficult for entrant firms to become successful by way of introducing sustaining technologies. The advantage of firms in the industry does not allow entrant firms to succeed[1]. If the goal of a new product is simply to improve upon a current product, the leading companies in the industry are typically leaders in presenting new technologies and products.

Disruptive technologies, on the other hand, are geared toward entrant firms because they usually aren't simply the next obvious technological leap in the path of increased performance, but instead offer value in other attributes not previously addressed by the existing technologies of dominant firms. The innovation must also compete against high-end market products where the competition is fierce because existing corporations in the markets will do everything they can to protect their most attractive profits and customers from new firms

Christensen gives the example of the laptop, which took a large share of PC sales when it entered the market. It was not designed necessarily to be a better PC with a faster processor, for example. Instead, it became a more convenient alternative to the PC. Whether the initial inventors had destined the marketing of the laptop for convenience instead of PC characteristics is unknown, but the effect is obvious: laptops have intruded and now occupy a large portion of the current computing market because they offered something completely different than PCs: comportability. The business lesson from this analysis is that it would be unwise to start a company centered on sustaining technology.

Specific examples of sustaining porous alumina template technologies include nanoelectronic devices, DRIE, and FEDs. All three of these innovations simply improve upon similar current technology. Additionally, these techniques would have their main competition stratified in high-end markets. Field emission displays, for example would be competing against other flat panel display technologies, including plasma screens and LCDs. These high-value products bring large profits and the markets in which they reside would be difficult to enter as a new company and to survive long term.

There are alternatives to starting a new company for sustaining technologies developed outside of existing companies, which are already entrenched in premium markets. Two specific business ideas exist, which can be pursued in this instance: licensing and consulting. Developing critical technologies that could be of benefit to larger companies may make the legal rights to its use valuable. Through research and intellectual property, one can make a profit on licensing technologies to large companies. Additionally, one can consult other companies who work on the same technology or have bought the rights to a given technology. Therefore, while the development of sustaining technologies is worthwhile, the marketing of a line of products seems a difficult task for a new company. The MIT group would be wise to actively patent and license their IP on sustaining technologies, as well as to consult as many companies as possible who may be interested in similar technologies. This would allow larger companies to use these PATT applications for their and the MIT group's collective benefit. The important result of licensing is that it would constitute a consistent in-flow of capital.

Most important to licensing, however, is the use of patents. A company described above would have to strive to consolidate intellectual property quickly. Parallel electron

beam lithography and certain FED devices may have IP potential, but to fully realize a business plan, a group must own the rights to the technologies they have developed. Once patents have been achieved, then the plan can be implemented.

While many porous alumina template technologies are sustaining, there are a couple that have disruptive qualities. What marks a disruptive technology different from a sustaining one is its ability to compete against non-consumption or low-end markets, where competition is less fierce and winning market share is less of an uphill battle. In high-end markets, where profits are large, corporate competitors will feel threatened and will fight an entrant firm to protect their market share. Two porous alumina template technologies which may prove to be disruptive are gas sensors and PEBL. Since the attacks of 9/11, increased national security and terrorism allegations have created a new market for gas sensors. There are many government agencies and corporate entities that may benefit from certain sensor applications, such as a device which can detect sarin nerve gas or other poisonous gases from close or long range. Therefore, many new customers may demand sensing applications, presenting a market opportunity for entrant firms who fabricate sensor technologies. In the case of gas sensor pursuits, therefore, the proper business strategy is to start a small company whose goal is the development, marketing, and sales of gas sensor technologies. The company would have to target non-consumers convincing them that gas sensors could be beneficial, and that the ones developed in-house are superior to others because of the unique technological capabilities allowed by PATT.

Another potentially disruptive application is PEBL. While the technology may be in some ways similar to other techniques, it could very easily target non-consumption markets, including research institutions who cannot afford the cost of current photolithography systems. Because the competitor is non-consumption, the customers would not be seeking highly developed systems. So it would not take long for a start-up company to develop, market and sell PEBL systems (assuming technology development goes smoothly). There are many small electrical engineering departments, for example, who perhaps can't afford EBL or IBL systems to fabricate small feature size components. Targeting these customers is key to a successful start-up company. Competing against

non-consumption is much easier to accomplish than competing against territorial corporations who would fight to protect high margin markets and customers.

7.0 Conclusions

Nanotechnology is in the process of replacing microtechnology in many fields, most notably electronics. There are already examples of the market appeal of nanotechnology from Hewlett Packard commercials to cutting edge scientific reports on the topic. The form that nanotechnology takes in the future, however, is undecided. It may be in the form of nanotechnological advances on silicon by extending lithographic techniques beyond their current limits to fabricated feature on the order of tens of nanometers. It may also be a future that benefits from the many intriguing properties of porous alumina templates. It may be some other nanoscience reality current under development. It will probably be a combination of many nanotechnologies, just as microtechnology is not limited to electronics, but exists in everything from MEMS to biological systems.

Porous alumina templates technology is a promising route to nanotechnology with many intriguing applications. Specifically, it serves as a vehicle for nanostructure growth and device fabrication. While much of the prior art has focused on physically fabricating templates, there is still room for significant intellectual property claims on various template processing and device application ideas. It is imperative that as technological developments evolve, IP is claimed to protect future business plans, whether they be geared towards sustaining or disruptive technologies. Because of the vast number of potential applications for PATT, securing the most fundamental pieces of IP is critical. However, any intellectual property that can be claimed at any technological level should be done so in earnest.

As in all technical pursuits, there are many competing forces to PATT. Certain technologies seek to accomplish similar aims, such as DRIE's high aspect ratio capability and EBL's small feature size capability. While all of these technologies have promise, they all have their own drawbacks as well, including cost, processing speed, and minimum feature size. Many interesting applications have been discussed which would uniquely benefit from PATT over other competing technologies due to one or a combination of many of PATT's attractive properties. Such properties are numerous and diverse. They include the ability to produce high aspect ratio pores, ordered over a 300

mm silicon wafer, allowing seamless integration with other silicon-based technologies. Porous alumina templates can also serve as a scaffold for the growth of many nanostructure arrays, such as dots, wires, and tubes. Other advantages of PATT include the stable material properties of alumina (thermal, electrical, etc.); nanometer-scaled and independently controlled pore diameters and spacings; and the ability to fabricate porous alumina templates on flexible polymer substrates. These attributes result in a technology that may be a unique fit to many applications, such as gas sensors, nanoelectronics, deep reactive ion etch masking, parallel electron beam lithography, and others.

Porous alumina template technology appears to have much potential. With continued dedication to scientific research, intellectual property claims, application identification, and business modeling, PATT could become a breakthrough and financially sustaining pursuit.

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Appendix

Technology	Advantages	Disadvantages
Feature/AR Limits		
Photolithography	cheap; widespread; well researched	DOF and resolution compete; limited by λ of light
70 nm		
SU-8	sensitive to near-UV light; low optical absorption	difficult to strip; limited by λ of light; moderate aspect ratios
14:1 at 300 nm		
X-ray/LIGA	very low λ (1 nm); doesn't require vacuum or optics	mask making very costly; synchrotron required;
100:1 at 1 μm		
10:1 at 30 nm		
EBL	extremely small feature sizes; no masks required	electron scattering limits resolution; requires vacuum; serially scanned
60 nm		
SPL	smaller beam spot than EBL	requires larger dose of electrons than EBL
60 nm		
IBL	excellent resolution	serially scanned; requires vacuum
60 nm		
DPL	allows greatest molecular control	extremely time-intensive; humidity-dependent process
45 nm		
S/A Liquid Scaffold	can create 3-D structures	very nascent, not widely studied; may not allow very high aspect ratios
S/A Nano Bending	ease of fabrication; allows 3-D shapes	no direct correlation to high aspect ratio structures
DRIE	good aspect ratio; off-shoot of heavily used RIE	requires constant sidewall passivation; no natural etch stop; high investment cost
30:1 at 1 μm		
PATT	ease of fabrication; allows long range repeatable ordering;	no natural etch stop for substrate-less approach; long range order
> 50:1 at 30 nm	template allows many functionalities: dots, rods, wires, tubes; substrate-less approach allows very high aspect ratios; alumina electrically, thermally, structurally stable, substrate-based approach allows CMOS integration	not required in many applications; nascent technology