Post-Assembly Process Development for Monolithic OptoPill Integration on Silicon CMOS

by

Yi-Shu Vivian Lei

BASc Electrical Engineering
University of Waterloo, 2002

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Master of Science in Electrical Engineering
at the
Massachusetts Institute of Technology

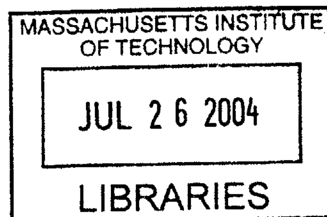
May 2004

Copyright © 2004 Massachusetts Institute of Technology.
All rights reserved.

Signature of Author________________
Department of Electrical Engineering and Computer Science
May 25, 2004

Certified by________________
Clifton G. Fonstad, Jr.
Professor of Electrical Engineering
Thesis Supervisor

Accepted by________________
Arthur C. Smith
Chairman, Department Committee on Graduate Theses
Department of Electrical Engineering and Computer Science


MASSACHUSETTS INSTITUTE OF TECHNOLOGY
JUL 26 2004
LIBRARIES

BARKER

Post-Assembly Process Development for Monolithic OptoPill Integration on Silicon CMOS

by

Yi-Shu Vivian Lei

Submitted to the Department of Electrical Engineering and Computer Science on May 25, 2004 in partial fulfillment of the requirements for the degree of Master of Science

Abstract

Monolithic OptoPill integration by means of recess mounting is a heterogeneous technique employed to integrate III-V photonic devices on silicon CMOS circuits. The goal is to create an effective fabrication process that enables the volume production of high performance optoelectronic integrated circuits (OEICs). This thesis focuses on the development of post-assembly processes and technologies, in which InGaAs/InP P-i-N photodiodes were integrated as long wavelength photodetectors with an optical clock receiver circuit. Fabrication procedures, challenges experienced, and results accomplished are presented for each process step including the formation of alloyed and non-alloyed ohmic contacts on n-type and p-type InGaAs contact layers, active area definition by dry-etching InGaAs/InP with ECR-enhanced RIE, BCB passivation and planarization, via opening by dry-etching BCB with RIE, and top contact metallization.

In conjunction, an InP-based test heterostructure was fabricated into discrete photodiodes. Decoupling the fabrication and benchmarking of III-V photonic device from the Si-CMOS electronic circuit allowed for the independent electrical and optical characterization of the photodetectors. Measurements and analysis of the P-i-N photodiodes will assist the forthcoming analysis of the final OEIC. Preliminary results and discussions of the calibration sample are presented in this thesis.

Thesis Supervisor: Clifton G. Fonstad, Jr.
Title: Professor of Electrical Engineering

Acknowledgements

"Be anxious for nothing, but in everything by prayer and supplication with thanksgiving let your requests be made known to God." Phil 4:6

First, I would like to acknowledge my grandfather, who has invested his faith in my abilities from the very beginning. Without my realizing it, he silently instilled hopes of greatness in me. Even today I am firmly guided by his beliefs and motivated by his encouragements. I look forward to meeting him again someday, and hearing him say how I have always made him proud.

I would like to thank my parents, Yuan Ho and Vei-Chyau Lei, for their boundless love and unwavering support throughout the past twenty four years of my life. They have both sacrificed many of life's simple pleasures and endured much hardship, only to craft for me a thriving world with a better tomorrow.

Then there are my friends, who are indeed God's unfailing way of taking care of me. Roo-Roo, Sheep, Chris/sy, Homogenous, Nati, Snoda, Mushroom, Tubby, Dough, Bubbs, Tdoggy, Yanfeng, Alex, BabySteps, Steveo, NuttyB and Mizhi all have helped to make the past two years the very best part of my life. If I had the luxury to describe in detail just how each of them has touched my heart, this acknowledgement would be substantially longer than the thesis itself. I would also like to send my thanks northbound to Remona, Michael, Harry, Bpko, Chris, Vincent, Ji-Yun, Brandon and Christine, for always having believed in me. They have been the truest of friends who have helped me become a person greater than I would have ever supposed; for that I will always be grateful.

A dream is just a dream, but "a goal is a dream with a deadline" - Napoleon Hill. On my path to achieving goals, I have been indebted with the kindness of many people, who have offered much of their knowledge, time and assistance. Along the way Kurt Broderick played a key role in my learning experience with semiconductor fabrications. He went above and beyond to help and brainstorm problems as if they were his own. It is through his unreserved enthusiasm and delightful attitude that I have learned much more than the mere techniques associated with research. The care and support from Marilyn Pierce were of

great emotional importance to me. I would like to thank her for being both a patient listener and a compassionate friend. I would also like to thank Professor Reif and Professor Chandrakasan for their counsel, understanding, and support during the first part of my time at MIT.

My research would not have begun as smoothly as it did without the help from my colleagues. Henry was the first one in the group with whom I became comfortable asking for help. Even at the oddest hours, he would assist me tirelessly with any questions or problems that I had. Not a staff trainer or even an obligated group member, Kostas always volunteered his time and oriented me around TRL when I first got my feet wet in processing wonderland. I would also like to express my sincere gratitude to my research partners, Eralp and Mindy, for their valuable teachings and collaborative efforts on this project; Wojtek, for his continuous help on lab equipments, from the RTA to the thermal evaporator, from the curve tracer to the probe station; to the two musketeers, James and Joe, for transforming EML into a place of jokes, laughter, humming tunes, and crossword puzzles; and finally, to Sheila, Ed and Mike for completing the awesome Fonstad group.

Last but not least, I would like to express my deep appreciation to Professor Fonstad. I am extremely grateful for having been granted the opportunity to learn as much as I did; his keen observations and profound insights, his unprejudiced openness and genuine sincerity, have all been the cornerstones of my gratifying SM experience.

On behalf of this project, I would like to acknowledge the continuing collaboration with Professor Boning and his students at MIT. This project has been funded by MARCO Interconnect Focus Center.

TABLE OF CONTENTS

Table of Contents 5

List of Figures 8

List of Tables 10

1 Introduction 11

1.1 Motivations for Optical Interconnects 11
1.2 Optoelectronic Integrated Circuits in Optical Interconnects 13
1.3 Heterogeneous Integration over Homogenous Integration 14
1.4 Hybrid Integration and Monolithic Integration 16
1.5 Recess Mounting by Monolithic Metallization 17
1.5.1 Epitaxy-on-Electronics 18
1.5.2 Aligned Pillar Bonding 20
1.5.3 OptoPill Assembly 22
1.6 Thesis Organization 23

2 OptoPill Assembly Integration 25

2.1 The Si-CMOS Optical Clock Receiver Circuit 25
2.2 The III-V Photodetectors 28
2.3 OptoPill Assembly Integration Process 32
2.3.1 Fabrication of OptoPills 32
2.3.2 Pick-and-Placement 34
2.3.3 Solder Bonding 35
2.3.4 Post-Assembly Processing 36

3 Post-Assembly Process Development 37

3.1 Post-Assembly Process Flow 37
3.2 Ohmic Contacts on InGaAs Layer 40
3.2.1 Fundamentals 40
3.2.2 Experimental 40
3.2.3 Transfer Length Method 43
3.2.4 OptoPill Photodiodes and Discrete Photodiodes 51
3.2.5 Non-Alloyed (Ti/Au) Ohmic Contacts on n-InGaAs 53
3.3 Active Area Definition by InGaAs/InP Etch with ECR-Enhanced RIE 55

3.3.1 Experimental 55
3.3.2 Results and Discussion 57
3.4 BCB Passivation and Planarization 61
3.4.1 Experimental 62
3.4.2 Results and Discussion 63
3.5 Via Opening by BCB Etch with RIE 64
3.6 Ti/Au Top Metallization 65
4 Discrete InP-Based P-i-N Photodiodes 66
4.1 Fundamentals 66
4.2 Fabrication Process Flow 69
4.3 Alloyed (AuZn) Ohmic Contacts on p-InGaAs 71
4.3.1 Experimental 72
4.3.2 Results and Discussion 73
4.4 Mesa Isolation by InGaAs/InP Etch with ECR-Enhanced RIE 75
4.4.1 Experimental 75
4.4.2 Results and Discussion 77
4.5 BCB Passivation and Planarization 78
4.5.1 Experimental 78
4.5.2 Results and Discussion 78
4.6 Via Opening by BCB Etch with RIE 80
4.6.1 Experimental 80
4.6.2 Results and Discussion 81
4.7 Ti/Au Top Metallization 82
4.7.1 Experimental 82
4.7.2 Results and Discussion 82
4.8 Final P-i-N Photodiode Structure 83
4.9 Pre-Passivation Characterization of Discrete P-I-N Photodiodes 84
5 Conclusions 88
5.1 Ohmic Formation 88
5.2 Active Area Definition 89
5.3 Planarization and Passivation 89
5.4 Via Opening 89

5.5 Top Metallization 90
5.6 Future Directions 90

Appendix A: Facilities and Procedures 91

Appendix B: Process Recipes 96

Appendix C: Transfer Length Method Data 102

Appendix D: Dry-Etch BCB Processing Procedures 104

Appendix E: Tencor P10 Profilometer Recipe 105

Appendix F: Silicon Photodiode Characterization 106

Bibliography 108

LIST OF FIGURES

Figure 1 Recess Mounting by Monolithic Metallization 18
Figure 2 Illustration of the Epitaxy-on-Electronics Integration Process.............................. 19
Figure 3 Illustration of the Aligned Pillar Bonding Integration Process 21
Figure 4 Illustration of the OptoPill Assembly Integration Process 22
Figure 5 Layout of the Variation-Robust Optical Clock Receiver Circuit 27
Figure 6 Final Device Structure Geometry with OptoPill Placed in Recess 28
Figure 7 InP/InGaAs Heterostructure Cross Section 30
Figure 8 OptoPill Stack Geometry Prior to Substrate Removal 32
Figure 9 SEM Image of Etched Diode Heterostructure using RIE...................................... 33
Figure 10 Picking a Gold Side Down OptoPill with a Probe Tip 34
Figure 11 InP-Based Pill Structure Solder Bonded on Copper Surface 36
Figure 12 OptoPill Placed in Recess Ready for Post-assembly Processing 38
Figure 13 OptoPill Post-Assembly Process Flow 39
Figure 14 Fabrication Procedure of Patterned Metallization 41
Figure 15 TLM Characterization Sample with 200 nm of p+ InGaAs Contact Layer 43
Figure 16 Chrome Masks for TLM Analysis.. 44
Figure 17 Graphical Analysis of Transfer Length Method.. 46
Figure 18 TLM Analysis of Cr/Au Contacts on Heavily Doped p-type InGaAs 48
Figure 19 Hole mobility in $In_{0.53}Ga_{0.47}As$ as a Function of Doping Concentration.............. 50
Figure 20 Illustrations of the Discrete and OptoPill P-i-N Photodiodes.............................. 52
Figure 21 Ti/Au Ohmic Ring on Silicon.. 54
Figure 22 Mask "LED MESA" Pattern for OptoPill Active Area Definition 55
Figure 23 SEM Image of the Coarse Profile Dry-Etch InP Floor.. 57
Figure 24 BCB as Planarization Layer Compared with Oxide Mask 62
Figure 25 BCB Curing Temperature Profile in Rapid Thermal Annealer............................ 63
Figure 26 Cross Section of one and two layers of BCB over Grooves................................ 64
Figure 27 Cross Section of an InP-Based P-i-N Photodiode 68
Figure 28 Complete Process Flow for InGaAs/InP Photodiode Fabrication 70
Figure 29 Ohmic Ring Mask... 72

Figure 30 Test Setup for AuZn Ohmic Contact Resistance Characterization 73
Figure 31 AuZn on p+ InGaAs Contact Layer I-V Curve 74
Figure 32 Process Flow for Mesa Definition Using Reactive Ion Etches 76
Figure 33 Mask "COMBO-4" Pattern for Mesa Etch 77
Figure 34 SEM Image of Dry Etched InGaAs/InP Mesa 78
Figure 35 InGaAs/InP Mesas Covered with One Layer of BCB 79
Figure 36 Profilometer Analysis of BCB Mesa Coverage 80
Figure 37 Mask "LED TRANS" Pattern for Open Via 81
Figure 38 Vias Opened in BCB Layer on Silicon Dummy Sample 81
Figure 39 Top Metallization on Silicon Dummy Sample 83
Figure 40 Schematic Cross Section of the Mesa Type Photodiode 84
Figure 41 Mesa-Type Photodiode Characterized Prior to BCB Passivation 85
Figure 42 Photodiode I-V Characteristics and Response to Optical Excitation 85
Figure 43 InGaAs/InP Photodiode I-V Curve Prior to BCB Passivation 86

LIST OF TABLES

Table I Basic Material Properties of Si, InP, and GaAs at 300K 15
Table II TLM Measurements and Theoretical Values of Cr/Au on p-InGaAs 51
Table III Contact Layers of TLM Sample, OptoPill, and Discrete Photodiodes 52
Table IV InGaAs/InP Dry-Etch Design of Experiment (25°C) 59
Table V InGaAs/InP Dry-Etch Experimental Results (25°C) 59
Table VI Epitaxial Layer Design of the Discrete InP-Based P-i-N Photodiode 68
Table VII Theoretical and Measured AuZn Contact Resistance on p-InGaAs 75

1 INTRODUCTION

The goals of this chapter are to provide an overview of optoelectronics and their applications in optical interconnects, to evaluate various integration approaches and their challenges, and to introduce OptoPill assembly, which is a novel heterogeneous monolithic integration technology most recently developed at Massachusetts Institute of Technology (MIT).

Motivations for optical interconnects are provided in Section 1.1. Realized by combining the optical and electrical components, the optoelectronic integrated circuits are discussed in Section 1.2. The heterogeneous integration of III-V optical devices and Si-CMOS VLSI electronic circuits is shown to be superior to the homogenous approach in Section 1.3. Then, the advantages of monolithic processing over hybrid packaging are presented in Section 1.4. MIT's novel monolithic heterogeneous integration philosophy is presented in Section 1.5. Finally, an outline of the thesis is provided in Section 1.6.

1.1 Motivations for Optical Interconnects

Gordon Moore's foretelling observation of the doubling of transistor density in integrated circuits (ICs) every twelve months [1] has held approximately true for nearly forty years. Efforts to increase device density have been traditionally focused on the dimension-scaling of silicon complementary metal-oxide-semiconductor (CMOS) transistors. With the aid of higher resolution photolithography systems, circuit miniaturization has been driving up the degree of integration density. The IC industry has evolved from small-scale integration (SSI), to medium-scale integration (MSI), to large-scale integration (LSI), and finally, to the very-large scale integration (VLSI) of logic density.

With VLSI technology, faster transistors and higher density circuits can now be produced at reduced costs. Today, it is not unusual to find on the order of a billion active and passive components on one single semiconductor chip. In February 2004, Intel released its latest microprocessor complete with cache memory and floating-point arithmetic units on a 122

mm^2 silicon die. Manufactured with the 90 nm process and seven layers of copper interconnects, this processor hosts 125 million transistors and operates at a clock speed ranging from 2.8 GHz to 3.4 GHz [2].

Unfortunately, the increasing transistor counts lead to the increasing levels of power dissipation. More adversely, the dense metal-based interconnections that carry signals from one point on the chip to another do not scale to keep pace with the shrinking of device feature sizes. The large wire parasitics grow to be especially taxing as operating frequencies become higher and higher. Consequently, energy dissipation and signal latency issues associated with metal interconnects begin to dominate the key metrics of circuit performance.

As the CMOS technology continues to scale down in dimension, the physics of electrical interconnections threaten to limit the benefits otherwise achieved from device miniaturization. To overcome this roadblock and allow for greater processing capacity, the Interconnect Focus Center (IFC) has identified the following seven areas of research initiatives: 1) system architecture (such as 3D structures and micro-architectures to shorten interconnect lengths); 2) physical design tools (more powerful CAD for chip layout and interconnect routing); 3) novel communications mechanisms (optical interconnect, I/O bandwidth enhancements); 4) chip-to-module interconnects; 5) new materials and processes (such as organic materials); 6) process modeling, simulation, and technology assessment; and 7) reliability and characterization [3].

Outlined as "Task 3" by the IFC, the use of optical interconnects as a novel communication medium has been diligently researched during the past decade. Low-loss, low-dispersion optical fiber has already established its unquestionable dominance over metal wires for long-haul communications such as advanced telephony and wide area computer networks. The mechanism of data transmission by optical beams is also common in applications with shorter distances such as server-to-server communications.

There exist many justifications for adopting optics at even shorter communication distances such as at the chip level. Not only do optical interconnects promise to reduce the power consumption and lessen the design and routing complexity, the fundamental physics of optics also reduce or eliminate problems including time-varying uncertainties such as clock skew, vulnerability to simultaneous switching noise, and frequency-dependent issues such as cross talk. Circuits integrated with optical devices have the potential to offer superior signal integrity, larger bandwidths, and significantly higher data transmission rates. The ever-increasing demand of high performance computing can therefore be met.

1.2 Optoelectronic Integrated Circuits in Optical Interconnects

Metal interconnect parasitics make the routing of on-chip electrical signals an onerous task, especially at higher operating frequencies. This bottleneck can be eliminated by employing optics as a means to transmit inter-chip and intra-chip data, and the on-chip optical clock distribution is an excellent example of the application of optical interconnects. The optical components that are needed to form an optical interconnection generally include some or all of the following: 1) photon sources (diode lasers, LED) to emit light, 2) modulators to alter the reflection or transmission of light, 3) photodetectors to absorb and convert the light to electrical signals, and 4) waveguides for carrying the signals.

When the photonic devices mentioned above are integrated with linear analog circuits or electronic digital components, the combination is called an optoelectronic integrated circuit (OEIC). In other words, optoelectronic integrated circuits incorporate both the electronic and optical devices in order to achieve functionalities that would not have been as well-accomplished with mere electronics [4]. The goal of optoelectronic integration is to provide a reliable and robust optical-to-electrical or electrical-to-optical interface in an efficient and economical manner. In addition to lower manufacturing costs, OEICs also enjoy benefits including compactness, ruggedness, increased reliability, reduction in parasitics, and improvements in circuit performance.

1.3 Heterogeneous Integration over Homogenous Integration

There are two ways to manufacture the electronic and optical components when producing optoelectronic integrated circuits: the homogenous integration of similar semiconductor material system, and the heterogeneous integration of dissimilar semiconductor material systems.

The first electronic integrated circuits of the early 1970s used bipolar technology. Not until the early 1980s when poly-silicon replaced aluminum as the gate material was it possible to fabricate both the n- and p-channel MOS transistors on the same integrated circuit (IC). The resulstant complimentary-MOS (CMOS) transistors consume much less power. Since it is very difficult, and prohibitively expensive, to form the insulating oxide layer for MOS structures on III-V materials [5], electronic circuits are conventionally made with silicon-based processes for which the growth of oxide is a simple practice involving heat and oxygen. Silicon CMOS (Si-CMOS) circuits and its components are more economically available than GaAs (MESFET) or bipolar silicon technologies, and the Si-CMOS technology has irrefutably dominated today's microelectronic applications and digital electronics industry.

Although silicon is the building block of CMOS-VLSI electronic circuits, it is nevertheless a very poor material for the manufacturing of optical devices. In fact, it is essentially impossible to fabricate many sophisticated optical devices such as the vertical cavity surface emitting laser (VCSEL) in silicon due to its indirect bandgap properties. Active photonic devices, such as lasers, are conventionally fabricated with III-V compound semiconductors, whose direct bandgaps allow for the direct recombination of electrons and photons, and thus the emission of light.

Only by joining the III-V optical devices with the Si-CMOS electronic circuits can the true benefits of integration be enjoyed by optoelectronic circuits. Research as presented in this thesis prefers the heterogeneous approach over the homogeneous one for its superior integrated performance and commercial feasibility. Focus was put on the heterogeneous

integration of the InGaAs/InP P-i-N photodiodes with the Si-CMOS optical clock distribution circuits.

Integrating heterogeneous material systems is not without challenges. There are several complicating physical factors: lattice constant mismatches, thermal expansion coefficient mismatches, and lattice polarity disparity. To quantify this statement, the basic material properties of Si, indium phosphide (InP), and gallium arsenide (GaAs) [6] are shown in Table I.

Table I Basic Material Properties of Si, InP, and GaAs at 300K

Properties	Si	InP	GaAs
Lattice constant [Å]	5.43	5.87	5.65
Thermal expansion [K^{-1}]	2.6×10^{-6}	6.3×10^{-6}	6.9×10^{-6}
Bandgap [eV]	1.11	1.35	1.43
Electron mobility [cm^2/V-s]	1350	4000	8500
Hole mobility [cm^2/V-s]	480	100	400
Dielectric constant	11.8	12.4	13.2

As one can see, it is difficult to realize high quality III-V material on CMOS electronic wafers because of these material mismatches. Conventional hetero-epitaxial growth on silicon suffers a high density of threading dislocations in the epitaxial films due to the lattice constant mismatch as well as the residual stresses caused by thermal expansion coefficient mismatches. Recombination-based optoelectronic devices, therefore, suffer much degradation in their performance, efficiency, and operating lifetime. Mismatches in thermal expansion coefficients also result in significant pattern misalignment if wafer bonding is used to combine the materials. A large amount of stress is induced on the bonded wafers, and this problem can only be aggravated by elevating temperatures. The heterogeneous OEIC vision is also obstructed by process incompatibilities of the CMOS and III-V technologies. Commercial wafers are only available in 150 mm for GaAs and 100 mm for InP, while industry standard Si wafers are either 200 mm (8 inch) or 300 mm (12 inch). The incompatible wafer diameters can limit the throughput of batch processing, diminishing the cost and yield advantages of wafer-scale integration unless it too is addressed.

1.4 Hybrid Integration and Monolithic Integration

Whereas the terms "homogenous" and "heterogeneous" describe the likeness of the electronic and optical material systems in an OEIC, the terms "monolithic" and "hybrid" describe the method of casing or enclosure of the electronic and optical components in an OEIC. While the hybrid integration assembles discrete elements together to create one physical entity, the monolithic integration incorporates disparate functionalities on one amalgamated platform.

The traditional hybrid integration is the multi-chip module assembly where numerous chip-level components are packaged into a single housing. Done one-chip-at-a-time, the hybrid approach directly assembles III-V device circuit chips with the fully processed Si IC chips. Therefore, problems related to material differences can be resolved. Using the long-established flip-chip solder bonding and substrate thinning techniques, numerous OEIC applications with functionalities such as laser emission [7] and high speed light detection [8] have been successfully demonstrated.

The hybrid assembly is attractive because it provides an immediate and economical solution for the low-risk fabrication of optoelectronics. However, it is only a temporary means to accomplish heterogeneous integration since it involves a great deal of specialized processing. Due to the piece-by-piece nature, the conventional hybrid assembly cannot benefit from the high integration density, high manufacturing yield, and other advantages of wafer-scale batch processing. In addition, parasitics of traditional packaging considerably degrade the performance and reliability of hybridized ICs. As a result, benefits originally awarded by the application of optics can be severely invalidated.

The monolithic integration incorporates both the optical and electronic device functionalities on a single chip of semiconductor. Structural robustness and the compactness of monolithic hardware relate positively to the circuit performance and reliability. More importantly, since all components are contained in a single rigid structure, monolithic OEICs can be batch-fabricated using commercial IC processes.

If indeed no modifications or additional procedures are required of the standard fabrication flow, it is then possible to achieve high-volume, high-yield productions of OEICs of VLSI complexity. Though the true monolithic integration offers many advantages when possible, it is important to keep in mind that there exists a range of "pseudo" or "quasi" monolithicity which can overcome many, if not all, of the material system differences, while also retaining many, if not all, of the advantages of true monolithic integration. The issue to be scrutinized here is how modular the integration can be in order to achieve the same goal with the maximum amount of benefits.

1.5 Recess Mounting by Monolithic Metallization

The ultimate goal of optoelectronic integration is to develop a commercially practicable platform that realistically addresses all the material mismatch issues (heterogeneous versus homogenous), while at the same time encapsulate multiple device functionalities into a single compact structure (monolithic versus heterogeneous).

A novel integration philosophy termed Recess Mounting by Monolithic Metallization (RM^3 or "RM-cubed") was conceived to surmount difficulties currently faced by competing monolithic technologies. RM^3 is a heterogeneous integration technology that offers the large-scale characteristics of monolithic integration, while at the same time, alleviates integration difficulties caused by material mismatches.

In RM^3 integrations, optical device functionalities are integrated with the electronics on an IC wafer in a modular fashion. Figure 1 (a) shows the cross-section of any empty recess which has been custom-designed in the dielectric layers of a commercial IC. Typically, an IC wafer would have thousands of such integration sites where the photonic devices are to be added. In Figure 1 (b), a III-V device heterostructure is "positioned" into the recesses. Then, post-assembly processing is done in Figure 1 (c) to monolithically transform the heterostructures into a functional optical device that is interconnected with the pre-existing electronics by thin film metallization. By this approach, parasitic elements, such as the node

junction capacitances, are much reduced, and consequently, high performance optoelectronic applications become a much closer reality.

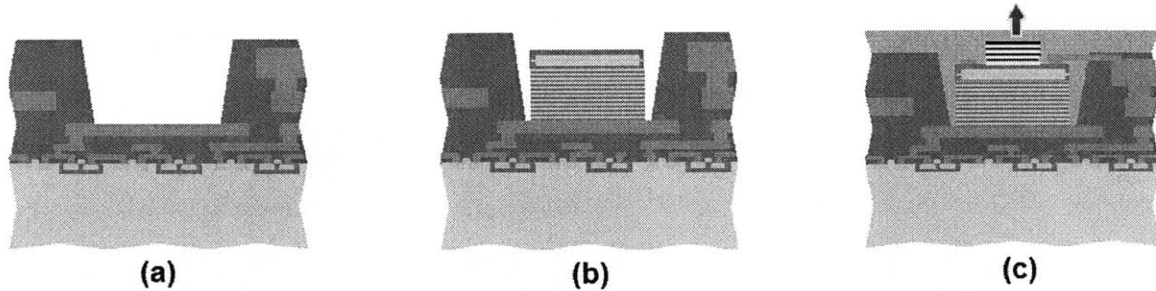


Figure 1 Recess Mounting by Monolithic Metallization
The innovative concept of RM^3 has been a vision jointly researched and developed by students in Professor Fonstad's group at MIT. In (a) is an empty recess previously designed in the dielectric layers of a commercial IC. This is the site where the photonic device is to be added. In (b), the photonic heterostructure is mounted into the recess. In (c), the heterostructures are monolithically processed into photonic devices, and interconnected with pre-existing electronics by thin film metallization.

RM^3 is a flexible and practical approach to accomplish heterogeneous integrations. Since this technique remains compatible with commercial integrated circuit, development efforts are much assuaged and a variety of optoelectronic devices can be integrated on VLSI electronic circuits. The power of RM^3 is in its concept, whereas the ingenuity lies in the filling of the recesses. Several generations have been developed over the years, and are discussed in the following subsections. Epitaxy-on-Electronics is presented in Section 1.4.1, Aligned Pillar Bonding in Section 1.4.2, and OptoPill Assembly in Section 1.4.3.

1.5.1 Epitaxy-on-Electronics

The first generation of RM^3 was a homogenous approach, in which an OE-VLSI integration was accomplished [9]. Epitaxy-on-Electronics (EoE) adopted GaAs integrated circuit processes and circumvented the difficulties experienced by the lattice-mismatched growths of III-V epilayers on silicon substrates. In Figure 2, the III-V optical heterostructures were grown epitaxially into the dielectric growth windows of a fully processed GaAs wafer. These windows, or recesses, that exposed the underlying substrate were pre-designed in the IC wafer. The backside contact to the optical device was established through the N-type implants. After the growth of the heterostructure, polycrystalline material remaining outside the recesses was removed. Then, the lattice-matched heterostructure device was processed

into a functional optical device such as a vertical cavity surface emitting laser (VCSEL) or a light emitting diode (LED). Finally, they were interconnected with the pre-existing MESFET electronic circuits. A highly planar, homogeneous monolithic OEIC was therefore produced.

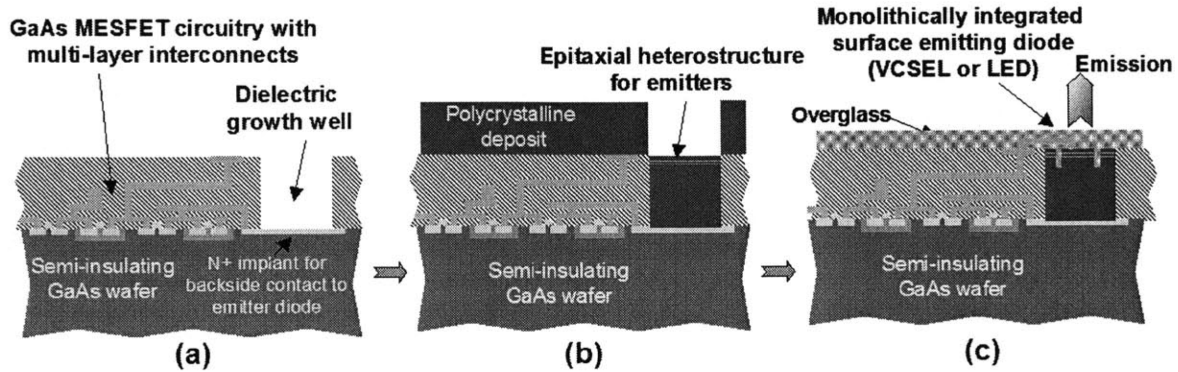


Figure 2 Illustration of the Epitaxy-on-Electronics Integration Process
The EoE process was developed by J. Ahadian in Professor Fonstad's group. Illustrated here are: (a) Processed GaAs IC wafer as received from the manufacturer. (b) The GaAs wafer sample after epitaxial growth of III-V layers. The thick polycrystalline deposit remained from MBE growth was removed from the surface of the wafer. (c) "Post-growth" optoelectronic device processing to complete the integration.

Disadvantages of EoE arise from the temperature incompatibility of molecular beam epitaxy (MBE) growth with the electronics and their metal interconnects. While high temperature steps of MBE were necessary for the growth of high quality materials, they compromised the thermal stability of electronic integrated circuits. In addition, metal interconnects exhibited undesirable grain boundary diffusions at temperatures exceeding a threshold value, whereby the sheet resistance would be drastically increased, and the circuit performance much degraded [10]. Furthermore, the EoE approach was restricted to III-V substrates only. This was very limiting because III-V technologies (such as GaAs MESFET) are not as commercially developed nor economically available as the Si-CMOS processes.

1.5.2 Aligned Pillar Bonding

Aligned pillar bonding (APB) was the initial heterogeneous approach of RM^3 integration. As shown in Figure 3, the heterostructure material was first patterned into pillars at positions on the "source wafer" that mirrored that of recesses on the electronic "target wafer". These pillars were then aligned and bonded. After the pillars were properly secured in the recesses of the commercial IC wafer, the source wafer substrate was removed. Post-bonding processes were carried out to monolithically transform the remaining heterostructure pillars into photonic devices. The optical and electronic components were then interconnected to complete the optoelectronic integrated circuit.

As opposed to direct hetero-epitaxy on electronic circuits, the III-V devices for APB were grown on lattice-matched substrates under optimal conditions, and were integrated by bonding. With the independent growth, high-quality III-V photonic heterostructures for high-complexity optical devices can then be realized. Furthermore, decoupling epitaxy from the IC wafers eliminated the high temperature steps originally conflicting with the electronics metallurgy.

Provided that the IC wafer had a thermal expansion coefficient that is well-matched with that of the heterostructure wafer, the APB technique was compatible with any VLSI processes. While EoE was restricted to GaAs wafers and the MESFET technology, APB expanded to include Si-CMOS process as part of its fabrication sequences. The ability to exploit silicon-based processes with VLSI technology made APB a much more flexible and desirable approach than EoE.

There were, however, several disadvantages associated with aligned pillar bonding. First, it was difficult to achieve a co-planar alignment of the source wafer and the target wafer. Secondly, pillars were created only at positions mirroring that of the recesses on the electronic wafer while the rest of what was discarded; this made for very inefficient use of the grown epitaxial material. Lastly, the thermal expansion coefficient mismatches and incompatible InP, GaAs, and Si IC wafer sizes had been restricting the APB integrations to chip-level processing only.

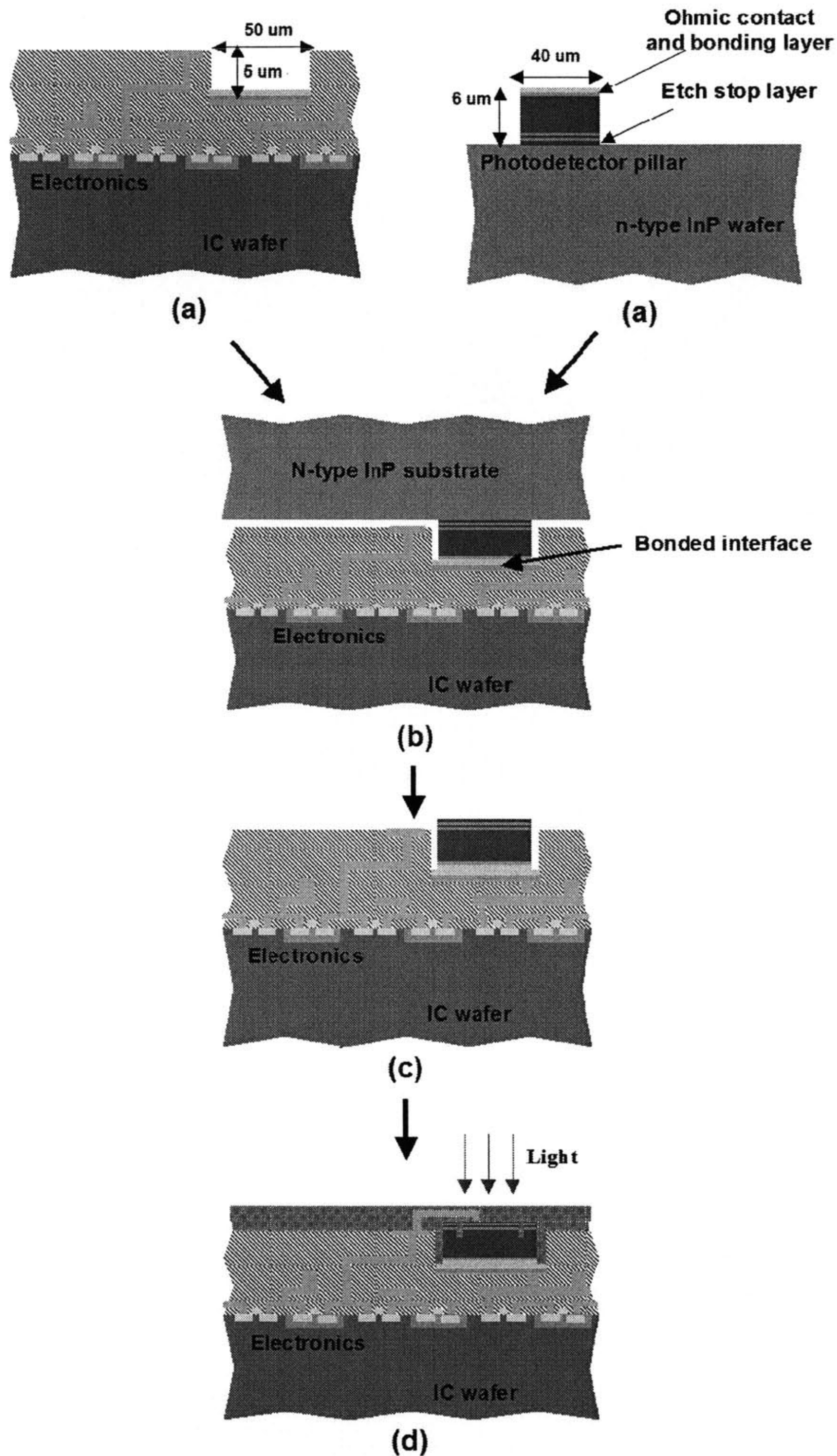


Figure 3 Illustration of the Aligned Pillar Bonding Integration Process
The aligned pillar bonding process involved several steps. Shown in (a) are the "target" wafer, which was the processed IC wafer as received from MOSIS, and the "source" wafer, which was the III-V material that had been patterned into pillars. The pillars on the III-V source wafer were at positions mirroring that of the recesses on the target wafer. (b) The pillars on the source wafer were aligned and bonded into the recesses on the target wafer. In (c), the backside substrate was removed and the APB process was brought to its completion in (d).

1.5.3 OptoPill Assembly

The latest approach in the evolution of RM^3 is the OptoPill Assembly (OPA). The OPA process is illustrated in Figure 4.

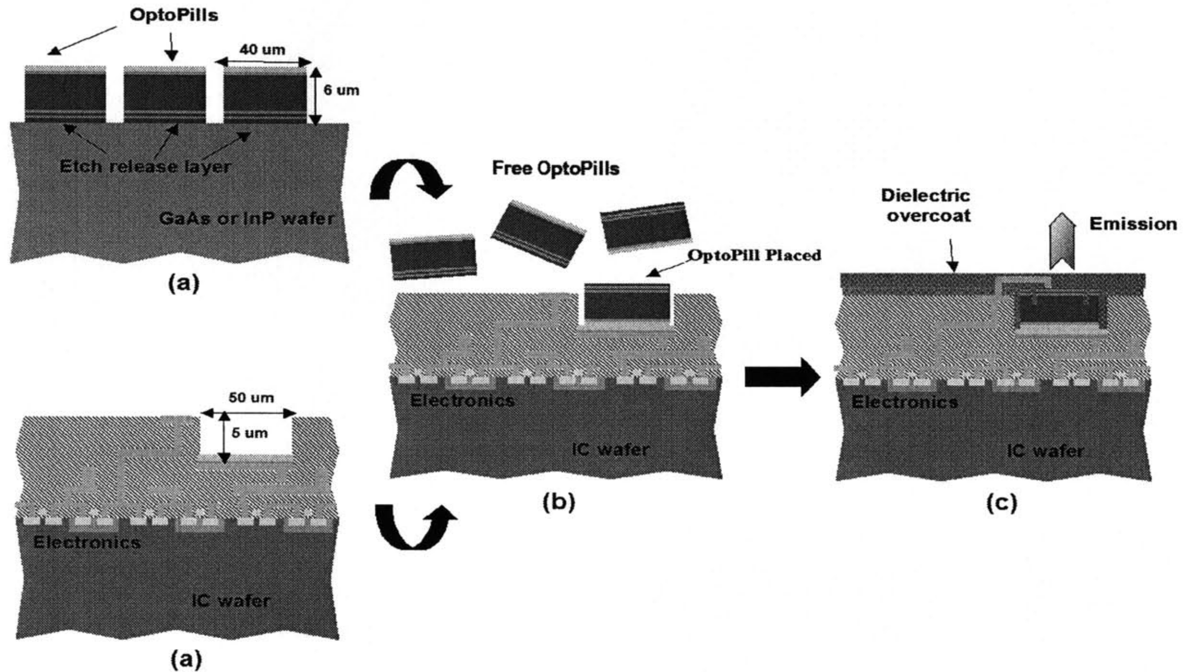


Figure 4 Illustration of the OptoPill Assembly Integration Process
As seen in (a), OptoPills were created by etching off the circular-pillars that were patterned on the heterostructure wafer. The target wafer was the commercially processed IC wafer containing the recesses. Recess-mounting of OptoPills as shown in (b) can be done manually by pick-and-placing, or magnetically using techniques developed in the Magnetically-Assisted Self Assembly (MASA) project. The Manual Pick-and-Place (MPAP) work was mainly developed by M. Teo, and the MASA project (funded by SRC), was developed by J. Rumpler and J. Perkins at MIT. Once the OptoPills have been assembled and bonded into the recesses, post-assembly processing is carried out in (c) in order to transform the OptoPills into finished devices, which were then interconnected with the Si-CMOS electronics. The monolithic OEIC was thus complete.

Like APB, OPA began with an electronic "target" wafer and a III-V "source" wafer. OptoPills were created by etching off the circular-pillars that were patterned on the source wafer. The pills were sized to "almost-completely" fill the recesses, such that its top surface would be nearly coplanar with the top surface of the processed wafer. Depending on the specific application, the heterostructure pill could be an un-processed, partially processed, or fully processed device, or even a small and fully processed circuit. The fabrication of OptoPills is discussed in Chapter 2. After the pills have been prepared, they were then assembled, either manually or magnetically, into the designated recesses. After placement,

the OptoPills were bonded onto the ohmic pads at the bottom of the recesses and a proper backside contact was ensured.

Following the assembly of pills, "post-assembly" processing was carried out on-chip in which the ohmic contacts were formed on the top-side of the heterostructure pills, the active areas of the photonic structure were defined, and the wafer surface was passivated and replanarized with a dielectric material, and the top metallizations were made. A fully monolithic and highly planar OEIC which was interconnected with the underlying electronic circuitry was then produced.

Compared to aligned pillar bonding techniques, alignment accuracy was significantly relaxed for OptoPill assembly due to the modularity of pill-placements. Not only did OPA possess the batch-processing capabilities of a monolithic approach, it also enjoyed the convenience and viability of a hybrid approach.

1.6 Thesis Organization

In Chapter 1, optoelectronic circuits and their applications in optical interconnects have been discussed. Advantages of the heterogeneous approach over the homogeneous method were provided, and its physical challenges were identified. Technical tradeoffs of the hybrid and monolithic integration techniques were discussed. Lastly, MIT's most recent monolithic integration technique, OptoPill Assembly (OPA), has been introduced.

The OPA process developed for heterogeneous optoelectronic systems is discussed in Chapter 2. A variation-robust Si-CMOS optical clock receiver circuit is provided. Encapsulated as "OptoPills", the fabrication, pick-and-placement, and bonding of the III-V P-i-N photodetector are discussed. A brief introduction to post-assembly processing is given at the end of the chapter.

As the focus of this thesis, Chapter 3 describes the post-assembly processing of OPA integrations. The procedures designed, techniques developed, challenges seen, and results learned from each processing step are discussed. Following an illustration of the overall

post-assembly flow, makings of ohmic contact formation, active area definition, passivation and planarization, via opening, and top metallization, are individually described.

In Chapter 4, the fabrication procedures and preliminary characterization results of discrete InP-based P-i-N photodiodes are presented. The processing steps are derived from the post-assembly processes. Final conclusions on the development of post-assembly processes and future research directions are remarked in Chapter 5.

2 OPTOPILL ASSEMBLY INTEGRATION

The philosophy of recess mounting by monolithic metallization was applied to an optical clock distribution project. The heterogeneous optical and electronic elements of this OptoPill assembly monolithic integration are presented. In Section 2.1, the rationales for optical clocking are justified, and the design of a variation-robust optical clock receiver circuit is briefly evaluated. In Section 2.2, the InP/InGaAs heterostructure is examined. Techniques and processes for the pick-and-place assembly and bonding of the pills in recesses, as well as the re-planarization of the wafer surface, are described in Section 2.3.

2.1 The Si-CMOS Optical Clock Receiver Circuit

Caused by differences in path lengths, clock skew can be compensated with a balanced H-tree network at the costs of hefty parasitics and higher power consumption. As the CMOS technology continues to scale down, such traditional distribution schemes are becoming more and more vulnerable to the increasing temporal and special variations introduced by the decreasing gate lengths and line widths.

On-chip optical clock distribution is a possible alternative to traditional balanced electrical distribution networks. By eliminating all together the need for metal interconnects, an optical network becomes effectively immune to the time-varying propagation delays, skew and crosstalk. Very precise synchronization can therefore be provided.

Variations are extremely difficult to control or compensate. In an optical network, variations affect the proper distribution and detection of optical signals. Although an optical network is theoretically variation-robust, the optical-to-electrical and the electrical-to-optical conversion circuits are still susceptible to process variations and timing uncertainties may still be introduced. Three main sources of variation have been identified [11]:

1) The Optical Network

Clock signal from a laser or laser-diode is distributed to multiple receivers across the chip by an optical network. The main components that constitute an optical network including the optical source, waveguides, couplers and photodiodes are all potential sources of variations which can cause significant skew and jitter.

For example, laser diodes bring about a nominal amount of clock jitter. Non-uniform waveguides can lead to varying index of refraction, which results in clock skew. Uneven splitting of the light beam gives rise to optical intensity variations. Process variations beget non-homogeneous photodiode materials, and the varying active areas alter the amount of photocurrent generated as well as the leakage current.

2) CMOS Process Variations

The largest variability comes from the CMOS processes. Such manufacturing variations are spatially independent. While the front-end variations alter the MOS parameters (such as gate length, gate width, threshold voltage and mobility), the back-end variations affect the interconnect structure (such as line width, spacing, line height and interlayer dielectric thickness).

3) Environmental Variations

Environmental sources such as power-supply variation caused by digital switching activities can cause noise and affect the circuit behavior. Parameters such as threshold voltage and mobility are also affected by temperature variations.

To minimize these dependencies, a variation-robust optoelectronic receiver operating at 2 GHz has been designed by N. Drego in Professor Boning's group at MIT. This receiver circuit adopted a fully differential architecture which offers high common-mode rejection ratio and power-supply rejection ratios, and consequently, high-bandwidth amplifiers were made possible. Offset compensation circuitry was developed to counteract deep sub-micron process mismatches. Replica feedback biasing and a process-compensated current reference

[12] were also incorporated into the optical clock distribution circuit for stable biasing. A layout of the optical clock receiver circuit is shown in Figure 5.

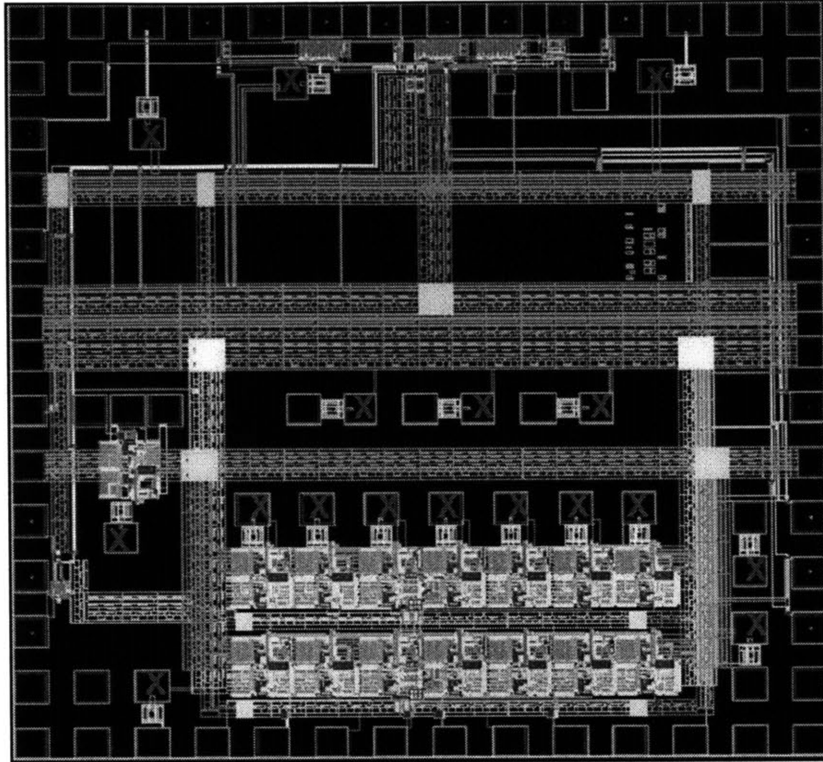


Figure 5 Layout of the Variation-Robust Optical Clock Receiver Circuit
A photomicrograph of an optical clock circuit chip, designed and laid out by N. Drego in Professor Boning's group at MIT. The die size was 2.2 mm by 2.2 mm, with seventeen 50 μm by 50 μm recesses pre-designed in the layout. This project was funded by MIT and MARCO IFC. Over the past few years, this receiver circuit has been designed, developed, and improved by S. Sam, A. Lum, and N. Drego.

This test chip was fabricated by MOSIS with TSMC 0.18 μm CMOS process. Each die was 2.2 mm by 2.2 mm. The seventeen "X" marks denote the locations of recessed windows, which were the sites for the heterostructure pills are to be placed. Identical to both the EoE and the APB processes, the recesses were previously laid out by the chip designer at designated locations where the III-V devices were to be added. Figure 6 shows the cross-sectional diagram of a recess and pill geometry situated in 7 μm of metal interconnections and dielectric layers of an electronic IC wafer. The square recesses were 50 μm by 50 μm, and the circular OptoPills were 40 μm in diameter.

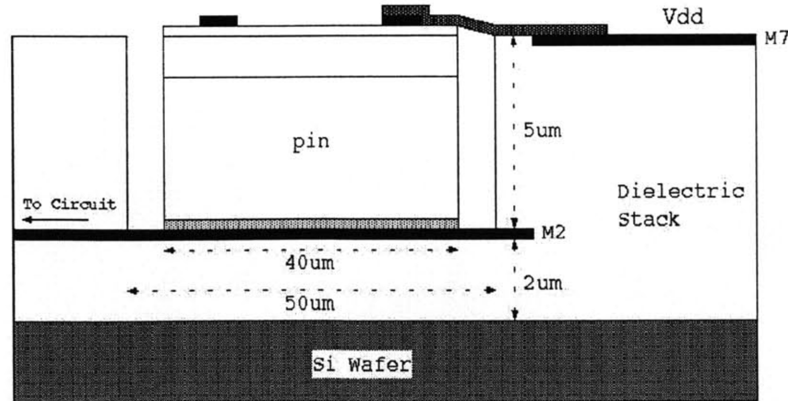


Figure 6 Final Device Structure Geometry with OptoPill Placed in Recess
As seen, the back contact pads were formed in metal layer 2 (M2) which resides 5 μm below the top wafer surface. The upper contact pad was formed in metal 7 (M7). The recess has dimensions of 50 μm by 50 μm. This size is suitably designed for the inhabitance of OptoPills that are 40 μm in diameter.

A metal mounting and a backside contact pad were formed at the bottom of the recess in metal layer 2 (M2), which was 5 μm below the top of the wafer surface. After normal back-end processing, metal-free dielectric layers above these metal pads were removed to form the recess. The designer also laid out upper-level metal patterns in metal layer 7 (M7) that can be exposed and used to provide electrical connection to the top-side of the photo-device.

2.2 The III-V Photodetectors

Different compositions of III-V compound semiconductor materials yield different bandgap energies, lattice constants, thermal expansion coefficients, and quantum efficiencies. Photonic devices such as lasers and photodiodes are typically manufactured on binary III-V systems such as GaAs or InP substrates. The active layers of photonic devices are solid-state alloys whose material properties are adjusted to respond to different wavelengths and for various optical applications.

Photodiodes are important instances of photonic devices used for the conversion of optical to electrical signals in optoelectronics applications. Like other optoelectronic devices, photodiodes are favorably made from monolithic crystal structures of various compound semiconductor layers. III-V heterostructures can be designed to provide control of the current flow and carrier injections, as well as the quantum confinement in selected layers.

As its name suggests, a "P-i-N" diode is a p-n junction designed to have an intrinsic, or "i" layer, which is sandwiched in-between a p-type "P" layer, and an n-type "N" layer. In practice, the i-region need not be truly intrinsic; it can be approximated by a high-resistivity p-type or n-type layer. When reverse-biased, the low doping profile of the i-layer causes the potential drop to appear almost entirely across this region. In other words, the width of the space charge region of a P-i-N photodiode is effectively the thickness of its intrinsic layer. In the space charge layer, generated hole-electron pairs are swept quickly across the junction due to large electric field. Therefore, performance can be optimized with wider depletion regions.

In addition to the semiconductor material used as the i-layer, the performance of a photodiode is also dependent on the device area, which is directly associated with the junction capacitance. In a P-i-N diode, lower capacitance per unit area allows for faster response time and higher performance of the photodiodes.

Indium phosphide is a very important III-V compound in the optoelectronics industry. Since photodetectors fabricated with InGaAs or InP-based material systems are commonly used for fiber-optic telecommunication systems and P-i-N photodiodes with InGaAs as the light-absorbing layers are naturally suited for the 1.3 μm and 1.55 μm wavelengths, InGaAs/InP P-i-N photodiodes were used to provide the photocurrent in this project.

The quality of the semiconductor epilayers is critical to the successful integration of OEICs. The InP-based diode heterostructure in Figure 7 was grown by Professor Fatt and his students at NangYang Technological University, Singapore.

Layer
0.2 μm p+ InGaAs contact (5E18 cm^{-3})
5 μm P+ InP buffer (5E18 cm^{-3})
0.05 μm InP spacer (un-doped)
1.1 μm InGaAs i-layer (un-doped)
0.05 μm InP spacer (un-doped)
0.25 μm N+ InP upper window (5E18 cm^{-3})
0.2 μm n+ InGaAs contact/etch stop (5E18 cm^{-3})
2.5 μm N+ InP buffer (5E18 cm^{-3})
N+ InP (100) substrate

Figure 7 InP/InGaAs Heterostructure Cross Section
The InP-based diode heterostructure was grown by Professor Fatt and his students at NangYang Technological University, Singapore. The structure consisted of a p+ and an n+ InGaAs contact layer, two heavily doped InP buffer layers, and 1.1 μm layer of intrinsic InGaAs that was sandwiched in-between. Circular-shaped pillars were first etched down to the n+ InGaAs etch stop layer. The P-i-N structure had a thickness of 6.65 μm.

Circular-shaped pillars were first etched down to the InGaAs etch stop layer. Then, turning the heterostructure wafer upside down, the backside substrate was removed. The revised structure was designed to provide sufficient height difference between the top of the placed OptoPill and the wafer surface, in order to effectively apply the pressure needed for bonding.

The photodiode structure consisted of a p-type and an n-type doped InP buffer layer, and a 1.1 μm layer of intrinsic InGaAs that was sandwiched in-between. The P-side contact of the photodiode was made on the p- doped ($N_A = 5 \times 10^{18}$ cm^{-3}) InGaAs semiconductor and the N-side contact was made on the n- doped ($N_D = 5 \times 10^{18}$ cm^{-3}) InGaAs semiconductor. The P-i-N layers add to a total height of 6.65 μm.

As discussed earlier in the section, the performance of photodiodes depends on the device capacitance. The RM^3 monolithic integration concept can be realized without adding many capacitive elements of related packaging, which in turn limit the response time of the

receiver circuits. At high frequencies and zero or reverse bias, the P-i-N diode appears as a parallel plate capacitor which is essentially independent of reverse voltage. The capacitance of the device is mainly due to the junction capacitance *C*, which is a function of the area of active region *A*, the intrinsic layer semiconductor material ε, and the thickness of the depletion region *d*.

Capacitance $C = \frac{\varepsilon A}{d}$, where

A = active area of the photodiode [μm^2],

d = thickness of depletion region [μm],

$\varepsilon_{r,InGaAs}$ = relative dielectric constant of InGaAs [unitless],

ε_o = permittivity of free space [F/μm],

ε_{InGaAs} = permittivity of InGaAs,

$= \varepsilon_{r,InGaAs} \bullet \varepsilon_o$

$= 13.9 \bullet 8.854 \times 10^{-18}$

$= 1.23 \times 10^{-16}$ [F/μm]

As one can see, capacitance *C* is inversely proportional to the depletion region width *d*. Wider active regions yield lower junction capacitances, as well as higher responsivity. The tradeoff with thicker depletion regions is, however, a slower transit time. Similarly, a smaller active area *A* minimizes the junction capacitance and reduces dark current.

The diode heterostructure shown in Figure 7 has an intrinsic layer thickness of $d = 1.1$ μm. Therefore, capacitance per unit area is $c = \frac{C}{A} = \frac{\varepsilon}{d} = \frac{1.23 \times 10^{-16}}{1.1} = 1.125 \times 10^{-16}$ [F/μm^2].

That is to say, a device with an active area of 40 μm by 40 μm fabricated from this sample would have an approximate capacitance of 180 fF, and a device with a smaller junction area, 5 μm by 5 μm, would have a capacitance of 3.2 fF. Pills that were fabricated from this heterostructure and used in the OPA process had a diameter of $d = 40$ μm. The surface area would be $A = \prod r^2 =$ 1256 μm^2, and the junction capacitance of these OptoPills was approximately 140 fF.

2.3 OptoPill Assembly Integration Process

OPA integration involves several main steps: fabrication and preparation of OptoPills, recess-mounting and bonding of the OptoPills, and post-assembly processing. The goal is to monolithically fabricate the OptoPills into discrete optical devices, and to interconnect such processed photodiodes with the Si-CMOS optical clock distribution circuit.

2.3.1 Fabrication of OptoPills

The device heterostructure used to manufacture OptoPills was grown "bottom-side-up" (N-i-P) in order to satisfy the pill-forming process requirement. The stack geometry of an OptoPill prior to substrate-removal is illustrated in Figure 8.

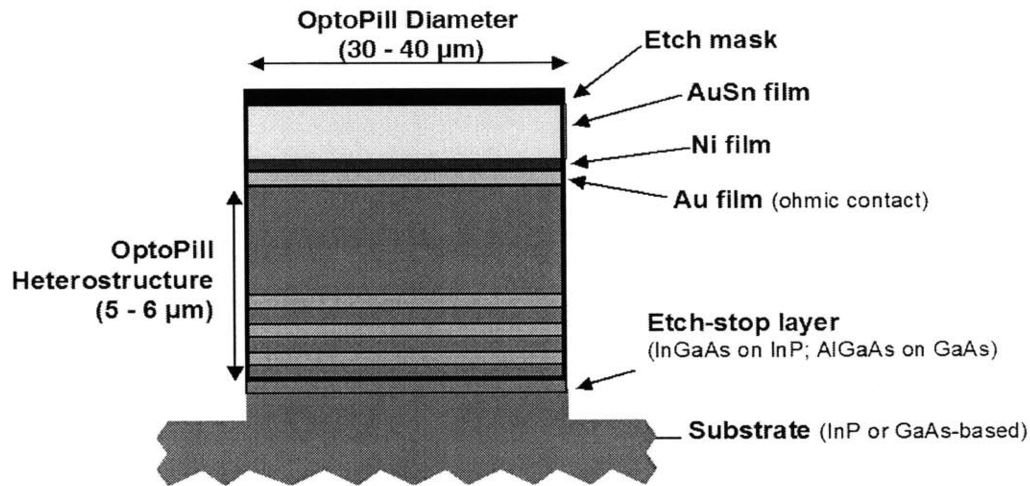


Figure 8 OptoPill Stack Geometry Prior to Substrate Removal
The heterostructure was designed and grown as according to the device structure needed. A stack of metal layers was first deposited for contact and bonding purposes. The metal layers were then patterned and used as mask to etch the III-V wafer into dense arrays of circular pillars. These circular pillars were approximately 40 μm in diameter and 6 μm in height. After backside substrate removal, pill-shaped tablets were finally etched free from the III-V substrate. After cleaning, they were collected as "OptoPills". The sequences for fabricating OptoPills were developed by J. Rumpler and J. Perkins in Professor Fonstad's group at MIT.

The OptoPills were processed as follows: first, a metal stack consisting of gold (Au), nickel (Ni), and gold-tin (AuSn with 20 wt% Sn)) were deposited using the e-beam evaporation system. The first thin layer of Au was used for ohmic contact formation on the semiconductor. The second thin layer of Ni was useful for the magnetic assembly of pills,

which is discussed briefly in the next subsection. A thick 3 μm layer of AuSn included as the outermost layer in the metal stack was used as the solder material for bonding. The AuSn solder can also be created by alternating layers of Au and Sn using electroplating or thermal evaporation.

Either silicon oxide (SiO_2) or thick photoresist can be used as the etch mask. The mask material was deposited on the sample and patterned into arrays of circles. Then, the heterostructure was etched into circular-shaped pillars of diameter 40 μm by reactive ion etching (RIE). For further discussion on the procedures and techniques of InGaAs/InP dry-etching, refer to Section 3.3.

A scanning electron microscopy (SEM) image of an etched heterostructure prior to substrate removal is shown in Figure 9. As one can see, the patterned and etched pills are situated compactly in arrays, making very efficient use of the epitaxial material.

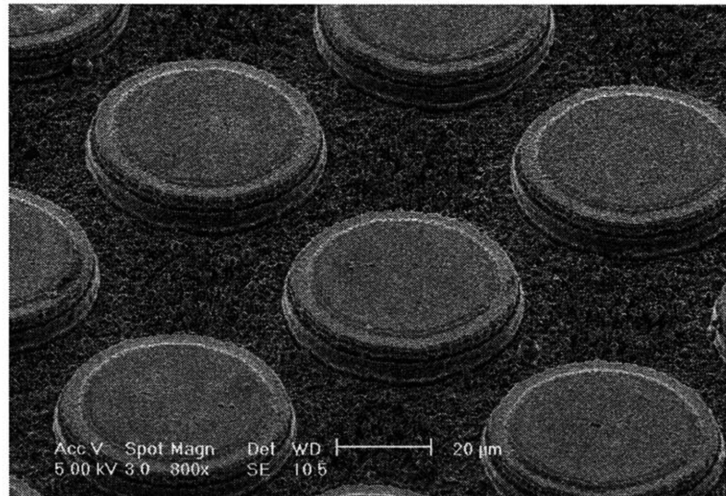


Figure 9 SEM Image of Etched Diode Heterostructure using RIE
III-V heterostructure wafer etched into densely packed arrays of pills, making efficient use of the epitaxial material. This is prior to substrate removal. Heterostructure device tablets known as "OptoPills" are created once they are etched free from the substrate. Cleverly, the OptoPill assembly techniques relaxed much demand on alignment accuracy. Pill processing was done by E. Atmaca, with help from J. Rumpler and J. Perkins at MIT.

After removal of the etch mask, the wafer was embedded face-down in wax. Then, the substrate was removed by etching down to the etch-stop layer of the heterostructure, releasing the tablets of device structure from the III-V substrate. Next, the pills were

cleansed with cycles of solvent rinse sequence. Finally, the OptoPills were collected and ready to be integrated with the Si-CMOS wafer.

2.3.2 Pick-and-Placement

Two techniques were investigated to place the InP-based P-i-N OptoPills into the recesses of an IC wafer: micro-scale manual pick-and-place (MPAP), and magnetically assisted statistical assembly (MASA). The latter approach is a SRC-funded project led by J. Rumpler and J. Perkins in Professor Fonstad's group at MIT [13] and will not be discussed further in this thesis.

Hand assembly was mainly developed by M. Teo, also in Professor Fonstad's group. The MPAP process began with a quantity of OptoPills dispensed on a microscope slide. Done at any manual probe station, pills can be picked up with probe tips wetted with solder flux. Figure 10 shows a gold-side-down pill that was picked up by an ordinary probe tip. Then, with careful manipulations of the microcontrollers, the pills were placed one at a time into the recesses of a Si-CMOS chip.

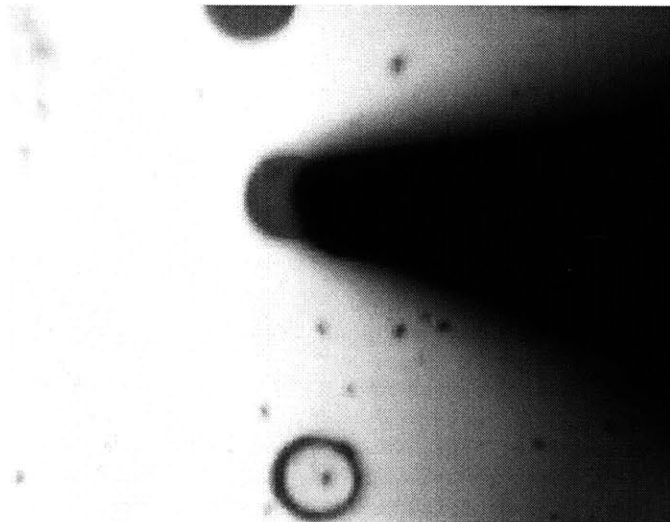


Figure 10 Picking a Gold Side Down OptoPill with a Probe Tip
Hand assembly was done at a probe station. The manual pick-and-place technique was mainly developed by M. Teo. The began with a quantity of pills dispensed on a microscope slide, then picking up only the pills that were oriented with their metal coated side down, and which do not show evidence of lateral etching having occurred when the substrate was removed.

2.3.3 Solder Bonding

Fixing the pills in recesses can be done by either soldering or bonding. While bonding requires high surface planarity, and a considerable amount of heat and pressure, soldering imposes much less stringent constraints on co-planarity. With soldering, irregular bonding surfaces such as that at the bottom of the recesses can then be accommodated; high bonding strengths can be attained with less heat and applied pressure. In this work, the OptoPills were fixed by the soldering techniques.

More than a mere hazardous material, the solder flux is damaging to photonics and the device sensitivity. Fluxless assembly eradicates the use of flux which removes the oxide formed on molten alloy, and the fluxless AuSn solder was chosen for this process. Used extensively in the optoelectronics industry, the AuSn solder is also attractive because it melts at 280°C - a temperature higher than what is expected during normal device operations but not so high that the underlying IC will be damaged during soldering. In addition, the AuSn solder offers high yield strength, resistance to corrosion and creep under repetitive thermal cycling and excellent thermal and electrical conductivity [14].

Square-shaped copper (Cu) pads were deposited at the bottom of the recesses of the Si-CMOS chip where the OptoPills were to be soldered in place. A 200 nm layer of gold was evaporated on Cu while the sample was still in high vacuum. This was done to prevent oxidation which would otherwise degrade the Cu-AuSn bond integrity. The dimensions of the bonding sites or the recesses were approximately 50 μm by 50 μm. After placement in the recesses, a downward pressure which can be provided by the mass of glass cover slip(s), was applied to the pills against the Cu substrate. This was done to ensure a firm contact for proper bonding.

Bonding experiments with varying time and temperature were conducted at a rapid thermal annealer (RTA) in a forming gas (nitrogen N_2 with 15% hydrogen H_2) ambient. The RTA consisted of a resistively heated graphite stage with a thermocouple embedded into the block. The temperature ramp rate used was 100°C per minute. The optimal bonding

temperature was found to be approximately 340°C. Figure 11 shows a SEM image of an InP-based OptoPill solder-bonded with its gold-side down on a flat copper substrate.

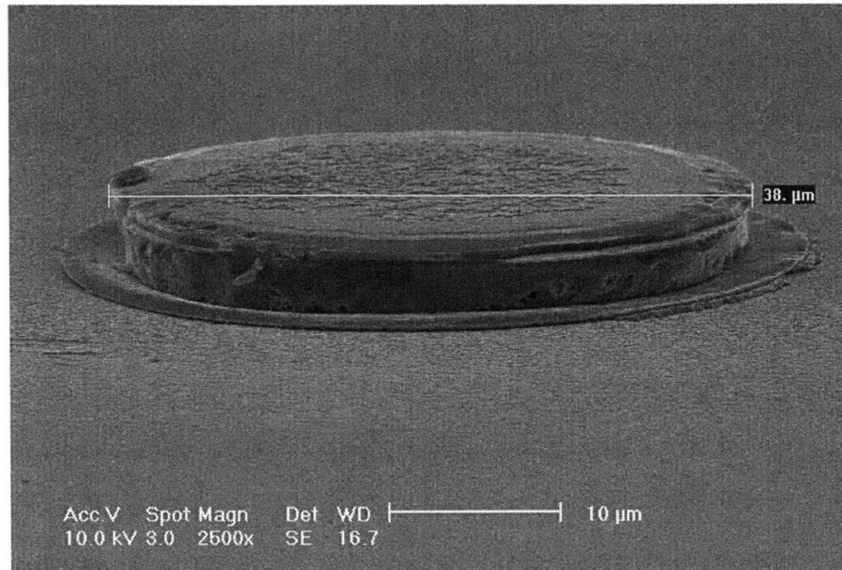


Figure 11 InP-Based Pill Structure Solder Bonded on Copper Surface
The OptoPill as shown has an approximate diameter of 40 μm and an approximate height of 5 μm. It has been found that a pill would not solder to the copper surface unless a slight pressure was applied. With the pills sitting on a flat copper-coated surface, a downward pressured was applied to force the pill against the surface. This pressure came from the mass of glass cover slip(s) which were placed on the pills. It was more challenging to apply the necessary pressure when the pills were in the recesses. This process step was jointly developed by the author herself, M. Teo, and E. Atmaca in Professor Fonstad's group at MIT.

It was more challenging to apply the necessary pressure when the pills were in the recesses. It was found that a strong permanent magnet placed under the IC wafer can provide sufficient attraction force to pull the pills down snugly into the recesses [15]. Recall from Section 2.3.1, the thin layer (0.25 μm) of Ni included in the metal stack can be used in bonding experiments by magnetic means.

2.3.4 Post-Assembly Processing

After Optopills were properly placed and bonded into the recesses, batch-scale post-assembly processing was done on the Si-CMOS wafers. Fabrication techniques, processing procedures, experimental results and discussions associated with each step, are described in Chapter 3.

3 POST-ASSEMBLY PROCESS DEVELOPMENT

Post-assembly process development for RM^3 optoelectronic integration has been the author's primary focus of research. The post-assembly process flow is illustrated in Section 3.1. In Section 3.2 to Section 3.6, the results accomplished for ohmic ring formation, active area definition, planarization and passivation, via opening, and top contact metallization, are discussed in detail. Through post-assembly processing, the photonic heterostructures were transformed into functional optical devices and interconnected with pre-existing electronics.

3.1 Post-Assembly Process Flow

Once the OptoPills have been properly secured in the recesses, any fabrication steps carried out from this point onward to complete the OPA integration are collectively termed as "post-assembly" processes. Post-assembly processing serves several purposes: first, to fabricate an unprocessed III-V heterostructure pill, as shown in Figure 12, into a functional optical device; second, to passivate and re-planarize Si-CMOS wafer surface; and third, to provide electrical interconnection to the optical device. A monolithically integrated optoelectronic circuit is produced at the end of the heterogeneous integration.

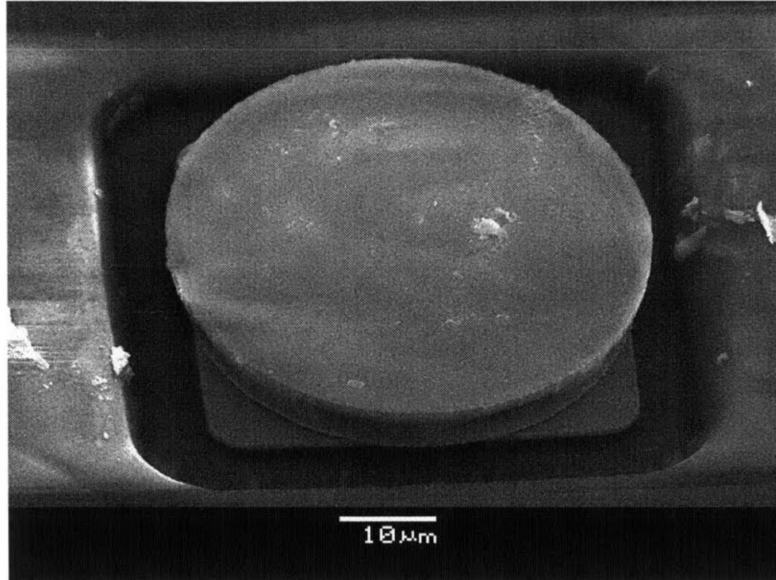


Figure 12 OptoPill Placed and Solder-Bonded in the Recess of an IC Circuit
An InGaAs/InP P-i-N photodiode heterostructure pill, 40 µm in diameter, was manually picked and placed in a 50 µm by 50 µm recess on a Si-CMOS IC chip. At this stage the OptoPill is ready for post-assembly processing. The silicon circuit used was the variation-robust optical clock receiver circuit, as described in the previous chapter.

The complete post-assembly process flow of OPA integration is illustrated in Figure 13. At the beginning of post-assembly processing, the OptoPills have already been placed and fixed in place using techniques described in Section 2.3.2 and Section 2.3.3. Ohmic rings were first formed on the contact layer of the heterostructure pills. Then, the active areas of the photonic device were defined. Then, the Si wafer surface was re-planarized with a passivating dielectric layer. Next, vias were opened to provide electrical access to the optical device from the outside world. Using patterned thin film metal lines, interconnections were made to join the functional optical devices with the pre-existing electronic circuitry. Since wafer surfaces maintained highly planar throughout the entire integration, fine photolithographic patterning can be used all through the OPA process.

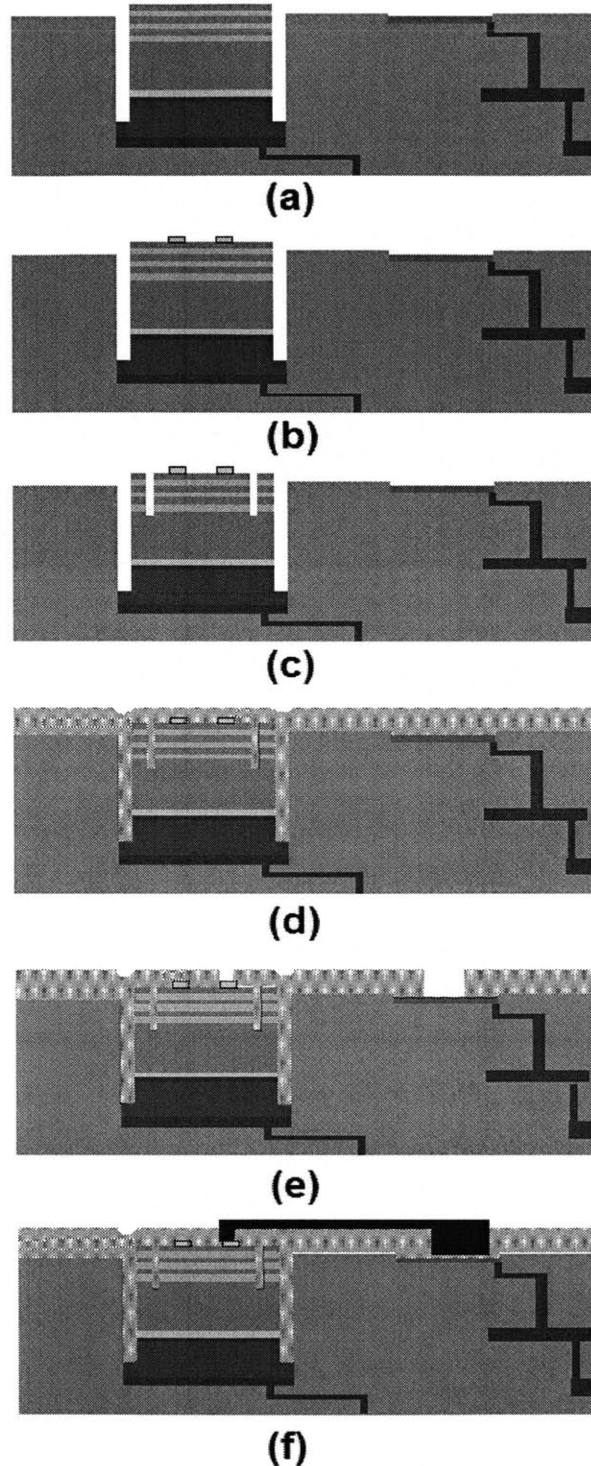


Figure 13 OptoPill Post-Assembly Process Flow
Once the OptoPills are assembled and bonded in recesses as shown in (a), any further processing done from this point forward is considered to be "post-assembly" processing. The first step of post-assembly processing is the formation of ohmic contacts on OptoPills as shown in (b). Then, active areas are defined in (c) by groove etching. The wafer surface is then passivated and re-planarized as seen in (d). In (e), the passivation layer is etched to open interconnect vias. Finally in (f), top contact metallization is created and the monolithic heterogeneous integration process is then complete.

3.2 Ohmic Contacts on InGaAs Layer

3.2.1 Fundamentals

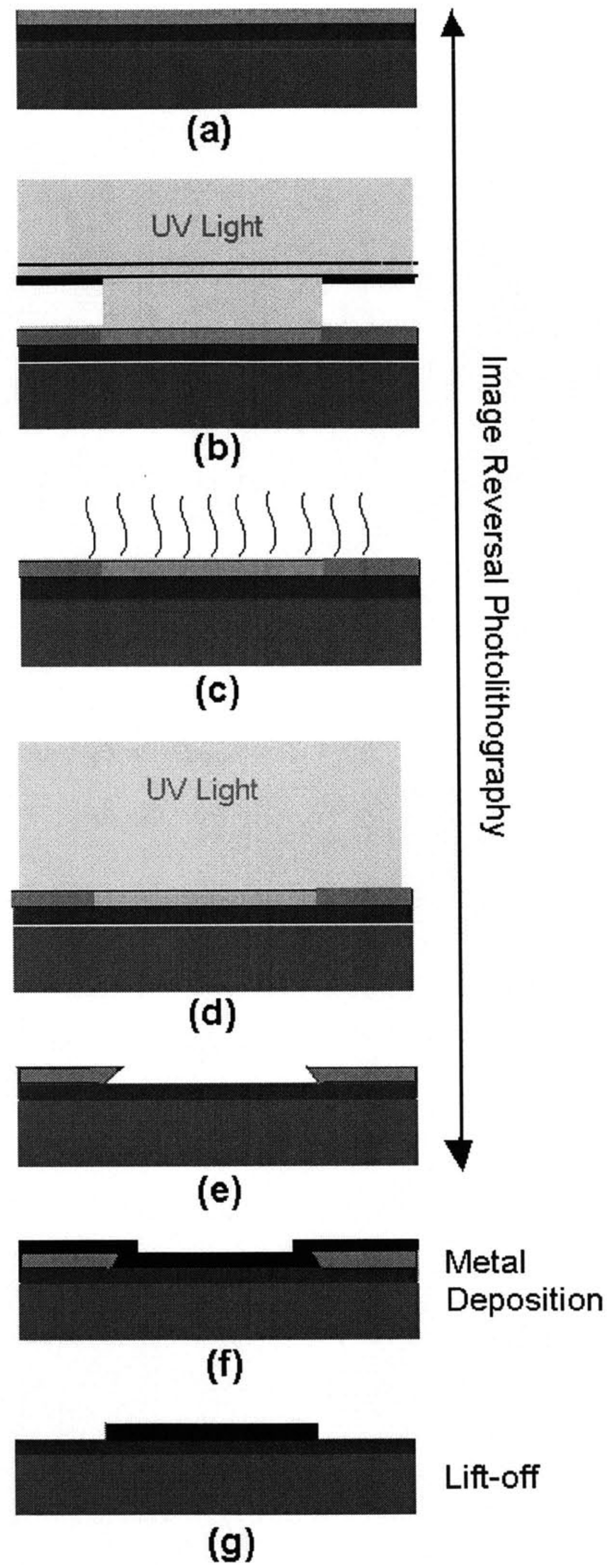
Reliable ohmic contacts play a critical role in the robust operation of integrated optoelectronics. Ohmic contacts are perfect sources and sinks of both carrier types, and they have no tendency to inject or collect either electrons or holes. Such metal-semiconductor contacts typically exhibit linear current-voltage characteristics.

Ohmic contacts act as the electrical links between the active region of the semiconductor device and the external circuit, which allow for a low-energy carrier transport mechanism through the contact volume while ensuring a negligible amount of voltage drop [16]. An abundance of free carriers is needed at the semiconductor surface in order to realize ohmic contacts. This abundance can be provided by the high doping concentration of an epitaxial layer initially incorporated during MBE growth. Since no heat treatment is needed in this case, this type of ohmic contacts is known as "non-alloyed" contacts.

Another common method is to introduce an external diffusion source of dopants. For this process, a heating cycle is required to drive the dopant species into the semiconductor. With sufficient thermal activation energy, migrated dopants intermix to form a heavily doped interfacial layer. This type of contacts is referred to as "alloyed" contacts. The metal-semiconductor interfacial geometries are different in alloyed and non-alloyed contacts [17].

3.2.2 Experimental

Metal patterns on various semiconductor or dielectric materials such as ohmic contacts, top-level pads or interconnects, are created in several main steps: photolithography to pattern the image reversal photoresist, substrate clean, metal deposition, lift-off and anneal. The fabrication procedure is illustrated in Figure 14.



<u>**Figure 14 Fabrication Procedure of Patterned Metallization**</u>

Patterned metallization can be achieved in the following steps: (a) application of image reversal photoresist, (b) exposure using dark field mask (c) post-exposure bake, (d) flood exposure without mask, (e) development, (f) metal deposition, and (g) lift-off.

Patterns of ohmic contact were transferred from the mask to resist by photolithography. First, the wafer was primed with Hexamethyldisilazane (HMDS) to promote surface adhesion of the resist film. Then, image reversal photoresist was spun on the wafer. After resist application, the wafer was pre-baked before exposure to reduce solvent content. The UV light during the first exposure caused the exposed areas of resist to be insoluble, or not-developable in a basic solution, once treated with heat. During a flood exposure, the initial dark field of the photoresist becomes exposed, and a negative-field pattern of the original mask was created in the resist film following development. Not only the tone of the photoresist but also the slope of the developed film, were reversed. The negative slope was highly desirable for subsequent liftoff processes. The detailed image reversal (AZ5214E) photolithography procedure is given in Appendix B.1.

To ensure ohmic connection of the evaporated metal to the semiconductor in exposed areas, samples must be cleaned immediately before deposition. With photoresist as the mask, the wafer was wet-etched in a diluted buffered oxide etchant (BOE) in order to remove any native oxide or surface contaminants that may exist. The sample was then cleaned and ready for metal evaporation.

The metal stack was deposited using an e-beam evaporator system. The e-beam is an intense, high-energy electronic beam ejected under the metal source crucibles. In addition to smooth profiles and shallow step sizes of the wafer piece, e-beam evaporation also facilitates the lift-off processes because of its very directional depositions. Evaporation rates in the order of 3Å/sec are appropriate for lift-off films. For high-quality films, it is important to ensure that a chamber pressure lower than 2×10^{-6} mTorr has been established.

Once the e-beam evaporation was completed, wafers were immersed in acetone to dissolve the photoresist. Metal films tend to break naturally at the edges as the photoresist is being dissolved. As such, metal evaporated in the open areas of the resist remained on the sample, whereas metal evaporated on top of the resist was removed. The lift-off process may be expedited with agitation in an ultrasonic bath.

To establish robust ohmic contact characteristics, the sample underwent heat treatments in a rapid thermal annealer (RTA) in a forming gas ambient. During this anneal process, the metal stack with a layer of dopant species is said to be "alloyed", while the non-alloyed type of metals are said to be "sintered". In either case, as a result of the heat process, the specific contact resistance can be significantly reduced due to the likely formation of a new metal-semiconductor interfacial microstructure.

3.2.3 Transfer Length Method

The transfer length method (TLM) is a classical approach for determining the sheet and contact resistances [18]. The measurements and results of TLM analysis were useful for the development of ohmic contacts for both the OptoPill photodiodes used in the OPA process, as well as the discrete photodiodes fabricated for characterization purposes.

A characterization sample consisting of a thin contact layer was prepared for TLM studies. TLM test structures were created in the semiconducting layer in order to evaluate the quality of non-alloyed, gold-based ohmic metals formed on the p-type InGaAs contact layer. As seen in Figure 15, 200 nm of p-type InGaAs with 53% of indium and 47% of gallium was grown lattice-matched on an undoped InP bulk substrate. This $In_{0.53}Ga_{0.47}As$ contact layer had a high p-type doping concentration of $N_A = 1 \times 10^{19}$ cm^{-3}.

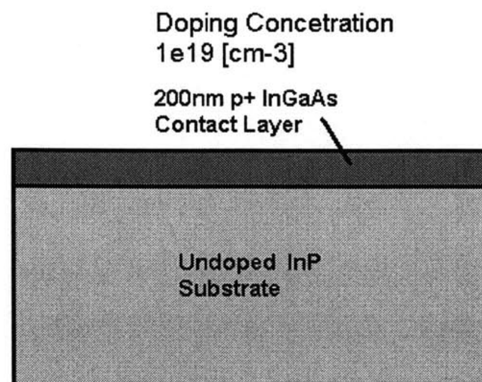


Figure 15 TLM Characterization Sample with 200 nm of p+ InGaAs Contact Layer
The TLM characterization sample was grown by H. Choy in Professor Fonstad's group at MIT. This "dummy" wafer piece was effectively a 200 nm layer of highly-doped p-type $In_{0.53}Ga_{0.47}As$ ($N_A = 1 \times 10^{19}$ cm^{-3}), which was epitaxially grown on an undoped InP substrate. TLM test patterns and structures were created in the contact layer in order to characterize the specific contact resistance of Cr/Au on this thin contact semiconductor.

3.2.3.1 Experimental

Photomasks used to create linear arrays of TLM test structures are as shown in Figure 16.

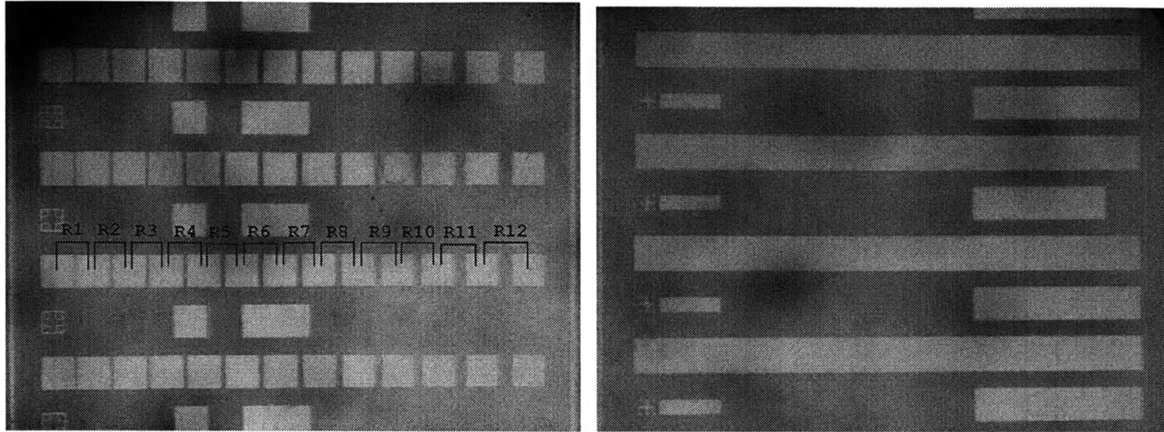


Figure 16 Chrome Masks for TLM Analysis
The chrome masks used for TLM analysis were obtained from Professor Hu's group at MIT. The mask used for ohmic contact pad formation is shown on the left ("mask1"), and the mask used for mesa definition is shown on the right ("mask2"). Both submasks had an area of 1 cm by 1 cm. As seen, the distances between the 100 μm by 100 μm pads were incrementally increasing from the left end of the row to the right end. A larger spacing between two conducting pads inferred a higher resistance path experienced by the carriers. As such, R_{12} (as labeled in the figure) was measured to have the largest equivalent resistance, and R_1 was the smallest. Columns of mesa confined the current flow in the rectangular paths. The pad and mesa patterns aligned with each other with the aid of alignment marks seen on the left hand side of both pictures.

The first photomask as seen in Figure 16 (left) consisted of a series of 100 μm by 100 μm square contact pads. The distance between each adjacent pair of pads was linearly increasing from 2 μm to 40 μm. The contact pads were deposited and patterned on the TLM sample using "mask1". The experimental procedures for fabricating ohmic pads were given in Section 3.2.2.

The photomask as shown in Figure 16 (right) was used for the formation of mesas that confined the current flow. With no current spreading, the pad resistances can be accurately measured. Once the metal pads were formed, a layer of positive photoresist was applied and lithographically patterned into mesas using "mask2". With this layer of photoresist as etch mask, the unprotected regions of sample were wet-etched down to the undoped InP substrate. Wet chemical etching was an adequate technique for removing the very thin layer of InGaAs semiconductor without suffering problems associated with low anisotropy. The

etch mixture consisting of sulfuric acid, hydrogen peroxide, and water (H_2SO_4:H_2O_2:H_2O) in ratio 1:1:50 was used. The height of the mesas was ensured to be at least the same thickness as the conducting InGaAs contact layer. The etch was selective for InGaAs and stopped naturally at the semi-insulating InP substrate 200 nm in below the surface.

3.2.3.2 TLM Equations

A constant current I_1 is passed through the first pair of pads immediately adjacent to each other, and the voltage drop is measured and recorded as V_1. Therefore, the total equivalent resistance between the two pads is given by $R_1 = V_1 / I_1$. This same measurement is repeated for the next eleven pairs of contacts and values of R_2, R_3 ... R_{12} are obtained. A linear line can be extrapolated from the averaged TLM data, as shown in Figure 17.

Three parameters: the sheet resistance, specific contact resistance and transfer length, can be extracted from the TLM graph. Assuming that the sheet resistance of the contact epilayer outside the contact area R_{sh} is the same as that beneath the contact area R_{sc}, then the total equivalent resistance between two adjacent pads R_e, is given by the sum of two contact pad resistances $2R_c$ and the resistance of the semiconductor layer between the two contact pads R_s, such that $R_e = 2R_c + R_s$.

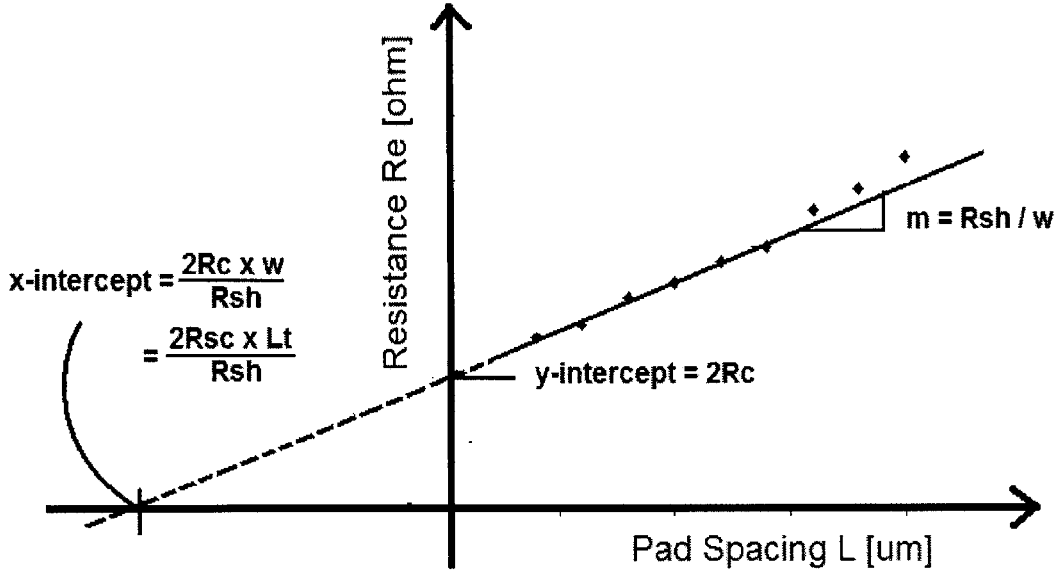


Figure 17 Graphical Analysis of Transfer Length Method
Three parameters can be extracted from this TLM graph: sheet resistance R_{sh}, specific contact resistance r_c, and transfer length L_t. Assuming that the sheet resistance of the contact epilayer outside the contact area R_c, is the same as that beneath the contact area Rs_c, then the total equivalent resistance between two adjacent pads R_e would be equal to $2R_c + R_s$.

The sheet resistance between the metal pads R_s is a function of its sheet resistance R_{sh}.

$$R_s = \frac{\rho L}{A} = \frac{\rho L}{tw} = \left(\frac{\rho}{t}\right)\left(\frac{L}{w}\right) = R_{sh}\left(\frac{L}{w}\right)$$, where

ρ = resistivity of InGaAs contact layer [Ω-cm],

L = pad spacing [μm],

w = width of contact pads [μm],

t = thickness of InGaAs contact layer [μm],

R_{sh} = sheet resistance [Ω/□].

Therefore, $R_e = 2R_c + R_{sh}\left(\frac{L}{w}\right)$.

Since R_e is plotted on the y-axis and L on the x-axis, the equation can be rearranged as:

$$R_e = 2R_c + \left(\frac{R_{sh}}{w}\right)L \Leftrightarrow y = b + mx$$

From the linear extrapolation of averaged data, several values can be extracted:

1) Sheet Resistance

The slope is $m = \left(\frac{R_{sh}}{w}\right)$, where w is the width of the contact pads.

The value of m is extracted from the TLM graph.

$\therefore$ Sheet Resistance $R_{sh} = m_{measured} \times w$ ■

2) Specific Contact Resistance

By setting $L = 0$, y-intercept = $2R_c$

Therefore, contact resistance is R_c = y-intercept / 2

The value of y-intercept is extrapolated from the TLM graph.

$\therefore$ Specific Contact Resistance $R_c = \frac{\text{y - intercept}_{measured}}{2} \times A_{contacts}$ ■

3) Transfer Length

By setting $R_e = 0$, x-intercept $= -\left(\frac{2R_c \times w}{R_{sh}}\right)$

Since $R_c = \left(\frac{R_{sc} \times L_t}{w}\right)$, x-intercept can be related to transfer length, L_t.

$|\text{x-intercept}| = \left(\frac{2R_c \times w}{R_{sh}}\right) = \left(\frac{2R_{sc} \times L_t}{R_{sh}}\right)$

The value of x-intercept is extrapolated from the TLM graph.

If the sheet resistance between the contacts R_{sh}, can be approximate as equaling to the sheet resistance of the material under the contact R_{sc}, then, |x-intercept| = $2L_t$.

$\therefore$ Transfer Length $L_t = \frac{\text{x - intercept}_{measured}}{2}$ ■

Note that additional data is needed in order to accurately determine the transfer length, $L_t = \sqrt{\frac{R_c}{R_{sc}}}$. The topic on transfer length measurement will not be discussed further in this thesis.

3.2.3.3 TLM Measurements of Cr/Au on p+ InGaAs Contact Layer

Since the doping level of the p-type InGaAs contact layer was relatively high ($N_A = 1 \times 10^{19}$ cm^{-3}), using an alloyed contact metal such as Au with a p-dopant layer, was not expected to be necessary [19]. For this TLM sample, the non-alloyed ohmic metals selected were 50 nm of chromium (Cr) and 200 nm of Au. The metal pads were sintered in order to reduce the associated contact resistances. All TLM experimental results including the pre- and post-anneal data, are provided in Appendix C.

A 370 Programmable Curve Tracer was used to measure the conductance between corresponding pads at room temperature. The current and voltage characteristics between all contact pads were observe to exhibit a linear behavior. Resistance measurements were carried out and data were obtained from a total of four rows. The linear averages are plotted as a function of contact pad spacing as shown in Figure 18.

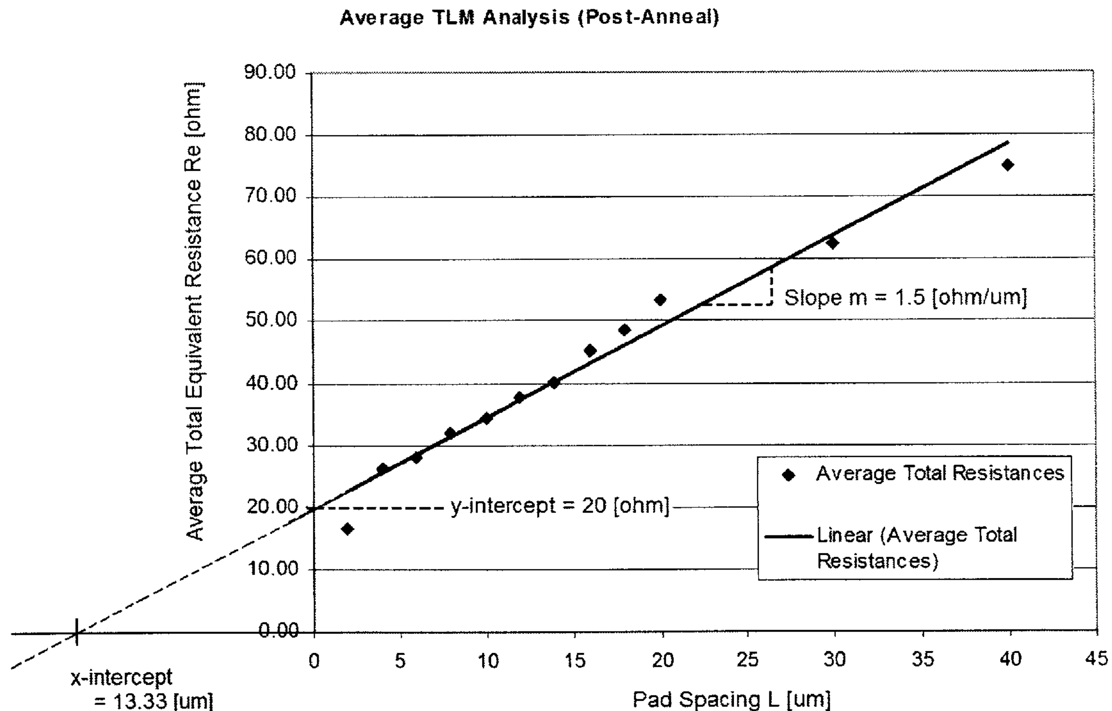


Figure 18 TLM Analysis of Cr/Au Contacts on Heavily Doped p-type InGaAs
This graph presents averages of resistance values obtained after an annealing treatment. The data were extrapolated using a linear computation method. Though only a minimal amount, the heat cycle reduced the contact resistance of the TLM sample from 11.25 Ω to 10 Ω. Sheet resistance and transfer length were also extracted from this graph. For pre-anneal results, refer to Appendix C.

Three parameters can be extracted as the following:

1) Measured slope $m \approx 1.5$ [Ω/□-μm]

   ∴ Sheet Resistance $R_{sh} = m \times w = 1.5$ [Ω/□-μm] x 100 [μm] = 150 [Ω/□] ■

2) Extrapolated y-intercept ≈ 20 Ω

   ∴ Measured Contact Resistance $R_c = 10$ Ω

   ∴ Specific Contact Resistance $r_c = R_c \times A_{contacts} = 10$ [Ω] x 100^2 [μm^2] = 10^{-3} [Ω-cm^2] ■

3) Extrapolated |x-intercept| ≈ 13.33 μm

   ∴ Transfer Length is L_t = |x-intercept| / 2 ≈ 6.7 μm ■

3.2.3.4 Theoretical Analysis of Cr/Au on p+ InGaAs Contact Layer

1) Sheet Resistance can be calculated from the resistivity ρ of InGaAs semiconductor

   $\rho = 1/\sigma = 1/\, q\, (\mu_n n + \mu_p p)$ [Ω-cm], where

   n = number of electrons [#/cm^3]

   p = number of holes [#/cm^3]

   μ_n = electron mobility [cm^2/V-sec]

   μ_p = hole mobility [cm^2/V-sec]

   q = electronic charge 1.60×10^{-19} [C]→[A-sec]→[V-sec/Ω]

Assuming all dopants were ionized at the room temperature (300K), the acceptor concentration, N_A, would be 1×10^{19} cm^{-3}. For this calculation, it is approximated that there were much fewer electrons than holes (n << p) in the heavily-doped p-type $In_{0.53}Ga_{0.47}As$ layer. Since $N_D \ll N_A$, the number of holes in the contact layer is therefore $p = N_A - N_D \approx N_A = 1 \times 10^{19}$ cm^{-3}.

From Figure 19, the hole mobility μ_p, of heavily doped p-type ($N_A = 1 \times 10^{19}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ is taken to be 100 [cm^2/V-sec] [20].

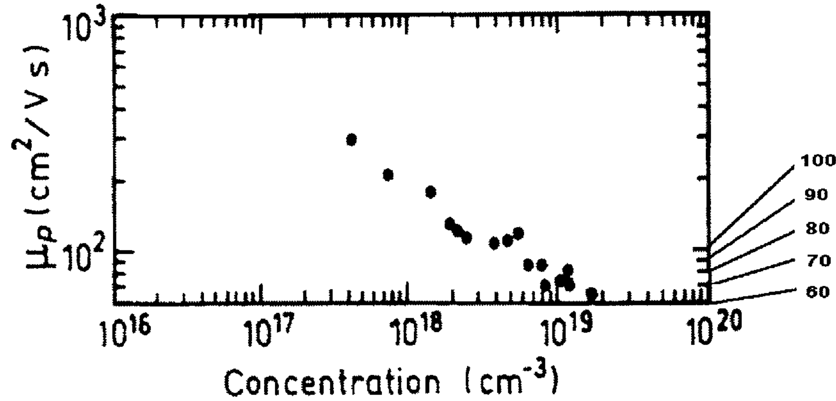


Figure 19 Hole mobility in $In_{0.53}Ga_{0.47}As$ as a Function of Doping Concentration
Measured hole mobility of $In_{0.53}Ga_{0.47}As$ at temperature (295 K) as a function of total impurity concentration $N_D + N_A$. For a p-type doping concentration of $N_A = 1 \times 10^{19}$ cm^{-3}, the hole mobility is taken to be approximately 100 [cm^2/V-sec]. Note that this value was read to be slightly higher in order to compensate for the electron carrier mobility, which was eliminated in the approximation.

Substituting in all values, the $In_{0.53}Ga_{0.47}As$ resistivity is calculated to be:

$$\rho_{InGaAs} = [q\,(\mu_n n + \mu_p p)]^{-1}$$
$$\approx [q\,(\mu_p p)]^{-1}$$
$$= [1.60 \times 10^{-19}\,(100 \bullet 1 \times 10^{19})]^{-1}$$
$$= 6.25 \times 10^{-3}\ [\Omega\text{-cm}]$$

Therefore, the sheet resistance of this heavily-doped p-type $In_{0.53}Ga_{0.47}As$ ($N_A = 2.0 \times 10^{19}$ cm^{-3}) is calculated to be $R_{sh} = (\rho/t) = 6.25 \times 10^{-3} / 2 \times 10^{-5} = 125$ [Ω/□]. The calculated sheet resistance value is close to that documented for an equally p-doped $In_{0.53}Ga_{0.47}As$ (with Ti/Pt/Au as the contact metallization), which was found to be 80.33 [Ω-cm^2] [21]. ■

2) <u>Specific Contact Resistance</u> of Cr/Au on p-type $In_{0.53}Ga_{0.47}As$ can be deduced from a variety of references. The specific contact resistance of a similar non-alloyed metallization (Ti/Pt/Au) on p-type $In_{0.53}Ga_{0.47}As$ ($N_A = 2.0 \times 10^{19}$ cm^{-3}) is reported to be 1.068×10^{-5} [Ω-cm^2] [21]. Based on this data point, the specific contact resistance of Cr/Au metallization on p-type $In_{0.53}Ga_{0.47}As$ ($N_A = 2.0 \times 10^{19}$ cm^{-3}) is approximated to be 10^{-5} [Ω-cm^2]. ■

3.2.3.5 TLM Results and Discussion

Table II summarizes the measured sheet resistance and specific contact resistance of Cr/Au metallization on a p-type $In_{0.53}Ga_{0.47}As$ layer with the theoretical and calculated values.

Table II TLM Measurements and Theoretical Values of Cr/Au on p-InGaAs

	R_{sh} [Ω/□]	r_c [Ω-cm^2]
Theoretical	80.33	10^{-5}
TLM Measured	150	10^{-3}

The sheet resistance of $In_{0.53}Ga_{0.47}As$ determines the amount of current flow in the contact layer. The measured sheet resistance agree closely with the theoretical value, which was less than two times smaller than what was obtained from the TLM characterization.

The quality of ohmic contacts is demonstrated by its specific contact resistance. A lower r_c value indicates a better ohmic contact. The measured specific contact resistance was two orders larger than the theoretical value. For the 100 μm by 100 μm contact pads, the resistance added to the circuit was 10 Ω. A lower contact resistance may be accomplished by a different metallization scheme.

Overall, good agreement was found in the measured and theoretical resistance values. The differences can be attributed to crude mathematical approximations, physical uncertainties, and instrumental errors. More work is to be done to better understand various ohmic contacts formations and to achieve lower contact resistances.

3.2.4 OptoPill Photodiodes and Discrete Photodiodes

Table III summarizes the n-type and p-type InGaAs layer dopings on three structures which were investigated, as well as their corresponding metallizations. The experimental results for the "OptoPill" and the "discrete" photodiodes are presented in Section 3.2.4 and Section 4.3 respectively.

Table III Contact Layers of TLM Sample, OptoPill, and Discrete Photodiodes

	TLM Sample	OptoPill Photodiode		Discrete Photodiode	
		N-Side UP	P-Side DOWN	P-Side UP	N-Side DOWN
Contact Layer Doping [cm^{-3}]	p+ InGaAs 1×10^{19}	n+ InGaAs 5×10^{18}	p+ InGaAs 5×10^{18}	p+ InGaAs 5×10^{18}	n+ InGaAs 5×10^{18}
Metal Scheme	Non-Alloyed Cr/Au	Non-Alloyed Ti/Au	Non-Alloyed AuSn on Cu	Alloyed AuZn (5%)	Non-Alloyed Ti/Au
Comments	Heavily doped dummy layer for characterization	Ohmic ring current output to Si-CMOS	Backside via Cu pad at bottom of recess (M2)	Ohmic ring on mesa for output measurements	Backside via top metal pads on InP substrate

The "discrete" and "OptoPill" photodiode heterostructures are shown In Figure 20. Special attention should be paid to the vertical orientation of the P-, i-, and N- layers of the diode device.

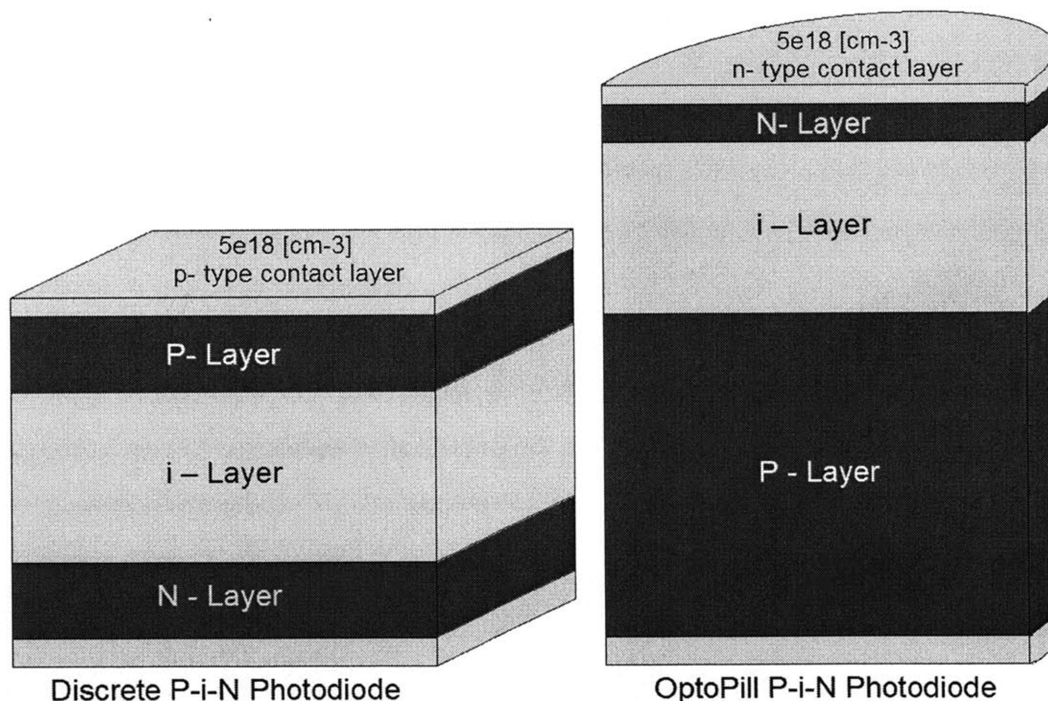


Figure 20 Illustrations of the Discrete and OptoPill P-i-N Photodiodes

The most important thing to take away from this picture is the vertical orientation of the P- and N-layers. The calibration sample was grown on n-type InP substrate, thus the discrete photodiodes had its P-side up and N-side as backside contact. The diode heterostructure used for RM^3 integration was also based on n-type InP bulk wafer. However, the fabrication of OptoPills effectively turns the structure up-side down, such that the N-side became the up-side that connects to the Si-CMOS circuit, and the P-side became the "bottom" backside contact. Note that all of the n- and p-type contact layers were doped with a carrier concentration of 5×10^{18} cm^{-3}.

Shown on the left is a "discrete photodiode" fabricated for characterization purposes. The P-i-N calibration sample was grown on an n-type InP substrate. The backside contact, or the

N-side of the mesa-type P-i-N photodiode, can be electrically accessed via simple, non-alloyed top metal pads that were deposited on the base substrate. The top side or the P-side of the photodiode can be accessed via an ohmic contact formed on the p-type InGaAs contact layer.

The diode heterostructure used for OPA integration, identified here as "OptoPill photodiode", was also grown on an n-type InP. However, the fabrication of OptoPills as described in Section 2.3.1 was designed in such a way that the manufactured P-i-N structures would be turned up-side down. Specifically, the N-side of the photodiode through which the device is electrically connected to external circuits by way of ohmic contacts, became the "up-side", and the P-side of the photodiode which was covered with AuSn metal stack and solder-bonded down on a Cu pad at the bottom of the recess, became the "down-side" of the device.

Note that both the n-type InGaAs contact layer of the OptoPill photodiode and the p-type InGaAs contact layer of the discrete photodiode were both doped with n-type and p-type carrier concentrations of 5×10^{18} cm^{-3} respectively. The p-type InGaAs layer of the TLM characterization sample was one-order more heavily doped with $N_A = 1 \times 10^{19}$ cm^{-3}. The differences in the type and concentration level of doping factor in the selection of ohmic metallization. Ohmic formation on "discrete photodiodes" will be discussed in Section 4.3.

3.2.5 Non-Alloyed (Ti/Au) Ohmic Contacts on n-InGaAs

Ohmic rings were formed on top of OptoPills to provide low resistance paths for the generated charge carriers to flow out of the photodiode device to external circuits. Ohmic contact rings were defined by standard liftoff technology described in Section 3.2.2.

A non-alloyed gold-based metal scheme consisting of titanium (Ti) and Au was adopted to manufacture the ohmic rings on the N-side of the InGaAs contact layer ($N_D = 5 \times 10^{18}$ cm^{-3}). Like Cr used in the TLM process, Ti acts as the adhesion promoter of Au to semiconductor. 20 nm of Ti and 300 nm of Au were evaporated by electron beam at 3.5 Å/sec and 3 Å/sec

respectively. The Ti/Au e-beam deposition process parameters are given in Appendix B.3. A SEM image of the ohmic ring is shown in Figure 21.

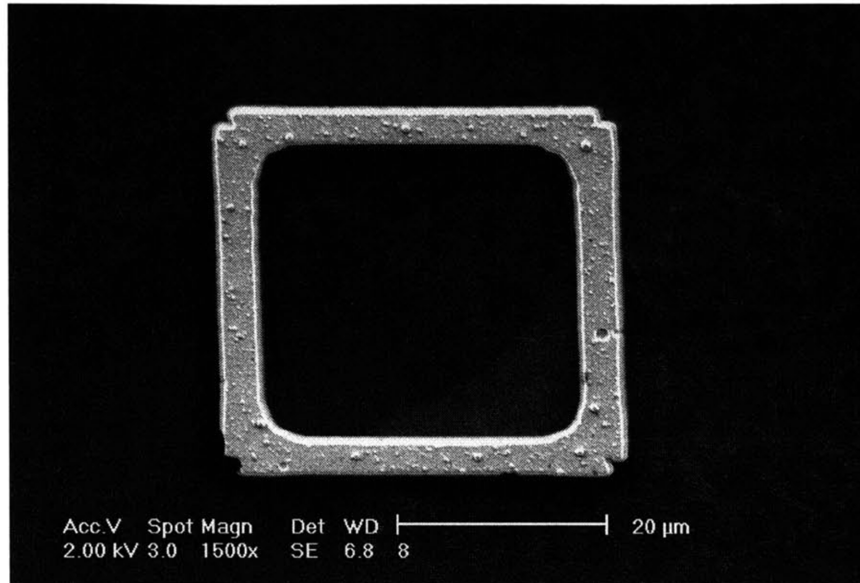


Figure 21 Ti/Au Ohmic Ring on Silicon
Silicon monitor pieces went through the same ohmic formation process. Shown here is an ohmic ring 40 μm by 40 μm in dimension, and 5 μm in width. The lithography resolution was found satisfactory for this process. Note the bubbling texture of the Ti/Au was the expected result of a sintering process.

The Ti/Au rings formed on the n-type InGaAs contact layer of OptoPill photodiodes were found to be ohmic. The doping concentration was sufficiently high $N_D = 5 \times 10^{18}$ cm^{-3} and the metallized rings were adequately sintered at 420°C for 10 seconds.

It has been reported that the Ti/Pt/Au metallization is non-ohmic on n-type $In_{0.53}Ga_{0.47}As$ of doping concentration lighter than $N_D = 2.7 \times 10^{18}$ cm^{-3}[21]. Ohmic contacts can only be obtained at a doping concentration higher than $N_D = 1.0 \times 10^{19}$ cm^{-3}, in which case the specific contact resistance was determined to be 0.55×10^{-6} [Ω-cm^2] [21]. On the other hand for wide bandgap InP semiconductor, Ti/Pt/Au ohmics can be formed with a lighter n-type concentration of $N_D = 2.0 \times 10^{18}$ cm^{-3}. The specific contact resistance was found to be on the order of 10^{-6} [Ω-cm^2] [23].

3.3 Active Area Definition by InGaAs/InP Etch with ECR-Enhanced RIE

3.3.1 Experimental

In order to confine current flow and define the active areas of the P-i-N photodiode, square-shaped grooves were etched through the n-type InP upper window of the heterostructure. The 40 μm by 40 μm groove pattern is shown in Figure 22.

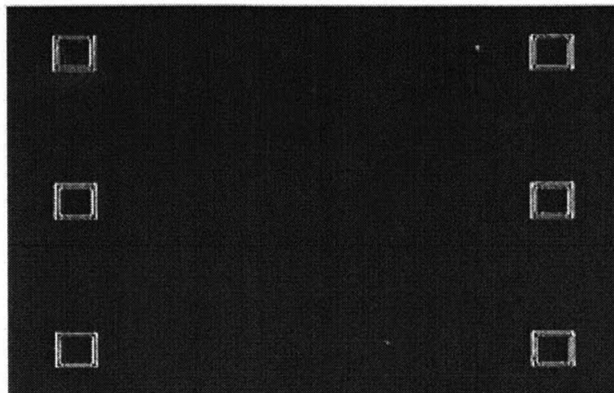


Figure 22 Mask "LED MESA" Pattern for OptoPill Active Area Definition
Groove rings are 40 μm by 40 μm. Picture was taken by Nikon BDPlan 20/0.4 (210/0) objective lens of a microscope station. A combination of soft and hard materials were used as etch masks in this process.

3.3.1.1 Mask Material Deposition and Patterning

The substrate heating characteristic of plasma etch processes necessitated the use of hard mask material, by which the lateral erosion and undesirable widening of grooves otherwise experienced with a soft resist mask were avoided. Although the number of processing steps was increased by the employment of a hard mask, the benefits attained, such as improved process control and higher throughput, were worthwhile. 0.5 μm of oxide was deposited on the sample by plasma-enhanced chemical vapor deposition (PECVD). After that, 1.5 μm of positive photoresist was spun on top of the oxide layer and lithographically patterned into grooves. With photoresist as the thicker soft mask, groove patterns were then transferred to the thinner oxide hard mask by reactive ion etching using CF_4 plasma, commonly known as Freon. The etch selectivity of oxide to photoresist is approximately 1:1. Detailed procedures and processing conditions for oxide growth using PECVD and oxide etch using RIE are given in Appendix B.2.

3.3.1.2 Dry Etch Chemistry

Although wet chemical etching is a simple technique that offers high selectivity, dry etching is more desirable for smaller features due to its high anisotropy and high controllability of etch characteristics. Smooth, residual-free dry-etching of InP-related materials has been reportedly successful with CH_4/H_2 etch chemistry. The incorporation of hydrogen alleviates the deposition of carbon-rich layers commonly seen when using methane. This organic-based gas mixture has a higher etch selectivity of semiconductor over common masking materials than the corrosive and environmentally unfriendly chlorinated (Cl-based) gases.

3.3.1.3 RIE and ECR Dry Etching

There are dry etch methods available in MTL, the conventional RIE as well as the Electron Cyclotron Resonance (ECR) plasma etching. In conventional RIE etching, increasing the RF biasing of the substrate increases the etch rate, but the high ion energies may introduce significant surface damage through ion bombardment, preferential etching of surface elements and hydrogen passivation of donors and traps.

The dry-etching of InP-based materials can also be achieved in ECR plasma etching. Microwave ECR is one type of dry etching that relies on magnetically enhanced discharges to provide high density plasmas with low self-biases. The name "electron cyclotron resonance" comes from the fact that free electrons orbit about the magnetic field lines while absorbing microwave energy in the plasma. The ion energies in an ECR plasma etch are less than the displacement threshold for damage in InP, InGaAs, and InAlAs, leading to a much lower level of damages than conventional RIE processes [27].

3.3.1.4 Process Conditions

"PlasmaQuest" is an electron cyclotron resonance (ECR) enhanced RIE system which is capacitively coupled with parallel plate electrodes. The process gases used were of 15/15 sccm of methane (CH_4) and hydrogen (H_2). The down-stream plasma was established at room temperature 25°C and 18 mTorr. The power levels were 275W of microwave power and 35W of RF power.

The etch selectivity of InP to the silicon oxide mask for this application was approximately 16:1 [28]. With 0.5 μm of oxide as the etch mask, approximately 0.4 μm grooves were etched through the InGaAs and InP layers of the OptoPills. Detailed processing conditions for InGaAs and InP etch using ECR-RIE are given in Appendix B.2.

3.3.2 Results and Discussion

The process using CH_4/H_2 chemistry for InP etching exhibited a very low etch rate of 0.05 μm per minute. It was difficult to control the uniformity of the etch profile by simple varying of the process parameters. The etching profile was examined by SEM as shown in Figure 23. Tilted at 60 degrees, the InGaAs/InP calibration sample shown underwent 60 minutes of CH_4/H_2 plasma-etch.

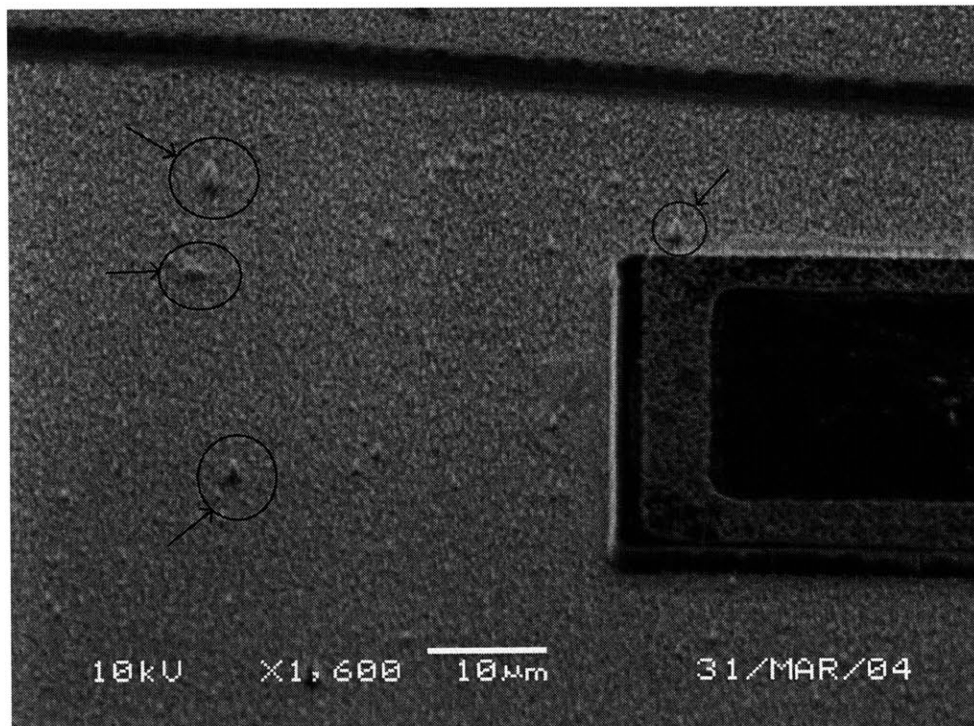


Figure 23 SEM Image of the Coarse Profile Dry-Etch InP Floor
The process conditions resulted in vertical profiles, but rough sidewalls and floor. Some of the larger coarse features are circled in the picture as shown. The dark line across the top of the picture was a scratch by the probe tip. The smooth profile underneath the scratch suggested the scraping of spiky structures off the coarse surface.

The InP sample underwent 60 minutes of CH_4/H_2 dry-etching and unfortunately, its surface indicated a "stucco-like" texture. An average roughness was measured to be about 0.5 μm. Such structures in III-V semiconductors caused by dry-etching plasmas can be created by lattice damage, chemical damage, and polymeric deposits, all of which have been shown to be harmful for the fabrication of optoelectronic devices [27]. In the present example, it was also evident that the etch chamber and wafer were subject to a significant amount of polymerization. These polymeric impurities which deposited onto the sample surface during the etch process act as sub-micron masking features while the high-energy ions continue to bombard the exposed InGaAs/InP semiconductor materials, giving rise to a very coarse etched surface.

3.3.2.1 Physical Sputtering

In order to avoid roughness it is necessary to remove the constituents of an alloy at equal rates. While hydrogen (H_2) behaves as a nearly pure chemical constituent, argon (Ar) behaves as a purely physical etchant. A smoother InP surface can be obtained by the bombardments from a beam of Ar+ ions, and the polymers can be physically etched or sputtered off as they are being deposited on the semiconductor surfaces. However, it may induce damage to the etch mask, and also cause the preferential loss of the lightest element, phosphide P in the case of InP, leaving In globules on the wafer.

3.3.2.2 Oxygen Plasma Dry-Etch Experiment

One other method to remove the carbon-induced particles is to introduce oxygen O_2. The O_2 plasma is commonly used to clean excessive hydrocarbon polymer generated by the CH_4 chemistry off the sample surface. As part of the $CH_4/H_2/O_2$ gas mixture, the optimal proportion of oxygen has been reported to range from 0.5% to 1.0% [29]. Further increase in the oxygen content would lead to excessive oxidation of the surfaces, resulting in surface roughness and very low etch rates.

Another technique is to cycle between the oxygen and the methane plasma-etch processes. To study the removal of surface roughness, dry-etch experiments with O_2 plasma have been

designed for InP dummy samples. A process characterized by 100W of RF power, 100W of ECR power, 30 sccm of O_2 at a pressure of under 22.5 mTorr has been reported to remove residual hydrocarbon after approximately twelve minutes [30]. The "etch-ash" sequence was designed to repeat every five to ten minutes intervals in order to remove polymer deposited during methane etches. The amount of polymeric residue on the wafer surface was to be periodically monitored through the experiment. Note that, the frequent plasma cleans significantly decreased the throughput. The designed dry-etch experiment is as shown in Table IV.

Table IV InGaAs/InP Dry-Etch Design of Experiment (25°C)

#	Gas Mixture	Flow Rate [sccm]	Power [W] RF / Microwave	Pressure [mTorr]	Time [min]	Predicted Etch Depth
1	CH_4 / H_2	15 / 15	35 / 275	18	10	0.5 μm
2	O_2	50	25 / 200	20	10	
3	CH_4 / H_2	15 / 15	35 / 275	18	10	1.0 μm
4	O_2	50	25 / 200	20	10	
5	CH_4 / H_2	15 / 15	35 / 275	18	10	1.5 μm
6	O_2	50	25 / 200	20	10	
7	CH_4 / H_2	15 / 15	35 / 275	18	10	2.0 μm
8	O_2	50	25 / 200	20	10	
9	CH_4 / H_2	15 / 15	35 / 275	18	10	2.5μm
10	O_2	50	25 / 200	20	10	

3.3.2.3 Oxygen Plasma Dry-Etch Results

Actual dry-etch processing and experimental results obtained are summarized in Table V.

Table V InGaAs/InP Dry-Etch Experimental Results (25°C)

#	Gas Mixture	Flow Rate [sccm]	Power [W] RF / Microwave	Pressure [mTorr]	Time [min]	Actual Etch Depth
1	CH_4 / H_2	15 / 15	35 / 275	18	5	0.55 ~ 0.62 μm
2	O_2	50	25 / 200	20	10	
3	O_2	50	25 / 200	20	10	
4	O_2	50	5 / 400	20	10	

First, the InP sample was ECR-etched with 15/15 sccm of CH_4/H_2 using 275W of microwave power and 35 W of RF power at a pressure of 18 mTorr. After five minutes, the etched depth was measured by a Dektak stylus profilometer. As predicted, the etched mesa height ranged between 0.5 μm to 0.6 μm. The same surface roughness shown in Figure 23 was observed.

Then, oxygen plasma was used with hopes to burn the deposited polymers off the sample surface. Note that the etch selectivity of the oxide mask to InP was approximately 1:16 for this combination of ECR and oxygen plasma etches. The wafer was treated by 50 sccm of oxygen at 200 W of microwave power and 25 W of RF power, and the plasma was established at room temperature 25°C under 20 mTorr of pressure. After ten minutes of oxygen plasma-etch, the surface roughness did not seem to improve. This step was then repeated for ten more minutes under original etch conditions. Since ECR etching yields a more smooth morphology, after seeing yet no signs of improvement on surface roughness, the InP wafer was then treated with ten more minutes of oxygen plasma at higher level (400 W) of microwave power and only 5 W of RF power. Unfortunately, the smoothness of the etch profile did not seem to improve still. Further work needs to be done in order to develop a better dry-etch process for InGaAs and InP-related semiconductors.

Aside from polymeric contaminants, possible damaged layers are reportedly removable by a wet chemical-etching process after RIE. Several etch chemistries have been documented as successful, including a combination of NH_4S_x and H_2SO_4 [31] prior to MOVPE InP regrowth, and H_3PO_4:H_2O_2:H_2O (1:1:150) [32] for HEMTs fabrications.

3.4 BCB Passivation and Planarization

Following ohmic ring formation and active area definition, the Si-CMOS chip surface was planarized and passivated with a protective layer. Passivation is an important step of the post-assembly process aimed at reducing the diode dark current. The "dark" current is a thermally generated current that flows in a reverse-biased diode even when no light is present. It is highly undesirable since it "leaks" past the p-n junction barrier while statically discharging the node capacitance. In a state with no optical excitation, the dark current or leakage current gives rise to noise in photoreceivers. In addition, the leakage current of an unprotected junction would increase drastically over time, deteriorating the photodiode in due course. The passivation layer prevents the leakage path from forming, and protects the device junction against eventual degeneration in exposed environment.

The other important purpose of this post-assembly process step is wafer replanarization. The wafer surface must remain planar throughout the integration process in order for conventional lithographical tools to perform high-resolution patterning of the vias and top metal interconnects. In addition, a smooth surface over the dielectric layers is necessary for the formation of continuous and conformal top-level metal interconnects. It also protects the heterostructures from the roughness of subsequent processing, and helps secure them in the recesses.

Benzocyclobutene (BCB) is a low dielectric constant polymer that has been used extensively in microelectronic packaging and interconnect applications. More important than its high optical clarity and good thermal stability, BCB was chosen for this RM^3 optoelectronic integration process primarily due to its excellent degree of planarization and passivation properties. Other desirable properties of BCB for GaAs and InP integrated circuits processing are low curing temperature, low water absorption, rapid curing, and low viscosity.

BCB is an attractive alternative to hard oxide for both its excellent passivating properties and planarizing capabilities. Moreover, it is difficult to grow oxide to suitably passivate III-V junctions, and BCB has been reported to be a good passivation material for InGaAs/InP

junctions [33]. Furthermore, the viscous BCB is much more proficient at filling deep gaps than is oxide. As illustrated in Figure 24, deep grooves formed in-between the side of an OptoPill and the walls of recess can be easily filled by spin-on BCB films.

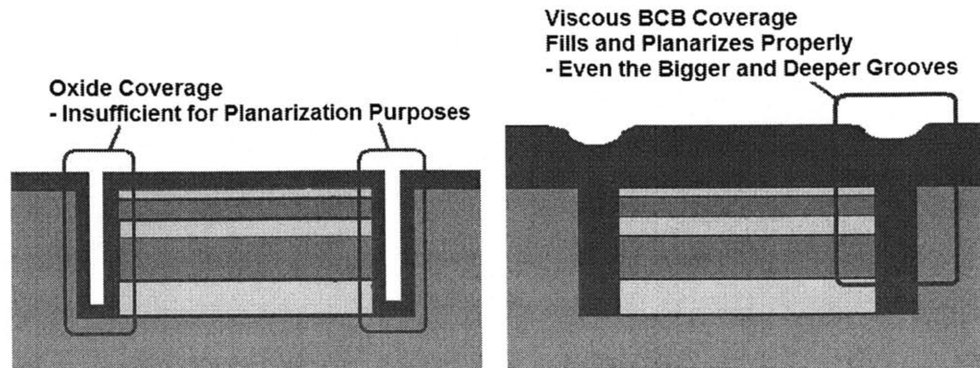


Figure 24 BCB as Planarization Layer Compared with Oxide Mask
As illustrated on the left, an oxide layer covers all parts of the sample, but it is insufficient at filling and planarizing deep grooves. On the right hand side, viscous BCB properly fills deep gaps on the wafer, leaving a highly planarized surface topology.

3.4.1 Experimental

BCB can be easily applied to the wafer by spin-on techniques. An adhesion promoter (AP3000) was first applied, after which the excess on the sample was gently blown dry with an N_2 gun. The BCB polymer was dispensed and spin-coated onto the Si-CMOS wafer. At spin speed of 5 krpm, the minimum BCB thickness after curing would be slightly over 1 μm. Edge bead removal and back side substrate clean can be done with the T1100 solvent

Curing increases resistance of the polymer films to subsequent processing operations. Since the BCB resins are susceptible to oxidation at elevated temperatures, the film must be under an inert atmosphere at high temperatures. Therefore, the curing step was done in the absence of oxygen (< 100 ppm) at a temperature higher than 150°C.

The film can be cured with a variety of tools. In this process, the BCB dry-etch films were cured using an RTA whose enclosed dome was flushed with forming gas. The temperature profile is shown in Figure 25.

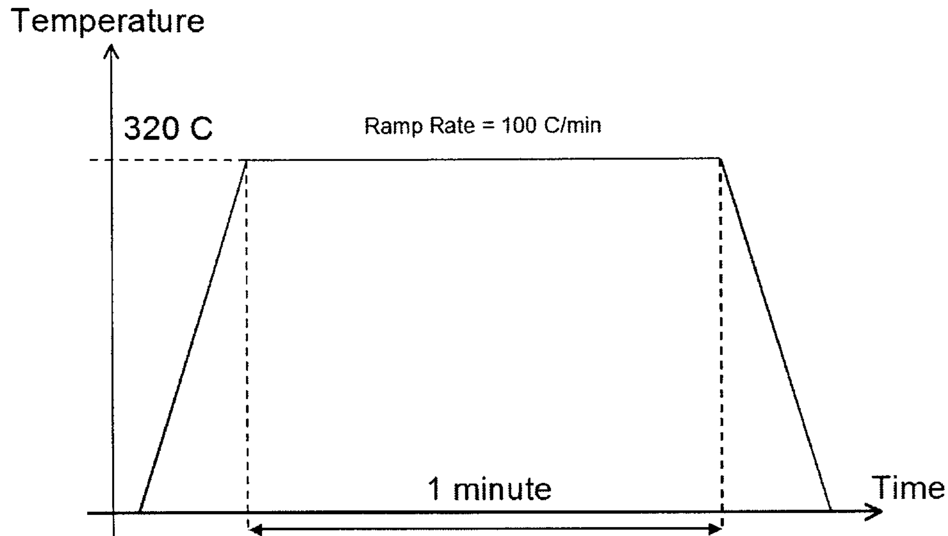


Figure 25 BCB Curing Temperature Profile in Rapid Thermal Annealer
The temperature profile used for curing BCB at a rapid thermal annealer flushed with forming gas. Curing was done immediately after BCB application and between successive layers of coating. Optimal curing condition was found to be 320°C for 1 minute, with the temperature ramp rate being 100°C/minute.

It has been suggested that the BCB films be soft cured between successive coats of the resin to enhance adhesion of the subsequent layers. After the final layer is deposited, a hard cure longer in time and higher in temperature is recommended to achieve a higher degree of polymer conversion.

3.4.2 Results and Discussion

Extensive experiments found that multiple layers of the thinner, dry-etch grade BCB gave better planarization result than one layer of thick, photo-sensitive grade BCB. As such, the gaps and grooves of the chip were sufficiently filled without the excessive film thickness.

The SEM images in Figure 26 show BCB coverage of 8 μm deep and 5 μm wide grooves created in a silicon dummy substrate. With two coatings of dry-etch grade BCB, a nearly planar (>95%) surface was achieved. Thus, it can be corroborated that BCB exhibits an excellent degree of planarization.

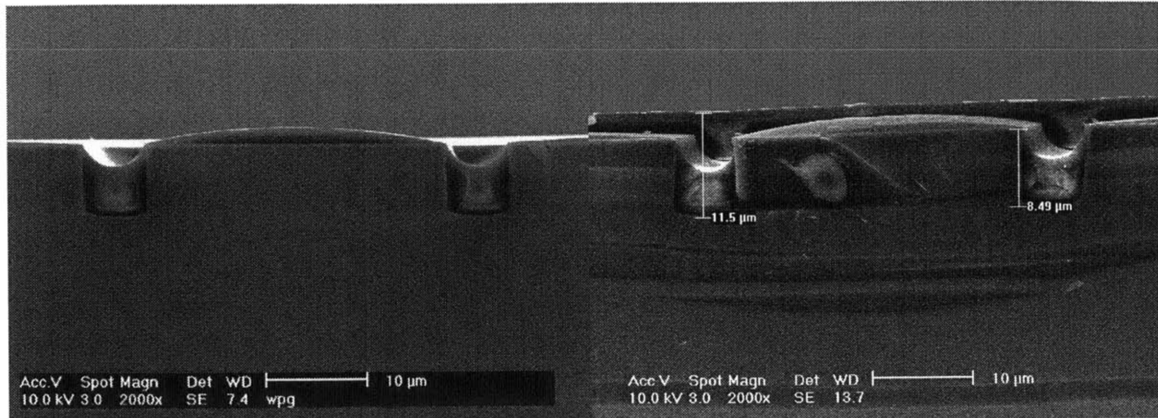


Figure 26 Cross Section of one and two layers of BCB over Grooves
The SEM images show the photosensitive grade (4024-40) BCB covering 8 μm deep and 5 μm wide grooves. The deep grooves were patterned and etched using STS-1 plasma etcher for 20 minutes. After removal of the positive photoresist etch mask, BCB was spun-on the substrate at a maximum spin speed of 5 krpm. Two layers of BCB as shown on the left image sufficiently filled the deep grooves and planarized the wafer surface. After softbaking, the solvent content in the BCB films was reduced and the final thickness was decreased to 3 μm.

3.5 Via Opening by BCB Etch with RIE

By dry-etching BCB, vias were created in the passivation layer to expose the contact pads of the CMOS chip and also the ohmic ring that connected to the N-side of the OptoPill heterostructure. See Section 4.6 for pictures of the mask pattern and a silicon dummy sample which was processed up to this step.

With thick photoresist as the etch mask, the BCB layer was plasma-etched by RIE. Compared to inductively coupled plasma (ICP) source, the lower process pressure of RIE gives an improved control over anisotropy. However, lower pressure results in lower ion density, therefore, a high degree of anisotropy was achieved at the cost of lower BCB etch rates. Alternatively, a hard mask can be used for higher resolution work.

The plasma used to etch BCB contains oxygen and a fluorine-containing gas. The fluorine component cleanly etches the silicon part in the backbone of the dry-etch grade BCB materials. Mixtures of SF_6/O_2, CF_4/O_2, or CHF_3/O_2 yield controlled BCB etches at rates greater than 1 μm per minute using parallel-plate or reactive ion plasma etchers [34].

The etch gas mixture selected for this process was 10/90 sccm of Freon (CF_4) and oxygen (O_2) respectively. The etch selectivity of the 3000 series dry-etch grade (3022-35) BCB resin to the thick photoresist (AZP 4620) mask was 0.7:1 [35]. Note here that the photoresist etches 1.4 times faster than BCB. For this application, the resist used was approximately 10 μm in thickness, while the BCB films ranged from 1 μm to 3 μm. By calculation and also by experiments even at a high oxygen flow rate, the soft mask was proven to be of sufficient thickness for BCB etch.

Under the etch conditions of 200 mTorr and 150 W of RF power, the etch rate of BCB using RIE was calibrated to be approximately 0.7 μm per minute. Detailed dry-etch processing conditions of BCB are provided in Appendix B.3.

3.6 Ti/Au Top Metallization

Top metallization is the last step for post-assembly process as well as the OEIC integration flow. After etching selective areas in the BCB layers, Ti/Au contact pads were deposited and patterned to electrically connect the OptoPill photodiode device to the Si-CMOS electronic circuit. The Ti/Au e-beam deposition process parameters are given in Appendix B.3.

A smooth and planar surface as a result of BCB planarization, plus wide via angles as a result of proper BCB dry-etching, were both demonstrated in the previous steps for the successful formation of continuous metal lines on the topmost layer, which were critical for the robust performance of the final optoelectronic integrated circuit. Top metallization was demonstrated to be successful on a silicon dummy sample that underwent the entire fabrication process. For further discussion on this topic, refer to Section 4.7.

4 Discrete InP-Based P-i-N Photodiodes

The procedures used to fabricate InP-based photodiodes are direct derivatives of the technology developed for the post-assembly processes. Diode fundamentals and discrete InGaAs/InP P-i-N photodiodes are discussed in Section 4.1. Then, the overall process flow is illustrated in Section 4.2. Materials and processing as applicable in each step are reviewed in Section 4.3 through Section 4.7. A schematic of the final structure is shown in Section 4.8. Lastly, preliminary characterization of the photodiode prior to BCB passivation is discussed in Section 4.9.

4.1 Fundamentals

A diode junction is formed when an N-type and a P-type semiconductor are joined together. This nonlinear device is said to be "reverse-biased" when the voltage applied to the n-region is higher than that of the p-region, and the opposite is true for forward-bias. An ideal diode is essentially a voltage controlled current source that allows current flow from the p-side to the n-side only when forward-biased, and no current flow if reverse-biased.

In reality, however, there exists a small current that flows from the n-side to the p-side of a reverse-biased diode junction. This current consists of two components: the thermally excited electron-hole pairs (EHPs) generated in the junction space charge layer or the depletion region, and minority carriers in the two quasi-neutral regions that diffused to the edges of the space charge layer, which are swept across it. The resulting current is known as the reverse saturation current, or the generation current.

The current-voltage coordinate system is defined as follows: the positive direction of the y-axis defines a current that flows from the p-side to the n-side, and the x-axis plots the voltage value applied to the p-side with respect to the n-side of the junction. A photodiode is effectively a junction diode operating in the third quadrant of its I-V characteristics, where

the photodiode is reverse-biased ($V<0$) and the current is flowing in the "negative" direction. In this regime, power is delivered to the photodiode by an external circuit.

Excess carriers in a photodiode are created by optical excitation. When light is incident on the active area, photons with energies greater than the bandgap of the intrinsic semiconductor layer are absorbed. Upon optical absorption, an electron is excited to the conduction band thus creating an EHP. The excess electron and hole in their respective bands increase photoconductivity by giving off energy to the lattice in scattering events, until they eventually recombine to return to thermal equilibrium. Like the thermally generated current, the optically generated current is also independent of applied bias voltage. Both the reverse saturation current and the photocurrent flow from the n-side to the p-side of the junction, contributing to the total current flow in the negative direction. The current-voltage curves are therefore shifted downwards with an amount of lowering that is directly proportional to the optical generation rate.

As illustrated in Figure 27, the P-i-N photodiode is a two terminal device constructed with a wide bandgap p-type top contact layer, a wide bandgap n-type bottom contact layer, and an undoped (i.e. intrinsic) narrow bandgap layer that is sandwiched in-between. Device sensitivity and speed are improved in this geometry because all of the light is absorbed and the EHPs are created in the high field depletion region that covers the entire i-layer. The width of the depletion region is directly controlled by the thickness of i-layer grown.

InP-based photodetectors with InGaAs as the intrinsic active layer are naturally suited for long distance fiber-optic communications of 1.3 μm and 1.55 μm wavelengths, and they can have very low dark current (high sensitivity) and very efficient absorptions (high responsivity) [36].

Figure 27 Cross Section of an InP-Based P-i-N Photodiode
The P-i-N photodiode structure as shown in this schematic consists of a wide bandgap p-type InP top contact layer (as shown near the top of the device), a wide bandgap n-type InP bottom contact layer (as show near the bottom of the device), and an undoped, intrinsic InGaAs narrow bandgap layer that is sandwiched in-between. InGaAs/InP photodiodes are naturally suited for fiber optic communication applications, and for this reason, they were selected in this research project as the detectors for optical clock distributions.

Like the heterostructures used for OptoPill fabrication, the photodiode calibration sample was also grown by Professor Fatt's group at NangYang University, Singapore. The layer sequence of the InP-based photodiode used for the calibration processes is summarized in Table VI. Mesa-type photodiodes are created by etching the calibration sample down to the InGaAs etch stop layer, yielding a device height of more than 2.35 μm.

Table VI Epitaxial Layer Design of the Discrete InP-Based P-i-N Photodiode

Thickness	Layer	Type	Doping [cm^{-3}]
0.2 μm	InGaAs Contact Layer	p+	5 x 10^{18}
0.5 μm	InP Buffer	P+	5 x 10^{18}
0.05 μm	InP Spacer	undoped	--
1.1 μm	InGaAs intrinsic Layer	undoped	--
0.05 μm	InP Spacer	undoped	--
0.25 μm	InP Upper Window	N+	5 x 10^{18}
0.2 μm	InGaAs Contact and Etch Stop	n+	--
0.5 μm	InP Buffer	N+	5 x 10^{18}
N+ InP (100) substrate			

4.2 Fabrication Process Flow

InGaAs/InP photodiodes were fabricated in conjunction with the development of post-assembly processes. The purpose of fabricating these discrete P-i-N photodiodes is to independently understand and characterize their electrical and optical behaviors. The diode calibration sample closely resembled the diode structure used in the actual OPA integration process, except for the fact that the integrated devices were inverted with their P-side down and N-side up. Nonetheless, data measured from this photonic structure will be very useful for the final analysis of the integrated photodetector in the Si-CMOS optical clock distribution circuit.

The epilayer sample was first cleaved into smaller specimens approximately 1 cm by 1 cm. As illustrated in Figure 28, the process transforming InP-based heterostructures into discrete P-i-N photodiodes began with the formation of AuZn (5%) ohmic rings on the p-type InGaAs contact layer. Then, mesas were defined and isolated from each other using reactive ion etching. The surface of the wafer piece, which acted as the anodes of the photodiodes, was planarized and passivated with BCB layers. Next, vias were etched through the polymer film to expose the ohmic contact of the photodiode and also the underlying substrate for backside contacts. Finally, the top-level metallization was formed with Ti/Au using e-beam deposition and lift-off.

The entire process developed for the fabrication of discrete photodiodes was first carried out on silicon dummy pieces before applying the techniques to the actual calibration sample. The SEM images shown up to Section 4.5 were of the InP-based device heterostructures, and the pictures shown in Section 4.6 and Section 4.7 were of the Si dummy sample.

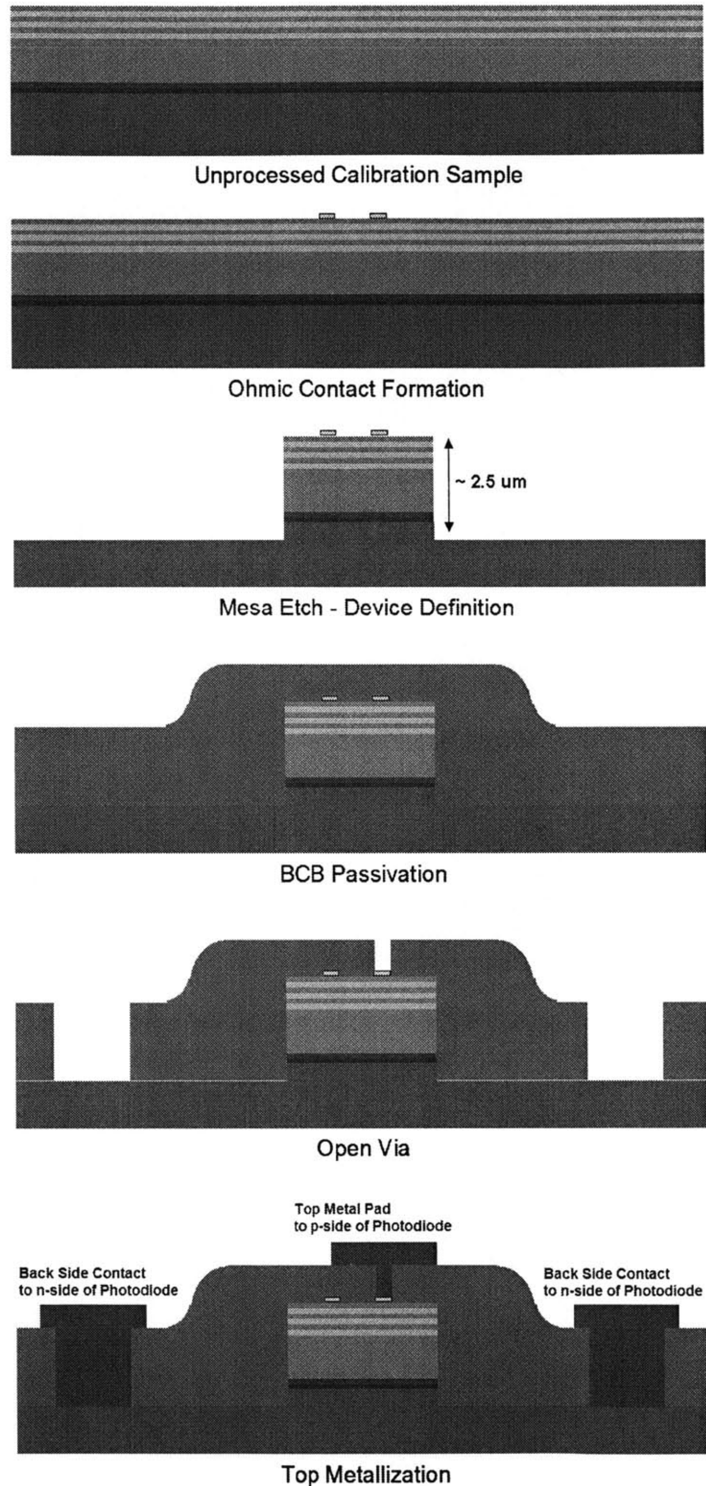


Figure 28 Complete Process Flow for InGaAs/InP Photodiode Fabrication
Photodiode fabrication process began with the formation of AuZn (5%) ohmic rings on the P-side of the heterostructure. The mesas were then isolated using reactive ion etching. The surface of the wafer piece and the anodes of the photodiodes were planarized and passivated with BCB layers. Vias were etched through in the polymer film to expose the ohmic contact of the photodiode and also the underlying substrate. Finally, the n-side metallization was formed with Ti/Au using e-beam deposition.

4.3 Alloyed (AuZn) Ohmic Contacts on p-InGaAs

It is easier to achieve low-resistance ohmic contacts on n-type InP than on p-type InP [16]. The calibration sample used for discrete photodiode fabrication was grown on an n-type InP substrate. The two-sided device was connected at the substrate via a simple n-type ohmic contact, and at the up-side contacting semiconductor layer via a p-type InGaAs contact formed in the neighborhood of the active layer.

The backside contacting to the N-side of the P-i-N photodiode was formed by depositing, patterning, and sintering Ti/Au pads directly onto the n-type InP substrate. This process utilizes the same material and procedure as that of the ohmic ring formation on the top N-side of the OptoPill photodiodes.

For contacts on the front or P-side of the photodiode, initial attempts to use Cr/Au or Ti/Au as ohmic contacts were found to unsuccessful. This negative result was confirmed by a reference in which the Ti/Pt/Au metallization on p-type $In_{0.53}Ga_{0.47}As$ ($N_A = 5.0 \times 10^{18}$ cm^{-3}) was reported to be non-ohmic [21]. As discussed previously, a high doping concentration is both favorable and necessary for the formation of low-resistance ohmic contacts. The doping concentration of the p-type InGaAs contact layer in the photodiode calibration sample was two orders of magnitude lower than the TLM characterization sample. From this experiment, it was concluded that the doping concentration $N_A = 5.0 \times 10^{18}$ cm^{-3} in the p-InGaAs contact layer was too low for the formation of non-alloyed ohmic contacts.

A high net hole concentration at the p-type InGaAs semiconductor surface is needed to achieve very low resistance, non-alloyed ohmic contacts. However, many problems arise at such high impurity concentrations, such as the diffusion of the acceptor dopants during epitaxial growth, which may lead to electrical compensation of adjacent layers, displacements of p-n junctions, or other detrimental effects [24].

The doping levels can be augmented with post-growth diffusion of dopant species into the semiconductor. Therefore for this application, an alloyed contact material with a p-type dopant, specifically Au with 5% zinc (Zn), was chosen as the p-contact material. AuZn

ohmic metal on p-type InGaAs epitaxial layer is documented to yield low specific contact resistances and sheet resistances. The specific contact resistance of AuZn contact metallization on p-type InGaAs was reported to range from 1×10^{-5} to 5×10^{-5} [Ω-cm^2] [25]. Comparatively, for contacts formed on wide bandgap p-type InP ($N_A = 2.0 \times 10^{18}$ cm^{-3}), the AuZn metallization was reported to yield a lower resistance value of 10^{-6} [Ω-cm^2] [26].

4.3.1 Experimental

AuZn ohmic contacts were formed on the discrete photodiodes by photoresist lift-off as described in Section 3.2.2, and the pattern of ohmic rings is illustrated in Figure 29.

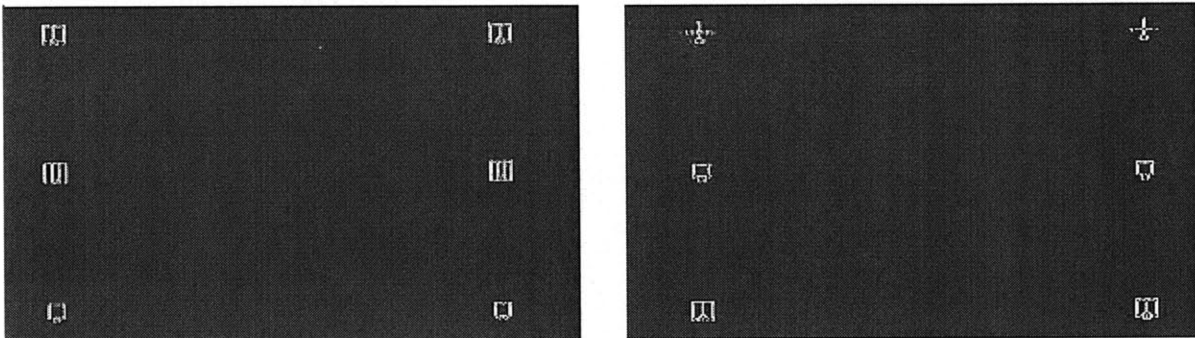


Figure 29 Ohmic Ring Mask

Image reversal photoresist was used to transfer the ohmic ring pattern to the InP-based sample. Since the resist of choice was negatively-acting, a light field mask was used. For visual clarity, shown here is a reversed polarity of the ohmic ring mask. The resist in the background (which would be the light field) was exposed to the UV rays and became insoluble. This part remained on the sample after photo step, whereas the photoresist in the dark field of ohmic patterns were flood-exposed and developed away,. The contact semiconductor layer underneath was exposed and ready for metal deposition.

A heat treatment was needed to provide sufficient thermal activation energy for Zn p-dopants to diffuse into the InGaAs top contact layer, acting as acceptors in the p-type semiconductor. To optimize the quality of AuZn contacts, samples were annealed for a variety of times and at different temperatures. First, they were first annealed at 400°C for 30 seconds, but no ohmic was formed and the results were unsatisfactory. Then, the AuZn metal was alloyed at a higher temperature 440°C for 30 seconds, and consequently, ohmics were formed on the heavily doped p^{++} metal-semiconductor interfacial layer. Annealing it yet again under the same conditions reduced the contact resistance. The i-v measurements to calculate contact resistance is presented in Section 4.3.2.

4.3.2 Results and Discussion

Although TLM measurements were not performed for these contacts, current-voltage characteristics of the AuZn contact on p-InGaAs were measured. The test setup is illustrated in Figure 30. A current was passed through two probe tips, and the conducting path would experience the resistance due to two AuZn contact pads and 200 μm of InGaAs semiconductor medium. The cross sectional area of the conducting path is the width of the contact pads w, multiplied by the thickness of the contact layer *t*.

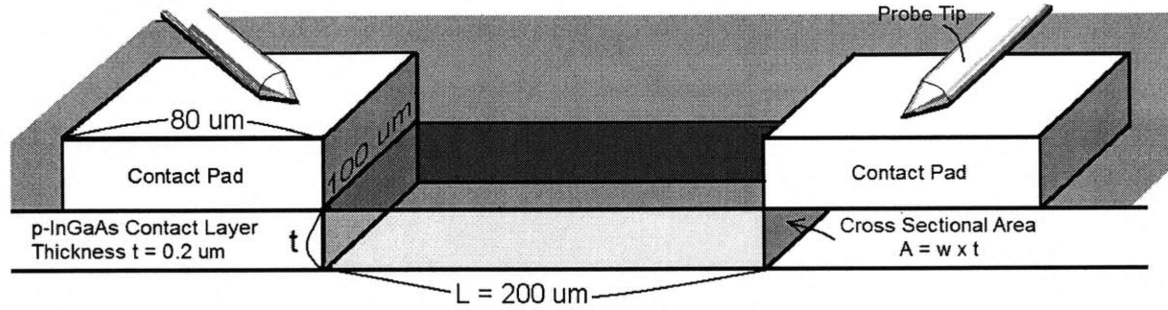


Figure 30 Test Setup for AuZn Ohmic Contact Resistance Characterization

Current was passed through two ohmic metal pads with dimensions as illustrated. For R_c calculation, the total area of two contact pads is $A_{contacts}$ = 2 x 80 μm x 100 μm. For R_{sh} calculation, the cross sectional area of the current path is $A = w \times t$ = 100 μm x 0.3 μm, and the length of the current path is the distance between two pads, L = 200 μm.

4.3.2.1 Theoretical Calculations

The resistance due to the contact pads is $2R_c = \frac{r_c}{A_{contacts}} \approx \frac{10^{-5}}{1.6\times10^{-4}} = 0.16\,\Omega$, where $A_{contacts}$ is the area of two contact pads: 2 x 80 μm x 100 μm = 16000 [μm^2] = 1.6 x 10^{-4} [cm^2]. The resistance due to the InGaAs contact semiconductor is $R_s = \frac{\rho L}{A} = \frac{\rho L}{tw} = \left(\frac{\rho}{t}\right)\left(\frac{L}{w}\right) = R_{sh}\left(\frac{L}{w}\right)$, where L is the variable pad spacing (200 μm), w is the width of contact pads (100 μm), t is the thickness of the InGaAs contact layer (0.2 μm), and R_{sh} is the sheet resistance (80 [Ω/□] [21]). Therefore, $R_s = R_{sh}\left(\frac{L}{w}\right) \approx 80\left(\frac{200}{100}\right) = 160\,\Omega$. Recall that the total equivalent resistance R_e is equal to $2R_c + R_s$. Since $2R_c$ is negligibly small compared to R_s, R_e is dominated by R_s and $R_e \approx 160\ \Omega$. ■

4.3.2.2 I-V Characteristics Measurements

The resultant current-voltage curve of the ohmic contact is shown in Figure 31. Clearly, AuZn metal on this relatively lightly-doped InGaAs contact layer exhibited linear i-v behavior. The linearity indicates that the AuZn contacts were ohmic. As mentioned earlier in this section, the anneal process was observed to enhance the integrity and behavior of the AuZn contact metallization.

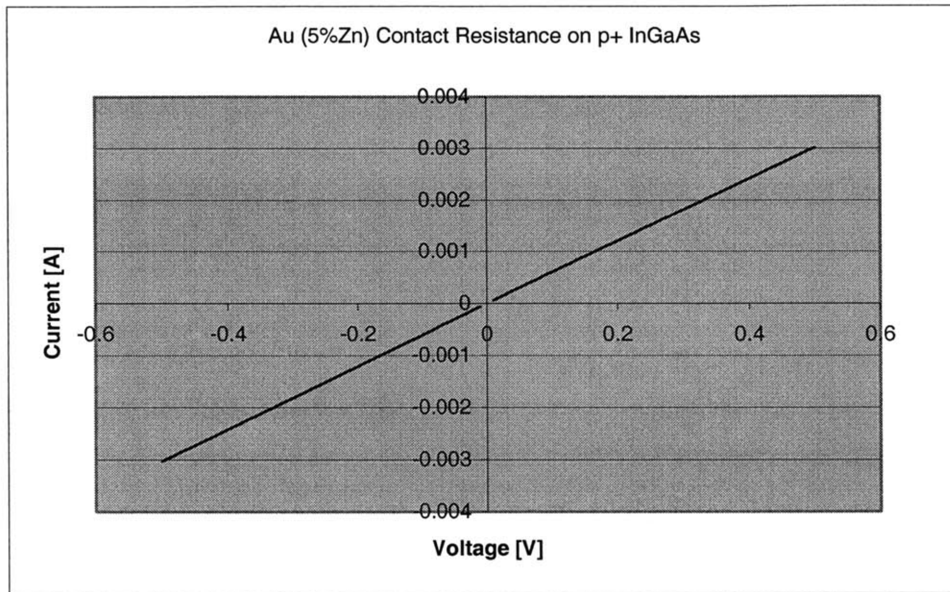


Figure 31 AuZn on p+ InGaAs Contact Layer I-V Curve
Non-alloyed, gold-based metal with 5% Zinc as the p-type dopant source, were formed on the p-InGaAs contact layer of the InP-based P-i-N photodiodes. The linearity of the current-voltage graph demonstrated that the contacts were ohmic. The resistance can be extracted from the measured characteristics where R = V / I = 167 Ω.

From the current-voltage curve, the equivalent resistance between the two contact pads was measured to be $R_e = \frac{1}{6}\left[\frac{V}{mA}\right] = 167\,\Omega$. ■

4.3.2.3 Summary

Table VII summarizes the theoretical and measured value of the AuZn ohmic pads on the p-type InGaAs contact layer of the discrete photodiode.

Table VII Theoretical and Measured AuZn Contact Resistance on p-InGaAs

	Equivalent R_e
Theoretical	160 Ω
Measured	167 Ω
% Error	4.4 %

In conclusion, the AuZn (5%) metal rings formed on p-InGaAs with $N_A = 5 \times 10^{18}$ cm^{-3} were found to be ohmic. The equivalent resistance between two ohmic pads was measured from its linear current-voltage curve and had a value of 167 Ω. The theoretical value was calculated as 160 Ω. The percentage error is $\frac{|\,Measured - Theoretical\,|}{Theoretical} \times 100\%$. The measured value agrees closely with the theoretical value with only a small deviation of 4.4 %. Overall, AuZn as ohmic contact metal was a satisfactory choice for the fabrication of the P-i-N calibration sample under consideration.

4.4 Mesa Isolation by InGaAs/InP Etch with ECR-Enhanced RIE

4.4.1 Experimental

This step of discrete photodiode fabrication is analogous to the groove etch developed in post-assembly processing, explained in Section 3.3. As illustrated in Figure 32, the mesa etch procedure involved several steps: 1) oxide mask deposition, 2) coating and patterning of the photoresist on top of the oxide mask, 3) transferring of the mesa pattern from the photoresist to oxide mask by dry etching, 4) InGaAs/InP mesa etching with oxide as the mask, and 5) removal of the oxide mask.

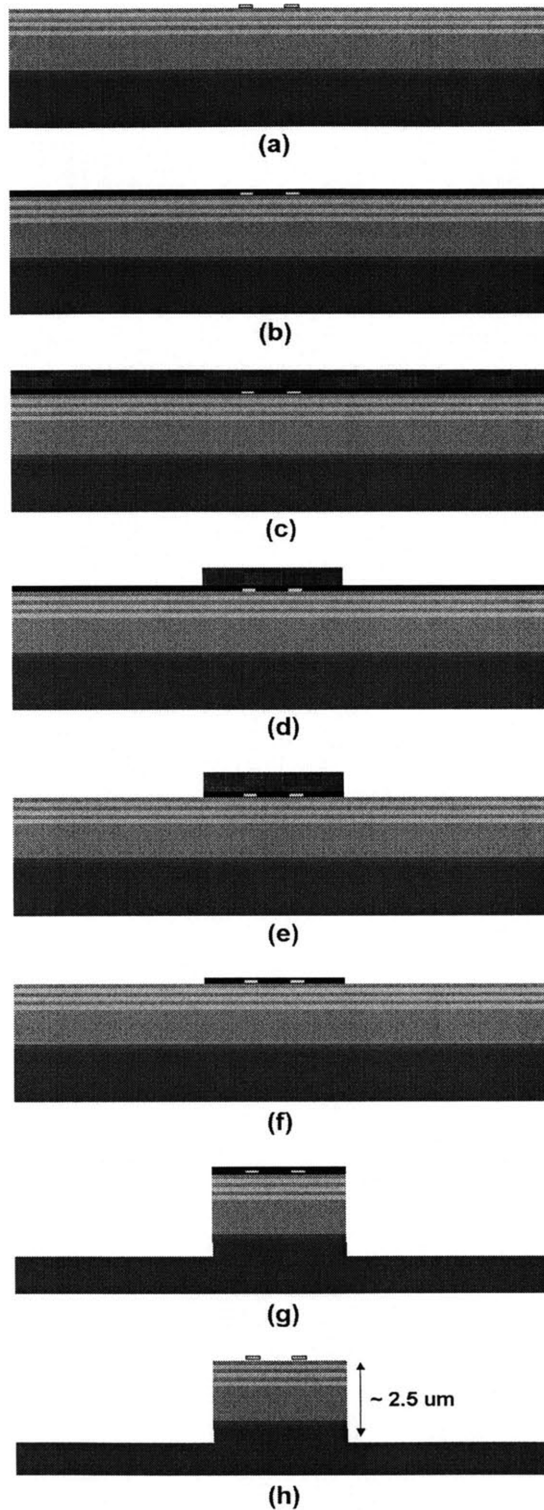


Figure 32 Process Flow for Mesa Definition Using Reactive Ion Etches

(a) Heterostructure after ohmic contact formation, (b) ~0.5 μm oxide mask growth, (c) Photoresist applied on oxide layer, (d) Photoresist exposed and developed into mesa patterns, (e) Oxide etched with photoresist as mask into mesa patterns, (f) Photoresist removal, (g) RIE mesa etch for device definition, (h) Oxide mask removal with RIE.

The InP-based heterostructure devices were isolated from each other by dividing the top surface into square-shaped islands having dimensions 40 μm by 40 μm. Figure 33 shows the mask used for the mesa pattern etch.

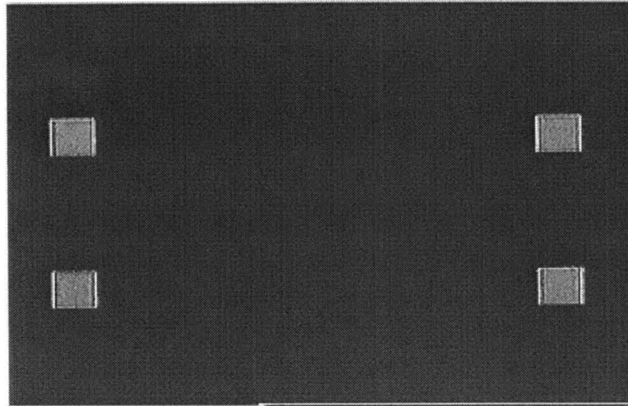


Figure 33 Mask "COMBO-4" Pattern for Mesa Etch
A soft resist mask was used to pattern a layer of silicon oxide, which in turn was used as the hard mask for InGaAs/InP etching in ECR-enhanced RIE. Since positive resist was used to transfer the pattern of mesas to the oxide film, the mask used was therefore light field. The picture shown here suggests a reversed mask polarity. The resist in the background was exposed to the UV light through the light field of the mask, and was dissolved away during development. On the other hand, the dark field square–shaped mesas remained unexposed on the sample throughout the photo step, protecting the semiconductor layers underneath from being etched during the subsequent RIE.

As seen in Table VI, the n-type InGaAs etch stop layer was situated 2.35 μm below the heterostructure surface. To ensure complete isolation of mesas, 2.5 μm of uncovered III-V materials was removed by ECR-Enhanced RIE with 15/15 sccm of CH_4/H_2. The etched depth, or mesa height, was periodically measured throughout the process. The etch rate was carefully monitored and observed to be approximately 0.05 μm per minute. It took approximately 60 minutes to etch greater than 2.5 μm of the calibration sample down to the etch stop layer.

4.4.2 Results and Discussion

A SEM image of a dry-etched mesa with a square AuZn ring on top is shown in Figure 34. Anisotropic etch along the entire photodiode heterostructure was established. As seen from the SEM image, the vertical etch rate was higher than the horizontal etch rate such that the sidewalls were highly perpendicular to the substrate base. However, it can be seen that the sidewalls of the mesa were not smooth, and the etched floor surface was very rough with

coarse features such as spikes and protrusions. Roughness caused by dry-etching, as well as solutions proposed were discussed in Section 3.3.

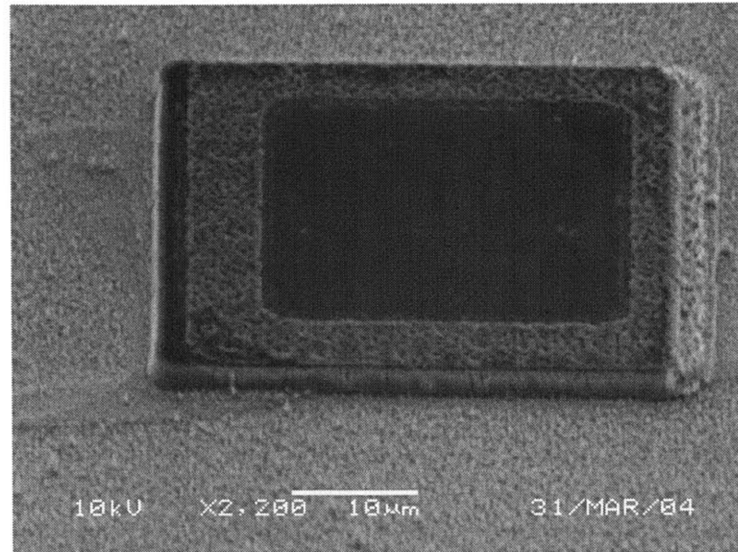


Figure 34 SEM Image of Dry Etched InGaAs/InP Mesa
The feature shown in this SEM is a 2.5 μm high, 40 μm by 40 μm mesa. The square ring on top is the alloyed AuZn (5%) ohmic ring formed in the previous step.

4.5 BCB Passivation and Planarization

4.5.1 Experimental

The purposes of passivation and planarization have been discussed in Section 3.4. In this step, mesas of very low aspect ratio (2.5 μm / 40 μm = 0.06) were covered by BCB polymer. The aspect ratio of a feature is defined as the ratio of its height to its width. The experimental procedures of BCB application and curing have been discussed in Section 3.4.1.

4.5.2 Results and Discussion

Figure 35 shows the top view of mesas covered by one layer of cured dry-etch grade BCB. A certain degree of BCB coverage over the top of mesas was observed by the fringe effects of rainbow-like fields.

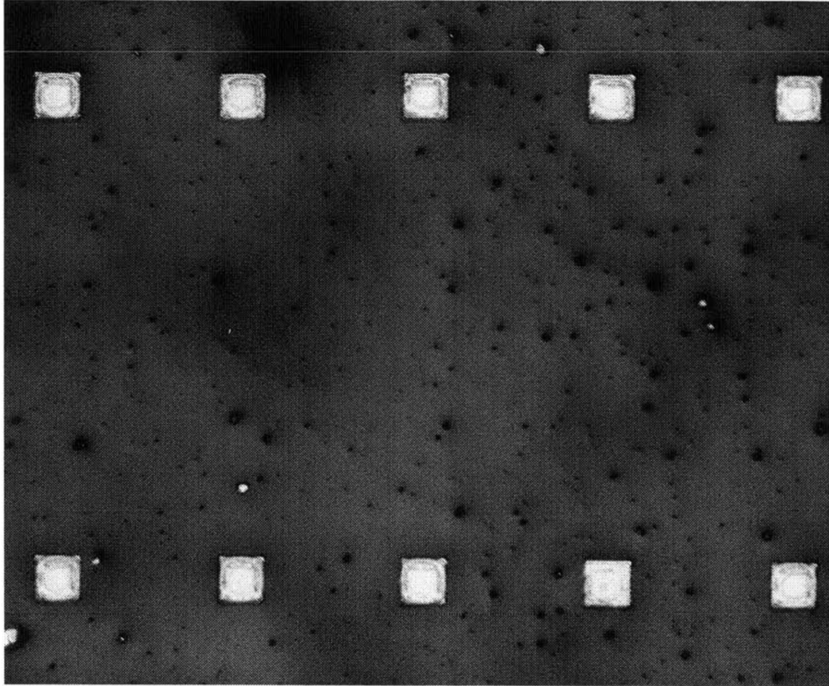
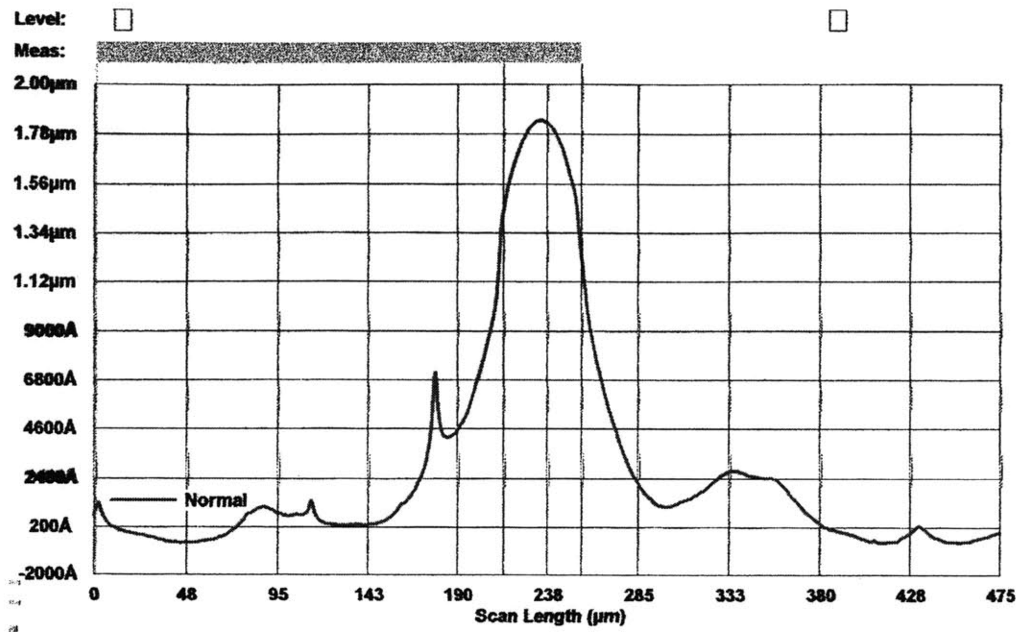


Figure 35 InGaAs/InP Mesas Covered with One Layer of BCB
The square mesas are 40 μm by 40 μm, with a height of 2.5 μm. The bubbles in the BCB film indicate an unsatisfactory coverage of the sample surface. It was concluded that the damages caused by CH_4/H_2 dry-etch created the coarse features that led to the poor planarization result.

There were many regions in the BCB film that were too thin or protruded with the underlying barbed structures, and evidently, the wafer was not satisfactorily planarized. The poor outcome was likely a result of the coarseness on the sample surface caused by CH_4/H_2 dry-etching. The size of the dark spots match closely with the size of coarseness on the InP substrate prior to the application of BCB. It was concluded that the spiky features created by dry-etch damages and deposits led to this poor planarization result. Techniques to achieve smoother etch profiles were discussed previously in Section 3.3.

The profiles of mesa features were examined with a 2 μm stylus at a Tencor P10 station, whose recipe "TEST" parameters are included in Appendix E. Figure 36 shows the dektak curve traced over a mesa feature that was 2.5 μm in height, 40 μm in width, and covered by one layer of dry-etch grade BCB. Notice the coarse features on the mesa floor. The dry-etch grade BCB polymer was spun at 5 krpm, yielding a final cured thickness of over 1 μm. Knowing the size and geometry of the mesa a priori, it can be deduced that there was approximately 0.4 μm of BCB on top of the mesa. The step height from top of the mesa to

the BCB level was approximately 1.3 μm. The top of 2.5 μm tall mesas were concluded to be sufficiently covered by one layer of dry-etch grade BCB resins.



<u>Figure 36 Profilometer Analysis of BCB Mesa Coverage</u>
The final, cured polymer film had a thickness of just over 1 μm. The covered mesa feature was 40 μm in width and 2.5 μm in height. It was therefore deduced that approximately 0.4 μm of BCB "beaded up" on top of the mesa, and the step height from top of the mesa to the BCB level was about 1.3 μm. Therefore, it was concluded that the top of the mesas were sufficiently covered by only one layer of BCB.

4.6 Via Opening by BCB Etch with RIE

4.6.1 Experimental

Vias were created in the passivation layer to expose the backside substrate which connected to the N-side of the photodiode, as well as the ohmic rings which were deposited on the P-side of the photodiode heterostructure. The via opening process for fabricating discrete P-i-N photodiodes was derived from that developed in the post-assembly processes as described in Section 3.5. The mask used for via opening is shown in Figure 37. The thin horizontal stripes are via windows that expose the back (N-side) of the discrete photodiodes. The small square in-between the two thin stripes provides connection to the ohmic ring on the P-side of the discrete photodiodes.

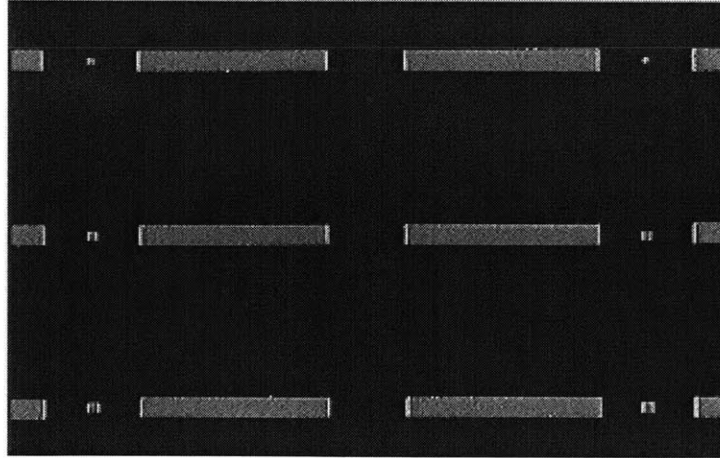


Figure 37 Mask "LED TRANS" Pattern for Open Via
Thick photoresist was used as mask for BCB etching. Since the thick photoresist was positive-acting, the mask pattern used was a dark field mask. After the photolithography steps, the light field of the pattern consisting of the thin stripes and the small openings in-between the stripes, was developed, exposing the BCB passivation layer underneath it. During BCB dry-etching, these unprotected areas were etched through and vias were thus created.

4.6.2 Results and Discussion

Figure 38 is a picture of a silicon sample which underwent all of the processing steps except for the final top metallization.

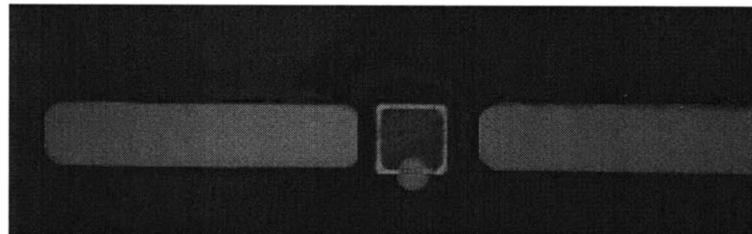


Figure 38 Vias Opened in BCB Layer on Silicon Dummy Sample
The square in the middle is the AuZn (5%) ohmic ring formed on top of a 40 μm by 40 μm silicon mesa. The opening at the bottom section of the square as well as the two horizontal stripes on the sides, are via windows created in the BCB layer. The dark background was the areas that were covered by BCB.

The 40 μm by 40 μm square ring in the middle is the AuZn (5%) ohmic contact as described in Section 4.3. The ohmic rings were on top of 2.5 μm tall, 40 μm by 40 μm mesas which were described in Section 4.4. For the silicon dummy sample process (described in Section 4.2), mesas were etched by a deep silicon trench etcher "STS-1" by Surface Technology Systems. The dark background indicated areas that were covered by BCB, as described in Section 4.5.

As seen at the bottom of the picture, the small 3 μm by 3 μm opening was the via that exposed the AuZn ohmic ring on the P-side of the mesa. The two horizontal stripes, approximately 150 μm by 20 μm and symmetrically on each side, were the vias that allowed connection to the backside side of the photodiode via the n-type InP substrate. The via-opening process as developed in the dry run was demonstrated to be successful, yielding successful etch profiles and enabling top metallization.

4.7 Ti/Au Top Metallization

4.7.1 Experimental

The top metallization pads provided electrical connection to the discrete photodiodes and served purposes such as biasing, optical measurements, and i-v characterization. The top metallization scheme adopted was titanium and gold (Ti/Au). No dopant species was necessary for the n-type InP (100) substrate. This process step was a convenient one-step procedure designed such that the Ti/Au metal inside the vias was deposited at the same time as that on top of the dielectric. The top metallization process for InP-Based P-i-N photodiode fabrication was a derivative of that developed in the post-assembly processes described in Section 3.6, and vice versa.

4.7.2 Results and Discussion

As shown in Figure 39, the square pad in the middle connected to the P-side of the discrete P-i-N photodiode structure. Specifically, the small rectangular extension aligned with the 3 μm by 3 μm via that exposed the underlying AuZn ohmic rings. The pads on each side aligned with the vias that connected to the backside of the photodiode through the n- InP substrate.

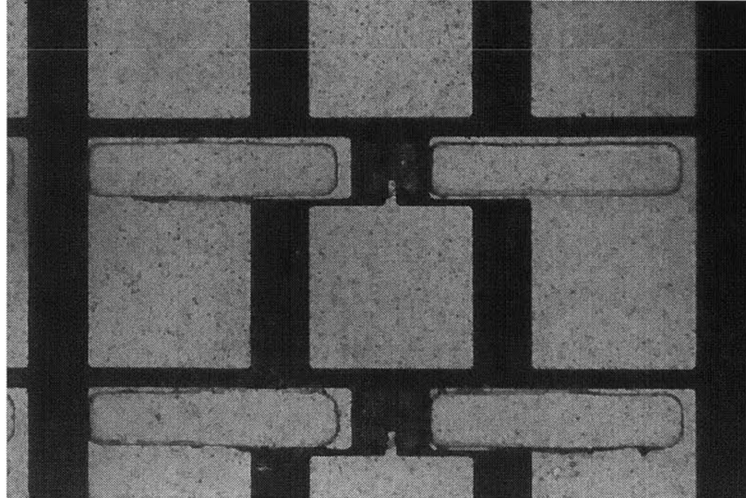


Figure 39 Top Metallization on Silicon Dummy Sample
The contact pads that were created in the final metallization step provided electrical connection to the anode and cathode of the photodiode. The 110 μm by 110 μm square pad in the middle connected to the P-side of the discrete P-i-N photodiode structure via AuZn ohmic rings, and the symmetrical pads on each side connected to the backside of the photodiode via the n-type InP substrate.

The top metallization step as developed for the Si dummy sample was shown to be successful. Although further electrical testing is needed to verify the ohmic characteristics, the metal pads as patterned by the lift-off procedure appeared to have properly filled the vias. The conformal topology indicated the continuous and robust formation of top interconnects.

4.8 Final P-i-N Photodiode Structure

The process for fabricating discrete InGaAs/InP photodiodes was thoroughly developed and practiced on silicon dummy samples. This technology is to be transferred and applied to the actual calibration sample. Figure 40 shows a schematic of the final cross section of the mesa-type P-i-N photodiode that is fully processed.

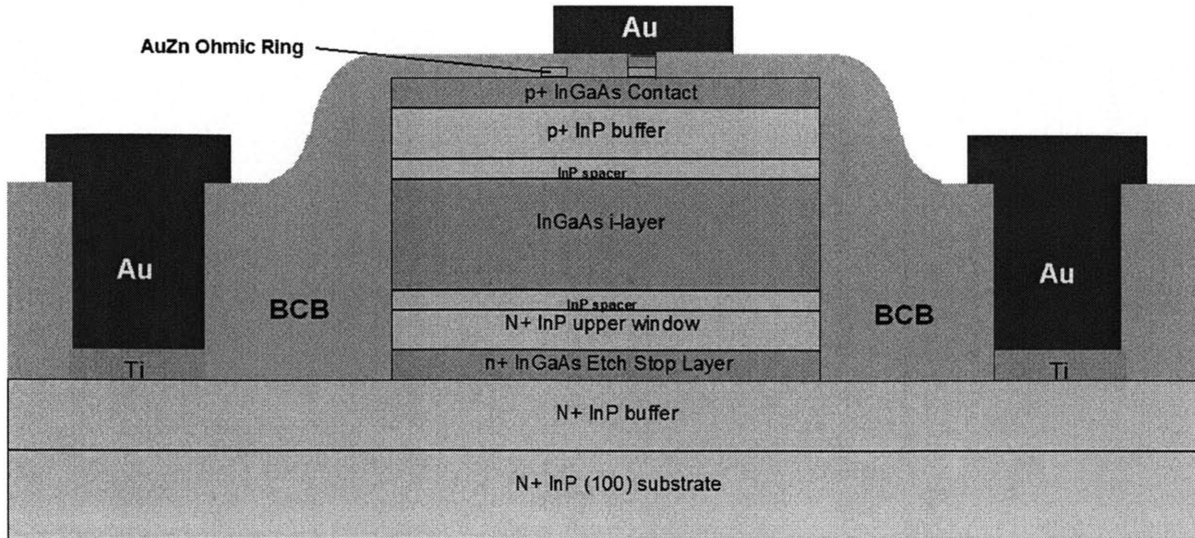


Figure 40 Schematic Cross Section of the Mesa Type Photodiode
The final device fabricated was a vertical P-i-N photodiode. The alloyed AuZn ohmic ring was first formed on the InGaAs contact layer using lift-off lithography and e-beam deposition. Then, with oxide as the hard etch mask, the mesa was isolated to define the active area of the device by ECR-enhanced RIE. The wafer was re-planarized and the junction was passivated with a layer of BCB polymer. With thick photoresist as mask material, BCB was etched using RIE to open vias and expose the backside contacts and the ohmic ring. Finally, Ti/Au top contacts were created using image reversal lithography and e-beam evaporation. The final device as shown here is ready for complete electrical and optical characterizations.

4.9 Pre-Passivation Characterization of Discrete P-I-N Photodiodes

Preliminary electrical testing of the photodiode was done prior to BCB planarization. A schematic of the test setup is shown in Figure 41. Voltage of -2.5V to +2.5V was swept across the junction, and the diode was reverse biased when a negative voltage was applied relative to the N-side substrate which was grounded. Various parameters such as the turn-on voltage, forward series resistance, reverse saturation or dark current, and breakdown voltage were extracted.

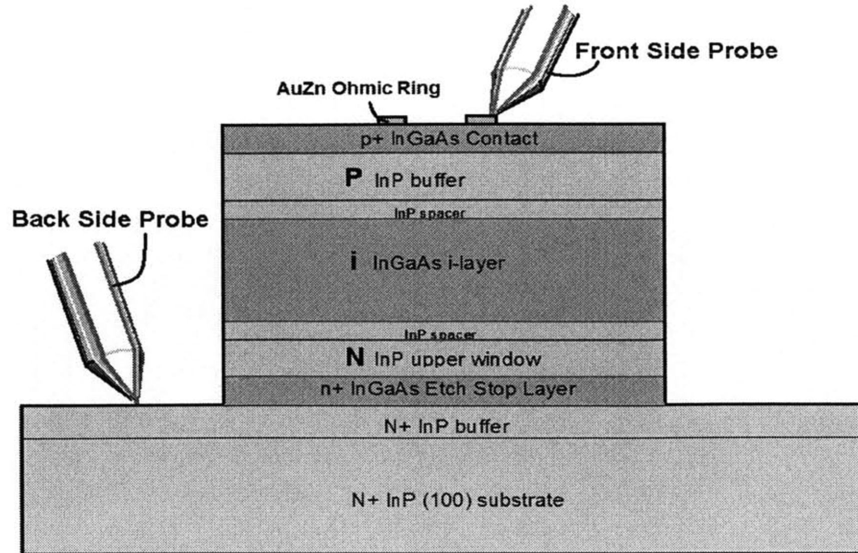


Figure 41 Mesa-Type Photodiode Characterized Prior to BCB Passivation
The back side connection was established through the substrate chuck holder which was grounded. Complete i-v characteristics were obtained by sweeping a range from negative to positive biases across the junction but when a negative voltage was applied by the front side probe via the ohmic ring on top, the diode was said to be reverse biased.

Figure 42 illustrates the current-voltage characteristics of a junction photodiode. The positive voltage axis indicates a forward bias, and the positive current indicated a flow from the p-side to the n-side of the junction. Superimposing the schematic of i-v characteristics with that measured helps to interpret the electrical behavior of the diode.

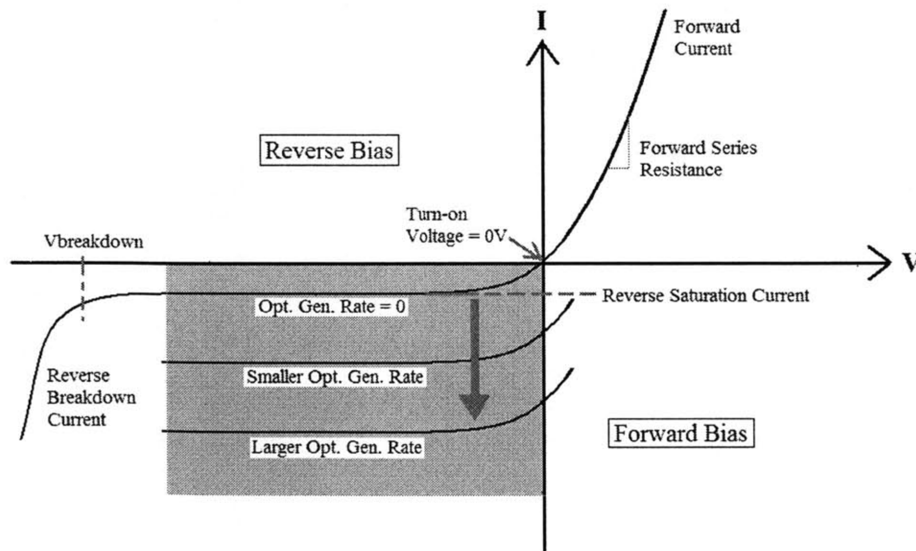


Figure 42 Photodiode I-V Characteristics and Response to Optical Excitation
Superimposed with Figure 43: InGaAs/InP Photodiode I-V Curve Prior to BCB Passivation, one can see much resemblances in the shape of the schematic and measured characteristics.

As shown in Figure 43, a curve tracer and a parameter analyzer were used to measure the current-voltage characteristic of the discrete InGaAs/InP diodes prior to BCB passivation, where much useful data were extracted.

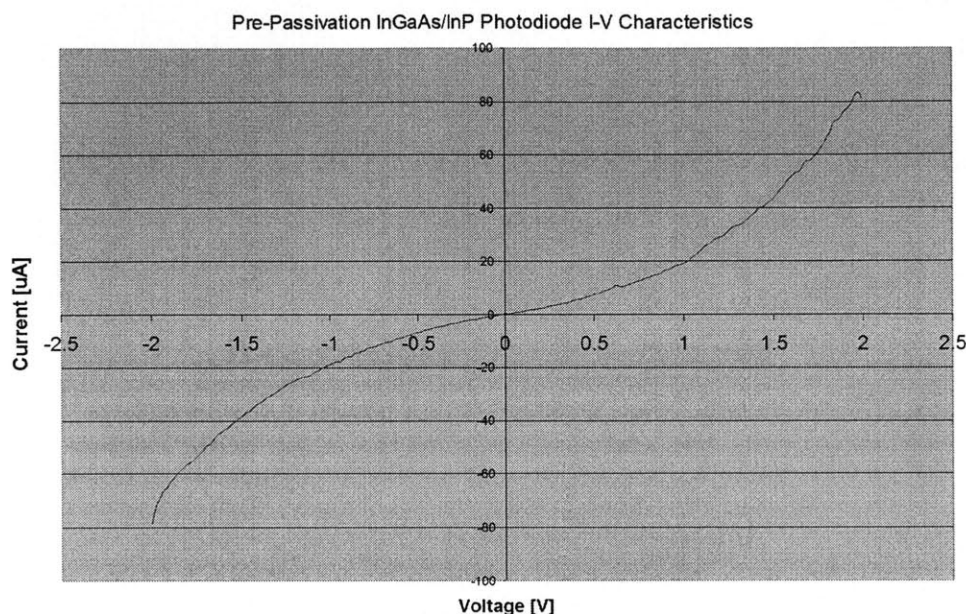


Figure 43 InGaAs/InP Photodiode I-V Curve Prior to BCB Passivation
Current-voltage characteristics of the discrete P-i-N photodiodes measured prior to BCB passivation. InGaAs/InP optical devices typically yield a wide spectral response and a low dark current.

The dark current was directly measured on the 40 μm by 40 μm active device. Without any source of light, the dark current or the reverse leakage current was observed to be very low. Passivation of the junction separates the edge leakage from the bulk leakage currents. Application of BCB is expected to reduce the dark current; post-passivation benchmarking is needed to draw further conclusions.

When measuring the breakdown voltage, a very large resistor (3 kΩ) was connected in series with the diode to limit the maximum current flow. From the curve obtained, the reverse $V_{breakdown}$ of the photodiode was observed to be approximately 2V. In addition, the forward turn-on voltage was observed to be +0.35V and the forward series resistance was measured to be $R = \frac{V}{I} = \frac{1}{40}\left[\frac{V}{uA}\right] = 25k\Omega$.

The pre-passivated diode structure was illuminated with visible light through the window in the p-type contact layer. Signs of response to optical excitation were evidently observed. Experimentally, the photocurrent generated by a known amount of laser power can be obtained by measuring the voltage drop across the bias resistor. Responsivity can be calculated by obtaining the output photocurrent and dividing it by the incident optical power, where $R = \frac{I_{photo}}{Power}\left[\frac{A}{W}\right]$. Since this parameter is a function of both the incident wavelength as well as the efficiency of the device in responding to that wavelength, it is therefore very useful for characterizing photodetector performances.

5 CONCLUSIONS

This thesis has focused on the development of post-assembly processes for the novel heterogeneous monolithic integration process called OptoPill assembly (OPA). The OPA approach provides a feasible solution for adding III-V functionality to state-of-the-art Si-based integrated circuits. This technique was applied to InGaAs/InP photodiodes and a Si-CMOS photoreceiver that was designed to alleviate timing uncertainties in on-chip optical clock distribution.

Techniques used, challenges seen, and results accomplished in developing each step of the post-assembly process, including the ohmic formation, active area definition, planarization and passivation, via opening, and top contact metallization have been discussed. In conjunction, InGaAs/InP photodiodes were fabricated in order to understand and characterize their electrical and optical behaviors independent from the Si-CMOS circuits. The procedures used to fabricate InP-based photodiodes are direct derivatives of the technology developed for the post-assembly processes. Key works accomplished and some directions for future research are highlighted below.

5.1 Ohmic Formation

Good agreement was found in standard TLM analysis of Cr/Au ohmic metallization on p-type InGaAs contact layers. The sheet resistance of InGaAs $In_{0.53}Ga_{0.47}As$ (N_A = 1 x 10^{19} cm^{-3}) was found to be 150 [Ω/□], which reasonably approximated the theoretical value of 80.33 [Ω/□]. The specific contact resistance of Cr/Au on the contact layer was measured to be 10^{-3} [Ω-cm^2]. More work can be done in the future to better understand various ohmic contacts formations and to achieve lower contact resistances.

For the fabrication of discrete photodiodes, the non-alloyed Cr/Au or Ti/Au metal failed to form ohmics on p-type $In_{0.53}Ga_{0.47}As$ with a lighter doping concentration of N_A = 5.0 x 10^{18} cm^{-3}. A high net hole concentration can be augmented with the post-growth diffusion of Zn

dopant species into the semiconductor. The alloyed AuZn metal was chosen as the P-side contact in the discrete photodiode process. The specific contact resistance was reported to range from 1 x 10^{-5} to 5 x 10^{-5} [Ω-cm^2]. Although no TLM testing was carried out on this structure, the equivalent resistance between two contact pads obtained from the current-voltage characteristics (167 Ω) agreed closely with the calculated value (160 Ω).

5.2 Active Area Definition

Dry etch process with the CH_4/H_2 gas mixture was used to define active areas in the InGaAs and InP layers. The uniformity of the etch profile was difficult to control by simply varying the process parameters. The etched InP sample had very rough sidewalls and surfaces, which possibly caused by the polymeric impurities which act as sub-micron masking features while the high-energy ions continue to bombard the exposed InGaAs/InP semiconductor materials. Methods to improve the floor coarseness, including that of the employment of oxygen plasma have been discussed. Further dry-etch experiments were carried out where the sample received 30 minutes treatment of oxygen plasma, 10 minutes of which were with 400 W of microwave power and 5 W of RF. This did not seem to improve the problem. Further work must be done in order to develop a better dry-etch process for InGaAs and InP-related semiconductors. Suggested directions include brief wet-etching after each interval of dry-etch, a lighter concentration (less than 50%) of methane relative to hydrogen in the gas mixture, or the incorporation of oxygen (0.5% to 1.0%) to create a $CH_4/H_2/O_2$ plasma.

5.3 Planarization and Passivation

Extensive experiments found that multiple layers of the thinner, dry-etch grade BCB gave better planarization result than one layer of thick, photo-sensitive grade BCB. An excellent degree of planarization was demonstrated with two coatings of dry-etch grade BCB, in which a nearly planar (>95%) surface was achieved.

5.4 Via Opening

The gas mixture for etching BCB was 10/90 sccm of Freon (CF_4) and oxygen (O_2) respectively. The etch selectivity of the 3000 series dry-etch grade (3022-35) BCB resin to the thick photoresist (AZP 4620) mask was 0.7:1 [35]. Even though the photoresist etches 1.4 times faster than BCB, 10 μm of thick photoresist was used while the BCB films ranged from 1 μm to 3 μm, and the soft mask was proven to be of sufficient thickness for the BCB etch. Under the etch conditions of 200 mTorr and 150 W of RF power, the etch rate of BCB using RIE was calibrated to be approximately 0.7 μm per minute. The via-opening process as developed on a silicon dummy sample was demonstrated to be successful, yielding successful etch profiles and enabling top metallization.

5.5 Top Metallization

A smooth and planar surface as a result of BCB planarization and wide via angles as a result of proper BCB dry-etching, were both demonstrated. The top metallization scheme adopted was titanium and gold (Ti/Au). Although further electrical testing is needed to verify the ohmic characteristics, the metal pads as patterned by the lift-off procedure appeared to have properly filled the vias. The conformal topology indicated the continuous and robust formation of top interconnects, and this process step as developed on a silicon dummy sample was demonstrated to be successful.

5.6 Future Directions

There are a number of areas in need of further work. First and foremost, better InGaAs/InP dry etch recipes need to be developed in order to achieve smoother etch profiles. Though fully carried out on silicon dummy samples, culminations of the process steps remain to be applied in entirety to the calibration sample in order to complete the fabrication of discrete P-i-N photodiodes. More work needs to be done to obtain pre- and post-passivation data in order to assist the final analysis of the integrated photodetector in the Si-CMOS optical clock distribution circuit. The quality of the heterostructure, the robustness of the ohmic ring and top metallization, and the electrical integrity of the junctions etched by RIE and passivated by BCB, all remain to be assessed and characterized by further optical testing in the near future.

APPENDIX A: FACILITIES AND PROCEDURES

A.1 E-beam Metal Evaporation

Location	Experimental Materials Laboratories (EML)
Machine	Electron-beam MDC-360
Purpose	Metal evaporation

1. Venting
   Open nitrogen vent valve
   Raise top chamber plate with mechanical hoist toggle switch
   Close vent valve

2. Chamber Preparation
   Clean off delaminating films and loose debris in the chamber
   Clean hearth (proper cooling prevents superheating, alloying, and crucible breakage)

3. Load Sample
   Mount sample onto wafer plate, load into chamber
   Place appropriate source crucibles into hearths
   Verify crystal thickness is above 85%
   Lower and seal top chamber plate

4. System Evacuation
   Open roughing valve, pump down to 500 mTorr
   Close roughing valve (note leak up rate)
   Open high vacuum (HiVac) valve
   Pump down to < $2x10^{-6}$ mTorr (measured by the ion gauge)

5. Programming the MDC-360 Deposition Controller (See appendix B.2)

6. Deposition Preparation
   Open water valves (to cool power supply and crystal oscillator)
   Turn on main and control circuit breakers
   Turn on gun control master key
   Set emission dial on PAK remote gun control to 0A
   Set x-y position at 0, sweep controls at .5

7. Deposition
   Turn on controller key to RUN
   Turn on gun control
   Slowly ramp up power as indicated by the Amps-Current gauge
   Center beam on source material
   Heat up at approximately .02 A increase per minute

8. Layer Completion
    Close Shutter
    Reduce filament current gradually
    Turn off filament key
    If another layer is needed, wait 5 minutes till the next deposition
    Repeat from Step 5

9. Shutdown
    Turn off gun control key to LOCK
    Close high vacuum (HiVac) valve
    Turn controller key to standby
    Turn off main and control circuit breakers

    Wait for 15 minutes for the system to cool down
    Shut off cooling water valves
    Open vent valve
    Raise top chamber plate and unload sample
    Lower and seal top chamber plate, pump down to 500 mTorr
    Close roughing valve

A.2 Plasmatherm (PECVD and RIE)

Location	Experimental Materials Laboratories (EML)
Machine	Plasmatherm
Purpose	Plasma Enhanced Chemical Vapor Deposition (PECVD) Reactive Ion Etch (RIE)

PECVD Chamber 1 (ch-1)

MFC ch 1-1	NH_3 (Ammonia)
MFC ch 1-2	SiH_4 (Silane)
MFC ch 1-3	CF_4, O_2 (Tetrafluormethane / Freon-14, oxygen for chamber clean)
MFC ch 1-4	N_2, N_2O, He, O_2

RIE Chamber 2 (ch-2)

MFC ch 2-1	BCl_3 (Boron Trifluoride)
MFC ch 2-2	SF_6 (Sulfur Hexafluoride), CH_4=HC14 (Methane)
MFC ch 2-3	Cl_2, H_2
MFC ch 2-4	He, Ar, O_2

1. Evacuate mass flow lines
   Select active chamber (Chamber 1 for PECVD, Chamber 2 for RIE)
   Pump chamber with turbo
   With gas cylinders closed, open valves from chamber toward tank
   Pump until mass flow reaches 0 sccm
2. Vent chamber
3. Load sample
4. Pump out chamber
5. Build Program Recipe
   Step 0 Initial Data and Evacuate Chamber
      Temperature Heat Exchange 1: 25°C
      Temperature Heat Exchange 2: 25°C
      Default Pump: Turbo
      Initial Pump down Pump: Turbo
      Base Pressure: 1×10^{-4} mTorr
      Hold After Base Pressure: No
   Step 1 Purge for 1 minute (to flush chamber with N_2)
   Step 2 Evacuate for 1 minute (to pump out chamber)
   Step 3 System Environment Stabilization (Process gas flow without RF)
      Flush gas lines and chamber (See Appendix B.3)
   Step 4 PECVD (Process gas flow with RF)
   Step 5 Evacuation for 1 minute
   Step 6 Purge for 1 minute
   Step 7 Evacuation for 1 minute
   Step 8 Purge for 1 minute
   Step 9 Evacuation for 1 minute
   Step 10 Purge for 1 minute

Step 11 End Sequence and Chamber Pump-out

Gas Line Cleanup: None

Final Pump: Turbo

Base pressure: 1×10^{-4} Torr

6. Open gas cylinders and Run Program
7. Process completion
8. Shut-Down

   Pump chamber to high vacuum

   Close toxic gas cylinders. Leave shut-off valves open.

   Evaluate toxic MFC lines until 0.0 sccm flow rate is reached.

   Close in-line and mixing valves from tank towards system

   Stop evacuation

   Stand by. Leave chamber pumping

A.3 PlasmaQuest

Location	Technology Research Laboratories (TRL)
Machine	PlasmaQuest
Purpose	Electron Cyclotron Resonance (ECR) Enhanced Reactive Ion Etcher (RIE) Chemical Vapor Deposition (CVD) system

This system uses both ECR and the radio frequency (RF).

Available process gases:
Nitrogen (N_2), Oxygen (O_2), Sulfur Hexafluoride (SF_6), Chlorine (Cl_2), Boron Trifluoride (BCl_3), Methane (CH_4), Tetrafluormethane (CF_4), Trifluorimethane (CH)

1. System Preparation
   Check the chiller water level.
   Check and set desired process temperature.
      25 °C for standard etches such as oxide, nitride, silicon, and polysilicon
      80 °C for etch processes using Cl_2, BCl_3, or metal etching
2. Chamber Clean (10 minutes per microns of deposition)
3. Select recipe (see Appendix B.3 for InGaAs/InP etch recipe)
4. Bring load lock to atmospheric pressure
5. Load sample onto loading arm
6. Run recipe
   RF TUNING: Reflected power should read less than 10 watts.
   ECR TUNING: Adjust microwave tuning stubs to achieve a reflected power of less than 10 watts, or as low as possible.
4. System Shutdown
   Vent Load Lock
   Unload sample from chamber after process completion.
   Pump load lock down to vacuum with dummy wafer on loading arm.

APPENDIX B: PROCESS RECIPES

B.1 Photolithography Process Recipes for Different Resists

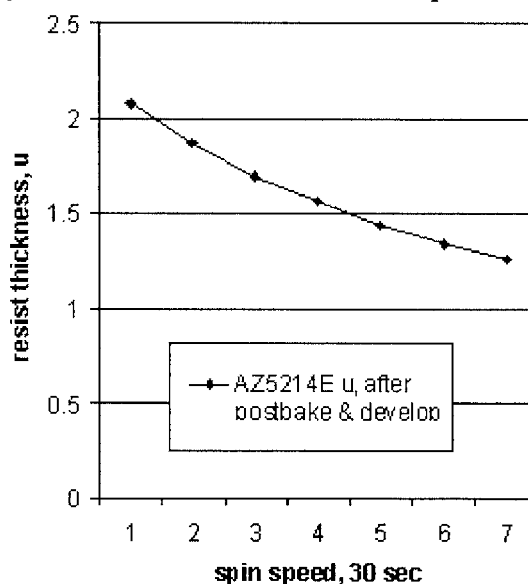
a) Image Reversal Positive Tone Photolithography Using AZ5214-E

Technology Research Laboratories (TRL)

Step 0 Wafer preparation and solvent clean
Step 1 HMDS application
Step 2 Spin-on photoresist AZ5214E

Purpose	Speed [krpm]	Time [sec]
Dispense	0.5	4
Spread	0.75	4
Spin	2	30

Image Reversal Photoresist (AZ 5214E) Spin Curve [37]



Step 3 Prebake in 90°C oven for 30 minutes
Step 4 Expose with Karl Suss Model MA-4 Mask Aligner for 35 seconds
Step 5 Bake in 120°C oven for 30minutes
Step 6 Flood exposure with Karl Suss Model MA-4 Mask Aligner for 3 minutes
Step 7 Develop with AZ422 for approximately 2 minutes, rinse with DI water

Experimental Materials Laboratories (EML)

Step 0 Substrate preparation and solvent clean
Step 1 Dehydration bake at 130°C for 20 minutes

Step 2 (Optional) HMDS application:

Static dispense at 4 krpm for 30 seconds, Bake at 130°C for 10 minutes

Step 3 Spin on photoresist AZ5214E

Purpose	Speed [krpm]	Time [sec]
Dispense	0 .5	6
Spread	0.75	6
Spin	2	30

Step 4 Prebake at 90°C for 30 minutes

Step 5 Expose with Karl Suss Model MJB-3 Mask Aligner for 5 seconds

Step 6 Bake at 90°C for 30 minutes

Step 7 Flood exposure with Karl Suss Model MJB-3 Mask Aligner for 45 seconds

Step 8 Develop with AZ 422 for approximately 2 minutes, rinse with DI water

b) Positive Photoresist OCG 825 Photolithography

Technology Research Laboratories (TRL)

Step 0 Wafer preparation and solvent clean

Step 1 HMDS application

Step 2 Spin-on photoresist OCG825

Purpose	Speed [krpm]	Time [sec]
Dispense	0.5	4
Spread	0.75	4
Spin	3	30

Step 3 Prebake in 90°C oven for 30 minutes

Step 4 Expose with Karl Suss Model MA-4 Mask Aligner for 30 seconds

Step 5 Develop with OCG 934 1:1 for 2 minutes, rinse with DI water

Step 6 Postbake in 120°C oven for 30 minutes

Experimental Materials Laboratories (EML)

Step 0 Wafer preparation and solvent clean

Step 1 Dehydration bake in 130°C for 30 minutes

Step 2 Spin-on photoresist OCG825

Purpose	Speed [krpm]	Time [sec]
Dispense	0.75	5
Spin	3	30

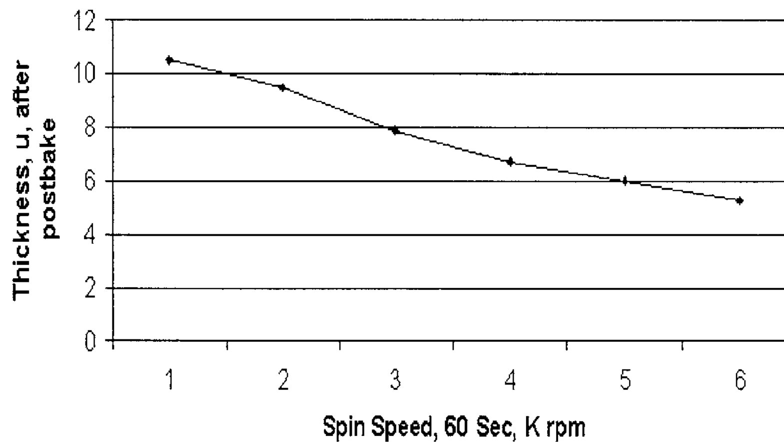
Step 3 Prebake in 90°C oven for 30 minutes
Step 4 Expose with Karl Suss Model MJB-3 Mask Aligner for 4 seconds
Step 5 Develop with OCG 934 1:1 for 2.5 minutes, rinse with DI water
Step 6 Postbake in 130°C oven for 30 minutes

c) Thick Photoresist AZ4620 Photolithography

Experimental Materials Laboratories (EML)

Step 0 Wafer preparation and solvent clean
Step 1 Dehydration bake in 130°C for 30 minutes
Step 2 Spin-on photoresist AZ4620

Purpose	Speed [krpm]	Time [sec]
Dispense	0 (Static)	10
Spread	0 (Static)	10
Spin	1.5	60



Step 3 Prebake in 90°C oven for 60 minutes
Step 4 Expose with Karl Suss Model MJB-3 Mask Aligner for 1 minute
Step 5 Develop with AZ 440 for about 4 minutes, rinse with DI water
Step 6 Postbake in 130°C oven for 30 minutes

B.2 E-beam Evaporation Recipes

The electron-beam evaporation system is located in both the Technology Research Laboratory (TRL) and the Experimental Materials Laboratory (EML) of the Microsystems Technology Laboratory (MTL).

Time to Rough to 500mTorr	20 minutes
High Vac Time	10 minutes
Min Pressure (baseline)	1.5 x 10^{-6} mTorr
Crystal Life	greater than 85%

	Ti	Au
Ramp-up Time [min]	7	7
Max. Run Pressure [Torr]	2 x 10^{-6}	2 x 10^{-6}
Rate [A/sec]	3	3
Amps – gauge [A]	.2	.2
X position (-1 to +1)	0	0
Y position (-1 to +1)	0.1	0.1
Sweep X (0 to 1)	0.5	0.5
Sweep Y (0 to 1)	0.5	0.5
Indicated Thickness [kÅ]	3	3

B.3 PECVD Deposition and RIE Etch Recipes

Oxide Deposition (PECVD)

Deposition Temperature: 250°C

Ch 1-2: 600 sccm (SiH_4 5%)
Ch 1-4: 300 sccm (N_2O)

Pressure: 500 mTorr
Process Pump: Lo Vac
RF Generator Used: RF1
RF Configuration: PECVD
RF Controlled by: INCP (incident power)
RF1 set point: 25 Watts
Termination Time: 20 min*

** Deposition rate is approximately 0.2 μm per 10 minutes*
Therefore, to deposit 0.4 μm of SiO_2 it took approximately 20 minutes

Chamber Clean (RIE)

Ch 2-4: 30 sccm (O_2)

Pressure: 50 mTorr
Process Pump: Turbo
RF Generator Used: RF1
RF Configuration: RIE
RF Controlled by: INCP (incident power)
RF1 set point: 300 Watts
Termination Time: 10 min

Oxide Etch (RIE)

Mask Material: Positive photoresist (OCG 825)
Ch 2-1: 20 sccm (CF_4=HC_{14})

Pressure: 25 mTorr
Process Pump: Turbo
RF Generator Used: RF1
RF Configuration: RIE
RF Controlled by: INCP (incident power)
RF1 set point: 300 Watts
Termination Time: 10 min*

** Etch rate is approximately 0.4 μm per 10 minutes*
Therefore, to etch 0.4 μm of SiO_2 it took approximately 10 minutes

Silicon Etch (RIE)

Mask Material: Positive photoresist (AZP 4620)

Ch 2-2: 10 sccm (SF_6)

Pressure: 20 mTorr
Process Pump: Turbo
RF Generator Used: RF1
RF Configuration: RIE
RF Controlled by: INCP (incident power)
RF1 set point: 200 Watts
Termination Time: 4 min*

** Etch rate is approximately 0.7 μm per minute*
Therefore, to etch 2.6 μm of Si it took approximately 4 minutes

BCB Etch (RIE)

Mask Material: Thick photoresist (AZP 4620)
Ch 2-1: 10 sccm (CF_4/HC_{14})
Ch 2-4: 90 sccm (O_2)

Pressure: 200 mTorr
Process Pump: Turbo
RF Generator Used: RF1
RF Configuration: RIE
RF Controlled by: INCP (incident power)
RF1 set point: 150 Watts
Termination Time: 2.5 min*

** Etch rate is approximately 0.7 μm per minute*
Therefore, to etch 1.3 μm of BCB it took approximately 2.5 minutes

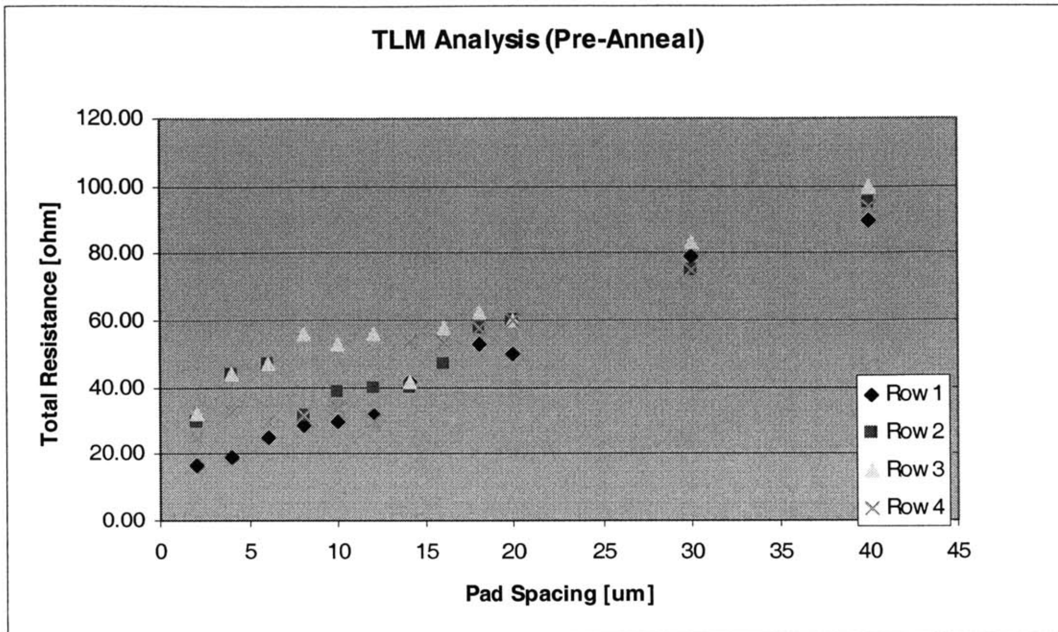
InGaAs/InP Etch (RIE)

Mask Material: Silicon oxide (SiO_2)
15 sccm CH_4
15 sccm H_2

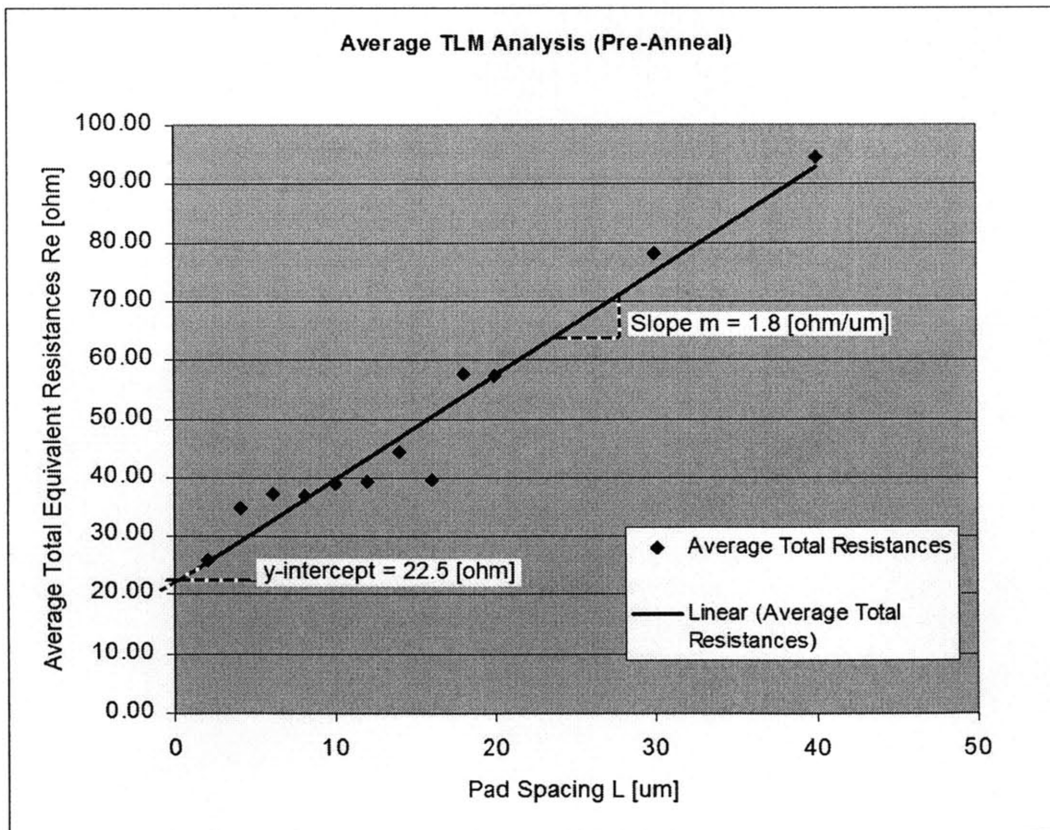
Temperature: 25°C
Pressure: 18 mTorr
Microwave power: 275W
RF power: 35W
Time: 60 min*

**Etch rate is approximately 0.05 μm per minute*
Therefore, to etch 2.5 μm of InGaAs/InP it took approximately 60 minutes

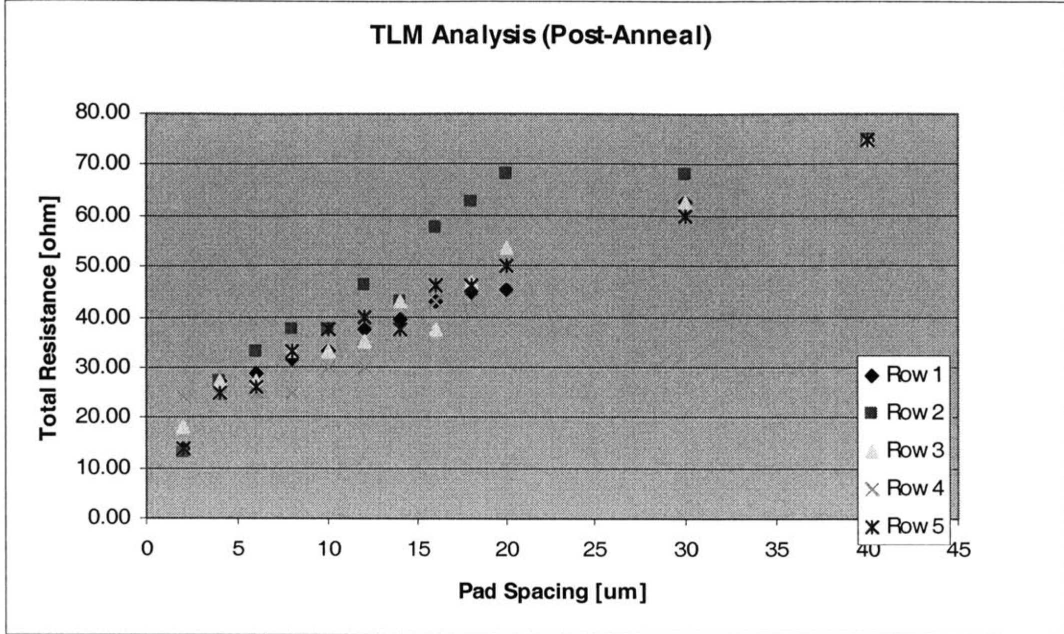
APPENDIX C: TRANSFER LENGTH METHOD DATA



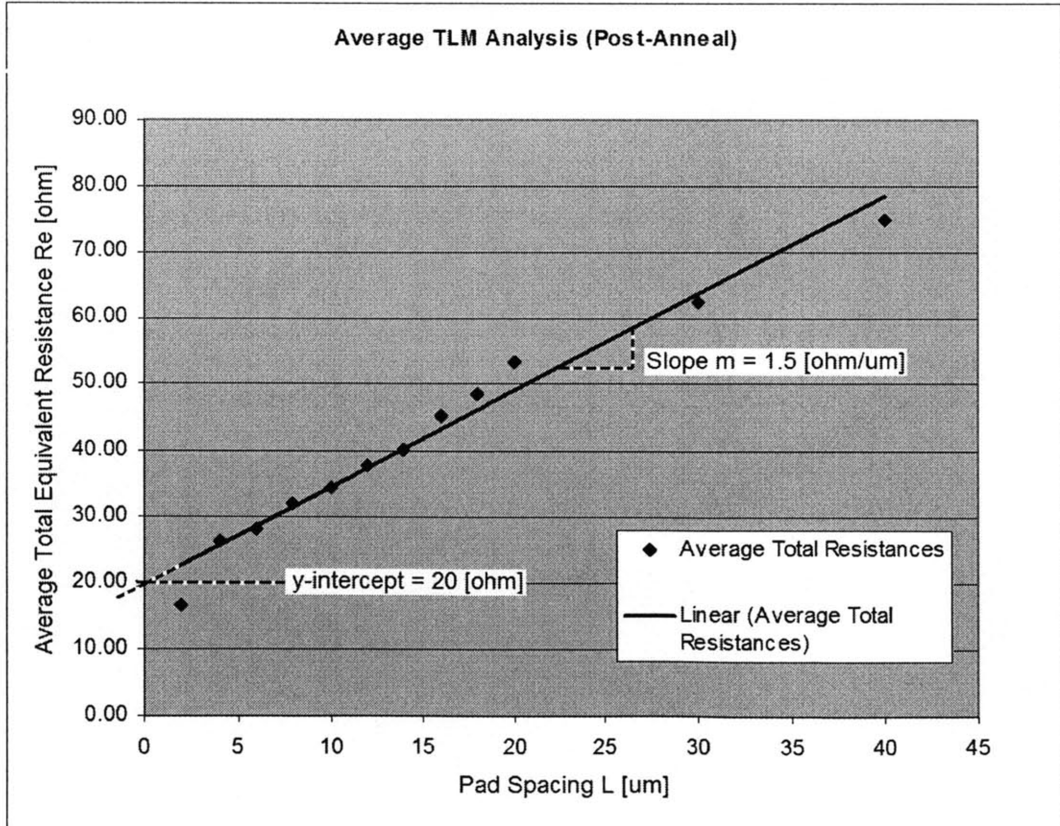
Pre-Anneal TLM Data Points



Pre-Anneal TLM Data Average Linear Approximation



Post-Anneal TLM Data Points



Post-Anneal TLM Data Average Linear Approximation

APPENDIX D: DRY-ETCH BCB PROCESSING PROCEDURES

The process procedure for the dry-etch CYCLOTENE 3022-35 advanced electronics resins described in this appendix is suggested by Dow Chemical Co. [35].

Step 1: Surface Preparation / Solvent Clean
Step 2: Adhesion Promoter (AP3000)

BCB Adhesion Promoter Application Recipe

Purpose	Speed [krpm]	Time [sec]
Dispense	1	15
Spin	2	20

Step 3: Coating BCB

BCB 3022-35 Application Recipe

Purpose	Speed [krpm]	Time [sec]
Dispense	0 .08	5
Spread	0.5	10
Spin	5	30

Step 4: Edge Bead Removal and Back side substrate clean with T1100 solvent
Step 5: Thermal Curing 320°C for 1 minute

The spin speed is inversely proportional to the final cured thickness as shown.

Typical Cured Thickness of 3022-35 BCB Films

Spin Speed [krpm]	Thickness [μm]
1	2.4
2	1.7
3	1.3
4	1.1
5	1.0

APPENDIX E: TENCOR P10 PROFILOMETER RECIPE

Scan Recipe

Parameter		Value
Scan Type	:	2D
Scan Direction	:	=>
Scan Length	:	225 µm
Scan Speed	:	20 µm/sec
Sampling Rate	:	50 Hz
Multi-Scan Average	:	1
Stylus Force	:	6 mg
Contact Speed	:	5
Vertical Range	:	13um/0.00
Profile Type	:	CENTER

PostProc Recipe

Parameter		Value
Filter Type	:	Gaussian
Noise Filter Cutoff	:	DEFAULT
Long Wave Filter	:	Off
Feature Detection	:	None
Fit and Level	:	Off

Cursors		X1	X2
Left Measurement	:	1.59867	1.59867
Right Measurement	:	219.017	219.017
Left Level	:	10.791	10.791
Right Level	:	196.636	196.636

General Parameters - normal trace

StpHt :	On	TIR :	On	Average:	On
Slope :	On	ProfL :	On	StpWd :	On
Area :	On	Area+ :	On	Area- :	On
Radius :	On	Edge :	On		

Waviness Parameters

Average:	On	RMS :	On	Peak :	On
Valley :	On	Wt :	On	Height :	On

Roughness Parameters

Average:	On	MaxRa :	On	RMS :	On
Peak :	On	Valley :	On	Rt :	On
Ht10pt :	On	Ht6pt :	On	Height :	On
Meanph :	On	Slope :	On	WaveL :	On
StdHt :	On				

Bearing Ratio (tp)

Status		Depth
Off	:	1 Å
Off	:	1 Å
Off	:	1 Å

Cutting Depth (CutDp)

Status		Ratio
Off	:	1
Off	:	1
Off	:	1

Peak Count (PC)

Status		Band
Off	:	1 Å
Off	:	1 Å
Off	:	1 Å

Mean Spacing Sm (1/PC)

Status		Band
Off	:	1 Å
Off	:	1 Å
Off	:	1 Å

High Spot Count (HSC)

Status		Height
Off	:	1 Å
Off	:	1 Å
Off	:	1 Å

Mean Spacing Sm (1/HSC)

Status		Band
Off	:	1 Å
Off	:	1 Å
Off	:	1 Å

APPENDIX F: SILICON PHOTODIODE CHARACTERIZATION

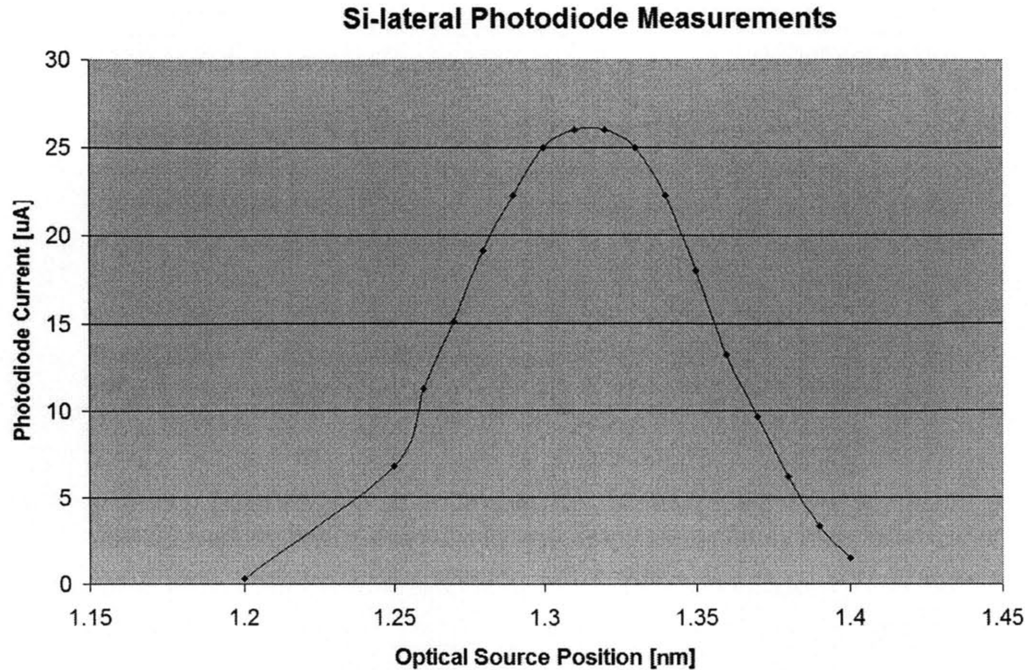
Silicon lateral photodiodes are simple to layout, fabricate, and easily integrated with Si-CMOS processes. The n- and p-type electrodes are formed at the surface of the device; the device is fabricated in CMOS process with identical steps as that used to form the source and drain of CMOS transistor structures.

A silicon lateral photodiode was characterized in comparison with the discrete III-V photodiodes. Previously designed by students in Professor Chandrakasan's group, this photodiode spanned approximately 100 μm by 100 μm, with finger width of 0.5 μm and adjacent spacing of 0.25 μm.

A circular optical source was swept across this square-shaped photodiode from varying distances. The generated photocurrent measured as a function of the optical source position is recorded in the table below.

Optical Source Position [nm]	Photodiode Current [uA]
1.2	0.3
1.25	6.8
1.26	11.2
1.27	15.1
1.28	19.1
1.29	22.3
1.30	25.0
1.31	26.0
1.32	26.0
1.33	25.0
1.34	22.3
1.35	18.0
1.36	13.2
1.37	9.6
1.38	6.2
1.39	3.3
1.40	1.5

The tabulated data are visually presented in the graph as shown below. As one can see, the current increased initially, flattened out, and then decreased as the optical source continued to move further away from the center of the photodiode active region.



This information was used to estimate the spot size, which was the width of the photodiode plus the distance for which the generated photocurrent appeared to be constant. The "flat" part of the current graph ranged approximately from 1.31 cm to 1.34 cm of the optical source distance. The difference calculated to be 0.03 nm, or 30 μm. Since the width of the silicon lateral photodiode was 100 μm squared, therefore, the spot size was 100 μm + 30 μm = 130 μm.

The total power in the beam used was 0.75 mW. The power input by area percentage can be calculated as $\frac{Power}{Area} = \frac{0.75}{100 \times 100} = 7.5 \times 10^{-5} \left[\frac{mW}{\mu m^2} \right] = 7.5 \left[\frac{W}{cm^2} \right]$.

BIBLIOGRAPHY

[1] G.E. Moore, “Progress in Digital Integrated Electronics,” *IEEE Int’l Electron Device Meeting Tech. Digest*, IEEE Press, 1975, pp. 11–13.

[2] “Intel Introduces Intel Pentium 4 Processors On High-Volume 90-Nanometer Manufacturing Technology”, Intel Press Release, Santa Clara, Feb. 2004. Available from the World Wide Web: <http://www.intel.com/pressroom/archive/releases/20040202comp.htm>

[3] “Interconnections for Gigascale Integration – Program Tasks”, Interconnect Focus Center, Georgia Institute of Technology, 2002. Available from the World Wide Web: <http://www.ifc.gatech.edu/tasks.shtml>

[4] D. L. Lile, “Optoelectronic Devices”, Chapter 16 in *Handbook of Compound Semiconductors - Growth, Processing, Characterization, and Devices*, edited by P.H. Holloway, G.E. McGuire, Park Ridge, N.J., Noyes / William Andrew Publishing, 1995, p. 813.

[5] A. Reisinger, et al, “Hybrid Integration: Production Ready.” Optoelectronic Technology, TeraConnect, Nashua, N.H. in EE Times, Feb. 20, 2002.

[6] B. Streetman, and S. Banerjee, *Solid State Electronic Devices*, Prentice Hall, New Jersey, 1999.

[7] R. Pu, C. Duan, and C. W. Wilmsen, “Hybrid integration of VCSEL's to CMOS integrated circuits”, *IEEE Journal of Selected Topics in Quantum Electronics*, Vol. 5, Issue 2, pp. 201–208, Mar.-Apr. 1999.

[8] K. W. Goossen, et al, "GaAs MQW modulators integrated with Silicon CMOS", *IEEE Photonis Technol. Lett.*, 1995, 7, (4), pp. 360-362.

[9] J. F. Ahadian, P. T. Vaidyanathan, S. G. Patterson, Y. Royter, D. Mull, G. S. Petrich, W. D. Goodhue, S. Prasad, L. A. Kolodziejski, and C. G. Fonstad, Jr., “Practical OEIC’s Based on the Monolithic Integration of GaAs–InGaP LED’s with Commercial GaAs VLSI Electronics,” *IEEE Journal of Quantum Electronics*, vol. 34, no. 7, pp. 1117-1123, 1998.

[10] C. G. Fonstad, "Very large scale monolithic heterogeneous optoelectronic integration: the Epitaxy-on-Electronics, Silicon-on-Gallium Arsenide, and Aligned Pillar Bonding techniques" in Heterogeneous Integration: Proceedings of a Conference held January 25-26, 2000 in San Jose, CA edited by Elias Towe (Critical Reviews of Optical Engineering, Vol. CR76, SPIE Optical Engineering Press, Bellingham, WA, 2000) Chapter 1.

[11] N. A. Drego, “A Low-Skew, Low-Jitter Receiver Circuit for On-Chip Optical Clock Distribution,” Master of Science Thesis, MIT EECS, June 2003.

[12] S. Rusu, and S. Tam, "Clock Generation and Distribution for the First IA-64 Microprocessor", *Proc. of IEEE Int. Solid-State Circuits Conf*, pages 176–177, 2000.

[13] J. Perkins, Master of Science Thesis, MIT EECS, Aug. 2002; J. Rumpler, Master of Science Thesis, MIT EECS, Dec. 2002.

[14] Kallmayer, et al, "Self-Aligning Flip-Chip Assembly Using Eutectic Gold/Tin Solder in Different Atmospheres", *IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium*, pp. 18-25. 1996.

[15] E. Atmaca, et al, "Development of RM^3 Technology to Integrate P-i-N Photodiodes on Si-CMOS for Optical Clock Distribution", MANTECH Extended abstract, 2004.

[16] A. Katz, "Physical and Chemical Deposition of Metals as Ohmic Contacts to InP and Related Materials", Chapter 4 in *Handbook of Compound Semiconductors - Growth, Processing, Characterization, and Devices*, edited by P. H. Holloway, G. E. McGuire, Park Ridge, N.J., Noyes / William Andrew Publishing, 1995.

[17] V. L. Rideout, "A Review of the Theory and Technology for Ohmic Contacts to Group III-V Compound Semiconductors", *Solid State Electronics*, 18, 1975, pp. 541–550.

[18] W. Shockley, "Research and investigation of inverse epitaxial UHF power transistors," Technical Documentary Report AL TDR 64.207, AF Avionics Laboratory, Research and Technology Division, Air Force Systems Command, Wright –Patterson AFB, Ohio, Sept. 1964.

[19] A. Katz, C. R. Abernathy, and S. J. Pearton, "Pt/Ti Ohmic Contacts to Ultrahigh Carbon Doped p-GaAs Formed by Rapid Thermal Processing", *Applied Physics Letters*, 56 (11), 1990, pp. 1026–1030.

[20] T. P. Pearsall, and J. P. Hirtz, *J.Cryst. Growth*, 54, no.1, 1981, pp.127-131.

[21] L. G. Shanthrama, et al, "Evaluation of Single Ohmic Metallizations for Contacting Both p- and n-Type GaInAs", *Electronics Letters*, July 19, 1990. Vol. 26 No. 15, pp 1127-1129.

[22] Kuphal, E., *Solid-State Electron.,* 1981, 24:69.

[23] R. Kaumanns, N. Grote, H. G. Bach, and F. Fidorra, *Inst. Phys. Conf. Ser.,* 1987, 91:501.

[24] R. L. S. Devine, C. T. Foxon, B. A. Joyce, J. B. Celgg, and J.P. Gowes, *Appl. Phys.* 44, 1987, pp. 195.

[25] P. Auvray, A. Guivarch, H. L. Haridon, and J. P. Mercier, *Thin Solid Films,* 1985, 127:139.

[26] E. Kaminska, A. Piotrowska, A. Bercz, and J. Adamczewska, *J. Solid State Electron.*, 1986, 29:279.

[27] S. J. Pearton, U. K. Chakrabarti, and F.A. Baiocchi, *Appl. Phys. Lett.*, 55, 1633, 1989.

[28] D. J. Thomas, et al, "High Density Plasma Etch Processes for the Manufacture of Optoelectronic Devices based on InP", *GaAs Mantech*, 2001.

[29] K. Shinoda, K. Nakahara, and H. Uchiyama, "InGaAlAs/InP ridge-waveguide lasers fabricated by highly selective dry etching in CH_4:H_2:O_2 plasma", Indium Phosphide and Related Materials, 2003. *International Conference on 12-16 May 2003*, pp. 550–553.

[30] N. Saga, T. Masuda, T. Kishi, M. Murata, A. Yamaguchi, T. Katsuyama, "Low damage InP sidewall formation by reactive ion etching", *Indium Phosphide and Related Materials, 2001.* 14-18 May 2001, pp. 256-259

[31] N. Yamamoto, K. Kishi, Y. Kondo, S. Matsumoto, R. Iga, Y. Kadota, H. Okamoto, and H. Mawatari, "Ammonium sulfide combined etching (ACE): an effective treatment for reducing impurities prior to MOVPE InP regrowth in a process using hydrocarbon gas reactive ion etching (RIE)," *J. Crystl. Growth,* 193, 15, 1998.

[32] H. C. Duran, L. Ren, M. A. Py, O. J. Homan, U. Lott, and W. Bachtold, "High performance InP-based HEMTs with dry etched gate recess for the fabrication of low-noise microwave oscillators", *Indium Phosphide and Related Materials*, 16-20 May 1999, pp. 319–322.

[33] W. Hafer, J. W. Lai, and M. Feng, "Submicron InP-InGaAs Single Heterojunction Bipolar Transistors with fT of 377 GHz", *IEEE Electron Dev. Lett.* 24, 2003, pp. 292-294.

[34] Y. So, P. Garrou, J. Im, and D. Scheck, "Benzocyclobutene-based polymers for microelectronics", Chemical Innovation, Vol. 31, No. 12, Dec. 2001, pp. 40-47.

[35] "Processing Procedures for Dry-Etch CYCLOTENE Advanced Electronics Resins (Dry-Etch BCB)", The Dow Chemical Co., Midland, Nov. 1997.
Available from the World Wide Web:
<http://www.dow.com/webapps/lit/litorder.asp?filepath=cyclotene/pdfs/noreg/618-00200.pdf&pdf=true>

[36] B. Cakmak, "Fabrication and characterization of dry and wet etched InGaAs / InGaAsP / InP long wavelength semiconductor lasers", 1 July 2002, Vol. 10, No. 13, Optics Express, pp. 530-535.

[37] "Standard Operating Procedures", Microsystems Technology Laboratories, MIT.
Available from the World Wide Web:
<http://www-mtl.mit.edu/mtlhome/3Mfab/sop.html>