SILICON CARBIDE PROCESS DEVELOPMENT FOR MICROENGINE APPLICATIONS: RESIDUAL STRESS CONTROL AND MICROFABRICATION

by

DONGWON CHOI

Submitted to the Department of Materials Science and Engineering
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2004

Author: Dongwon Choi
Department of Materials Science and Engineering
October 29, 2003

Certified by: SM Spearing
Professor S. Mark Spearing
Associate Professor of Aeronautics and Astronautics
Thesis Supervisor

Certified by: Carl V. Thompson
Professor Carl V. Thompson
Stavros Salapatas Professor of Materials Science and Engineering

Certified by: Yet-Ming Chiang
Professor Yet-Ming Chiang
Kyocera Professor of Ceramics

Certified by: Martin A. Schmidt
Professor Martin A. Schmidt
Professor of Electrical Engineering and Computer Science
Director, Microsystems Technology Laboratories

Accepted by:
Professor Harry L. Tuller
Professor of Ceramics and Electronic Materials
Chairman, Departmental Committee on Graduate Students

SILICON CARBIDE PROCESS DEVELOPMENT FOR MICROENGINE APPLICATIONS: RESIDUAL STRESS CONTROL AND MICROFABRICATION

by

DONGWON CHOI

Submitted to the Department of Materials Science and Engineering
on October 29, 2003, in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

ABSTRACT

The high power densities expected for the MIT microengine (silicon MEMS-based micro-gas turbine generator) require the turbine and compressor spool to rotate at a very high speed at elevated temperatures (1300 to 1700 K). However, the thermal softening of silicon (Si) at temperatures above 900 K limits the highest achievable operating temperatures, which in turn significantly compromises the engine efficiency. Silicon carbide (SiC) offers great potential for improved microengine efficiency due to its high stiffness, strength, and resistance to oxidation at elevated temperatures. However, techniques for microfabricating SiC to the high level of precision needed for the microengine are not currently available. Given the limitations imposed by the SiC microfabrication difficulties, this thesis proposed Si-SiC hybrid turbine structures, explores key process steps, identified, and resolved critical problems in each of the processes along with a thorough characterization of the microstructures, mechanical properties, and composition of CVD SiC.

Three key process steps for the Si-SiC hybrid structures are CVD SiC deposition on silicon wafers, wafer-level SiC planarization, and Si-to-SiC wafer bonding. Residual stress control in SiC coatings is of the most critical importance to the CVD process itself as well as to the subsequent wafer planarization, and bonding processes since residual stress-induced wafer bow increases the likelihood of wafer cracking significantly. Based on CVD parametric studies performed to determine the relationship between residual stresses in SiC and H_2/MTS ratio, deposition temperature, and HCl/MTS ratio, very low residual stress (less than several tens of MPa) in thick CVD SiC coatings (up to ~50 μm) was achieved. In the course of the residual stress study, a general method for stress quantification was developed to isolate the intrinsic stress from the thermal stress. In addition, qualitative explanations for the residual stress generation are also offered, which are in good agreement with experimental results.

In the post-CVD processes, the feasibility of SiC wafer planarization and Si-to-SiC wafer bonding processes have successfully been demonstrated, where CVD oxide was used as an interlayer bonding material to overcome the roughness of SiC surface. Finally, the bonding interface of the Si-SiC hybrid structures with oxide interlayer was verified to retain its integrity at high temperatures through four-point flexural tests.

Thesis Supervisor: S. Mark Spearing
Title: Associate Professor of Aeronautics and Astronautics

ACKNOWLEDGEMENTS

First, I have to thank God for blessing me with the abilities and patience to make it to and through MIT, and the encouragement of many friends and family. The completion of this long endeavor would not have been possible without the help and encouragement of a great many people. I find myself lacking the words to tell the many important people in my life how much their help and support have meant to me. I apologize for any omissions; so many people deserve mention that I am sure to forget someone.

I am deeply grateful to my thesis advisor, Professor S. Mark Spearing, for his guidance and unwavering support throughout my stay at MIT. He always supported my research work even at times when I doubted its merits. Most importantly, I will remember the consistent friendship he has shown me over the last five years. I would also like to thank my thesis committee members, Professors Carl V. Thompson, Martin A. Schmidt, and Yet-Ming Chiang, for their valuable insights and suggestions. Their counsel and advice helped me bring my research and this document to final fruition.

Tremendous thanks and credits must be given to my collaborators, Robert J. Shinavski at Hyper-Therm. Inc., and Hyung-Soo Moon, who played critical roles in fabricating several hundreds of CVD SiC wafers and designing Si-SiC hybrid turbine structures, respectively. I would also like to thank the colleagues of Prof. William Sharpe group at Johns Hopkins University, in particular Kamili Jackson, who performed mechanical tests on the MEMS SiC specimens that I had provided. Thanks also go to Skip Hoyt at the MIT Lincoln Laboratory for his efforts in the polishing and planarization of the SiC wafers in the very early stage of my process development. Also, special thanks to the other members of the Materials, Structures, and Packaging group (past and present), including Kuo-Shen Chen, Todd Harrison, Kevin Lohner, Bruno Miller, Erin Noonan, Jeremy Gregory, Andrew Ie, Dong-Jin Shim, Srikar Vengallatore, Christine Tsau, Carissa Tudryn, and Kevin Turner, for their help and support.

Special thanks go to the staff at the MIT Microsystems Technology Laboratories (MTL) and in particular, Daniel Adams, Kurt Broderick, Vicky Diadiuk, and Paul Tierney, for the long hours of training and advice on many microfabrication processes in the clean room. I would also like to thank the research staff of the MIT Center for Materials Science and Engineering (CMSE), particularly, Michael Frongillo, Timothy Mcclure, and Elisabeth Shaw, for their training and help with several important tools for materials characterization including SEM, TEM, AFM, and so on. Thanks to John Kane for his help with the mechanical tests in the basement of building 37 (TELAC).

I should also thank the other faculty and staff members on the MIT Microengine project (past and present), including Prof. Alan Epstein, Prof. John Brisson, Prof. Jack Kerrebrock, Prof. Jeffrey Lang, Prof. Steven Senturia, Prof. Ian Waitz, Dr. Choon Tan, Dr. Steven Umans, Dr. Arturo Ayon, Dr. Reza Ghodssi, Dr. Yifang Gong, Dr. Stuart Jacobson, Dr. Ravi Khanna, Dr. Carol Livermore, Dr. Norihisa Miki, Dr. Yoav Peles, Dr. Hongwei Sun, and Dr. Xin Zhang. Thanks should also go to all other graduate student members of the MIT Gas Turbine Laboratory (GTL) and the Microengine team (past and present), including Jinwoo Bae, Anthony Chobot, Taek Choi, Luc Frechette, Beilene Hao, Jinyoung Hong, Dan Kirk, Jinwook Lee, Vai-Man Lei,

Adam London, Jun Luo, Brenda MacLeod, Lodewyk Steyn, Amit Mehra, Jhongwoo Peck, Chris Protz, John Protz, Nick Savoulides, Boris Sirakov, Chris Spadaccini, Chiang-Juay Teo, and Huu Duc Vo, for their stimulus to my passion for excellence in research and good humor that made my life at the GTL a fun and rewarding experience. I also owe thanks to the staff of the GTL, especially, Paul Warren, Lori Martinez, Diana Park, Susan Parker, Holly Anderson, Julie Finn, and Mary McDavitt for their technical and administrative assistance.

Some of the best times I have spent in Boston have been with the members of Korean Graduate Students Association (KGSA) at MIT and other friends I made here, including Sanghoon Ahn, Choongyeon Cho, Jeeyoung Choi, Jihwan Choi, Yoonjoon Choi, Zungsun Choi, Minha Hwang, Gyooyeol Jung, Wonjoon Jung, Sunghoon Kang, Daekeun Kim, Dohyoung Kim, Heejae Kim, Jaejoong Kim, Jinsang Kim, Sungjee Kim, Kwanghee Koh, Yongnam Kwon, Daniel Lee, Jinwook Lee, Joonsuk Lee, Kevin Kidoo Lee, Kwangduk Lee, Seonah Lee, Youngsu Lee, Yongki Min, Cheolmin Park, Jinwoo Park, Joonsang Park, Sanghyuk Park, Taesoon Park, Joonil Seog, Michael Shin, Hyuntae Yoo, Jongseung Yoon, and so on. There are many, many more people that I could list here. Even though I am not naming all of you, I know my life has truly been enriched with your presence.

Almost finally, I would like to thank my girl friend, Shinwoo, for her consistent non-technical (emotional) support, patience, and unshakable belief in me. Thank you for keeping me sane and well fed, especially, while I was in "thesis mode". Finally, I thank my family for all of their support and never-ending love. My mother, father, grandmother, brother and sister-in-law, Jeonghyun and Jihye have been a constant source of motivation and encouragement. I owe them many of my accomplishments and very special thanks for always praying for me and believing in me.

This work was primarily supported by the United States Army Research Office, Dr. R. Paur and Dr. T. Doligalski, technical managers (ARO MURI #DAAG55-98-1-0292). Additional support was provided through an Army Research Laboratory Collaborative Technology Alliances (CTA) program, subcontracted by Honeywell Inc. (ARL CTA #DAAD19-01-2-0010). The financial support of all these institutions and individuals is gratefully acknowledged.

TABLE OF CONTENTS

Abstract 3
Acknowledgements 5
Table of Contents 7
List of Figures 11
List of Tables 15
1 Introduction to Power-MEMS 17
1.1 MIT micro gas turbine generators 17
1.1.1 "Demo" engine structures 17
1.1.2 System design and constraints 19
1.1.2.1 Turbomachinery: turbine and compressor spool 19
1.1.2.2 Bearing systems 20
1.1.2.3 Micro-combustor 20
1.2 Motivation for research 21
1.2.1 Microfabrication fundamentals and materials selection 21
1.2.1.1 Basic MEMS fabrication techniques 21
1.2.1.2 All-silicon demo engine fabrication 23
1.2.1.3 Limitation of single-crystal silicon as a high temperature material 25
1.2.1.4 Refractory materials selection - CVD SiC 26
1.3 Research objectives and approaches 27
1.4 Organization of thesis 29
1.5 References 32
2 Silicon-Silicon Carbide Hybrid Turbine Structures Concept 33
2.1 SiC fabrication routes and process compatibilities 33
2.1.1 Crystalline structures and material properties of SiC 33
2.1.1.1 Crystalline nature of SiC 34
2.1.1.2 Hardness and chemical inertness of SiC 38
2.1.2 SiC etching techniques and difficulties 39
2.1.2.1 Wet chemical etching of SiC 39
2.1.2.2 Dry etching of SiC 41
2.2 Design of turbine and compressor structures 43
2.2.1 Consideration of SiC process compatibilities and difficulties 43
2.2.1.1 Positive, negative, and hybrid mold concepts 43
2.2.1.2 Selection of viable concept: Si-SiC hybrid structures 44
2.2.2 Si-SiC hybrid turbine structures and potentials 45

2.3 Fabrication of Si-SiC hybrid turbine structures 48
2.3.1 Overview of key process steps 48
2.3.2 Critical issues of each of the process steps 48
2.3.2.1 Chemical vapor deposition (CVD) of SiC on silicon substrates 48
2.3.2.2 SiC planarization / polishing 49
2.3.2.3 Si-SiC wafer bonding 49
2.4 References 51
3 Characterization of CVD Silicon Carbide On Silicon Wafers 53
3.1 Chemical vapor deposition of SiC on Si 53
3.1.1 Fundamentals of CVD SiC 53
3.1.2 Basic process conditions for the present study 54
3.2 Physical characterization of CVD SiC on Si wafers 56
3.2.1 Surface of CVD SiC 57
3.2.2 Wafer coverage and conformality 58
3.2.3 Thickness uniformity of SiC coatings 61
3.2.4 Microstructures 64
3.3 Mechanical properties of CVD SiC 67
3.3.1 Bulk properties of SiC 67
3.3.2 Mechanical properties of CVD SiC films 68
3.3.2.1 Biaxial flexural strength tests by Hyper-Therm 68
3.3.2.2 Tensile tests using ISDG technique by Johns Hopkins University 73
3.3 References 80
4 Residual Stress Control In CVD Silicon Carbide 81
4.1 Components of residual stress and calculations 81
4.1.1 Components of residual stress in polycrystalline materials 81
4.1.1.1 Thermal residual stress 81
4.1.1.2 Intrinsic residual stress 82
4.1.2 Residual stress calculation using laminated plate theory 82
4.1.2.1 Calculation of thermal residual stresses in SiC and Si layers 84
4.1.2.2 Calculation of intrinsic residual stress in SiC layer 86
4.2 Residual stress control in SiC by changing CVD parameters 87
4.2.1 Gas ratio vs. residual stress 87
4.2.2 Deposition temperature vs. residual stress 88
4.2.3 HCl concentration vs. residual stress 89
4.2.4 SiC thickness vs. residual stress 90
4.2.5 Si (substrate) thickness vs. residual stress 92
4.2.6 Wafer curvature measurements as a function of temperature 92
4.2.7 Summary of residual stress control in CVD SiC 95
4.3 Origins of residual stresses in CVD SiC 95
4.3.1 Origin of thermal residual stress 95
4.3.2 Origins of intrinsic residual stresses 96

4.3.2.1 Compositional study of CVD SiC 96
4.3.2.2 Surface stress of SiC 101
4.3.2.3 Qualitative explanation of variation of compression with CVD parameters 103
4.3.2.4 Tensile stress development due to grain coalescence 106
4.3.2.5 Discussion of the relaxation process during further growth 107
4.4 Another approach to tackle residual stress - SiC/SiN_x layers 108
4.5 References 110
5 Planarization and Wafer Bonding Processes of CVD Silicon Carbide 113
5.1 Planarization / Mechanical polishing of SiC 113
5.1.1 Difficulties in SiC polishing 113
5.1.1.1 Chemical mechanical polishing (CMP) 114
5.1.1.2 Mechanical polishing - process of choice for Si-SiC hybrid structures 117
5.1.2 Sources of wafer failures during planarization 118
5.1.2.1 Residual stress in SiC coatings 118
5.1.2.2 Thickness gradient of SiC coatings 120
5.1.2.3 Rough SiC coatings on wafer edges - large nodules 120
5.1.3 Approaches to improve SiC polishing process 122
5.1.3.1 SiC deposition on both Si faces 122
5.1.3.2 CVD process using modified wafer fixtures 122
5.1.3.3 Turning over wafers during planarization 123
5.1.3.4 Si shadow masking - approach to minimize unwanted SiC deposition 124
5.1.4 Remaining problems 126
5.2 Si-SiC wafer bonding using CVD oxide as an interlayer material 128
5.2.1 Deposition of PECVD oxide on polished SiC surface 129
5.2.2 CMP of CVD oxide 131
5.2.3 Pre-bonding at room temperature followed by high temperature anneal 132
5.2.4 Problems in SiC/oxide-to-Si wafer bonding 135
5.2.5 Si-SiC wafer bonding result and discussion 136
5.2.6 General approaches towards successful SiC/oxide-to-Si wafer bonding 138
5.3 References 140
6 Mechanical Tests of Bonded Silicon-Silicon Carbide Wafers 141
6.1 Measurement of bond strength 141
6.1.1 Methods of measuring bond strength 141
6.1.2 Four-point flexure method 145
6.2 Four-point bending tests of Si-SiC specimens at room temperature 147
6.2.1 Specimen fabrication 147
6.2.2 Test apparatus 149
6.2.3 Test procedure 151
6.2.4 Test results 151
6.3 Bonding integrity of Si-SiC specimens at high temperatures 153
6.3.1 Appatus for high temperature four-point bending test 153

6.3.2 Test procedure 155
6.3.3 Test results 155
6.4 Discussion of the test results 158
6.4.1 Comparison between the results of room and high temperature tests 158
6.4.2 Discussion of the effect of oxide interlayer on structural integrity 163
6.5 References 165
7 Conclusions and Future Work 167
7.1 Overall summary 167
7.2 Conclusions 169
7.3 Contributions 170
7.4 Future work 171
7.5 References 173
Appendix 175
A Kinetic processes invovled in SiC deposition on Si substrate 175
B Thermal expansion coefficients of silicon carbide and silicon 178
References for Appendices 181

LIST OF FIGURES

Figure 1-1 (a) Cross-sectional view of the demo microengine turbojet. The device is axisymmetric about the centerline. (b) 3-D forward and aft views of the demonstration turbojet. The compressor and turbine rotor are shaded in dark gray 18

Figure 1-2 (a) Demo engine six-wafer stack assembly. (b) Infrared (IR) image of a bonded wafer stack 24

Figure 1-3 Strength as a function of temperature for silicon and CVD silicon carbide. Trends based on literature data from Pearson 1957, Mura 1996, Castaing 1981, Patel 1963, Huff 1993, Pickering 1990, Hirai & Sasaki 1991, Chen 1999 26

Figure 2-1 (a) Stacking sequence of 3C-SiC. (b) Stacking sequence of 6H-SiC 35

Figure 2-2 Schematics of β-SiC (cubic) and α-SiC (hexagonal) showing the tetrahedral structures ... 36

Figure 2-3 Atomic structures of 3C-SiC and Si: (a) Zinc-blende structure of 3C-SiC. (b) Diamond structure of Si 38

Figure 2-4 Illustration of positive, negative, and Si-SiC hybrid turbine rotor configurations 44

Figure 2-5 Proposed conceptual design of a Si-SiC hybrid turbine structure 45

Figure 2-6 Geometrical configurations considered in Moon's FE analyses 47

Figure 2-7 Key fabrication steps for the Si-SiC hybrid turbine structure 48

Figure 3-1 CVD reactor used for SiC 56

Figure 3-2 AFM image of the surface of an 85 μm thick SiC coating, which shows a mean surface roughness of 33 nm 57

Figure 3-3 SEM image of a 35 μm thick SiC coating 58

Figure 3-4 (a) CVD SiC filling a 100 μm wide by 150 μm deep trench 100. (b) Imperfect conformality of CVD SiC showing a keyhole-like pore along the centerline of the width of a trench 59

Figure 3-5 CVD SiC filling trenches of various aspect ratios 59

Figure 3-6 (a) CVD SiC perfectly fills trenches of an aspect ratio of 2.0 (25 μm wide by 50 μm deep trenches) when they are evenly placed 25 μm apart. (b) Image of higher magnification 60

Figure 3-7 Rounding of CVD SiC around the sharp corners of closely spaced negative mold features 61

Figure 3-8 Thickness profiles of CVD SiC from various batches of different target thicknesses 62

Figure 3-9 (a) Radial profiles of three CVD SiC coatings of different target thicknesses. (b) Normalized radial profiles of the three SiC coatings 63

Figure 3-10 Reduced radial profile (red dots) of the CVD SiC produced using the modified wafer fixtures 64

Figure 3-11 XRD analyses of three SiC coatings produced under different CVD conditions show different diffraction patterns. However, all three patterns show a strong preferred orientation of (111) planes at 35.6 ° 2θ 65

Figure 3-12 TEM image showing the strong preferential growth orientation of CVD SiC on (100) silicon wafers 66

Figure 3-13 (a) TEM image showing the acicular grains and stacking faults. (b) TEM image showing a perpendicular image of columnar grains with twinning 66

Figure 3-14 (a) Schematic of biaxial flexural strength test fixture. (b) Procedure of the biaxial strength test 69

Figure 3-15 Results of biaxial flexural strength tests of CVD SiC and Si at room and elevated temperatures 70

Figure 3-16 (a) Cumulative probability of failure of CVD SiC at room temperature. (b) Weibull plot of the biaxial flexural strength tests at room temperature 72

Figure 3-17 (a) Weibull plot of the biaxial flexural strength tests at 600 °C. (b) Weibull plot of the biaxial flexural strength tests at 800 °C 73

Figure 3-18 (a) Schematics of the biaxial specimen and the metal markers. (b) Finished 73SiC tensile specimen 74

Figure 3-19 Schematics showing the basic principle of ISDG technique 76

Figure 3-20 Schematics of tensile testing equipment 76

Figure 3-21 Tensile test curve showing both the axial and lateral strains 77

Figure 3-22 Weibull analysis for the data obtained from ISDG tensile tests 78

Figure 4-1 Geometry of the SiC-Si two-layer laminate material 84

Figure 4-2 Residual stress variance with gas ratio α (H_2:MTS) 88

Figure 4-3 Residual stress variance with deposition temperature (°C) 89

Figure 4-4 Intrinsic stress variation with MTS/HCl ratio 90

Figure 4-5 Residual stress variance with SiC thickness 91

Figure 4-6 Intrinsic stresses for thin SiC layers 91

Figure 4-7 Intrinsic stresses variance with silicon substrate thickness 92

Figure 4-8 Variations of radius of curvature at a function of temperature: (a) 4.1 μm thick SiC in residual tension at room temperature. (b) 37 μm thick SiC in residual compression at room temperature 93

Figure 4-9 Conversion of radii of curvature of Figure 4-8 into residual stresses: (a) 4.1 μm thick SiC with a compressive intrinsic stress of ~100 MPa. (b) 37 μm thick SiC with a compressive intrinsic stress of ~240 MPa 94

Figure 4-10 SIMS analysis showing oxygen and nitrogen concentrations 98

Figure 4-11 XPS compositional analyses: (a) Sample 1 was in intrinsic compression of 296 MPa. (b) Sample 2 was in intrinsic compression of 536 MPa 99

Figure 4-12 Binding energies determined by XPS shows that only Si-C bonding (as SiC) can be detected within the bulk of the film as indicated by Si2p and C1s binding energies. N1s is

present only at the surface. SiO_2 and $Si_xO_yC_z$ bindings of Si2p can be detected as the surface to a depth of ~50 nm 100

Figure 4-13 (a) TEM image of SiC/SiN_x layered material. (b) A higher magnification image of SiC/SiN_x layered material 108

Figure 4-14 TEM image showing that the SiN_x interrupter layers deposited on SiC layers have amorphous structures 109

Figure 5-1 (a) Planarized wafer with dies of turbine-shape. (b) Magnified view of an individual die on the planarized wafer 118

Figure 5-2 (a) SEM image of the rough edge of an as-received Si wafer. (b) SEM image of the CVD SiC coated on the rough Si edge, which contains an abnormally grown large nodule 121

Figure 5-3 SEM image of the wafer edge coated with SiC using the modified wafer fixtures, in which no abnormally grown large nodule is found 123

Figure 5-4 (a) Planarized Si wafer with SiC reinforcements. (b) Cross-sectional view of the SiC reinforcements deposited into circular trenches 124

Figure 5-5 SiC deposition using Si shadow mask 125

Figure 5-6 Successfully planarized silicon wafer containing SiC reinforcements. The SiC was deposited using a shadow mask approach 126

Figure 5-7 Unwanted SiC deposition caused by slight misalignment 127

Figure 5-8 (a) Gas bleeding through the gap between mask and object wafers. (b) Unwanted SiC deposition around the target 30 μm deep circular trench 127

Figure 5-9 (a) Hydrogen bridges during wafer contact at room temperature. (b) Si-O-Si bonds formed after high temperature anneal 133

Figure 5-10 Abnormally grown large SiC nodule protruding out of 15 μm thick SiC coating 136

Figure 5-11 SiC-to-Si wafer bonding using CVD oxide as an interlayer material 137

Figure 5-12 Cross-sectional image of SiC/oxide-to-Si wafer bonding 137

Figure 6-1 Schematic of crack opening method – razor blade insertion 142

Figure 6-2 Schematic of blister test method 143

Figure 6-3 Schematic of the tensile test setup 144

Figure 6-4 Schematic of four-point flexure specimen 145

Figure 6-5 Procedure for creating a pre-crack: (a) Unnotched top layer is a Si wafer coated with CVD SiC layers (on both faces), which is bonded to the notched (by DRIE) bottom Si layer using PECVD oxide interlayer. (b) Following wafer bonding, a diesaw cut is made to complete the pre-crack 149

Figure 6-6 (a) Cross-section of a four-point flexure specimen showing the central pre-crack fabricated by DRIE and diesaw cutting. (b) Schematic showing a wider field of view 149

Figure 6-7 Configuration of a four-point flexure specimen in the fixture with four loading rollers 150

Figure 6-8 Overall configuration of the room temperature four-point flexure test machine 150

Figure 6-9 (a) A typical load-displacement plot for a four-point flexure test at room temperature, which shows a complete plateau. (b) A load-displacement plot showing an incomplete plateau 152

Figure 6-10 Configuration of high temperature four-point flexure testing machine 154
Figure 6-11 High temperature four-point flexure test setup 154
Figure 6-12 Specimen fractures along mode I path: (a) Test at 850 °C. (b) Test at 950 °C 156
Figure 6-13 Load-displacement plot for a four-point bending test at 950 °C and a rate of 0.001 mm/sec 156
Figure 6-14 Four-point bending test of a 525 μm thick single-crystal Si specimen at 850 °C and a rate of 0.002 mm/sec 157
Figure 6-15 Geometries of cracks: (a) Interface crack. (b) Crack deflected into material 2 159
Figure 6-16 Energy release rate ratio $G_i / G_s^{\max}$ versus phase angle of loading Ψ for $\alpha = 0.5$ and $\beta = 0$ 160
Figure A-1 LPCVD reactor and wafer configurations 175
Figure B-1 Thermal expansion coefficients of Si and β-SiC as a function of temperature 180

LIST OF TABLES

Table 1-1 Thermo-mechanical properties of silicon 25
Table 2-1 Lattice parameters for difference polytypes of SiC 37
Table 2-2 Summary of FE calculations of the Si-SiC hybrid turbine rotor 47
Table 3-1 Bulk properties of SiC 68
Table 3-2 Mechanical properties of Hyper-Therm's CVD β-SiC measured using ISDG technique 77
Table 4-1 GDMS results of CVD SiC 97

CHAPTER 1

INTRODUCTION TO POWER-MEMS

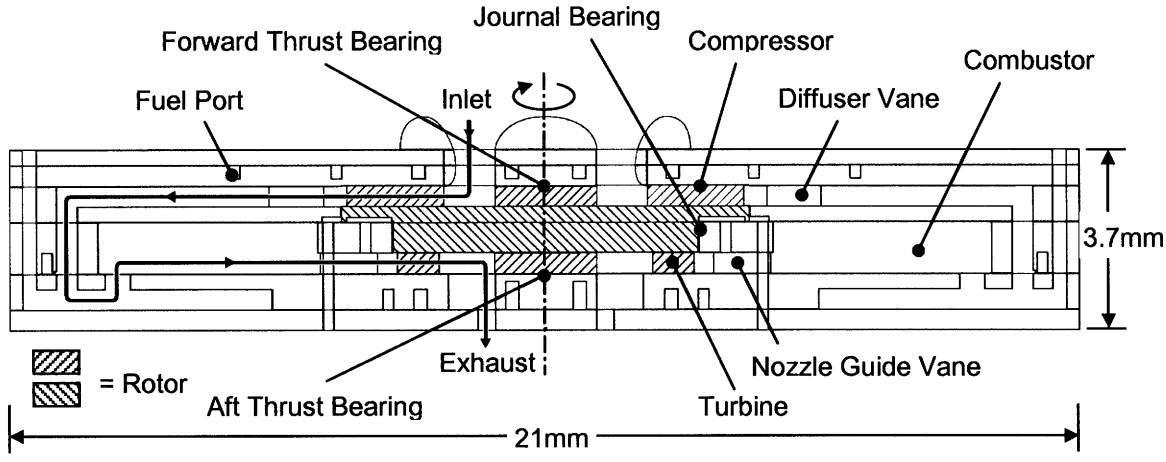
1.1 MIT micro gas turbine generators

Micro-electro-mechanical systems (MEMS)-based gas turbine engines are being developed by a large group of scientists and engineers at the Massachusetts Institute of Technology for use as button-sized portable power generators or micro-aircraft propulsion sources. The micro-gas turbine engines are intended to be capable of producing either 50 W of electrical power or 0.2 N of thrust in a package less than one cubic centimeter in volume. Such devices would have performance advantages over traditional compact power sources such as batteries and fuel cells. The cornerstone on which this effort is based is the ability to microfabricate refractory, structural ceramics with low density and high strength such as silicon carbide and silicon nitride, as well as single-crystal silicon, a conventional semiconductor material used for computer chips. The "microengines" can be considered the first of a new concept of MEMS devices, power-MEMS, which are characterized by the ability of generating high power in sub-centimeter-sized packages [1].

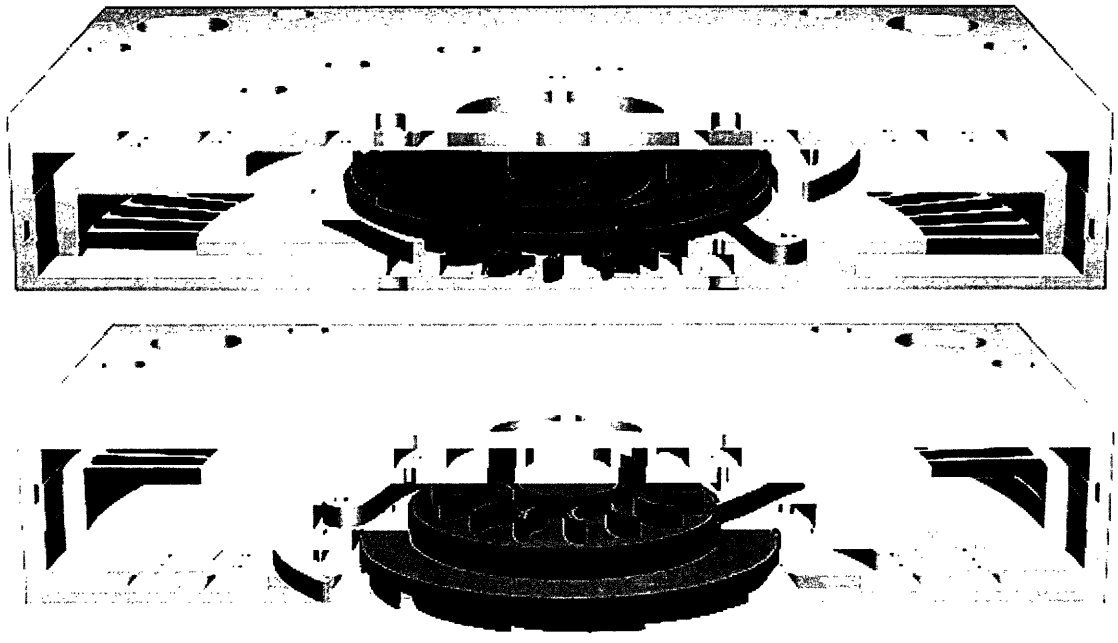
1.1.1 "Demo" engine structures

Initial efforts have been focused on the development of an all-silicon, hydrogen fueled microengine for the purpose of demonstrating the overall power-MEMS concept. The first prototype demonstration engine is a 21 mm square, 3.7 mm thick heat engine designed for an air flow of 0.36 grams/second and a hydrogen fuel burn rate of 16 grams/hour, producing either 10-20 W of electric power or 0.05-0.1 N of thrust. High

speed rotating turbomachinery, which is located at the core of the microengine, consists of an 8 mm diameter compressor and a 6 mm diameter turbine of which static and rotating structures are designed to operate at 1200 K and 950 K, respectively [2]. The cross-section of the "demo" engine and its three-dimensional schematic showing the compressor and turbine are illustrated in Figure 1-1.



(a)



(b)

Figure 1-1 (a) Cross-sectional view of the demo microengine turbojet. The device is axisymmetric about the centerline. (b) 3-D forward and aft views of the demonstration turbojet. The compressor and turbine rotor are shaded in dark gray [K. A. Lohner, S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, 1999].

1.1.2 System design and constraints

Microengines consist of many tiny individual components that must operate together in a reliable manner at extremely high rotational speeds and temperatures. This implies that the precise fabrication of microengines is extremely challenging, and thus, requires the intensive collaboration of many engineers specializing in turbomachinery and fluid dynamics, bearing and rotor dynamics, combustion, engine structures, materials, electronic circuits and controls, device fabrications and packaging. Due to the interdisciplinary nature of the microengine research, and the importance of the system constraints on the materials and microfabrication issues to be addressed in the bulk of this thesis, it is worthwhile reviewing the overall demo engine design.

The demo engine is composed of three primary subsystems: high speed rotating turbomachinery, gas bearing systems, and an annular micro-combustor.

1.1.2.1 Turbomachinery: turbine and compressor spool

The turbine and compressor disks are directly bonded together without any shaft. The bonded spool is designed for a structural temperature of 950 K, a rotational speed of 1.2 million RPM, and a compressor pressure ratio of 1.80. The upper limit of the design temperature is chosen to be 950 K as a consequence of considerations of the thermal softening of silicon; the yield strength of silicon drops significantly from about 1 GPa to 100 MPa as temperature increases from 900 K to 1000 K [3]. To cool the silicon turbine structure below 950 K, the demo engine spool is designed such that a heat flux of 50 W occurs from the turbine into the compressor. However, this heat transfer significantly compromises the engine efficiency. Moreover, when exposed to the centrifugal stresses caused by high rotational speeds, the turbine structure may even fail at temperatures lower than 950 K due to the creep mechanisms that are initiated at temperatures greater than approximately 40-60 % of the materials' homologous melting temperatures.

1.1.2.2 *Bearing systems*

To prevent the turbine and compressor rotors from colliding with adjacent wall surfaces, the spool is hydrostatically supported by a pair of forward and aft thrust bearings axially, and a circular journal bearing radially. Both the thrust and journal bearings are supplied with pressurized external air. The gaps of the forward and aft thrust bearings are 3.5 μm each, while the gap of the journal bearing is 15 μm. The bearing gaps are among the most critical of microengine dimensions, which are constrained by the microfabrication capabilities. Due to the very tight tolerance of the bearing gaps, any axial deflection or distortion of rotor blades caused by high centrifugal stresses can lead to catastrophic failures during the engine operation.

1.1.2.3 *Micro-combustor*

To generate power, the compressor discharge flow needs to be energized to rotate the turbine, which is achieved by burning fuel in a micro-combustor to convert the fuel's chemical energy to fluid thermal and kinetic energy [4]. A complete combustion process involves fuel mixing and combustion. Fuel mixing is the process of injecting fuel and dispersing it into the compressor discharge air to form a mixture of the fuel and air, while combustion involves the ignition and chemical reaction of the fuel and air mixture. The micro-combustor is a static structure, the design of which is much easier than that of a moving structure such as the rotating turbomachinery. However, due to the small size of the micro-combustor, achieving the physical and chemical processes required for complete combustion is highly constrained by the limited flow residence time.

The heat transfer through the walls of the micro-combustor is also a critical design problem since the high surface-to-volume ratio of the micro-combustor, which is two orders of magnitude larger than that of a conventional combustor, leads to a significant amount of energy loss. This energy loss could result in very low combustor efficiency. However, the large amount of heat transfer can be beneficial for structural integrity since the silicon wall temperature needs to be kept below 950 K to avoid an abrupt decrease in material strength at high temperatures. This is one of many examples in the microengine

project of engineering design problems representing a trade-off between several conflicting constraints.

1.2 Motivation for research

The high power densities expected for microengines require the turbine and compressor spool to rotate at a very high speed at elevated temperatures. The research presented in this thesis was motivated by extreme operational conditions, which require the development of proper engine materials and structures capable of withstanding high stresses at elevated temperatures, and ultimately achieving high power densities.

1.2.1 Microfabrication fundamentals and materials selection

Microfabrication or micromachining is the key to the creation of MEMS. Many techniques used for manufacturing MEMS devices were originally developed for the integrated circuit (IC) industry, which relies on silicon as the primary structural material, with lithography in concert with etching or deposition processes as the key patterning method [5].

1.2.1.1 Basic MEMS fabrication techniques

Basic fabrication tools for MEMS devices can be roughly divided into three major categories: surface micromachining, bulk micromachining, and LIGA or LIGA-like micromolding techniques.

Surface micromachining involves the deposition, patterning using photolithography, and selective etching of multilayered films to make device structures, where the substrate itself--in most cases, a single crystal silicon wafer--is not etched. Typically, layers of materials such as silicon dioxide, silicon nitride, and poly-crystalline silicon (polysilicon) are deposited to be used as a sacrificial material, an electrical isolation layer, and a

structural material, respectively. Surface micromachining is based on the same fabrication technologies as microelectronics, with some modifications for the formation of mechanical structures. Instead of etching the substrate, sacrificial thin film layers are first deposited on the substrate to provide an underlying platform for the deposition of structural layers [6]. Either or both of the sacrificial (silicon dioxide) and structural (polysilicon) layers are later etched to form (freestanding) components of the device. A final etch in hydrofluoric acid (HF) releases the movable mechanical components from the substrate and the other additive layers by etching the sacrificial silicon oxide layer. Reactive ion etching (RIE) is the most frequently used method to pattern the silicon dioxide and polysilicon layers since RIE plasmas provide high etch selectivity between polysilicon and silicon dioxide, which allows the anisotropic etching and multilevel processing to proceed through the polysilicon layer without damaging the underlying sacrificial oxide layer. In surface micromachining, the substrate is not etched. Instead, the substrate just provides the mechanical supports for the device. This is different from the typical case of bulk micromachining where the substrate is etched to form device components. Surface micromachining can also be distinguished from bulk micromachining by the thickness of the layers in which functional components are fabricated [7].

Bulk micromachining implies that select regions of the substrate--the bulk of the (silicon) wafer itself, typically with thicknesses of over 500 μm--are etched to form desired three-dimensional device structures, while surface micromachining refers to processing layers of polysilicon that are, at most, up to ~2 μm. The two typical ways to etch silicon wafers are isotropic and anisotropic etching. Isotropic etching etches silicon wafers in all crystallographic directions at almost the same rate, and thus, results in rounded (hemispherical or cylindrical) depressions on the wafer surfaces. On the other hand, anisotropic etching is performed using etchants such as potassium hydroxide (KOH), which etches certain crystallographic planes much faster than others. Therefore, anisotropic etching results in V-grooves or channels deep in the silicon surfaces. Bulk micromachining extensively uses deep reactive iron etching (DRIE), an aggressive type of RIE producing straight walled structures with very high aspect ratios, and wafer

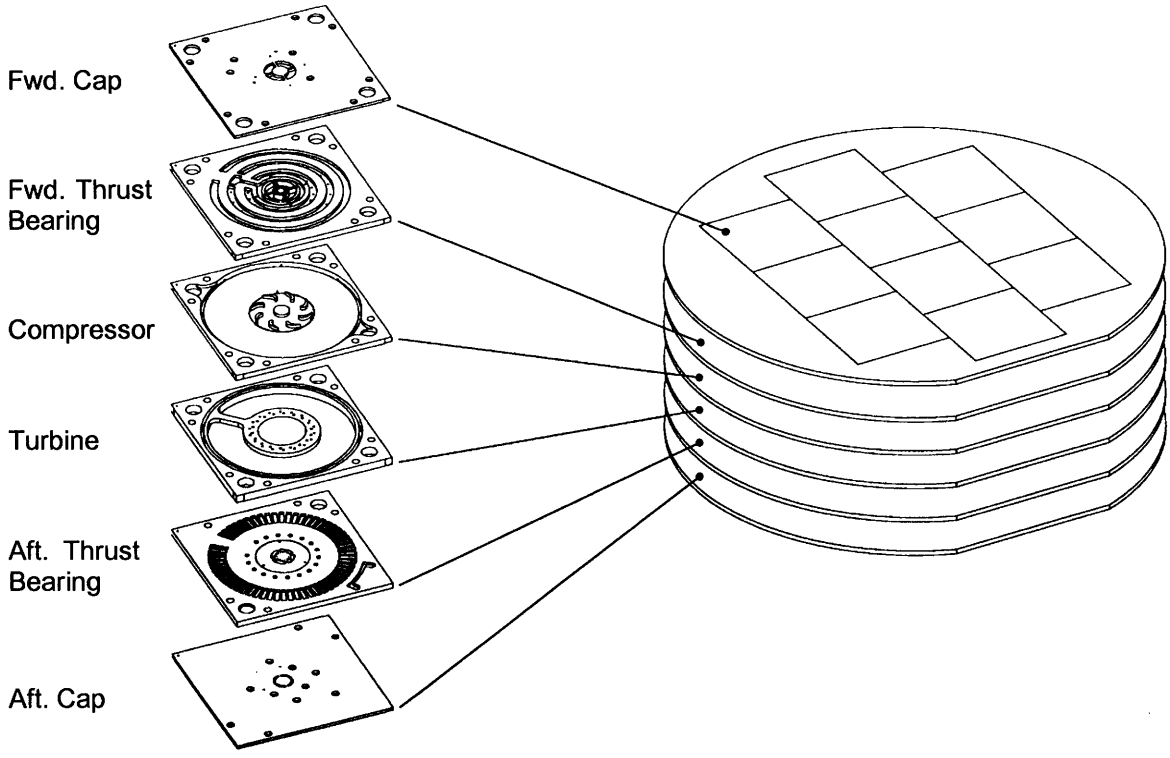
bonding techniques. A combination of bulk micromachining using DRIE and wafer bonding techniques offers a very powerful tool for producing three-dimensional mechanical structures of great complexity.

LIGA is a German acronym (LIthographie Galvanoformung Abformung) for lithography, electroplating, and molding. LIGA process uses X-ray synchrotron radiation as a lithographic light source, and subsequent electroplating and replication to produce high-aspect-ratio microstructures [8, 9]. It is capable of producing finely defined structures of up to 1000 μm high. A very thick X-ray sensitive photoresist, typically polymethylmethacrylate (PMMA), is irradiated by high-energy X-rays for patterning. Once the irradiated PMMA is developed, the remaining nonconductive mold is filled with a metal such as copper, nickel, and gold by electrodeposition. After dissolving the PMMA, the electroplated metal structures are removed from the substrate and used as mechanical components or as a mold insert for polymer replications using injection molding or hot embossing. Over the past decades, LIGA-like processes using UV radiation, instead of synchrotron radiation, have been developed. In addition to the development of new light sources for LIGA processes, new techniques other than polymeric replication have also been developed to extend the range of materials that can be used in LIGA; they include ceramic and metal injection molding, and cold pressing of nanoparticles.

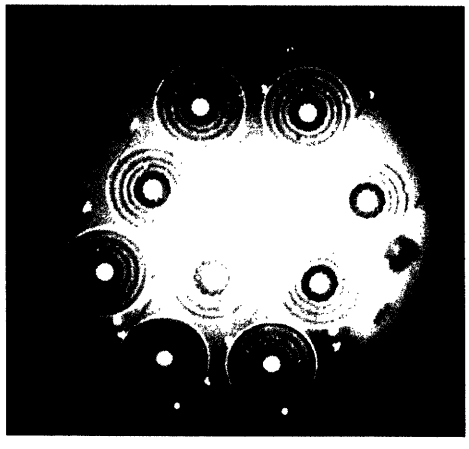
1.2.1.2 All-silicon demo engine fabrication

To minimize technical risks associated with manufacturing by taking advantage of the well-established precise silicon microfabrication techniques developed for the silicon IC industry, single-crystal silicon, the most commonly used material for semiconductor and MEMS devices, was chosen as the material for the demonstration microengine. The demo engine is made of six single-crystal silicon wafers that are individually etched using deep reactive ion etching (DRIE) to define two-dimensional features, and then bonded together to form three-dimensional complete engine structures; each wafer layer

corresponds to one or two engine components. The six-wafer stack assembly of the demo engine and an infrared (IR) image of the bonded wafers are illustrated in Figure 1-2.



(a)



(b)

Figure 1-2 (a) Demo engine six-wafer stack assembly. (b) Infrared (IR) image of a bonded wafer stack [A. H. Epstein et al., Microengine Program Review, MIT-Army Research Office Annual Review, MIT, 2000].

1.2.1.3 *Limitation of single-crystal silicon as a high temperature material*

From a mechanical strength point of view, single-crystal silicon has been observed to be sufficiently robust to serve as structural components such as beams and membranes in various MEMS devices including sensors and actuators. Basic mechanical and thermal properties of silicon are summarized in Table 1-1. The superior mechanical performance of silicon, however, is limited by its thermal softening behavior at high temperatures, as briefly mentioned in 1.1.2.1. As shown in Figure 1-3, the mechanical strength of silicon decreases significantly at temperatures above ~950 K, and thus, better refractory materials are necessary for applications involving higher temperatures.

Table 1-1 Thermo-mechanical properties of silicon

Material properties of silicon	Values
Density	2.33 [g/cm^3]
Elastic stiffness (at room temperature and atmospheric pressure)[1]	C_{11} = 165.6 [GPa] C_{12} = 63.9 [GPa] C_{44} = 79.5 [GPa]
Average Young's modulus[2]	E_{avg} = 165.6 [GPa]
Poisson's ratio[2]	ν = 0.218
Coefficient of thermal expansion (CTE)[3]	2.6 - 4.0 [10^{-6}/K]
Thermal conductivity[3]	125 - 150 [W/m-K]
Melting temperature	1414 °C

1. The data were reported by Hall [10]. Silicon is an anisotropic material (constructed from two interpenetrating face-centered cubic lattices), and thus, its mechanical properties are dependent on crystallographic orientations [3].
2. The approximation of isotropic behavior is often made for simplicity. The isotropic approximation was performed by Voigt averaging [11].
3. Most of mechanical properties are temperature-dependent [12].

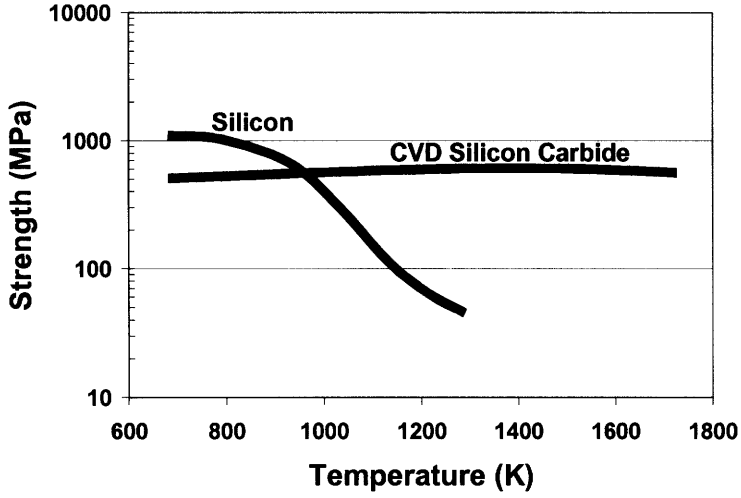


Figure 1-3 Strength as a function of temperature for silicon and CVD silicon carbide. Trends based on literature data from Pearson 1957, Mura 1996, Castaing 1981, Patel 1963, Huff 1993, Pickering 1990, Hirai & Sasaki 1991, Chen 1999 [K. A. Lohner, S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, 1999].

1.2.1.4 Refractory materials selection – CVD SiC

Figure 1-3, which shows the yield strength of silicon versus temperature, which implies that the hotter engine components made of silicon must operate at lower stress levels, and 950 K is a practical limit for highly stressed rotating components. The low strength of silicon at elevated temperatures dictates the critical need for developing refractory materials. Several high temperature materials ranging from metals to ceramics, which have been previously considered for conventional large-scale engine applications, were surveyed by Lohner, and their feasibilities were considered in terms of their thermo-mechanical properties and available routes for microfabrications.

From a high speed-rotating spool design standpoint, important mechanical properties of interest are failure (flexural) strength (σ_f), centrifugal strength ($\sigma_f^{1/2}/\rho$), maximum design or operating temperature, and thermal conductivity [12]. The centrifugal strength is important since it determines the maximum rotational speed of a turbine rotor; the rotor stress scales with the square of the rotor speed [2]. The maximum design or operating temperature up to which a material can maintain its strength and integrity without a

significant degradation, is critical for designing efficient spool structures since it determines the level of turbine cooling required for a given gas temperature. The thermal conductivity also has a strong effect on the engine efficiency as it determines the degree of heat transfer from the hot components (turbine rotor) to the cold components (compressor) of a given engine structure. In addition, resistance of a candidate material to creep and oxidation at high temperatures must also be taken into account.

Based on these criteria for materials selection, chemical vapor deposited (CVD) silicon carbide (SiC) was identified as the most promising candidate for the turbine structure of the microengine due to its high stiffness, toughness, and strength at elevated temperatures. Silicon nitride (SiN_x) was another candidate for the turbine structure, but SiC was eventually chosen since the film or coating thickness of silicon nitride is limited only to a few micrometers due to its extremely high level of residual stresses. Figure 1-3 shows that CVD SiC maintains its yield strength of about 600 MPa at temperatures up to 1700 K, while the yield strength of silicon decreases rapidly from about 1 GPa to 100 MPa as temperature increases from 900 K to 1000 K.

1.3 Research objectives and approaches

The research effort presented in this thesis falls within the scope of a larger project currently underway at MIT to develop micro gas turbine generators. As a part of the MIT microengine project, the research reported here was motivated by the critical need for incorporating SiC, an excellent structural material for high temperature MEMS applications, into silicon-based microengine structures.

SiC offers great potential for improved microengine efficiency due to its high stiffness, strength, and resistance to oxidation at elevated temperatures. However, techniques for microfabricating single-crystal SiC to the high level of precision needed for the microengine are not currently available due primarily to the lack of precise and

rapid SiC patterning and etching techniques. Moreover, any SiC fabrication route must be compatible with the other microengine fabrication processes such as wafer bonding and turbine release, which makes it extremely challenging to make all-SiC turbine structures [12, 13]. Therefore, it is critical that new microfabrication routes be developed to incorporate SiC into the silicon-based microengine structures.

To circumvent the technical difficulties caused by the lack of precise SiC microfabrication techniques, the approach adopted in this research is to develop silicon-silicon carbide hybrid turbine structures. The Si-SiC hybrid structure concept combines the chemical vapor deposition (CVD) of SiC on silicon wafers with post-deposition processes such as SiC planarization and wafer bonding to yield a turbine rotor that contains SiC reinforcements in strategic locations to increase its strength and stiffness at high operating temperatures.

The advantage of using the Si-SiC hybrid structures is that the performance of the microengines could be significantly increased by exploiting the superior SiC properties at elevated temperatures, while minimizing the technical difficulties caused by currently immature SiC microfabrication techniques. The great potential of the Si-SiC hybrid structures was verified by a series of finite element (FE) studies showing that a Si-SiC hybrid turbine structure with a 30 % SiC volume fraction can significantly increase the operating power levels of the microengine by increasing the allowable working temperature by 150-200 K [13, 14].

The goals of this research are to develop key processes required to realize the Si-SiC hybrid structures and verify their feasibility. Three key process steps for the Si-SiC hybrid structures are CVD SiC deposition on silicon wafers, wafer-level SiC planarization, and Si-to-SiC wafer bonding [15]. To realize the Si-SiC hybrid structures, the critical tasks to be performed include:

- Residual stress control of SiC coatings by optimizing chemical vapor deposition (CVD) process variables

- Development of a general method for residual stress calculation
- Development of post-CVD processes including SiC planarization and silicon to SiC wafer bonding using silicon oxide as an interlayer material
- Reliability tests of bonded Si-SiC specimens using four-point bend tests (at high temperatures up to ~1200 K)

1.4 Organization of thesis

The chapters of this thesis are organized according to the steps required to achieve the goals outlined in section 1.3.

Chapter 2 presents the basic concept of Si-SiC hybrid turbine structures from a microfabrication point of view. A brief review of the crystal structure and mechanical properties of SiC is given, followed by an introduction to the currently available microfabrication routes for SiC using silicon molds and their limitations. Analytical results performed to estimate the efficiency improvement obtained by incorporating SiC into Si based microengines are also reviewed. The chapter briefly describes three key process steps for the Si-SiC hybrid turbine structures: chemical vapor deposition (CVD) of SiC on silicon wafers, SiC planarization, and SiC-to-Si wafer bonding. The last section of the chapter identifies critical issues of each of the three process steps from both structural and fabrication standpoints.

Chapter 3 characterizes the material properties of chemical vapor deposited (CVD) SiC produced by Hyper-Therm, Inc., a collaborator of the MIT microengine team. The thickness uniformity and conformality of SiC deposited on silicon wafers is described, and a simple kinetic model is subsequently presented as an effort to understand the thickness variations of CVD SiC along the direction of the wafer diameter. Data for

important mechanical properties such as Young's modulus and Poisson's ratio of Hyper-Therm's CVD SiC are also presented.

Chapter 4 describes the efforts made to control residual stresses of thick CVD SiC films deposited on silicon wafers. The main concerns associated with SiC deposition on Si substrates are residual stress-induced wafer warping and cracking. To characterize the residual stress of SiC, the chapter identifies the major components of the residual stress in CVD SiC coatings. An analytical method based on classical laminated plate theory is developed and used to quantify the level of residual stress states in the SiC layers by separating the residual stress components from one another. The residual stress variations with deposition temperature, source gas ratio, SiC coating thickness, and Si substrate thickness are presented to provide engineering approaches to producing CVD SiC in the states of net-zero residual stress. A discussion on the origins of each of the residual stress components and a multilayered material composed of alternating SiC and SiN_x layers is given as another approach to achieving net-zero residual stress states.

Chapter 5 addresses important fabrication issues associated with two post-CVD processes: SiC planarization and SiC-to-Si wafer bonding. After SiC deposition, it is necessary to remove the excess SiC coatings for the subsequent wafer bonding process. Due to the chemical inertness of SiC, chemical mechanical polishing (CMP) is not yet available to improve the surface smoothness of SiC to the level adequate for direct wafer bonding. Therefore, a combination of mechanical polishing using diamond grit and the wafer bonding process involving CVD oxide deposition and subsequent oxide CMP is adopted in this research. The chapter describes the technical difficulties encountered during the SiC planarization, oxide deposition and CMP, wafer contact at room temperature, and high temperature annealing process which finalizes the wafer bonding process, along with the practical lessons learned from each of the process steps.

Chapter 6 investigates the bonding qualities of Si-SiC bonded wafer pairs to verify the strength and reliability of the Si-SiC hybrid structures during the engine operation at

high temperatures. The test specimens are cut from a bonded pair of Si and planarized SiC wafer with CVD silicon oxide as an interlayer material. The bond strength of the specimens is estimated using four-point bending tests at room temperature as well as high temperatures (up to ~1200 K) [13, 16]. A discussion is given on the observations of the delaminated (bonding) interfaces during the four-point bend tests, and the comparisons of the mechanical behavior of the Si-SiC hybrid structures with the structural model using FE analyses predicted by Moon [3].

Finally, Chapter 7 presents an overall summary of the research and recommendations for future work in this research area.

1.5 References

1. A. H. Epstein, S. D. Senturia, "Macro Power from Micro Machinery," Science Magazine, Vol. 276, p. 1211, May 1997.
2. J. Protz, "An Assessment of the Aerodynamics, Thermodynamics, and Manufacturing issues for the Design, Development, and Micro-fabrication of a Demonstration Micro Engine," Ph. D. Thesis, Dept. of Aeronautics and Astronautics, MIT, Cambridge, MA, 2000.
3. H.-S. Moon, "Design of Si/SiC Hybrid Structures for Elevated Temperature Micro-Turbomachinery," Ph. D. Thesis, Dept. of Mechanical Engineering, MIT, Cambridge, MA, 2002.
4. I. A. Waitz et al., "Combustor Research," The MIT Microengine Project, 2001 Annual Technical Report, MIT Proprietary, Cambridge, MA, 2001.
5. M. Madou, Fundamentals of Microfabrication, 1st edition, CRC Press, 1997.
6. M. Mehregany and C. A. Zorman, "Surface micromachining: A brief introduction," MRS bulletin, Vol. 26, No. 4, April 2001.
7. J. Elders, V. Spiering, and S. Walsh, "Microsystems Technology (MST) and MEMS applications: An overview," MRS bulletin, Vol 26, No. 4, April 2001.
8. J. Mohr, "LIGA – A Technology for Fabricating Microstructures and Microsystems," Sensors and Materials, 10, p. 363-373, 1998.
9. J. Hruby, "LIGA technologies and applications," MRS bulletin, Vol. 26, No. 4, April 2001.
10. J. J. Hall, Phys. Rev., Vol. 161, p. 756, 1967.
11. Properties of crystalline silicon, INSPEC, the Institution of Electrical Engineers, 1999.
12. K. A. Lohner, "Microfabricated Refractory Ceramic Structures for Micro-Turbomachinery," S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, Cambridge, MA, 1999.
13. B. Miller, "Hybrid Silicon/Silicon Carbide Microstructures and Silicon Bond Strength Tests for the MIT Microengine," S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, Cambridge, MA, 2000.
14. S. M Spearing et al., "Materials, Structures, and Packaging," The MIT Microengine Project, 2000 Annual Report, MIT Proprietary, Cambridge, MA, 2000.
15. D. Choi, R. J. Shinavski, W. S. Steffier, S. Hoyt, S. M. Spearing, "Process Development of Silicon-Silicon Carbide Hybrid Micro-Engine Structures," Mat. Res. Soc. Symp. Proc., Vol. 687, p. 197, Fall 2001.
16. K. T. Turner, "An Evaluation of Critical Issues for Microhydraulic Transducers: Silicon Wafer Bonding, Strength of Silicon on Insulator Membranes and Gold-Tin Solder Bonding," S. M. Thesis, Dept. of Mechanical Engineering, MIT, Cambridge, MA, 2001.

CHAPTER 2

SILICON-SILICON CARBIDE HYBRID TURBINE STRUCTURES CONCEPT

The Si-SiC hybrid turbine structures concept is a mid-term approach to increasing the microengine's performance by exploiting the superior SiC properties at elevated temperatures, given the limitations imposed by currently immature SiC microfabrication techniques. The design of a proposed Si-SiC hybrid turbine structure and the rationale leading to the conceptual design are described in this chapter along with a brief introduction of the key process steps required for the Si-SiC hybrid structure.

2.1 SiC fabrication routes and process compatibilities

Not many materials have been as extensively studied and used as Si, which implies that Si is still currently the most readily available material to fabricate delicate MEMS devices with. Therefore, from a fabrication standpoint, it would be advantageous if the reliable and proven Si microfabrication technology can be adopted as much as possible when designing microengines. In view of this, it would be worthwhile reviewing currently available SiC fabrication techniques, and their limitations and compatibilities with other Si fabrication steps required for the microengine.

2.1.1 Crystalline structures and material properties of SiC

Any discussion of silicon carbide (SiC) as a structural material for the hybrid turbine structures requires basic knowledge regarding the crystalline nature and key material properties of SiC.

SiC is an outstanding material for high temperature and high frequency microelectronics, thanks to its wide energy bandgap and high saturation drift velocity [1]. However, the great potential of Si-SiC hybrid turbine structures lies not in any of the electrical properties of SiC, but in the superior mechanical properties of SiC to which the following discussion is limited.

2.1.1.1 Crystalline nature of SiC

SiC is one of the most well known materials that exhibit polytypism, which is one-dimensional polymorphism. Polymorphism is the phenomenon of assuming different crystal structures with an identical chemical composition, which brings about three-dimensional variations in crystal structures. Polytypism is a special type of polymorphism, which takes place in certain close-packed structures where only a one-dimensional variation is allowed along the c-axis perpendicular to the close-packed planes [2].

SiC exists in more than 200 polytypes or stacking arrangements of the Si-C bilayers along the direction of closest packing. The arrangement of Si and C atoms in SiC is described as covalently bonded tetrahedra, as represented schematically in the circle of Figure 2-1(a) [3]. All polytypes of SiC have the identical Si-C bilayer arrangement in two dimensions, but they differ in terms of the stacking sequence of the bilayers in the third dimension, i.e., the c-axis perpendicular to the bilayers. Despite the large number of polytypes, the bilayer arrangement scheme allows only three crystalline structures: cubic, hexagonal, and rhombohedral.

The cubic SiC is referred to as β-SiC, and the hexagonal and rhombohedral phases are collectively known as α-SiC. The cubic SiC is also called 3C-SiC. 3C-SiC is the only cubic (zinc-blende) polytype known to exist, where the "3" indicates the number of bilayers in the unit cell; the stacking sequence is denoted ABCABCABC. The most common hexagonal polytypes are 4H-SiC and 6H-SiC, which have stacking sequences of ABCBABCB and ABCACBABCACB respectively. Both the cubic and hexagonal

structures occur in more complex intermixed forms producing the wide range of ordered hexagonal or rhombohedral structures [4]. The stacking sequences and the schematics of three-dimensional structures for 3C-SiC and 6H-SiC are illustrated in Figure 2-1 and Figure 2-2, respectively.

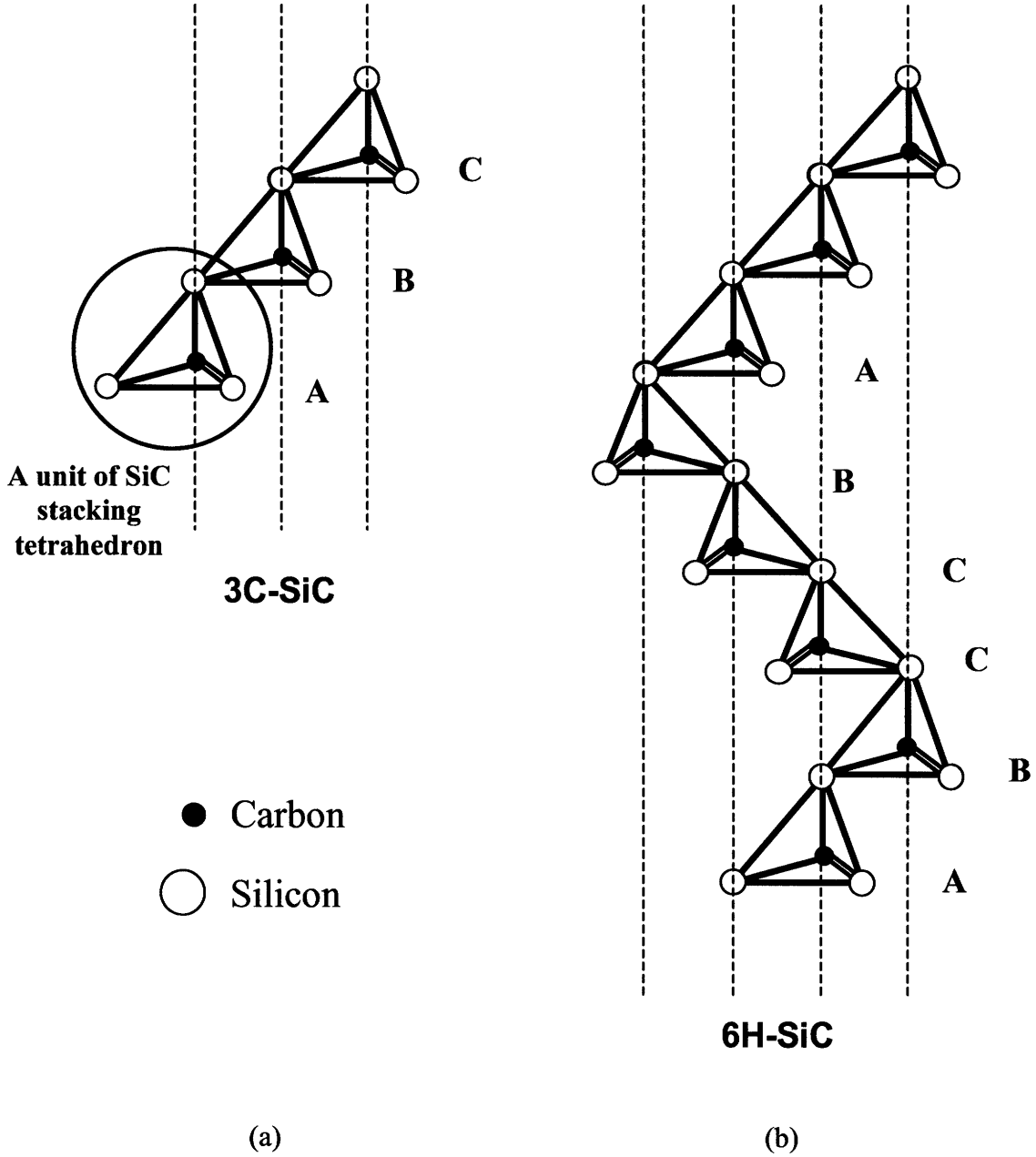


Figure 2-1 (a) Stacking sequence of 3C-SiC. (b) Stacking sequence of 6H-SiC [M. Mehregany et al., International Materials Reviews, Vol. 45, No. 3, 2000].

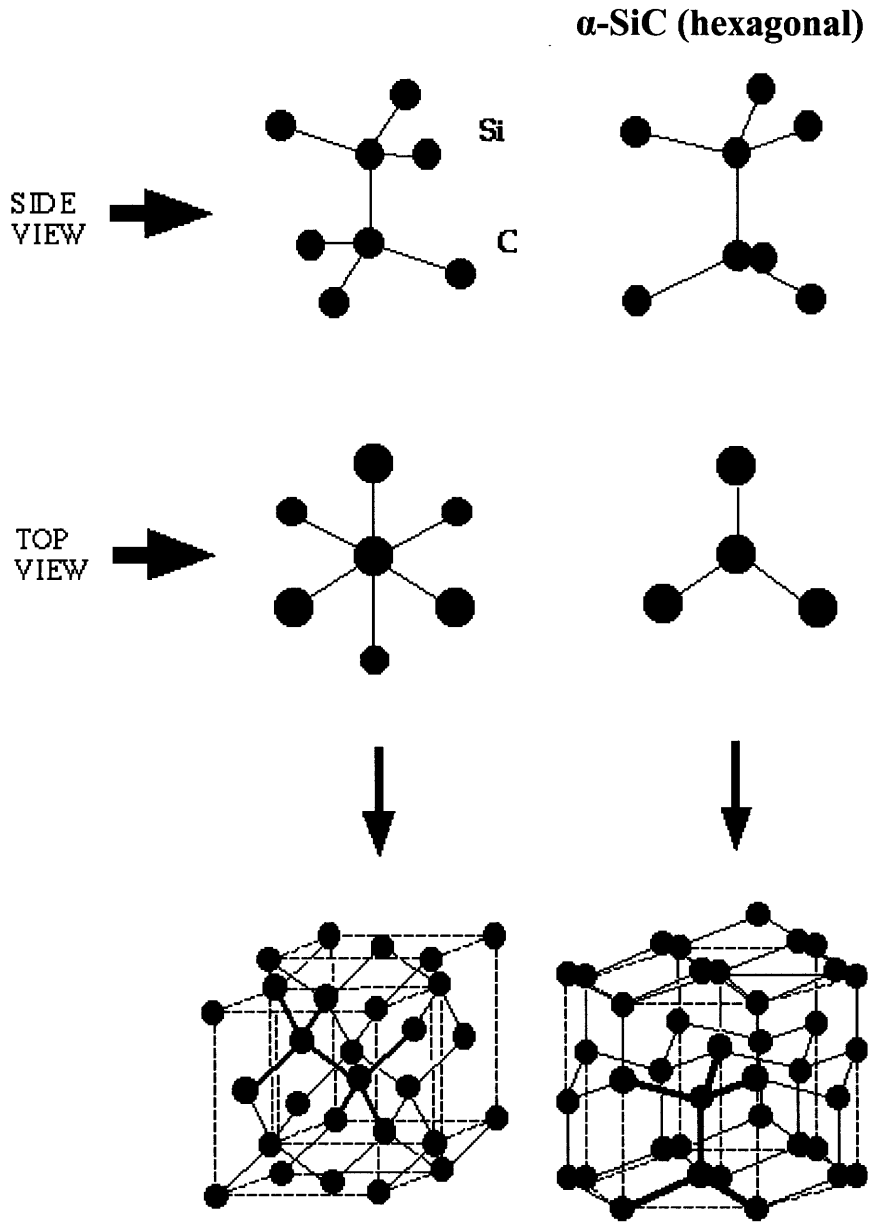


Figure 2-2 Schematics of β-SiC (cubic) and α-SiC (hexagonal) showing the tetrahedral structures [V. B. Shields, 1994, See "http://vshields.jpl.nasa.gov/SiC/CubicHex.html"].

Only 3C-SiC, 4H-SiC, and 6H-SiC are commonly used out of over 200 SiC polytypes due to the availability of conventional growth methods. Because the bonding

between Si and C is covalent and short-ranged, the characteristic of SiC structures can be understood in terms of a close-packed stacking of spheres with radii *a*/2, where '*a*' is the edge length of the unit tetrahedron, centered either at Si atoms or at C atoms, with central force interactions between nearest neighbors [5]. Under the assumption of close packing of spheres with only nearest neighbor interactions, the energy of a crystal is independent of the stacking order. Therefore, any close-packed structure has an equal probability of occurring. This could be the underlying explanation for the origin of polytypism in SiC. The large number of polytypes implies that the stacking faults are easily generated during the deposition or synthesis of SiC. The lattice parameters for 3C-SiC, 4H-SiC, and 6H-SiC are summarized in Table 2-1, and a comparison of the atomic structures of 3C-SiC (zinc-blende) and Si (diamond) is shown schematically in Figure 2-3.

To date, no single model is yet available to explain the formation and transformation of SiC polytypes. In general, however, 3C-SiC is stable at low temperatures, while 4H-SiC and 6-SiC are stable at higher temperatures. 3C-SiC can be grown at temperatures below 1000 °C, while 6H-SiC is formed at temperatures above 1400 °C. A transformation from β-SiC to α-SiC has been observed to occur at temperatures around 2000 °C [6].

Table 2-1 Lattice parameters for difference polytypes of SiC [7]

Polytype	Crystalline structure	Lattice constant a (Å)	Lattice constant c (Å)
3C-SiC	Face-Centered Cubic	4.3596	•
4H-SiC	Hexagonal	3.076	10.046
6H-SiC	Hexagonal	3.08065	15.11738

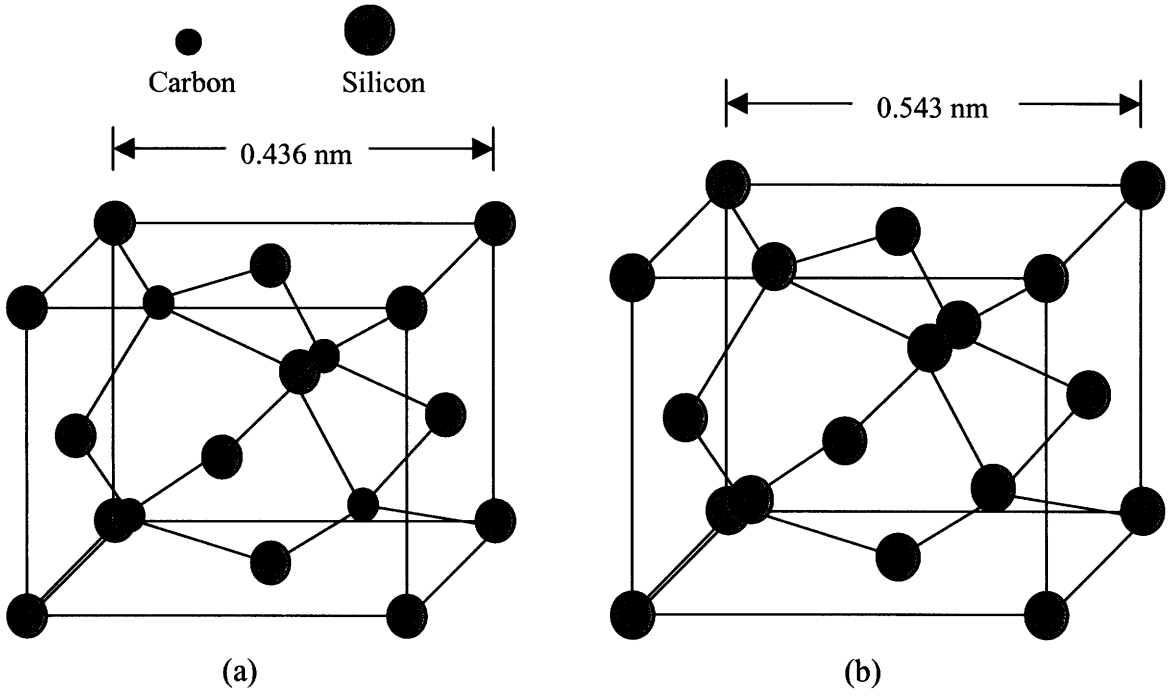


Figure 2-3 Atomic structures of 3C-SiC and Si: (a) Zinc-blende structure of 3C-SiC. (b) Diamond structure of Si [M. Mehregany et al., International Materials Reviews, Vol. 45, No. 3, 2000].

2.1.1.2 Hardness and chemical inertness of SiC

SiC has traditionally been used as an abrasive material owing to its excellent mechanical properties: hardness and wear resistance. SiC has a Mohs hardness of nine, as compared to 10 for diamond, the hardest natural material. The wear resistance of SiC is 9.15, as compared to 10 for diamond and 9 for Al_2O_3 [8].

SiC is well known for its remarkable chemical resistance to most acids, especially those used for silicon IC microfabrication. The chemical inertness of SiC can be attributed to the very strong Si-C bond, which must be broken before etching can occur. SiC can be etched by molten alkaline hydroxide bases such as potassium hydroxide (KOH), but this requires high temperatures above 400 °C. However, wet chemical etching--even at high temperatures--cannot be used for high-precision microfabrication or

patterning. It can only be used for etching along defects or grain boundaries for microscopic observations.

SiC does not melt, but sublimes at a temperature around 3000 °C, which is much higher than the melting temperature of silicon (1414 °C). A stable thermal oxide layer can be formed on the surface of SiC, but the oxidation rate is very slow compared with Si, which can also be attributed to the strong Si-C bond.

2.1.2 SiC etching techniques and difficulties

Most MEMS fabrication technologies have been developed on the basis of the process techniques that were originally designed for the silicon integrated circuit (IC) industry. This was largely due to the cost benefits that could be obtained by taking advantage of the well-established silicon IC technologies and microfabrication infrastructure. Therefore, any microfabrication techniques involving IC incompatible chemicals or high temperatures are not favorable and impractical. The chemical inertness of SiC, which requires extreme process conditions such as wet chemical etching using strong acids at very high temperatures, causes significant difficulties in the development of SiC fabrication processes. For this reason, microfabrication techniques for SiC with the precision comparable to those for silicon are not yet available to date.

2.1.2.1 Wet chemical etching of SiC

As previously noted, because of the chemical inertness of SiC, standard microfabrication techniques for silicon using wet chemical etchants are generally not applicable to SiC etching. Although some molten salts and molten metals have been proven to be effective in etching SiC, chemical etching at reasonable rates using molten salts can be performed only at very high temperatures ranging from 700 to 1000 °C, which is not compatible with standard silicon bulk micromachining processes [3]. The molten salt etchants effective in SiC etching at high temperatures include Na_2O_2, Na_2CO_3, and some alkaline hydroxide bases such as KOH and NaOH, and their etch rates vary

from 0.3 to 7 μm/min [7]. No etching mechanism is available for all polytypes of SiC. In other words, the SiC of one specific polytype may have different etching mechanisms from other polytypes of SiC. For 6H-SiC, wet etching generally requires the presence of oxygen to continue the etch reaction by facilitating the oxidation of (0001) planes of 6H-SiC. Recently, a similar mechanism based on the oxidation of silicon-terminated (0001) planes of 6H-SiC was suggested by Zhou et al. to explain the chemical reaction during the chemical mechanical polishing (CMP) of SiC, which will be revisited in Chapter 5 [9]. However, it is still unclear whether the same etching mechanism is applicable to different polytypes of SiC such as 3C-SiC.

Currently, the only known technique for SiC etching at room temperature is photoelectrochemical (PEC) etching where a set of SiC sample, standard calomel reference electrode (SCE), and platinum (Pt) counter electrode is placed in an HF solution to form an electrolyte required for the etching to take place. The etching reaction occurs by the dissolution of SiC following the chemical reaction shown below, where Si is first oxidized, followed by HF solution etching of the silicon oxide, while C is removed in the form of CO or CO_2 gases [10].

$$2SiC + 6H_2O + 12h^+ \rightarrow SiO_2 + CO_2 + SiO + CO + 12H^+$$

The chemical reaction is promoted by the formation of holes (minority carriers) near the SiC/electolyte interface. Therefore, for PEC etching of n-type SiC, which requires a generation of a large concentration of holes, a combination of a light source with proper intensity and an anodic potential applied to the SiC sample in an aqueous HF solution is used to photochemically dissociate the Si-C bond. On the other hand, for PEC etching of p-type SiC, any photoexcitation process is required since p-type SiC has already excess holes in it by its nature.

The Si-C bond energy is about 375 kJ/mol, which corresponds to a wavelength of 320 nm [11]. The wavelengths of various light sources range from 250 nm to 400 nm on which the etch rate is strongly dependent. PEC has mainly been used for 6H-SiC to make

high temperature pressure sensors [12]. However, for n-type 3C-SiC, two PEC etching techniques using a laser and an ultraviolet (UV) source have also been developed [11].

The PEC etching still suffers from the poor etching directionality, which is a common limitation for most wet chemical etching processes. In summary, wet chemical etching of SiC cannot be practically used primarily due to the lack of precision required for accurate dimensional control, and incompatibility with many of standard silicon microfabrication techniques.

2.1.2.2 *Dry etching of SiC*

Due to the unavailability of wet etching methods for SiC under practical conditions, dry etching has been the main focus of research efforts on SiC patterning. However, even dry (plasma) etching techniques suffer from relatively low selectivity over common masking materials since the chemical inertness of SiC requires physical bombardments using high fluxes of ions with high kinetic energy.

The most widely used dry etching technique is reactive ion etching (RIE), in which both chemical etching by the reactions of radicals in the plasma with target materials, and physical etching by ion bombardment play roles in the removal and patterning of target materials. In order for the etching to take place, it is necessary that the chemistry used for the plasma etching of SiC be reactive with SiC, and also the species produced by the chemical reactions be volatile to avoid any residues on the target surface. SiC RIE generally uses the same F-based plasma chemistries that have been developed for Si, Si_3N_4, and SiO_2, where silicon and carbon atoms are removed by different mechanisms separately. The most commonly used fluorinated compounds include NF_3, SF_6, CF_4, and CHF_3, and the etching mechanisms of SiC in these F-based chemistries can be described by the following separate reactions for each of the Si and C atoms [13]:

$$Si + 4F \rightarrow SiF_4$$
$$C + xF \rightarrow CF_x$$

As shown above, both Si and C are etched by the fluorinated species. However, it has been reported that some fluorine radicals may also play a role in the removal of C in certain cases. In most cases, the fluorinated compounds are mixed with O_2 to achieve higher etch rates by producing oxygenated species, which take part in removing C atoms, according to the following reaction [14]:

$$C + xO \rightarrow (CO, CO_2)$$

Anisotropy and etch selectivity over masking materials are of great importance in MEMS fabrication, in which deep etching is often required for structures with vertical sidewalls. If necessary, the sputtering component can be enhanced with the addition of inert gases such as He or Ar, which is often combined with high dc biases to accelerate the ions towards the target SiC surface. Enhancing the sputtering component is effective in creating vertical walls with high anisotropy because the direction of ion bombardment is parallel to the vertical sidewalls. Although effective in enhancing anisotropy, the sputtering component is not desirable in terms of etch selectivity. Common photoresists cannot stay intact when exposed to recipes containing oxygenated plasmas for SiC etching. The ion bombardment can even exacerbate the degradation of photoresists. Moreover, the etch recipes for SiC have significantly higher etch rates for polysilicon and SiO_2, two typical materials used for sacrificial layers and dielectric isolation in surface micromachining processes. For SiC samples heated to 300 °C, reasonably good etch selectivities of about 5:1 and 4:1 have been reported for SiC to Si and SiC to SiO_2, respectively [15]. However, the necessity for heating to high temperatures makes the process incompatible with many processes. To achieve high selectivity, hard materials such as Al or Ni are often used for masks. Although advantageous in terms of etch selectivity, metal masks could cause "micromasking", when they are sputtered by ions and redeposited on the target surface. The redeposited residues act as local masks and prevent the target surface from being uniformly etched, which results in a very rough etch surface. It has been reported that the occurrence of micromasking could be reduced by adding hydrogen to the etch chemistry or using graphite electrodes [16, 17].

2.2 Design of turbine and compressor structures

The microengine's performance can be significantly improved by reducing the heat transfer from turbine to compressor by introducing thermal barriers between the two rotor components. Decreasing the heat transfer, however, may cause the turbine wall temperature to increase, even up to a point when silicon starts to fail in yield and creep. Therefore, a high performance refractory material such as SiC has to be incorporated into the turbine and compressor spool. However, introducing SiC into the Si-based microengine gives rise to another issue, namely manufacturing difficulties associated with the currently immature microfabrication technology that are unable to meet the requirements for both precision and compatibility. The following sections describe the limitations involved in SiC fabrication in detail, and a design approach to achieve the high engine efficiency given the current state of microfabrication technology.

2.2.1 Consideration of SiC process compatibilities and difficulties

To circumvent fabrication difficulties, chemical vapor deposition (CVD) of SiC over pre-patterned silicon molds for the fabrication of the SiC turbine structures and their feasibility have been studied. Three mold concepts were suggested and their feasibilities were evaluated in terms of the process integration and compatibility with other process steps, the level of residual stress, and the conformality and structural defects such as micro-cracks in CVD SiC coatings [18]. They are positive mold, negative mold, and hybrid mold configurations.

2.2.1.1 Positive, negative, and hybrid mold concepts

The positive mold concept is to deposit a thin (<10 μm) layer of CVD SiC over a fabricated silicon turbine rotor to avoid direct exposures of the inner Si turbine structure to the high temperature environment for the purpose of increasing its stiffness and resistance to creep and oxidation at high operational temperatures. The negative mold

concept consists of fabricating the inverse pattern of the turbine rotor into the silicon substrate, and filling the mold cavity with thick CVD SiC. The Si mold is then selectively dissolved by a 1:1:2 solution of $HF/HNO_3/H_2O$ to yield a free standing SiC turbine rotor. The hybrid mold concept combines the CVD SiC deposition with post-deposition processes to yield a turbine rotor containing SiC reinforcements in strategic locations to locally reinforce the turbine structures. The three mold concepts are illustrated in Figure 2-4.

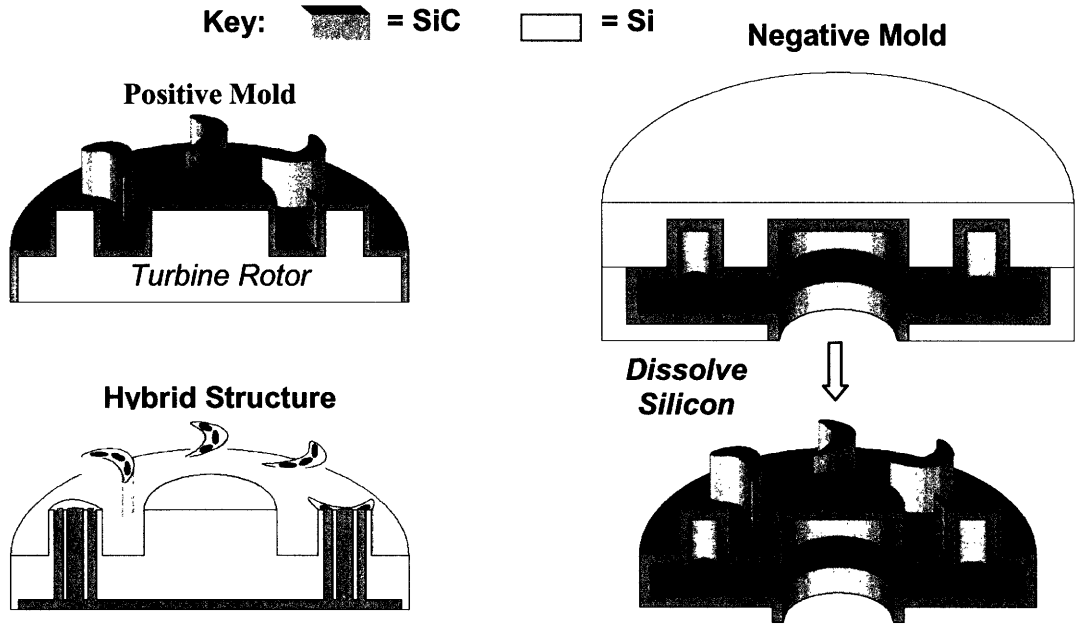


Figure 2-4 Illustration of positive, negative, and Si-SiC hybrid turbine rotor configurations [K. A. Lohner, S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, 1999].

2.2.1.2 Selection of viable concept: Si-SiC hybrid structures

Among the three mold concepts, the positive and negative mold techniques turned out to be impractical for the microengine fabrication. The positive mold concept has difficulties in yielding CVD SiC coatings that precisely conform to critical parts of the Si turbine rotor such as sharp blade fillet areas whose dimensions must be controlled within several μm. Moreover, this technique provides no obvious means of creating a

freestanding turbine rotor, and inserting in or bonding to other Si wafer stacks corresponding to other engine components. The negative mold concept is advantageous over the positive mold technique in terms of the ease of controlling the engine component dimensions. However, similar to the positive mold technique, this concept does not provide solutions to the problems of SiC bonding and suffers from the drawback of poor conformality near narrow cavity areas.

Considering the microfabrication difficulties in precisely making an all-SiC turbine rotor and the process compatibility with other microengine fabrication processes, such as wafer bonding and rotor release, it has been concluded that the Si-SiC hybrid (mold) concept is the most promising approach towards improving the microengine performance. The Si-SiC hybrid turbine concept is designed to minimize the technical difficulties involved in SiC fabrication as well as to maximize the use of precise Si microfabrication techniques.

2.2.2 Si-SiC hybrid turbine structures and potentials

Even when parts of the Si turbine structures undergo local plastic deformation, they may retain sufficient strength to maintain the structural integrity of the whole turbine structure, if reinforcement is achieved using small amounts of SiC.

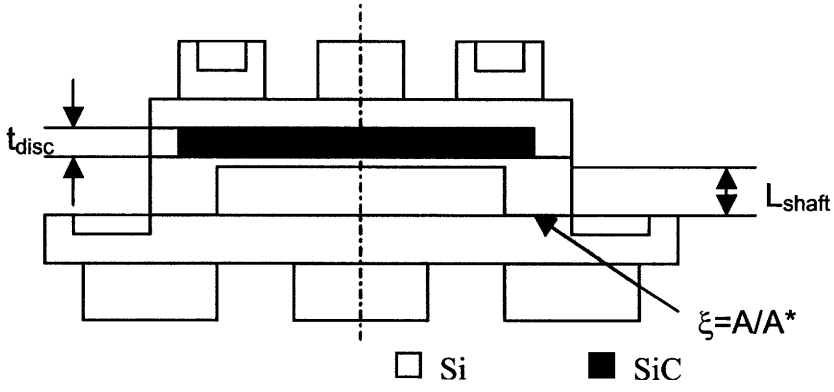


Figure 2-5 Proposed conceptual design of a Si-SiC hybrid turbine structure.

Figure 2-5 shows a schematic of a Si-SiC hybrid turbine structure, which was proposed with the intention of minimizing the technical risks involved in SiC fabrications, yet meeting the critical requirements for improving high temperature capabilities. The rationale for this structural design is the main focus of the discussions that follow.

The initial finite element (FE) study performed by Miller has shown that the Si-SiC hybrid turbine structures have a great potential to significantly increase the operating power levels of the microengine by increasing the allowable working temperature by 150-200 K [19]. Three-dimensional FE simulations for the Si-SiC hybrid turbine rotor have also been performed by Moon with a refined model combining the turbine disc and blades to corroborate Miller's structural analysis, in which the hybrid disc with SiC and blades had been considered as separate bodies. Four different hybrid blade and disc configurations were considered in Moon's 3-D simulation, as shown in Figure 2-6 [20]. As summarized in Table 2-2, the 3-D FE simulation results confirmed the potential of the Si-SiC hybrid structure concept for improving the microengine's efficiency by increasing the maximum allowable working temperature. Although there was little difference in the achievable maximum operating temperatures among the four cases, Case 2 (all-silicon hollow blade and disc reinforced with SiC) stood out as the best candidate for the hybrid turbine structure when microfabrication difficulties are taken into account. In addition, a one-dimensional cycle analysis performed by the system engineering group has also shown that a Si-SiC hybrid spool having a disc with 30 % SiC reinforcement and hollow blades would be capable of further enhancing the engine efficiency when combined with a design reducing turbine-to-compressor contact areas [21]. The percentage of the SiC reinforcement needs to be determined by considering the trade-off between the overall system requirement such as the maximum rotor speed, and the constraints imposed by SiC fabrication difficulties [22]. However, it is estimated that about 30~60 um thick SiC layer would be necessary to achieve the desired engine efficiency.

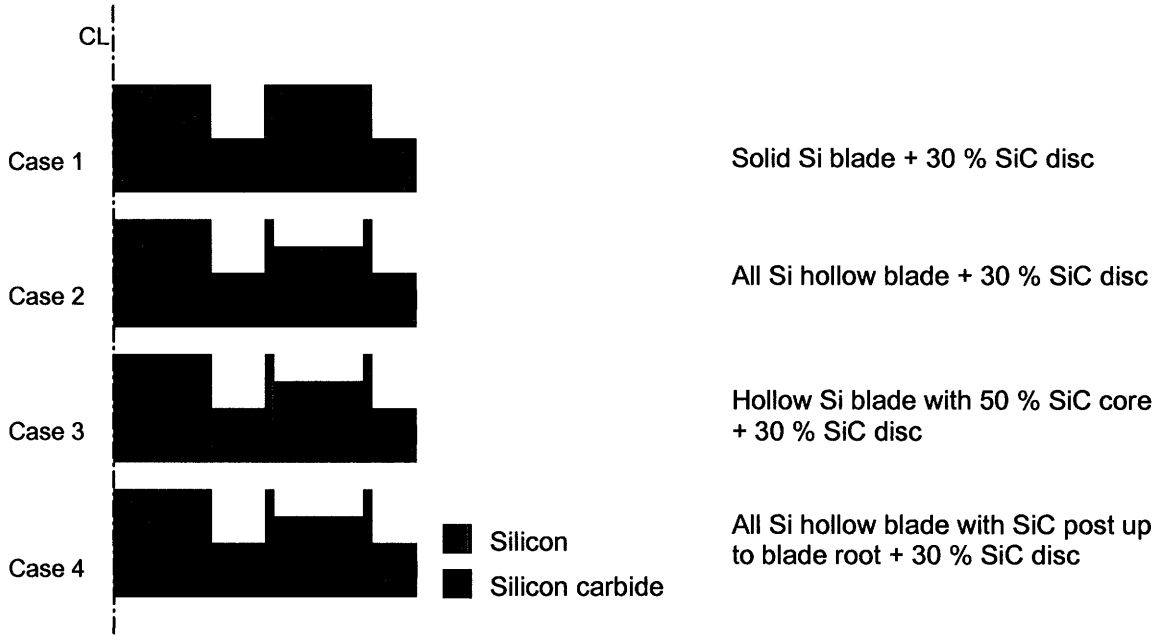


Figure 2-6 Geometrical configurations considered in Moon's FE analyses [H.-S. Moon, Ph. D. Thesis, Dept. of Mechanical Engineering, MIT, 2002].

Table 2-2 Summary of FE calculations of the Si-SiC hybrid turbine rotor [20]

Case	Max. temperature [K]	Max. stress in SiC [MPa]	Max. radial expansion [μm]	Max. tangential deflection [μm]	Max. vertical deflection [μm]
Solid Si blade + 30% SiC disc	1160	514	2.2	1.8	4.6
All Si hollow blade + 30% SiC disc	1175	509	2.1	2.0	4.0
Hollow Si blade with 50% SiC core + 30% SiC disc	1190	644	2.4	1.6	5.8
All Si hollow blade with SiC post up to blade root + 30% SiC disc	1175	510	2.0	1.7	3.9

* Stress and deflection values were obtained at the corresponding maximum temperature.

2.3 Fabrication of Si-SiC hybrid turbine structures

2.3.1 Overview of key process steps

Figure 2-7 outlines the key process steps required for the proposed Si-SiC hybrid turbine structures illustrated in Figure 2-5. The three main processes are chemical vapor deposition of SiC on a pre-patterned Si wafer corresponding to the turbine rotor, planarization of the SiC coated Si wafer, and wafer bonding between the planarized wafer and another Si wafer that will be microfabricated to form the compressor. The main issues and problems encountered in each of the process steps will be discussed in greater detail in the following chapters.

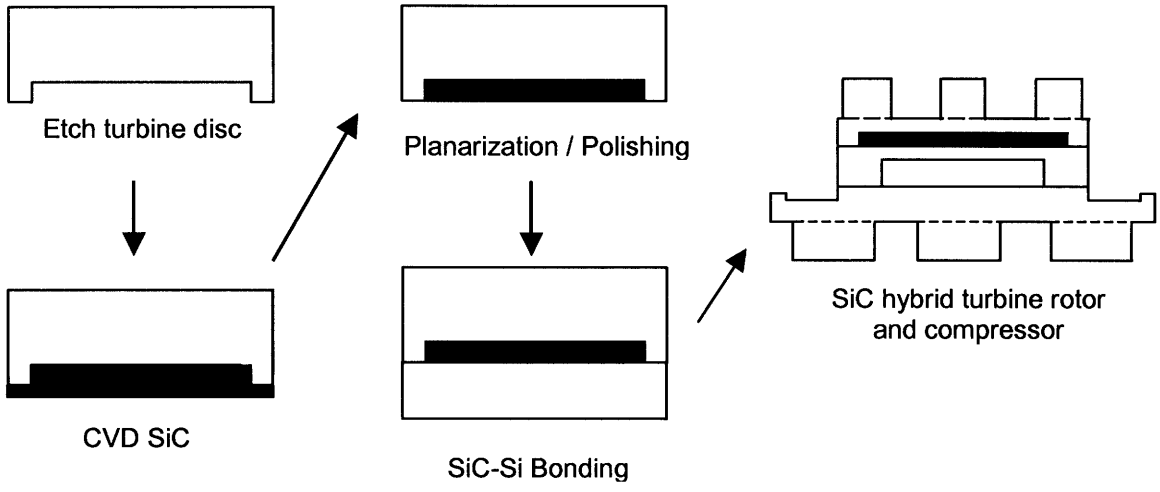


Figure 2-7 Key fabrication steps for the Si-SiC hybrid turbine structure.

2.3.2 Critical issues of each of the process steps

2.3.2.1 Chemical vapor deposition (CVD) of SiC on silicon substrates

The most critical issue in the CVD SiC deposition is residual stress control. Residual stress control is of critical importance to the entire Si-SiC hybrid turbine structure

fabrication steps, since a high level of residual stress can cause excess wafer bow, which is detrimental to the subsequent planarization and wafer bonding processes. Moreover, the microengine requires thick SiC coatings (up to several tens of μm), which result in sufficiently high residual stresses to cause wafer cracking even during the deposition process. Therefore, the control of residual stresses by properly changing CVD process variables is the first step towards the successful fabrication of the Si-SiC hybrid turbine structures. The development of residual stresses and their origins will be discussed in greater detail in Chapter 4 along with several research efforts made to achieve a low level of residual stress.

2.3.2.2 SiC planarization / polishing

Following SiC deposition, unnecessary SiC has to be removed by planarization and polishing processes prior to bonding. For successful wafer bonding, it is necessary to achieve a considerably high degree of surface smoothness and flatness after planarization. The surface finishing of SiC, however, is extremely challenging because of its high hardness and chemical stability. Due to the chemical inertness of SiC, chemical mechanical polishing (CMP) is not yet available to improve the surface smoothness of SiC to a level adequate for direct wafer bonding. Hence, the current planarization technique adopted in this research uses only mechanical polishing with diamond grits. In addition to the surface finish, wafer cracking is another serious problem encountered in SiC polishing process. Small cracks can be easily induced on the surface being polished due to the brittleness of SiC. Once initiated, the small cracks can propagate rapidly to the entire wafer areas during the polishing. The polishing procedure and associated difficulties will be further discussed in Chapter 5.

2.3.2.3 Si-SiC wafer bonding

As mentioned in the previous section, surface smoothness is the most critical factor towards achieving intimate contact between a pair of wafers, which is a measure of the success of wafer bonding. However, mechanical polishing using diamond grits unavoidably produces relatively rough hill-and-valley like structures on the SiC surface,

which are not able to the requirements for successful wafer bonding. To circumvent this problem, interlayer materials must be deposited on the rough surface of the polished SiC to fill the grooves introduced by the planarization / polishing processes. In this research, CVD silicon oxide has been studied for use as an interlayer material. A detailed discussion of the Si-to-SiC wafer bonding process will be given in Chapter 5.

2.4 References

1. H. Morkoc et al., "Large-band-gap SiC, III-V nitride, II-VI ZnSe-based semiconductor device technologies," J. Appl. Phys., Vol. 76, No. 3, p. 1363-1398, 1994.
2. W. S. Yoo, S. Nishino, and H. Matsunami, "Polytype Change of Silicon Carbide at High Temperatures," Springer Proceedings in Physics, Vol. 43, p. 35, 1989.
3. M. Mehregany et al., "Silicon carbide for microelectromechanical systems," International Materials Reviews, Vol. 45, No 3, p. 85-108, 2000.
4. R. F. Davis, "Silicon Carbide: The premier paradigm for structural and microelectronic device applications in severe environments," Mat. Res. Soc. Symp. Proc. Vol. 410, p. 365, 1996.
5. H. Sato and S. Shinozaki, "One-Dimensionally Disordered Structure and Polytypism in SiC," Mat. Res. Bull. Vol. 10, p. 257, 1975.
6. W. J. Moberlychan et al., "Microstructural Development to Toughen SiC," Mat. Res. Soc. Symp. Proc. Vol. 410, p. 257, 1996.
7. R. C. Marshall et al., "Silicon Carbide – 1973," Proceedings of the Third International Conference on Silicon Carbide, Miami Beach, Florida, p. 668-676, September 17-20, 1973.
8. M. Mehregany et al., "Silicon Carbide MEMS for Harsh Environments," Proceedings of the IEEE, Vol. 86, No. 8, p. 1594-1610, August 1998.
9. L. Zhou et al., "Chemomechanical Polishing of Silicon Carbide," J. Electrochem. Soc., Vol. 144, No. 6, p. L161-L163, June 1997.
10. J. S. Shor and R. M. Osgood, J. Electrochem. Soc., Vol. 140, No. 8, p. L123-125, August 1993.
11. Y. Hibi et al., "Excimer laser assisted chemical machining of SiC ceramic," Appl. Phys. Lett, Vol. 66 (7), p. 817-818, February 1995.
12. R. Okojie et al., "6H-SiC pressure sensors for high temperature applications," Proc. 9th Ann. Int. Workshop Microelectromechanical Systems, M. Allen and M. Reed, Eds., San Diego, CA, Feb. 11-15, p. 146-149, 1996.
13. J. Sugiura et al., "Reactive ion etching of SiC thin films using fluorinated gases," J. Vac. Sci. Technol. B, Vol. 4 (1), p. 349-354, 1986.
14. W. S. Pan and A. J. Steckl, "Reactive Ion etching of SiC thin films by mixtures of fluorinated gases and oxygen," J. Electrochem. Soc., Vol. 137, p. 212-220, 1990.
15. C. Richter et al., "Rapid plasma etching of cubic SiC using HF_3/O_2 gas mixtures," Mater. Sci. Eng., Vol. B46, p. 160-163, 1997.
16. P. Yih and A.J. Steckl, "Effects of hydrogen additive on obtaining residue-free reactive ion etching of β-SiC in fluorinated plasmas," J. Electrochem. Soc., Vol. 140, p. 1813-1824, 1993.
17. W. Reichert et al., "Fabrication of smooth β-SiC surfaces by reactive ion etching using a graphite electrode," Mater. Sci. Eng., Vol. B46, p. 190-194, 1997.
18. K. A. Lohner, "Microfabricated Refractory Ceramic Structures for Micro Turbomachinery," S. M. Thesis, Department of Aeronautics and Astronautics, MIT, Cambridge, MA, 1999.

19. B. Miller, "Hybrid Silicon/Silicon Carbide Microstructures and Silicon Bond Strength Tests for the MIT Microengine," S. M. Thesis, Department of Aeronautics and Astronautics, MIT, Cambridge, MA, 2000.
20. H.-S. Moon, "Design of Si/SiC Hybrid Structures for Elevated Temperature Micro-Turbomachinery," Ph. D. Thesis, Dept. of Mechanical Engineering, MIT, Cambridge, MA, 2002.
21. H.-S. Moon et al., "Materials, Structures, and Packaging," The MIT Microengine Project, 2000 Annual Report, MIT Property, Cambridge, MA, 2000.
22. H.-S. Moon et al., "Development of Si/SiC hybrid structures for elevated temperature micro-turbomachinery," submitted to J. MEMS, 2003.

CHAPTER 3

CHARACTERIZATION OF CVD SILICON CARBIDE ON SILICON WAFERS

Chemical vapor deposition of SiC on Si substrates is the first process step towards the fabrication of Si-SiC hybrid turbine structures. This first step deserves a great deal of research attention because of its critical importance to the entire Si-SiC hybrid structure fabrications. The Si-SiC hybrid structure requires the CVD SiC coatings to be structurally strong and intact as well as to be in low levels of residual stress that present no problem in the subsequent planarization and bonding processes. This chapter describes the CVD procedure and physical characterizations of the SiC deposited on Si wafers including microstructures and mechanical properties.

3.1 Chemical vapor deposition of SiC on Si

3.1.1 Fundamentals of CVD SiC

The preparation of CVD SiC requires sources of both Si and C. SiH_4, $SiCl_4$, and CH_4 are commonly used to produce SiC by a chemical reaction involving two source gases such as

$$SiCl_4 + CH_4 \leftrightarrow 4HCl + SiC$$

CVD SiC can also be produced by chemical reactions involving just a single source gas such as CH_3SiCl_3 (MTS) and CH_3Cl_2SiH (MDS), which contain both Si and C. An example of such reactions is the decomposition of CH_3SiCl_3, which is shown below [1].

$$CH_3SiCl_3 \leftrightarrow 3HCl + SiC$$

In general, a carrier gas such as H_2 is passed through $SiCl_4$, MDS, MTS, or some other Si-containing gas. In some cases, hydrogen chloride gas (HCl) is used as an additive to avoid the formation of either excess carbon or silicon making the SiC stoichiometric. The chemical reactions involved in CVD SiC using H_2 as a carrier gas can be generalized by the following reaction [2]:

$$nH_xSiCl_{4-x} + C_nH_m + \alpha H_2 \rightarrow nSiC + n(4-x)HCl + [\alpha + (m + nx) / 2 - n(4-x) / 2]H_2$$

where the silanes are either dichlorosilane or trichlorosilane, and the hydrocarbons are methane or propane. From a thermodynamic point of view, SiC deposition occurs when the amounts of Si and C in the gases are greater than the equilibrium amounts in the potential gases, where Si and C are believed to deposit separately, and then combine on the substrate surface.

The reaction chamber can be of either the cold wall or hot wall type. The main advantage of cold wall-type reactors is the ability to control the reaction such that the deposition does not occur on the chamber walls. This makes the CVD process more efficient [1]. However, in terms of the ability to deposit SiC simultaneously on many substrates, hot wall-type reactors are superior. In addition, hot wall reactors are better to eliminate contamination from the susceptor, when the CVD is performed under very low-pressure conditions [3].

3.1.2 Basic process conditions for the present study

Among the various chemical reactions used for CVD SiC, decompositions of single source gases are preferred, where the ability to maintain stoichiometric composition and control the residual stress in the SiC is of great interest. In this regard, methyltrichlorosilane (MTS or CH_3SiCl_3) has been used as a preferred SiC precursor in CVD processes because of its 1:1 atomic ratio of silicon to carbon. It has been reported by Chiu et al. that stoichiometric β-SiC thin films were successfully grown on Si (100) substrates from a mixture of MTS and H_2 in a hot wall low pressure chemical vapor deposition (LPCVD) quartz tube [3].

In the present research, all CVD SiC coatings were produced by Hyper-Therm, Inc., a research collaborator of the MIT microengine team. The basic CVD process for SiC has been well characterized, and thus, no significant process development was believed to be necessary to initiate SiC research if Hyper-Therm's existing knowledge of the CVD process for SiC was properly used. However, the microengine's critical demand for relatively thick (several tens of micrometers) SiC required intensive study of the correlations between CVD process parameters and residual stresses in the thick SiC coatings. At Hyper-Therm, SiC was produced by the thermal decomposition of vaporized MTS using H_2 as a carrier gas at elevated temperatures and reduced pressures according to the following chemical reaction:

$$CH_3SiCl_3 + \alpha H_2 \rightarrow SiC + 3HCl + \alpha H_2$$

where α is the molar ratio of hydrogen to MTS. MTS was chosen to take advantage of its 1:1 atomic ratio of silicon to carbon and simple chemistry by which the parametric studies can be performed in a more systematic and easier manner. This process using a mixture of MTS and H_2 is similar to that used by Chiu et al., and so is the CVD chamber, which is a traditional LPCVD reactor [3].

The CVD SiC was deposited on 100 mm diameter Si (100) wafers, which were typically 525 μm thick. The CVD was performed in a vertical cross-flow reactor, in which the Si wafers were placed with uniform spacing such that the target surfaces were

perpendicular to the gas stream, as shown schematically in Figure 3-1 [4]. Deposition was performed at various temperatures between 950 and 1300 °C at sub-atmospheric pressures [5].

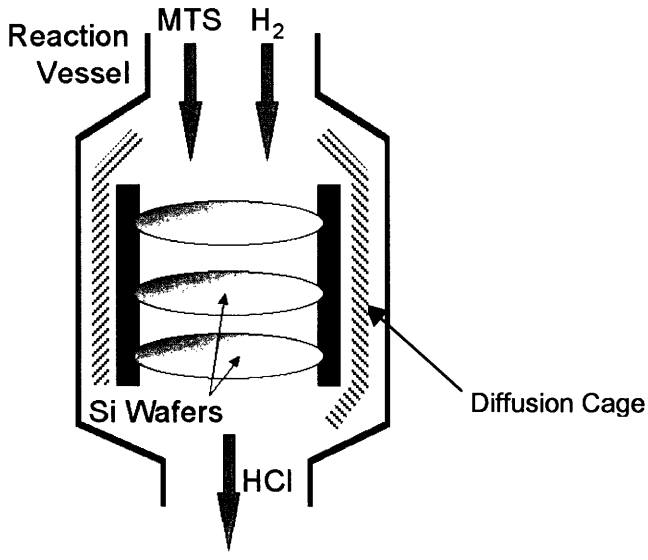


Figure 3-1 CVD reactor used for SiC [K. A. Lohner, S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, 1999].

As many as thirty Si wafers can be evenly placed in the reaction chamber with uniform spacing, but processing this many number of wafers simultaneously is not desirable because of significant variations in the resulting SiC thickness [See Appendix A]. Therefore, typically eight to twelve wafers were processed in a batch to minimize the thickness variation of SiC coating across the diameter of a wafer as well as to enhance the deposition uniformity between wafers in the same batch.

3.2 Physical characterizations of CVD SiC on Si wafers

Lohner previously performed initial characterization of Hyper-Therm's CVD SiC [4]. However, it was necessary for more characterizations to be conducted on recently

produced CVD SiC as the knowledge and experience of the CVD process for microengine applications advance. This section describes the characterization of the CVD SiC from recent batches.

3.2.1 Surface of CVD SiC

CVD SiC coatings of various thicknesses ranging from 4 to 120 μm have been deposited on Si wafers by Hyper-Therm, and the top surfaces of all the CVD SiC deposits appear as very smooth mirror-like planes to the naked eye. However, atomic force microscopy (AFM) performed over a 50 × 50 μm area to observe the micro-scale morphologies of the SiC surfaces revealed that thicker SiC coatings always resulted in rougher surfaces than thinner ones when they were produced under an identical set of process conditions. An AFM image of an 85 μm thick SiC coating is shown in Figure 3-2, where the mean surface roughness (R_a) and the maximum range of roughness or height (R_{max}) are 33 nm and 360 nm (only 0.4 % of the coating thickness), respectively. Thinner SiC coatings had much smoother surfaces with a 10 - 20 nm range of R_a values.

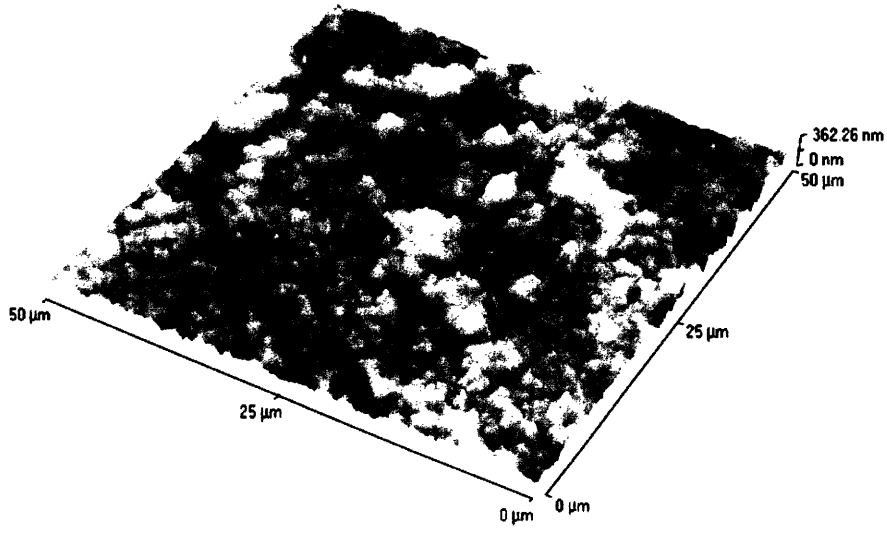


Figure 3-2 AFM image of the surface of an 85 μm thick SiC coating, which shows a mean surface roughness of 33 nm [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

A scanning electron microscope (SEM) image of the top surface of a 35 μm thick CVD SiC deposit is shown in Figure 3-3, in which SiC grains appear as hills and valleys of several tens of nanometers.

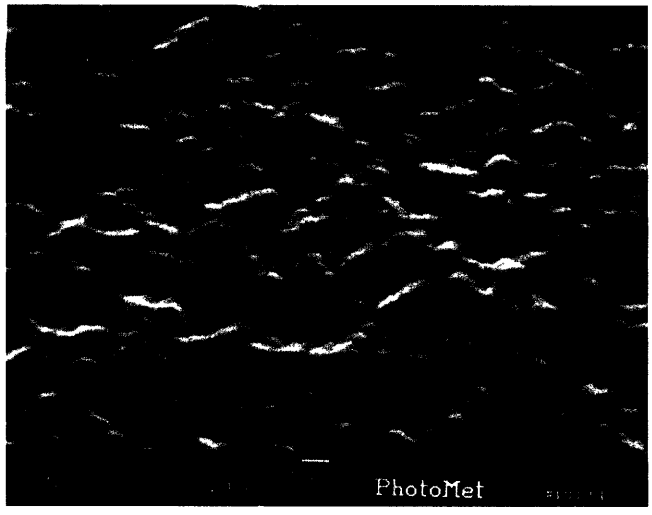
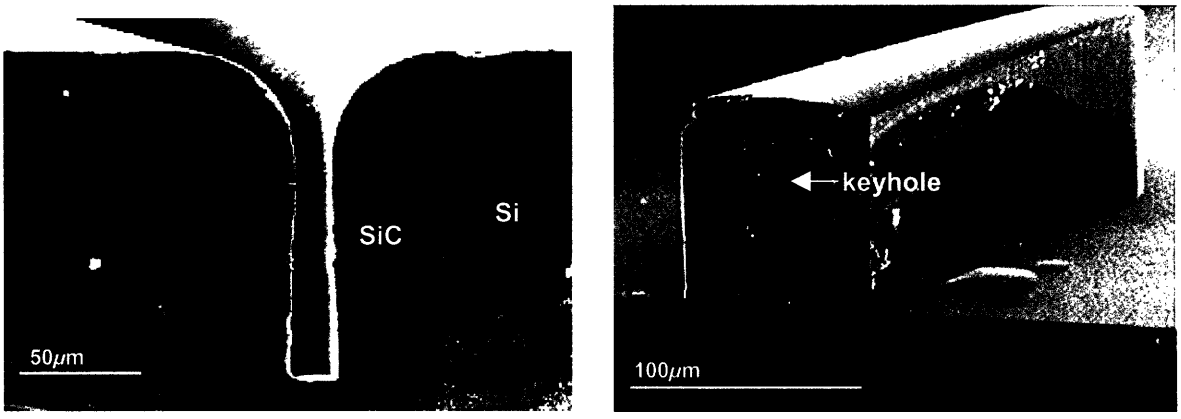


Figure 3-3 SEM image of a 35 μm thick SiC coating [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

3.2.2 Wafer coverage and conformality

It is important that etched or molded features on the silicon wafers be uniformly coated with CVD SiC to achieve maximum benefit from the Si-SiC hybrid turbine structures. A perfect conformal CVD process will uniformly deposit SiC on all surfaces of the etched features. Lohner previously examined the conformality of the CVD SiC deposited on vertical trenches. Figure 3-4 (a) shows SiC coated on the wall of a 100 μm wide by 150 μm deep trench. The SiC on the sidewall is thicker than that on the top surface, and this becomes more pronounced as the aspect ratio or the ratio of depth to width increases. Narrow trenches of high aspect ratios can result in pores with 'keyhole' shapes, which are wider at the bottom and narrower at the top of the trenches, as shown in Figure 3-4 (b).



(a) (b)

Figure 3-4 (a) CVD SiC filling a 100 μm wide by 150 μm deep trench 100. (b) Imperfect conformality of CVD SiC showing a keyhole-like pore along the centerline of the width of a trench [K. A. Lohner, S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, 1999].

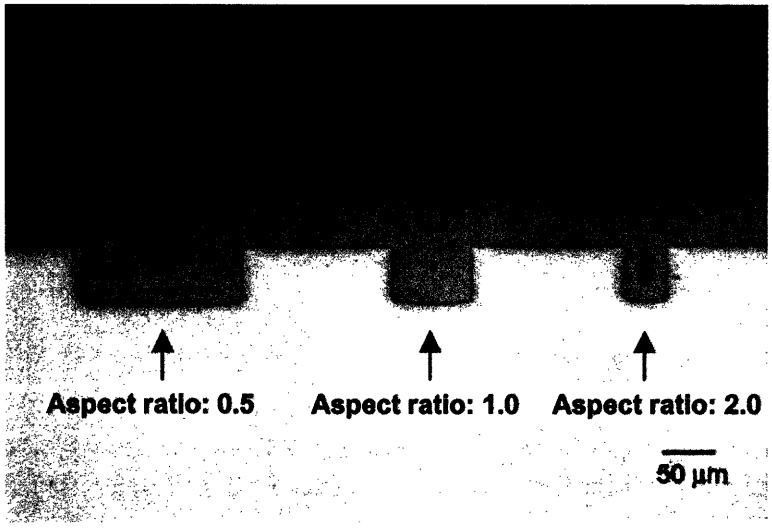
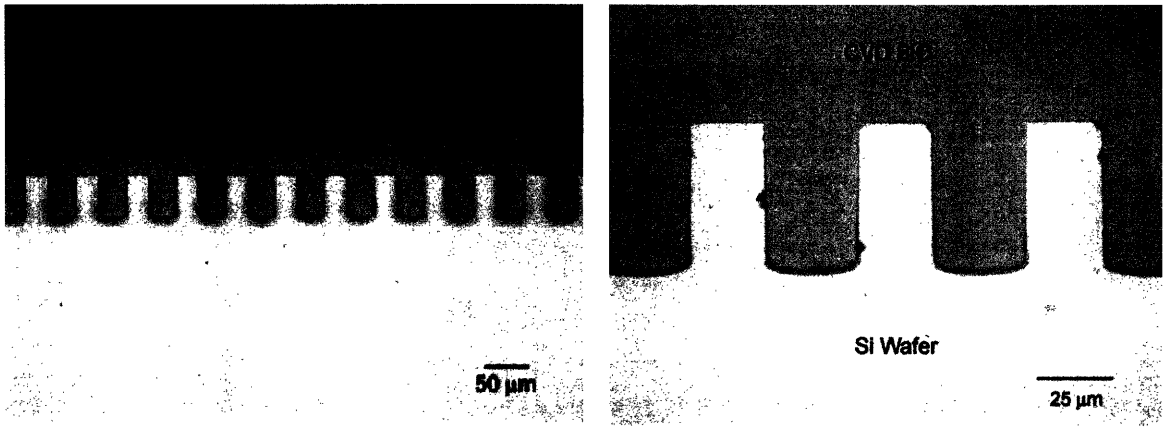


Figure 3-5 CVD SiC filling trenches of various aspect ratios [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

Further conformality studies were conducted on the CVD SiC from recent batches. The conformality was examined by depositing CVD SiC in 50 μm deep trenches of various widths and spacings as shown in Figure 3-5. In widely spaced negative features on a silicon mold, the CVD SiC was observed to perfectly fill a trench with an aspect ratio (depth to width) of 0.5, and nearly completely a trench with an aspect ratio of 1.0, while leaving a big keyhole behind in a trench with an aspect ratio of 2.0.

The cause of the imperfect conformality is not clear, but is believed to be due to an enhanced deposition rate in the entrance regions around the sharp corners of the trenches. However, even in the trenches of aspect ratio 2.0, perfect conformality of the CVD SiC was observed when the trenches were evenly placed one width (25 μm) apart, as shown in Figure 3-6.



(a) (b)

Figure 3-6 (a) CVD SiC perfectly fills trenches of an aspect ratio of 2.0 (25 μm wide by 50 μm deep trenches) when they are evenly placed 25 μm apart. (b) Image of higher magnification.

The etched trenches in Figure 3-6 can be considered as either a closely spaced array of negative or positive mold features, which turned out to be effective in reducing the higher deposition rate in the regions around the sharp corners of the features. The enhanced

deposition of SiC around the sharp corners is greatly pronounced when negative mold features of aspect ratios smaller than 1.0 are closely spaced, as shown in Figure 3.7. Significant rounding of the deposited SiC is observed around the sharp corners of closely spaced negative mold features, some of which already have voids (keyholes).

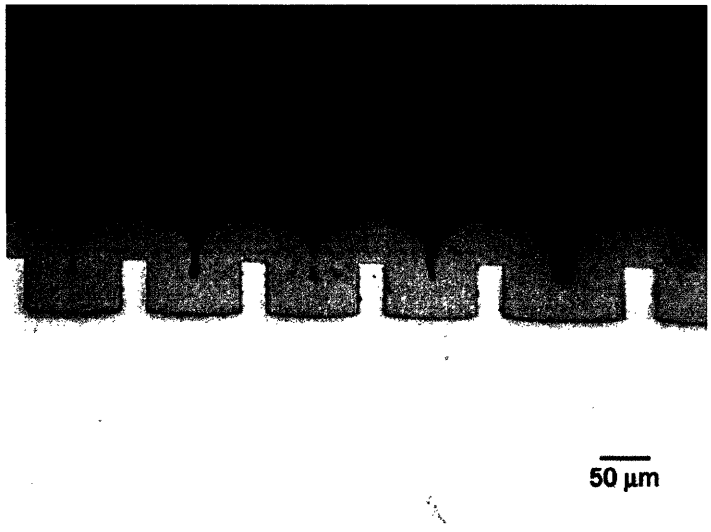


Figure 3-7 Rounding of CVD SiC around the sharp corners of closely spaced negative mold features [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

More study is necessary before it is possible to understand the abnormal gas flow or flow disruption, which is thought to be responsible for the higher deposition rate at the sharp corners. However, the current knowledge regarding the conformality of CVD SiC is believed to be sufficient for the fabrication of the Si-SiC hybrid turbine structures since the aspect ratio of the reinforcement trenches for the hybrid structure is much greater than 2.0, and also because they are spaced very far apart on a Si wafer.

3.2.3 Thickness uniformity of SiC coatings

Depositing SiC of uniform thickness over the entire surface area of a silicon wafer is of great importance to the planarization process, which was identified as one of the most difficult technical barriers in fabricating Si-SiC hybrid turbine structures. Details of

problems encountered during the planarization of Si wafers coated with SiC are discussed in Chapter 5.

Lohner previously obtained the thickness profiles of CVD SiC coatings from initial batches of various target thicknesses by examining their cross-sections along the wafer diameter under a scanning electron microscope (SEM). As shown in Figure 3-8, the coating thicknesses were most uniform across the central 60 mm of the wafers, but significantly thicker SiC coatings are found near the outer edges of the wafers [4].

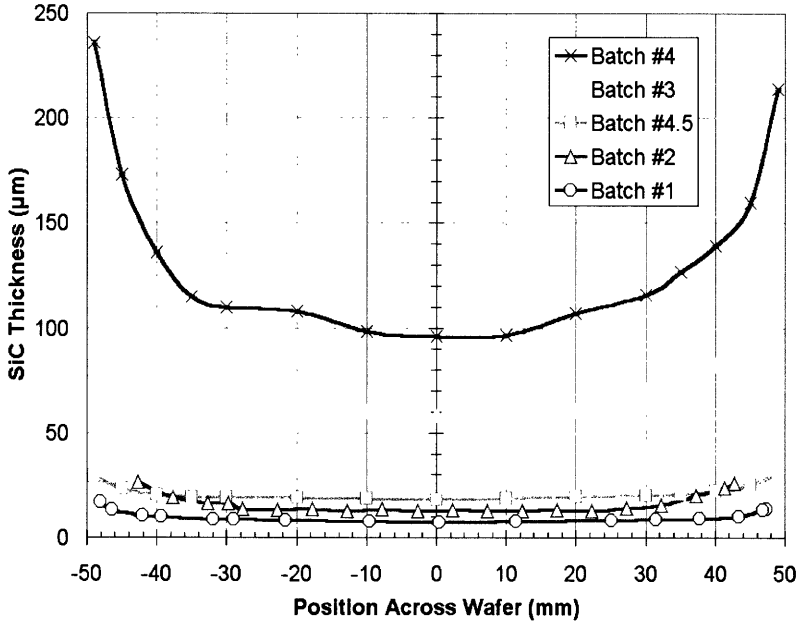


Figure 3-8 Thickness profiles of CVD SiC from various batches of different target thicknesses [K. A. Lohner, S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, 1999].

The radial profiles of three CVD SiC coatings from more recent batches of target thicknesses ranging from 20 to 45 µm were also obtained by Hyper-Therm using optical microscopy to avoid wafer destruction. Again, a significant increase in thickness was observed near the outer edges of the wafers, as shown in Figure 3-9 (a). All specimens

showed similar U-shapes, which were very consistent with one another when normalized by their target thicknesses as shown in Figure 3-9 (b).

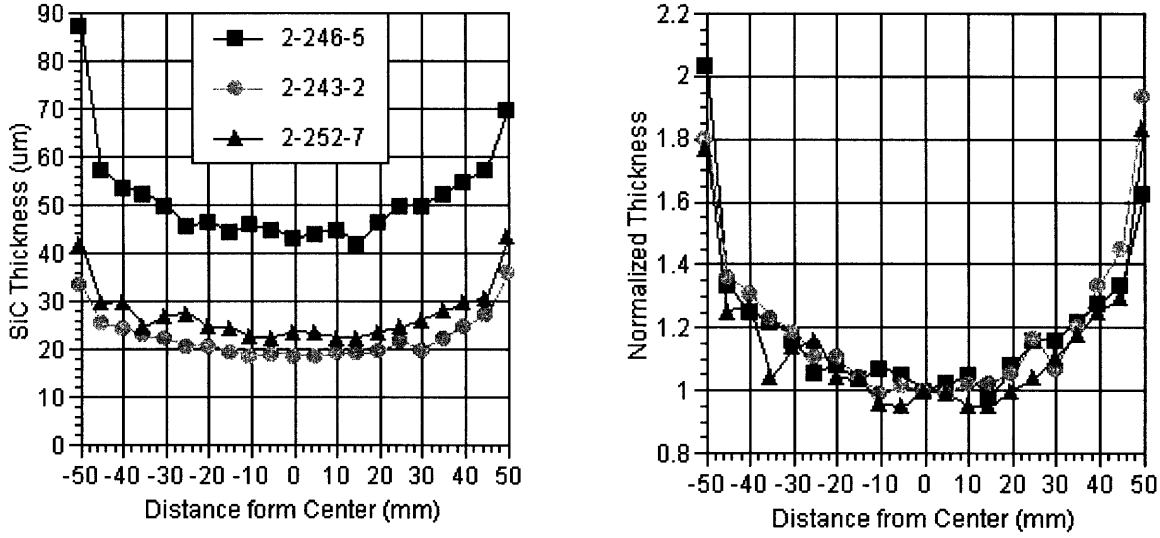


Figure 3-9 (a) Radial profiles of three CVD SiC coatings of different target thicknesses. (b) Normalized radial profiles of the three SiC coatings [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

The SiC coatings deposited on the outer edges of the wafers were nearly twice as thick as those deposited in the central areas. These undesirable U-shape profiles are due to the kinetics involved in the CVD process, in which competitions exist between the chemical reactions of source gases and diffusion processes proceeding from outer edges to central areas of the wafers. A simple model describing the kinetic process involving the two competing processes can be found in Appendix A, which also briefly discusses the effect of wafer configurations (e.g., gap between neighboring two wafers) in the CVD chamber on the uniformity of coating thickness.

Hyper-Therm has recently demonstrated that the radial gradient of SiC coatings on Si wafers can be significantly reduced by using modified wafer fixtures with rims that are designed to be in close proximity to the outer edges of the wafers and which retard the

SiC deposition near the edges. This approach is desirable since the fixture modification does not alter the residual stress states of the SiC coatings, while being effective in reducing the maximum thickness variation to 20 % near the perimeters of the wafers. The comparison between the improved process (red dots) using the modified fixtures and the original process without modification is depicted in Figure 3-10.

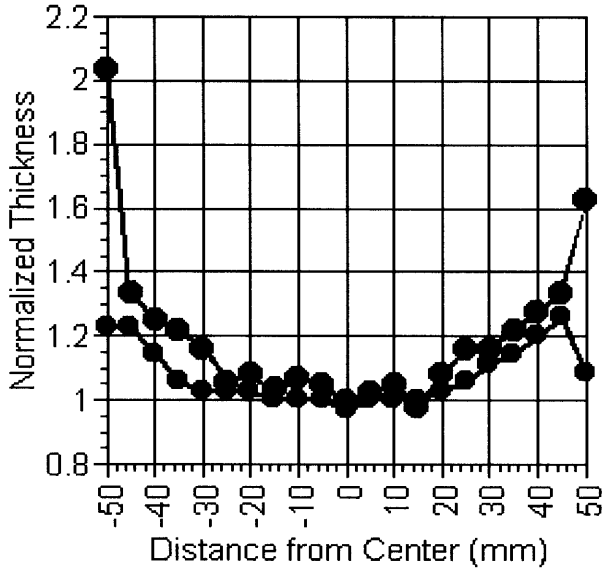


Figure 3-10 Reduced radial profile (red dots) of the CVD SiC produced using the modified wafer fixtures [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

3.2.4 Microstructures

X-ray diffraction (XRD) analyses revealed that the CVD SiC produced by Hyper-Therm was polycrystalline, face-centered cubic (3C), β-SiC with a strong preferential growth orientation of (111) planes, as shown in Figure 3-11. Although the texture of CVD SiC is strongly dependent on deposition conditions, generally (200), (220), and (311) peaks were detected along with the dominant (111) peak. The two-dimensional peak (10) at 2θ of 35.6 ° in Figure 3-11 could only be detected when high-resolution diffraction was employed. The XRD data also showed that the crystallite size of the CVD SiC ranged from 50 to 70 nm. An XRD analysis performed by Johns Hopkins

University showed that Hyper-Therm's CVD SiC had a random in-plane texture with additional orientations of (100), (110), and (311) planes [6].

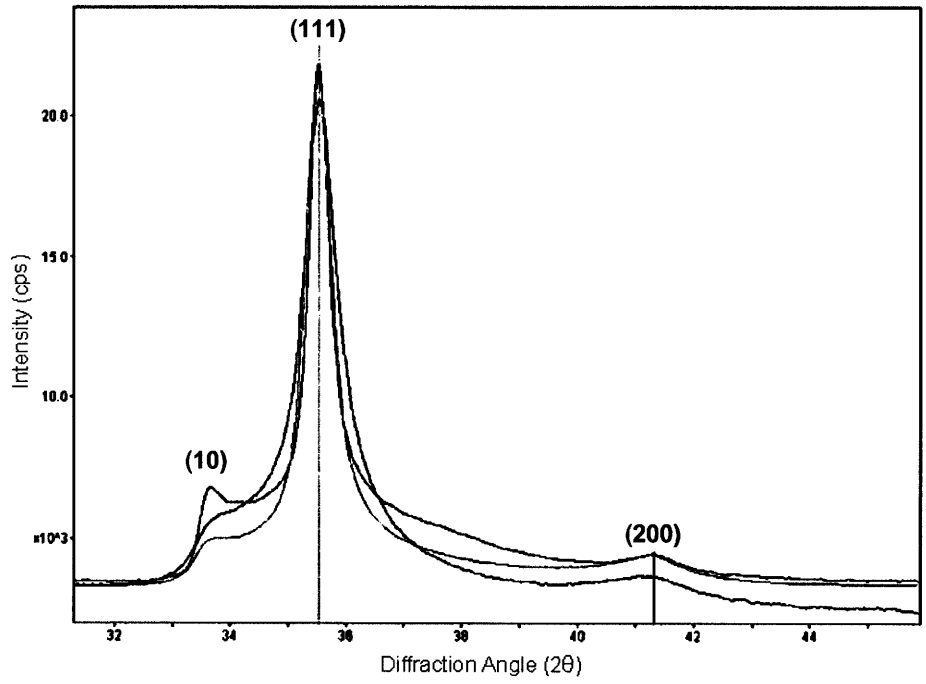


Figure 3-11 XRD analyses of three SiC coatings produced under different CVD conditions show different diffraction patterns. However, all three patterns show a strong preferred orientation of (111) planes at 35.6 ° 2θ [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

Transmission electron microscopy (TEM) was also performed to further characterize the microstructure of CVD SiC. A TEM image in Figure 3-12 shows that the strong preferred orientation develops in the very early stage of film growth. Figure 3-13 (a) shows a higher magnification TEM image from which the grain size is inferred to be about 100 - 150 nm wide. Figure 3-13 (b) is a TEM image taken by Johns Hopkins University, which also shows grains of approximately the same size. Based on the XRD and TEM studies, the fully-grown grain size is believed to be in the rage of 50 - 150 nm. Both the TEM images in Figure 3-13, show that the CVD SiC contains a relatively high density of stacking faults or twins. The abundance of such structural defects has commonly been observed in CVD SiC, as the stacking fault energy in SiC is very small, and the (formation) energies of many SiC polytypes are quite similar [7]. For instance,

the layers of α-SiC can be formed by a simple rotation of the stacking arrangement of β-SiC, and thus, they are considered to be metastable states of β-SiC.

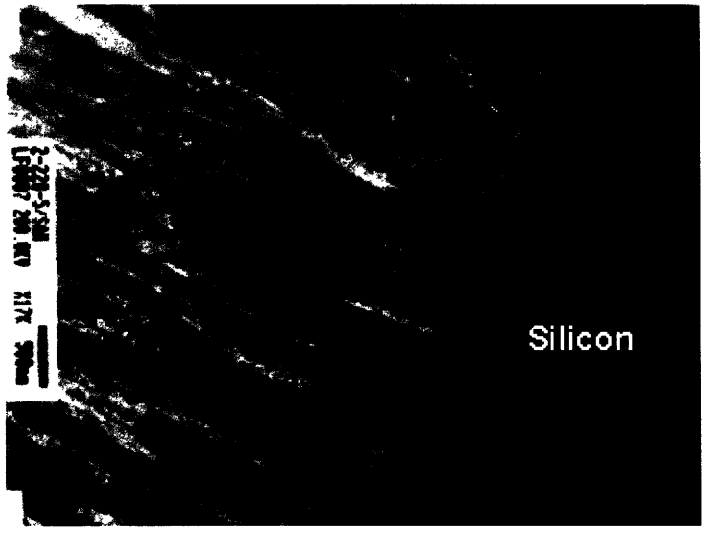
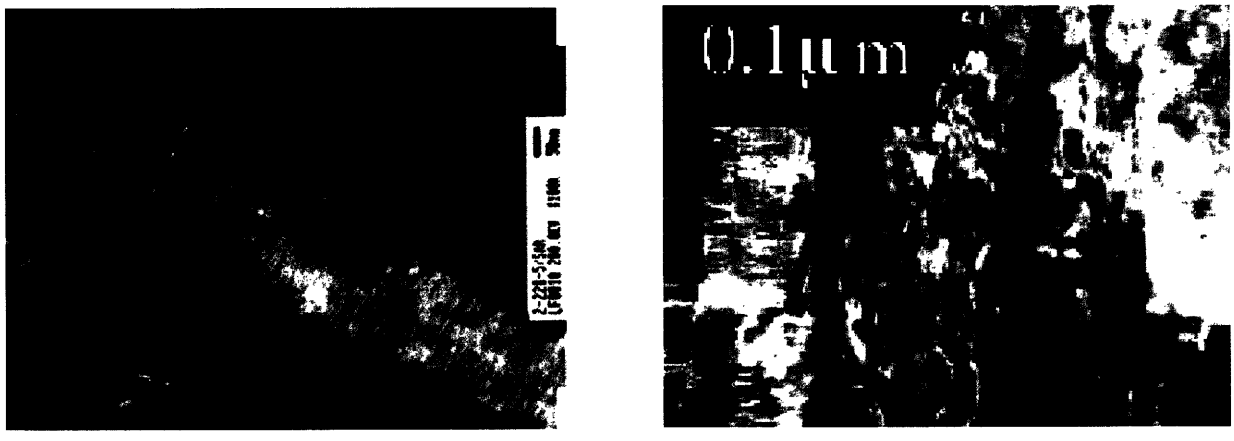


Figure 3-12 TEM image showing the strong preferential growth orientation of CVD SiC on (100) silicon wafers [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].



(a) (b)

Figure 3-13 (a) TEM image showing the acicular grains and stacking faults [Hyper-Therm, Inc.]. (b) TEM image showing a perpendicular image of columnar grains with twinning [K. M. Jackson et al., Mat. Res. Soc. Symp. Proc., Vol. 687, B6.3, Fall 2001].

3.3 Mechanical properties of CVD SiC

MEMS research has raised many materials issues largely due to the lack of knowledge about the mechanical properties of the (relatively) thin film materials being fabricated. The microstructures of materials are strongly dependent on the process conditions adopted to fabricate the MEMS devices. Therefore, in many cases, the mechanical properties of thin film materials are expected to be different from their bulk counterparts. This dictates the need for newly measuring the mechanical properties of thin film materials to be used as structural components, which is one of the difficulties encountered when designing or developing new MEMS processes.

3.3.1 Bulk properties of SiC

The bulk properties of SiC have been measured by several researchers, although with considerable variation in the values measured [8, 9, 10]. However, the bulk values for mechanical properties such as strength, elastic modulus, and Poisson's ratio cannot simply be accepted as those for the CVD β-SiC to be incorporated into the microengine structure for the following major reasons [11].

- To compare crystallographic orientation-dependent mechanical properties such as elastic modulus and Poisson's ratio, it is necessary to have information regarding the materials' crystal structures. In many cases, bulk SiC is made by sintering or hot pressing, and thus, is usually composed of randomly oriented grains, while the (relatively) thin CVD SiC tend to have grains with preferred orientation. As described in section 3.2.4, Hyper-Therm's CVD β-SiC is of columnar microstructure showing a very strong preference for (111) direction.

- The fabrication or processing route significantly affects the strength of SiC, which is largely determined by the microstructural parameters such as grain size as well as the distribution and density of flaws and structural defects.

- In general, ceramics display much higher strengths in compression than in tension. Many of the reported strength values for bulk SiC were obtained from compression tests. Therefore, they cannot be taken as proper values for designs requiring tensile loading.

- The strength of brittle ceramics is a function of lengthscale. Generally, small specimens exhibit higher strength than lager (bulk) ones due to the reduced population of structural defects or flaws [12, 15].

Despite the problems mentioned above, the bulk values would still be useful as approximate reference values and for comparison purposes. Some bulk properties of SiC are summarized in Table 3-1.

Table 3-1 Bulk properties of SiC

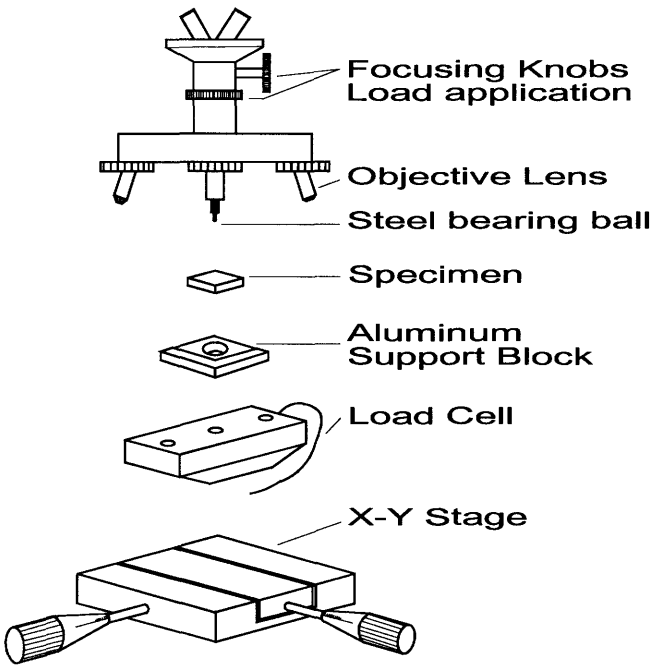
Bulk properties of silicon carbide	Values
Elastic modulus	E = 470 [GPa]
Poisson's ratio	$\nu = 0.21$
Tensile strength[1]	0.160 – 0.505 [GPa]
Compressive strength[1]	4.6 [GPa]
Density	3.20 [g/cm^3]

1. The data were summarized by Jackson [11]. Low tensile strength values were typically reported for SiC produced by hot pressing or sintering, which contained some amounts of porosity.

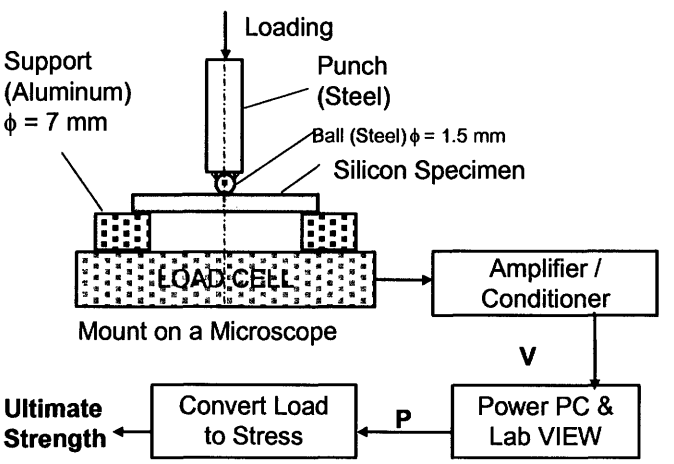
3.3.2 Mechanical properties of CVD SiC films

3.3.2.1 Biaxial flexural strength tests by Hyper-Therm

Chen previously tested the mechanical strength of single crystal Si under biaxial stress on 1 cm square dies, and Lohner extended the biaxial flexural tests to 1 cm square Si dies coated with 250 μm thick CVD β-SiC [13, 4].



(a)



(b)

Figure 3-14 (a) Schematic of biaxial flexural strength test fixture. (b) Procedure of the biaxial strength test [K.-S. Chen, Ph. D. Thesis, Dept. of Mechanical Engineering, MIT, Cambridge, MA, 1999].

To apply forces with a 1/64" steel ball, the specimen dies were placed on a biaxial fixture equipped with a load cell, which coverts fracture forces to failure stresses. The test setup is schematically shown in Figure 3-14. High temperature strength could also be tested using a four-point bending apparatus, which is discussed in Chapter 6.

Hyper-Therm used a similar test method to measure the biaxial flexural strength of CVD SiC. Plain and SiC coated silicon wafers were tested at both room and elevated temperatures. Although a significant variation or dependence of the biaxial strength of SiC coatings on the CVD conditions, the only consistently observed trend was that SiC coatings under high residual tensile stresses resulted in much lower strengths than those under compressive stresses and low net residual stresses. Samples with both compressive stresses and low residual stresses resulted in similarly higher strengths. The thickness of SiC coatings ranged from 25 to 43 μm, and all of them were deposited on 525 μm thick standard 4-inch silicon wafers. The test results are summarized in Figure 3-15.

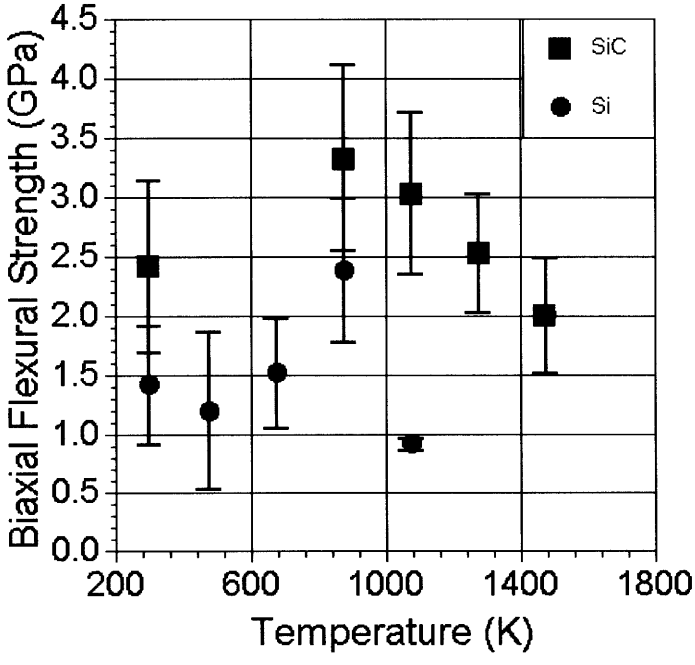


Figure 3-15 Results of biaxial flexural strength tests of CVD SiC and Si at room and elevated temperatures [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

SiC always showed much higher strength than silicon at all temperatures. The biaxial flexural strength of the CVD SiC was measured to be 2.41 ± 0.73 GPa and 3.33 ± 0.78 GPa at room temperature and 600 °C, respectively. The silicon was observed to (partially) yield at temperatures above 600 °C, and no abrupt cracking or catastrophic failure occurred even though its ability to carry loads was marginal. Since the abrupt failure of the underlying silicon can be eliminated in high temperature tests, the 3.33 GPa measured at 600 °C is believed to be a more plausible value representing the real strength of the SiC samples over the temperature range of tests. One point to be noted here is that the biaxial strength test does not measure yield strength of materials, but provides the ultimate strength. Thus, the slight increase in strength of silicon with increasing temperature is due probably to the prevention or delay of rapid crack propagation by plastic deformation of silicon in high temperature ranges. The biaxial strength of SiC was observed to decrease down to 2.0 GPa at 1200 °C with increasing temperature above 600 °C. Considering the polycrystalline nature of the CVD SiC with small grain sizes, the initiation of creep mechanisms by diffusion at these high temperatures (above $0.3T_m$) could be a possible explanation for the decrease in strength with temperature [14]. The effect of oxidation on the strength degradation was also tested with SiC samples heated at 1000 °C in the air for 5, 20, and 80 hours. The biaxial flexural strengths of the heat-treated samples were measured at room temperatures. Their mean strengths were 2.60 ± 0.98, 2.58 ± 0.47, and 2.46 ± 0.48 GPa, respectively. Compared with the mean strength of untreated samples (2.41 GPa), no strength degradation due to the oxidized SiC surface is likely to occur during the prolonged operation. In conclusion, the strength of CVD SiC (when converted to tensile strength) was measured to be higher than the preliminary design strength of 600 MPa in the range of temperature of interest [13].

Weibull analyses were performed to examine the data composed of about 150 individual biaxial strength tests in a statistical way. Figure 3-16 (a) shows a cumulative probability of failure of the CVD SiC at room temperature, where the maximum biaxial

flexural strength was nearly 4 GPa. The data set in Figure 3-16 (a) was replotted in Figure 3-16 (b) using Weibull's two-parameter distribution model, which is defined as

$$P_s = 1 - P_f = \exp\left[-\left(\frac{\sigma}{\sigma_0}\right)^m\right]$$

where P_s is the survival probability, P_f is the failure probability, σ is the failure strength, and σ_0 is the reference stress when P_s is equal to 37 %. The constant m is the Weibull modulus, which indicates how rapidly the strength falls as the stress approaches σ_0. The greater variability of strength is expected for the lower Weibull modulus m [15].

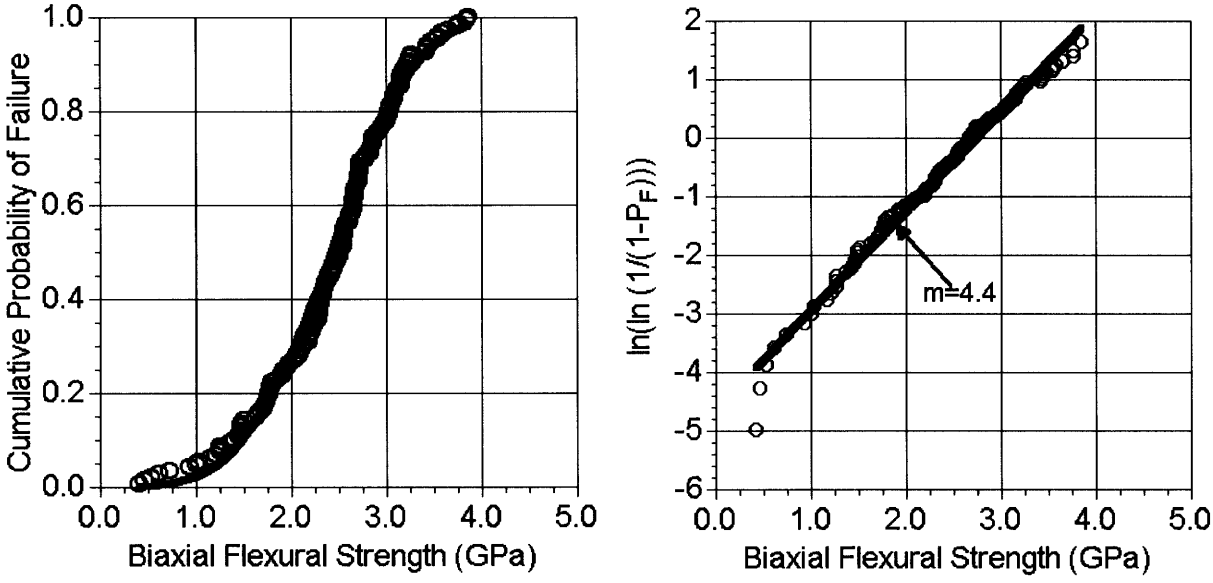


Figure 3-16 (a) Cumulative probability of failure of CVD SiC at room temperature. (b) Weibull plot of the biaxial flexural strength tests at room temperature [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

The Weibull modulus m was found to be 4.4 in Figure 3-16 (b), where the linearity of the data indicates the existence of a single dominant failure mode; it is believed to be the fracture caused by the surface flaws or defects of the CVD SiC. Weibull analyses were also performed on the SiC samples tested at 600 °C and 800 °C, as shown in Figure 3-17.

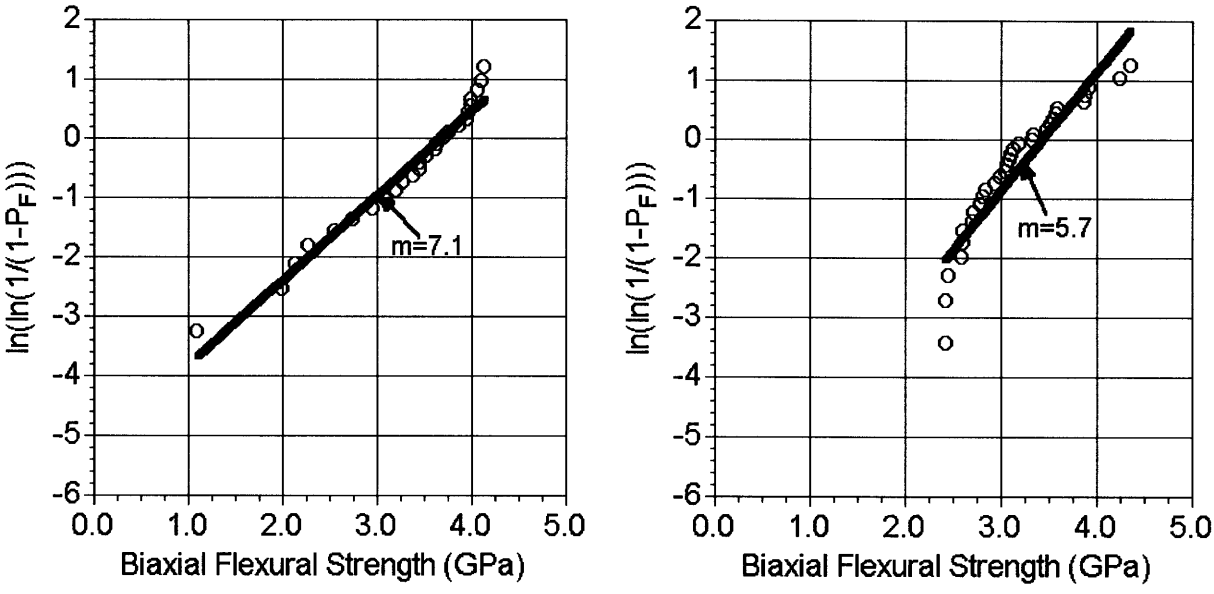


Figure 3-17 (a) Weibull plot of the biaxial flexural strength tests at 600 °C. (b) Weibull plot of the biaxial flexural strength tests at 800 °C [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

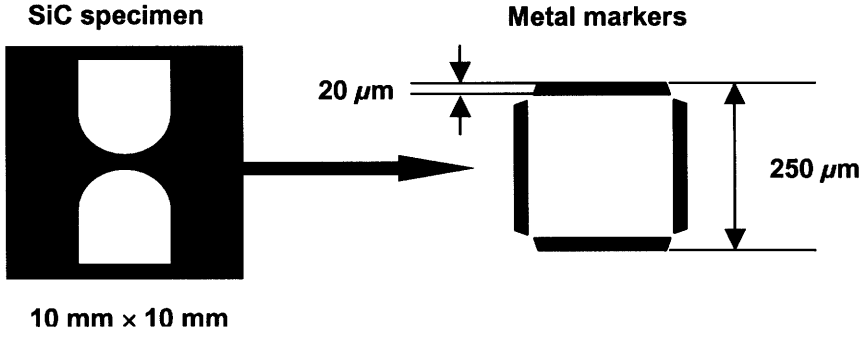
The SiC samples tested at elevated temperatures were found to have higher Weibull moduli, 7.1 and 5.7 for 600 °C and 800 °C, respectively. The biaxial flexural strength tests have revealed that the CVD SiC is capable of maintaining sufficient strength as a reinforcement material for the microengine structures at elevated temperature up to 1200 °C, which is about 85 % of the melting temperature of silicon.

3.3.2.2 Tensile tests using ISDG technique by Johns Hopkins University

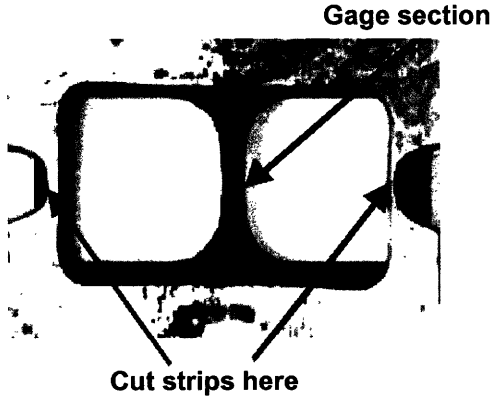
CVD SiC films deposited on Si molds were supplied to Johns Hopkins University to measure the elastic modulus, Poisson's ratio, and tensile strength of Hyper-Therm's CVD β-SiC. The researchers at Johns Hopkins University led by Sharpe, used an optical method called interferometric strain displacement gage (ISDG), which has been found to be particularly useful for measuring the strain of small specimens at the microscale level [16]. The ISDG uses the interference of a beam of light, which is well known from Young's double-slit experiment; if a coherent beam of light is incident upon two closely spaced slits of size similar to the wavelength of the light, interference fringes appear on a

screen perpendicular to the direction of the light beam. Therefore, the ISDG technique can be used only when reflective (metal) markers can be placed on the specimens.

The fabrication of specimens was performed at four different facilities. First, the author made the mask for specimens, and then patterned 20 - 40 μm deep molds on Si wafers using deep reactive ion etching (DRIE) at the Microsystems Technology Laboratory (MTL) at MIT. Secondly, CVD SiC was deposited on the Si molds by Hyper-Therm, and the wafers with SiC coatings were sent to Johns Hopkins Applied Physics Laboratory (APL) for dicing with a diamond saw.



(a)



(b)

Figure 3-18 (a) Schematics of the biaxial specimen and the metal markers. (b) Finished SiC tensile specimen [K. M. Jackson et al., Mat. Res. Soc. Symp. Proc., Vol. 687, B6.3, Fall 2001].

Third, Johns Hopkins University (JHU) polished excessive SiC from the top of the Si molds and from the back of the specimens. Fourth, two sets of metal markers were deposited on the individual specimen dies using lift-off masks at APL. The top layer of the markers was 5000 Å thick gold, but two other metals had been deposited as adhesion layers before the gold deposition. A 300 Å layer of titanium was first deposited on SiC surfaces followed by a 600 Å layer of platinum on the titanium. Fifth, bulk silicon etching was performed using xenon difluoride (XeF_2) while the front sides were fully covered with photoresist for protection. Finally, the photoresist was removed to obtain the final SiC specimens with an average thickness of 30 μm [11]. Figure 3-18 (a) shows the specimens having the dimensions of a 1 cm square, and the schematic of the placement and dimensions of the four metal lines for strain measurements. A finished SiC specimen is also shown in Figure 3-18 (b).

After fabrication, the specimens were attached to grips with epoxy adhesives, and then pulled with a piezoelectric actuator, while laser light was incident upon the gage sections of the specimens. The tensile forces were recorded with a load cell, while the corresponding strains were measured and calculated by following the movement of the fringes during loading. The two sets of metal markers, which were placed perpendicular to each other, allowed Poisson's ratio to be calculated along with the tensile strength and elastic modulus. Figures 3-19 and 3-20 briefly illustrate the principle of the ISDG technique and the schematic for the experimental setup, respectively.

A typical result of the tensile tests is shown in Figure 3-21, where both the axial and lateral strains were measured. Elastic modulus, Poisson's ratio, and fracture strength can be calculated from the curve.

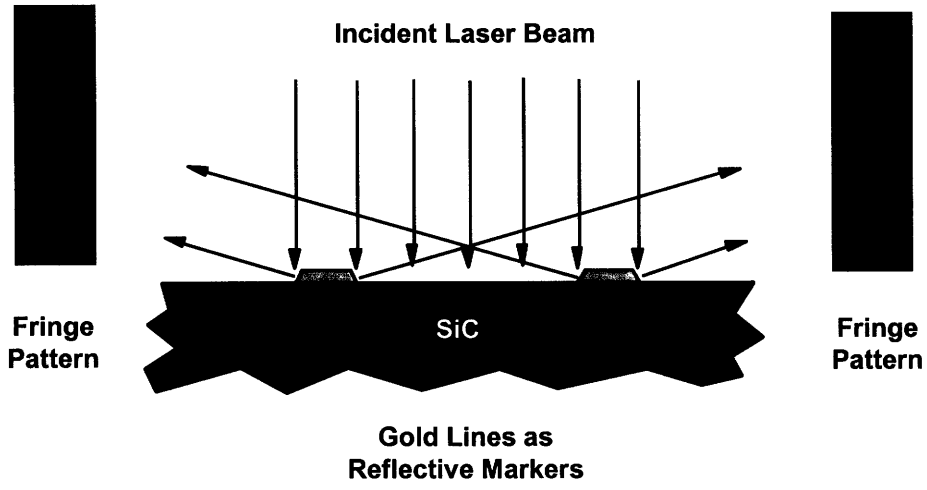


Figure 3-19 Schematics showing the basic principle of ISDG technique [W. N. Sharpe et al., Mat. Res. Soc. Symp. Proc. Vol. 444, 1997].

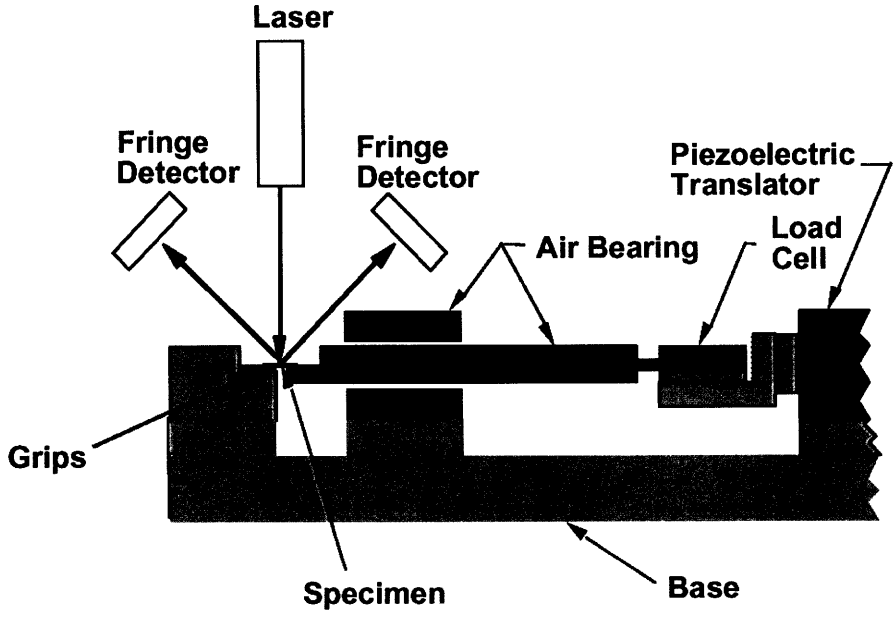


Figure 3-20 Schematics of tensile testing equipment [K. M. Jackson et al., Mat. Res. Soc. Symp. Proc., Vol. 687, B6.3, Fall 2001].

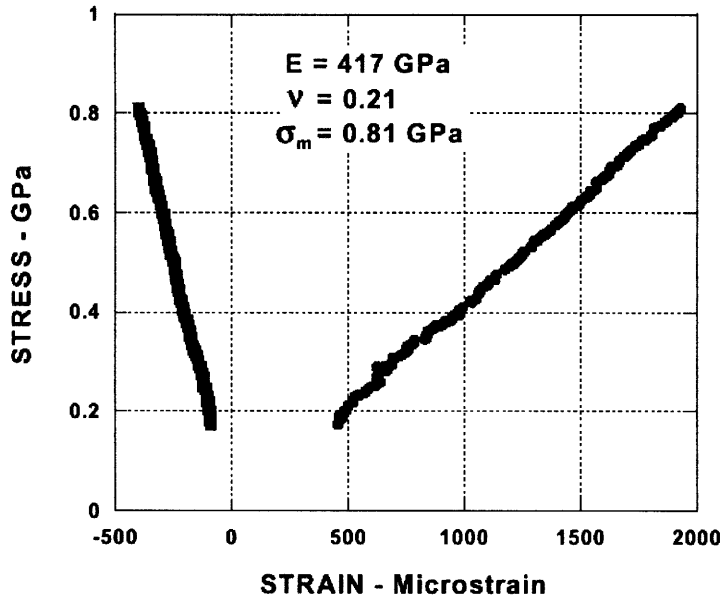


Figure 3-21 Tensile test curve showing both the axial and lateral strains [K. M. Jackson, Ph.D. thesis, Dept. of Mechanical Engineering, Johns Hopkins University, Baltimore, MD, 2002].

Results for the elastic modulus, fracture strength, and Poisson's ratio of the Hyper-Therm's CVD SiC are summarized in Table 3-2 [6].

Table 3-2 Mechanical properties of Hyper-Therm's CVD β-SiC measured using ISDG technique [6].

Mechanical properties of CVD SiC	Values*
Elastic modulus	E = 430 ± 40 [GPa] (4)
Poisson's ratio	ν = 0.24 (2)
Fracture strength	0.49 ± 0.2 [GPa] (11)

* The numbers in parentheses are the number of tests considered in each average value.

The average thickness of the SiC specimens was 30 μm. It should also be noted that the SiC was composed of mostly <111> oriented grains and small amounts of <110>, <100>, and <311> oriented grains. Therefore, the elastic modulus in Table 3-2 is an averaged value. A more accurate calculation of elastic modulus and Poisson's ratio might be possible if the volume fractions of the grains of different orientations were known. The success of measuring the elastic modulus and Poisson's ratio was strongly dependent on the yield of specimens and the quality of the deposited metal markers.

Jackson performed a Weibull statistical analysis for the fracture strength data. From the log plot of probability of failure and fracture strength m shown in Figure 3-22, the Weibull modulus and the normalized strength σ_0 were found as 2.3 and 0.56, respectively.

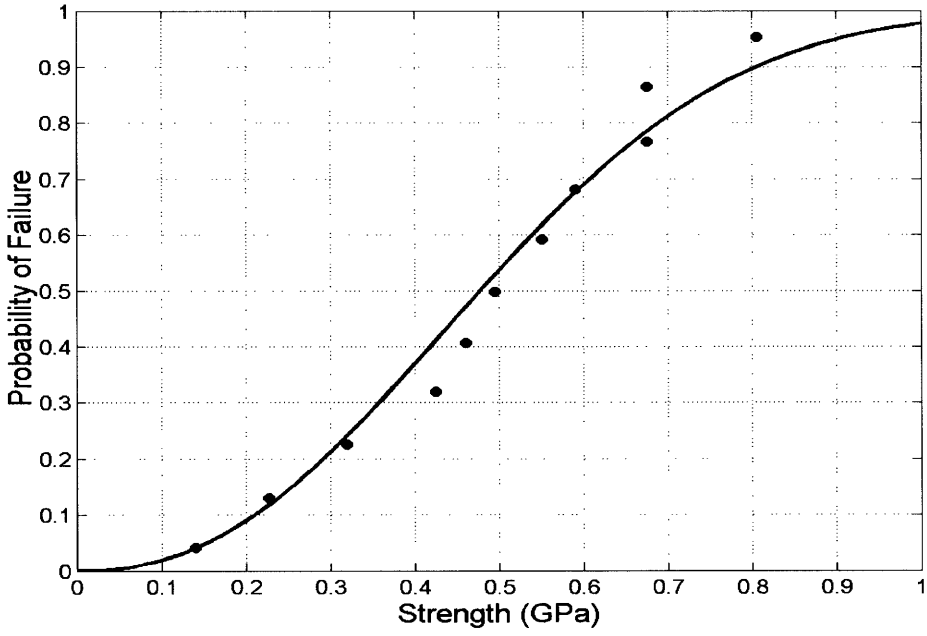


Figure 3-22 Weibull analysis for the data obtained from ISDG tensile tests [K. M. Jackson et al., Mat. Res. Soc. Symp. Proc., Vol. 687, B6.3, Fall 2001].

The Weibull modulus measured by JHU is much lower than that obtained by Hyper-Therm's biaxial tests. The lower Weibull modulus indicates the larger scatter in the data.

The scatter in the strength data is always expected for brittle materials, and some changes to the Weibull modulus will be apparent if more data are added to the statistical analysis, but the lower Weibull modulus might be attributed to the lower quality of the polishing process. The smallest size of the diamond grit used by JHU was 1 μm, and great care was taken during the polishing process, it appears that polishing flaws or damages on the SiC surfaces were unavoidable. This, again, reflects the importance and effect of the surface quality on the strength of brittle materials.

3.4 References

1. F. S. Galasso, Chemical Vapor Deposited Materials, CRC Press, Boca Raton, 1991.
2. R. J. Shinavski, "High Strength, CVD Silicon Carbide for Micro-Gas Turbine Power Generation," Hyper-Therm, Inc., Phase II final report (DAAD19-00-C-0021) to U.S. Army Research Office, December 2002.
3. C. C. Chiu et al., "Low pressure chemical vapor deposition (LPCVD) of β-SiC on Si (100) using MTS in a hot wall reactor," J. Mater. Res., Vol. 8, No. 10, p. 2617-2626, 1993.
4. K. A. Lohner, "Microfabricated Refractory Ceramic Structures for Micro-Turbomachinery," S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, Cambridge, MA, 1999.
5. R. J. Shinavski, "Enhanced Strength, Nanolayered SiC for Micro-Gas Turbine Portable Power Generation," Hyper-Therm, Inc., Phase I final report (DAAD19-99-C-0021) to U.S. Army Research Office, June 1999.
6. K. M. Jackson et al., "Mechanical Properties of Thin Film Silicon Carbide," Mat. Res. Soc. Symp. Proc., Vol. 687, B6.3, Fall 2001.
7. F. Ernst and P. Pirouz, "The formation mechanism of planar defects in compound semiconductors grown epitaxially on {100} silicon substrates," J. Mater. Res., Vol. 4, No. 4, p. 834-842, 1989.
8. P. T. Shaffer, "Engineering properties of carbides," Engineered Materials Handbook, S. J. Schneider (Ed), ASM international, 1991.
9. T. Ohji et al., "Tensile rupture strength and fracture defects of sintered silicon carbide," J. Am. Ceram. Soc., Vol. 72, No. 4, p. 688-690, 1989.
10. S. G. Seshadri et al., "Tensile testing of ceramics," J. Am. Ceram. Soc., Vol. 70, No. 10, p. C242-C244, 1987.
11. K. M. Jackson, "The Mechanical Properties of 3C Thin-Film Silicon Carbide," Ph.D. thesis, Ph. D. Thesis, Dept. of Mechanical Engineering, Johns Hopkins University, Baltimore, MD, 2002.
12. K.-S. Chen et al., "Controlling and testing the fracture strength of silicon on the mesoscale," J. Am. Ceram. Soc., Vol. 83, No. 6, p. 1476-1484, 2000.
13. K.-S. Chen, "Materials Characterization and Structural Design of Ceramic Micro Turbomachinery," Ph. D. Thesis, Dept. of Mechanical Engineering, MIT, Cambridge, MA, 1999.
14. M. F. Ashby and D. R. Jones, Engineering Materials I, 2nd Ed. Butterworth-Heinemann, Oxford, 1996.
15. M. F. Ashby and D. R. Jones, Engineering Materials II, 2nd Ed. Butterworth-Heinemann, Oxford, 1998.
16. W. N. Sharpe, Jr. et al., "A New Technique for measuring Poisson's ratio of MEMS materials," Mat. Res. Soc. Proc., Vol. 444, p. 185-190, 1997.

CHAPTER 4

RESIDUAL STRESS CONTROL IN CVD SILICON CARBIDE

Residual stress control of the SiC coatings is of critical importance not only to the CVD process itself, but also to all other post-CVD processes since residual stress-induced wafer bow is detrimental to planarization and wafer bonding processes. Therefore, it is important to characterize and quantify the residual stress in the SiC coatings on Si wafers. This chapter presents the characterization efforts made to examine the relationships between key CVD process parameters and the corresponding residual stress states in SiC coatings. Engineering approaches to achieve low-levels of residual stress states are also described along with the explanations of the origins of residual stress components in the CVD SiC coatings.

4.1 Components of residual stress and calculations

4.1.1 Components of residual stress in polycrystalline materials

A brief introduction to the development of residual stresses in CVD SiC deposited on Si wafers is first presented. In general, the residual stress development in polycrystalline materials is associated with the two components: thermal and intrinsic stresses.

4.1.1.1 Thermal residual stress

Thermal residual stress develops in the SiC film during cooling to room temperature following the deposition at high temperatures, due to the thermal mismatch between the SiC and the Si substrate. For a relatively thin SiC film, the thermal stress can be calculated by the following equation [1]:

$$\sigma_{th} = \Delta T(\alpha_{SiC} - \alpha_{Si}) E_{SiC}/(1 - \nu_{SiC}) \tag{4-1}$$

where ΔT is the temperature difference between the deposition and room temperatures (= $T_{dep} - T_{room}$), α is the (average) coefficient of thermal expansion (CTE), and $E/(1-\nu)$ is the biaxial modulus with the subscripts SiC and Si referring to the two materials.

4.1.1.2 Intrinsic residual stress

Intrinsic residual stress, the second contribution to the total residual stress, develops during the film deposition process. Intrinsic stress magnitudes and sign (tension or compression) are governed by multiple interacting mechanisms that are not well understood for many deposition processes [2]. Grain boundaries and impurities are generally known as sources of intrinsic tensile and compressive stresses, respectively. The presence of grain boundaries in polycrystalline materials introduces tensile stresses owing to attractive atomic forces acting across the grain boundaries [2, 3]. Compressive intrinsic stresses are generally observed in metal films produced under the conditions that favor energetic particles striking the growing films as in a sputtering process. In the cases of non-energetic particle depositions, impurities such as water vapor, oxygen, and hydrogen gases have been reported to be the sources of intrinsic compressive stresses. The sources of intrinsic residual stress in CVD SiC will be discussed in section 4.3.2.

4.1.2 Residual stress calculation using laminated plate theory

Curvature measurement is one of the most widely used techniques for measuring stresses in thin films deposited on substrates. The well-known Stoney formula relates the

residual stress in a thin film to the curvature κ of the substrate to which the film is bonded [4]. The advantage of using the Stoney equation is that the residual stress in the film can be determined without knowing the mechanical properties of the film material, since the equation is derived based on the assumptions that the film thickness is much less than the substrate thickness, and the stiffness of the film-substrate system of interest is dependent only on the mechanical properties of the substrate [5]. However, many film-substrate systems exist where these assumptions are violated. A thick CVD SiC coating deposited on a silicon substrate for use as a refractory reinforcement in the micro-engine is an example, in that the relative thickness of the SiC coating to Si substrate is not negligible. Moreover, the stiffness of SiC is much greater than that of silicon [6]. Hence, more general approaches are required so that the residual stress levels of such systems can be properly determined. In this work classical laminated plate theory has been used as a general approach to determine the stress levels in SiC coatings deposited on Si substrates. By use of the theory, the intrinsic stress in the SiC coatings, inherent to the CVD process, involving materials deposition and growth at high temperatures, can be isolated from the thermal stress which is induced during cooling to room temperature after high temperature deposition.

A laminate is composed of two or more laminae bonded together to act as an integral structural element, and the constitutive equation that relates the mid-plane strains ε and curvatures κ of the laminate to the imposed forces and moments is given by [7]:

$$\begin{bmatrix} N \\ M \end{bmatrix} = \begin{bmatrix} A & B \\ B & D \end{bmatrix} \begin{bmatrix} \varepsilon \\ \kappa \end{bmatrix} \tag{4-2}$$

where $[A]$, $[B]$, and $[D]$ are the in-plane, coupling, and bending stiffness matrices of the laminate, respectively. N and M are the stress and moment resultants acting on the laminate. To determine both the thermal and intrinsic stresses, the general constitutive equation 4-2 is first solved directly for the coating (SiC) and substrate (Si) thermal stresses, as the thermoelastic properties of the laminate and temperature change from its

deposition temperature (at which a thermal stress-free state is assumed) are known. Following the determination of thermal stresses, the equation is solved once again for the intrinsic stress components via superposition. The intrinsic in-plane strain is therefore given by the difference between the total in-plane strain and the thermal in-plane strain. Likewise the intrinsic curvature can be obtained from the difference between the total curvature and the thermally-induced curvature. The total curvature can be measured by laser profilometry. The procedure for calculating thermal and intrinsic stresses is described below in greater detail.

4.1.2.1 *Calculation of thermal residual stresses in SiC and Si layers*

The system of interest here is a SiC-Si two-layer laminate whose geometry is depicted in Figure 4-1.

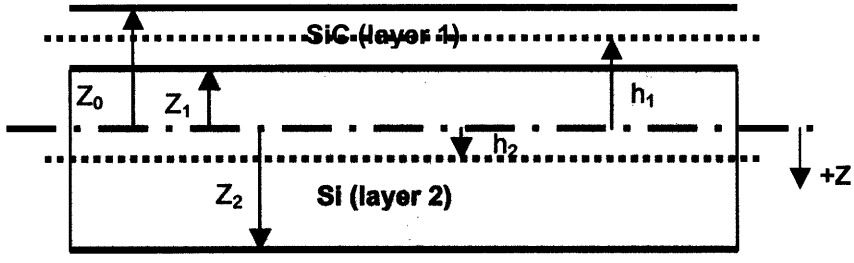


Figure 4-1 Geometry of the SiC-Si two-layer laminate material.

The geometry of the SiC-Si laminate is defined in terms of the thicknesses of SiC and Si layers as follows.

$$z_0 = -t_{sum}/2,\ z_1 = -t_{sum}/2 + t_{SiC},\ z_2 = t_{sum}/2 \tag{4-3}$$

where t_{sum} is the sum of the thicknesses of all the existing layers. That is $t_{sum} = \sum_{k=1}^{n} t_k$ and is just the sum of the thicknesses of SiC (t_{SiC}) and Si (t_{Si}) layers.

Thus the in-plane, coupling, and bending stiffnesses are given as:

$$A = \sum_{k=1}^{n} \frac{E_k}{1-\nu_k}(z_k - z_{k-1}),\ B = \frac{1}{2}\sum_{k=1}^{n} \frac{E_k}{1-\nu_k}(z_k^2 - z_{k-1}^2),\ D = \frac{1}{3}\sum_{k=1}^{n} \frac{E_k}{1-\nu_k}(z_k^3 - z_{k-1}^3) \quad (4\text{-}4)$$

where E and ν are the Young's modulus and Poisson's ratio of each layer, respectively. Here, $k = 1$ and 2 correspond to layer 1 (SiC layer) and layer 2 (Si layer). $E_{SiC} = 420$ GPa, $E_{Si} = 165$ GPa, $\nu_{SiC} = 0.21$, and $\nu_{Si} = 0.27$ are used for the present study. Equations 4-4, however, can also be used for multilayers composed of any number of layers. The resultant thermal stresses and moments acting on the SiC-Si laminate, which are induced during the cooling process down to room temperature following the SiC deposition at high temperature, are obtained by the integration of the stresses in each layer across the laminate thickness.

$$N_{therm} = \sum_{k=1}^{n} \int_{z_{k-1}}^{z_k} \sigma dz = (T_0 - T_{dep}) \sum_{k=1}^{2} \frac{E_k \alpha_k}{1-\nu_k}(z_k - z_{k-1}) \quad (4\text{-}5)$$

$$M_{therm} = \sum_{k=1}^{n} \int_{z_{k-1}}^{z_k} \sigma z dz = \frac{(T_0 - T_{dep})}{2} \sum_{k=1}^{2} \frac{E_k \alpha_k}{1-\nu_k}(z_k^2 - z_{k-1}^2) \quad (4\text{-}6)$$

where α is the thermal expansion coefficient of each layer and T_{dep} and T_0 are the SiC deposition temperature and room temperature, respectively. The integration is performed on a unit length basis and thus N_{therm} is a force per unit width of the cross section of the laminate and M_{therm} is also a moment per unit width. The thermally-induced mid-plane strain ε_{therm} and curvature κ_{therm} of the SiC-Si laminate can now be calculated from Equation 4-2 where all the matrix components are known. The thermal residual stresses in SiC and Si layers are obtained by substituting the calculated ε_{therm} and κ_{therm} values via:

$$\sigma_k^{therm} = \frac{E_k}{1-\nu_k}[\varepsilon_{therm} + h\kappa_{therm} - \alpha_k(T_0 - T_{dep})] \quad (4\text{-}7)$$

Here again, k = 1 and 2 correspond to layer 1 (SiC) and layer 2 (Si), and h is the distance from the mid-plane of the laminate to the plane where the stress is to be calculated. A thermal residual stress at any particular plane perpendicular to the z-direction can be easily determined by using an appropriate value for h. For example, the average thermal residual stresses in the SiC coating and Si substrate can be obtained by setting $h = h_1 = (z_0 + z_1)/2$ and $h = h_2 = (z_1 + z_2)/2$, respectively. The thermal residual stress on the top surface of the SiC layer can also be obtained by setting $h = z_0$.

4.1.2.2 *Calculation of intrinsic residual stress in SiC layer*

Based on the assumption of superposition (i.e., the total residual stress consists of the two components of thermal and intrinsic stresses), the intrinsic mid-plane strain-curvature state in the SiC can be obtained by:

$$\begin{bmatrix} \varepsilon_{tot} - \varepsilon_{therm} \\ \kappa_{tot} - \kappa_{therm} \end{bmatrix} = \begin{bmatrix} A & B \\ B & D \end{bmatrix}^{-1} \begin{bmatrix} N_{int} \\ M_{int} \end{bmatrix} \tag{4-8}$$

where the total in-plane strain (ε_{tot}), the intrinsic stress resultant (N_{int}) and the intrinsic moment resultant (M_{int}) are unknown quantities. κ_{tot}, the total curvature of the SiC-Si laminate, is easily measured using a laser profilometer, in this case the Tencor FLX-2320^{TM}. The intrinsic residual stress originates solely from the SiC layer as the deposition of CVD SiC progresses and thus the integration of N_{int} along the z-direction simply results in the product of N_{int} and h_1, the distance from the mid-plane of the laminate to the mid-plane of the SiC layer. That is M_{int} can be described as a function of N_{int} as follows.

$$M_{\text{int}} = N_{\text{int}} h_1 \tag{4-9}$$

The unknown quantities are now reduced to ε_{tot} and N_{int}, both of which can be calculated from Equation 4-8. ε_{int} and κ_{int}, the mid-plane strain and the curvature of the SiC-Si laminate caused by the intrinsic stress, are obtained simply by subtracting ε_{therm} and κ_{therm} from ε_{tot} and κ_{tot}, respectively. The intrinsic residual stress in the SiC layer can now be obtained from the following equation.

$$\sigma_{SiC}^{\text{int}} = \frac{E_{SiC}}{1-\nu_{SiC}}[\varepsilon_{\text{int}} + h\kappa_{\text{int}} - \frac{1-\nu_{SiC}}{E_{SiC}t_{SiC}}N_{\text{int}}] \tag{4-10}$$

where the last term in the bracket of Equation 4-10 is a term equivalent to the $\alpha\Delta T$ term of Equation 4-7 used for thermal residual stress calculation. This term accounts for the intrinsic strain difference when the SiC layer is attached to the Si substrate and when the SiC layer is separated from the Si substrate and is thus free to extend or shrink without any restriction.

4.2 Residual stress control in SiC by changing CVD parameters

Chemical vapor deposition using the thermal decomposition of methyltrichlorosilane (MTS) in the presence of hydrogen has been found to be an efficient way of controlling residual stress in SiC. The intrinsic stresses over the range of process parameters in this study were always observed to be compressive, and varied from 100 MPa to 1.5 GPa. These results were found to be very reproducible. Therefore, the engineering approach to achieving a net-zero residual stress state in CVD SiC at room temperature was to balance the compressive intrinsic stresses with the tensile thermal stresses. The intrinsic stress was investigated as a function of source gas ratio (H_2/MTS), deposition temperature, and the amount of HCl addition (MTS/HCl).

4.2.1 Gas ratio vs. residual stress

Figure 4-2 shows the variation of the thermal stress and the intrinsic stress as well as the total stress with the molar gas ratio of H_2 to MTS. Less dilution of the MTS with hydrogen results in a more compressive intrinsic stress state. In this case, the thermal stresses are nearly constant as all the data points were obtained from the SiC layers deposited at the same temperature (~1000 °C). The small variations found in the thermal stresses are due to small variations in the thickness of the SiC coatings and silicon substrates.

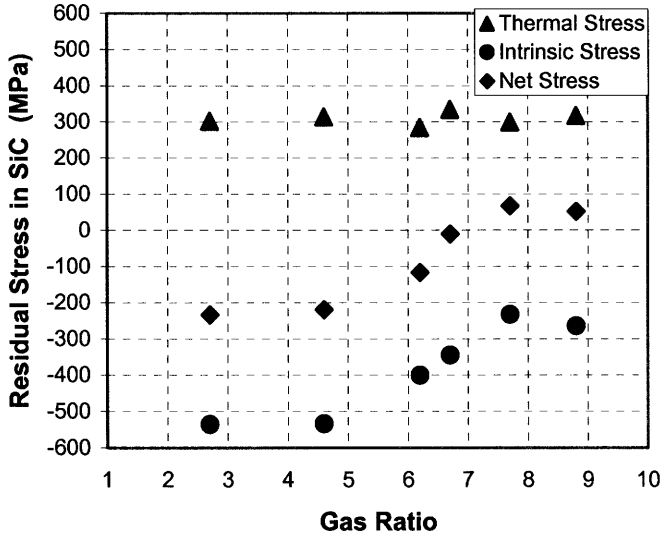


Figure 4-2 Residual stress variance with gas ratio α (H_2:MTS).

4.2.2 Deposition temperature vs. residual stress

Similarly, the residual stress variation with deposition temperature is shown in Figure 4-3, where all the data points were obtained from ~30 μm thick SiC coatings deposited on 525 μm thick silicon substrates. The intrinsic stress was found to be a very strong function of deposition temperature; lower temperatures result in a more compressive intrinsic stress. The intrinsic stress changes by more than 200 MPa as the deposition temperature changes by only 25 °C.

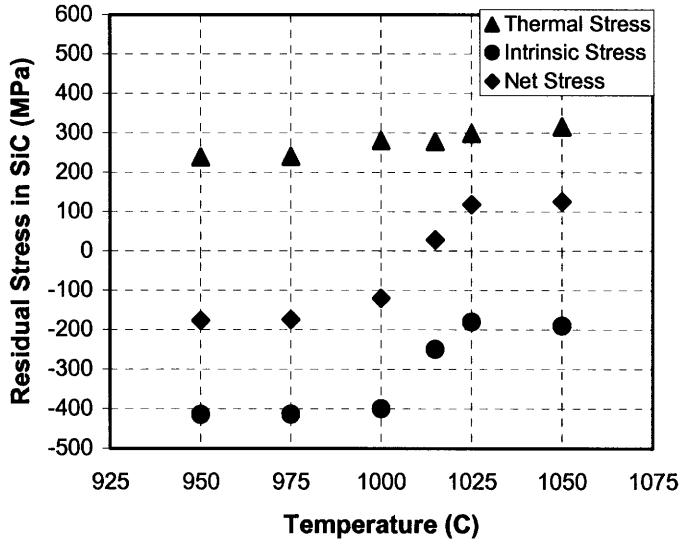


Figure 4-3 Residual stress variance with deposition temperature (°C).

The plateau of intrinsic stress at -400 MPa is believed to be an artifact of the deposition process. That is, high compressive stresses in the SiC coatings at the deposition temperatures would result in significant wafer bow, which allows SiC to deposit on the backside of the wafers. This effect, which could balance the stress in the SiC on the front (target) sides, was not taken into consideration in the stress calculations, leading to an apparently lower stress level than was actually present. Therefore, the precise measurement of residual stress by curvature measurements is significantly limited by the ability to process and handle wafers.

4.2.3 HCl concentration vs. residual stress

Adding HCl into the MTS-H_2 gas stream was found to have a significant effect on the intrinsic stress states in the SiC layers, which results in very high compressive stresses. Figure 4-4 shows the intrinsic stress state for a number of CVD conditions, where a clear correlation between the intrinsic stress and the MTS/HCl ratio was found, suggesting that this is the most effective way of producing very high compressive

residual stress states in CVD SiC. Compressive intrinsic stresses on the order of 1.5 GPa were observed for a large amount of HCl addition, this is a far higher value than could be obtained by changing either gas ratio or deposition temperature.

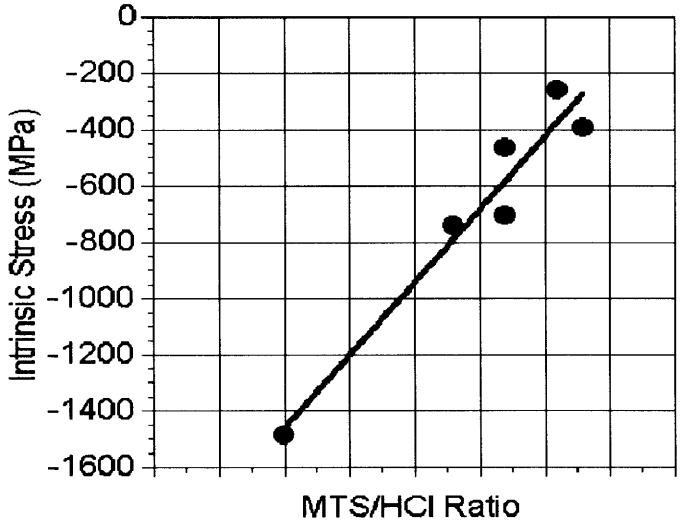


Figure 4-4 Intrinsic stress variation with MTS/HCl ratio.

4.2.4 SiC thickness vs. residual stress

The effects of SiC film and silicon substrate thicknesses on the residual stress states were also investigated to determine the behavior of intrinsic stress as well as to confirm the assumption of superposition of residual stress components. The net residual stress in CVD SiC was observed to change significantly (by more than 200 MPa) with SiC thickness as shown in Figure 4-5. It should be noted in Figure 4-5 that the residual stress change is due entirely to the change in thermal stress component, and the intrinsic stress does not change significantly with SiC thickness and is essentially constant at 200~300 MPa in compression. This observation is further supported by Figure 4-6 in which the intrinsic stress is plotted as a function of SiC thickness, for much thinner films (0.2 - 0.4 μm) than those of Figure 4-5. Although data scatter exists, the intrinsic stress was found to range from -200 to -350 MPa. This variation in stress is within the scatter observed when the CVD process was repeated several times. Therefore, the intrinsic stress level in

CVD SiC appears to be developed fully at the early stage of film growth and then maintained without significant change during further growth.

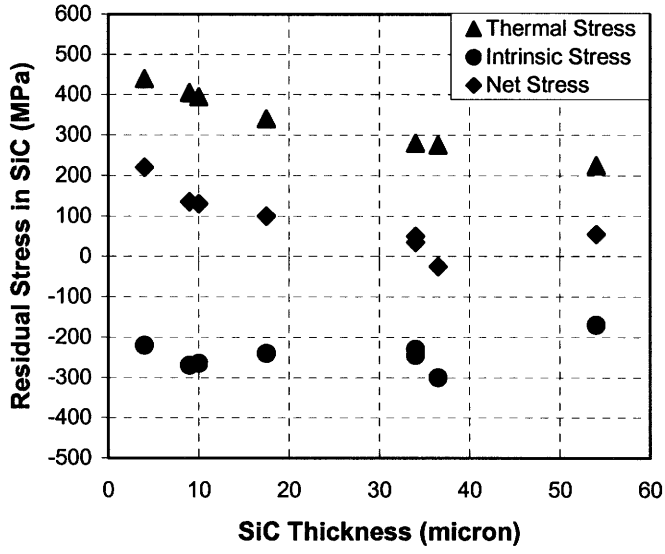


Figure 4-5 Residual stress variance with SiC thickness.

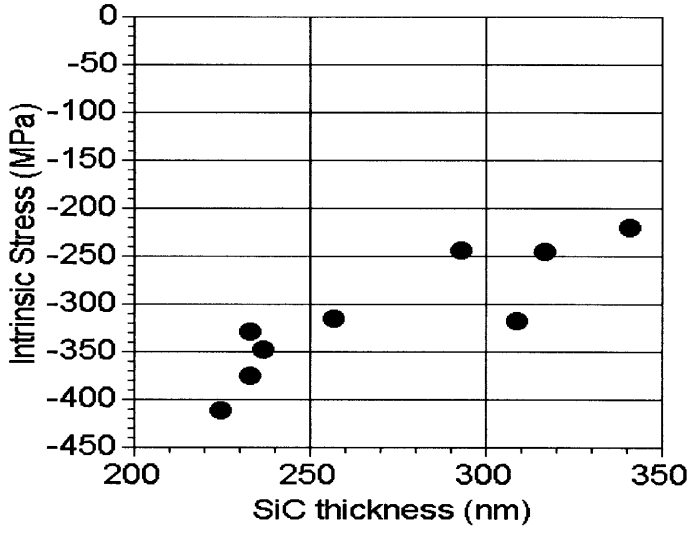


Figure 4-6 Intrinsic stresses for thin SiC layers.

4.2.5 Si (substrate) thickness vs. residual stress

The observation of the intrinsic stress variance with silicon substrate thickness is shown in Figure 4-7, which can be used to validate the assumptions of superposition and deconvolution of residual stress components. Figure 4-7 demonstrates that the intrinsic stress is independent of the silicon substrate thickness, while the thermal stress is dependent on it. However, even the thermal stress is largely unaffected by the wafer thickness above a value of 1000 μm. This reflects the configuration approaching the thin film limit. Again, the range of intrinsic stresses was observed to be between -200 to -300 MPa, the variation of which is considered to be within the nominal scatter.

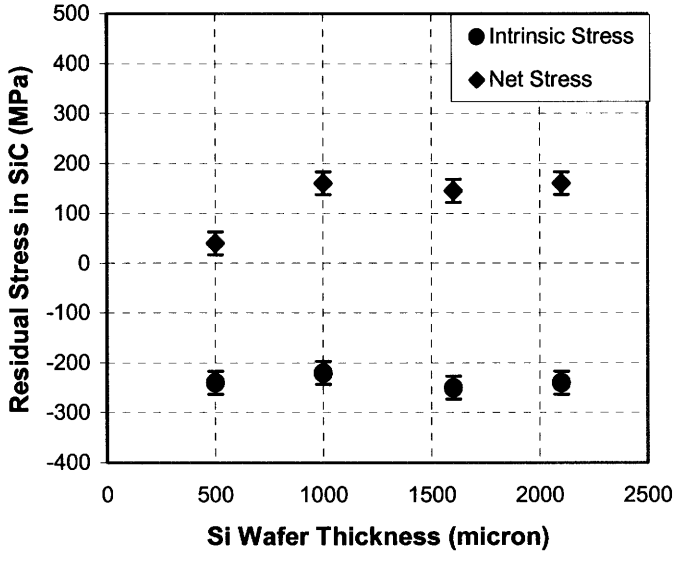


Figure 4-7 Intrinsic stresses variance with silicon substrate thickness.

4.2.6 Wafer curvature measurements as a function of temperature

Curvature measurement was also performed on two SiC coated 4-inch, 525 μm thick Si wafers as a function of temperature up to 800 °C using a Tencor FLX-2908™ laser profilometer. The two wafers were in different residual stress states: one had a relatively

thin (~4.1 μm thick) SiC, which was in a net residual tensile stress (~240 MPa), while the other had a much thicker (~37 μm thick) SiC coating, which was in a net residual compressive stress (~40 MPa) at room temperature. Figure 4-8 shows the variations of radii of curvature for the two wafers as a function of temperature.

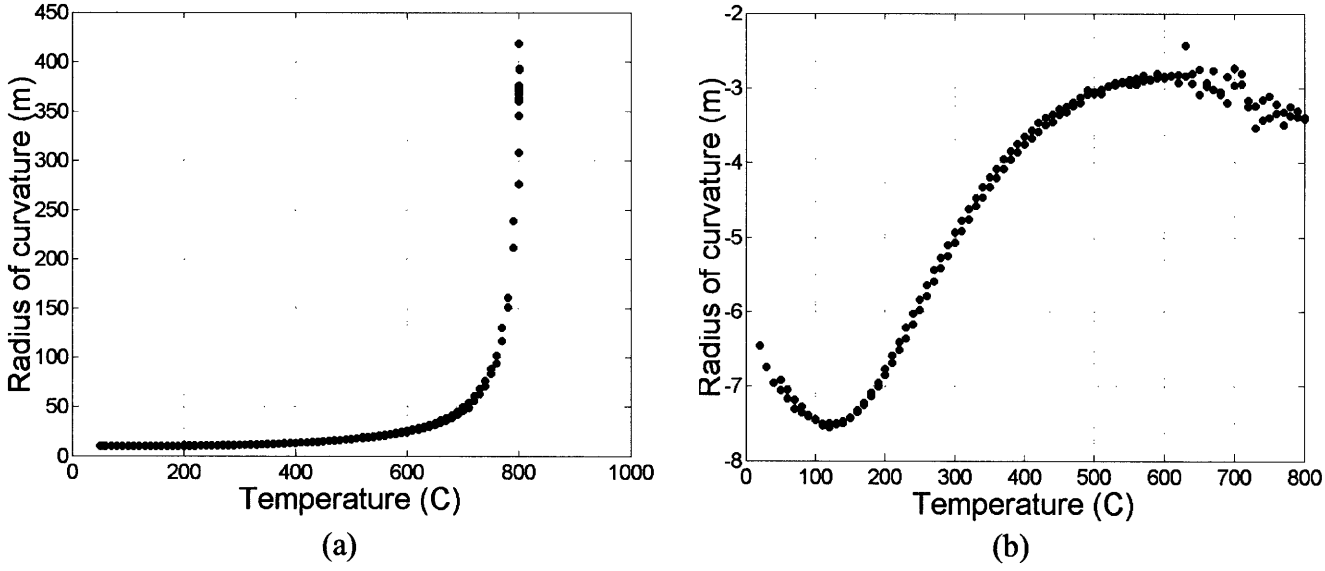


Figure 4-8 Variations of radius of curvature at a function of temperature: (a) 4.1 μm thick SiC in residual tension at room temperature. (b) 37 μm thick SiC in residual compression at room temperature.

The behavior of the wafer with 4.1 μm thick SiC was simple and close to the expectation that the thermally-induced residual tensile stress is released continuously as temperature increases, while the wafer with 37 m thick SiC showed a complex shape with two vertical points, a maximum and a minimum point. The radii of curvature were also converted into the corresponding residual stresses as shown in Figure 4-9, where the intrinsic stress components appeared to increase at low temperatures from ambient to ~200 °C in both cases. However, the increase in intrinsic stresses is unlikely to be real, but is believed to reflect the overestimation of the thermal residual stress components; the overestimation of the thermal residual stress would result in an underestimation of the intrinsic stress given a fixed total (net) residual stress. The overestimation of thermal

residual stresses in the lower temperature range seems to be attributable to the use of incorrect CTE values of SiC. The difference in CTE between Si and SiC might be smaller than that used for the calculation of thermal stresses in Figure 4-9, a detailed discussion of which is described in Appendix B.

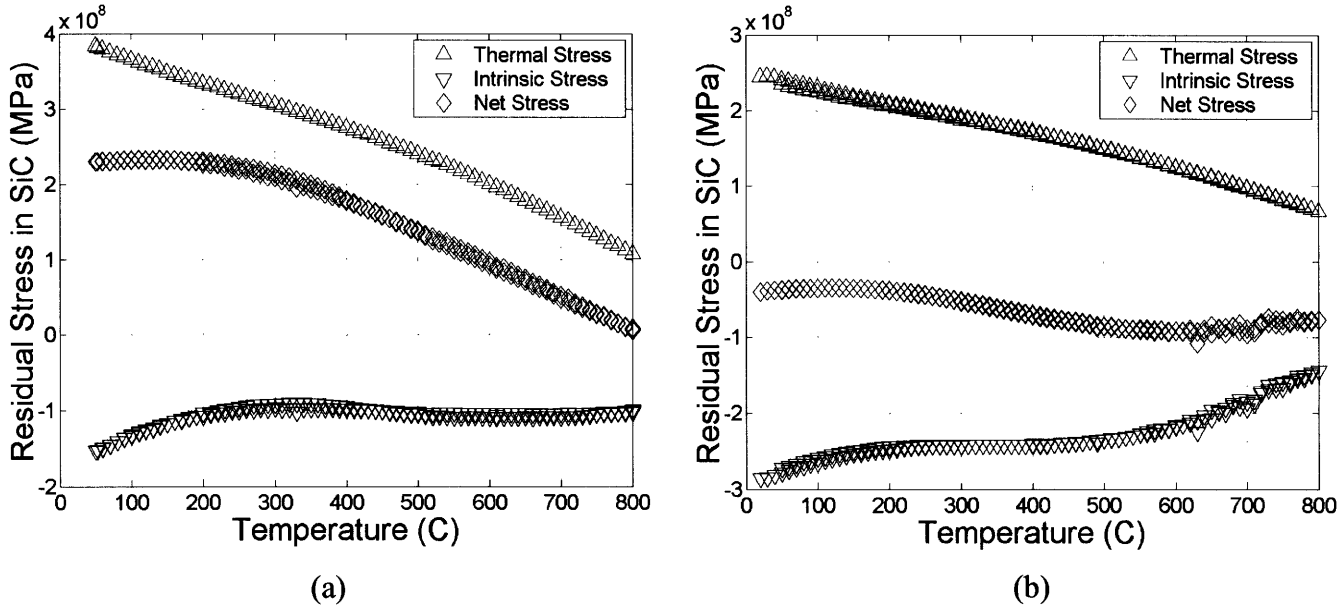


Figure 4-9 Conversion of radii of curvature of Figure 4-8 into residual stresses: (a) 4.1 μm thick SiC with a compressive intrinsic stress of ~100 MPa. (b) 37 μm thick SiC with a compressive intrinsic stress of ~240 MPa.

As mentioned in earlier parts of section 4.2, the intrinsic stress is believed to remain almost constant with varying temperatures. Then, the intrinsic stresses of the 4.1 μm and 37 μm thick SiC coatings can be considered as constants of -100 MPa and -240 MPa, respectively. While the slight increase in intrinsic stress at low temperature ranges is believed to originate from the incorrect CTE data, the increase in intrinsic stress and the noise in the data for the thicker SiC at temperature above 600 °C in Figure 4-9 (b) may be attributable to the local yielding of the Si substrate at high temperatures.

4.2.7 Summary of residual stress control in CVD SiC

In conclusion, low levels of residual stress can be achieved either by changing each of the process parameters such as gas ratio, temperature, and HCl addition individually or by varying two or more of them simultaneously.

Hyper-Therm's CVD process was found to be reproducible. The intrinsic stress of SiC can be controlled to within a standard deviation of 15 - 16 MPa between wafers both from the same and between different CVD process runs.

While the intrinsic residual stress was found to be always compressive and independent of SiC thickness up to ~50 μm, the thermally-induced tensile stress changes with SiC thickness. Therefore, whenever the target SiC thickness changes, (slight) modifications need to be made to the CVD parameters. That is, the thinner the target SiC coating is, the higher the tensile thermal stress. To compensate for the higher tensile thermal stresses, CVD recipes generating higher compressive intrinsic stresses must be used for thinner SiC coatings.

4.3 Origins of residual stresses in CVD SiC

It is critical that the mechanisms of residual stress generation during the CVD process be understood in order to control the residual stress to a level that would be acceptable for subsequent processing steps and in the final application. In general, stress developments in polycrystalline films are associated with both thermal and intrinsic stresses.

4.3.1 Origin of thermal residual stress

As described in the method of stress calculation, thermal stress development is simply due to the thermal mismatch between SiC and Si substrates. It should be noted that the coefficient of thermal expansion (CTE) of a material is a function of temperature, and thus, the mean CTE values of SiC and Si obtained from integration over the temperature ranges of interest must be used for thermal stress calculation. More detailed discussion of the method of obtaining mean CTE values of SiC and Si can be found in Appendix B. For the present work, $\alpha_{SiC} = 4.6 \times 10^{-6}$ K^{-1} and $\alpha_{Si} = 3.9 \times 10^{-6}$ K^{-1} were used as the mean CTE values for SiC and Si, respectively. The thermal expansion mismatch between SiC and Si causes the CVD SiC to be in tension and the Si substrate to be in compression, since SiC tends to shrink more than Si during cooling, assuming both SiC and Si to be in zero-stress state during the deposition. This corresponds to the fact that SiC has a greater mean CTE value than Si.

4.3.2 Origins of intrinsic residual stresses

4.3.2.1 Compositional study of CVD SiC

Intrinsic stress is more interesting since it develops during the film growth in a way that is determined by both the thermodynamics and kinetics of the deposition process [2]. Intrinsic stress arises when a film undergoes any microstructural evolutions that cause its density to change, while still being firmly attached to its substrate throughout the growth process [8]. Intrinsic stress can be generated by the existence of grain boundaries or defects such as dislocations, voids, etc. [9]. As is well known from the grain boundary relaxation model, grain boundaries are the most widely known sources of tensile intrinsic stress [2]. The presence of grain boundaries in polycrystalline materials introduces tensile stresses during the material growth due to the volume decrease caused by attractive atomic forces acting across the grain boundaries [3]. Compressive intrinsic stress is generally observed in metal films prepared under the conditions where the growing films are bombarded by energetic atoms that penetrate into interstitial or lattice positions and eventually push neighboring atoms into interstitial positions [10]. Thus, the remaining gas atoms that do not escape from a film during the deposition (atomic

peening) generate compressive stresses. In the cases of non-energetic particle depositions, impurities such as oxygen, water vapor, and hydrogen gases, have been observed to be the principal sources of intrinsic compression. For instance, it has been reported that water vapor and oxygen produce compressive stress in fluorinated silicon-oxide thin films and iron and nickel alloy films, respectively [11, 12]. For columnar polycrystalline silicon films, excess (interstitial) atoms deposited at grain boundaries have been suggested to be a cause of intrinsic compression [13, 14]. Similarly, oxygen was considered a probable cause of compressive stress in LPCVD SiC films by Hurtós et al. such that higher oxygen content was expected to produce a higher compressive stress state [9].

To identify the purity of the LPCVD SiC in the present work, glow discharge mass spectrometry (GDMS) and secondary ion mass spectrometry (SIMS) were used. The GDMS analysis indicated that the CVD SiC was of very nearly stoichiometric composition containing metallic impurities at levels less than 5 ppm in total with chlorine and boron as the major impurities as shown in Table 4-1.

Table 4-1. GDMS results of CVD SiC[1]

C	30 wt%
Si	70 wt%
B	1.9 ppm wt
Cl	3.8 ppm wt
Na	0.02 ppm wt
Al	0.01 ppm wt
P	0.06 ppm wt
S	0.09 ppm wt
Fe	0.31 ppm wt

[1] 66 other elements below the detection limits

Although the GDMS analysis does not provide reliable information about oxygen and nitrogen contents due to the desorption of species adsorbed on the SiC surface, it indicates that the CVD SiC is of high purity (better that 99.999 %), which implies that it should not cause any contamination issues in the fabrication steps using standard silicon wafer processes as encountered by some researchers [15].

Secondary ion mass spectrometry (SIMS) was used to analyze the oxygen and nitrogen contents in the SiC films. Three SiC samples with significantly different states of compressive stress, achieved by controlling deposition temperatures, were analyzed. A typical SIMS analysis for oxygen and nitrogen concentrations is shown in Figure 4-10. Oxygen concentration was observed to range from 20 to 74 ppm while nitrogen concentration was 0.1 ppm in all samples. Oxygen concentration for all SiC samples was significantly higher within ~50 nm in depth from the surface, which is presumably due to the formation of a native oxide on the surface and subsequent diffusion. However, no correlation was found between oxygen content and intrinsic compression (and thus deposition temperature). This suggests that the impurity atoms of oxygen and nitrogen do not cause the generation of compressive intrinsic stress in SiC coatings.

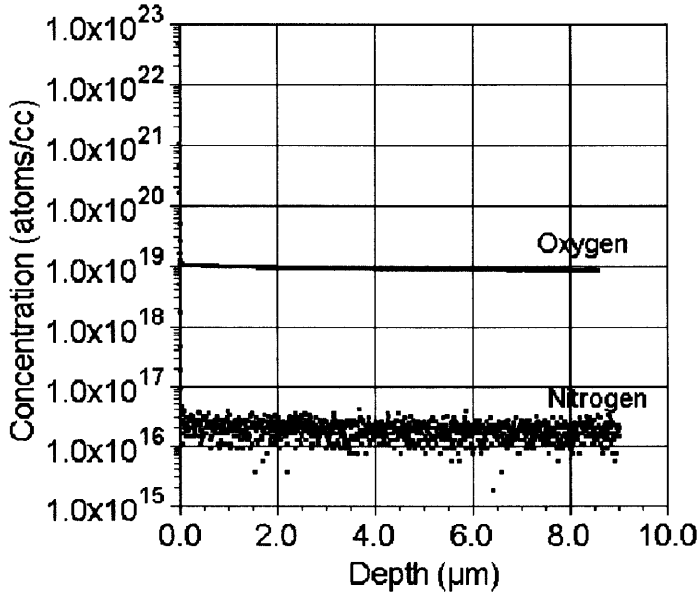


Figure 4-10 SIMS analysis showing oxygen and nitrogen concentrations.

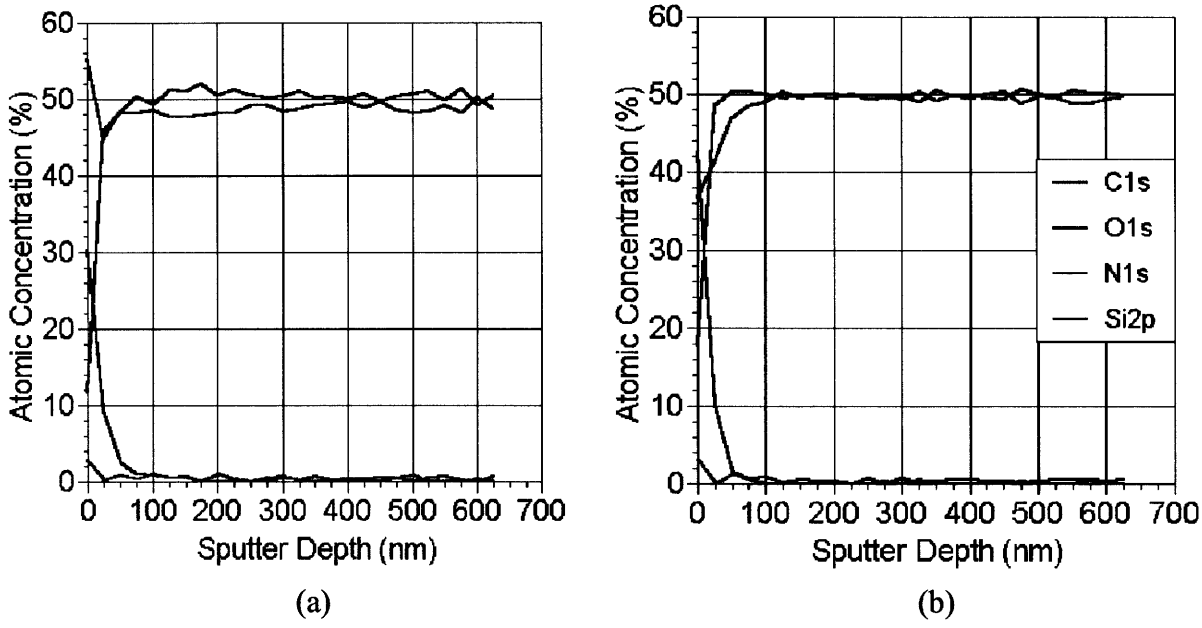


Figure 4-11 XPS compositional analyses: (a) Sample 1 was in intrinsic compression of 296 MPa. (b) Sample 2 was in intrinsic compression of 536 MPa.

Having excluded impurity gas inclusions as a source of compressive stress, attention was paid to the C:Si stoichiometry of CVD SiC as incorporation of excess carbon or silicon atoms could have the same "push" effects as other impurity atoms causing compressive stress. To identify more accurately the C:Si stoichiometry, x-ray photoelectron spectroscopy (XPS) analyses were performed on two samples of CVD SiC with significantly different intrinsic compressive levels. Although the compressive (intrinsic) stress levels of samples 1 and 2 were -296 MPa and -536 MPa respectively, the XPS analyses showed only very slight compositional differences between the two samples, as depicted in Figure 4-11.

Sample 1 shows a slightly higher C/Si ratio of 1.03 ± 0.03 as compared to 1.00 ± 0.02 in sample 2. This slight difference could be attributed to either an actual stoichiometric difference between the two SiC samples or simply an artifact caused by the readsoprtion of hydrocarbon from the vacuum environment. However, even if the slight non-

stoichiometry is a real effect, sample 1 does not show the significantly higher level of compressive stress, which is expected due to the effect of small impurity atoms on the deposit. Therefore, such non-stoichiometry, regardless of whether it is real or apparent, does not correlate with the observations of intrinsic compressions in CVD SiC. This conclusion could be further confirmed by the XPS analysis on the elemental bonding states as shown in Figure 4-12.

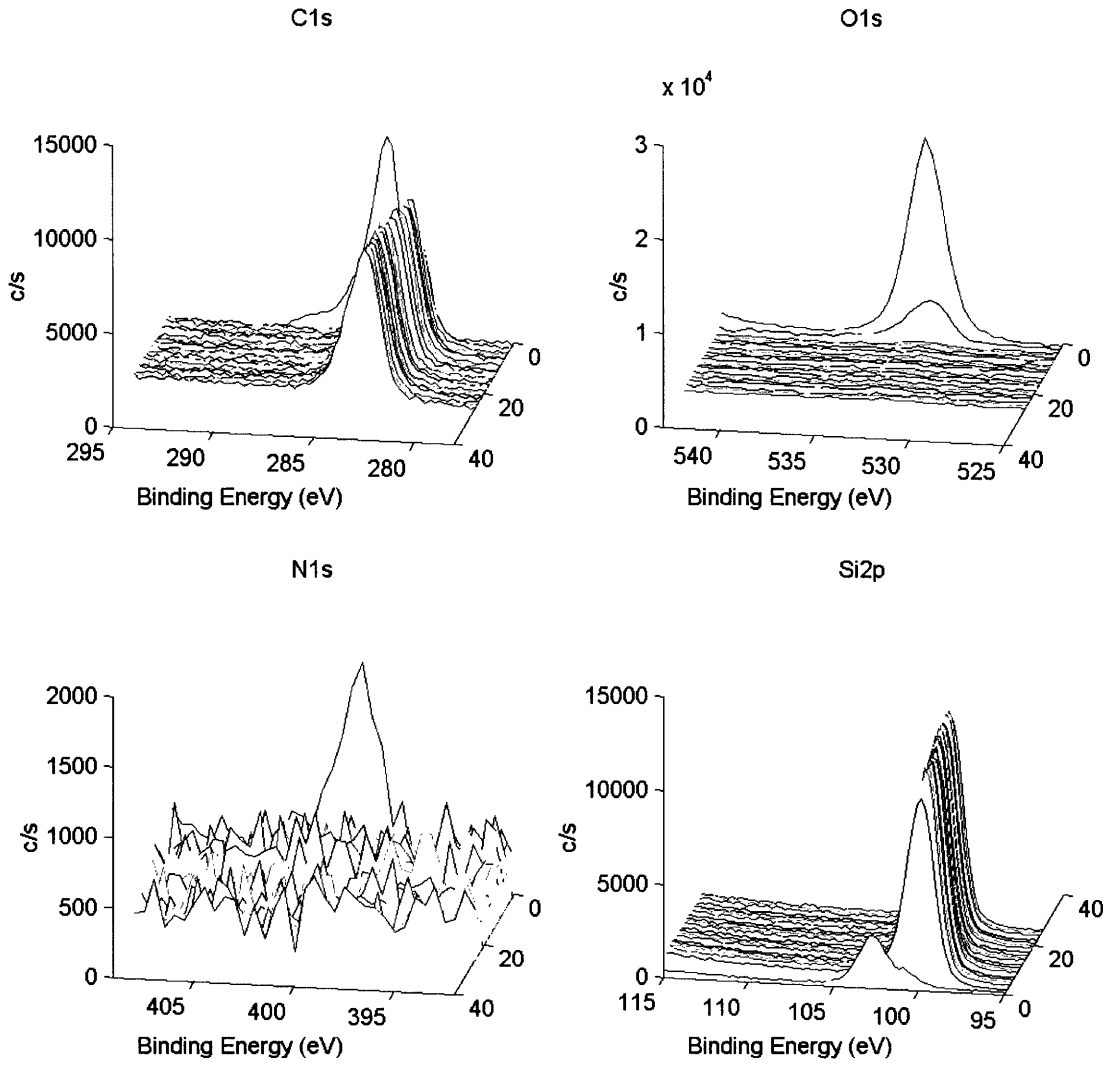


Figure 4-12 Binding energies determined by XPS shows that only Si-C bonding (as SiC) can be detected within the bulk of the film as indicated by Si2p and C1s binding energies. N1s is present only at the surface. SiO_2 and $Si_xO_yC_z$ bindings of Si2p can be detected as the surface to a depth of ~50 nm.

Only Si-C bonding was observed in the samples, except for significant SiO_2 bonding and a small fraction of $Si_xO_yC_z$ at the surface, which is presumed to be from native oxide on the surface. Neither any evidence of C-C and Si-Si bonding nor inclusion of excess silicon atoms was observed in the SiC samples as reported by Garshasb [16]. Thus, the CVD SiC films are likely to be stoichiometric within the bulk of the deposit without excess carbon or silicon atoms, which is supported by previous reports that the CVD SiC films produced under similar process conditions showed stoichiometric compositions without excess silicon or carbon atoms [17].

4.3.2.2 Surface stress of SiC

In an effort to explain the origin of intrinsic stresses that have always been observed to be compressive in the CVD SiC deposits on silicon substrates, consideration was given to surface stress, another important contribution to the stress evolution of deposited thin films featuring island growth. Surface stress in a crystalline solid arises as the atoms in the vicinity of the surface have a different number of bonds from the interior atoms [18]. As a result, the surface atoms have an equilibrium interatomic distance that is different from that of the interior atoms unless the surface atoms were forced to remain coherent with the underlying lattice of the bulk material [19]. The compressive stress generation during the island growth of a film can be explained from this premise. One key feature of the model is the prediction of a crystal size effect. As an island increases in size, the lattice distance of the island keeps being adjusted to its equilibrium distance were it not constrained by the substrate. Therefore, at some point during a film deposition, if the island grows and reaches a critical size at which the island is firmly attached to the substrate and is no longer able to elastically deform to adjust its in-plane lattice distance to the equilibrium spacing, any further film growth beyond that point will result in an intrinsic stress generation.

In an effort to model the intrinsic stress developing in the island growth mode, Nix and Clemens proposed a two-dimensional model based on an array of crystallites with an

elliptical shape that coalesce to become very long cycloidal islands [20]. However, a more realistic model for the very early stage of film growth would be a two-dimensional array of cylindrical disks placed on the substrate with the cylindrical axes normal to the substrate surface [21]. When consideration of a balance between the surface and volume stresses at equilibrium (which is well known as the Laplace formula) is given to a cylindrical disk of thickness t and radius r (where r is much greater than t), a surface stress f, including the effects from both the top and bottom surfaces, is expected to exert a hydrostatic pressure equal to $2f/t$ [18]. Therefore, if the cylindrical island is of critical size with thickness t_0 and radius r_0 at which the island becomes firmly attached to the substrate, any further growth beyond the critical dimensions will generate a biaxial stress that can be expressed as

$$\sigma = (f_1 + f_2)\left(\frac{1}{t} - \frac{1}{t_0}\right) + \beta f_3\left(\frac{1}{r} - \frac{1}{r_0}\right) \tag{4-11}$$

where f_1, f_2, and f_3 are isotropic surface stresses associated with the top (free surface), interfacial surface between the bottom and the substrate, and the curved surface (perimeter) of the cylindrical island, respectively [19]. $\beta = (1-3\nu)/(1-\nu)$ for an elastically isotropic material, where ν is Poisson's ratio. It should be noted that the resulting stress was assumed to be a volume-averaged stress that is uniform throughout the cylinder, which is valid only when the cylindrical island has restricted geometries such that the radius is much greater than the thickness. When this assumption is applied to the above equation, the contribution from the second term on the right side of the equation is relatively small and thus negligible. Moreover, if the final (target) thickness t is significantly larger than t_0 (which is generally valid in most cases), the above equation can be simplified to

$$\sigma_{t,0} = -(f_1 + f_2)/t_0 \tag{4-12}$$

Therefore, if the values of f_1, and f_2 are known, the intrinsic stress owing to surface stress effects can be estimated. It should be noted that, for solids, the surface stress f_{ij}, which is a 2×2 tensor defined such that the surface work required to elastically strain a unit

surface by $d\varepsilon_{ij}$ is $f_{ij}d\varepsilon_{ij}$, is different from the surface free energy γ, which is a scalar equal to the excess free energy per unit area due to the existence of a new surface [22]. The surface stress tensor, however, can be treated as isotropic and reduced to a scalar f for some crystallographic faces or interfaces with symmetries such as (111) faces, which is of threefold symmetry [23]. Generally, most of the surface stresses for surfaces of single component materials are positive and of the same order of magnitude as the surface free energy except for inert gas crystals [18]. Rather than experiments, theoretical calculations of surface stresses have been attempted using both first principles and atomistic potential calculations as the experimental measurement of surface stresses is not easy. Few reliable data sets are available on the surface stress or free energy of β-SiC. The only value in the recent literature is the surface free energy of β-SiC (111), which is reported to be 2.180 N/m [24]. As for the interfacial stress or energy, the (0001) faces of 6H-SiC are reported to have an interfacial energy with silicon of the order of 1 N/m at 1750 °C [25]. However, the (111) faces of β-SiC have the same atomic configuration as the (0001) faces of 6H-SiC such that the stacking sequences of β-SiC and 6H-SiC are the same down to at least four layers from the surface. Moreover, the low energy electron diffraction (LEED) patterns for the two polytypes of SiC are reported to be essentially identical, which suggests that the data on the energy of interface between 6H-SiC (0001) and silicon may be used for β-SiC (111) [26]. Based on the above statements, if $f_1 + f_2$ is assumed to be of the order of ~3 N/m, Equation 4-12 would yield a compressive stress of 300 MPa for SiC films of critical thickness of ~10 nm. This order-of-magnitude calculation is in good agreement with the compressive intrinsic stresses ranging from 200 to 300 MPa in Figures 4-5 and 4-7.

4.3.2.3 *Qualitative explanation of compressive stress variation with CVD parameters*

Bearing in mind that the compressive stress owing to the surface stress effect is determined by the critical thickness of thin films at coalescence, consideration is now given to the variation of the critical thickness t_0 with deposition H_2/MTS ratio, deposition temperature, and the amount of HCl added to the source gas stream. It would be

reasonable to assume that growing islands first become constrained when the islands reach a size sufficiently large for grain coalescence to occur and substantial impingement starts [18]. A simple analysis has previously been performed by Thompson regarding the dependence of the grain size or film thickness at impingement on the deposition rate R and deposition temperature T [27]. The grain size at impingement is determined by the relative magnitudes of the growth rate G and nucleation rate I, and the width of diffusion zone δ (i.e., nucleation depletion zone). The diffusion zone δ is defined such that all adatoms arriving within a distance δ of an existing stable island attach to the island rather than desorb or become involved in any other nucleation process. Both G and I are proportional to the deposition rate R, and δ is determined by the surface diffusivity and the residence time of adatoms. In the case of a relatively low deposition rate R, the grain size at coalescence increases with decreasing R, while it is independent of R for higher R values, which can be expected from considerations of a rate-determining process in general nucleation theories. Under the CVD conditions that were used for the current SiC study, the deposition rate is relatively low. Therefore, an increase in H_2/MTS ratio (i.e., a decrease in concentration of carbon and silicon in the gas phase) will decrease the SiC deposition rate R, which in turn, increases the grain size at impingement at constant temperature [28]. This is in good agreement with the observation of a decrease in compressive stress (owing to the increase in t_0) with increasing H_2/MTS ratio as shown in Figure 4-2. However, when the deposition rate R is very low (at very high H_2/MTS ratio), the grain size may start to decrease with decreasing R since the growth rate G could significantly diminish. This could be a possible explanation for the increase of compressive stress (decrease in grain-size-at-impingement) at a H_2/MTS ratio of approximately 9 in Figure 4-2.

The variation of compressive stress with deposition temperature can also be explained in a similar manner. The grain-size-at-impingement is a strong function of deposition temperature due to the exponential dependence of Boltzmann distributions. In general, as deposition temperature increases, growth rate G also increases due to the diffusion zone δ increasing with temperature, while nucleation rate I decreases since the

supersaturation required to achieve a critical cluster size goes down as temperature goes up. The temperature effects on the grain-size-at-impingement are determined by the relative magnitudes of the activation energy for surface diffusion and adatom desorption energy, and the dissociation energy of a cluster of critical size [27]. Considering the fact that the grain size is strongly dependent on the adatom mobility, and an increase in temperature increases adatom mobility, the grain-size-at-impingement is expected to increase with increasing deposition temperature in general. In most cases, the desoprtion energy is higher than the surface diffusion energy since desoprtion requires adatoms to break bonds, and thus, the adatom diffusion distance δ is determined only by the surface diffusivity Therefore, over the temperature range studied in this work, the compressive stress due to the surface stress effect decreases with increasing deposition temperature since the increase in temperature results in greater grain-size-at-impingement or t_0 values, which is observed in Figure 4-3. However, at very high temperatures, adatoms may obtain an activation energy sufficient for desorption, which could result in a decrease in grain size. This could be an explanation for the increase in compressive stress (decrease in grain-size-at-impingement) around 1050 °C in Figure 4-3.

The strong dependence of compressive stress in CVD SiC on the addition of HCl can be explained by the site-blocking effect of HCl. HCl has been known to inhibit CVD SiC and decrease the growth rate significantly by a site-blocking mechanism such that dissociated Cl covers and blocks available deposition sites for SiC on the substrate surface [29]. Therefore, the addition of HCl into the source H_2-MTS gas stream is expected to decrease significantly the available deposition sites for Si or C atoms. At very high HCl fluxes and at relatively low deposition temperatures, the substrate surface could even be completely covered with Cl. The strong site-blocking effect of HCl will decrease the surface mobility, and thus the SiC growth rate significantly. HCl can even constrain and inhibit pre-existing SiC islands from adjusting to their equilibrium lattice spacing, which would lead to the generation of high residual stresses. However, as the HCl flux decreases or the temperature increases, the site-blocking effect would diminish, and thus, the growth rate will increase owing to the increased rate of HCl desorption

which provides the Si or C atoms with a higher probability of finding available sites for deposition. The very strong effect of the addition of HCl on the compressive intrinsic stress is evident in Figure 4-4, where a very high compressive intrinsic stress of the order of 1.5 GPa was observed for a large amount of HCl. Compressive intrinsic stresses of such a high level could not be obtained within the range of parameters examined for either gas ratios or deposition temperatures.

4.3.2.4 Tensile stress development due to grain coalescence

As was first recognized by Hoffman, during a thin film growth following the Volmer-Weber growth mode, adjacent islands with parallel vertical surfaces (i.e., one-dimensional) elastically snap together and form grain boundaries as they grow to reach some critical gap size [30]. This is a thermodynamically favorable process as the reduction of surface energy is greater than the increase of elastic energy. To improve the simple island geometry used in Hoffman's model, Nix and Clemens proposed a more sophisticated two-dimensional model treating grain boundary formation based on the Griffith's criterion for crack propagation which has been used in fracture mechanics [20]. A more realistic model for the island geometries upon coalescence has recently been considered by Freund and Chason as an approach to obtain a general equation describing a volume-averaged stress developing in an island model of dimensionality ranging from one to three [21]. For the case of a two-dimensional array of identical disk-shaped islands, the volume-averaged stress induced by grain coalescence is

$$\sigma_{ave} = 0.44 \frac{E^{1/3} \gamma^{2/3}}{R^{2/3}} \tag{4-13}$$

where γ is the difference between the surface and half the grain boundary energy (i.e., $\gamma = \gamma_s - \gamma_{GB}/2$), E is the elastic modulus of the material, and R is the radius of identical disk-shaped islands. It should be noted that $\gamma_s > \gamma_{GB}/2$ is a necessary condition for the grain coalescence to occur, and thus, the above equation will result in a tensile stress upon

coalescence. For CVD SiC, if reasonable values are assumed for the elastic modulus E = 420 GPa, interfacial energy difference γ = 1 J/m^2, and for the radius of cylindrical islands upon impingement R = 100 - 200 nm, the above equation predicts an average tensile stress of the order of magnitude 100 - 150 MPa.

4.3.2.5 *Discussion of the relaxation process during further growth*

The net residual stress predicted by summing up the two stress contributions in CVD SiC films (i.e., compressive + tensile stress) is in good agreement with the experimental results. However, the predicted stress levels should be viewed as upper limit values both for the compressive and tensile stresses calculated using the surface stress model and the grain coalescence based on the elastic contact of solids, respectively. In other words, there exist several mechanisms that are expected to lead to stress relaxation during further growth after grain coalescence, which includes diffusion or preferential incorporation of atoms into grain boundaries as suggested by Nix and Clemens [20]. Such processes associated with grain boundaries exert a relaxation effect not only on the tensile stress component from coalescence but also on the compressive stress component since they are surface-energy-driven mechanisms involving the generation or elimination of surfaces. Therefore, any processes that decrease the tensile stress contribution from grain coalescence are expected to decrease the compressive stress contribution from the surface stress mechanism as well [19]. However, under the circumstances in which the assumption of the present study is valid; that the radius of the cylindrical islands is much larger than the thickness (i.e., the fraction of interfacial areas for grain boundary formation is small), the relaxation processes at grain boundaries would not result in considerable relaxation of the tensile and compressive stresses during growth after coalescence. Furthermore, the strong tendency toward an epitaxy-like growth mode of CVD SiC in certain preferential directions, which is evidenced by the columnar SiC structures, is also unlikely to affect the stress states significantly. Thus, once the residual stress state of CVD SiC is determined upon coalescence, it is expected to be maintained without significant changes during further growth [20, 31].

4.4 Another approach to tackle residual stress – SiC/SiN_x layers

There have been efforts reported to develop MEMS materials composed of alternating tensile and compressive layers that can display a very low-level of residual stress. For instance, it has been demonstrated by Yang et al., that LPCVD polysilicon films composed of alternating tensile and compressive layers can display a near-zero residual stress and gradient, if their microstructures and relative thicknesses are properly controlled [14]. With the same aim of producing locally stress-balanced wafers, a layered silicon carbide-silicon nitride coating has been studied in parallel with the homogeneous CVD SiC coatings [6].

Silicon nitride (SiN_x) can be deposited on SiC layers by cyclic gas switching during the CVD process. By interrupting continuous deposition of SiC with the addition of ammonia gas to the process gas stream, SiC/SiN_x layered material was deposited on Si substrates. A TEM image of the SiC/SiN_x coatings is shown in Figure 4-13.

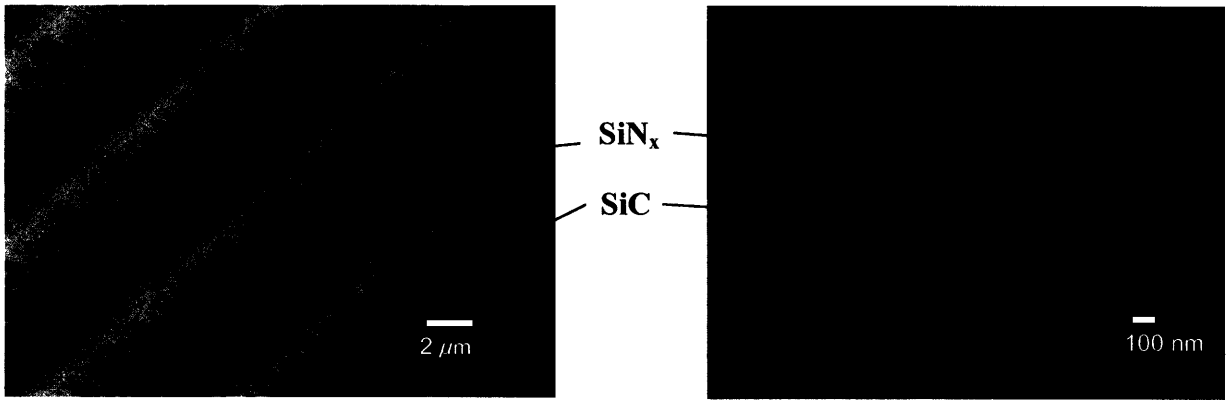


Figure 4-13 (a) TEM image of SiC/SiN_x layered material. (b) A higher magnification image of SiC/SiN_x layered material.

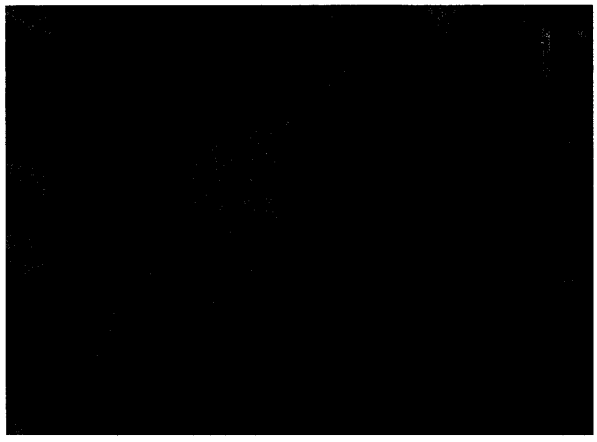


Figure 4-14 TEM image showing that the SiN_x interrupter layers deposited on SiC layers have amorphous structures [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

The interrupter SiN_x layers were observed to have amorphous microstructures as shown in Figure 4-14. The amorphous SiN_x layers deposited on SiC layers always displayed tensile stresses. Therefore, a desirable material displaying near-zero stress or stress gradients, should be able to be produced by controlling the residual stress states in the SiC/SiN_x coatings such that the residual stresses between SiC layers under residual compression and interrupter SiN_x layers under residual tension, balance to 'net-zero' over a very small thickness range. The 4-inch, 525 μm thick Si wafer coated with the SiC/SiN_x layered material was observed to have a large radius of curvature greater than 100 m, which implies that the total residual stress of the wafer is very small.

4.5 References

1. C. M. Su et al., "Stresses in chemical vapor deposited epitaxial 3C-SiC membranes," J. Appl. Phys., Vol. 77, No. 3, p. 1280-1283, 1995.
2. R. W. Hoffman, "The Mechanical Properties of Thin Condensed Films," Physics of Thin Films, Vol. 3, p. 211, Academic Press, New York, 1966.
3. M. F. Doerner and W. D. Nix, CRC Crit. Rev. Solid State Mater. Sci. 14, p. 225, 1988.
4. G. G. Stoney, "The tension of metallic films deposited by electrolysis," Proc. Roy. Soc. London A82, p. 172-175, 1909.
5. L. B. Freund et al., "Extensions of the Stoney formula for substrate curvature to configurations with thin substrates or large deformations," Appl. Phys. Lett., Vol. 74, No. 14, p. 1987-1989, 1999.
6. D. Choi et al., "Process development of silicon-silicon carbide hybrid micro-engine structures," Mat. Res. Soc. Symp. Proc., Vol. 687, p. 197, Fall 2001.
7. R. M. Jones, Mechanics of composite materials, Scripta Book Co., Washington, D.C., 1975.
8. J. A. Floro et al., "Physical origins of intrinsic stresses in Volmer-Weber thin films," MRS bulletin, Vol. 27, No.1, p. 19-25, 2002.
9. E. Hurtós and J. Rodríguez-Viejo, "Residual Stress and Texture in Poly-SiC Films Grown by Low-Pressure Organometallic Chemical-Vapor Deposition," J. Appl. Phys., Vol. 87, No. 4, p. 1748-1758, 2000.
10. E. S. Machlin, Materials Science in Microelectronics: The Relationships Between Thin Film Processing and Structure, Giro Press, New York, 1995.
11. S. P. Kim et al., "Effect of water absorption on the residual stress in fluorinated silicon-oxide thin films fabricated by electron-cyclotron-resonance plasma-enhanced chemical-vapor deposition," Appl. Phys. Lett., Vol. 79, No. 2, p. 185-187, 2001.
12. D. Winau et al., "The influence of oxygen on intrinsic stress and growth of iron and nickel films," Appl. Phys. Lett., Vol. 59, No. 9, p. 1072-1074, 1991.
13. D. Maier-Schneider et al, "Elastic properties and microstructure of LPCVD polysilicon films," J. Micromech. Microeng., Vol. 6, p. 436-446, 1996.
14. Yang, et al., "A New Technique for Producing Large-Area As-Deposited Zero-Stress LPCVD Polysilicon Films: The MultiPoly Process," J. Microelectromech. Syst., Vol. 9, No. 4, p. 485-494, 2000.
15. W. E. Wagner et al., "Contamination of Si devices by SiC," Silicon Carbide and Related Materials, Vol. 142, Nakashima et al. Eds. Bristol, UK: IOP Publishing, p. 1107-1110, 1996.
16. M. Garshasb, "Chemical Vapor Deposition of SiC: Thermodynamic Calculation and Compositional Characterization," International Conference on Metallurgical Coatings and Thin Films, 1991.
17. C. C. Chiu et al., "Low pressure chemical vapor deposition of β-SiC on Si(100) using MTS in a hot wall reactor," J. Mate. Res., Vol. 8, No. 10, p. 2617-2626, 1993.
18. R. C. Cammarata, "Surface and interface stress effects in thin films," Progress in Surface Science, Vol. 46, No. 1, p. 1-38, 1994.
19. R. C. Cammarata et al., "Surface stress model for intrinsic stresses in thin films," J. Mater. Res., Vol. 15, No. 11, p. 2468-2474, 2000.

20. W. D. Nix and B. M. Clemens, "Crystallite coalescence: A mechanism for intrinsic tensile stresses in thin films," J. Mater. Res., Vol. 14, No. 8, p. 3467-3473, 1999.
21. L. B. Freund and E. Chason, "Model for stress generated upon contact of neighboring islands on the surface of a substrate," J. Appl. Phys., Vol. 89, No. 9, p. 4866-4873, 2001.
22. F. Spaepen, "Substrate curvature resulting from the capillary forces of a liquid drop," J. Mech. Phys. Solids, Vol. 44, No. 5, p. 675-681, 1996.
23. A. L. Shull and F. Spaepen, "Measurement of stress during vapor deposition of copper and silver thin films and multilayers," J. Appl. Phys. Vol. 80, No. 11, p. 6243-6256, 1996.
24. T. Takai et al., "Reconstruction and energetics for surface of silicon, diamond and β-SiC," Surface Science, Vol. 164, p. 341-352, 1985.
25. M. Syväjärvi et al., "Interfacial properties in liquid phase growth of SiC," J. Electrochem. Soc., 146 (4), 1565-1569, 1999.
26. R. Kaplan, "Surface structure and composition of β- and 6H-SiC," Surface Science, Vol. 215, p. 111-134, 1989.
27. C. V. Thompson, "On the grain size and coalescence stress resulting from nucleation and growth processes during formation of polycrystalline thin films," J. Mater. Res., Vol. 14, No. 7, p. 3164-3168, 1999.
28. J. R. Weiss and R. J. Diefendorf, "Chemically Vapor Deposited SiC for High Temperature and Structural Applications," Silicon Carbide-1973, p. 80-91, Proceedings of the 3rd International Conference on Silicon Carbide, Miami, Florida, 1973.
29. M. T. Schulberg et al., "The interaction of HCl with polycrystalline β-SiC: Evidence for a site-blocking mechanism for HCl inhibition of SiC CVD," Mat. Res. Soc. Symp. Proc. Vol. 410, p. 471-476, 1996.
30. R. W. Hoffman, "Stresses in thin films: the relevance of grain boundaries and impurities," Thin Solid Films, Vol. 34, No. 2, p. 185-190, 1976.
31. F. Spaepen, "Interfaces and stresses in thin films," Acta mater., Vol. 48, p. 31-42, 2000.

CHAPTER 5

PLANARIZATION AND WAFER BONDING PROCESSES OF CVD SILICON CARBIDE

Planarization / polishing of SiC on Si substrates is required to remove excess CVD SiC coating deposited on areas other than those (etched patterns or trenches) designated for reinforcement. The polished SiC surface is then contacted to another Si wafer at room temperature, followed by a high temperature anneal to form a strong, permanent wafer bond. The bonded wafer pair is subsequently etched to form a hybrid turbine-compressor spool containing SiC reinforcement at the center of the turbine; the two wafers of the bonded pair correspond to the third and fourth wafer in the six-wafer stack assembly of the microengine, shown in Figure 1-2. However, both planarization and wafer bonding processes involving SiC present significant technical challenges, mostly due to the physical and chemical nature of SiC. This chapter describes the efforts made to planarize CVD SiC and to achieve wafer bonding between the planarized SiC and Si wafers, followed by difficulties encountered and lessons learnt, along with technical approaches to improve both processes.

5.1 Planarization / Mechanical polishing of SiC

5.1.1 Difficulties in SiC polishing

The development of a wafer-level planarization / polishing process has been focused on achieving two primary goals: removing the excess CVD SiC uniformly from the entire

wafer as well as achieving high surface qualities sufficient for the subsequent wafer bonding process. It is also critical to avoid cracking of the coating or the wafer. However, polishing SiC at the wafer level has been identified as one of the greatest technical challenges towards achieving Si-SiC hybrid turbine structures. Initial attempts to polish Si/SiC wafers suffered from low yields due to cracking and large areas of high roughness that made bonding impossible.

5.1.1.1 Chemical mechanical polishing (CMP)

In an effort to identify a suitable process to achieve the goals, consideration was initially given to chemical mechanical polishing (CMP). In this process, the combined action of mechanical abrasion and chemical reaction has proved effective for the planarization of wafers by smoothing surfaces at high polishing rates for various materials employed in semiconductor devices such as silicon oxide, polycrystalline Si (poly-Si), and some metals including copper, tungsten, and aluminum. The removal mechanisms of CMP are complex, and different for each type of material being polished. The removal rate is also strongly dependent upon the process conditions such as material type, pressure, temperature, slurry particle size, slurry feed rate, rotational speed, and hardness of pad. While a comprehensive review of CMP processes for various materials is neither possible nor appropriate, a brief review of CMP for oxide and polycrystalline silicon (poly-Si), the two most popular non-metallic materials in CMP industry, will be helpful to provide some insights into the viability of SiC CMP. The section on CMP of silicon oxide is also relevant to the use of this material as an interlayer for bonding, as described in section 5.2.2.

Oxide CMP has been a main focus of the CMP process in the semiconductor industry, as the significant increase in the number of device levels in an interconnect technology requires a technique to planarize topographies produced when CVD (dielectric) oxide films are deposited onto etched polysilicon gate (interlevel dielectric or ILD) and metal patterns (intermetal dielectric or IMD). Thus, oxide CMP is already well established, and industry standards exist for both pad and slurry. The standard pad for ILD and IMD CMP has been the stacked pad of IC-1000/Suba-IV, with a hard polyurethane-pad (IC-

1000) on top of a soft-pad (Suba-IV). The stacked pad is designed such that the hard top-pad planarizes the topography while the soft-pad improves the within-wafer-non-uniformity (WIWNU) [1]. Slurries for oxide CMP are primarily composed of colloidal silica or fumed silica suspended in an alkaline solution such as KOH or NH_4OH, diluted with DI water. Colloidal silica is produced by the hydrolysis of sodium silicate, followed by an ion exchange to avoid the possibility of sodium contamination, while fumed silica is produced by oxidizing $SiCl_4$ at high temperature in a flame. The colloidal or fumed silica must be dispersed and blended into the final slurry without agglomeration, which can be achieved by controlling the pH properly. The typical pH and solid particle content of slurries for oxide CMP are 9.0 - 11.0, and 5 - 35 wt%, respectively [1]. A buffering agent is also added to the slurry to maintain the proper pH level throughout the slurry volume. Generally, the polishing rate of oxide can be enhanced by increasing the pH, concentration and size of the slurry particle. Nowadays, colloidal silica slurries find more extensive use in shallow trench isolation (STI), ILD, and polysilicon CMP processes than fumed silica slurries, due to its enhanced stability and lower tendency for particle agglomeration.

Poly-Si CMP has been developed for some IC fabrication applications, most of which are associated with STI structures. The non-planar topographies near the edges of STI structures are replicated even after poly-Si is deposited on them due to the conformality of CVD poly-Si deposition [1]. Such undulated poly-Si topographies can be effectively planarized by CMP. Although the pads and slurries used for poly-Si CMP are quite similar to those for oxide CMP, the slurries for poly-Si can be modified to have a high selectivity to oxide primarily by changing the pH. Yasseen et al. reported that a 15:1 selectivity of poly-Si to oxide was achieved using slurry of pH 14 [2].

Unlike oxide and poly-Si CMP, research on SiC CMP has seen few successes primarily due to the chemical inertness of SiC. To the author's knowledge, the only wet CMP process described in the literature is that reported by Zhou et al., who employed concentrated colloidal silica slurries of high pH values at elevated temperatures to improve the surface quality of Si-terminated (0001) faces of 6H or 4H-SiC samples [3].

Although reported to be effective in achieving low-defect surfaces, improvements still need to be made in several respects before Zhou et al.'s CMP process can be considered a practical and global planarization technique for SiC. All the SiC samples used in Zhou et al.'s CMP were commercially available single crystal substrates produced by sublimation techniques, and their sizes ranged from about 30 to 130 mm^2. This implies that the as-received SiC samples had already been treated by lapping and polishing processes, and thus, their surface quality was reasonably high with a root mean square (RMS) surface roughness of about 2 nm. The purpose of the CMP was to further improve the surface quality of the SiC samples before growing epitaxial layers of CVD SiC on them. A reduction in the RMS surface roughness from 2 nm to 0.5 nm was observed after the CMP using colloidal silica slurry of high alkalinity (pH > 10) at elevated temperatures higher than 55 °C. However, the maximum polish rate--even when using the aggressive slurry conditions to enhance chemical etching--was less than ~0.1 μm/hr, which is at least an order of magnitude lower than that of mechanical polishing using diamond paste or wet Cr_2O_3 of 1 μm grit. Therefore, CMP is not likely to be practical for the initial or intermediate stage of polishing of SiC, where the bulk SiC needs to be removed in a reasonable time. However, it may be useful in the final stages of SiC surface finishing.

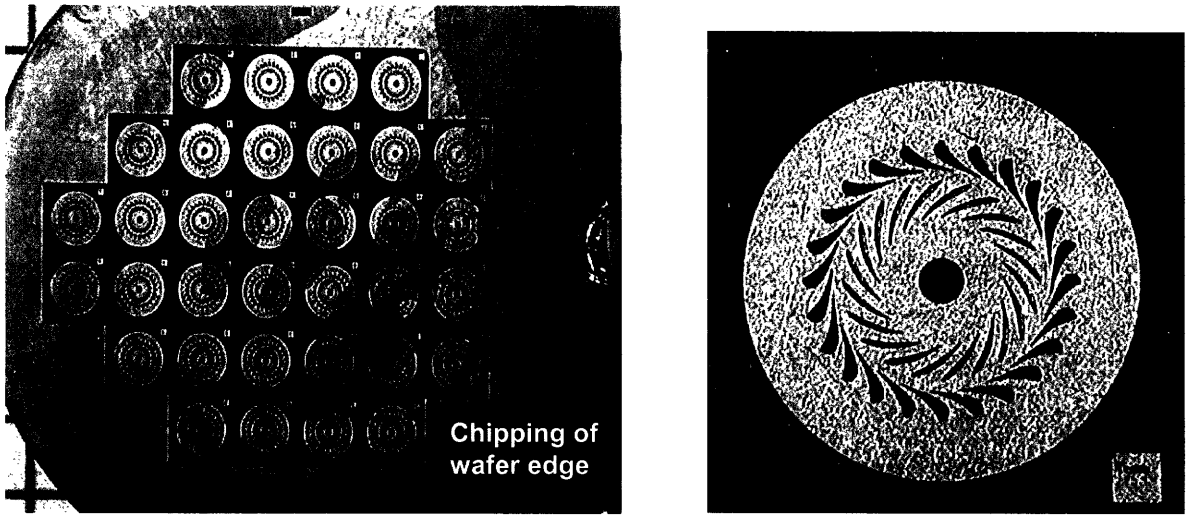
Another point to be noted is that no single etching mechanism is available for all polytypes of SiC. Zhou et al. speculated that an oxidation process caused by the highly alkaline slurry containing OH^-, plays a key role in the chemical etching of SiC CMP. This is similar to a removal process involving the oxidation of Si surfaces by OH^- groups and subsequent mechanical polishing actions leaving the surfaces H-terminated, suggested by Pietsch et al. to explain the CMP of (111) surfaces of Si using colloidal silica slurry [4]. That is, OH^- groups in the alkaline slurry weaken the Si-C bonds by inducing a dipole, as well as attacking the dangling bonds of Si atoms on the (0001) surfaces of 6H or 4H-SiC, allowing the formation of SiO_2 by the H_2O or oxygen in the slurry. However, it is unclear whether the proposed removal mechanism is applicable to either the carbon-terminated $(000\bar{1})$ faces of 6H and 4H-SiC or the surfaces of 3C-SiC; it may be possible that the identical mechanism is applicable to the (111) surfaces of 3C-SiC since they have the same atomic configuration as the (0001) faces of 6H-SiC as

mentioned in Chapter 4, but it is not clear what mechanisms, if any, operate on the other crystal planes. Considering the fact that SiC for the microengine is polycrystalline (with much rougher surface than single crystal) and thick (30 - 50 μm) 3C-SiC deposited on Si substrates of much greater size (~7850 mm^2) than SiC samples used by Zhou et al., it can be concluded that CMP is not a practical approach towards the fabrication of Si-SiC hybrid turbine structures.

5.1.1.2 Mechanical polishing – process of choice for Si-SiC hybrid structures

Due to the immaturity and impracticality of using a CMP technique for SiC as described above, the planarization process adopted in this research uses mechanical polishing with diamond grits, which provides a means of removing bulk SiC at reasonably high rates.

An initial wafer-level SiC planarization experiment was performed in collaboration with MIT Lincoln Laboratory for proof of concept purposes. A conventional mechanical lapping process using diamond paste of 5 - 10 μm grit size was employed to polish a 4-inch wafer with 36 individual dies bearing a turbine pattern, leaving SiC reinforcements in the ~30 μm deep trenches comprising arrays of stator and rotor blades. After 14 hours, the lapping process yielded the wafer shown in Figure 5-1 (a). A magnified view of one of the dies is shown in Figure 5-1 (b), in which the remaining SiC reinforcements filling the trenches appear in black. Although broadly successful in removing excess SiC, the experiment revealed technical difficulties involved in the mechanical planarization of a brittle material: wafer cracking and chipping of the edges. Many tiny cracks were found with the highest concentration around the Si-SiC interfaces, and the wafer edges, which were in direct contact with the mounting chuck of the polisher, were severely chipped. Moreover, the coarse diamond grit, which was used to achieve a high polish rate, resulted in a very rough surface with deep scratches all over the wafer area.



(a) (b)

Figure 5-1 (a) Planarized wafer with dies of turbine-shape. (b) Magnified view of an individual die on the planarized wafer.

5.1.2 Sources of wafer failures during planarization

More wafer-level planarization experiments were performed in conjunction with two vendors: Lapmaster International and Valley Design Corporation. Several SiC coated Si wafers have been sent to the vendors to take advantage of their commercial techniques for mechanical lapping and polishing. However, the initial efforts resulted in no success. All the wafers were found to crack severely during their planarization and wafer handling. Efforts were made accordingly to trace the primary sources of wafer cracking during the planarization process.

Several sources have been identified to be directly or indirectly responsible for the wafer failures during SiC planarization, the discussion of which is followed.

5.1.2.1 Residual stress in SiC coatings

As already mentioned in Chapter 4, residual stress control in SiC coatings is of critical importance to the wafer planarization for the following two reasons.

Wafer bow caused by the residual stress in SiC coatings have been found to be the most important reason for wafer failures in the early stage of the polishing process. Although experiments (documented in Chapter 4) have demonstrated the possibility to control the net residual stress in SiC coatings on Si wafers within the range of tens of MPa, which is very low considering the biaxial modulus of SiC is ~530 GPa, it was found that the wafers' radius of curvature corresponding to such levels of residual stresses is not sufficiently large (i.e., the wafer surface is not sufficiently flat) for a reliable planarization. Most conventional polishing machines adopt vacuum-type wafer chucks on which flat wafer surfaces are designed to be placed to firmly hold them during the polishing. For 4-inch wafers, it has been found from experience that wafer flatness with a radius of curvature greater than ~80 m is desirable for a stable polishing process without causing problems associated with the vacuum-holding such as wafer blowout or cracking due to vibrations. However, even the Si wafers with SiC coatings deposited under conditions for low residual stresses of several tens of MPa, are unable to meet the desired wafer flatness. For instance, a premium-grade, 4-inch Si wafer (~525 μm thick) coated with 30 μm thick SiC, with a net residual stress of ± 30 MPa (which is tensile or compressive depending on the sign of the radius of curvature), has a radius of curvature of ~10 m, which is much smaller than desired. A wafer bow or curvature of such a large magnitude turned out to be intolerable. Many wafers sent to the vendors for planarization were broken either when they were forced down to the vacuum chuck for tight contact between the wafers and the vacuum fixtures or when the fixed wafers were initially brought into contact with the rotating polishing (diamond) pads.

Another aspect of the residual stress in SiC coatings is that the net residual stress state becomes increasingly tensile as the polishing process reduces the SiC thickness. This happens because only the thermal stress component--which is always tensile--increases as the SiC thickness decreases, while the intrinsic component stays the same. This observation has already been presented in Figure 4-5, which shows that the residual

stress in a SiC coating of initial thickness of ~50 μm can be increased (to become more tensile) by more than 200 MPa when its thickness is reduced to several μm in the final stages of the polishing process. The likelihood of wafer failure during mechanical planarization increases as the state of residual stress in the SiC coating becomes more tensile, since crack propagation is much easier under tensile stress than compressive stress.

In summary, the residual stress in SiC coatings acts as a primary source of wafer failures throughout the polishing process from the initial stages by causing the wafer to bow, to the later stages by gradually changing the state of residual stress towards states of higher tensile stress.

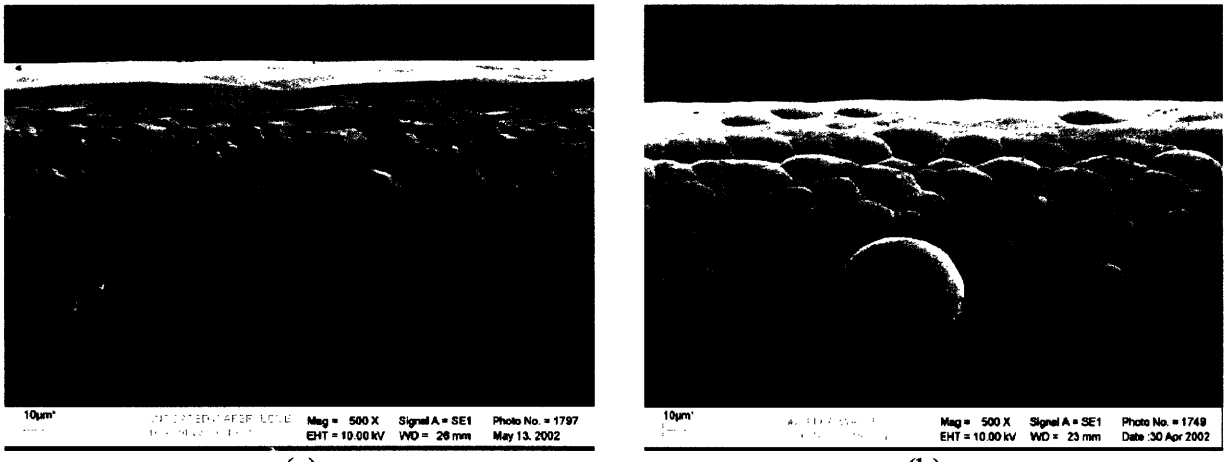
5.1.2.2 *Thickness gradient of SiC coatings*

Besides the wafer bow caused by the residual stress, the radial profile of the SiC coating itself makes the planarization very challenging. As shown in Figure 3-10, the thickness of SiC coating near the wafer perimeter can be greater by more than 20 % of that near the center of the wafer even when deposited using advanced wafer fixtures. Such a thickness gradient can alter the residual stress state of the wafer or even make the wafer locally wavy, which can trigger cracking when excessive downward forces are concentrated on the prominent areas of the wavy wafer. Another serious problem associated with the U-shape profile is that substantially more SiC must be removed from the periphery of the wafer. Although the patterns or trenches for SiC reinforcements are generally designed such that they are not located very close to the edges of the wafer, some of the patterns will lose significant amounts of SiC reinforcements by over-polishing, which is inevitable in order to ensure that the unwanted SiC is completely removed over all regions of the wafer.

5.1.2.3 *Rough SiC coatings on wafer edges – large nodules*

Many wafers have been found to start cracking at the edges in the early stage of planarization. To find the reason for the weakness of wafer edges, the microstructures of

the Si wafer edges were investigated using SEM before and after CVD SiC deposition. In general, the surface quality of as-received (from vendors) Si wafers was observed to be much lower at the edges than other areas. This was found to be true even for premium microelectronics-grade Si wafers, and this is thought to be quite systematic in terms of manufacturing; the Si wafer edges with lower surface quality would not cause a problem in most applications where devices are not placed close to the wafer edges unless the wafer needs to be planarized after the deposition of a thick film.



(a) (b)

Figure 5-2 (a) SEM image of the rough edge of an as-received Si wafer. (b) SEM image of the CVD SiC coated on the rough Si edge, which contains an abnormally grown large nodule [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

Figure 5.2 (a) shows an SEM image of the edge surface of an as-received Si wafer before SiC deposition, in which the surface appears quite rough. The initial roughness of the Si edge surface is much more pronounced when the Si wafer is coated with SiC. Figure 5.2 (b) shows the significantly rougher surface of the SiC that was deposited on the rough Si edge, where a large nodule was found to have grown in the middle of the SiC coating. The resulting rough surfaces significantly weaken the strength of the SiC coatings, and thus can trigger wafer cracking or chipping of edges. Furthermore, the

nodule, which is presumably a large single-grain that grew abnormally, can aggravate the surface quality by inducing serious defects if uprooted during planarization.

5.1.3 Approaches to improve SiC polishing process

5.1.3.1 SiC deposition on both Si faces

Efforts were made to minimize the detrimental effects of residual stress. However, as mentioned above, it has been found that it was practically impossible to obtain wafer flatness desirable for planarization if the wafer has a 30 - 50 μm thick SiC coating on its front face only, even when the CVD conditions for low residual stress are used. This suggests that SiC must be deposited on both faces of a Si wafer to guarantee wafer flatness with a radius of curvature greater than ~30 m, which was found to be a marginal value for a successful planarization, if it is performed with great care throughout the whole process. Therefore, all the wafers to be planarized must have SiC coatings on both faces to obtain minimum achievable wafer flatness by balancing the residual stresses between the front and backside.

5.1.3.2 CVD process using modified wafer fixtures

In order to reduce the wafer cracking originating from wafer edges, modifications can be made to the wafer fixtures used for SiC CVD, as mentioned in Chapter 3. The use of the modified wafer fixtures with rims surrounding the wafer periphery can significantly reduce the SiC thickness variation near the wafer perimeters, which helps reduce wafer failures near the wafer edges early in planarization. In addition to the reduction of coating thickness, such an approach was shown to be effective in improving the surface quality of SiC on the wafer edges by eliminating nodules completely or suppressing their excessive growth as shown in Figure 5-3. The surface of SiC deposited on the wafer edge using the modified fixtures (Figure 5-3) appears more similar to the initial edge surface of the as-received Si (Figure 5-2 (a)) than the SiC coating with large nodules (Figure 5-2 (b)).

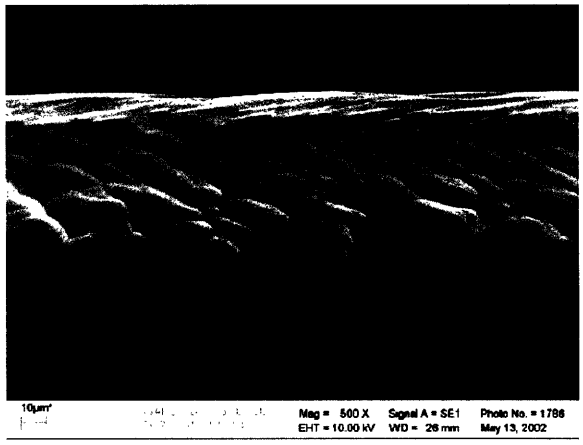


Figure 5-3 SEM image of the wafer edge coated with SiC using the modified wafer fixtures, in which no abnormally grown large nodule is found [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

5.1.3.3 Turning over wafers during planarization

SiC planarization experiments more recently conducted in collaboration with MIT Lincoln Laboratory have been found to be effective in polishing SiC without cracking. As in the earlier study, the planarization was performed using a conventional mechanical polishing method, but instead of a vacuum chuck, the wafer was attached to a polishing chuck made of cast iron using a quartz wax adhesive, which can be applied by heating it up with the iron chuck. When cooled down, the quartz wax has sufficient strength to support a wafer during the polishing as well as the capability of filling the small gaps between the polishing chuck and the wafer with insufficient flatness, which can easily lead to cracking if the wafer is held by a vacuum chuck. The rotational speed of the polishing wheel was 40 rpm, and the wafer was also rotated at 18 rpm. Both of them rotated counterclockwise while the wafer slowly moved back and forth from the center of the polishing wheel with a 17 mm amplitude.

The planarization result and the cross-sectional view of the wafer are presented in Figure 5-4. Most unwanted SiC coatings were successfully removed without cracking by mechanical polishing using a diamond paste of 3 μm grit size in 8 hours. The most

important feature of this experiment involves the frequent turning over of the wafer during the polishing to minimize the imbalance in residual stresses between the two faces of the wafer, which would arise as the SiC on one wafer face becomes thinner than that on the other face in a single-side polishing operation [5].

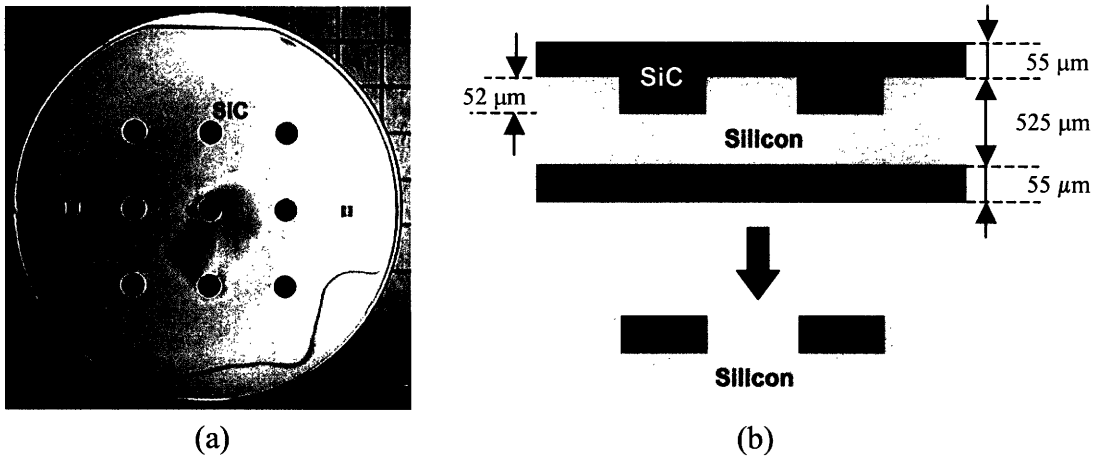


Figure 5-4 (a) Planarized Si wafer with SiC reinforcements. (b) Cross-sectional view of the SiC reinforcements deposited into circular trenches.

5.1.3.4 Si shadow masking - approach to minimize unwanted SiC deposition

The Si-SiC hybrid turbine structures concept aims to deposit SiC solely in the strategic (target) locations with the aim of increasing the strength and stiffness of the turbine-compressor spool at high operating temperatures. Unlike this concept, however, the current CVD process used by Hyper-Therm described in Chapter 2, has no capability of restricting the deposition of SiC coatings to the target areas that are pre-patterned in the silicon surfaces for reinforcement columns by deep reactive ion etching (DRIE). Therefore, the whole silicon wafer surface is covered with thick SiC layers during the CVD process, which results in a large amount of unwanted SiC coating covering the entire silicon surface. This is primarily due to the fact that no relevant masking material exists that is capable of withstanding high CVD temperatures ranging from 950 to 1300 °C. As the easiest approach to this problem, silicon wafers have been adopted as a

(shadow) masking material to verify the feasibility of selectively restricting the deposition of SiC to target areas. The silicon shadow mask is made by etching holes through the thickness using DRIE. The shadow masks have holes that are exactly matched with the trenches on the object silicon wafers such that source gases for CVD are allowed to flow only through the holes when precisely aligned. The concept of the CVD SiC deposition using silicon shadow masks is illustrated in Figure 5-5.

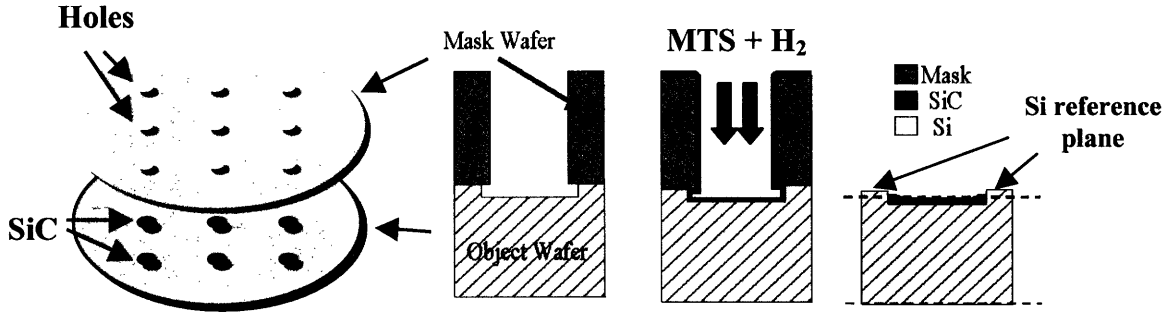


Figure 5-5 SiC deposition using Si shadow mask.

The primary advantage of depositing SiC using a shadow mask is that unwanted SiC deposition can be significantly minimized, which results in a much easier and faster SiC planarization process, thus leading to higher planarization yields. Another important aspect of the shadow masking approach for selective deposition is that the original silicon surface can still be preserved after CVD process as a reference plane for polishing. Without the reference plane, it is very difficult to decide when to stop the polishing process.

An intact wafer planarized following the shadow mask SiC deposition is illustrated in Figure 5-6, in which the SiC reinforcements deposited deep in the silicon surface appear as black circular patterns. This approach appears to have good potential for success.

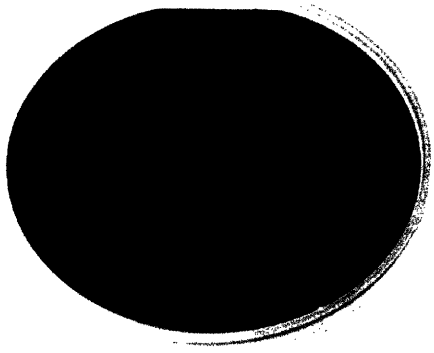


Figure 5-6 Successfully planarized silicon wafer containing SiC reinforcements. The SiC was deposited using a shadow mask approach.

5.1.4 Remaining problems

The polishing technique, however, still needs to be refined to improve surface finish, especially around the peripheries of circular target areas. For instance, discontinuous steps are very likely to remain on the borders between the SiC and Si due to differential polishing rates of the two materials with different stiffness and hardness. This phenomenon is called the 'dishing' effect. The dishing is abundant in several CMP processes, one example of which is the CMP of CVD oxide layers deposited to fill trenches for the fabrication of shallow trench isolation (STI) structures [1]. Various approaches have been proposed to reduce the dishing effect encountered during CMP processes, but they are not applicable to the mechanical polishing of stiff SiC. Therefore, more efforts must be made to improve polishing techniques in combination with wafer bonding techniques using interlayer materials to overcome the dishing effect since removing such steps is critical to achieving a complete SiC-to-Si wafer bonding.

Despite its advantages, the current shadow mask SiC deposition also needs to be modified to improve wafer alignment, which may result in a slightly more complex overall fabrication route. The shadow masks are not firmly bonded to object wafers, but

merely placed in the CVD chamber after being aligned and then slightly clamped together with the object wafers. This is done because it will be impossible to detach the mask wafers from the object wafers if the mask-object wafer pairs were covered with thick and continuous SiC coating during the CVD process. Ensuring a precise alignment immediately before the CVD process is critical to achieving the selective SiC deposition as intended since the slightest misalignment would result in a significant amount of excess SiC deposition around the target patterns, as demonstrated in Figure 5-7.

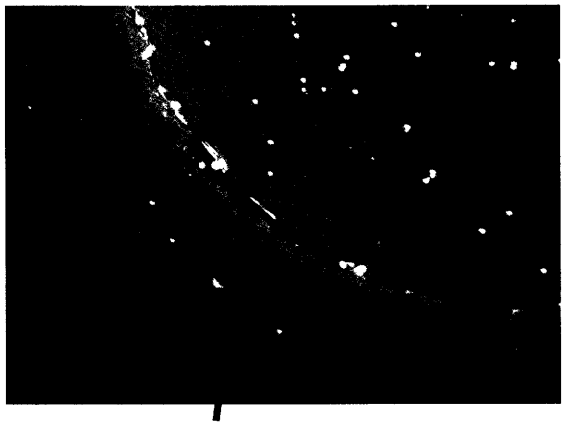
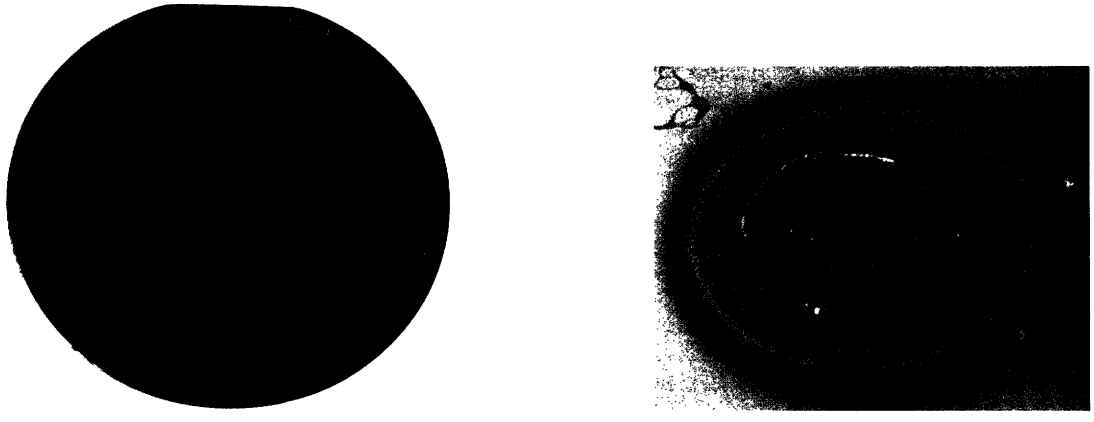


Figure 5-7 Unwanted SiC deposition caused by slight misalignment.



(a) (b)

Figure 5-8 (a) Gas bleeding through the gap between mask and object wafers. (b) Unwanted SiC deposition around the target 30 μm deep circular trench [Courtesy R. J. Shinavski, Hyper-Therm, Inc.].

Even when a precise and tight mask-object wafer contact is initially made, unwanted SiC deposition still occurs around target areas due to gas bleeding through the gap between the mask and object wafers. This gas bleeding through the gap is caused when either or both mask and object silicon wafers bend during the CVD process due to residual stresses. Unwanted excess SiC deposition around target areas due to the gas bleeding is shown in Figure 5-8, in which the rainbow-like patterns indicate that thin layers of SiC layers with thicknesses ranging from several μm to several tens of μm were deposited around the periphery of the object wafer.

The current shadow mask deposition is not an economical method since silicon shadow masks are not reusable due to the significant wafer bending caused by thick SiC coatings piling up during the CVD process. If shadow masks were made of some metallic materials with very high stiffness, it might be possible to use them repeatedly. However, more careful consideration is required since much wider gaps could develop between the mask and object wafer during the CVD process due to the large thermal mismatch between two different materials.

5.2 Si-SiC wafer bonding using CVD oxide as an interlayer material

For successful wafer bonding, all the wafer surfaces to be bonded must be sufficiently clean, flat, and smooth for intimate contact, which is critical for van der Waals attraction forces to act between atoms or molecules on the two surfaces. Van der Waals attractions are activated when electrically polarized atoms or molecules are attracted to each other, and diminish rapidly as the distance between two interacting atoms or molecules increases [6]. When two very smooth and clean Si wafer surfaces are brought into contact at room temperature, van der Waals attractions are activated and hydrogen bonds are formed between the wafer surfaces. These bonds are relatively weak, but still sufficient to hold the wafer pair together. The weak bonding strength can be

increased up to the (fracture) strength of the Si itself by a high temperature anneal. However, the strengthening by high temperature annealing occurs only when the intimate, short-ranged contact was already achieved between the two wafer surfaces at room temperature. Therefore, it is critical that defect-free wafer contact be achieved at room temperature for a complete wafer bonding, which is finalized by high temperature annealing.

However, neither as-deposited CVD SiC surfaces nor mechanically planarized SiC surfaces reach the degree of smoothness required for the atomic-level proximity to another Si surface. To render the rough SiC surface acceptable for bonding, silicon oxide has to be deposited on the SiC surfaces as a groove-filling material. Plasma enhanced chemical vapor deposition (PECVD) is used for this purpose. However, the surface qualities of CVD oxide deposited on rough SiC surfaces are quite low, and are still insufficient for direct wafer bonding. Therefore, oxide CMP must be performed before wafer contact is made at room temperature, followed by high temperature annealing. More detailed discussions of each process step necessary for Si-to-SiC wafer bonding are presented below.

5.2.1 Deposition of PECVD oxide on polished SiC surface

As noted above, for successful wafer bonding, it is essential to achieve a very high degree of surface smoothness before wafer contact at room temperature. For instance, it has been experimentally observed that the wafers should have a roughness of no greater than about ~10 Å for a successful Si-to-Si bonding [7]. In the case of SiC-to-Si wafer bonding, it has been reported by Tong et al. that 3C-SiC layers deposited on Si wafers by rapid thermal chemical vapor deposition (RTCVD) can be transferred onto thermal oxide surfaces grown on Si substrates by wafer bonding and etchback process if the SiC surface is oxidized [8]. In their study, 500 Å thick thermal oxide was grown on SiC at 1050 °C in dry oxygen environment, and the oxide on the SiC had a mean surface roughness of ~23 Å, which is significantly rougher than desired for good bonding. Although the

roughness was reported to be overcome by applying external forces for intimate wafer contact, significant fractions of bonded areas were eventually peeled off during the Si thinning process. This is a good example showing that achieving a good wafer contact at room temperature is of critical importance to the finial bonding strength.

In the current SiC process for the Si-SiC hybrid structures, it is not possible to achieve the desired level of surface smoothness for good wafer bonding by mechanical polishing using diamond grit. Moreover, SiC wafer bonding involving the thermal oxidation of SiC is not feasible, in view of the fact that the planarized SiC surface is much rougher than in Tong et al.'s case, and the thermal oxidation of SiC is extremely slow. To take advantage of the simplicity of the CVD process and the chemical similarity to that of the thermal oxide, CVD silicon oxide has been chosen as an interlayer material to fill the grooves of rough SiC surfaces with. Therefore, like Tong et al.'s approach, wafer bonding of the current SiC research is SiC/oxide-to-Si wafer bonding; the SiC coated with CVD silicon oxide will be termed as "SiC/oxide" for simplicity. Although non-stoichiometric, the chemistry of CVD oxide is similar to that of thermal oxide, and thus its mechanism of wafer bonding is expected to be very similar to that of well-established thermal oxide bonding, which is characterized by hydrophilic attractions between bonding surfaces.

Initial consideration was also given to the use of CVD polycrystalline silicon (poly-Si), which has been used as an interlayer material for Si-to-Ge wafer bonding [9]. However, CVD oxide was selected over CVD poly-Si for several reasons. First of all, CVD oxide, which is amorphous, has generally better coating uniformity and step coverage than poly-Si, which consists of many small grains. If deposited at temperatures below ~575 °C, poly-Si can also be amorphous, but recrystallization and grain growth always occur upon exposure to higher temperatures (~1000 °C) for annealing. Moreover, despite the recent advance of poly-Si CMP, surfaces of amorphous materials are always easier to smooth by CMP than polycrystalline materials containing a high density of grain boundaries.

Silane-based PECVD oxide was deposited on planarized SiC wafer surfaces using Concept One (Novellus Systems Inc., San Jose, CA), a five-station continuous plasma processing system. The source gases for PECVD oxide were SiH_4 (nominal gas flow rate of 300 sccm), N_2O (~9000 sccm), and N_2 (1500 sccm), and the deposition temperature was 400 °C. The plasma environment makes it possible to achieve a high deposition rate of ~1 μm/min even at the relatively low temperature, but it compromises the quality of the oxide due to the remnants of intermediate species, radicals, and gases such as H_2. Therefore, the quality of as-deposited PECVD oxide is much lower than that of thermal oxide in terms of both structural and electronic properties. Thus, the PECVD oxide film must be annealed at high temperatures (~1000 °C) for densification [10]. The densification is also necessary to prevent the wafer from bending during the high temperature anneal, which will be performed subsequently to wafer contact at room temperature. In the case when thick (≥ ~3 μm) oxide deposition is necessary, the oxide needs to be deposited on both wafer faces to prevent excessive wafer bowing upon high temperature anneal. The oxide thicknesses on both wafer faces can be engineered appropriately to prepare the wafer if the planarized wafer is not sufficiently flat for the bonding process. In any case, the oxide deposited on the backside can be easily removed by HF etching after the wafer bonding process is completed.

5.2.2 CMP of CVD oxide

After densification, chemical mechanical polishing (CMP) is performed on the oxide surface to render it sufficiently smooth for intimate contact with another Si wafer. Conversely, CMP may also be performed before the oxide densification. It has been observed that the oxide densification neither changes the surface roughness nor affects the subsequent CMP process significantly. The smoothness of the oxide surface after CMP is examined using atomic force microscope (AFM) before pre-bonding at room temperature.

For the current research, the oxide CMP was performed using a Strasbaugh GEC system (San Luis Obispo, CA) along with a hard polyurethane IC-1000 pad (Rodel Corporation, Newark, DE) and KOH-based Semi-Sperse® dielectric CMP slurry (Cabot Microelectronics, Aurora, IL) with a pH of 10.8 - 11.2, and particle content of 12 - 25 wt%. Typical process variables used were a downward force of 8.0 pounds per square inch (psi), back-pressing of 3.0 psi, a polishing pad speed of 30 rpm, a wafer carrier speed of 15 rpm, and a slurry flow rate of 150 ml/min, which provided an oxide polish rate of ~0.12 μm/min. About 0.05 - 0.2 μm of oxide was removed in the CMP process depending on the initial roughness of as-deposited CVD oxide surface.

After oxide CMP, the polished wafers were thoroughly rinsed with DI water to remove the slurry particles. However, the sudden pH drop due to the rinse causes the slurry particles to lose their zeta potential, which served to prevent them from agglomerating each other in alkaline solutions. This causes some of the particles to stick to the polished oxide surface, which is sufficiently strong that even vigorous DI water rinse is unable to remove them. Therefore, in an effort to remove any remaining particles attached to the wafer surfaces, the polished surfaces were subsequently rubbed with a hydrophilic polyvinyl alcohol (PVA) sponge brush. However, in order to remove such particles completely, it is preferable to use a cleaning solution with a high pH (> 7) such as dilute NH_4OH (1:50 with DI water), which helps the repulsive component of the force between particles and the oxide surface, making it easier to remove them [1].

5.2.3 Pre-bonding at room temperature followed by high temperature anneal

Following the oxide CMP, the oxide surface must be thoroughly cleaned with piranha (3:1 H_2SO_4:H_2O_2) several times. The oxide surface is then treated by standard RCA™ clean (without HF dip) along with Si wafers to make both the surfaces hydrophilic.

For hydrophilic surfaces, the interface energy is determined by the number of Si-OH (silanol) groups, thus the bonding energy can be increased by increasing the density of silanol groups. Through the RCA™ activation treatment, both native oxide-covered Si and thermally oxidized Si surfaces are saturated with a high density of silanol groups. Upon intimate contact at room temperature, the hydrogen bonds of hydroxyl groups and van der Waals forces cause the two wafer surfaces to stick together as shown in Figure 5-9 (a) [11]. The wafer bonding mechanism can be considered from a thermodynamics standpoint, which is essentially the same as the mechanism used to explain crack propagations in fracture mechanics. That is, for wafer bonding to occur at room temperature, the energy decrease due to the disappearance of two wafer surfaces must exceed the energy increase caused by the elastic deformation of wafers required for intimate surface contact [12]. Conversely, the debonding of a bonded wafer pair occurs when the energy decrease due to the release of stored elastic energy of deformed wafers exceeds the energy increase due to the generation of two new (wafer) surfaces.

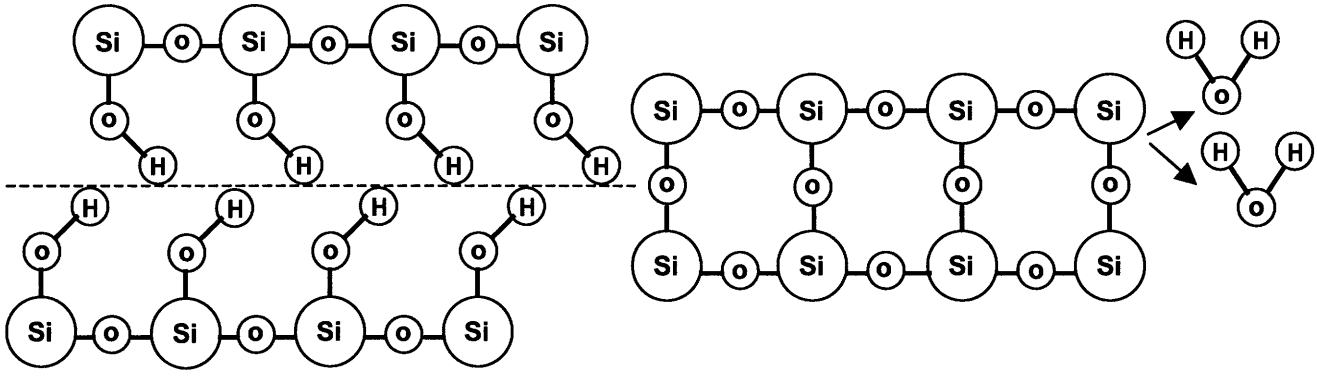


Figure 5-9 (a) Hydrogen bridges during wafer contact at room temperature. (b) Si-O-Si bonds formed after high temperature anneal [F. E. H. Tay (ed.), Materials & Process Integration for MEMS, Kluwer Academic Publishers, p. 135-156, 2002].

To increase the bonding strength to a maximum, the pre-bonded wafers are put in a furnace tube and annealed in a nitrogen environment. During the high temperature anneal, hydrogen diffuses out of the wafer surfaces and strong Si-O-Si bonds are formed across the bond interface as depicted in Figure 5-9 (b) [11].

For the current research, the CMPed oxide surfaces were piranha (3:1 H_2SO_4:H_2O_2) cleaned first. Both the oxide surface and the pair-Si wafer surfaces were subsequently treated by a standard RCA™ clean (without HF dip) to render surfaces clean and hydrophilic. The basic RCA™ clean involves two solutions: SC-1 (standard clean-1) and SC-2 (standard clean-2). SC-1 is designed to remove water-insoluble organic compounds and some metal contaminants such as Cu, Ag, Ni, Co, and Cd, while SC-2 serves to remove alkali and heavy metal contaminants such as Na, Al, Fe, Mg, Cu, Cr, Ni, W, Co, and Pb [6]. For all the wafers used for bonding, SC-1 clean was performed for 10 minutes using a solution of 5:1:1 H_2O:H_2O_2:NH_4OH at 75 - 80 °C. After the SC-1 clean, the wafers were thoroughly rinsed using deionized (DI) water, followed by SC-2 clean. In the case when thin native oxide layers on Si surfaces need to be removed, an HF dip can be performed using a solution of 50:1 H_2O:HF. However, for the current research, the HF dip was bypassed to avoid the etching of CVD oxide layers on the planarized wafer. SC-2 clean was then employed for 15 minutes using a solution of 6:1:1 H_2O:H_2O_2:HCl at 75 - 80 °C, which was immediately followed by DI water rinse, and spin-drying to finalize the cleaning procedure.

After drying, the wafer surfaces become hydrophilic with a high density of silanol groups as shown in Figure 5-9 (a). To avoid contamination, the wafer surfaces were immediately brought into contact for pre-bonding at room temperature using a wafer bonder, Electronic Visions™ AB1-PV (Electronic Visions Incorporation, Phoenix, AZ). The chamber was typically evacuated up to 5×10^{-2} mbar, and then the center of the wafer pair was forced down to initiate a bonding wave with a pressure ranging form 1000~2000 mbar over a period of ~10 minutes. After the chamber was vented to atmosphere, the pre-bonded wafer pair was taken into a furnace tube and then annealed in a 40 % N_2

environment at temperatures above 1000 °C. Typical annealing times should be at least one hour.

5.2.4 Problems in SiC/oxide-to-Si wafer bonding

In the case of the same PECVD oxide deposited on bare silicon surfaces, which has been prepared for comparison purposes, perfect wafer bonding (Silicon/oxide-to-Silicon) could be achieved whenever the root mean square (RMS) surface roughness (R_q) of the oxide was smaller than ~0.7 nm after CMP. However, even when the RMS surface roughness of oxide was smaller than 0.7 nm, no wafer bonding (SiC/oxide-to-Si) has been achieved in many cases of the CMPed oxide on SiC surface. Significant efforts were made to reveal the source of this problem.

In the case of thick SiC coatings, abnormally grown large SiC nodules protruding out of SiC surfaces have been identified to be the cause of the serious problem encountered during wafer bonding process. An example of such abnormally grown nodules is shown in Figure 5-10, in which the average thickness of SiC coating was 15 μm. Assuming that the nodule of Figure 5-10 has a hemispherical shape, the nodule is almost ~5 μm high, which implies that the thickness of CVD oxide must be greater than at least 5 μm in order to cover the entire rough SiC surface. Although the number of these nodules is quite small, only a few such big nodules could culminate in unsuccessful wafer bonding, even when most surface areas of the CVD oxide have RMS surface roughness smaller than ~0.7 nm. This can be understood from the deleterious effect of impurity particles on wafer bonding; for 4-inch, 525 μm thick Si wafers, even a very small particle of about 1 μm diameter can lead to a circularly unbonded area with a diameter of about 0.5 cm [6].

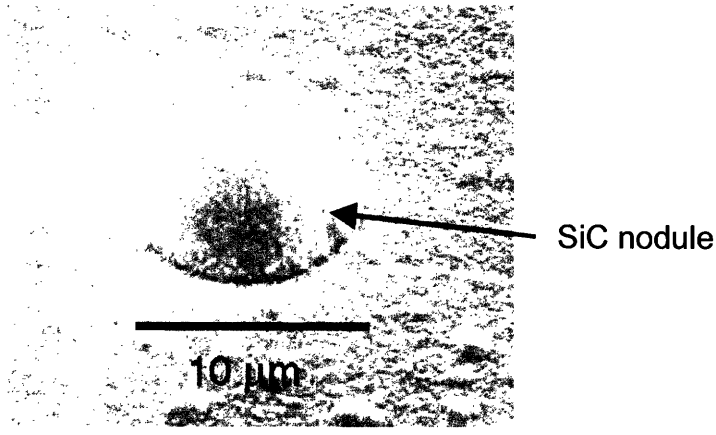


Figure 5-10 Abnormally grown large SiC nodule protruding out of 15 μm thick SiC coating.

In fact, the RMS roughness can only represent the quality of local surface areas since atomic force microscope (AFM) scanning provides information pertaining to a very limited surface area. One more important issue to note is that the large nodules can affect the CMP process significantly. Generally, CMP pads used for silicon oxide are very much conformable to any surface with hard particles, and thus it cannot actually polish the areas near the huge nodules. For this reason, the oxide surface of the areas near the nodules would not be smoothened even after CMP. This could explain why SiC/oxide-to-Si wafer bonding has been such a big challenge.

5.2.5 Si-SiC wafer bonding result and discussion

A result of SiC/oxide-to-Si wafer bonding is shown in Figure 5-11, in which a relatively thick CVD oxide layer (~2.5 μm) was deposited on a 2.5 μm thick SiC coating. The relatively thick oxide coating thickness was used to cover the entire SiC surface, which might have a small number of abnormally grown nodules. The wafer pair was annealed at 1000 °C following pre-bonding at room temperature. Although imperfect, most areas were successfully bonded. The unbonded regions in Figure 5-11 might be

attributed to dirt, debris of silicon or oxide, insufficient oxide CMP, and lack of wafer flatness.

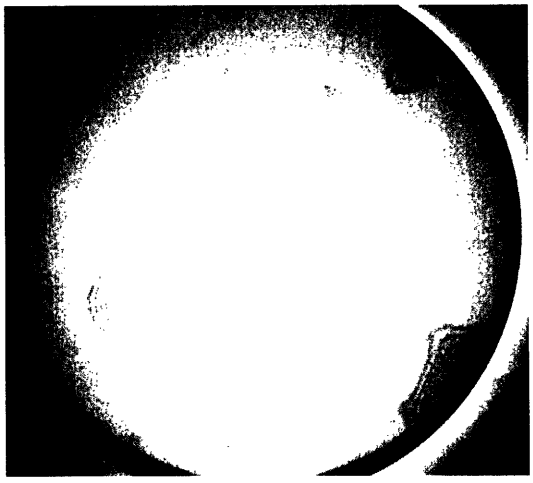


Figure 5-11 SiC-to-Si wafer bonding using CVD oxide as an interlayer material.

In the case of SiC/oxide-to-Si wafer bonding, the importance of wafer flatness is more pronounced than Si-to-Si wafer bonding due to the much higher stiffness of SiC than Si. That is, SiC is so stiff that it can easily regain its original shape or position when external forces are released.

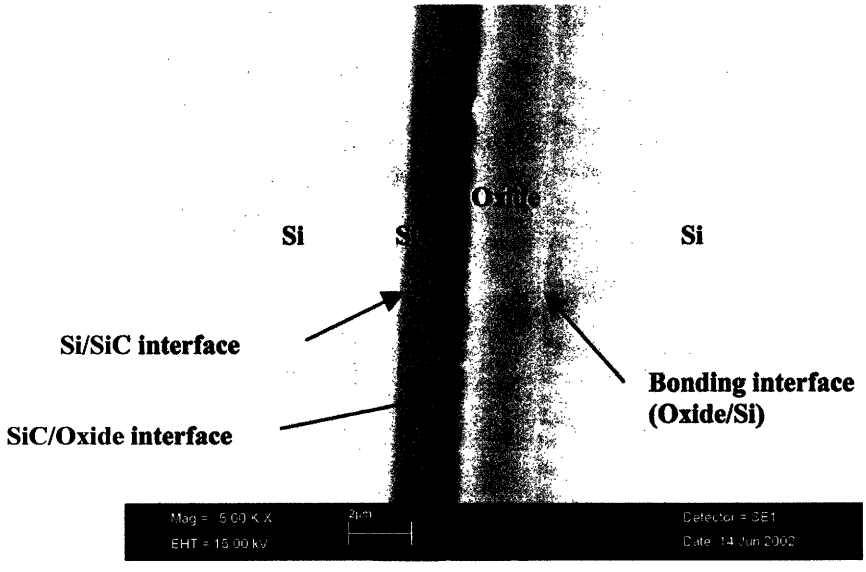


Figure 5-12 Cross-sectional image of SiC/oxide-to-Si wafer bonding.

A cross-sectional image of the bonded SiC/oxide-to-Si wafer pair is shown in Figure 5-12. In this scanning electron microscope (SEM) image, the SiC/oxide interface appears very rough while the oxide/Si bonding interface is smooth after oxide CMP. This picture is a clear evidence of the critical need for using oxide as a groove-filling material.

In general, the surface of as-deposited SiC becomes rougher as its thickness increases. Moreover, the rougher SiC surface has a higher probability of containing abnormally grown large nodules. Therefore, the thickness of CVD oxide layer relative to that of SiC is very important to successful SiC/oxide-to-Si wafer bonding. This is the explanation for the relatively thick oxide of Figure 5-12, which was designed to be about 2 μm so that its thickness is comparable to that of the SiC layer.

5.2.6 General approaches towards successful SiC/oxide-to-Si wafer bonding

SiC/oxide-to-Si wafer bonding is the highest technical risk. Therefore, a general procedure assuring successful SiC/oxide-to-Si wafer bonding is of great interest. Most of all, efforts have to be made to eliminate or suppress the growth of large nodules during the SiC deposition. The simplest way to suppress nodule growth is to keep the Si wafer surface clean and intact as much as possible. Any small contaminant particles and surface defects act as potential sites for abnormal growth of SiC nodules because they are energetically favorable for CVD SiC to grow. Thus, keeping the Si wafer surface clean is the first step to preventing the growth of large nodules.

Thicker SiC layers always have rougher coating surfaces and higher likelihood of containing large nodules than thinner SiC. In the case of thick SiC coatings (e.g., ~30 μm), a general approach to improve SiC/oxide-to-Si wafer bonding would be to deposit relatively thick (≥ ~5 μm) CVD oxide on the SiC coating to completely cover the rough surface, and then to increase the duration of oxide CMP. However, the mechanical

strength of silicon oxide at high temperatures is somewhat questionable. Thus, such a thick oxide layer may not be desirable from a structural integrity standpoint. In such cases, a better approach would be to polish the thick SiC surface to remove any large nodule-like structures and then to deposit CVD oxide of reasonable thickness on the polished SiC surface.

Upon the completion of the high temperature annealing step, attention has to be focused on the structural integrity of bonded SiC/oxide-to-Si wafer pairs, since questions still remain as to the strength of oxide and Si when they are exposed to the high operational temperature of microengines. Therefore, mechanical tests must be performed to identify the weakest parts in the Si-SiC hybrid structures, the discussion of which is the topic of Chapter 6.

5.3 References

1. S. Wolf, Silicon Processing for the VLSI era, Vol. 4. Deep-Submicron Process Technology, Lattice Press, 2002.
2. A. A. Yasseen et al., "Chemical-mechanical polishing for polysilicon surface micromachining," J. Electrochem. Soc., Vol. 144, No. 1, p. 237-242, 1997.
3. L. Zhou et al., "Chemomechanical Polishing of Silicon Carbide," J. Electrochem. Soc., Vol. 144, No. 6, p. L161-L163, 1997.
4. G. J. Pietsch et al., "Chemomechanical polishing of silicon: Surface termination and mechanism of removal," Appl. Phys. Lett., Vol. 64, No. 23, p. 3115-3117, 1994.
5. D. Choi, R. J. Shinavski, W. S. Steffier, S. Hoyt, S. M. Spearing, "Process Development of Silicon-Silicon Carbide Hybrid Micro-Engine Structures," Mat. Res. Soc. Symp. Proc., Vol. 687, p. 197, Fall 2001.
6. Q.-Y. Tong and U. Gösele, Semiconductor wafer bonding, John Wiley & Son, Inc., 1999.
7. M. A. Schmidt, "Wafer-to-Wafer Bonding for Microstructure Formation," Proceedings of the IEEE, Vol. 86, No. 8, p. 1575-1585, 1998.
8. Q.-Y. Tong et al., "Silicon carbide wafer bonding," J. Electrochem. Soc., Vol. 142, No. 1, p. 232-236, 1995.
9. C. G. Goetz, "Generalized reaction bonding," Proceedings of 1st International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, Vol. 92-97, p. 65. 1992.
10. X. Zhang et al., "Residual stress and fracture in thick tetraethylorthosilicate (TEOS) and silane-based PECVD oxide films," Sensors and Actuators A 91, p. 373-380, 2001.
11. F. E. H. Tay (ed.), Materials & Process Integration for MEMS, Kluwer Academic Publishers, p. 135-156, 2002.
12. S. M. Spearing et al., "Materials, Structures, and Packaging," The MIT Microengine Project, 2000 Annual Report, MIT Proprietary, Cambridge, MA, 2000.

CHAPTER 6

MECHANICAL TESTS OF BONDED SILICON-SILICON CARBIDE WAFERS

The mechanical integrity of Si-SiC hybrid turbine structures is largely determined by the bond quality of SiC/oxide-to-Si wafer pairs. Therefore, the bond strength of the SiC/oxide-to-Si wafer pairs is of crucial importance to the microengine's performance, particularly at high operational temperatures. The bond strength or toughness of the SiC/oxide-to-Si wafers has been examined using four-point flexure specimens. This chapter describes the four-point flexure tests of bonded Si-SiC wafers at both room and high temperatures as well as the efforts to identify the weakest link of the Si-SiC hybrid structures.

6.1 Measurement of bond strength

In accordance with increased number of semiconductor or MEMS devices fabricated by bonding multiple layers of wafers, many techniques have been developed to evaluate the bond strength of those structures. Among the various techniques, the discussion here is limited to some of the methods with wide applications and relevance to current research on bonded Si-SiC wafers.

6.1.1 Methods of measuring bond strength

The most commonly used techniques to characterize bond quality of Si wafer (fusion) bonding are probably the following three methods: crack opening method, blister test, and tensile strength test.

The crack opening method has been one of the most widely used techniques to measure bond strength of wafers due to its convenience. This test, which was developed by Maszara et al., is based on the equilibrium between surface energies (bonding forces) at the crack tip, and elastic forces of the separated wafer parts. The test involves introducing a crack by inserting a thin razor blade between the bonding interface of a wafer pair, and subsequently measuring the crack length (or the extent of crack propagation), as shown in Figure 6-1 [1].

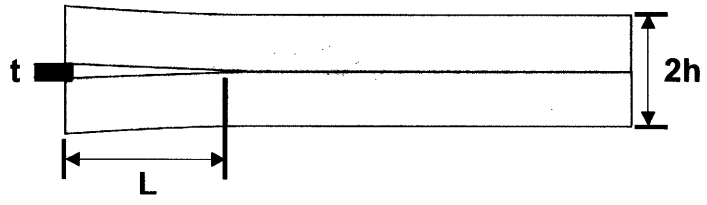


Figure 6-1 Schematic of crack opening method – razor blade insertion.

The length of crack propagation is typically measured using an infrared (IR) imaging system, and then incorporated into the following equation to calculate the critical strain energy release rate G_c or specific surface energy γ_s; the critical strain energy release rate is a material property, which quantifies the energy absorbed per unit area of crack.

$$G_C = 2\gamma_S = \frac{3}{16}\frac{t^2h^3}{L^4}\frac{E}{1-\nu^2} \tag{6-1}$$

In equation 6-1, L is the measured crack length, t is the thickness of razor blade, h is the thickness of bonded wafer, E is the elastic modulus, and ν is the Poisson's ratio of the

wafer. This method offers a well-defined loading. Moreover, it is very convenient because no preparation is necessary to fabricate the bonded wafer pair into a specimen for the test. In addition, most variables can be easily and correctly measured. However, the accurate calculation of G_c can be significantly compromised due to its fourth power dependence on crack length L, which is difficult to measure correctly using an IR or optical imaging system [2]. Furthermore, the fractured surface energy measured using this method is not completely reproducible due to the sensitivity of the measured values to humidity and time [3]. Moreover, this method is not applicable to wafer pairs with high bond strength (after or even before high temperature annealing), since razor blade insertions become either very difficult or even impossible [4].

The blister test has also been used to measure wafer bond toughness. The main advantage of this technique arises from its simple specimen fabrication, which involves etching holes through the thickness of the bottom wafer, subsequent wafer bonding, and cutting. The critical pressure P_f for wafer failure or debonding is measured by applying hydrostatic oil pressure through the hole in the specimen, as shown in Figure 6-2 [5].

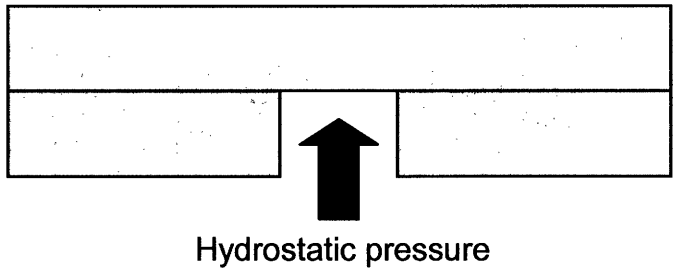


Figure 6-2 Schematic of blister test method.

The measured P_f value is then incorporated into the following equation to calculate the failure stress.

$$G_C = 2\gamma_S = \frac{0.176 F_f^2 r^4}{E t_w^3} \tag{6-2}$$

In Equation 6-2, E and t_w are the elastic modulus and thickness of the top wafer, respectively, and r is the radius of the hole. While it is simple to fabricate the specimens, it can be difficult to determine P_f if debonding occurs in an unstable manner due to the complicated stress state around the hole and bond interface [6].

The tensile test is also a very popular technique to characterize the bond strength of wafer pairs, in which tensile forces are applied to the specimen normal to the bonding interface until debonding occurs, as shown in Figure 6-3. Although straightforward and simple to use, this test generally provides much lower values of bond strength than the actual value due to the introduction of defects across the bonding interface induced during specimen dicing, and residual stresses stored during joint formation [7]. When the applied stress is concentrated at such defects, debonding can occur at low stresses. Thus, great care must be taken when dicing specimens to minimize damage around the cut edges or at the bonded interfaces. Even in the case of carefully prepared specimens, the maximum allowable tensile strength is always below the tensile strength of the epoxy adhesives used to attach the specimen to the test stubs. This specimen is also very sensitive to the alignment. Even slight misalignment of the test stubs may induce bending moments, which will lead to premature failure of the specimen.

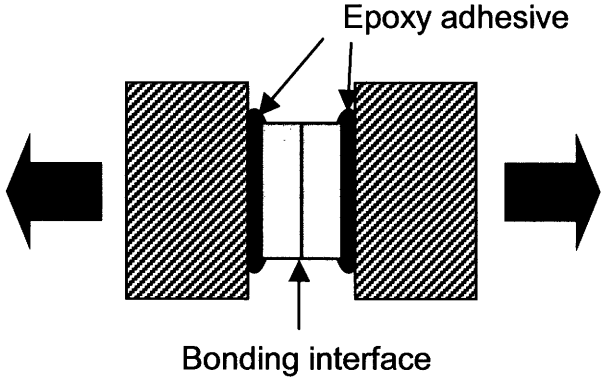


Figure 6-3 Schematic of the tensile test setup.

6.1.2 Four-point flexure method

Wafer bond toughness can also be measured using the four-point flexure (bending) method, which was originally developed to characterize bimaterial interfaces [8, 9]. Using the four-point flexure method, the critical strain energy release rate for crack propagation, G_c can be determined from a critical load and geometrical dimensions of a specimen. The specimen, which is schematically shown in Figure 6-4, offers a well-defined loading comparable to that of the crack-opening method, and enables a delamination to occur in a stable manner. It is made of two bonded layers with a central notch on the bottom layer, and a symmetric pre-crack at the center of its bonding interface.

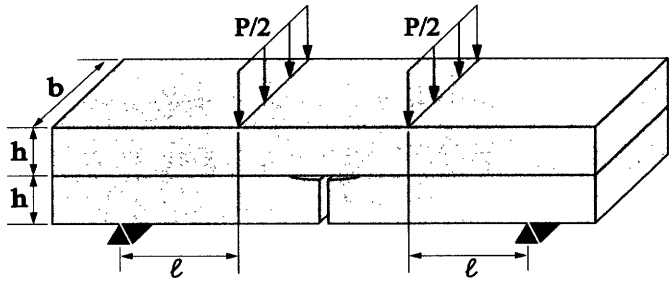


Figure 6-4 Schematic of four-point flexure specimen [A. A. Ayon et al, Sensors and Actuators A (Physical), Vol. A103, No. 1-2, p. 1-8, 2003].

In the case where two layers of the four-point flexure specimen are of the same thickness and elastic properties (E and ν) as illustrated in Figure 6-4, G_c can be calculated by:

$$G_C = 2\gamma_S = \frac{21}{16}\frac{P_c^2 l^2}{b^2 h^3}\frac{1-\nu^2}{E} \tag{6-3}$$

where P_c is the applied critical load, l is the distance between the inner and outer loading points, b and h are the width and thickness of the specimen beam, respectively [10]. The critical load, P_c is a load at which the strain energy release rate at the interface starts to

exceed the critical strain energy release rate or toughness, G_c and delamination occurs. P_c can be identified from the plateau in a load-displacement curve because a crack propagates at a constant load between the inner loading points. It should be noted that the loading at the interface of the four-point flexure specimen is a mixed mode of I and II. The ratio of mode I to mode II can be described by the phase angle of loading, Ψ (= $\tan^{-1}K_{II}/K_I$), which is determined by the ratio of moduli and thicknesses of the bonded layers [11]. In the case where the two bonded layers have equal elastic modulus and thickness values (e.g., Si-Si fusion bonding), Ψ is about 40°, which implies that mode I cracking (tensile opening mode) is slightly more predominant than mode II cracking (slip mode) at the interface [12]. Depending on the relative ratio of interface toughness and material toughness, the crack at the interface either stays in the interface, or deflects out of it and kinks into the substrate material following a mode I path [13]. This phenomenon will be further discussed later in this chapter.

The four-point flexure method has several advantages over other techniques. First of all, the experimental parameters in Equation 6-3 can be easily measured with high accuracy. The applied load can be measured with a load cell, and the geometric dimensions such as the length, height, and width of the four-point flexure specimen are determined from the specimen design stages, which can be confirmed after fabrication by easy measurements. A clear advantage of this method over the crack opening method is that the crack length does not need to be measured. Moreover, the test setup equipped with a four-point flexure specimen creates a constant moment between the two inner loading points during the test, which renders its G_c independent of crack length, when the crack is located within the inner loading points. This simplifies the test procedure by eliminating the need for precisely locating specimens with their notches at the exact symmetric central position. Due to these several advantages, the four-point flexure method was chosen for the current research to characterize the bond quality of the SiC/oxide-to-Si wafer pairs. This method had previously been employed by Miller and Turner to measure the bond toughness of silicon fusion bonds, and also by Tsau to characterize the integrity of wafer-level gold-gold thermocompression bonds [14, 6, 4].

6.2 Four-point bending tests of Si-SiC specimens at room temperature

6.2.1 Specimen fabrication

The specimens for four-point bending tests are fabricated simply by dicing bonded SiC/oxide-to-Si wafer pairs into pieces. The wafer bonding process follows the procedures described in Chapter 5: (slight) polishing of as-deposited SiC surfaces to improve smoothness, deposition and CMP of PECVD oxide on the polished SiC surfaces, wafer cleaning and RCA surface treatment, SiC/oxide-to-Si wafer contact at room temperature followed by high temperature (1000 °C) anneal.

The top layers of the specimens were fabricated from 4-inch, 525 μm thick, single-side polished, single crystalline (100) Si wafers coated with CVD SiC of initial thickness of either ~3.5 μm or ~28 μm. Both wafer faces were coated with SiC to avoid wafer bow and achieve higher flatness with the aim of facilitating the wafer bonding process. The as-deposited SiC surfaces were planarized and polished to improve their smoothness by eliminating any nodule-like structures. After planarization and polishing processes, the thickness of ~3.5 μm and ~28 μm thick SiC coatings was reduced to ~3.0 μm and ~25 μm, respectively. The RMS surface roughness (R_q) of the polished ~3 μm and ~25 μm thick SiC coatings before CVD oxide deposition was 1.1 nm and 1.9 nm, respectively. Following the slight polishing of the SiC coatings, 3 μm and 6 μm thick PECVD oxide was deposited on the polished 3 μm and 25 μm thick SiC surfaces. The wafers were annealed at 1000 °C for one hour for oxide densification. Finally, oxide CMP was performed until the surface roughness (R_q) of the oxide became smaller than ~0.7 nm.

The bottom layers of the specimens were fabricated from Si wafers with the same specifications used for the top layers. Instead of SiC coatings, the Si wafers for the bottom layers have to be etched to define ~100 μm deep and 600 μm wide single-line (rectangular) trenches, which will act as notches for the four-point flexure specimens. To

pattern the trenches, the Si wafers were first spin-coated with thick photoresist, AZ4620, exposed with a mask, and then developed. Finally, the Si wafers protected with the patterned thick photoresist layers were deep reactive ion etched (DRIE) to a depth of ~100 μm. The typical recipe for the DRIE process for Si wafers achieves an etch rate of 2.0 - 2.6 μm/min. After the etching is completed, the photoresist residue must be thoroughly removed from the Si wafer surfaces by 'piranha' clean (3:1 H_2SO_4:H_2O_2).

Both the top and bottom layer wafers were then cleaned with 'piranha', and their surfaces were subsequently treated by RCA™ clean to make them hydrophilic. To finalize the SiC/oxide-to-Si wafer bonding process, wafer contact at room temperature and high temperature anneal (at 1000 °C) were performed following the procedures described in Chapter 5.

Following wafer bonding, specimens were cut from the bonded wafer pair using a diamond saw (die-saw). The first cut was made through the bottom layer wafer to fabricate a central notch such that it intersects with the previously etched single-line trench. Combined with the etched trench, this first cut completes the fabrication of central notches in four-point flexure specimens. The procedure for creating a pre-crack is schematically shown in Figure 6-5. Achieving a precise cut is important for the successful initiation of crack propagation or specimen delamination. Therefore, care must be taken to ensure the cut intersects the etched single-line trench as shown in Figure 6-6. An effective way to make a successful notch cut is to make one cut at each end of the bonded wafer in a direction parallel to the specimens. These two cuts help spot and mark the exact location of the single-line trench, which facilitates precise cutting. Following the first cut for notch fabrication, the wafer is diced in a direction normal to the first cut to make eight to nine specimens of 8 mm width. Finally, the diced wafer is immersed in acetone for several hours to allow the easy removal of the mounting tape, which was used to hold the wafer during the saw cutting. This helps to avoid excessive forces from being applied to the specimens, which might generate residual stresses or

invisible small cracks in the specimens, when detaching them from the sticky mounting tape.

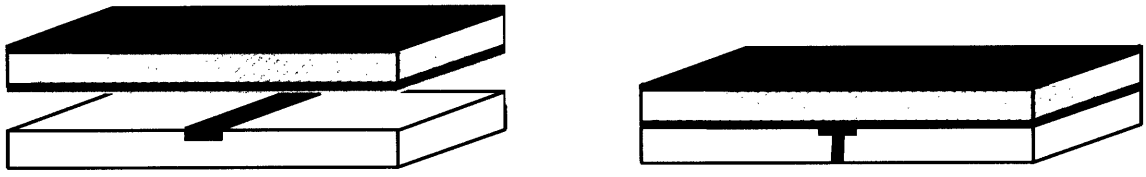


Figure 6-5 Procedure for creating a pre-crack: (a) Unnotched top layer is a Si wafer coated with CVD SiC layers (on both faces), which is bonded to the notched (by DRIE) bottom Si layer using PECVD oxide interlayer. (b) Following wafer bonding, a diesaw cut is made to complete the pre-crack.

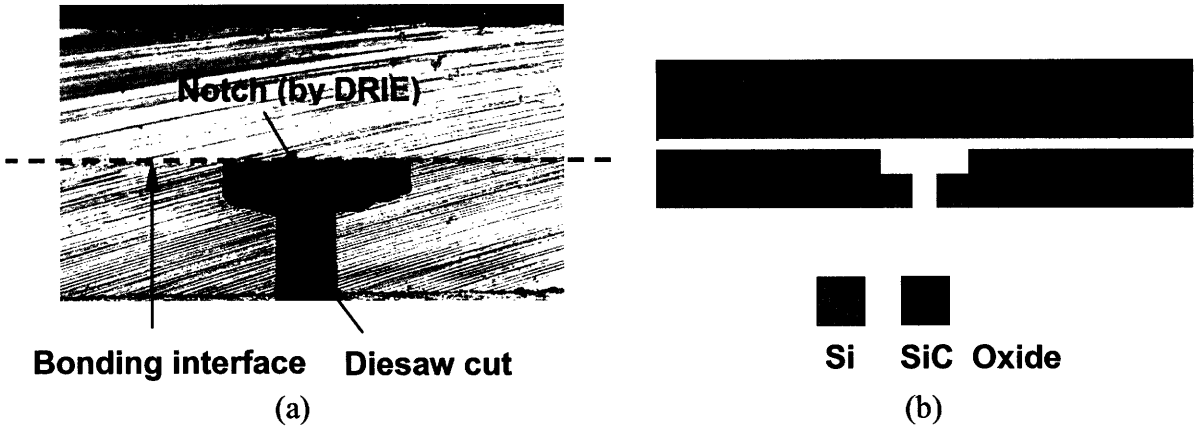


Figure 6-6 (a) Cross-section of a four-point flexure specimen showing the central pre-crack fabricated by DRIE and diesaw cutting. (b) Schematic showing a wider field of view.

6.2.2 Test apparatus

Mechanical tests were performed using a commercial servo-hydraulic machine (INSTRON™) with a four-point flexure fixture, which is installed at the MIT Technology Laboratory for Advanced Composite (TELAC). The four-point flexure fixture is designed to fit specimens of any thickness and width up to 8 mm. The distance between the two inner loading points is 20 mm, while the two outer loading points are 40

mm apart, with the specimen notch placed exactly at the center of the two inner or outer loading points, as shown in Figure 6-7. The four rollers corresponding to the four loading points are 4.8 mm diameter carbon steel cylinders. The testing machine is equipped with a 100 N load cell, and both the applied force and the corresponding crosshead displacement values are directly measured and recorded using LabVIEW™ 5.0 data acquisition software. A Questar™ telemicroscope was used to observe the crack initiation and subsequent propagation during the tests. The configuration of the test machine is shown in Figure 6-8.

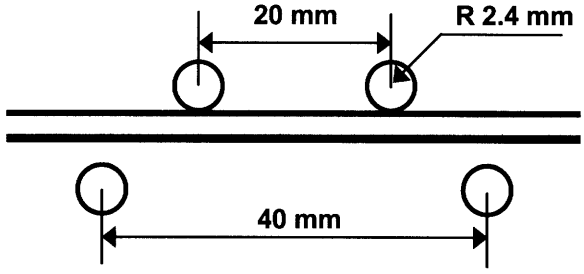


Figure 6-7 Configuration of a four-point flexure specimen in the fixture with four loading rollers.

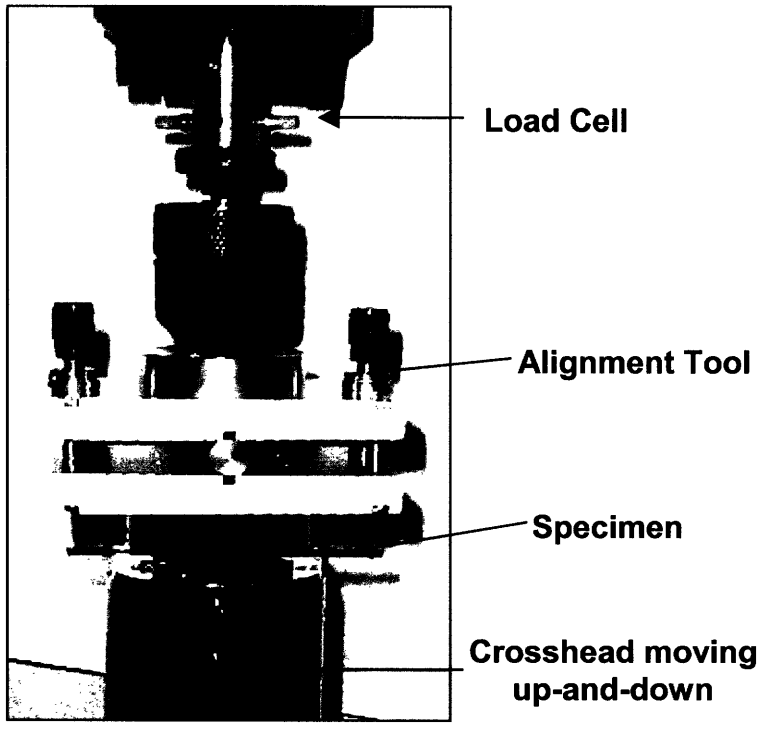


Figure 6-8 Overall configuration of the room temperature four-point flexure test machine.

6.2.3 Test procedure

Before placing specimens in the fixture, the four-point jig needs to be aligned carefully to achieve a uniform loading of the specimen. Early tests showed that the crack consistently propagates on one side of the specimen first, and the load was not maintained constant during the delamination [6]. This behavior was attributed to the misalignment of a test jig, which causes one of the inner loading rollers to touch and press the specimen before the other inner roller. Therefore, three-point bending occurs, which results in a larger loading of one side of the specimen. An attempt was made to correct for the misalignment using an 8 mm wide by 1 mm thick silicon beam with two piezoresistive strain gages. Detailed procedure for use of the four-point jig alignment was described by Turner [4]. The employment of the strain gage alignment tool turned out to be effective in achieving a uniform loading of the specimen, and thus, this alignment procedure was performed before each test.

Following alignment, a specimen was placed in the fixture such that the central notch of the specimen was aligned with the center of the fixture. Although the moment is maintained constant between the two inner loading points, aligning the specimen with the center of the fixture enables a clear and larger critical load (i.e., a plateau in the force-displacement curve) to be obtained. The specimen was loaded by controlling the displacement control at a rate of 0.10 mm/min, which was monitored using the telemicroscope. Loading was applied until the crack propagates up to the inner loading points. Once the crack reached the inner loading points, the specimen was unloaded.

6.2.4 Test results

Seven four-point flexure specimens were tested at room temperature. All of them had 3.0 μm thick SiC layers on both faces of unnotched 525 μm thick Si side, and 3 μm

thick PECVD oxide interlayer. All the specimens delaminated along the oxide/silicon bonding interfaces.

Figure 6-9 (a) shows a typical load-displacement plot, where a clear plateau at a critical load of ~ 4 N is observed. The loading path does not appear to be smooth, which is believed to be caused by the settlement of the specimens and loading rollers. Once initiated, the (delamination) crack proceeded at a constant load of 4 N until the crack reached the outer loading points where the load starts to increase again. Finally, the specimen was unloaded, which follows a different path with a smaller slope than the loading path. This is due to the existence of the crack, which propagated at the interface.

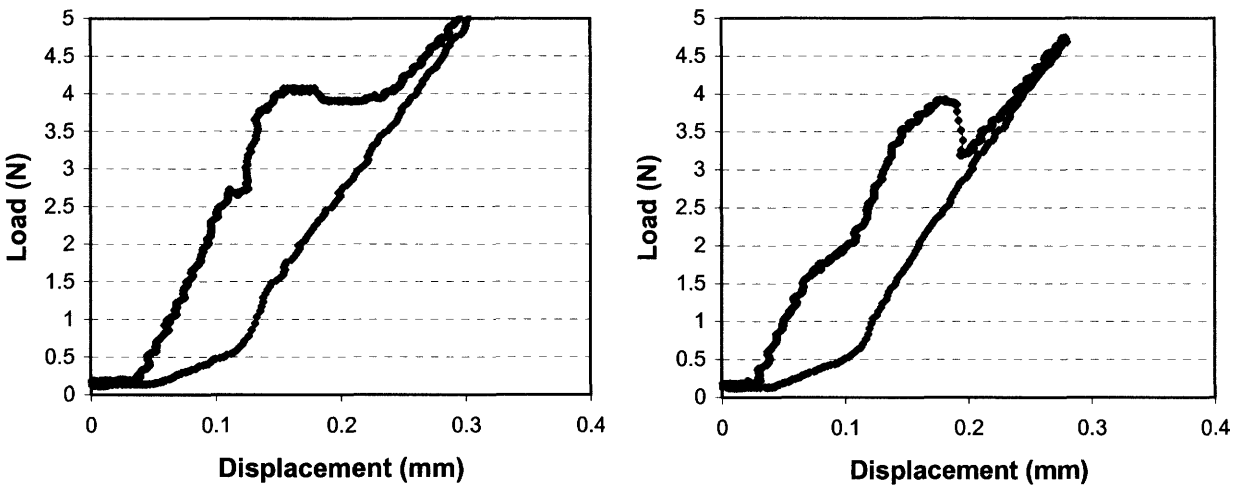


Figure 6-9 (a) A typical load-displacement plot for a four-point flexure test at room temperature, which shows a complete plateau. (b) A load-displacement plot showing an incomplete plateau.

The plot in Figure 6-8 (b) shows an incomplete plateau, which proceeded for a while, followed by an abrupt load drop. This is believed to be caused by an incomplete bonding

interface, which might have contained partially unbonded areas at the interface. However, this plot also showed that the delamination initiated at a load of approximately 4 N.

The thickness of SiC was relatively thin compared to that of Si, and thus, the stiffening contribution of the SiC on the unnotched top layer may be neglected. Thus, the toughness of the bonding interface can be obtained using Equation 6-3, which is calculated to be G_c = 1.3 - 1.4 J/m^2. This value is comparable to those for Si-Si interfaces bonded at relatively lower temperatures of 500 - 600 °C for 24 hours [6, 4].

6.3 Bonding integrity of Si-SiC specimens at high temperatures

6.3.1 Apparatus for high temperature four-point bending test

The system used for high temperature four-point bending tests consists of an MTS^{TM}-810 load frame, an INSTRON^{TM}-3118 ceramic testing system connected with an INSTRON^{TM}-8500 controller and a LabVIEW^{TM} 5.0 data acquisition software. To increase temperatures, the ceramic testing system is equipped with a vertically mounted split to be furnace, which is composed of electrical heating elements, alumina push rods attached with a water-cooling system, and SiC testing fixtures. The system has an INSTRON^{TM} load cell with a maximum capacity of 1000 lb. The overall configuration of the testing system and the SiC four-point fixture are shown in Figure 6-10 and Figure 6-11, respectively. The distance between the inner loading rollers and outer loading rollers of the four-point flexure fixture (Figure 6-11) are 20 mm and 40 mm, respectively, which is the same configuration as the fixture used for room temperature tests shown in Figure 6-7.

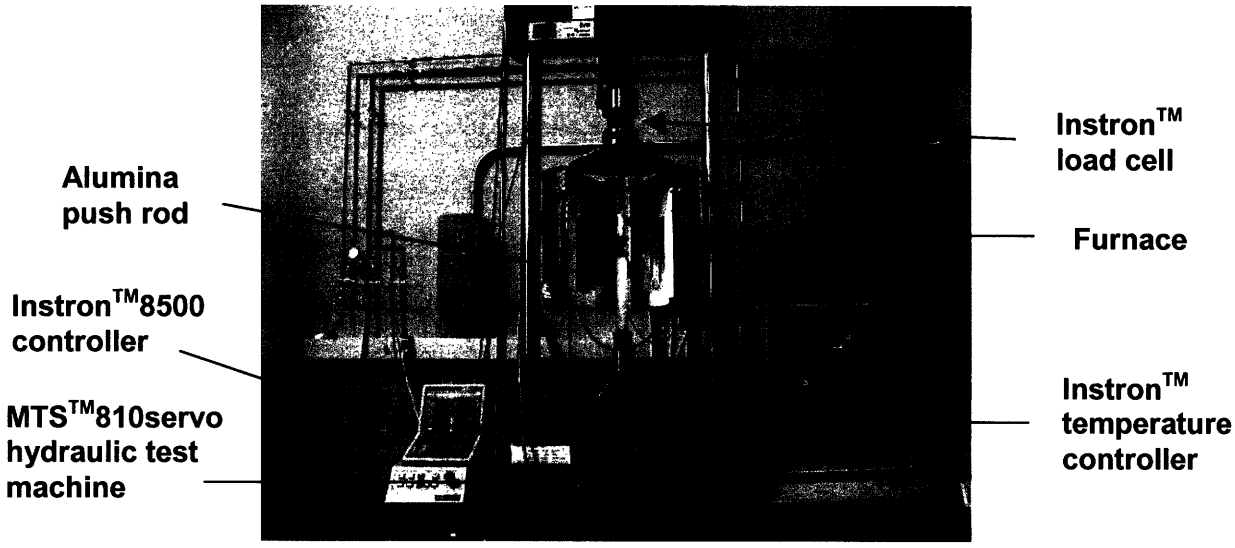


Figure 6-10 Configuration of high temperature four-point flexure testing machine.

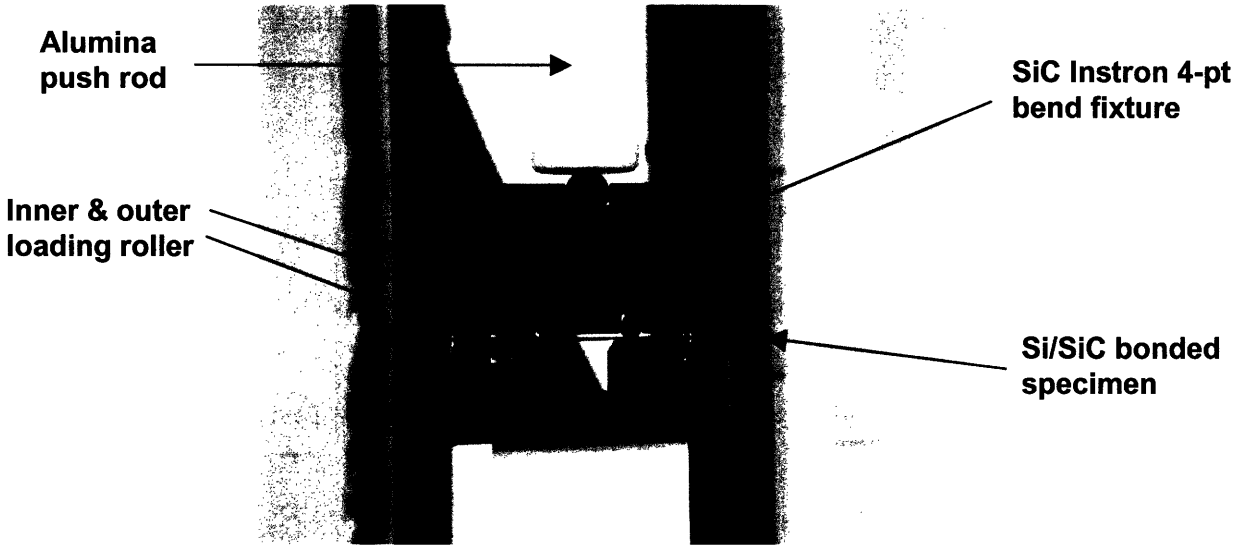


Figure 6-11 High temperature four-point flexure test setup.

6.3.2 Test procedure

The four-point flexure specimen is located in the fixture with the etched notch located at the center of the fixture. The entire fixture is then transferred into the alumina push rod, and the specimen is heated to the desired temperature. Before heating up, the initial gap between the top-most push rod and the fixture is adjusted to about 1 cm. After the furnace reaches the desired temperature, the testing system needs to be kept at the temperature for at least 1.5 - 2 hours to allow the specimen and fixture to reach an equilibrium temperature and thermal expansion. Following this temperature hold, the fixture is slowly brought up to make a slight contact with the top-most alumina push rod. The actuator is then operated to move up the push rod at a rate of 0.001 mm/sec to apply a monotonic load to the specimen until it fractures or reaches a desired maximum displacement. After the test is completed, the specimen is unloaded to the original position, and the furnace is cooled down to ambient temperature. The load-displacement data has to be stored during the whole loading and unloading procedures. Chen and Moon previously described a detailed test procedure and cautions for high temperature four-point bending tests and creep tests [15, 16].

6.3.3 Test results

Eight specimens were tested at high temperatures ranging from 850 °C to 950 °C. Five of them had 3 μm thick SiC coatings, and the other three had 25 μm thick SiC coatings. Unlike room temperature tests, no delamination was observed in the high temperature tests. Instead of delamination along the bonding interface, all the specimens were observed to be fractured by a mode I crack that propagated through the unnotched top layer, as shown in Figure 6-12.

A load-displacement plot for the high temperature tests is shown in Figure 6-13, where the load increases linearly up to approximately 5.0 N, and then abruptly drops at the point of specimen failure. One of the specimens with 25 μm thick SiC coatings

showed a maximum load approaching approximately 7.0 N, but the other two specimens with 25 μm thick SiC coatings showed the same load-displacement behavior as Figure 6-13. It is not clear whether the increased load capability of one of the specimens with 25 μm thick SiC coatings was a real effect of SiC stiffening or was just a noise during the data acquisition. However, consistent sudden load drops at specimen failures are believed to indicate that the failure of the specimens at high temperatures is governed by a brittle fracture. For a brittle fracture of materials, the density of defects on the surface or in the bulk material significantly affects the material strength. Therefore, if the increased load capability of one of the specimens with 25 μm thick SiC was a real effect, the lower maximum loads of the other two specimens may be attributed to the scatter in the surface or material quality of the CVD SiC.

(a) (b)

Figure 6-12 Specimen fractures along mode I path: (a) Test at 850 °C. (b) Test at 950 °C.

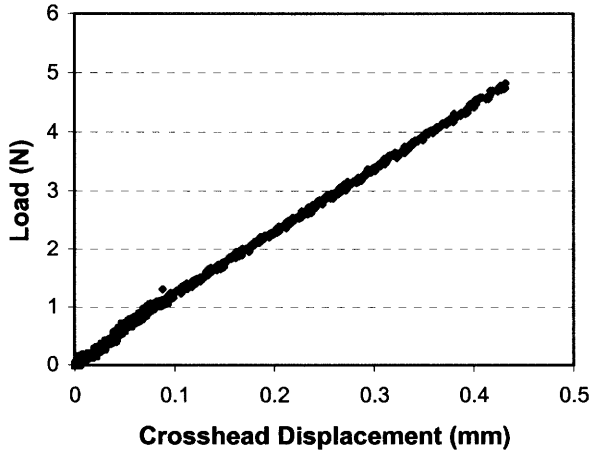


Figure 6-13 Load-displacement plot for a four-point bending test at 950 °C and a rate of 0.001 mm/sec.

To obtain a better idea of what part of the specimen triggered the crack, a four-point bending test was performed on a 525 μm thick, monolithic single-crystal Si specimen at 850 °C and a strain rate of 0.002 mm/sec. Figure 6-14 shows the load-displacement plot for the test, where the load appears to increase continuously up to approximately 5.3 N, and suddenly drop down to 2.0 N at which a plateau is observed. This suggests that the Si specimen was able to carry the applied loading up to a point somewhat higher than 5.0 N. Beyond that point, however, the load-carrying capability of the Si specimen drops significantly (to 2.0 N) due to a pronounced localized deformation under the loading rollers. Figure 6-13 does not exactly match with Figure 6-14 in terms of the maximum load capability and the corresponding displacement; this may be due to the different strain rate and test temperature, which can have significant effects on the mechanical behavior of a material at high temperatures. However, it is believed that the SiC coating (probably the side under tensile stress), which is the most brittle part of the specimen at test temperatures, triggered a crack when the load approached approximately 5.0 N. The crack initiated in the SiC layer seems to have propagated through the (unnotched) Si layer quickly, resulting in a mode I fracture since even the increased ductility or compliance of the Si layer at high temperatures was not sufficient to arrest the crack within the Si layer.

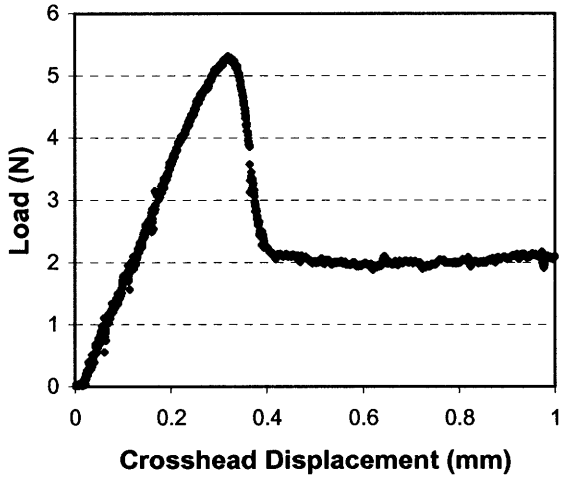


Figure 6-14 Four-point bending test of a 525 μm thick single-crystal Si specimen at 850 °C and a rate of 0.002 mm/sec.

6.4 Discussion of the test results

6.4.1 Comparison between the results of room and high temperature tests

As described in the previous sections, all the four-point flexure specimens tested at room temperature delaminated along the bonding interface (oxide/silicon interface), while all the others tested at high temperatures were broken by a mode I crack that quickly propagated through the unnotched top Si layer with SiC coatings. While it is difficult to analyze rigorously and quantitatively the competition between room and high temperature cracking, primarily due to the lack of reliable data of mechanical properties at varying temperatures for oxide, Si, and SiC, efforts are made here to provide an insight into the competition between interface cracking and substrate cracking.

A useful criterion was previously proposed by He and Hutchinson to determine whether an interface crack will remain and propagate in the interface or will deflect out of the interface and propagate into the substrate [13, 17]. The geometries analyzed by He and Hutchinson are shown in Figure 6-15, where plane strain cracks are considered, and the two materials bonded at the interface are assumed to be elastic and isotropic. In Figure 6-15 (b), a straight crack of angle ω and length a (which is assumed to be very small compared with all other geometric length quantities including the crack segment in the interface) deflects downward into material 2. Therefore, their analysis is asymptotic, but still provides a valuable insight into the behavior of a crack lying in the interface between two brittle materials.

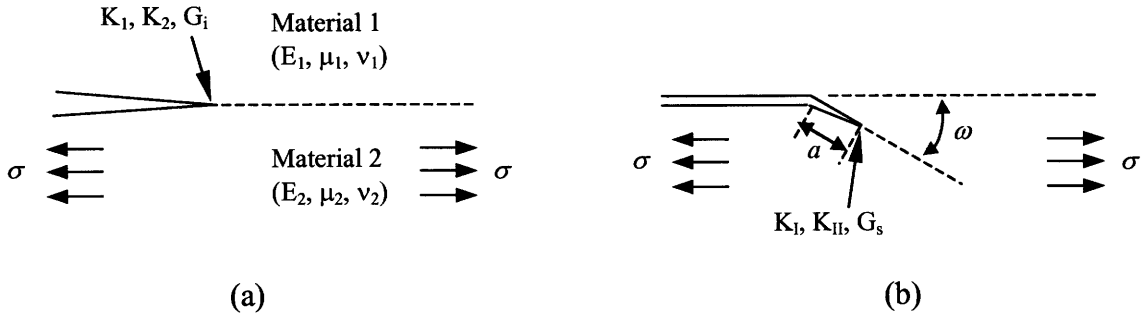


Figure 6-15 Geometries of cracks: (a) Interface crack. (b) Crack deflected into material 2 [M-Y. He et al., J. Am. Ceram. Soc., Vol. 74, No. 4, p. 767, 1991].

He and Hutchinson's criterion regarding this competition can be summarized by Equation 6-4, an inequality comparing the ratio of the energy release rates for interface cracking and for substrate cracking (which deflects out of the interface) to the ratio of interface toughness to substrate toughness.

$$\Delta = \frac{\Gamma_i}{\Gamma_s} - \frac{G_i}{G_s^{\max}} \tag{6-4}$$

where Γ_i is the interface toughness, Γ_s is the substrate toughness, G_i is the energy release rate for crack propagation at the interface, and $G_s^{\max}$ is the energy release rate for the crack deflecting into the substrate (maximized with respect to the deflection angle). If $\Delta < 0$ in Equation 6-4, the interface crack continues to advance in the interface and substrate cracking (or deflection into the substrate) will not occur since the condition for continuing crack advance in the interface is met at an applied (tensile) load lower than that necessary for the substrate cracking (i.e., the condition $G_i = \Gamma_i$ is reached before $G_s^{\max} = \Gamma_s$) [17]. Conversely, if $\Delta > 0$ in Equation 6-4, the condition for substrate cracking requires an applied load lower than that for interface cracking. Therefore, the crack segment lying in the interface initiates a kink, which deflects into the substrate. He and Hutchinson performed this analysis for various combinations of materials 1 and 2

with different stiffness values. The ratio of normalized G_i / G_s^{max} for $\alpha = 0.5$ and $\beta = 0$ is plotted in Figure 6-16 as a function of phase angle of loading Ψ for various values of nondimensional stress parameter η.

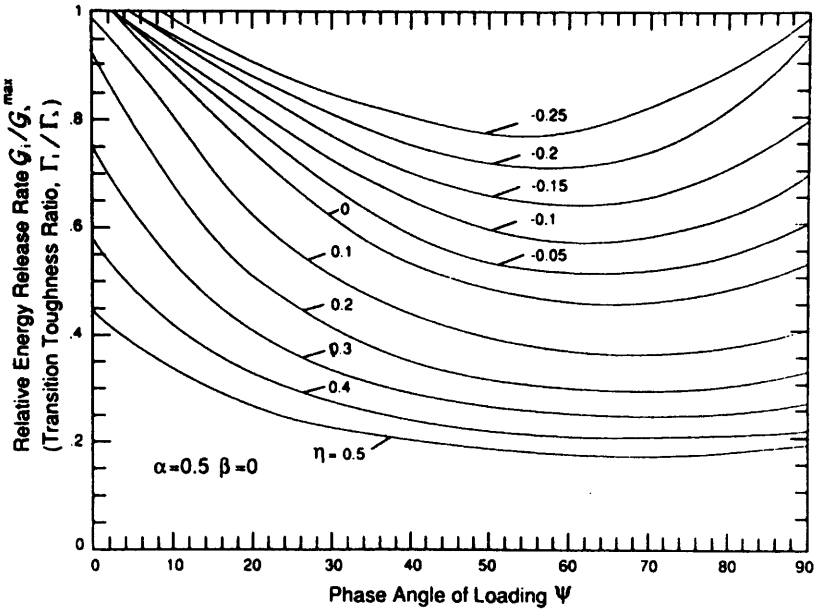


Figure 6-16 Energy release rate ratio G_i / G_s^{max} versus phase angle of loading Ψ for $\alpha =$ 0.5 and $\beta = 0$ [M-Y. He et al., J. Am. Ceram. Soc., Vol. 74, No. 4, p. 767, 1991].

In Figure 6-16, α and β are Dundurs' two elastic mismatch parameters defined as:

$$\alpha = (\overline{E}_1 - \overline{E}_2)/(\overline{E}_1 + \overline{E}_2) \tag{6-5}$$

$$\beta = \frac{1}{2}\frac{\mu_1(1-2\nu_2) - \mu_2(1-2\nu_1)}{\mu_1(1-\nu_2) + \mu_2(1-\nu_1)} \tag{6-6}$$

where E, μ, and ν are elastic modulus, shear modulus, and Poisson's ratio, respectively, and $\overline{E} = E/(1-\nu^2)$; Dundurs has reported that wide class of plane problems of elasticity

for bimaterials are dependent upon only α and β, the two nondimensional combinations of the elastic moduli, [18]. The energy release rates for advance of the crack in the interface (G_i) and kinked crack (G_s) are [17]:

$$G_i = (K_1^2 + K_2^2)/E_* \tag{6-7}$$

$$G_s = (K_I^2 + K_{II}^2)/\overline{E}_2 \tag{6-8}$$

where $E_* = \overline{E}_2(1+\alpha)/(1-\beta^2)$.

In addition, Ψ is a measure of the relative amount of mode II to mode I loading on the (parent) interface crack, which is defined by:

$$\Psi = \tan^{-1}(K_2/K_1) \tag{6-9}$$

and the nondimensional stress parameter η is:

$$\eta = \sigma\sqrt{a}/(E_* G_1)^{1/2} \tag{6-10}$$

In an effort to understand the difference between four-point flexural tests at room and high temperatures, consideration is now given to the tendency of the bonding (oxide/silicon) interface of the specimens for interface cracking or substrate cracking. Using the notation and conventions in Figure 6-15, the notched silicon layer and PECVD oxide layer are assumed to be material 1 and material 2, respectively, and the oxide/silicon bonding interface is considered to be the interface, where the pre-patterned notch can act as a parent crack or initiate a crack lying in the interface. For the Si-oxide bimaterial system, α = 0.35, if the following values are assumed for the elastic moduli and Poisson's ratios for Si and oxide (SiO_2) layer: E_{Si} = 165 GPa, ν_{Si} = 0.27, E_{Oxide} = 83 GPa, and ν_{Oxide} = 0.167 [19]. The effect of β on the ratio G_i/G_s^{max} was observed to be relatively weak for most representative materials combinations, and thus, attention is paid only to the case of β = 0, which is sufficient for the purpose of the present simple analysis

[13]. The toughness of the (bonding) interface at room temperature $\Gamma_i \approx 1.4$ J/m^2, which is obtained from the room temperature four-point bending tests. The fracture toughness of SiO_2 is reported to be in the range $K_{IC} = 0.85$ - 1.15 MPa$\sqrt{\text{m}}$, and thus, its toughness is in the range $\Gamma_s = 8.5$ - 15.5 J/m^2, which can be calculated from $\Gamma_s = K_{IC}^2 / \bar{E}_2$ [20, 21]. Therefore, the ratio of the interface toughness to substrate toughness is in the range $\Gamma_i / \Gamma_s \approx 0.09$ - 0.16 at room temperature. Figure 6-16 is plotted for $\alpha = 0.5$ and $\beta = 0$, while $\alpha = 0.35$ for the present analysis. Thus, it would be worth noting the directional dependence of $G_i / G_s^{\max}$ on α values. According to He and Hutchinson's analyses, all other parameters being the same, the larger α (i.e., material 2 is the more compliant material into which the crack deflects), the smaller the energy release rate ratio $G_i / G_s^{\max}$ [13]. Therefore, more appropriate $G_i / G_s^{\max}$ plots for $\alpha = 0.35$ are expected to be obtained by moving all the curves in Figure 6-16 upward a little further. From the comparison of the Γ_i / Γ_s values (≈ 0.09 - 0.16) with those plotted in Figure 6-16, it can be expected that the (parent) interface crack tends to stay and continue to advance in the interface rather than kinking into the substrate (oxide) layer, since the condition $\Delta < 0$ in Equation 6-4 is met for all the situations plotted in Figure 6-16. Even without the comparison with the curves in figure 6-16, it is evident from the small values of ratio Γ_i / Γ_s that the condition $G_i = \Gamma_i$ can be reached at much lower applied load than $G_s^{\max} = \Gamma_s$ at room temperature.

Unlike room temperature tests, no interface cracking or specimen delamination was observed in high temperature tests. Instead, all the specimens tested at high temperatures showed a mode I cracking that propagated through the unnotched top Si layer with SiC coatings. A possible explanation for this observation can be made based on the consideration of a change in the ratio $G_i / G_s^{\max}$ or Γ_i / Γ_s at high temperatures. The PECVD oxide layer is a solid at ambient temperature, but its mechanical behavior at high temperatures is just like all other glasses. It experiences a softening over a broad range of temperatures, which can be characterized by a continuous change in viscosity with temperature. The oxide layer experiences a softening and becomes more compliant at

high temperatures due to a reduction in viscosity, which is a measure of the resistance to flow upon exposure to an applied shear stress. Assuming all other factors stay the same, the increased compliance of the oxide layer at high temperatures would result in a decrease in G_i / G_s^{max}, which indicates an increase in the tendency for cracking through the (oxide) substrate. Therefore, it is believed that the bonding interface would not delaminate at high temperatures under the same applied load that resulted in interface cracking at room temperature. Rather, the condition for cracking through the (oxide) substrate might be satisfied before the condition for interface cracking (delamination). Even in this case, however, the crack deflecting into the oxide substrate is likely to be arrested in the oxide layer without further propagating into the SiC layer. From an observation of the abrupt facture of the four-point flexure specimens at high temperatures (shown in Figure 6-13), the cracking of the specimens appears to have been triggered from the SiC layer on the tensile (bottom) side when a condition for SiC fracture is met; the toughness of CVD SiC (in a direction parallel to the deposition), Γ_{SiC} = 16 J/m^2, which is a room temperature value, but it is believed that the value does not change significantly over the temperature range 850 - 950 °C [22]. Once initiated, the crack seemed to propagate through the Si substrate quickly following a mode I path. No delamination or peeling-off of the SiC coatings from the Si substrate was observed as previously mentioned in Moon's four-point flexural tests of Si-SiC specimens, which indicates that the (bonding) toughness of the interface between Si/SiC is higher than the toughness of either Si or the SiC layer [16]. Even the increased compliance or ductility of the Si substrate at high temperatures did not appear to be sufficient to suppress and arrest the propagation of cracks from the SiC layer.

In summary, interface cracking or specimen delamination along the oxide/silicon (bonding) interface occurred at room temperature, while mode I cracking propagating through the SiC and Si layers was observed at high temperatures.

6.4.2 Discussion of the effect of oxide interlayer on structural integrity

From the four-point bending tests, the oxide/silicon bonding interface at room temperature appears to offer lower toughness (~1.4 J/m^2) than a well-bonded Si/Si interface ($\geq$ 2.5 J/m^2). However, the relatively low toughness of oxide interlayer does not seem to be problematic at high temperatures from a materials fracture point of view. The microengine is designed to operate at high temperatures over which the cracking of the four-point flexure specimens is likely to be triggered from the most brittle SiC layer. While a more rigorous study needs to be conducted on the variation of the load-carrying capability with oxide thickness, it is believed that thinner oxide interlayer will generally be sufficient to improve the microengine performance.

6.5 References

1. W. P. Maszara et al., "Bonding of silicon wafers for silicon-on-insulator," J. Appl. Phys., Vol. 64, No. 10, p. 4943-4950, 1988.
2. M. A. Schmidt, "Wafer-to-Wafer Bonding for Microstructure Formation," Proceedings of the IEEE, Vol. 86, No. 8, p. 1575-1585, 1998.
3. T. Martini, "The crack opening method in silicon wafer bonding. How useful is it?," J. Electrochem. Soc., Vol. 144, No. 1, p. 354-357, 1997.
4. K. T. Turner, "An Evaluation of Critical Issues for Microhydraulic Transducers: Silicon Wafer Bonding, Strength of Silicon on Insulator Membranes and Gold-Tin Solder Bonding," S. M. Thesis, Dept. of Mechanical Engineering, MIT. Cambridge, MA 2001.
5. Q.-Y. Tong and U. Gösele, Semiconductor wafer bonding, John Wiley & Son, Inc., 1999.
6. B. Miller, "Hybrid Silicon/Silicon Carbide Microstructures and Silicon Bond Strength Tests for the MIT Microengine," S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, Cambridge, MA 2000.
7. A. Plößl and G. Kräuter, "Wafer direct bonding: tailoring adhesion between brittle materials," Materials Science and Engineering, R25, p. 1-88, 1999.
8. H. C. Cao and A. G. Evans, "An experimental study of the fracture resistance of bimaterial interfaces," Mechanics of Materials, Vol. 7, p. 295-304, 1989.
9. P. G. Charalambides et al, "Development of a test method for measuring the mixed mode fracture resistance of bimaterial interfaces," Mechanics of Materials, Vol. 8, p. 269-283, 1990.
10. A. A. Ayon et al, "Characterization of silicon wafer bonding for Power MEMS applications," Sensors and Actuators A (Physical), Vol. A103, No. 1-2, p. 1-8, 2003.
11. P. G. Charalambides et al., "A test specimen for determining the features resistance of biomaterial interfaces," Journal of Applied Mechanics, Vol. 56, p. 77-82, 1989.
12. M-Y. He and J. W. Hutchinson, "Crack deflection at an interface between dissimilar elastic materials," The Processing and Mechanical Properties of High Temperature/High performance Composites Annual Report, Ed. by A. G. Evans, University of California Santa Barbara, 1989.
13. M-Y. He and J. W. Hutchinson, "Kinking of a Crack Out of an Inteface," J. Appl. Mech., Vol. 56, p. 270-278, 1989.
14. C. H. Tsau et al, "Characterization of low temperature, wafer-level gold-gold thermocompression bonds," Mat. Res. Soc. Symp. Proc., Vol. 605, p. 171-176, Fall 1999.
15. K.-S. Chen, "Materials Characterization and Structural Design of Ceramic Micro Turbomachinery," Ph. D. Thesis, Dept. of Mechanical Engineering, MIT, Cambridge, MA, 1999.
16. H.-S. Moon, "Design of Si/SiC Hybrid Structures for Elevated Temperature Micro-Turbomachinery," Ph. D. Thesis, Dept. of Mechanical Engineering, MIT, Cambridge, MA, 2002.
17. M-Y. He et al., "Kinking of a Crack out of an Interface: Role of In-Plane Stress," J. Am. Ceram, Soc., Vol. 74, No. 4, p. 767-771, 1991.

18. J. Dundurs, "Edge-bonded dissimilar orthogonal elastic wedges," J. Appl. Mech., Vol. 36, p. 650-652, 1969.
19. S. M. Hu, "Stress-related problems in silicon technology," J. Appl. Phys., Vol. 70, No. 6, p. R53-R80, 1991.
20. National Institute of Standards and Technology (NIST) Property Data Summaries for Silicon Dioxide: See "http://www.ceramics.nist.gov/srd/summary/ftgsio.htm".
21. M. Iwasa et al., "Fracture toughness of quartz and sapphire single crystals at room temperature," Journal of the Society of Materials Science, Japan, Vol. 30, No. 337, p. 1001-1004, 1981.
22. National Institute of Standards and Technology (NIST) Property Data Summaries for CVD Silicon Carbide: See "http://www.ceramics.nist.gov/srd/summary/ftcvd.htm".

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Overall summary

The SiC process development was motivated by the critical need for improving the microengine's performance by incorporating an excellent refractory material (SiC) into the Si-based microengine structures. In an effort to achieve the goal, given the limitations imposed by the microfabrication difficulties in SiC processes, Si-SiC hybrid turbine structures have been proposed as an effective mid-term approach, which minimizes the technical risks associated with SiC processes by taking full advantage of the precision of Si microfabrication. The proposed Si-SiC hybrid structures require the implementation of SiC into strategic locations (i.e., patterned Si turbine discs) of the Si-based microengine, the fabrication of which entails the following key process steps:

- DRIE patterning of disc-shape trenches for reinforcement on a Si wafer (which corresponds to the turbine of an assembly of six-wafer stacks for microengine structures)
- Chemical vapor deposition of SiC on the patterned Si wafer
- Mechanical planarization of the Si wafer coated with SiC
- Wafer bonding of the planarized wafer to another Si wafer (which corresponds to the compressor in a six-wafer stack assembly for the microengine)

The research efforts described in this thesis have been focused on demonstrating the feasibility of the proposed Si-SiC hybrid structures, which were verified to be effective in improving the microengine's performance by increasing its allowable operational

temperature [1, 2, 3]. To achieve the primary goal, critical issues in each of the proposed SiC process steps have been identified.

In the process of SiC deposition on Si wafers, the primary concern has been the relationship between residual stresses in the SiC coatings and the CVD process variables. Residual stress control in SiC coatings is of the most critical importance to the CVD process itself as well as to the subsequent wafer planarization process, because residual stress-induced wafer bow could increase the likelihood of wafer cracking significantly during both the CVD and post-CVD processes. The study of the CVD process was focused on the variation of residual stress in SiC coatings with CVD parameters, including: H_2/MTS ratio, deposition temperature, and HCl/MTS ratio. In the course of the CVD parametric study, a method for residual stress calculation was also developed to isolate the intrinsic residual stress from the thermal residual stress. The residual stress study has demonstrated that very low residual stress in CVD SiC coatings can be achieved (to less than several tens of MPa) consistently. In addition to the quantification of residual stresses, qualitative explanations for the generation of intrinsic stresses in CVD SiC (with varying CVD parameters) were also offered based on the surface stress model, which had been postulated as the mechanism responsible for the intrinsic compressive stresses in other deposited materials. Along with the effort to achieve low residual stresses, the microstructures and mechanical properties of CVD SiC have also been characterized in order to estimate the mechanical behavior of SiC in Si-SiC hybrid structures for the microengine and other applications.

In the post-CVD processes, key barriers to wafer planarization and Si-to-SiC wafer bonding processes have been identified, and efforts were made to circumvent these problems. In an effort to minimize unwanted SiC deposition on object Si wafers, Si shadow mask wafers were developed. These were placed in the CVD chamber along with the object wafers to allow for selective SiC deposition. This proved to be an effective way to increase planarization yields. Si-to-SiC wafer bonding was achieved successfully using CVD oxide as an interlayer material. This overcame the surface topography variations caused by SiC nodules deposited on the Si substrate.

Finally, the mechanical integrity of specimens cut from the bonded Si-SiC wafers was investigated using four-point flexural tests. The test results demonstrated that the bonding interface of the Si-SiC hybrid structures with oxide interlayer retained its integrity at high temperatures.

7.2 Conclusions

The primary objective of the process development of Si-SiC hybrid structures was to demonstrate the feasibility of fabricating an advanced turbine-compressor spool structure, which is capable of increasing the microengine's power density. The overall research goal was achieved through the integration of the key process steps of SiC chemical vapor deposition, wafer-level planarization, and wafer-level bonding.

Relatively thick CVD SiC coatings (of the order of several tens of μm, which is much thicker than most other thin deposited materials for microelectronics devices) were successfully deposited on Si wafers by controlling the residual stress in the SiC to within several tens of MPa. An improved understanding of the sources of residual stress in CVD SiC and its dependence on process variables was achieved. The post-CVD processes; wafer planarization and Si-to-SiC wafer bonding using an oxide interlayer were also developed successfully. In addition, the mechanical integrity of the bonding interface of the Si-SiC hybrid structures at high temperatures was confirmed by four-point bending tests.

This thesis demonstrates the potential for implementing refractory materials into Si-based MEMS structures to improve their power efficiency. Although the focus was confined to CVD SiC, the research work presented in this thesis is expected to serve as a reference for future research on other power-MEMS materials and structures.

7.3 Contributions

The work presented in this thesis established the basis and design guidelines for power-MEMS materials and structures, by demonstrating the overall feasibility of Si-SiC hybrid turbine structures based on the development and refinement of the key process steps.

The contributions of the present work include the following specific achievements:

- Conducted a thorough characterization of CVD SiC including study of microstructures, composition, and mechanical properties.
- Demonstrated control of residual stress in CVD SiC via CVD process parameters such as source gas ratio (H_2/MTS), deposition temperature, and HCl concentration.
- Developed a method for residual stress calculation by which the intrinsic stress component can be isolated from the thermal stress component.
- Identified the underlying mechanisms governing residual stress in CVD SiC.
- Demonstrated the feasibility of CVD SiC deposition using Si shadow masks by which unwanted SiC deposition can be effectively minimized.
- Demonstrated wafer-level mechanical planarization of SiC deposited on Si substrates.
- Identified key barriers to Si-to-SiC wafer bonding, and demonstration of wafer-level Si-SiC bonding using CVD oxide interlayer.
- Performed mechanical testing of Si-SiC hybrid structures at room and high temperatures via four-point bending tests, and verified the bond integrity.
- Identified and analyzed the change in failure mode of Si-SiC bonded specimens between room temperature and high temperature.

7.4 Future work

This thesis represents comprehensive research efforts to verify the feasibility of building Si-SiC hybrid structures. As such it should be viewed as a solid foundation for future work.

SiC planarization is currently the process step with highest technical risk. Future efforts must be focused on increasing the planarization yield, which is highly dependent on the polishing machines' performance. A faster and more effective planarization may be possible if a high performance polisher is used such as one with the capability of polishing both wafer faces simultaneously. In parallel, the shadow masking technique should be refined further to reduce unwanted SiC deposition from gas bleeds. Efforts should also be made to improve the surface finish, which determines the success of subsequent wafer bonding.

Future Si-to-SiC wafer bonding efforts should target achieving complete bonding, in parallel with improvement of the planarization process. For the present work, the wafer bonding efforts were focused on making four-point flexure specimens out of Si-SiC bonded wafer pairs, for which Si wafers with plain and uniform SiC coatings (without patterns) were used. The bonding experiments have to be extended to wafers with SiC reinforcement patterns (for actual microengine devices), which is expected to be more challenging due to dishing effects around the circumference of patterns during planarization. The detrimental effect of the discontinuous steps (height difference around the SiC reinforcements) on wafer bonding may be attenuated by using an oxide interlayer appropriately, which has to be accompanied by the advancement of oxide CMP and concomitant post-CMP cleaning steps.

Finally, it should be noted that the microengine is a bonded assembly of six wafer stacks consisting of several individual components. Therefore, any approach to modify

the existing wafer processes involving SiC fabrication has to be viewed in terms of the overall microengine process sequence with regard to its compatibility with other process steps that have been proven to be reliable. The mechanical integrity of the Si-SiC hybrid structures in an actual operational environment (high temperatures and rotational speeds) can be tested only if the hybrid turbine-compressor spool is successfully implemented within the microengine structures.

7.5 References

1. H.-S. Moon et al., "Development of Si/SiC hybrid structures for elevated temperature micro-turbomachinery," Accepted for publication, J. MEMS, 2004.
2. B. Miller, "Hybrid Silicon/Silicon Carbide Microstructures and Silicon Bond Strength Tests for the MIT Microengine," S. M. Thesis, Dept. of Aeronautics and Astronautics, MIT, Cambridge, MA 2000.
3. S. M. Spearing et al., "Materials, Structures, and Packaging," The MIT Microengine Project, 2000 Annual Report, MIT Property, Cambridge, MA, 2000.

APPENDIX

A. Kinetic processes involved in SiC deposition on Si substrates: An LPCVD reactor model

To illustrate the competition between the diffusion process and chemical reaction on the silicon substrates during the CVD SiC deposition, a simple first-order surface reaction in the LPCVD reactor is considered here.

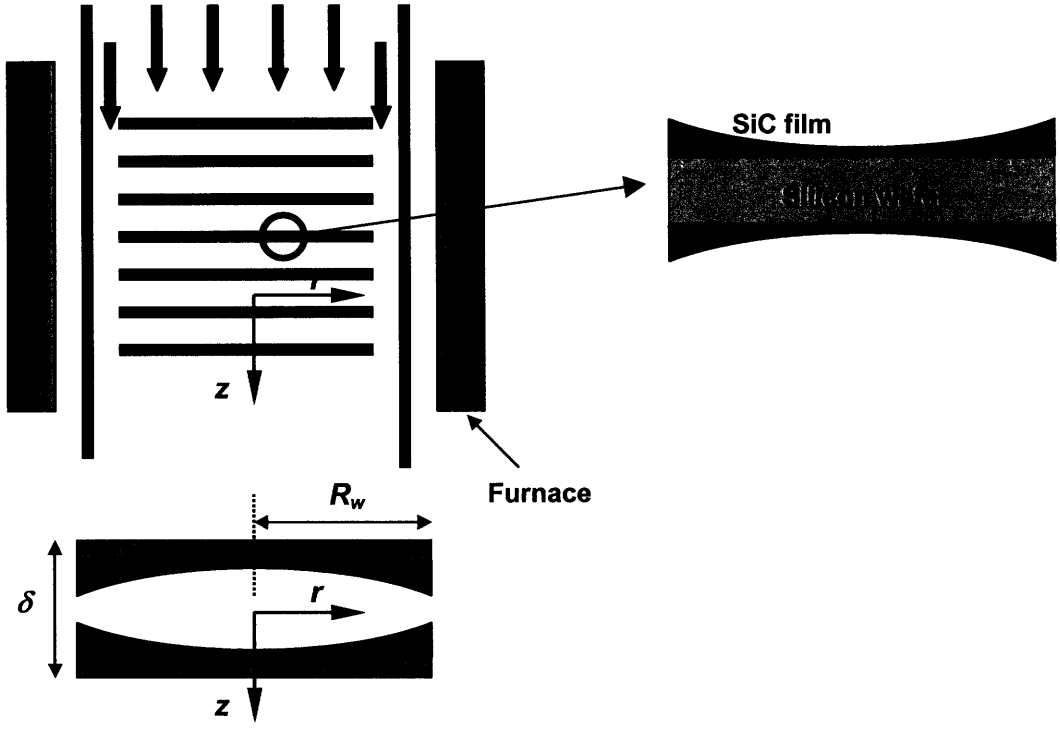


Figure A-1 LPCVD reactor and wafer configurations.

The model is based on the schematic representation of the LPCVD reactor shown in Figure A-1, where the silicon substrates are placed concentrically and perpendicularly to

the direction of the gas flow. The temperature difference between the wafers and the furnace wall is negligible at high deposition temperatures and low pressures, which eliminates the need for an energy balance consideration. The details of the flow field are not accounted for here, and just a simple plug flow is assumed in the annular region of the wafers. Because the wafer spacing, δ, is small relative to the wafer diameter, R_w (= 50 mm), the system can be considered as a two-dimensional problem such that the variation of reactant concentration in the r-direction is much greater than that in the z-direction. Therefore, diffusion can be assumed to be the main transport mode in the space between the silicon wafers.

Based on the above assumptions, the reactant concentration can be described in the wafer region by the equation for the balance between the diffusion and chemical reaction [1]:

$$-\left(2\pi r\delta D\left.\frac{dc}{dr}\right|_r\right)-\left(-2\pi r\delta D\left.\frac{dc}{dr}\right|_{r+\Delta r}\right)-2\left(2\pi r\Delta r k_s c\right)=0$$

$$\longrightarrow \qquad \frac{D}{r}\frac{d}{dr}\left(r\frac{dc}{dr}\right)-\frac{2k_s c}{\delta}=0 \qquad \text{(A-1)}$$

where c is the reactant (gas) concentration, r is the radial coordinate, δ is the distance between two neighboring wafers, D is the diffusion coefficient, and k_s is the surface reaction rate constant. Equation A-1 has the following boundary conditions:

$$\left.\frac{dc}{dr}\right|_0=0 \qquad\qquad c\big|_{r=R_w}=c_b$$

where c_b is the bulk concentration, R_w is the radius of Si wafers.

Equation A-1 can be simplified to the following dimensionless equation:

$$\frac{1}{\xi}\frac{d}{d\xi}\left(\xi\frac{dy}{d\xi}\right)-(Da)y=0 \tag{A-2}$$

with

$$\left.\frac{dy}{d\xi}\right|_0=0 \qquad y|_{\xi=1}=1$$

and

$$y=\frac{c}{c_b} \qquad \xi=\frac{r}{R_w} \qquad Da=\frac{2k_sR_w^2}{D\delta}$$

where Da is a dimensionless Damkoehler number.

The solution for Equation A-2 has the form of a modified Bessel function:

$$y=\frac{I_0\left(\xi\sqrt{Da}\right)}{I_0\left(\sqrt{Da}\right)} \tag{A-3}$$

where I_0 is a modified Bessel function. From Equation A-3, it is expected that the film thickness should increase as the distance from wafer center increases.

Equation A-3 also offers information regarding the film thickness variation with Da values. In the case where $Da \gg 1$, the deposition process is controlled by the diffusion (mass transfer) process, while it is controlled by the chemical reaction if $Da \ll 1$. Therefore, smaller Da numbers are required for uniform deposition thickness (across the wafer diameter). This implies that larger values of D (diffusion coefficient) and δ (distance between two neighboring wafers) are desired for uniform film thickness.

B. Thermal Expansion Coefficients of Silicon Carbide and Silicon

To calculate thermally-induced residual stress in CVD SiC coatings on Si wafers, it is critical to obtain reliable thermal expansion coefficients of SiC and Si.

It is important to note that the coefficient of thermal expansion (CTE) of a material is a temperature-dependent property; in general, it gradually increases with temperature. Typical CTE values for metals and alloys range from 10×10^{-6} to $30 \times 10^{-6}\ K^{-1}$, while ceramics usually have lower values ranging from 1×10^{-6} to $20 \times 10^{-6}\ K^{-1}$ [2]. Two physical quantities, displacement and temperature, are required to determine CTE values. One of the most widely used techniques for CTE measurement is push rod dilatometry, in which the displacement resulting from a specimen with increasing temperature is mechanically measured by two rods in contact with opposite faces of the specimen located in a furnace [3]. The measured displacement data are transmitted to a sensor located away from the furnace, yielding a displacement-temperature plot from which the CTE can be calculated.

The measurement of thermal expansion coefficient of the Hyper-Therm's CVD SiC films on Si wafers was not performed for the present study mainly due to the difficulties associated with the specimen preparation for push rod dilatometry such as buckling or cracking of the SiC films separated from the Si substrates. Therefore, efforts had been made to find reliable CTE values of β-SiC from the literature, and two data sets were selected and used for the thermal stress calculation. They are Li & Bradt and Reeber & Wang's data.

Li and Bradt used XRD to precisely measure the change in the lattice parameter of β-SiC [4]. They used specimens prepared as a powder form to obtain CTE values for

several crystallographic orientations, and calculated an average CTE for a specimen of random orientations. Li and Bradt's average CTE of β-SiC is given by the following function of temperature:

$$\alpha_{SiC}(T) = 3.19\times10^{-6} + 3.60\times10^{-9}[T-273] - 1 - 1.68\times10^{-12}[T-273]^2 \qquad \text{(B-1)}$$

Reeber and Wang obtained the CTE of β-SiC as a function of temperature using a multi-frequency Einstein model, the parameters of which were evaluated by fitting to an experimental lattice parameter at room temperature [5]. Reeber and Wang's suggested CTE of β-SiC is given by:

$$\alpha_{SiC}(T) = -2.15\times10^{-6} + 1.99\times10^{-8}T - 2.04\times10^{-11}T^2 + 9.47\times10^{-15}T^3 - 1.65\times10^{-18}T^4 \qquad \text{(B-2)}$$

The CTE of single crystal silicon has been relatively well studied, and reliable data sets existed. Soma and Kagaya summarized the existing values and suggested the following equation [6]:

$$\alpha_{Si}(T) = 3.725\times10^{-6}[1 - e^{-5.88\times10^{-3}(T-124)}] + 5.548\times10^{-10}T \qquad \text{(B-3)}$$

As described above, CTE is a temperature-dependent property. Therefore, mean CTE values need to be used to determine thermal residual stresses precisely. A mean CTE can be calculated by integrating the CTE functions over the temperature ranges of interest:

$$\alpha_{mean} = \frac{\int_{T_0}^{T}\alpha(T)dT}{\int_{T_0}^{T}dT} \qquad \text{(B-4)}$$

Equations B-1, B-2, and B-3 are depicted as curves in Figure B-1, where curve B-1 (Li and Bradt) deviates significantly from curve B-2 (Reeber and Wang) at temperatures below ~540 K.

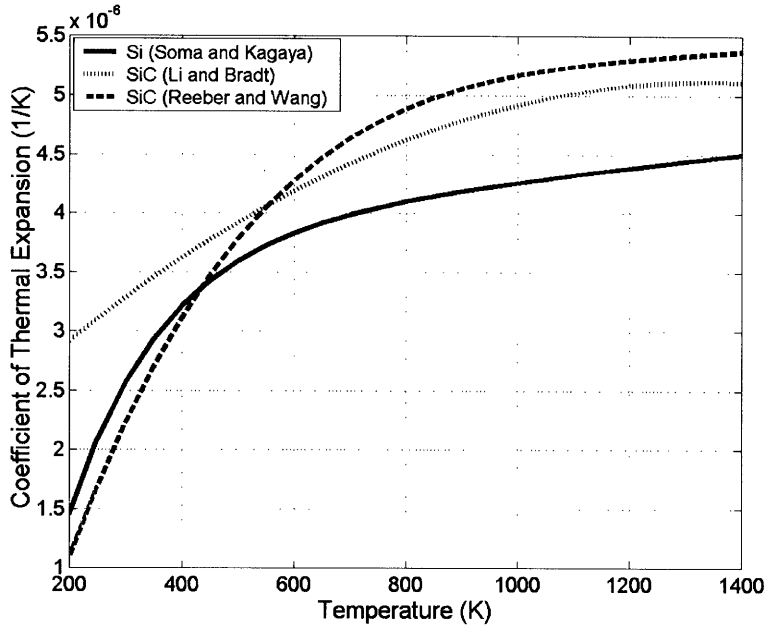


Figure B-1 Thermal expansion coefficients of Si and β-SiC as a function of temperature.

To determine more appropriate CTE data for β-SiC, residual stress calculations were performed using both Equations B-1 and B-2. From the calculations, it has been found that Li and Bradt's curve (B-1) offers more consistent thermal and intrinsic stress values than Reeber and Wang's curve (B-2) based on the modeling. Therefore, Equation B-1 was primarily used for the calculation of a mean CTE of β-SiC. However, as presumed from the plots of residual stresses as a function of test temperature (Figure 4-9), Li and Bradt's equation dose not seem to provide proper CTE values for β-SiC in low temperature ranges below ~500 °C. One interesting point to note is that a maximum in thermal stress was observed at ~150 °C (= 423 K), which corresponds to the minimum point in Figure 4-8 (b). This implies that the CTE values of Si and SiC are equal at this temperature. This interpretation is surprisingly well matched with the intersection between curves B-3 and B-2 (Reeber and Wang) in Figure B-1. Therefore, it appears that following curve B-2 at temperatures up to ~540 K, and then changing to B-1 at higher temperatures would result in more accurate calculation of thermal residual stresses.

References for Appendices

1. K. F. Jensen, "Chemical Vapor Deposition," Advances in Chemistry, Vol. 221, p. 199-263, 1989.
2. J. D. James et al., "A review of measurement techniques for the thermal expansion coefficient of metals and alloys at elevated temperatures," Measurement Science and Technology, Vol. 12, p. R1–R15, 2001.
3. J. Valentich, "A vitreous silica tube dilatometer for the measurement of thermal expansion of solids from –195 to 1000 degrees C," Journal of Materials Science, Vol. 14, No. 2, p. 371-378, 1979.
4. Z. Li and R. C. Bradt, "Thermal expansion and thermal expansion anisotropy of SiC polytypes," Journal of the American Ceramic Society, Vol. 70, No. 7, p. 445-448, 1987.
5. R. R. Reeber and K. Wang, "Lattice parameters and thermal expansion of important semiconductors and their substrates," Materials Research Society Symposium Proceedings, Vol. 622, p. T6.35.1-6.35.6.
6. T. Soma and H.-M. Kagaya, "Thermal expansion coefficient of Si," EMIS Datareviews Series No. 4, p. 33-34, 1988.