A LOW-DRIFT TRANSISTORIZED DIRECT-CURRENT AMPLIFIER

by

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Certified by _____
Thesis Supervisor

Accepted by _____
Chairman, Departmental Committee on Graduate Students

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ABSTRACT

New packaging techniques and new semi-conductor devices are investigated for use in a direct-current amplifier. Three amplifiers are designed and evaluated for use in a servo-loop which switches the amplifier alternately from one load to another.

The first amplifier design evaluates the use of two silicon planar transistors packaged in a single can for a straight d.c. amplifier.

The second amplifier design again utilizes two silicon planar transistors used as switches for a chopper d.c. amplifier.

The last design considers the use of a pair of field-effect transistors in the first stage of a d.c. amplifier.

Thesis Supervisor: Paul E. Gray

Title: Assistant Professor of Electrical Engineering

Acknowledgment

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Chapter I

The Problem

1.1 Introduction

Rapid development in the art of semi-conductor device manufacturing has given the circuit designer new solid state components with greater stability and reliability than was possible only a short time ago. More and more instrumentation and control systems are being constructed with semi-conductor devices as the critical components. Perhaps one of the more difficult problems of instrumentation is the direct current amplifier. It is the purpose of this paper to investigate the newer semi-conductor components available and apply them to the design of a highly stable direct current amplifier.

1.2 The Application

The amplifier will be used in a feedback system which accurately controls the current in an inductive load. Figure 1.1 is a schematic block diagram of this system. To further complicate the matter, the current will be alternately switched from one load to another. A highly stable source such as a standard cell can be used to supply the reference. The sensing resistor can be a high precision, low-drift wire wound resistor. The only other critical component of the system is the amplifier. The problem is that any drift of the amplifier can not be distinguished from signal changes and, therefore, it is desired that the drift of the amplifier referred to the input be less than the smallest signal that the amplifier will see.

1.3 The Specifications

Defining the current in the loop that is being controlled as I_o, total system performance can be expressed:

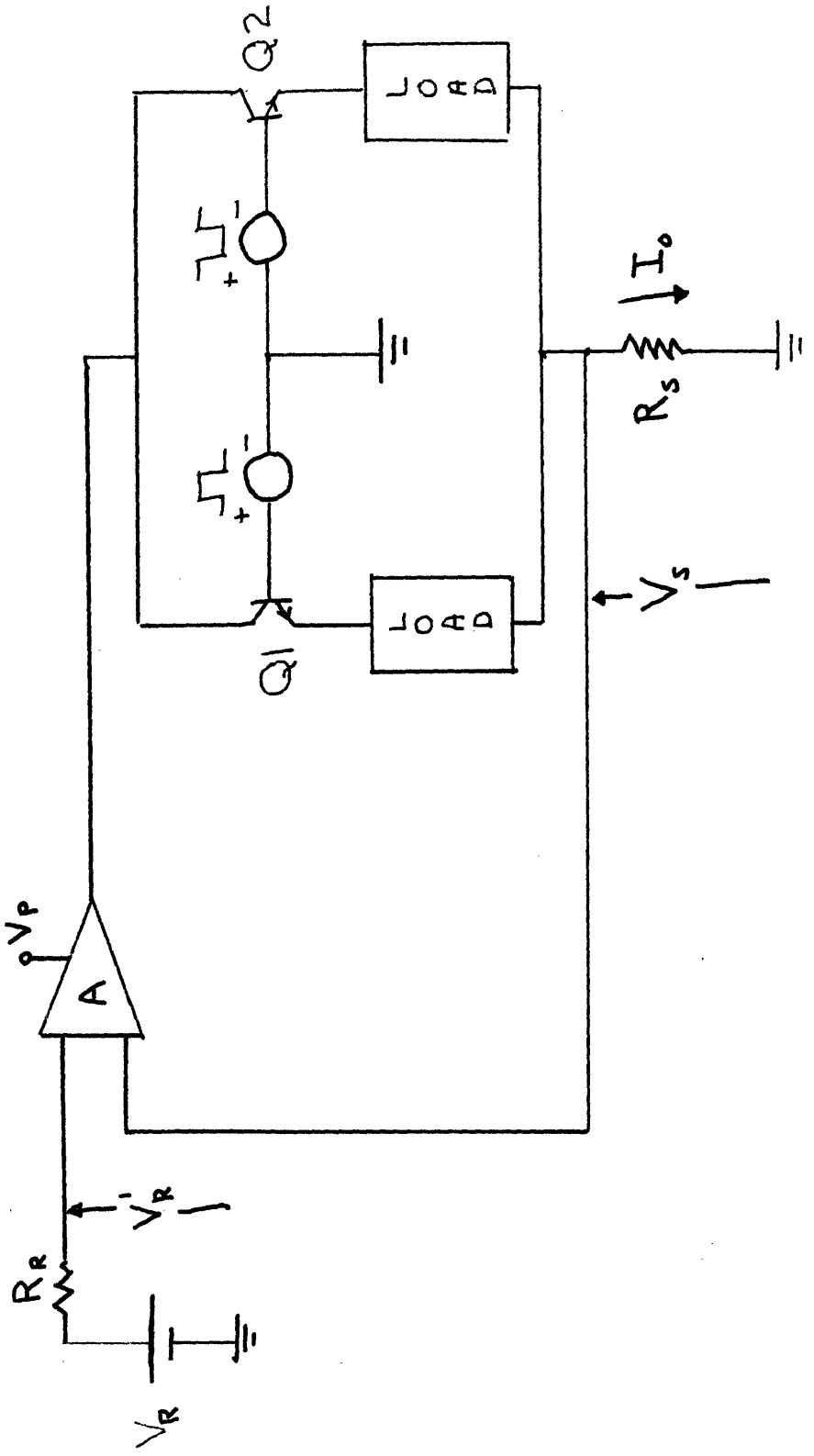

Figure 1.1

$$\frac{\Delta I_o}{I_o} = \text{Stability of controlled current} \qquad (1.1)$$

Referring to Figure 1.1 it is seen that

$$V_s = I_o \frac{R_s R_{in}}{R_s + R_{in}}$$

where R_{in} is the input resistance of the amplifier and since

$$V_e = V_r' - V_s = V_R' - I_o \frac{R_s R_{in}}{R_s + R_{in}}$$

Where V_e is the error voltage at the amplifier input it is seen that the error signal to the amplifier depends upon its input resistance; and also that any change in input impedance will affect the amplitude of I_o.

Defining $\quad R_p = \frac{R_s R_{in}}{R_s + R_{in}}$

the change due to input resistance variations can be found to be

$$\Delta R_p = \frac{R_s^2}{(R_m + R_s)^2} \Delta R_{in}$$

If we assume that $R_{in} >> R_s$, then

$$\Delta R_p = \left(\frac{R_s}{R_{in}}\right)^2 \Delta R_{in}$$

and

$$\frac{\Delta R_p}{R_p} = \frac{R_s}{R_{in}} \frac{\Delta R_{in}}{R_{in}} \qquad (1.2)$$

If we associate an output resistance with the reference a similar analysis can be made. Defining the voltage at the input of the amplifier as V_R', it is seen that:

$$V_R' = \frac{R_{in}}{R_R + R_{in}} V_R$$

and it is found that:

$$\frac{\Delta V_R'}{V} = \frac{R_R}{R_{in}} \frac{\Delta R_{in}}{R_{in}} \qquad (1.3)$$

Solving both equations (1.2) and (1.3) for R_{in}:

$$R_{in} = R_s \frac{\Delta R_{in}/R_{in}}{\Delta R_p/R_p} = R_s \frac{\text{Stability of the input resistance}}{\text{Stability of the sensing resistor}} \qquad (1.4)$$

$$R_{in} = R_R \frac{\Delta R_{in}/R_{in}}{\Delta V_R'/V} = R_R \frac{\text{Stability of the input resistance}}{\text{Stability of the reference}} \quad (1.5)$$

These equations will be used to determine input resistances necessary in the designs that follow.

For the present, consider the two transistor switches in Figure 1.1 to be ideal. Then, for either switch position the following block diagram is a valid representation of the system.

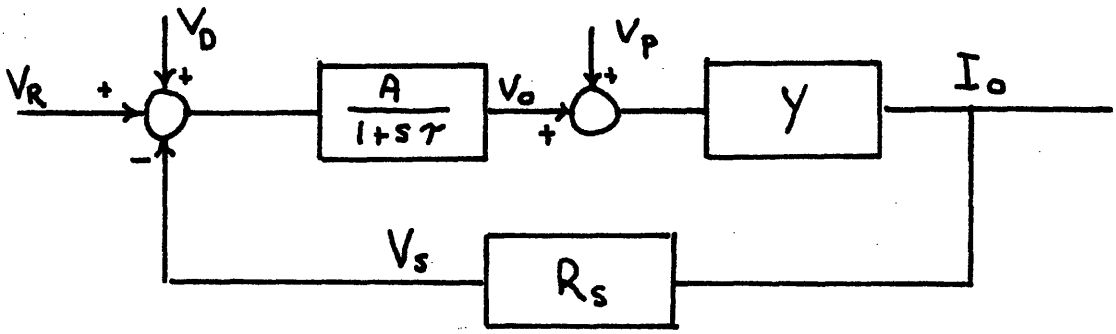

Figure 1.2

Where the parameters are as follows:

V_R the reference voltage

V_s the feedback voltage developed across the feedback resistor

V_o the output voltage of the amplifier

V_p the supply voltage

V_D the drift referred to the input of the amplifier

Y the total admittance of the load and the sensing resistor

R_s the sensing resistor

I_o the controlled load current

A the voltage gain of the amplifier

τ the significant break-point of the amplifier

The only inputs to the system are the voltage reference, amplifier drift, and power supply variations. Dynamic performance of the loop would depend only on power supply variations and switching. Now if the switches are not considered ideal and have saturation voltages that are different and if the load in both switch legs is different, then switching will cause a step voltage change across these elements. In terms of dynamic performance, the effect on I_o is the same as for a step change in V_p. If switching transients are neglected, the block

diagram of Figure 1.2 will hold for the switching system with V_p containing variations due to mismatching of loads and switches. From the block diagram of Figure 1.2 the following relationships hold:

$$\frac{I_o(s)}{V_p(s)} = \frac{Y}{1 + \frac{AR_sY}{1 + s\tau}} = \frac{Y}{1 + AR_sY} \frac{s\tau + 1}{\frac{s\tau}{1 + AR_sY} + 1}$$

$$\frac{I_o(s)}{V_p(s)} = \frac{Y}{K} \frac{s\tau + 1}{\frac{s\tau}{K} + 1} = Y \frac{s + 1/\tau}{s + K/\tau} \tag{1.6}$$

where $K = 1 + AR_sY$

Considering $V_p(s)$ to be a step voltage of magnitude V_m, $I_o(s)$ is found to be:

$$I_o(s) = \frac{YV_m}{K} \left[\frac{1}{S} - \frac{(1 - K)}{S + K/\tau}\right] \tag{1.7}$$

and finding the inverse LaPlace transform leads to:

$$i_o(t) = \frac{V_mY}{K}[1 - (1-K)e^{-K/\tau t}]$$

Assume that $AR_sY >> 1$ then:

$$i_o(t) = \frac{V_m}{AR_s} [1 + AR_sYe^{-K/\tau t}] \tag{1.8}$$

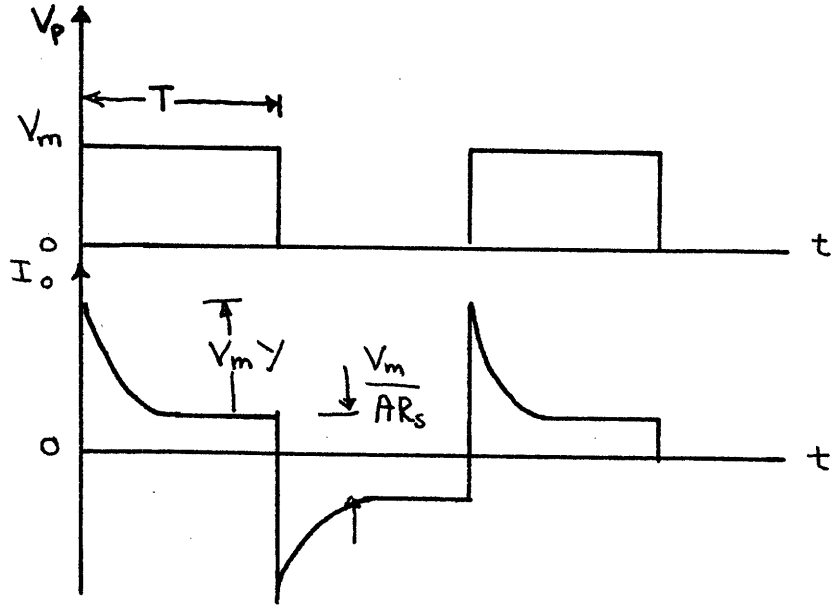

Figure 1.3

The transients shown in Figure 1.3 are added to the constant steady state value of I_o and for symmetrical switching the average value of these transients is zero. Since the possibility for unsymmetrical switching does exist an attempt will be made to minimize the error due to this transient over one period T. From Figure 1.3 the following definitions are made:

$$I_{o.s.} = \frac{V_m}{AR_s} = \text{Offset current}$$

$$I_e = V_m Y = \text{Peak transient current}$$

Then the average current over one period is:

$$I_{av} = I_o + I_{os} + \frac{1}{T}\int_0^T I_e e^{\frac{-K}{\tau}} dt$$

$$I_{av} = I_o + I_{os} + \frac{I_e}{T}\frac{\tau}{K}\left(1 - e^{\frac{-K}{\tau}T}\right)$$

For $T \gg \tau$

$$I_{av} = I_o + I_{os} + \frac{I_e}{T}\frac{\tau}{K} \qquad (1.9)$$

If the current to be controlled is 100 m.a. and the total offset is 1 microamp, the gain can be solved for. (Knowing the other parameters). Considering the known characteristics of the system, V_m can be as much as 24 volts. With $R_s = 60$ ohms and $Y = \frac{1}{800}$ the gain is found to be:

$$A = \frac{V_m}{I_{o.s}R_s} = \frac{24}{1 \times 10^{-6} \times 60} = .4 \times 10^6 = 400{,}000$$

Allowing the average error for the transient also to be 1 microamp, the time constant τ can be found from equation (1.9).

$$\tau = \frac{KT}{I_e} I_{av}\ \text{error} = \frac{AR_s YT}{I_e} I_{av}\ \text{error}$$

for $T = 500$ micro seconds

$$I_e = 24 \times \frac{1}{800} = 30 \text{ m.a.}$$

$$\tau = 5 \times 10^{-4}$$

so that the break frequency of the amplifier should be at $f_b = 314$ cps.

The previous results were determined by assuming that the transistor switches are ideal and that they switch simultaneously. This assumption is not exactly true. The effects of non-ideal switching will be discussed in a later section.

Chapter II

The Conventional D.C. Amplifier

2.1 Difficulties of D.C. Amplifier Design

The design of transistorized d-c amplifiers has proven difficult due to the variations in transistor parameters. The major cause of variation is temperature with secondary effects caused by the drift with time of these parameters. The critical parameters in a transistor are the base to emitter voltage (V_{BE}), the collector to base leakage current (I_{CBO}), and the d-c beta (h_{FE}). In a transistor amplifier, any drift of these parameters produces outputs which can not be distinguished from outputs caused by a signal change at the input.

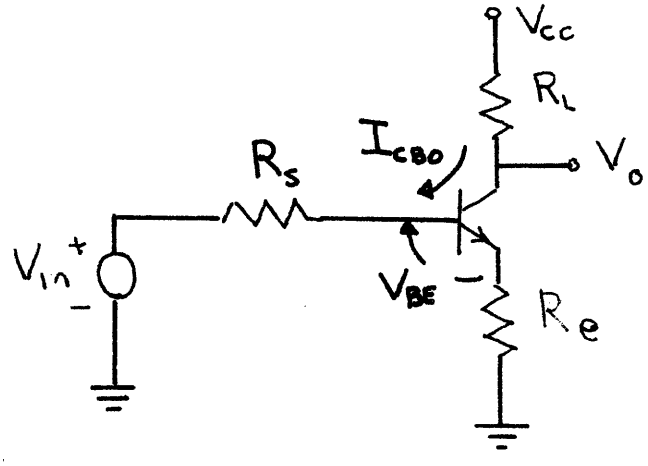

Figure 2.1

Figure 2.1 is a schematic of a single stage amplifier. As shown in Appendix A, analysis of this stage leads to the following expression.

$$V_o = V_{cc} - \frac{h_{FE}R_L}{\Delta} V_{in} + \frac{h_{FE}R_L}{\Delta} V_{BE} + \frac{h_{FE}R_sR_L}{\Delta} I_{CBO} - I_{CBO} R_L \qquad (2.1)$$

Where $\Delta = R_s + (1 + h_{FE}) R_E$

In equation (2.1) V_{CC}, V_{BE}, I_{CBO}, and h_{FE} have been treated as independent variables. As a first order approximation, so as to understand the effects of the various transistor parameters, this assumption is valid. V_{BE}, h_{FE}, I_{CBO} depend primarily upon the base current, junction temperature and ambient temperature. For the silicon planar transistor the effect of I_{CBO} is negligible (typically less than 10^{-8} amperes) compared to the other parameters so that it will be neglected for all further analysis. Over small variations of base current h_{FE} can be considered essentially constant. For the transistors studied in this paper, doubling the base current changes h_{FE} by 10% at 25°C. Over a limited range V_{BE} can be expressed as a linear function of the base current, where $V_{BE} = R_{BE} I_B$. If the dependency of V_{BE} is inserted into equation (2.1) then $\Delta = R_s + R_{BE} + (1 + h_{EE})R_E$. For the transistors tested R_{BE} is found to be about 2.5 K ohms. for a base current of 15 microamps. The temperature variation of V_{BE} and h_{FE} at around room temperature is large enough to cause large error voltages at the output. One other deficiency of this circuit is the need for a well-stabilized power supply.

2.2 The Differential D.C. Amplifier

The shortcomings of the single-ended amplifier stage can be reduced considerably by use of the Slaughter circuit. Figure 2.2 is a schematic representation of this circuit. The analysis is

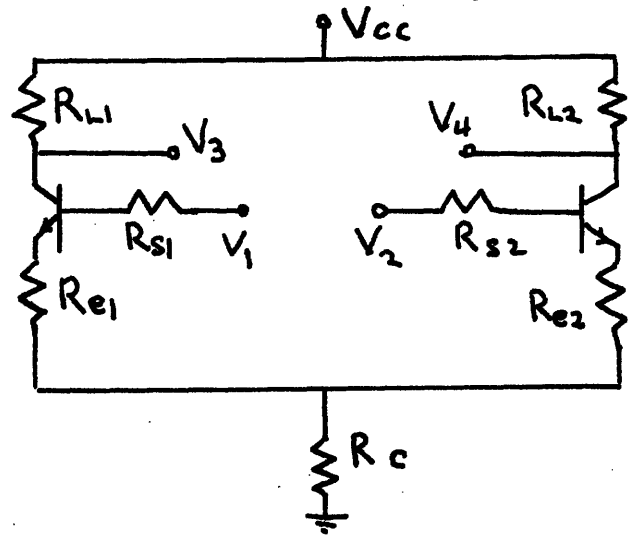

Figure 2.2

developed in Appendix A with the following result:

$$V_o = V_3 - V_4 = \frac{-h_{FE1} R_{L1}}{\Delta R_{S1}} \left[1 + \frac{R_c + R_{e2}}{R_{S2}} (1 + h_{FE2})\right](V_1 - V_{BE1})$$

$$+ \frac{h_{FE2} R_{L2}}{\Delta R_{S2}} \left[1 + \frac{R_c + R_{e1}}{R_{S1}} (1 + h_{FE1})\right](V_2 - V_{BE2})$$

$$+ \frac{h_{FE1}(1 + h_{FE2}) R_c R_{L1}}{\Delta R_{S1} R_{S2}} (V_2 - V_{BE2}) - \frac{h_{FE2}(1 + h_{FE1}) R_c R_{L2}}{\Delta R_{S1} R_{S2}} (V_1 - V_{BE1}) \quad (2.3)$$

where

$$\Delta = 1 + \frac{R_c + R_{e1}}{R_{S1}} (1 + h_{FE1}) + \frac{R_c + R_{e2}}{R_{S2}} (1 + h_{FE2})$$

$$+ \frac{R_{e1}}{R_{S1}} (1 + h_{FE1})\left[\frac{R_c + R_{e2}}{R_{S2}} (1 + h_{FE2})\right] + \frac{R_c R_{e2}}{R_{S1} R_{S2}} (1 + h_{FE1})(1 + h_{FE2}) \quad (2.4)$$

Equations (2.3) and (2.4) are nearly exact; the only approximation made is the neglecting of the output impedances of the transistors. The output impedance is normally about 50K ohms for the transistors used in the common-emitter configuration. Again, V_{BE} and h_{FE} have been chosen as independent parameters so that their effects on amplifier performance are placed in evidence. Assuming that $R_{L1} = R_{L2} = R_L$, $R_{S1} = R_{S2} = R_S$, $R_{e1} = R_{e2} = R_e$, and $h_{FE} \gg 1$ then equation (2.3) reduces to:

$$V_o = \frac{2h_{FE1} h_{FE2} R_c R_L}{\Delta R_S^2} (V_2 - V_1) + \frac{2h_{FE1} h_{FE2} R_c R_L}{\Delta R_S^2} (V_{BE1} - V_{BE2})$$

$$+ \frac{h_{FE1} h_{FE2} R_e R_L}{\Delta R_S^2} (V_2 - V_1) + \frac{h_{FE1} h_{FE2} R_e R_L}{\Delta R_S^2} (V_{BE1} - V_{BE2})$$

$$+ \frac{R_L}{\Delta R_S} (h_{FE2} V_2 - h_{FE1} V_1) + \frac{R_L}{\Delta R_S} (h_{FE1} V_{BE1} - h_{FE2} V_{BE2}) \quad (2.5)$$

A study of equation (2.5) reveals that if $V_{BE1} = V_{BE2}$ and $h_{FE1} = h_{FE2}$ and if the rate of change of these parameters with respect to temperature is also equal, then the effects of these parameters have canceled. This is due to the differential action of the amplifier. Even if these parameters are not perfectly matched, it is reasonable to expect that temperature effects have been greatly reduced. Power supply variations have completely

canceled out. Use of this type of amplifier connection has eliminated the undesired characteristics of the single-ended amplifier.

Further approximations to equations (2.4) and (2.5) will point out useful facts necessary to the design of a differential amplifier. Assuming that $R_c >> R_s$, $R_c >> R_e$, $V_{BE1} = V_{BE2}$, then equations (2.4) and (2.5) can be combined and reduced to:

$$V_o = \frac{2h_{FE1}\, h_{FE2}\, R_L\, (V_2 - V_1)}{(h_{FE1} + h_{FE2})\, R_S + 2h_{FE1}\, h_{FE2}\, R_e} \tag{2.6}$$

If the transistors are perfectly balanced so that $h_{FE1} = h_{FE2} = h_{FE}$, then

$$V_o = \frac{h_{FE}\, R_L}{R_S + h_{FE}\, R_e}\ (V_2 - V_1) \tag{2.7}$$

which is the expression for the voltage gain of the differential amplifier stage. If, however, $R_s = R_e = 0$ then it would appear that the voltage gain goes to infinity. As found in the analysis of the single-ended stage, this result appears because of the assumption that V_{BE} is independent of the input. Appendix A shows the effect of considering the dependency of V_{BE} upon the input. Considering this, it is found that

$$V_o = \frac{h_{FE}\, R_L\, (V_2 - V_1}{R_{BE} + R_S + h_{FE}\, R_e} \tag{2.8}$$

where R_{BE} is still defined as in section 2.1.

Another important measure of quality of a differential amplifier is its common-made rejection (CMR). The output, as previously defined, is taken between the collectors. One form of unwanted signal or noise is the signal that appears simultaneously at both inputs. This signal may be due to pickup through stray wiring capacity, or appear due to power supply variations or to a number of other reasons. If there are unbalances in the amplifier, an output voltage will occur. The output terminals have no way of distinguishing this signal from a wanted signal and therefore the unwanted signal should be as small as possible. CMR can be defined as the ratio of the gain A_c of the amplifier with the input signals equal and apposite (differential signal), to the gain A_d of the amplifier with the input signals equal and of the same polarity. So that for equation (2.3) with variations due to V_{BE} ignored and all symmetrical resistors matched:

$$CMR = \frac{A_D}{A_{CM}} = \frac{(h_{FE1} + h_{FE2})(R_S + R_e + 2R_c) + 4h_{FE1}\, h_{FE2}\, R_c}{(h_{FE2} - h_{FE1})(R_e + R_S)}$$

and assuming that $h_{FE} \gg 1$ then

$$CMR = \frac{4h_{FE1}\, h_{FE2}\, R_c}{(h_{FE2} - h_{FE1})(R_e + R_S)} \qquad (2.9)$$

The higher the common mode rejection, the better the amplifier will reject common made signals. Ideal matching of h_{FE}'s will give the best performance but for the non-ideal case, the larger R_c, the better the common mode rejection.

2.3 Drift in a D.C. Differential Amplifier

Drift in an amplifier can be divided into two categories; random and predictable. The latter can be traced to the variation of known parameters such as temperature and power supply. Once the limits of these disturbances are known, drift performance of any amplifier can be easily determined. Random drift can not be determined in advance; it is a function of parameters that vary in a manner difficult to describe.

It has been pointed out in section 2.2 that use of a differential mode of amplification reduces the effects of drift considerably. Equation (2.5) indicates that if both h_{FE} and V_{BE} were to have the same rate of drift and if both values were matched for a particular pair of transistors then surely the effects of these parameters would cancel. The problem that exists is how to achieve this matching. Fairchild Semiconductor Corporation has come close to solving this problem. Instead of trying to match two transistors from one or more production runs, they choose their matched transistors before they are even placed on a header. This selection consists of taking the silicon dice from the same slab of the production run. The planar technique of diffusion allows the transistors to be selected before encapsulation in a transistor package. After the units have been selected they are both mounted on the same header and sealed in the can with six leads coming to the outside. The units are electrically isolated. Clearly, thermal gradients between transistors are kept to

a minimum by this technique if the transistors are operated symmetrically so that internal heating may be neglected. Also, it is hoped that drifts of the transistor parameters due to aging will be in the same direction.

For the purpose of this paper, three matched units type FSP-2 were obtained from Fairchild. No specifications other than those listed in Appendix C were asked for. Performance tests to determine the devices stability with temperature and time were conducted. Experimental determination of some parameters of signifigance were also determined. The results of these tests will be discussed in later sections.

2.4 Practical Design of the Differential D.C. Amplifier

Figure 2.3 is a schemetic of a three stage differential amplifier. Each pair of transistors is a FSP-2.

In the first stage the common resistor has been replaced by transistor Q5 with its associated circuitry. The zener diode in the base circuit of Q5 assures that nearly constant collector current flows. Therefore, Q5 is operated in the common base mode, causing its output impedance to be high and as has been shown this will improve the common mode rejection. The collector resistors are ±1% tolerance low temperature coefficient resistors with their values chosen so that 10 volts appears at each collector when 1 milliamp of collector current flows. This current was chosen to take advantage of the higher h_{FE} at this value and to keep the load impedance of this stage from being too large. Generally, it is true that the noise should be a minimum at a lower current, but the tests later showed that noise was not a significant factor. A potentiometer is used to balance out any mismatches in the circuit. Under operating conditions, the voltage at inputs 1 and 2 is 6 volts and the output voltage is 85 volts. This neccessitates raising the voltage level at each successive stage.

The second stage design is similar to the first with the exception that emitter resistors are used so that loading of the first stage is not too large and a resistor is used for the emitter coupling.

The third stage converts the differential signal to a single-ended signal by taking the output only at the collector of Q6 and shorting out the resistor in the collector circuit of Q5.

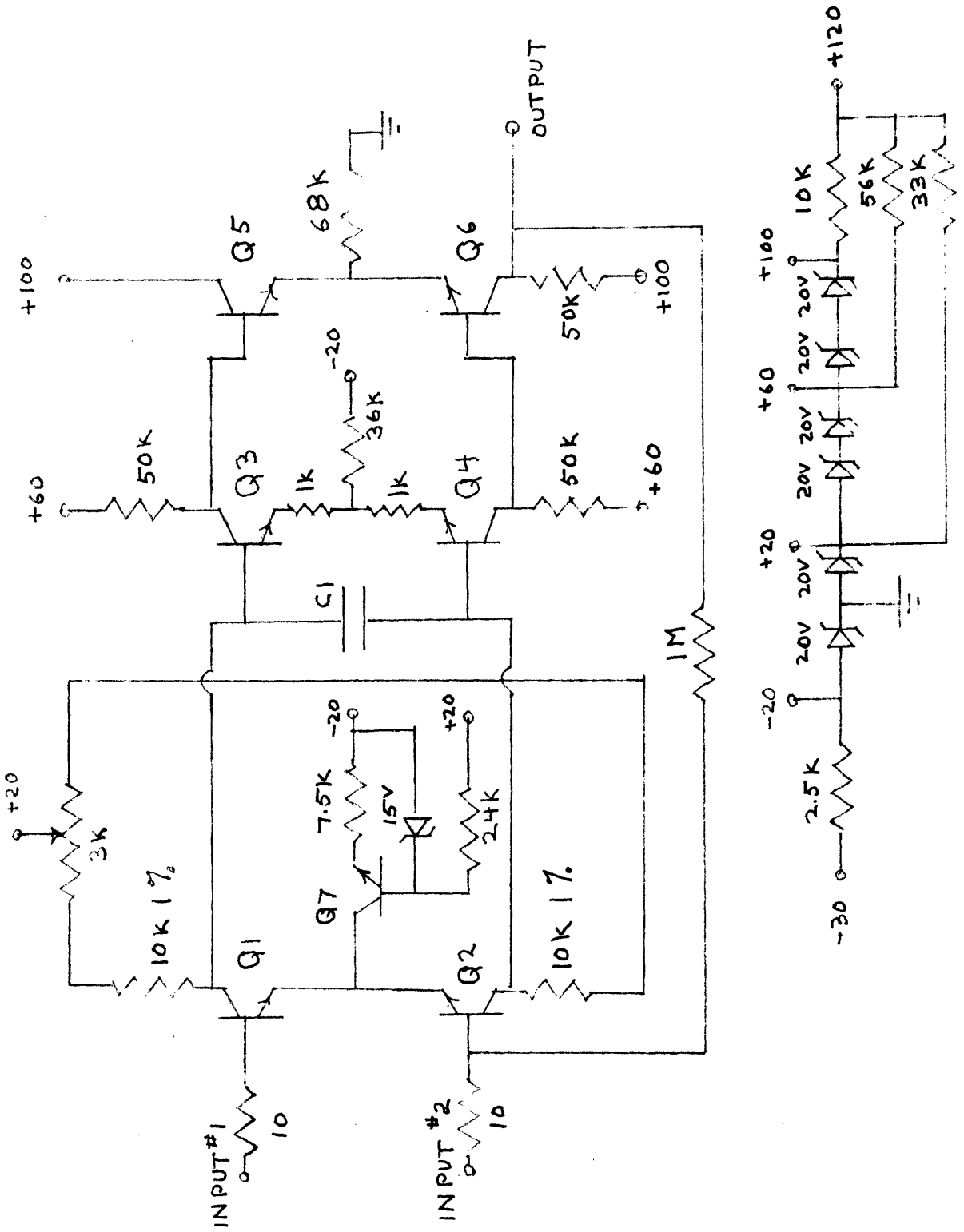
+120
+100
+60
+20
-20
-30
10K
56K
33K
20V
2.5K
OUTPUT
68K
Q5
Q6
50K
-20
36K
Q3
1K
Q4
C1
1M
+20
3K
10K 1%
Q1
7.5K
15V
Q7
24K
Q2
INPUT #1
INPUT #2
10

Figure 2.3

The supply voltages are all taken from a tapped, zener regulated supply. The addition of the zener diodes further helps to regulate the voltages supplied to each stage.

Capacitor C1 is provided to limit the upper cut-off frequency and its effect will be discussed in a later section.

Feedback is incorporated in the amplifier in order to lower the gain to the value determined in the specifications. Feedback also helps to accomplish closed loop stability and to limit the effect of h_{FE} variations on gain from unit to unit.

2.5 Temperature Effects on the First Stage

Tests to determine temperature dependency were run so that performance of the FSP-2 transistors could be evaluated. The results of the tests also were studied to see if transistor performance could be estimated by simple test procedures.

Temperature control was accomplished by use of a Delta Temperature Chamber that can control to 1° Centigrade. The use of liquid CO_2 to cool the chamber quickly allowed tests to be run in a short time at temperatures below ambient as well as at elevated temperature. The output of the first stage was monitored using a Hewlett Packard Microvolt ammeter.

Figure 2.4 is a graph of the output variation as a function of temperature for the three FSP-2's. The voltage gain of the stage varies from 295 to 310 for the three units. Unit 2 has a temperature coefficient, referred to the input of this amplifier, of only 8.16 microvolts/°C. at 27°C. It also shows the most linear variation over this range. Units 1 and 3 exhibit greater temperature coefficients at 27°C but at higher temperatures there are bands where the coefficient is less than that of unit 2. There are marked differences in the three transistor-pairs. A graph of the base characteristics is shown in Figure 2.5 a, b, c. The base to emitter voltage of unit 1 follow very closely, except at high base currents. At high base currents there is a heating of the transistors due to the large collector currents flowing. This should cause a change in V_{BE} at the rate of about -2mv per °C. The change is evident in the dropping off of the curves. Since the h_{FE}'s are not perfectly matched, the power

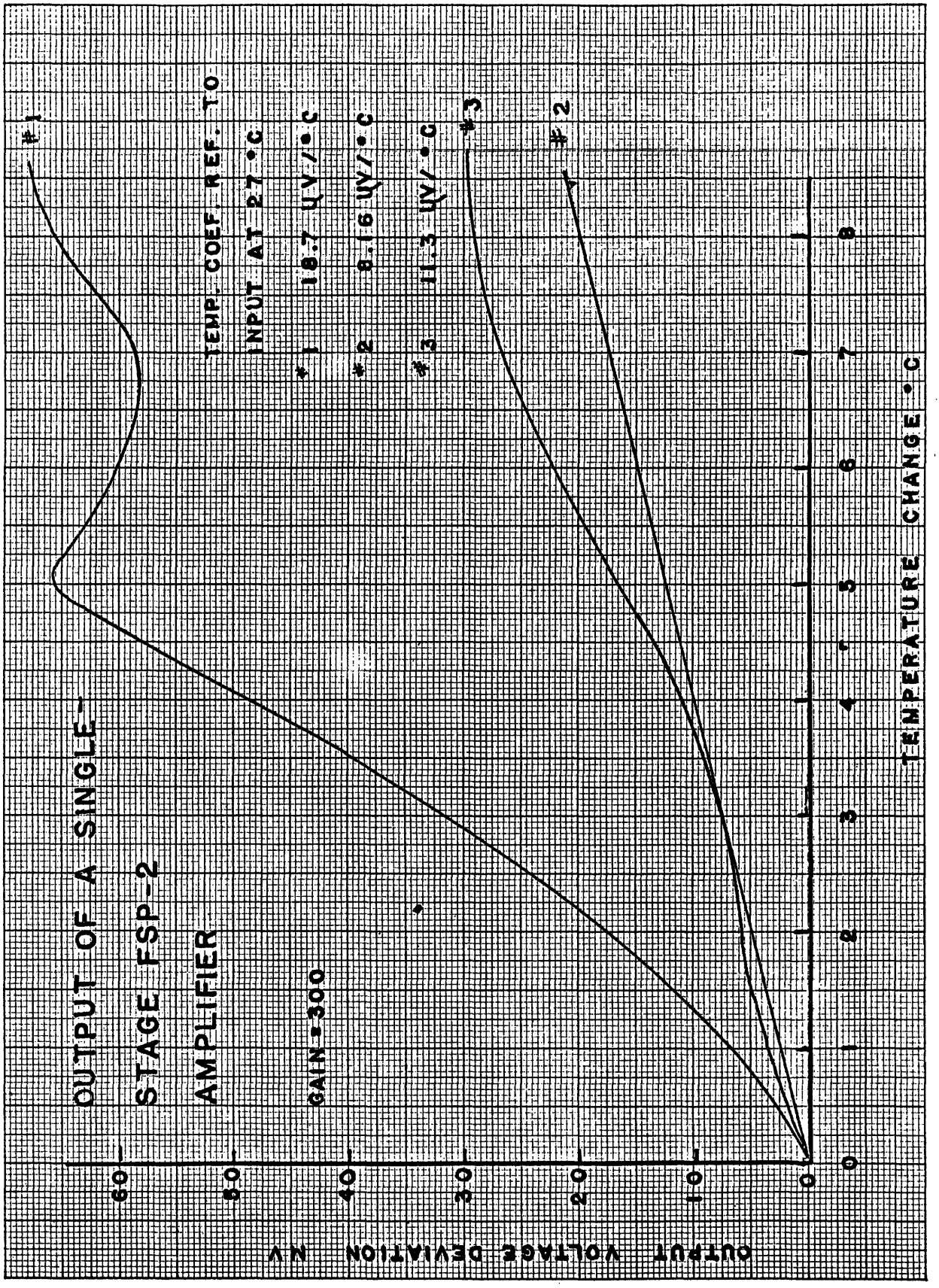
OUTPUT OF A SINGLE-STAGE FSP-2 AMPLIFIER
GAIN = 300
TEMP. COEF. REF. TO INPUT AT 27 °C
#1 18.7 µV/°C
#2 8.16 µV/°C
#3 11.3 µV/°C
#1
#2
#3
OUTPUT VOLTAGE DEVIATION MV
-60
-50
-40
-30
-20
-10
0
0
1
2
3
4
5
6
7
8
TEMPERATURE CHANGE °C

Figure 2.4

BASE CHARACTERISTICS
OF FSP-2 NO. 1
VCE = 10 V, T = 28°C
hFE1 = 71.8 hFE2 = 77
#3
#25
BASE VOLTAGE MV
-800
-600
-400
-200
0
BASE CURRENT UA
100
10
1
.1

Figure 2.5a

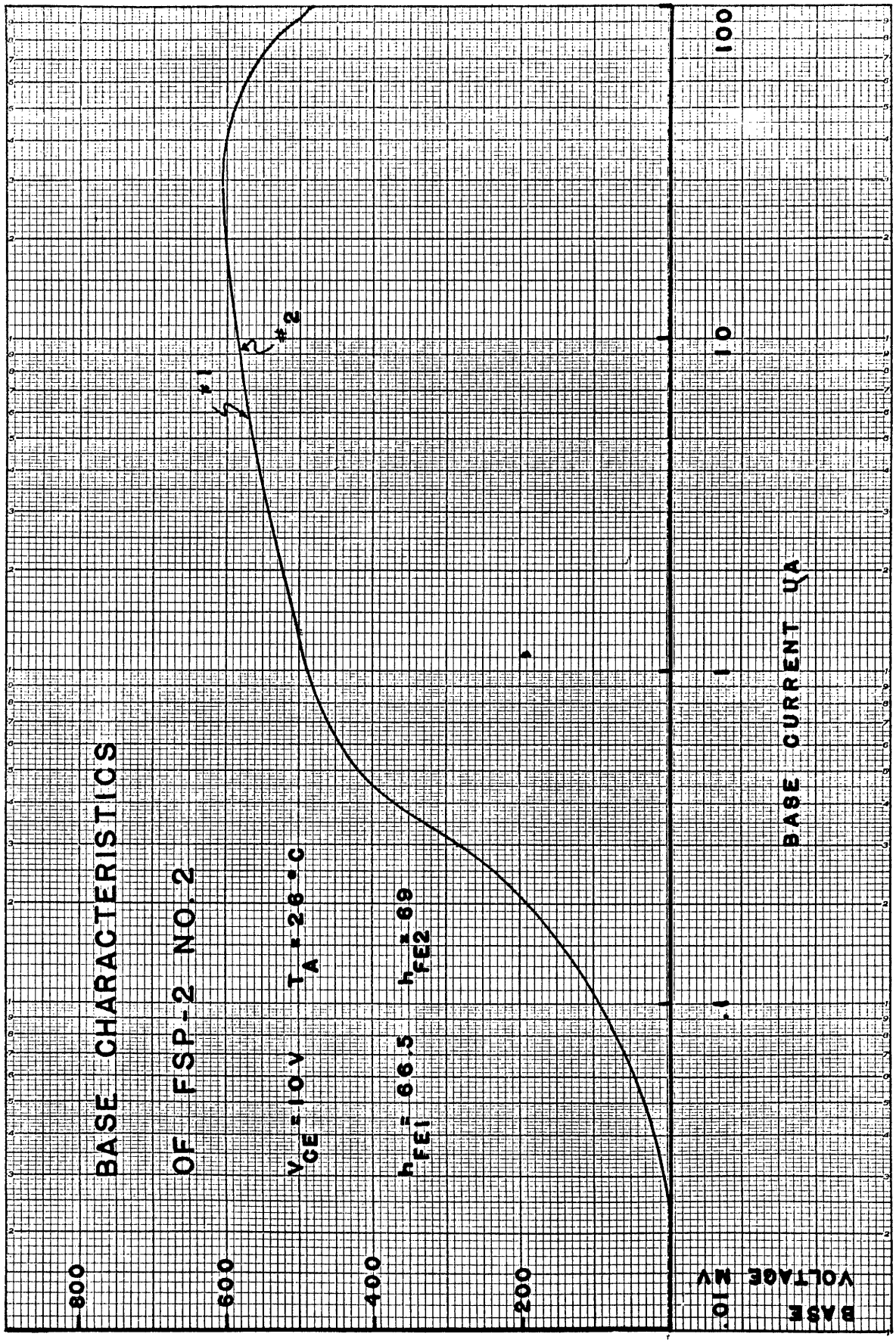
BASE CHARACTERISTICS
OF FSP-2 NO. 2
V_{CE} = 10 V
T_A = 26 °C
h_{FE1} = 66.5
h_{FE2} = 69
#1
#2
BASE VOLTAGE MV
800
600
400
200
.01
.1
1
10
100
BASE CURRENT UA

Figure 2.5b

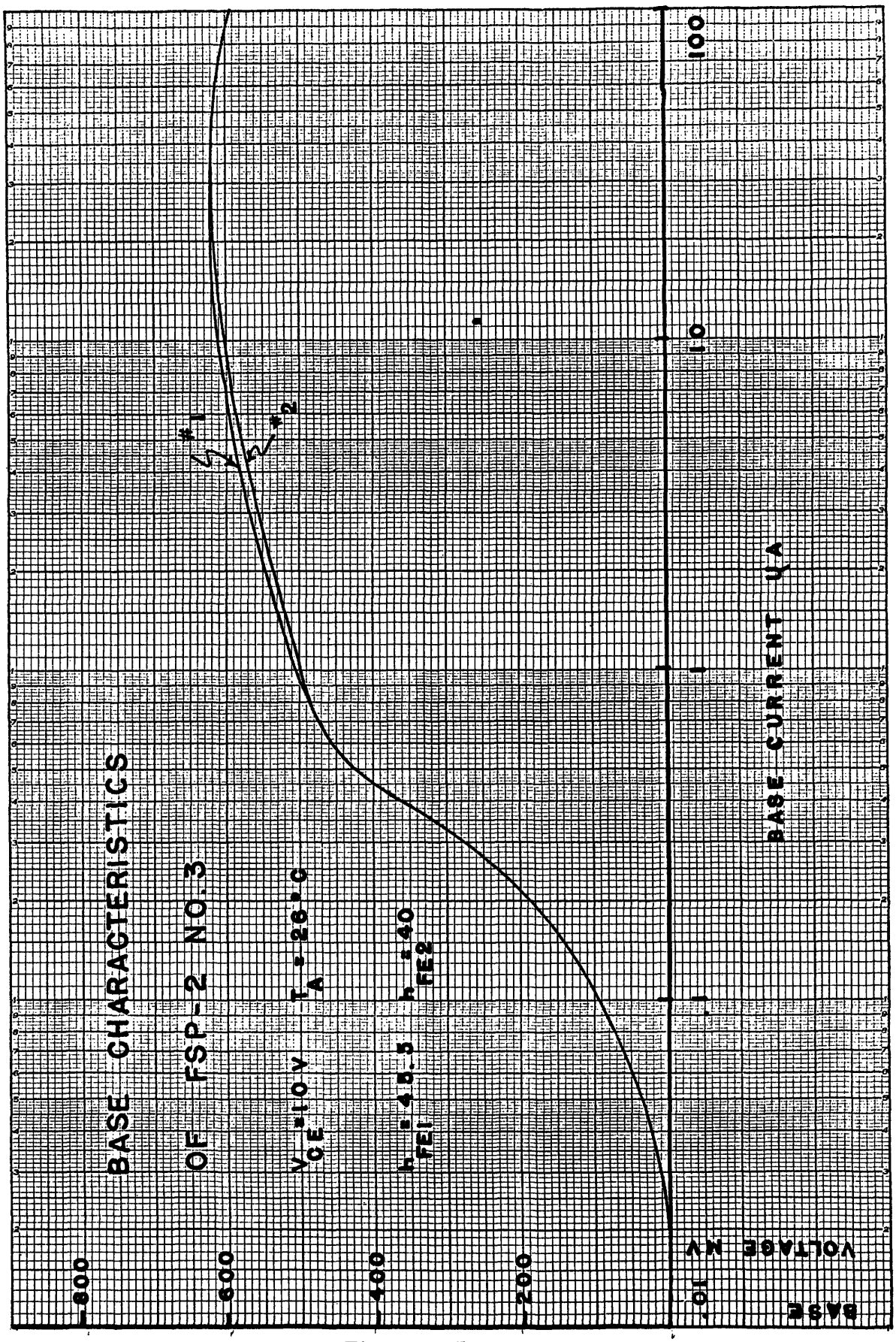
BASE CHARACTERISTICS
OF FSP-2 NO. 3
VCE = 10 V TA = 26°C
hFE1 = 45.5 hFE2 = 40
#1
#2
BASE VOLTAGE MV
800
600
400
200
10
100
1
10
BASE CURRENT UA

Figure 2.5c

dissipated in the transistors is not equal due to the different collector currents. This would cause some of the mismatch, but it is believed that the greatest contributing factor is $\frac{\Delta V_{BE}}{\Delta T}$. Neither unit 2 nor 3 has its h_{FE}'s exactly matched, but the V_{BE} differential does not occur at higher base currents. Unit 2 appears to be matched very closely over all base currents. It is also true that this unit had the best temperature coefficient. Unit 3 is poorly matched between 1 and 30 microamps. These data would suggest that unit 2 had the best-matched characteristics, and this was borne out by previous tests.

Figures 2.6a, b, c show the variation of V_{BE} as a function of temperature at a constant base current and collector voltage. There is very close agreement for all three units. Unit 3 is the only one showing any marked differences.

2.6 Performance of the Amplifier

With the amplifier operating open loop, data would be hard to obtain because of the high gain. The voltage gain of the amplifier is greater than 1 million and therefore feedback is used to lower the gain so that measurements may be made more easily. Figure 2.7 [1] shows diagrammatrically one test setup that was used. The amplifier was connected as a gain of 10,000 amplifier. One volt output drift on the recorder was referred to

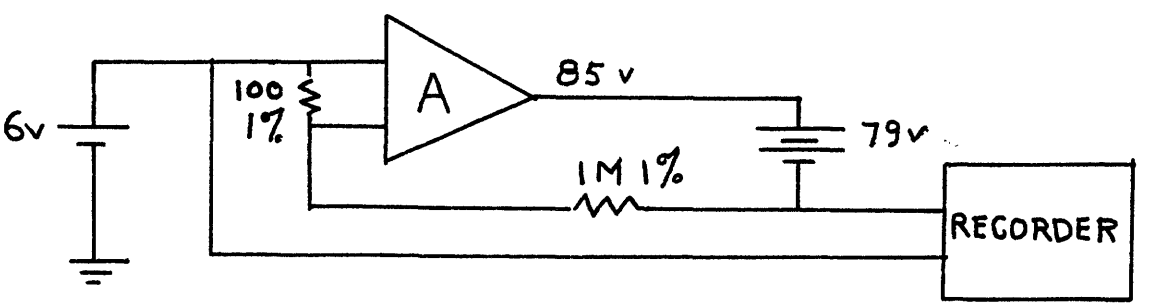

Figure 2.7

the input of the amplifier as an equivalent input drift signal. The 79 volt battery was used to step the voltage down so that the quiescent voltage at the input was zero for the output adjusted to 85 volts. Stable 1% resistors were used to minimize error due to these components. The

[1] Test circuit devised by G. Rubissow of the MIT Instrumentation Laboratory

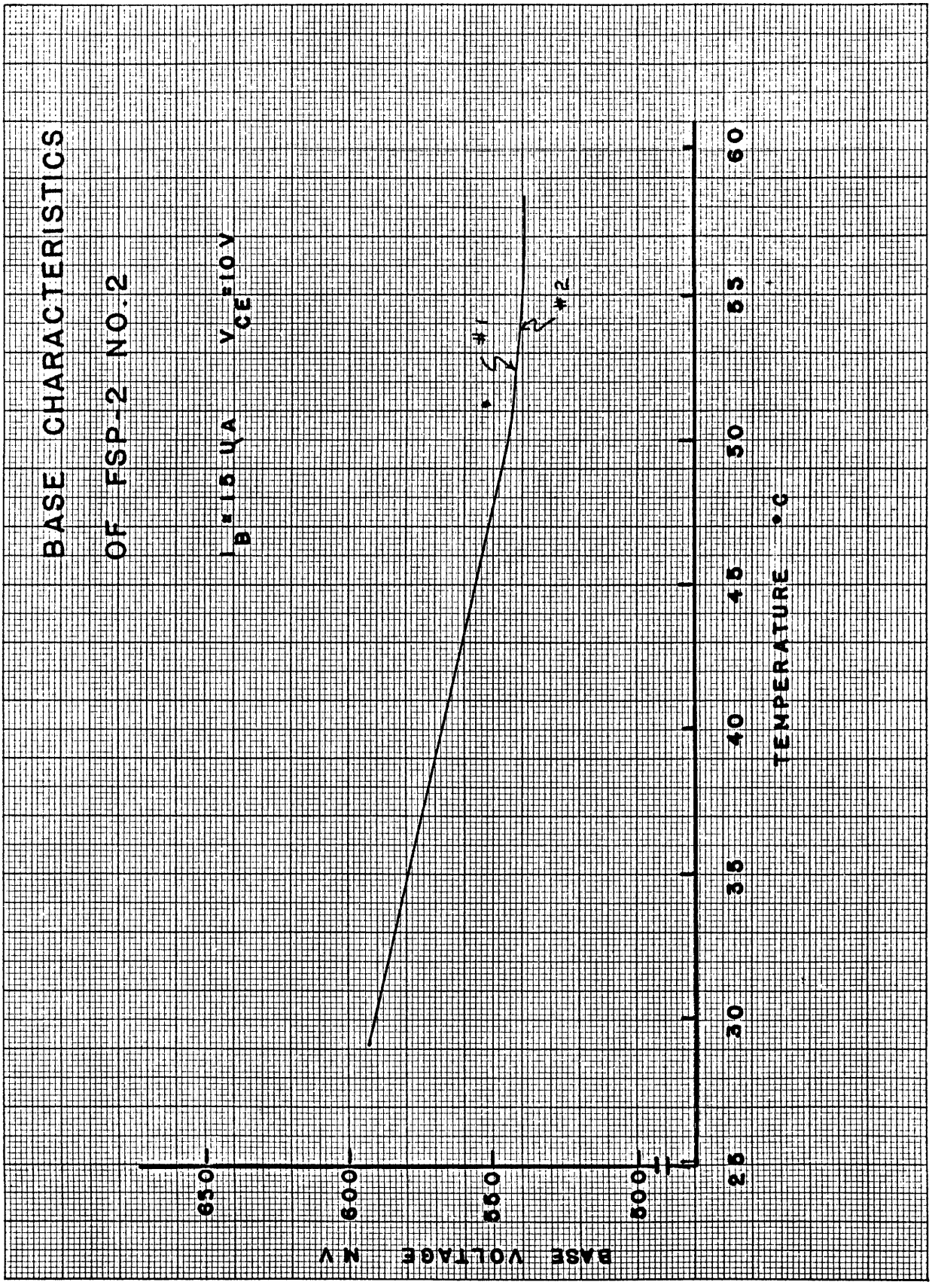

Figure 2.6a
-28-

BASE CHARACTERISTICS
OF FSP-2 NO I
I_B = 15 μA
V_{CE} = 10 V
BASE VOLTAGE MV
600
550
500
25
30
35
40
45
50
55
60
TEMPERATURE °C

Figure 2.6b

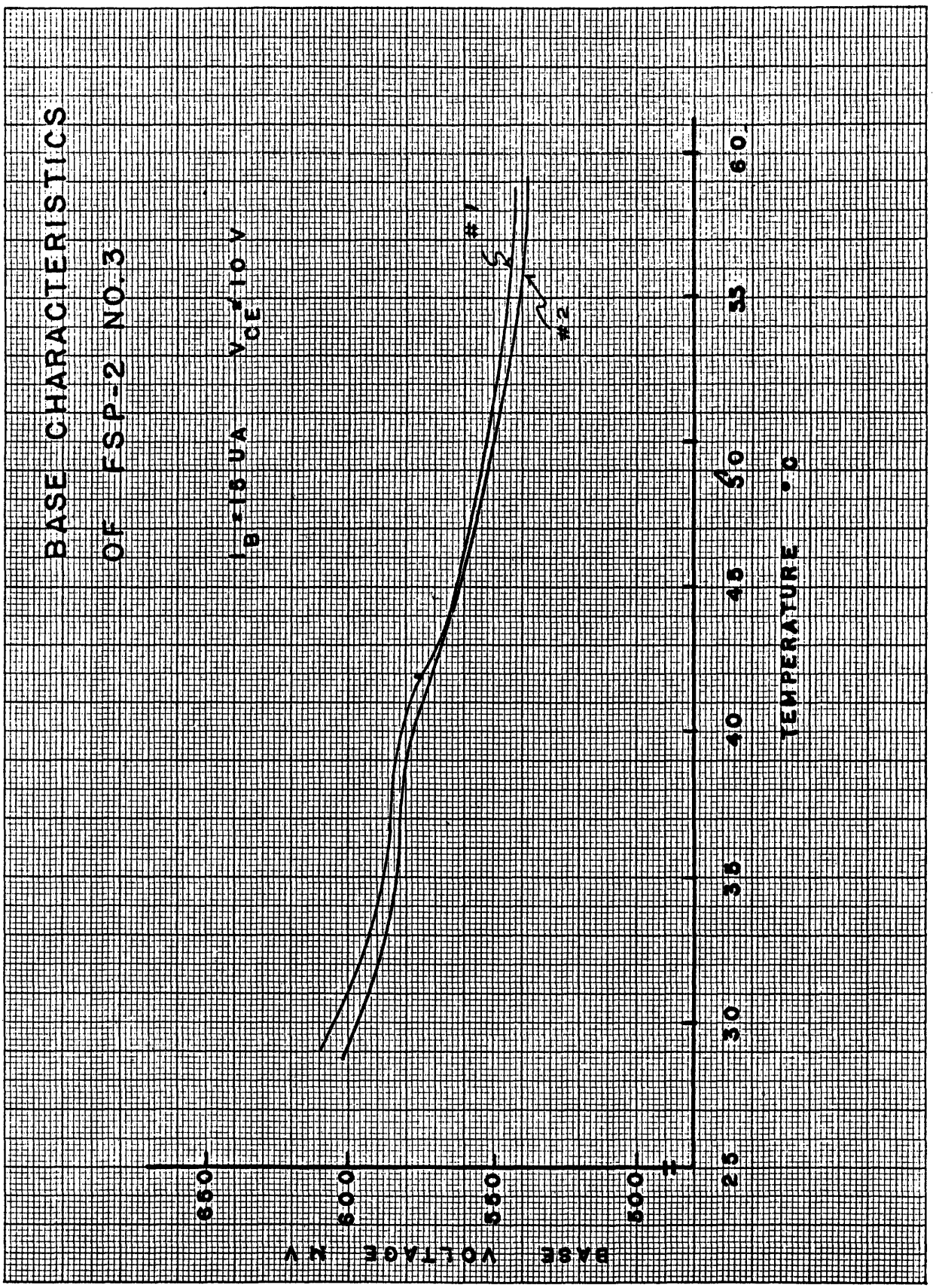
BASE CHARACTERISTICS
OF FSP-2 NO.3
I_B=18 UA
V_{CE}=10 V
#1
#2
BASE VOLTAGE MV
800
600
500
400
300
TEMPERATURE °C
25
33
40
45
50
60

Figure 2.6c

six volt battery was a standard cell. With unit 2 in the first stage, the temperature drift of the amplifier is shown in Figure 2.8. The drift was in close agreement with the expected drift of the first stage alone.

For power supply variations of ±10%, the worst off-set occurred when both the +120 volt supply and the -30 volt supply decreased to +108 volts and -27 volts. The variation referred to the input was 75 microvolts.

Tests for frequency response and long-time drift were taken in the test setup of Figure 2.9. This is the system loop without switching and also operating at lower power levels. The current being controlled is 12 milliamps. Over a fifteen hour period, the peak to peak drift was less than 10 microvolts with the amplifier at constant temperature.

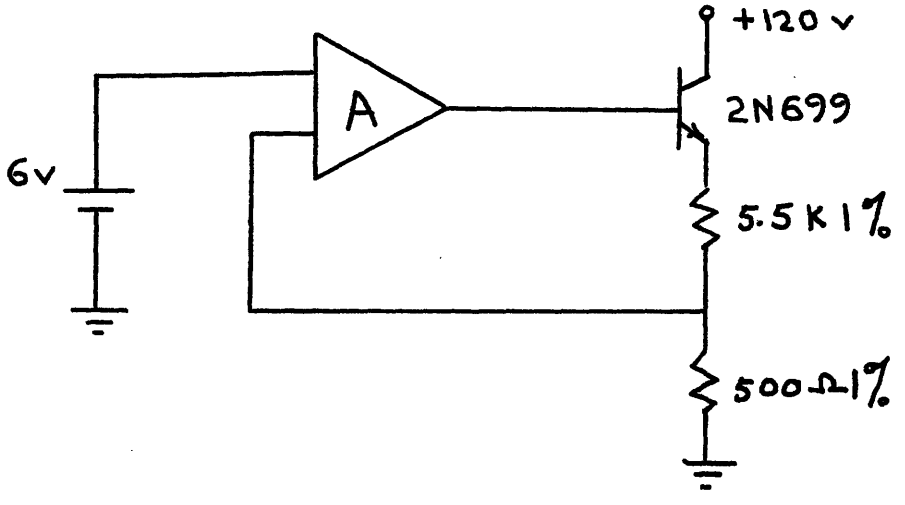

Figure 2.9

Without the capacitor across the input to the second stage, the system oscillates at a frequency of 320 K.C. Since this is a three stage amplifier, this might be expected due to its high gain. Figure 2.10 shows the effect of this capacitor upon the frequency response. As the capacitor is increased in value, the damping of the system is also increased as is evidenced by the reduction of the peaking. The cross-over slope is -12 db/octave so that this system looks like a second-order system at lower frequencies. A measure of stability of a system is its phase margin, and for a second-order system a good approximation is:[2]

$$\phi_{pm} = \frac{360}{\pi} \zeta \qquad (2.10)$$

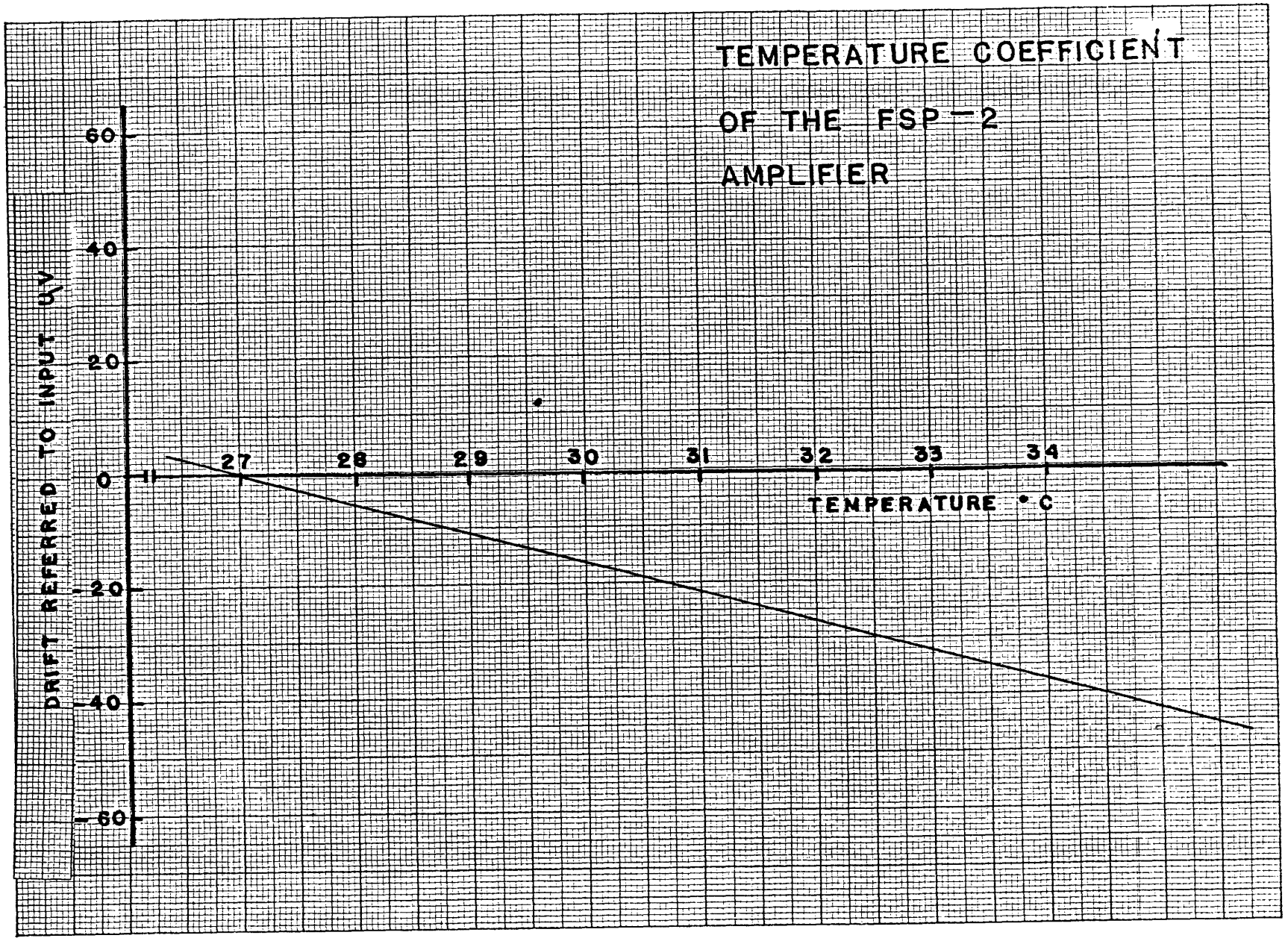
TEMPERATURE COEFFICIENT
OF THE FSP-2
AMPLIFIER
DRIFT REFERRED TO INPUT uV
60
40
20
0
-20
-40
-60
11
27
28
29
30
31
32
33
34
TEMPERATURE °C

Figure 2.8

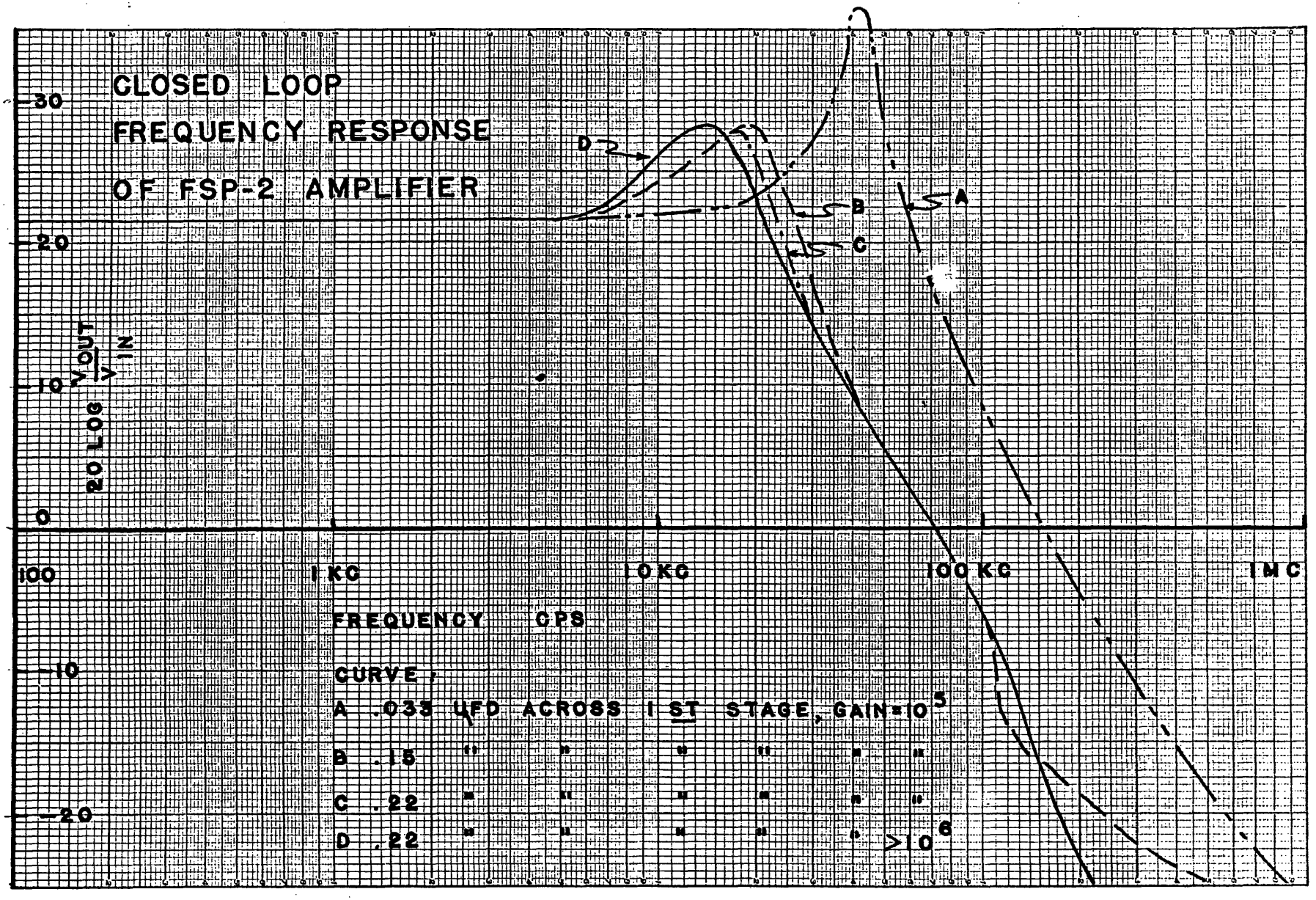
CLOSED LOOP
FREQUENCY RESPONSE
OF FSP-2 AMPLIFIER
D-2
A
B
C
30
20
10
0
20 Log Vout/Vin
100
1 KC
10 KC
100 KC
1 MC
FREQUENCY CPS
-10
-20
CURVE ;
A .033 UFD ACROSS 1ST STAGE, GAIN=10^5
B .15 " " " " "
C .22 " " " " "
D .22 " " " " >10^6

Figure 2.10

Where ζ is the damping coefficient. From standard curves of second-order systems, it is found for curve C that ζ is .25 so that $\phi_{pm} = 28.5°$. This indicates that it will take another 28.5° phase shift to make the system go absolutely unstable. For comparison, curve A has about 9° phase margin.

---

[2] Deltoro, V. and Parker, Principles of Control Systems Engineering Dept. of Electrical Engineering, C.C.N.Y. 1958

Chapter III

The Chopper D.C. Amplifier

3.1 The Chopper Modulator

It has been pointed out that the most difficult design problem in "straight" d.c. amplifiers is the drift of parameters. A solution to the problem is the use of a chopper modulator. The modulator shifts the information from being centered around zero frequency to being centered around some carrier frequency. This shift in frequency allows the signal to be amplified by conventional a.c. amplifier techniques. Due to the capacitive coupling of an a.c. amplifier, V_{BE} and h_{FE} drifts are not amplified by successive stages and are thus negligible as long as the amplifier remains in its linear region. After amplification, the signal is demodulated.

Figure 3.1 is a simple block diagram of a chopper amplifier. The input signal is modulated by the carrier signal w_c which is produced by the oscillator. After amplification the signal is demodulated by the same oscillator so that synchronism is maintained.

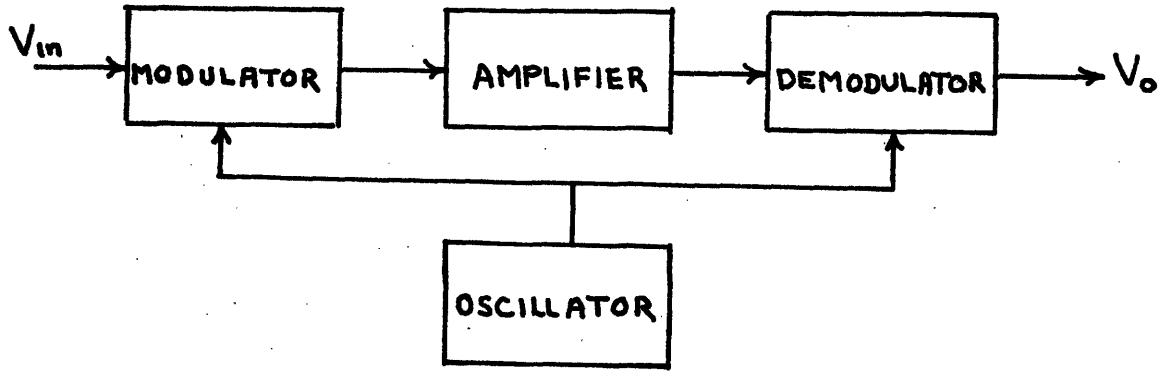

Figure 3.1

As shown in Figure 3.2 the chopper modulator is a synchronized switch. In practice this is very often a mechanical switch which has the advantage of being a passive device that comes very close to having zero impedance when closed and infinite impedance when open. When the switch is open the input appears unattenuated at the output terminals; when closed, the output is zero. The limitations of the mechanical chopper are its short lifetime, limited switching speed, and its size. An answer to these shortcomings is to use a transistor switch.

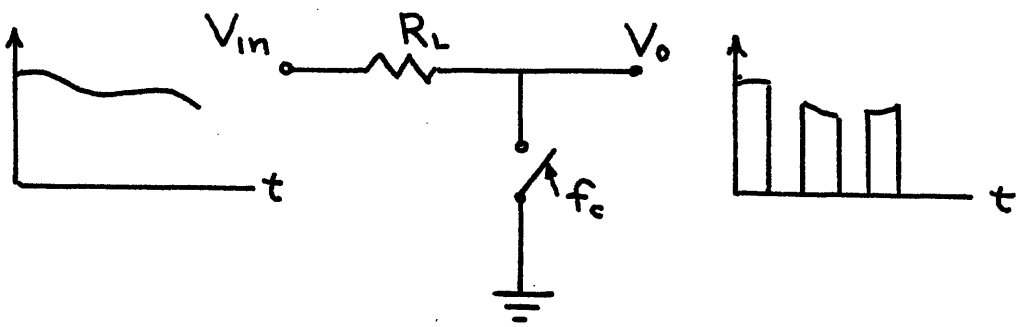

Figure 3.2

Transistors operated as switches do not suffer from any of the mechanical chopper deficiencies but, instead, have their own particular drawbacks. Figure 3.3 shows a simple transistor chopper along with its equivalent circuit. The switch is considered ideal. V_p is the voltage from collector

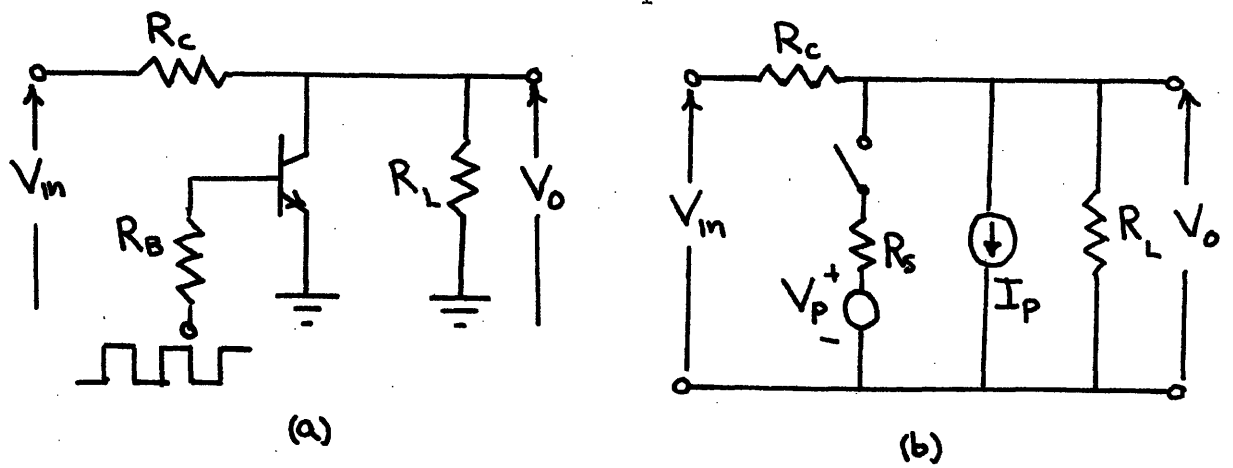

Figure 3.3

to emitter when the switch is closed with R_s being the dynamic resistance. When the switch is open the current I_p represents the leakage current. It is assumed that the driving source is positive enough to drive the transistor into its saturation region. If we consider the switch open, then

$$V_o = \frac{R_L}{R_L + R_C} V_{in} - \frac{R_C R_L}{R_L + R_C} I_p \qquad (3.1)$$

and for the switch closed

$$V_o = \frac{R_L R_S}{\Delta} V_{in} + \frac{R_L R_C}{\Delta} V_p - \frac{R_L R_C R_S}{\Delta} I_p \qquad (3.2)$$

where

$$\Delta = R_L R_S + R_L R_C + R_S R_C \qquad (3.3)$$

It is clear that the output voltage is a function of the transistor parameters V_p, I_p, and R_s. These parameters are functions of the operating conditions and of temperature for any transistor. Clearly, then, the drift problem has not been completely solved. If we consider that $R_L >> R_C$, then

$$V_o = V_{in} - R_c I_p \qquad (3.4)$$

for the switch closed. A lowering of R_c would decrease the effect of I_p, but this would also lower the impedance seen at the input terminals to the chopper. If, also, $R_L >> R_S$, $R_C >> R_S$, then

$$V_o = \frac{R_S}{R_C} V_{in} + V_p - R_s I_p \qquad (3.5)$$

for the switch closed. Therefore, even if $R_S = 0$ the effect of V_p would limit the magnitude of the signal that could be detected. For a typical silicon transistor V_p is in the order of 100 millivolts or more. I_p will usually be less than 100 milli-microamps at 25°C and R_S will normally be less than 200 ohms.

In order to reduce the magnitude of V_p and I_p the transistor is often operated in the inverted connection, the roles of collector and emitter are interchanged. The advantages of this mode of operation are reduced offset voltages and leakage currents. An approximate expression for the offset voltage in the normal connection is[1]

$$V_{PN} = -\frac{kT}{q} \ln \frac{1}{\alpha_I} = -\frac{kT}{q} \ln \left(1 + \frac{1}{\beta_I}\right) \qquad (3.6)$$

1 Sperry Semiconductor Division "Chopper Transistors" Technical Application Bulletin No. 2107 November 1960.

where

k - Boltzmann's constant 1.38×10^{-23} joule/°K
T - temperature degrees Kelvin
q - electric charge 1.6×10^{-19} coulombs
α_I - forward current transfer ratio measured near the saturation region with collector and emitter reversed in the common base configuration (inverse alpha)
β_I - inverse beta near the saturation region

If the expression for the offset voltage in the inverse connection is found, it is

$$V_{PI} = -\frac{kT}{q} \ln \frac{1}{\alpha_N} = -\frac{kT}{q} \ln \left(1 + \frac{1}{\beta_N}\right) \tag{3.7}$$

Where α_N and β_N are the normal alpha and beta near the saturation region. Normally β_I is much less than β_N so that V_{PI} is lower than V_{PN}. If $\beta_N = 50$ and $\beta_I = 2$ then $\frac{V_{PI}}{V_{PN}} \approx \frac{1}{20}$, a considerable reduction.

A relationship can also be expressed for I_p so that for the normal connection[2]

$$I_{PN} = \frac{1 - \alpha_I}{1 - \alpha_N \alpha_I} \cdot I_{CBO} = \frac{1 + \beta_N}{1 + \beta_N + \beta_I} I_{CBO} \tag{3.8}$$

and for the inverse connection

$$I_{PI} = \frac{1 - \alpha_N}{1 - \alpha_N \alpha_I} \cdot I_{EBO} = \frac{1 + \beta_I}{1 + \beta_N + \beta_I} I_{EBO} \tag{3.9}$$

Where I_{CBO} is the collector to base cutoff, current and I_{EBO} is the emitter to base cutoff current. Again, it is seen that the inverted connection has a distinct advantage since $\alpha_N I_{EBO} = \alpha_I I_{CBO}$. Therefore, the ratio of offset currents is

$$\frac{I_{PI}}{I_{PN}} = \frac{1 + \beta_I}{1 + \beta_N} \frac{I_{EBO}}{I_{CBO}} = \frac{1 + \beta_I}{1 + \beta_N} \frac{\alpha_I}{\alpha_N} = \frac{1}{25}$$

The dynamic resistance R_S can also be described for the normal and inverted connections with the following approximate results.[3]

$$R_{SN} = \frac{kT}{qI_B} \frac{\beta_N + \beta_I}{\beta_N(1 + \beta_I)} \tag{3.10}$$

$$R_{SI} = \frac{kT}{qI_B} \frac{\beta_N + \beta_I}{\beta_I(1 + \beta_N)} \tag{3.11}$$

---

[2] Ibid

[3] Ibid

where I_B is the base drive. There is little difference in the order of magnitude for either connection, although R_{SI} will be slightly lower than R_{SN}. R_S is also a function of base drive.

A method of further reducing the effects of V_p and I_p is to connect two transistors in the manner indicated in Figure 3.4. This is a differential chopper mode where both transistors are turned on and off simultaneously. The input signal V_{in} is equal to $V_1 - V_2$ and the output signal V_o is equal to $V_3 - V_4$. It is seen that for the switches open

$$V_o = \frac{R_{L1}}{R_{L1} + R_{C1}} V_1 - \frac{R_{L2}}{R_{L2} + R_{C2}} V_2 - \frac{R_{C1}\, R_{L1}}{R_{L1} + R_{C1}} I_{P1} + \frac{R_{C2}\, R_{L2}}{R_{L2} + R_{CL}} I_{P2}$$

If $R_{L1} = R_{L2} = R_L$, $R_{C1} = R_{C2} = R_C$ then

$$V_o = \frac{R_L}{R_L + R_C} (V_1 - V_2) - \frac{R_C\, R_L}{R_L + R_C} (I_{P1} - I_{P2}) \qquad (3.10)$$

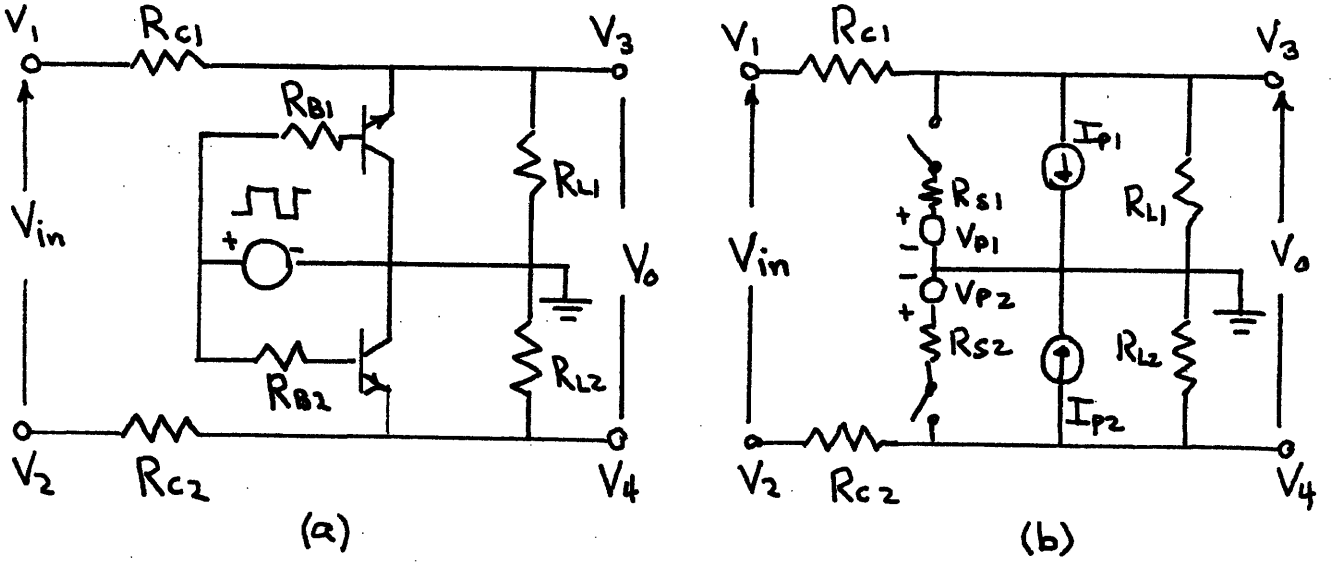

Figure 3.4

Any error due to the offset current is constrained to the difference between transistor leakage currents which for a matched pair of transistors may be made quite low. For the switches closed

$$V_o = \frac{R_{L1}\, R_{s1}}{\Delta_1} V_1 - \frac{R_{L2}\, R_{s2}}{\Delta_2} V_2 + \frac{R_{L1}\, R_{c1}}{\Delta_1} V_{p1} - \frac{R_{L2}\, R_{c2}}{\Delta_2} V_{p2}$$

$$- \frac{R_{L1}\, R_{C1}\, R_{s1}}{\Delta_1} I_{p1} + \frac{R_{L2}\, R_{c2}\, R_{s2}}{\Delta_2} I_{p2} \qquad (3.11)$$

where $\Delta_1 = R_{L1} R_{s1} + R_{L1} R_{c1} + R_{s1} R_{c1}$

$\Delta_2 = R_{L2} R_{s2} + R_{L2} R_{c2} + R_{s2} R_{c2}$

and for $R_{L1} = R_{L2} = R_L$, $R_{c1} = R_{c2} = R_c$, $R_{s1} = R_{s2} = R_s$

$$V_o = \frac{R_L R_S}{\Delta} (V_1 - V_2) + \frac{R_L R_C}{\Delta} (V_{P1} - V_{P2}) - \frac{R_L R_C R_S}{\Delta} (I_{P1} - I_{P2}) \qquad (3.12)$$

Errors with the switch closed due to V_p and I_p are again constrained to differences.

A matched pair of transistors used for a chopper application brings up many problems such as those mentioned in Chapter 2. Drifts of V_p and I_p tend to be the major source of trouble. A solution to the problem is to use the same technique discussed before: two transistors in a single can. Fairchild has available silicon planar transistors selected primarily for chopper application. In this case only five terminals are brought out of the device. The transistors have common collectors as shown in Figure 3.4a. The device is called a FSP-1.

3.2 Performance of the FSP-1

By using a Tektronix transistor curve tracer it was determined that β_N is about 50 and that β_I is about 2 for two separate units (four transistors) tested, so that the ratios developed in section 3.1 are of the proper magnitude. Fairchild lists the maximum value of I_{EBO} at 25°C of 10 X 10^{-9} amperes. Using equation (3.9) it is found that I_{PMAX} = .377 X 10^{-9} amperes. So if $R_L >> R_C$ and if R_L = 100K then the maximum offset due to leakage current on one side of the chopper of Figure 3.4(b) would be only 37.7 microvolts. Since differences are used in the differential chopper, this offset due to leakage can be ignored when the switch is open.

Fairchild claims a maximum offset voltage of 100 microvolts at $I_E = 0$. and I_B = 300 microamps. Since it is conceivable that emitter current might be flowing in the differential chopper, tests were conducted at emitter currents of 1.3 milliamps, 110 microamps and 10 microamps to determine the effect of temperature upon the offset voltage. Figure 3.5 shows the results of experimental data obtained using a Delta Temperature chamber to control temperature. At the high current ΔV_p has a slope of 10 microvolts per °C

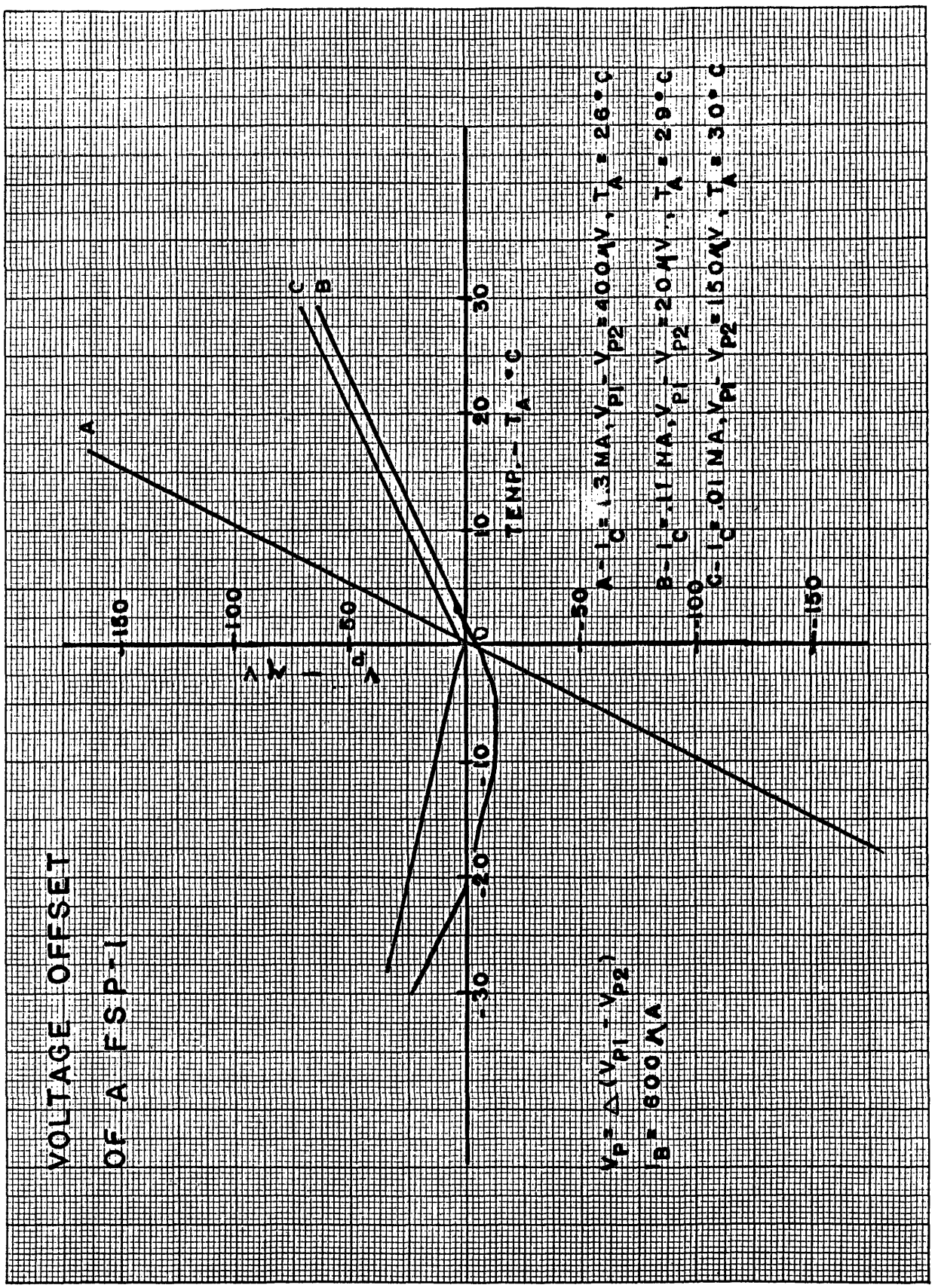
VOLTAGE OFFSET
OF A FSP-1
$V_P = \Delta(V_{P1} - V_{P2})$
I_B = 600 nA
ΔV_{P1-P2} (mV)
-150
-100
-50
-30
-20
-10
10
20
30
TEMP. - T_A °C
A - I_C = 1.3 mA, V_{P1-P2} = 400 mV, T_A = 26 °C
B - I_C = 1.1 mA, V_{P1-P2} = 200 mV, T_A = 28 °C
C - I_C = .01 mA, V_{P1-P2} = 150 mV, T_A = 30 °C
A
B
C

Figure 3.5

whereas at lower currents this is decreased appreciably. For a current of 110 microamps there is actually a region in which the differential voltage is essentially constant over ten degrees. It also appears that at lower currents the transistor offset voltages change at different rates so that the temperature coefficient changes sign. From this data it would seem that the current should be kept below or around 100 microamps for minimum effect of V_{PI} if emitter current must flow in the circuit.

Another consideration of importance is the frequency of chopping. Up to this point, the capacitance of the chopper has been neglected. The collectors of the transistors have a capacitance of about 25 picofarads maximum. When the transistor is turned off the capacitance must be charged. If the rise time of a circuit is defined as the time that it takes the output to rise from one-tenth to nine-tenths of its final value then it is found that the rise time is[4] $t_r = 2.2\ RC$ (3.13)
If the input signals are at a six volt level with respect to ground, then R_c should be about 50K in order to operate at the desired current level. For this value of resistance the rise time is 2.75 μs. To minimize errors due to changes in rise time with aging and drift of components it is necessary to chop at a low enough frequency so that the rise time is short compared to half the period of the chopper frequency. The chopping frequency chosen is 1 K.C. This allows the rise time to be slightly more than 1/2% of the half period. It is reasonable to expect that RC will not drift more than 10% in value so that the total change of rise time should be less than 1/20% of the half period.

3.3 Practical Design of the Chopper Amplifier

Figure 3.6 shows one possible chopper amplifier design. The design is divided into five sections.

The oscillator is a simple astable multivibrator designed to oscillate at 1 K.C. The output swings from approximately 14 volts positive to 5 volts negative, delivering about 600 microamps to the FSP-1 transistors and 140 microamps to the 2N697 demodulator.

The chopper is the differential configuration discussed earlier. Since the transistors are on only half the time, the impednace is 50K

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[4] Millman and Taub "Pulse and Digital Circuits" Chapter 2 P. 41 McGraw Hill Co. New York 1956

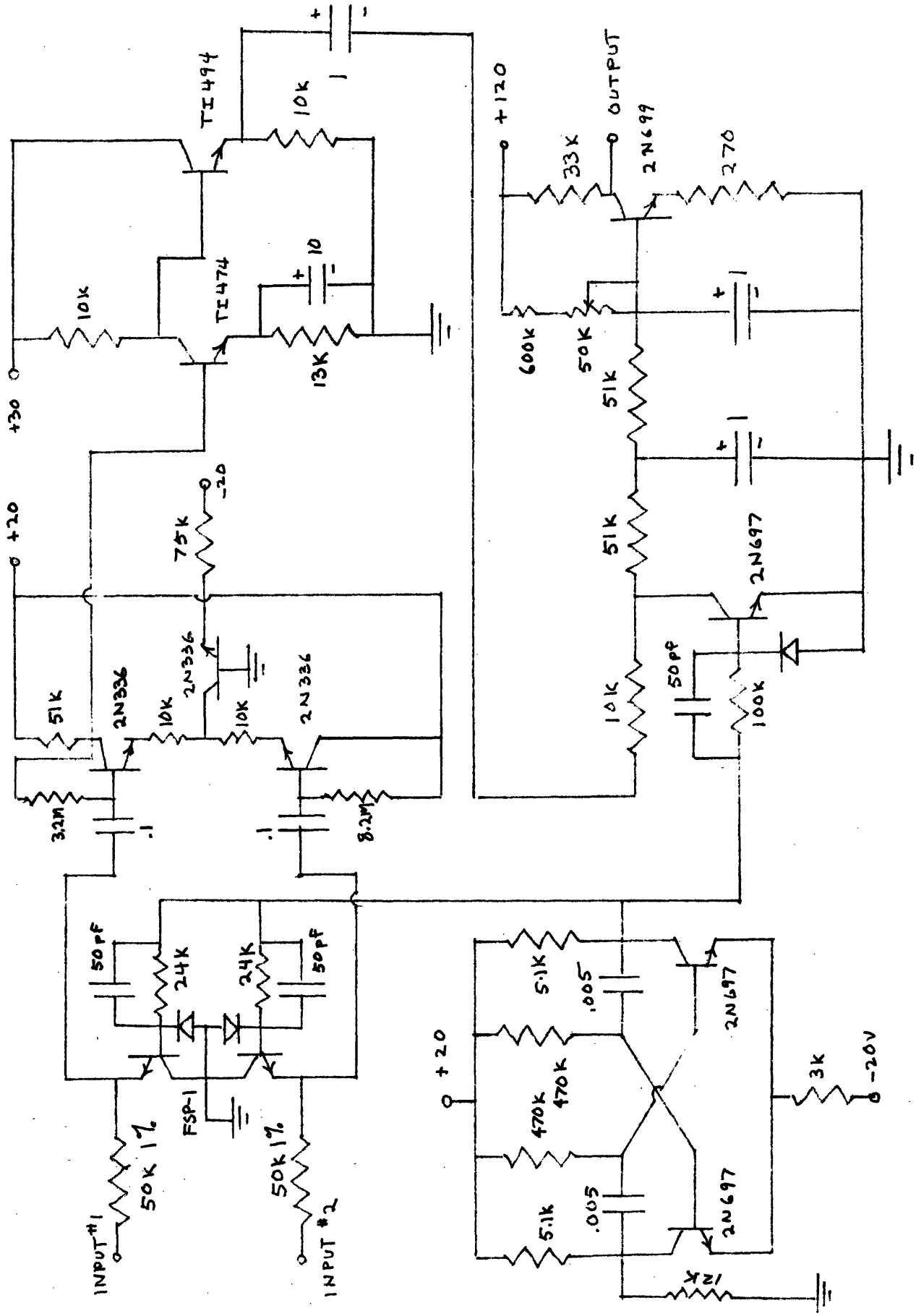
TI494
10k
TI474
10k
10
13K
+30
+20
75k
-20
51k
2N336
10k
2N336
10k
2N336
.1
.1
3.2M
8.2M
50pF
24K
24K
50pF
FSP-1
50k 1%
50k 1%
INPUT #1
INPUT #2
+120
OUTPUT
33k
2N699
270
600k
50K
51k
51k
2N697
10k
50pF
100k
5.1k
.005
2N697
+20
470k
470k
3k
-20V
5.1k
.005
2N697
12k

Figure 3.6

when the switch is closed and infinite when the switch is open. Stable resistors are used for the reasons discussed in Chapter 1. The diodes used in the base-collector circuit are protective devices and limit the reverse voltage to the breakdown of the IN660 diodes, about 500 millivolts. The capacitors are added in the base circuit in order to improve the turn-on switching time.

The first stage of the a.c. amplifier is a differential to single-ended stage. As in the d.c. amplifier the differential stage has the advantage of high common mode rejection. The small signal beta of the 2N336 is about 100 so that use of a 10K in the emitter branches of the input stages allows a high input impedance. The gain of the first stage is about five. The second stage is direct-coupled to the first, thereby allowing the second stage bias scheme to be as simple as possible. A high voltage gain is accomplished by using a TI 474 high beta transistor. The small signal beta is about 150 at the bias level used. A low impedance emitter follower output is used to drive the demodulator. Internal d.c. drifts within the amplifier will not be coupled to the demodulator because of the capacitive coupling.

The demodulator stage uses a synchronized switch to sample the output. The action is similar to the modulator action, except that errors caused at this stage by offsets are not as significant as at the input, since any offset here is divided by the preceeding gain when referred to the input as drift. The switch section drives a filter with a break frequency below 10 cps. The filter then drives an output d.c. stage with a control to set the output at 85 volts for a zero differential input.

3.4 Frequency Considerations

In order to illustrate more completely the effect of the chopper frequency on the bandwidth, a frequency domain analysis on a chopper model will be done. Figure 3.7 is a block diagram of a chopper amplifier. Consider that the bandwidth of the amplifier is large enough to pass $f_1(t)$ completely. The form of $f_m(t)$ is as shown in Figure 3.8, so that the Fourier transform is

$$F_m(n) = \frac{1}{T}\int_0^T f(t)e^{-jnw_1 t}\,dt = \frac{1}{T}\int_0^{T/2} e^{-jnw_1 t}\,dt$$

$$= \frac{1}{2}\,\frac{\sin(nw_1 T/4)}{nw_1 T/4}\, e^{-jnw_1 T/4} \qquad (3.14)$$

where $T = \frac{2\pi}{w_1}$

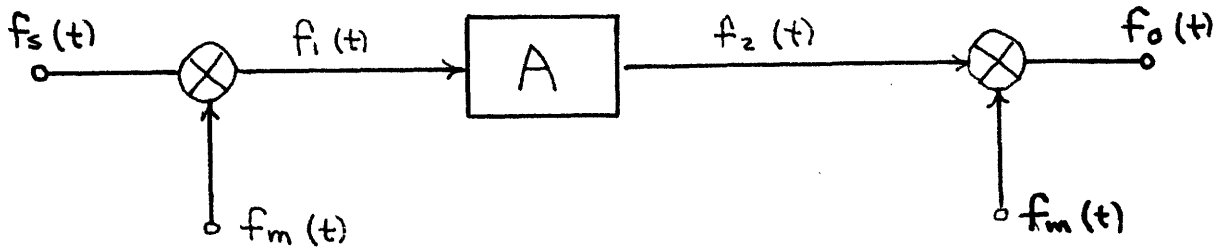

Figure 3.7

If the input signal is considered to have a rectangular spectrum with bandwidth of $2w_s$ as shown in Figure 3.9 then $F_1(w)$ can be found by convolution of $F_m(n)$ and $F_s(w)$ so that

$$F_1(w) = \int_{-\infty}^{\infty} F_m(\tau)\, F_s(\quad -\tau)\,d\tau \qquad (3.15)$$

The convolution is done graphically in Figure 3.10. It is seen that if $2w_s > w_1$, then there is overlapping of the spectra and distortion will occur since a filter could not be built to extract the information.

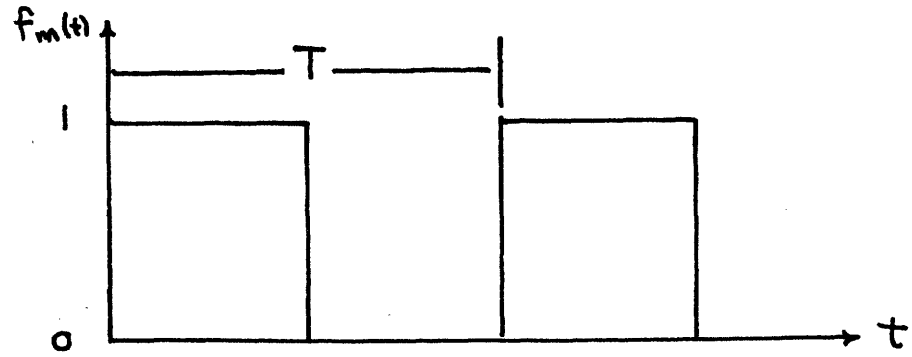

Figure 3.8

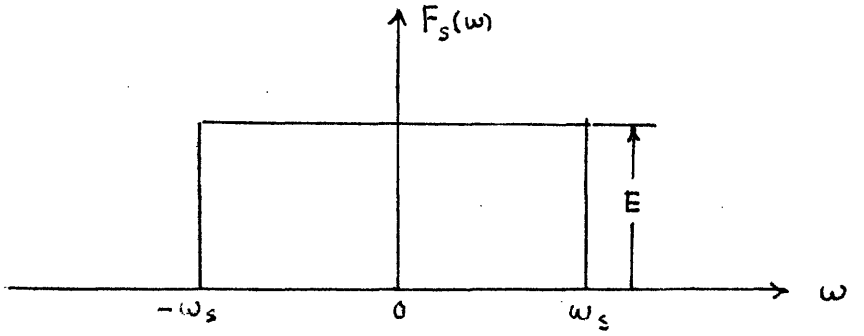

Figure 3.9

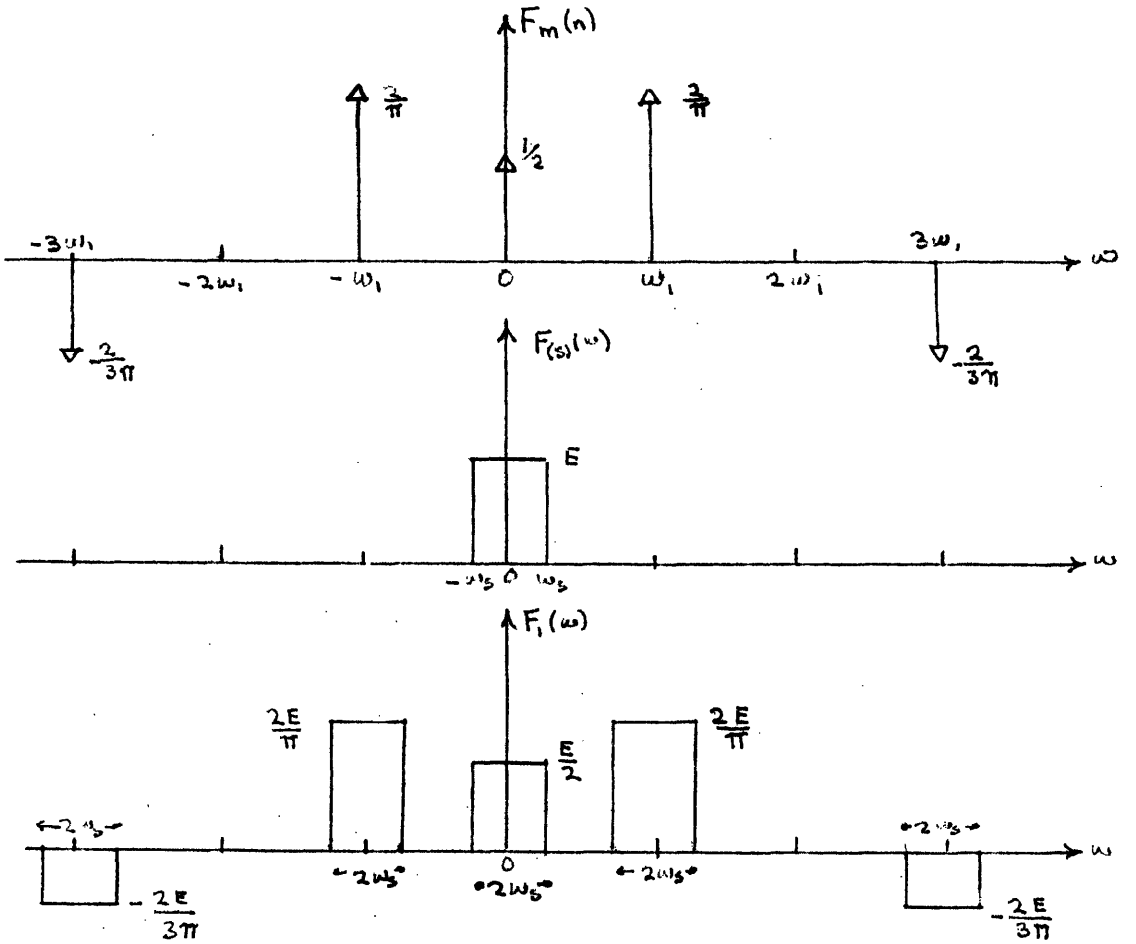

Figure 3.10

Since the chopper amplifier is operating at 1K.C. the filter cut-off was purposely made low enough to filter out any high frequency components in the signal, so that the current being controlled in the system will have a minimum of high frequency noise. The chopper amplifier designed will not meet the transient specifications of the system but since the purpose of this paper is to achieve a low-drift amplifier, the design was tested. The transient specifications can be met by utilizing the chopper amplifier in a chopper-stabilized amplifier[3] using a d.c. amplifier or by using another a.c. amplifier in parallel with the chopper amplifier to increase the bandwidth.

3.5 Drift of the Chopper

A forty-seven hour drift test of the chopper amplifier described was run using the test setup of Figure 3.11. The amplifier had an average drift of less than ten microvolts when allowed to operate at room temperature. The temperature variation was probably about 4°C during the run of the test.

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3 Okada, R.H. "Stable Transistor Wide-Band D-C Amplifiers" Communication and Electronics March 1960 Page 26

Chapter IV

The Field Effect Transistor Amplifier

4.1 The Field Effect Transistor

Recently a device called a field-effect transistor has appeared on the market. Although not involving minority charge movement as does the conventional transistor, it will be referred to as a transistor throughout this paper. It was originally proposed by Shockley in 1952 with much of his original transistor work. In 1953 Dacey and Ross[1] constructed the first few units on the basis of Shockley's equations. These transistors appeared to operate according to predictions, yet very little was done with them.

Figure 4.1 is a representation of the field effect transistor. By applying a negative potential to the gate leads, the resistance of the channel can be controlled. Keeping the drain voltage constant allows the following definition of transconductance:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D \text{ constant}} \qquad (4.1)$$

If the drain current is plotted as a function of drain voltage with the gate voltage as a parameter, the family of Figure 4.2 results. There is a striking similarity to a pentode.

Dacey and Ross have shown the following relations to be true. The resistance of the channel is:

$$R_o = \frac{L}{2aZ\sigma} \qquad (4.2)$$

where: σ conductivity of the n-type material
L length of the channel
2a the channel thickness
Z the channel width

[1] Dacey G. and Ross, I.M. Unipolar Field Effect Transistors, Proc. of the IRE 1953 Vol. 41 Page 970.

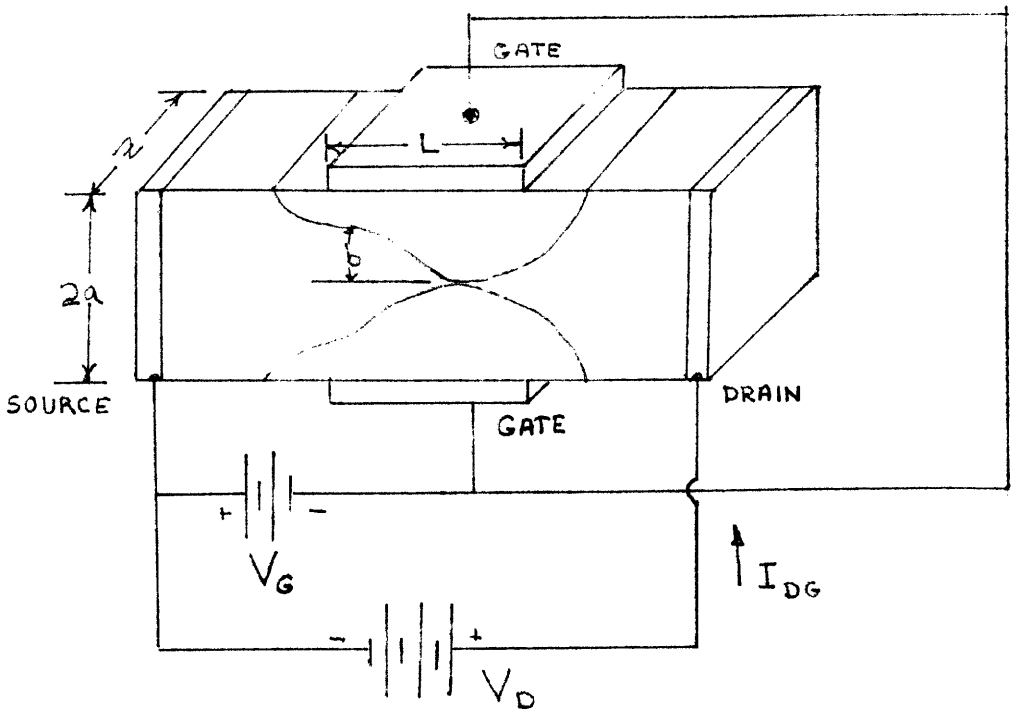


Figure 4.1

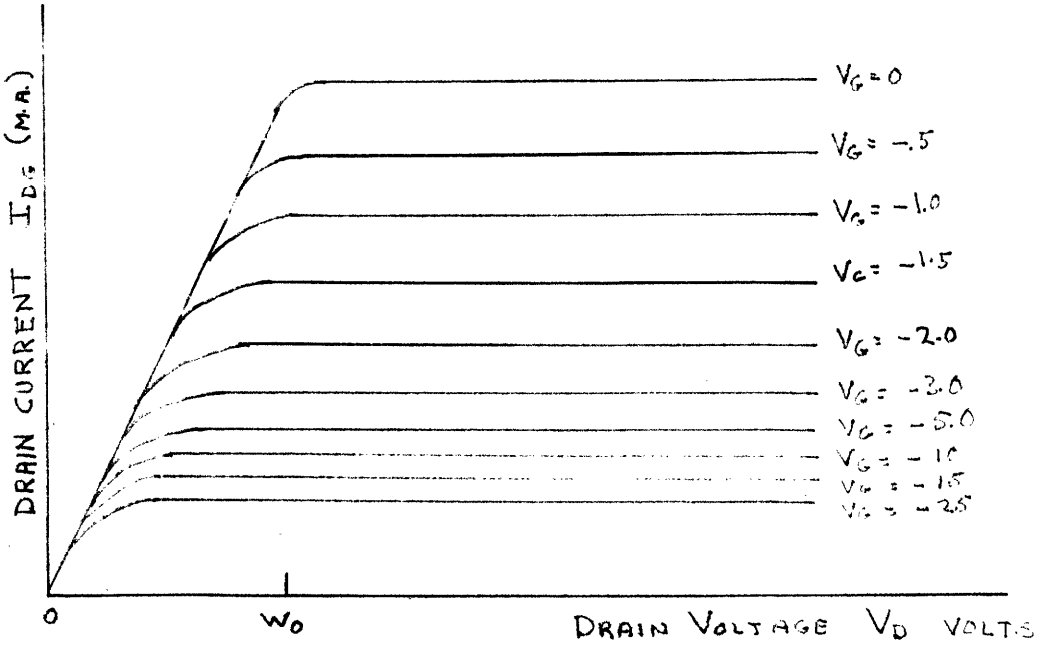


Figure 4.2

The pinch-off voltage is:

$$W_o = qNa^2/2K \qquad (4.3)$$

Where: qN = magnitude of the fixed donor charge density

K = dielectric constant

If $V_D - V_G = W_o$ then the transconductance is $g_{mo}[1 - (- \frac{V_G}{W_o} 1/2]$ (4.4)

Where $g_{mo} = \frac{2\sigma a}{L}$ which is the maximum transconductance. The saturation drain current is

$$I_{DG} = I_{DO} [1 + \frac{V_G}{W_o} (3 - 2 - \frac{V_G}{W_o})] \qquad (4.5)$$

Where $I_{DO} = \frac{g_{mo} W_o}{3}$ which is the maximum current.

The input impedance of the field effect transistor is essentially that of a back-biased p-n junction and is normally in the order of 100 megohms for silicon. The output impedance is usually greater than 1 megohm. Figure 4.3 is a circuit model of the transistor that will hold over a wide frequency range.

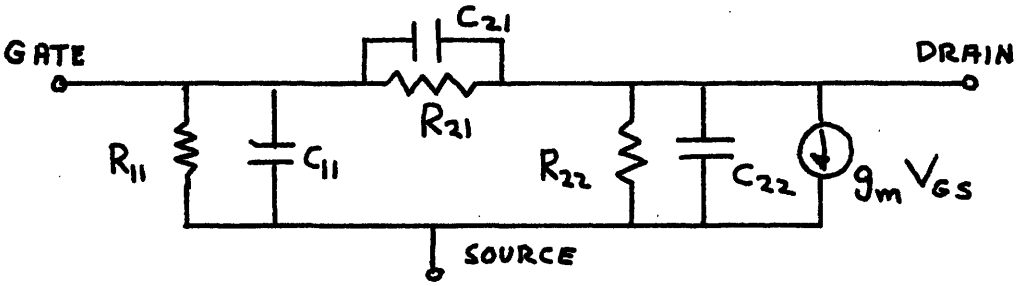


Figure 4.3

Where $C_{11} = 35$ mmf, $C_{21} = 7$ mmf, $C_{22} = 2$ mmf. It can be seen that a field-effect transistor can be handled in much the same manner as a pentode tube.

4.2 Field-Effect Transistor D.C. Amplifier

The design of an amplifier[2] using a field-effect transistor is basically simpler than a conventional amplifier design but some care must be taken to utilize fully the characteristics of the device. Equation (4.4) describes the transconductance as a function of the gate voltage V_G if $V_D - V_G = W_o$. The transistor will be used under normal operating conditions so that V_G will never be allowed to go positive. This would forward-bias the gate to

[2] The only commercial supplier of field-effect transistors at the present is is Crystalonics, Inc., All the following tests were performed on devices obtained from this company. A list of the significant characteristics can be found in Appendix C.

source junction and consequently limit the device's use as an amplifier. For all V_G negative, equation (4.4) can be plotted as a function of V_G as shown in Figure 4.4a.

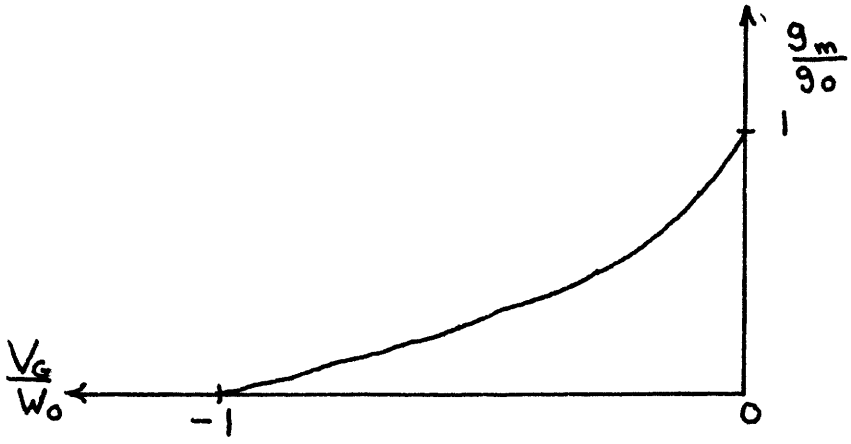


Figure 4.4a

g_m is a maximum when $V_G = 0$ and goes to zero when $V_G = W_o$. Therefore, for maximum gain it would appear that the bias should be operated at zero or slightly negative.

The second critical factor in the design is the saturation drain current. Equation (4.5) also expresses this quantity as a function of V_G. Figure 4.4 shows this relationship graphically. Clearly the maximum saturation current occurs for $V_G = 0$. The curve of Figure 4.4a is the derivative of the curve of Figure 4.4b.

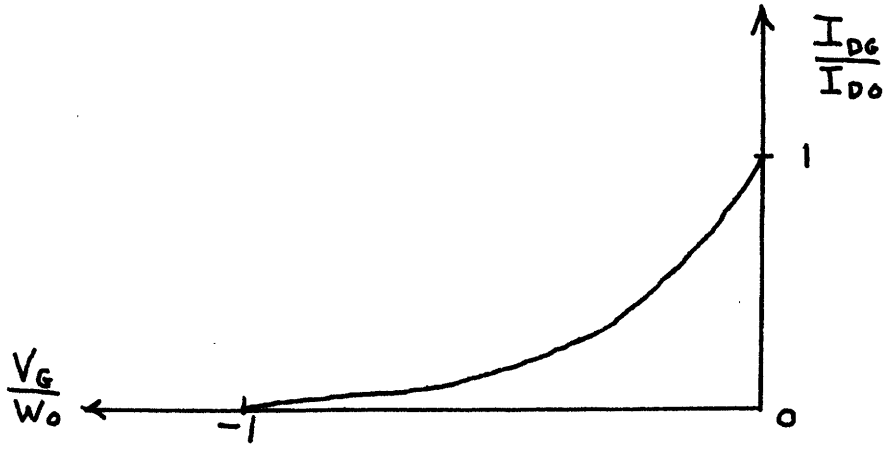


Figure 4.4b

The circuit of Figure 4.5 is a single stage amplifier. The d.c. output voltage is $V_{cc} - I_{DG} R_L$. If $V_{in} - V_{BB} = 0$, then $I_{DG} = I_{DO}$. For small variations, the small-signal equivalent model of Figure 4.3 can be used. Ignoring the capacitors and assuming that all impedances are large compared to R_S and R_L, the change in output is $\Delta V_o = -g_m R_L \Delta V_{in}$ (4.6)

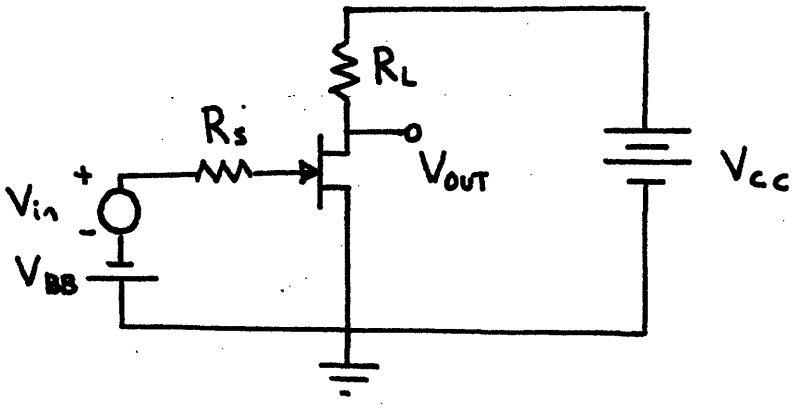


Figure 4.5

It can be seen that if a large voltage gain is desired, both g_m and R_L should be large. Normally, the higher g_m is, the higher the drain current will be and in order to operate in the linear portion of the characteristics V_{cc} will have to be large. For example, if a voltage gain of 100 is desired and if $g_m = 1000$ micromhos, then $R_L = 100$ K, so that for $I_{DG} = 1$ m.a. a supply voltage of about 130 volts would be required to operate in the saturated region. With this high a supply voltage, care must be taken that the drain-to-gate voltage does not exceed the breakdown voltage.

Another important point in the d.c. amplifier design is that both g_m and I_{DG} are temperature dependent. From equation 4.4, for $V_G = 0$ it is found

$$\frac{dg_m}{dT} = \frac{2a}{L} \frac{d\sigma}{dT} \qquad (4.7)$$

The temperature dependency of g_m is due mainly to the effects of temperature on conductivity. Experimental work[2] has been done which expresses conductivity as a function of temperature. At temperatures below 300°K the temperature dependency of the conductivity is controlled by the impurity content as shown in the sketch of Figure 4.6a. Pure intrinsic silicon has a positive

[2] Conwell, Esther M. "Properties of Silicon and Gemanium" Proc. of the I.R.E. 1952 Vol. 40 Page 1333.

temperature coefficient but as the doping increases, the temperature coefficient actually changes sign. As found from the data sheet distributed by Crystalonics, the temperature coefficient of g_m is negative and therefore the device is being used in the extrinsic region. Since data on the conductivity were not obtained from Crystalonics at the writing of this paper, only experimental determination of the temperature coefficient was possible.

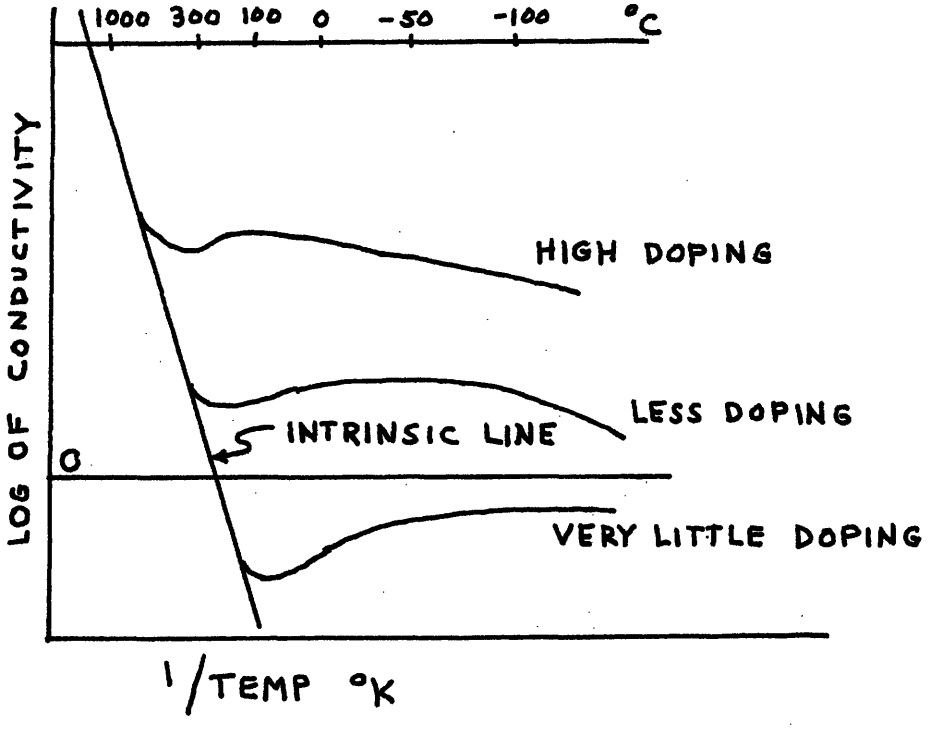


Figure 4.6

From equation (4.5), for $V_G = 0$, it is found that $\frac{dI_{DG}}{dT} = \frac{W_o}{3}\frac{dg_m}{dT}$. For the devices tested W_o is approximately 15 volts, so that the temperature coefficient of I_{DG} is about three times that of the transconductance. Figure 4.6b is a graph of the change in I_{DG} as a function of temperature for a typical C610 field-effect transistor. The measured temperature coefficient is -.845% per °C. A differential d.c. amplifier configuration would be superior to the single-ended stage. Drifts in saturation current between stages would tend to cancel one another. A simple differential stage is shown in Figure 4.7. The circuit can be biased so that the source

voltages of both transistors are close to the d.c. level of the signals V_1 and V_2. V_1 and V_2 must also be kept from going positive with respect to the source. If the circuit and the transistors are perfectly balanced the differential voltage $V_3 - V_4$ will be zero. For imbalances it will be: $I_{DG2} R_{L2} - I_{DG} R_{L1}$. The small signal gain is found to be:[3]

$$A_D = \frac{V_3 - V_4}{V_1 - V_2} = -\frac{g_m R_L}{1 + g_m R_s} \tag{4.8}$$

where $g_m = g_{m1} = g_{m2}$, $R_L = R_{L1} = R_{L2}$, $R_S = R_{S1} = R_{S2}$

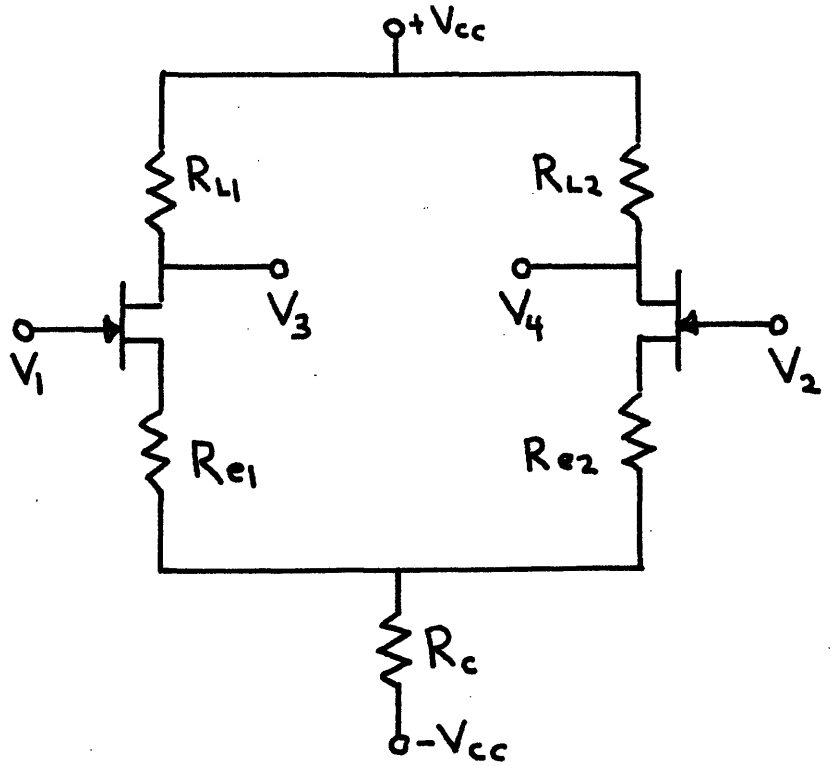


Figure 4.7

The differential field-effect amplifier offers some advantages over the conventional transistor differential amplifier. The input impedance is much higher for the field-effect amplifier. This is an important consideration for the system in which this amplifier will find use. There is no V_{BE} drift term to consider but instead a I_{DG} drift term. The drift voltage due to a ΔI_{DG} is referred to the input of the amplifier

by dividing ΔI_{DG} by g_m. From the curve of Figure 4.6, it is found that $\frac{\Delta I_{DG}}{\Delta T} = -2\,\mu a/^{o}C$ at 25.5°C. For these transistors $g_m = 200$ micromhos, so that $\frac{\Delta V_G}{\Delta T} = -10$ mv/°C. A typical silicon transistor has a $\frac{\Delta V_{BE}}{\Delta T}$ of about -2.5mv/°C, so it is seen that the field-effect transistor has a slight disadvantage in this respect. Both g_m and h_{FE} changes with respect to temperature depending upon the drain current and collector current in the transistors. From the typical curves given by Crystalonics $\frac{\Delta_{gm}}{\Delta T} = -.25\%/°C$ at a drain current of 1.5 m.a. and at 25°C. At the same collector current and temperature for a 2N338 transistor, $\frac{\Delta h_{FE}}{\Delta T} = .55\%/°C$. The field-effect has a very slight advantage.

4.3 Temperature Compensation of the Field-Effect Amplifier

In order to achieve temperature stability in a field-effect transistor amplifier, it is necessary to temperature compensate. Matching of transistors should help considerably but since the units are in two cans, temperature gradients will undoubtedly exist. Figure 4.8 shows one scheme of compensating a differential amplifier. The resistor R_T is temperature sensitive. If the input to the amplifier is zero, then the following relationships hold:

$$V_o = I_2 R_2 - I_1(R_1 + R_T)$$

and if only the effects of temperature are considered,

$$\frac{dV_o}{dT} = R_2 \frac{dI_2}{dT} - (R_1 + R_T) \frac{dI_1}{dT} - I_1 \frac{dR_T}{dT}$$

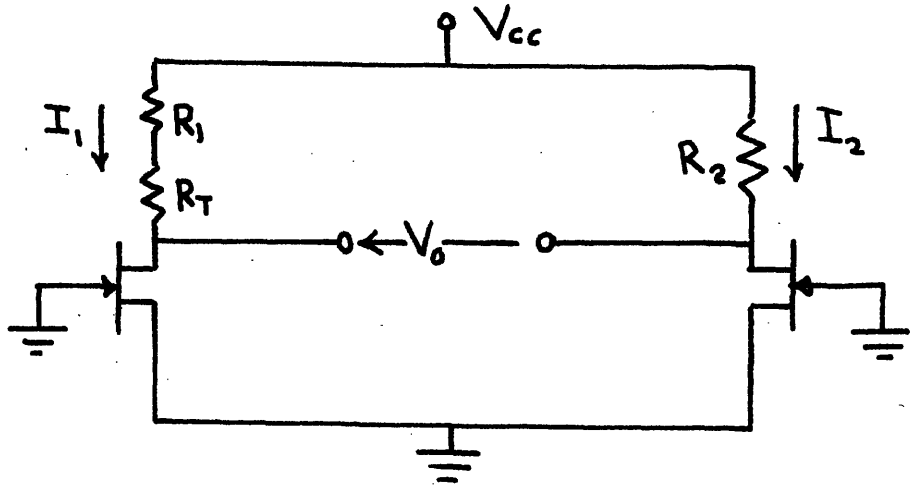


Figure 4.8

SATURATED DRAIN CURRENT
OF A C610 FIELD-EFFECT
TRANSISTOR
TEMPERATURE °C
CHANGE IN DRAIN CURRENT μA
30
20
10
0
-10
-20
-30
0
10
20
30
40
50
60
V_G = 0
I_{DO} = 2.6 MA
W_O = 15 V
T_{REF} = 25.0 °C

Figure 4.6 b

If the amplifier is originally balanced for T_o with $R_1 + R_T = R_2 = R$ and $I_1 = I_2 = I$ and if it is desired that $\frac{dV_o}{dT} = 0$, then

$$R \frac{dI}{dT} = I \frac{dR_T}{dT} \tag{4.9}$$

where

$$\frac{dI}{dT} = \frac{dI_2}{dT} - \frac{dI_1}{dT}$$

If the temperature sensitive resistor has a positive temperature coefficient then $\frac{dI}{dT}$ must also be positive. In the actual case this can be accomplished by interchanging the transistors if $\frac{dI}{dT}$ is negative. In order to have some idea of the order of magnitude involved some typical data was taken. With $R = 100K$, $I = .25$ m.a. and $\frac{dR_T}{dT} = 0$, $\frac{dI}{dT}$ was found to be .2 microamps per °C. In order to satisfy equation (4.9) the temperature coefficient of R_T must be 80 ohms per °C. This coefficient was obtained from unmatched transistors; it is expected that matched transistors might do better. This current imbalance reflects to the input as a 1 mv/°C voltage imbalance.

4.4 Practical Design of the Field Effect Differential Amplifier

Figure 4.9 is a schematic of a differential amplifier using a pair of field effect transistors in the first stage. The drain current in both field-effect transistors is .3 m.a. For input voltages of 6 volts the common sources will be at 6.2 volts, thereby backbiasing the transistors by -.2 volts. The temperature compensation is accomplished by means of a network in one of the drain branches of the amplifier. Control of the temperature coefficient is accomplished by means of the 10K potentiometer. The 51R6 thermistor has a temperature coefficient of -4.4% per °C at 25°C. Its absolute value is about 100K. For a parallel network of a standard resistor and a thermistor the temperature coefficient can be found to be

$$\frac{dR_p}{dT} = \frac{R^2}{(R + R_T)^2} \frac{dR_T}{dT} \tag{4.10}$$

Where R_p is the parallel combination of the standard resistor R and the thermistor R_T. Use of a negative coefficient thermistor necessitates selection of the transistor location so that temperature coefficients will cancel.

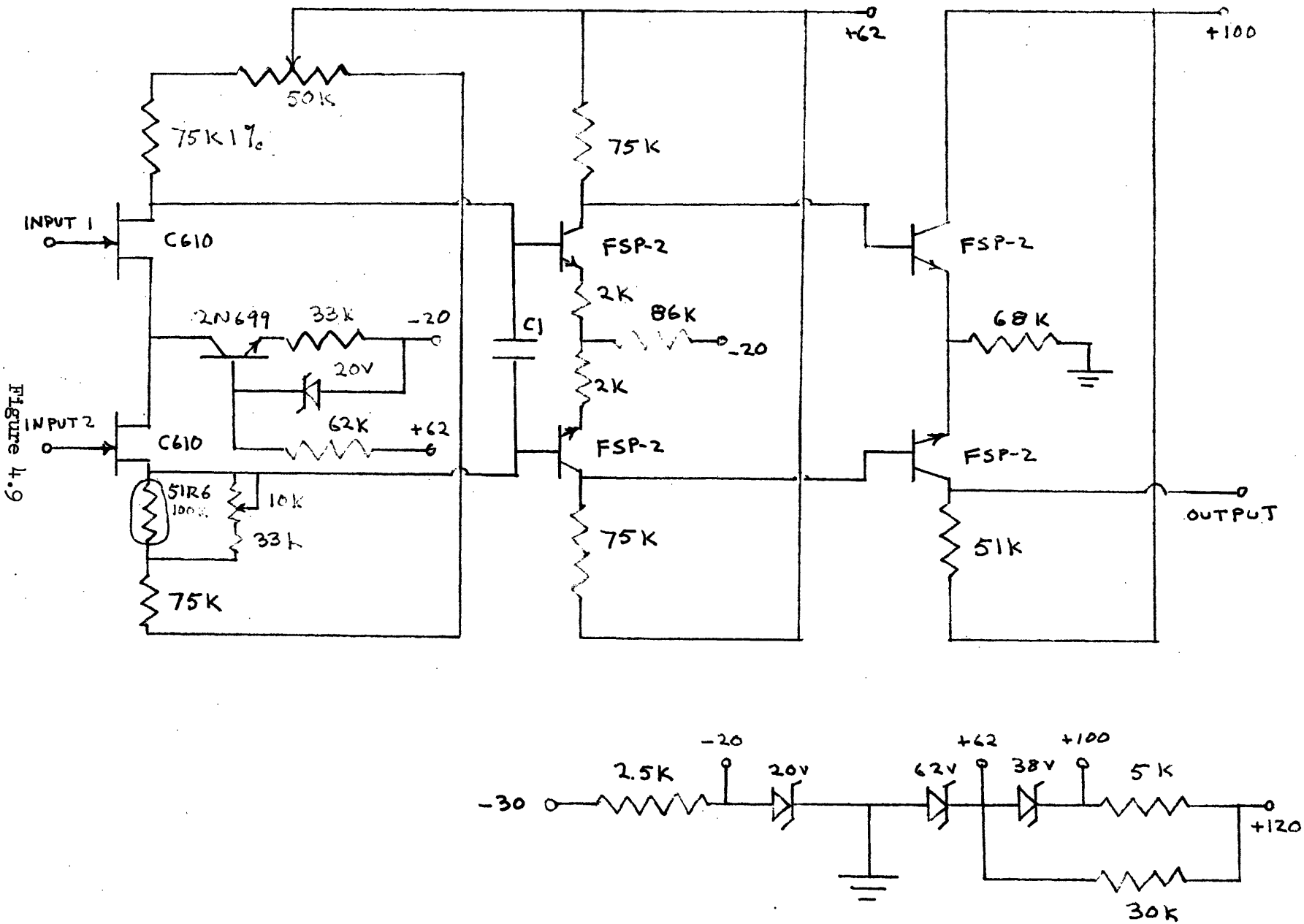

+62
+100
50K
75K 1%
75K
INPUT 1
C610
FSP-2
FSP-2
2K
2N699
33K
-20
C1
86K
-20
68K
20V
2K
INPUT 2
C610
62K
+62
FSP-2
FSP-2
OUTPUT
51R6
100K
10K
33K
75K
75K
51K
-20
+62
+100
2.5K
20V
62V
38V
5K
-30
+120
30K

Figure 4.9

Transistor Q7 is used as a current source in the same manner as for the conventional d.c. amplifier. The remainder of the amplifier uses standard resistors and the design is similar to that discussed in Chapter 2. FSP-2 units were used for the final two stages.

The test set-ups were identical to those described in Chapter 2. In order to accomplish temperature compensation the entire amplifier was immersed in a denatured kerosene bath that was controlled by a Gebrueder Haake temperature controller. This allowed temperature to be controlled to within 0.1°C.

Figure 4.10 shows the frequency response of the field-effect transistor amplifier. The capacitor across the input to the second stage is a .01 microfarad capacitor chosen so that the predominent break point is at about 100 cps. The peaking that occurs at 22 K.C. is due to the significant break points of the second two stages.

A drift run at a constant temperature for a period of fifteen hours showed drifts less than 100 microvolts.

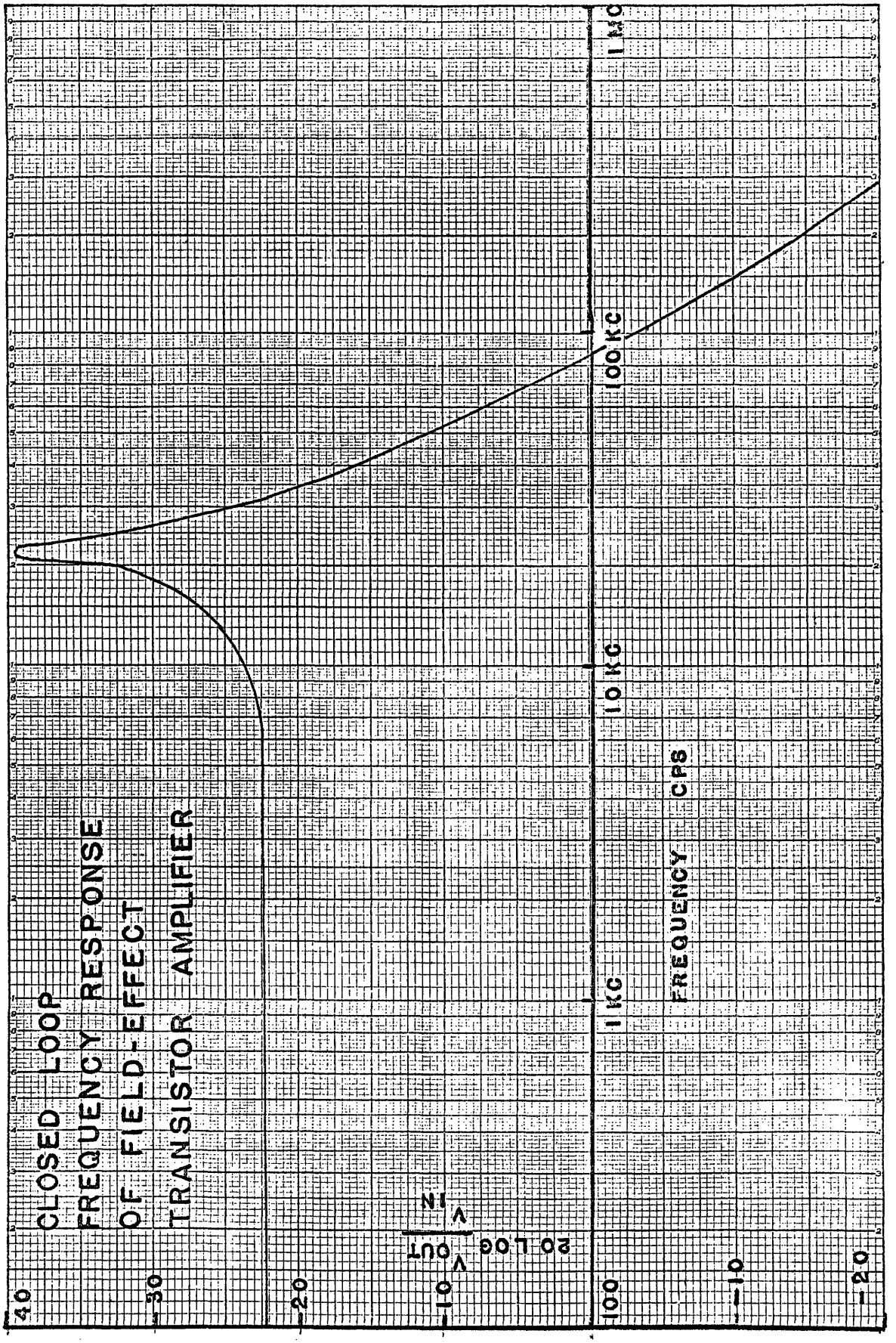

CLOSED LOOP
FREQUENCY RESPONSE
OF FIELD-EFFECT
TRANSISTOR AMPLIFIER
40
30
20
10
0
-10
-20
20 LOG V OUT / V IN
100
1 KC
10 KC
100 KC
1 MC
FREQUENCY CPS

Figure 4.10

Chapter V

The Current Switch

5.1 Performance of Transistors as Switches

It has been assumed until now that the transistor switches described in Chapter I are perfect. In the actual case there are delays associated with the turn-on and turn-off times of the transistor. Figure 5.1 shows a typical common-emitter switch. The response of the collector current to a step base current is shown in Figure 5.2. When a base current large enough to saturate the transistor is applied the time from t_o until the

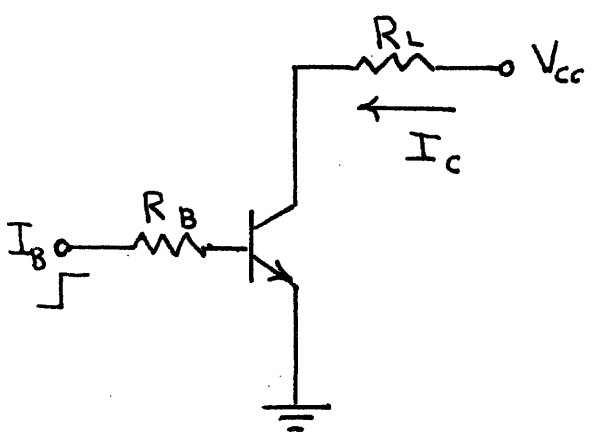


Figure 5.1

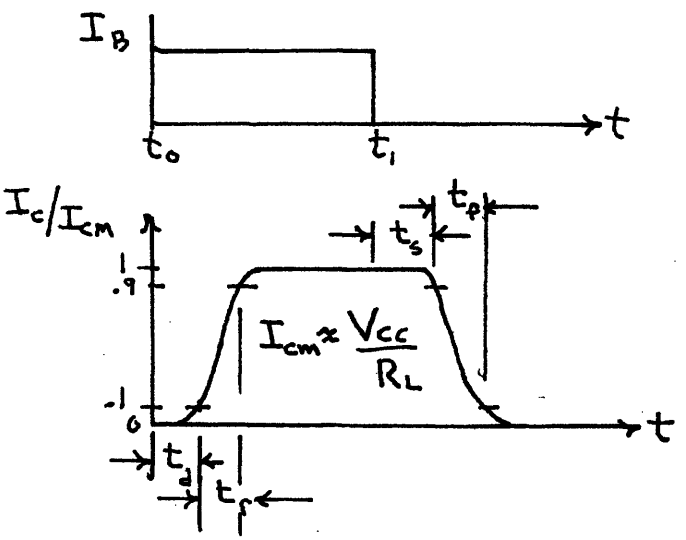


Figure 5.2

collector current reaches 10% of its steady state value is the delay time t_d. The rise time, t_r, is as defined previously from 10% to 90% of the steady state value. When the base current is returned to zero, the transistor does not respond immediately but is delayed a time t_s, the storage time, from t_1 to 90% of the steady state current. The time from the 90% to 10% of steady state current is the fall time t_f.

The delay time is a function of the reverse bias applied before switching and the time required for the carriers to diffuse across the base region. Since the d.c. beta is a function of the emitter current, the delay time is also a function of the rate of the increasing d.c. beta as the emitter current increases.

The rise time is a function of the alpha-cutoff frequency, the amount of base drive and the d.c. beta. The larger the base drive, the shorter the rise time.

When the transistor is saturated the collector voltage falls below the base voltage, thereby forward biasing the collector-base junction. The collector then injects a charge into the base region. The collector current can not begin to decrease until this stored charge is swept away. This is the cause of the storage time. The storage time is a function of the length of time the transistor is on, h_{FE}, the inverse alpha, and the drive-on and drive-off currents.

The fall time is similar to the rise time and depends upon the frequency response of the transistor. It also depends upon the drive-off currents. If the voltage driving the base through resistor R_B in Figure 5.1 is allowed to go negative, the turn-off current will go negative until the transistor is turned off.

5.2 Design of the Current Switch

It has been mentioned that the load being switched is an inductive load. The switching of an inductive load would cause problems due to high voltage transients which may cause transistor voltage breakdowns. Another problem might be closed loop instability. One solution to the problem is compensation of the inductive network. Figure 5.3a shows

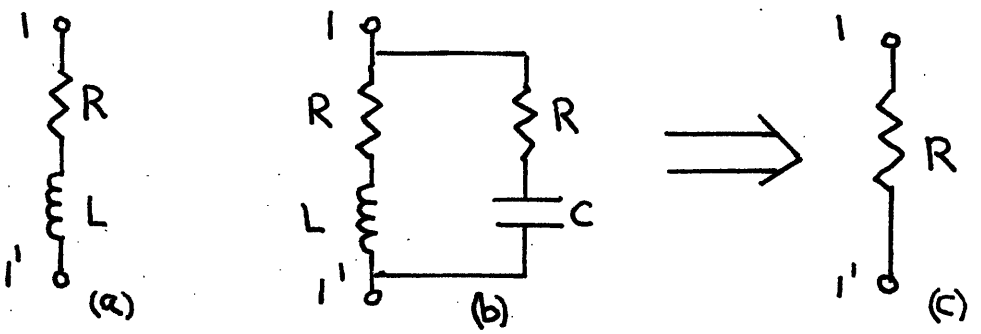


Figure 5.3

the uncompensated network having an inductance L and a resistance R. The admittance of this network is $\frac{1}{R + sL}$. The network may be complemented so that the admittance seen across its terminals is a pure conductance 1/R. The complement of the RL network is an RC network with an admittance of $\frac{1}{R + 1/sC}$ where $C = \frac{L}{R^2}$. With the compensation the network is resistive for all frequencies. When the switch is turned off the energy stored in the capacitor and inductor is dissipated in the two resistors. The circuit is critically damped so that the decay current through the inductor will have a critically damped exponential wave form. Use of the compensated network allows the design to be made without consideration of inductive transients. Figure 5.4 is a schematic diagram of the current switch. The two transistor switches (Q3 and Q4) in series with the load are driven from the two driver transistors (Q5 and Q6), which in turn are driven by the flip-flop pair (Q7 and Q8). The flip-flop is a bi-stable multivibrator driven by negative pulses in a complementary mode. The frequency of oscillation is therefore determined by the pulse source.

The two driver transistors are driven just slightly into saturation. Also, "speed-up" capacitors are used in order to decrease the rise time of Q5 and Q6 by allowing a large transient base current to be drawn. The capacitors are variable trimming capacitors; the reason for their use will be explained shortly. Since the transistors are not driven deeply into saturation, storage time is decreased.

The switch transistors Q3 and Q4 are driven by Q5 and Q6. When Q5 is turned off, Q3 is driven on. The base current for Q3 is determined by the +120 volts, the 8K resistor and the emitter voltage. Since the d.c. amplifier controls the voltage across the 60 ohms to be 6 volts, 100 milliamperes will flow through the switch. For this circuit R = 750 ohms, so that the voltage at the emitter of Q3 is 81 volts. This causes the base current to be 7.5 milliamperes, driving the transistor just slightly into saturation, thereby decreasing the storage time. When Q5 is turned off the emitter is slightly reverse biased by use of the 200 ohm resistor in the emitter branch. Q4 and Q6 operate in an identical manner.

Transistors Q1 and Q2 are connected in a Darlington connection. The output of the d.c. amplifier is connected to the base of Q1. The input

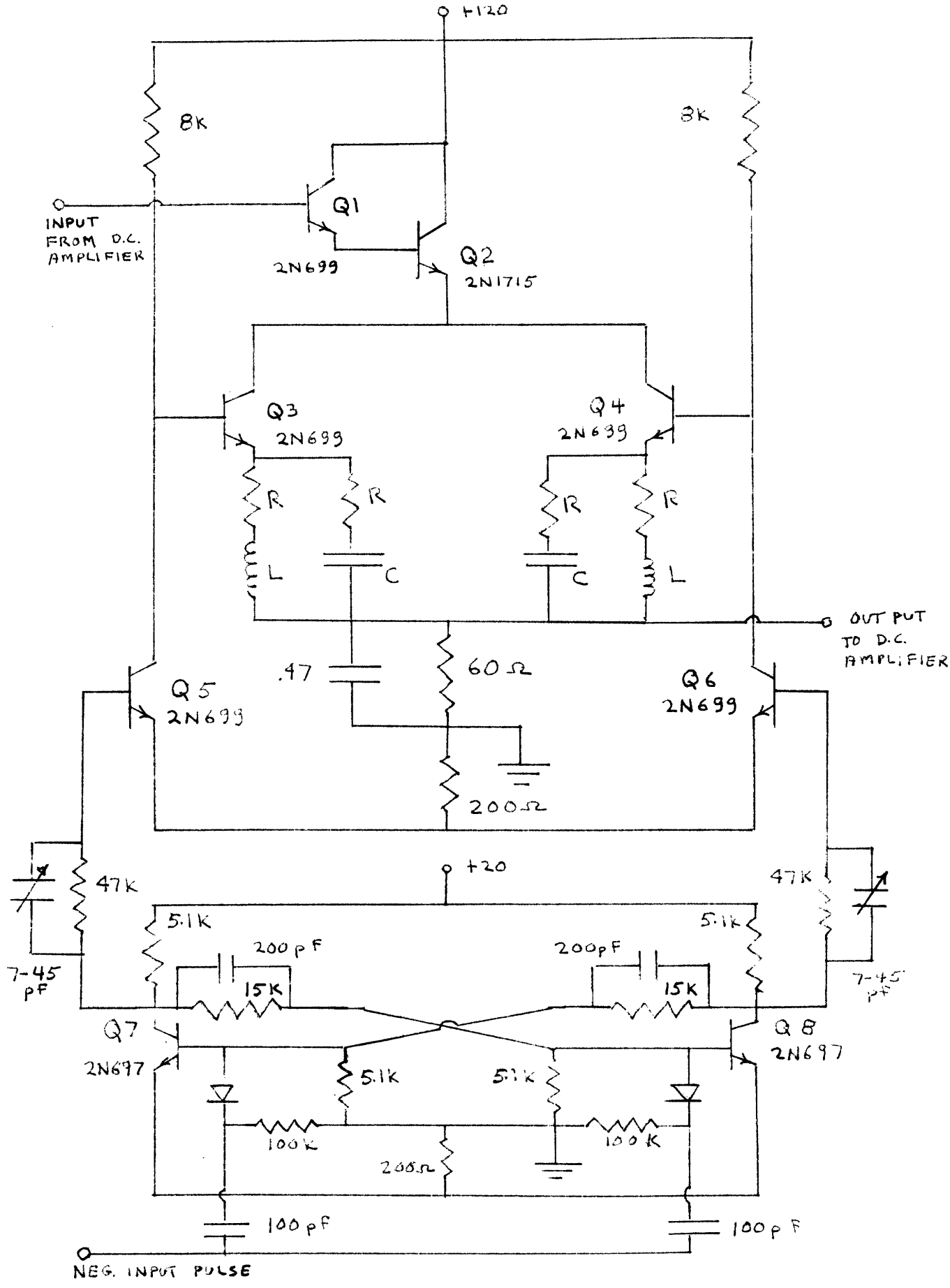

+120
8K
8K
INPUT FROM D.C. AMPLIFIER
Q1
2N699
Q2
2N1715
Q3
2N699
Q4
2N699
R
R
L
C
C
R
R
L
OUT PUT TO D.C. AMPLIFIER
.47
60Ω
Q5
2N699
Q6
2N699
200Ω
+20
47K
47K
5.1K
5.1K
200pF
200pF
15K
15K
7-45 pF
7-45 pF
Q7
2N697
Q8
2N697
5.1K
5.1K
100K
100K
200Ω
100pF
100pF
NEG. INPUT PULSE

Figure 5.4

impedance seen at the base terminals is approximately $h_{FE1}\ h_{FE2}\ R$ where h_{FE1} is the d.c. beta of Q1 and h_{FE2} the d.c. beta of Q2. For the transistors used the input impedance is approximately one megohm which is sufficiently high to cause a negligible effect upon the d.c. amplifier gain.

Transients caused by switching will cause an error in the average current being controlled by the d.c. amplifier, which senses the voltage across the 60 ohm resistor. The transients are caused by the various delays discussed earlier. For example, it can be seen that the current flowing through Q3 is delayed in time from the triggering pulse by the delays of Q7, Q5, and Q3 itself. The three transistors turn on, off, and on respectively. Clearly, the delays are due to the turn-on times $(t_d + t_r)$ of transistors Q7 and Q3 and to the turn-off time $(t_s + t_f)$ of transistor Q5. While this sequence of events is occurring, the complementary sequence is occurring for transistors Q8, Q6, and Q4. Three separate limiting cases can occur as shown in Figure 5.5.

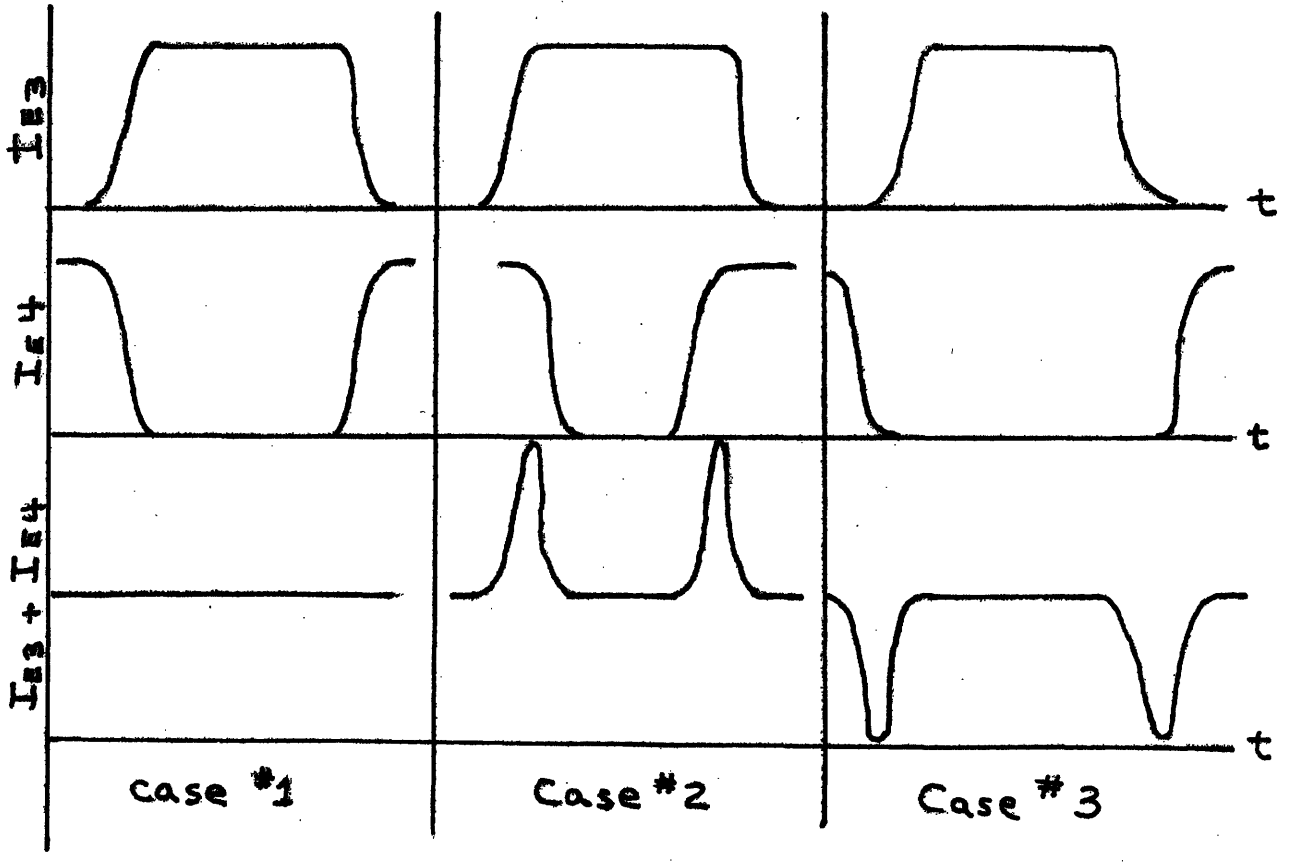


Figure 5.5

The delays have been greatly exaggerated in respect to the switching frequency so that their effect can be more easily shown.

Case 1 is the desired effect. Although the delays may occur in the transistors, the effect on the sampled waveform, which is the sum of the two emitter currents of Q3 and Q4, is a constant if the rise time and fall times are equal and if they occur simultaneously (assuming the same type wave form for each). This case is unlikely.

Case 2 in Figure 5.5 shows the effect of one transistor turning on before the other has turned off. This assumes that the response of the d.c. amplifier is too slow to sense the change.

The illustration of the third case in Figure 5.5 shows what occurs if one transistor turns off before the other turns on. For this case, the amplifier can not respond since the loop is open for this brief period.

For this circuit without the .47 microfarad capacitor across the 60 ohm resistor experimental results indicated that case 3 was the actual case. Using a Tektronix 545 oscilloscope to record the waveform across the 60 ohm resistor it was found that there was a negative pulse of slightly less than a micro-second duration. Since the pulse went completely six volts negative, this showed that one transistor turned off completely before the other turned on. Two schemes were used to minimize the pulse. First the "speed-up" capacitors of transistors Q5 and Q6 were made adjustable so that the rise times of the transistors could be varied. This allowed better balancing of the delays to both transistor switches. The ranges of the capacitors were determined experimentally by observing the oscilloscope pattern. The second scheme used was correcting of a .47 microfarad capacitor across the 60 ohm resistor. The filtering action was sufficient to cause the pulse to be decreased to less than 100 millivolts. Since the frequency break-point of this filter is at about 5000 cps, the effect upon the d.c. amplifier performance is negligible.

Chapter VI

Closed Loop Dynamic Performance of the Amplifiers

6.1 Evaluation of the Amplifiers

The three amplifiers designed in this paper were tested in the complete closed loop. The tests included the effects of switching frequency and of load imbalances upon the drift stability of the loop.

Figure 6.0 shows the complete test set-up for each amplifier. With this arrangement all the necessary information was obtained.

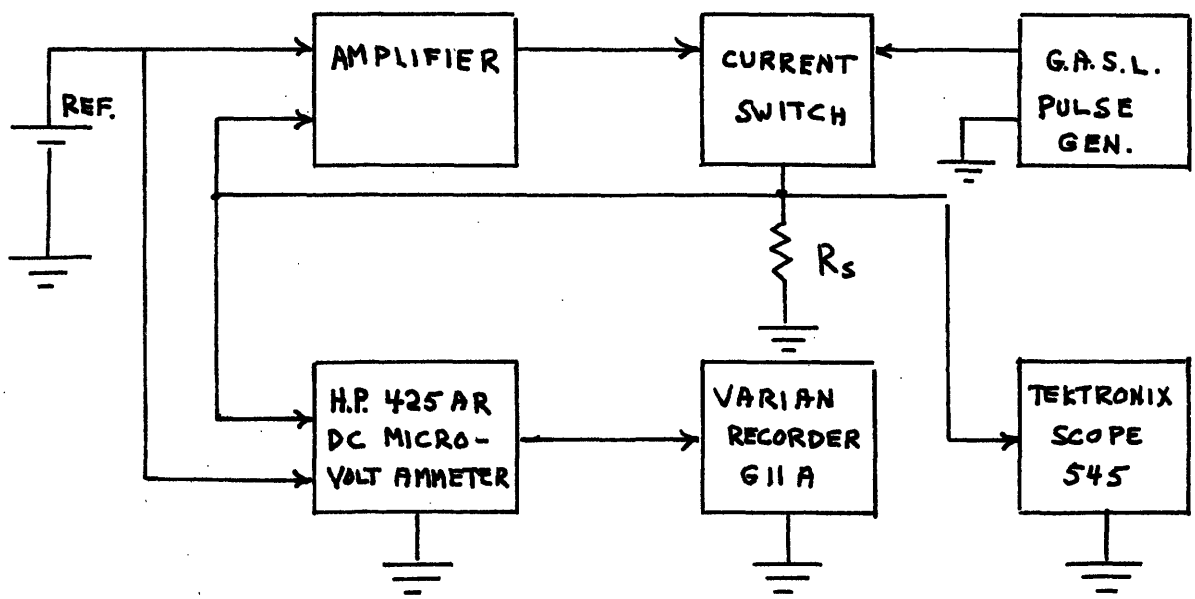


Figure 6.0

6.2 Performance of the FSP-2 Amplifier

With the FSP-2 amplifier connected in the loop about 15 microamps of base current is drawn at each input. The use of internal feedback in

the amplifier tends to increase the dynamic input impedance. For this amplifier the input impedance is greater than 100K.

The output impedance of the amplifier is the parallel combination of the 51K output resistor and the output impedance of final stage transistor. The total impedance is in the order of 25K, which is sufficiently low so that the switch does not load the amplifier.

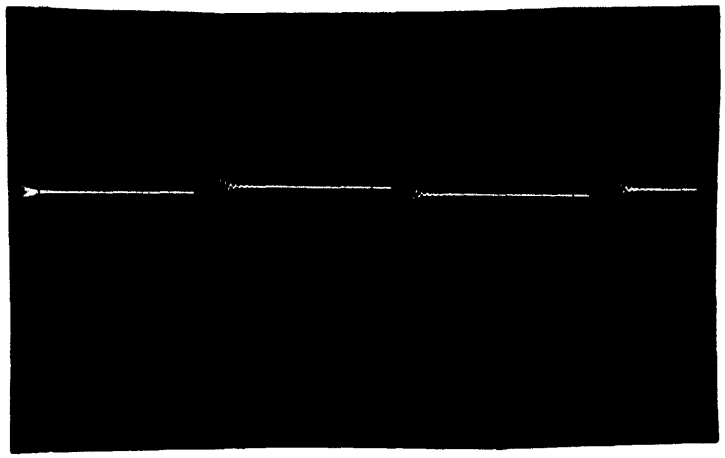
The photographs in Figure 6.1 show the dynamic performance of the amplifier while switching 1600 times a second. Figure 6.1a is the output of the amplifier with the switch loads matched to give an offset of less than .5 volts. Because the amplifier is underdamped, ringing of the output occurs for every switching time. Figure 6.1b shows the effect of an approximate 2.5 volt mismatch of loading upon the amplifier output. The positive pulse occurring just before the drop in level is caused by both transistor switches being off simultaneously. The voltage across the sensing resistor is shown in both Figures 6.1c and 6.1d. The difference in switching levels can not be noticed on the Tektronix scope when the load is mismatched but the difference between levels is 100 microvolts as measured on the d.c. microvolt meter. This is equivalent to about a 1.6 microampere error in the average current. The negative pulse caused by both switch transistors being off simultaneously can be seen in Figure 6.1c. The last photograph, Figure 6.1d is an enlarged view of the transient.

Random drift is a difficult parameter to define for a d.c. amplifier since it can consist of a constantly increasing error and also an error that oscillates at random frequencies. Figure 6.2 is a four hour section of a drift-test on the FSP-2 amplifier. There is a consistent noise level of about 10 microvolts. There is also a peak to peak drift of about 40 microvolts. The transients of sometimes 200 microvolts can be attributed chiefly to line surges and temperature control transients. There appears to be no constant drift over this short time interval and this section is taken from a 24 hour test in which every 4 hour section is essentially the same.

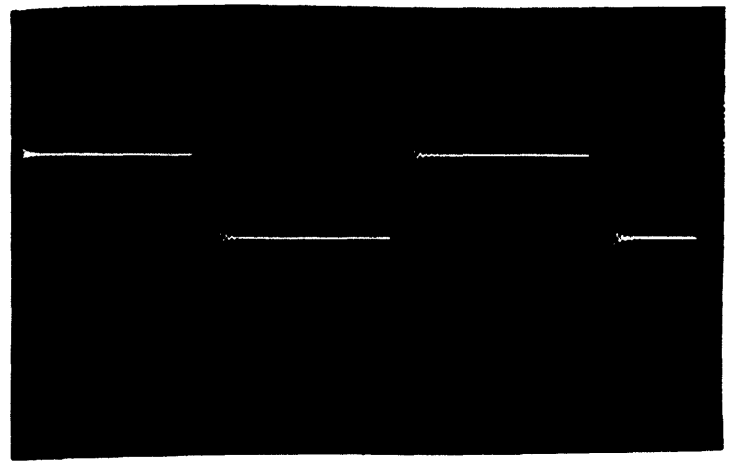
6.3 Performance of the Chopper Amplifier

As mentioned earlier, the input impedance of the chopper amplifier 50K with switch closed. The input current into the amplifier is 120

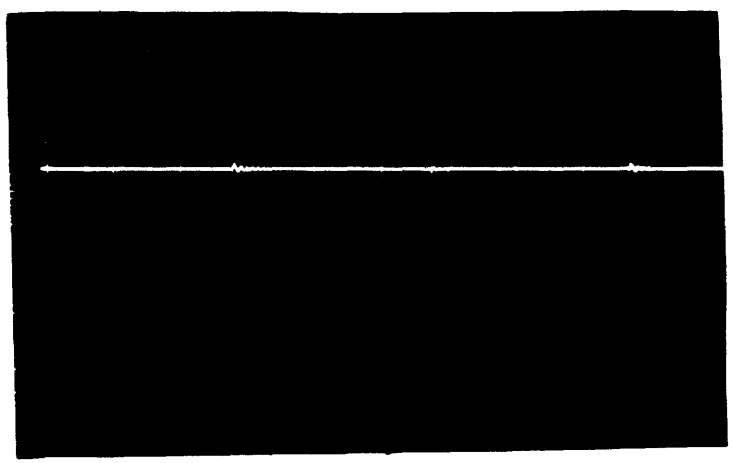
Figure 6.1



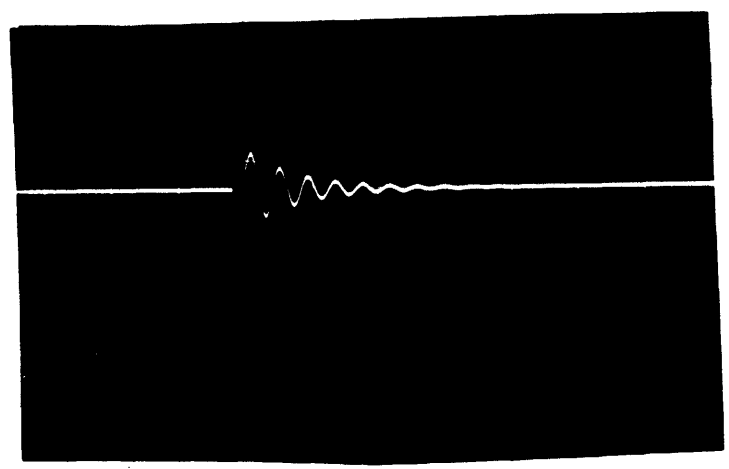
(a) Vert. 2v/cm
Horiz. 200 μs/cm



(b) Vert. 2v/cm
Horiz. 200 μs/cm



(c) Vert. 2v/cm
Horiz. 200 μs/cm



(d) Vert. 100 mv/cm
Horiz. 4 μs/cm

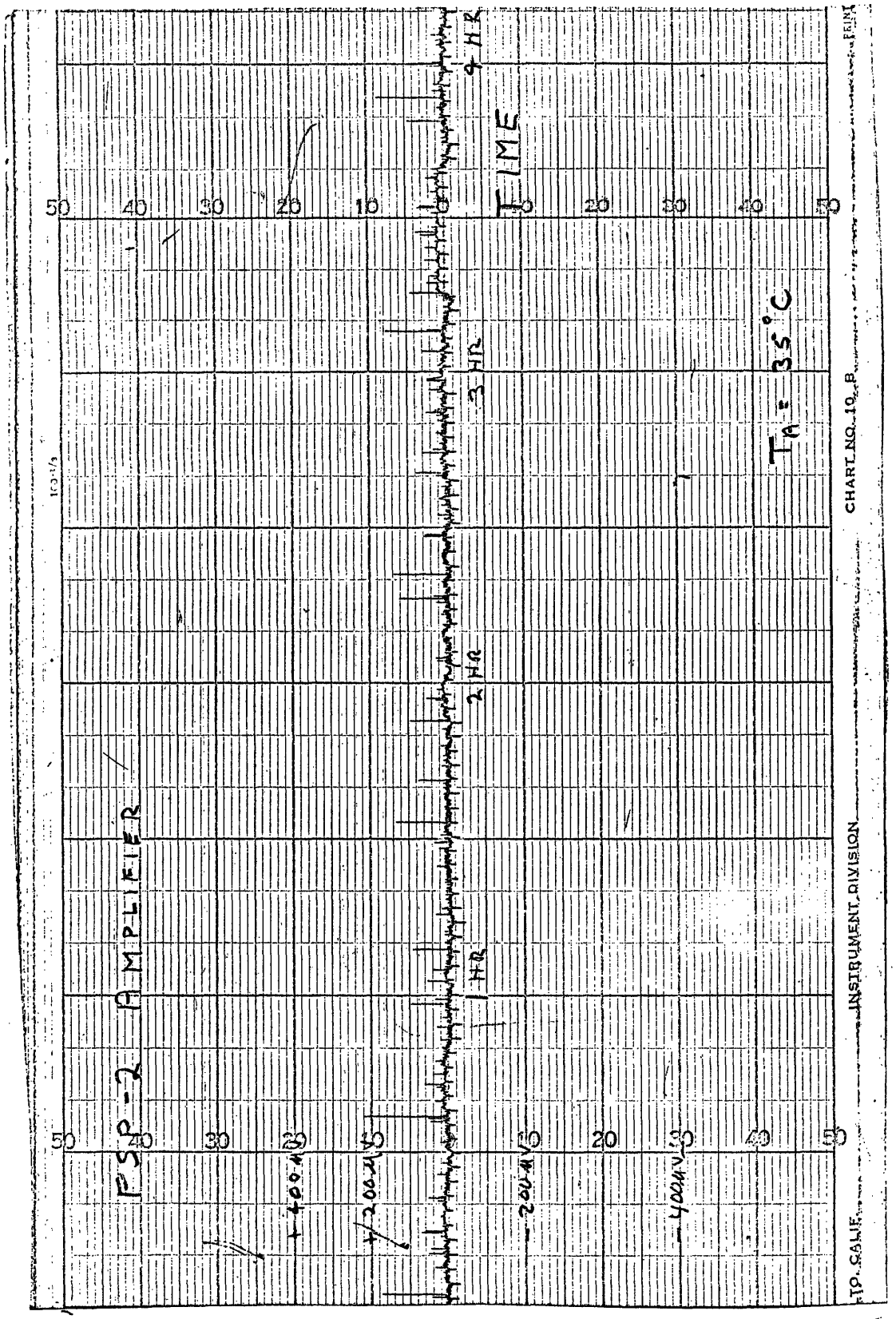

PSP-2 AMPLIFIER
TIME
1 HR
2 HR
3 HR
4 HR
TA = 35°C
CHART NO. 19_B
INSTRUMENT DIVISION

Figure 6.2

microamperes when the transistor switches are closed or an average of 60 microamperes. Since the resistors used in the chopper are highly-stable components, the drift of input impedance should be small.

The output impedance of the chopper is approximately 20K and is therefore small enough so that the switch does not appreciably load the amplifier.

Figure 6.3 is a collection of waveforms taken from the chopper amplifier. The output voltage at the chopper output is shown in Figure 6.3a. The transients are caused by the current switch and on the scale of this photograph the chopper transients are not noticable. Figure 6.3b is the waveform across the sampling resistor with the loads matched. It is noticed that the frequency response is too low, as was mentioned earlier, by the long time constant (about 30 microseconds) that is shown in Figure 6.3c. The effect of the lower gain is seen in the photograph of Figure 6.3d. The load had been mismatched to 2.5 volts with a differential of 40 millivolts occurring between levels at the sensing resistor. This corresponds to an error of about 330 microamps in the controlled current. The noise pulses that appear at switching are caused by feedthrough of the triggering pulse from the pulse generator.

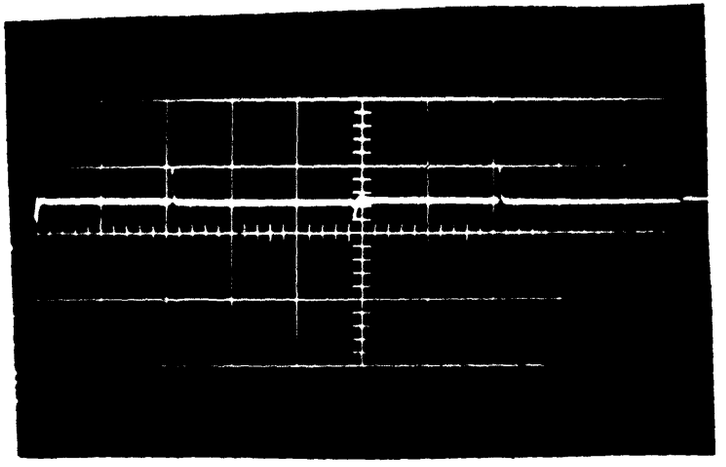
A section of a twenty-four hour drift test is shown in Figure 6.4. There is an obvious drift of about -100 microvolts per hour. It should be pointed out, however, that as the test progressed the drift reversed direction from time to time so that the drift was not constant over the entire 24 hours. There is also a peak to peak noise of about 100 microvolts riding on top of the drift.

6.4 Performance of the Field-Effect Amplifier

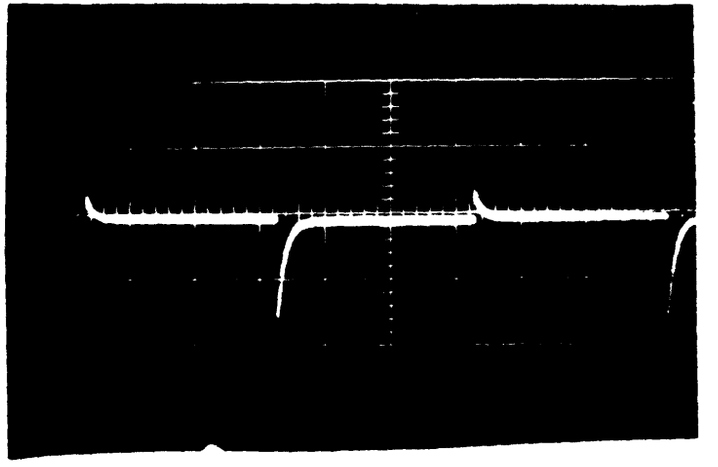
The field-effect amplifier has the advantage of having a very high input impedance, so there are no input stability problems with which to contend.

Since the output stage of the amplifier is identical to that of the FSP-2 amplifier, the output impedance is also in the order of 25K.

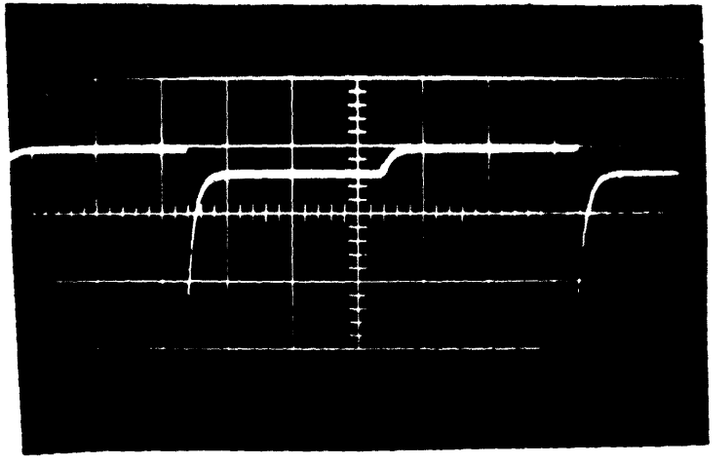
Figure 6.5 shows the waveforms at the amplifier output and across the sensing resistor. The photograph of Figure 6.5a is the output of



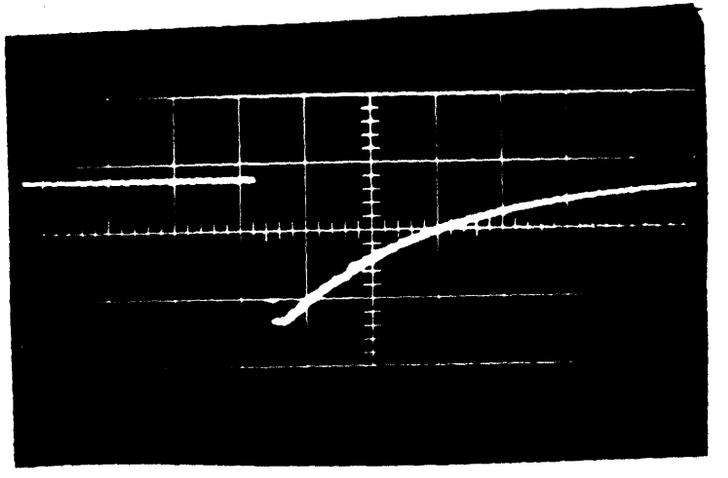
(a) Vert. 50 mv/cm
Horiz. 200 μs/cm



(b) Vert. 100 mv/cm
Horiz. 200 μs/cm



(c) Vert. 100 mv/cm
Horiz. 200 μs/cm



(d) Vert. 100 mv/cm
Horiz. 10 μs/cm

Figure 6.3

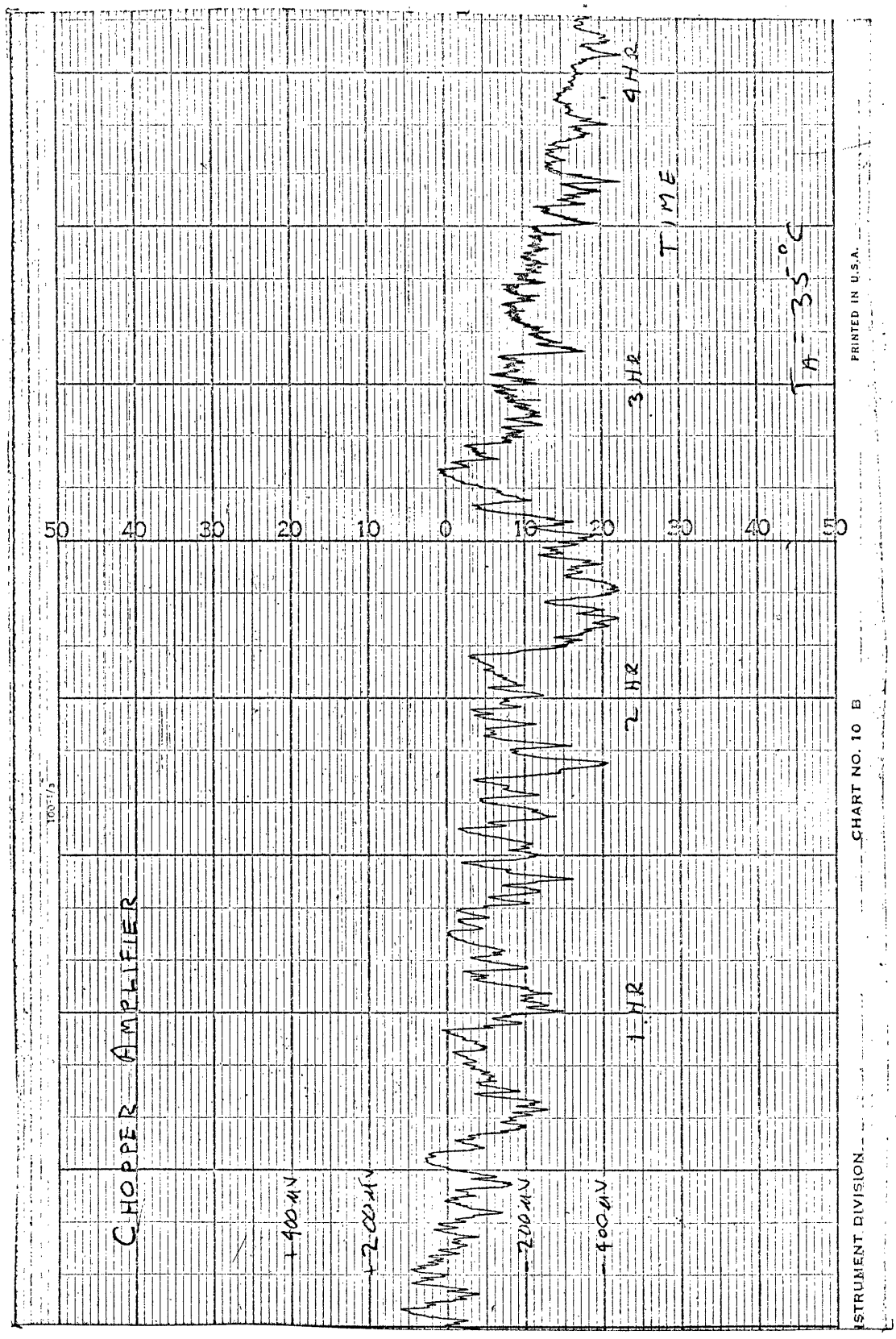

CHOPPER AMPLIFIER
+400 uV
+200 uV
-200 uV
-400 uV
1 HR
2 HR
3 HR
4 HR
TIME
50
40
30
20
10
0
10
20
30
40
50
CHART NO. 10 B
PRINTED IN U.S.A.
INSTRUMENT DIVISION

Figure 6..4

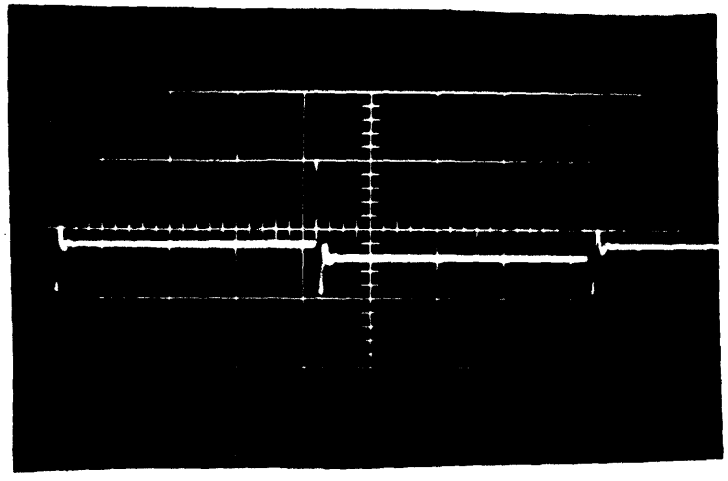
the amplifier for the loads matched to within 100 millivolts. The photograph of Figure 6.5b shows the same output when the loads are mismatched to 600 millivolts. There was no noticable effect upon the waveform of the sensing resistor which is shown in Figure 6.5c. The transient that occurs at switching is shown expanded in Figure 6.5d. As expected, the waveform indicates that the loop is under-damped.

A four hour section of the drift test is shown in Figure 6.6. The transients occurring approximately every two minutes are caused by the turning on of the temperature controller. The constant noise level is about 50 microvolts. It is seen that the drift over four hours was in the order of 50 microvolts for this sample. As was the case for the other amplifiers, this drift would change direction from time to time.

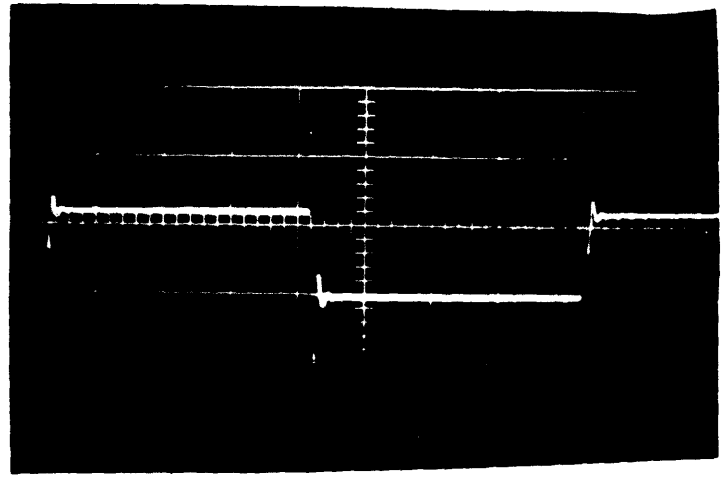
6.5 Summary of Performance

The table below summarizes the performance of the three amplifiers.

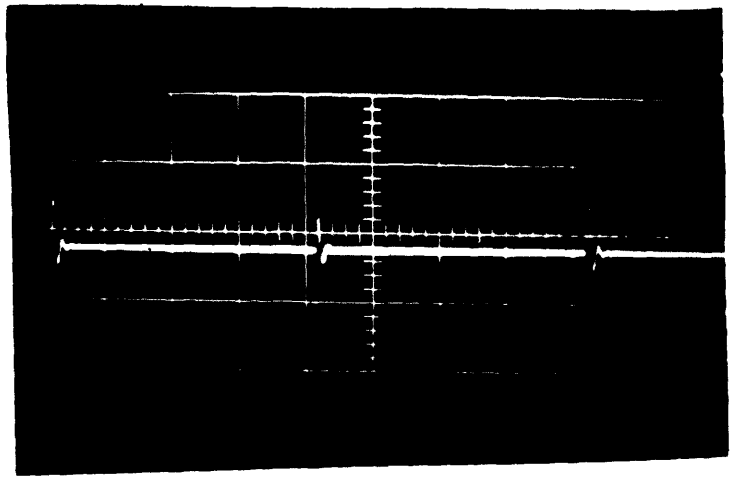
Amplifier	FSP-2 Straight D.C. Amplifier	Chopper d.c. Amplifier	Field-effect d.c. Amplifier
Input Impedance	> 100K	50K or >100 Meg.	> 10 Meg.
Output Impedance	25K	20K	25K
Transient Response	Underdamped	Overdamped	Underdamped
Freq. Response (closed loop)	0 to 30 K.C.	0 to 38 K.C.	0 to 5 cps
Short term drift	< 5 μv/day	100 μv/hr	12 μv/hr



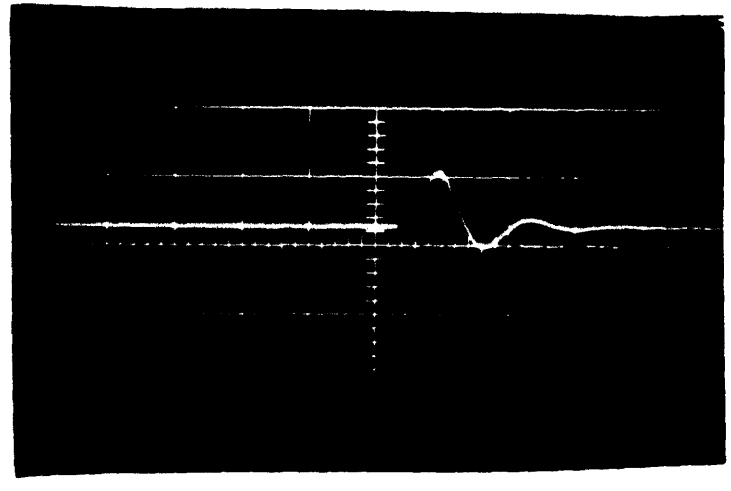
(a) Vert. 500 mv/cm
Horiz. 1 ms/cm



(b) Vert. 500 mv/cm
Horiz. 1 ms/cm



(c) Vert. 50 mv/cm
Horiz. 1 ms/cm



(d) Vert. 50 mv/cm
Horiz. 100 μs/cm

Figure 6.5

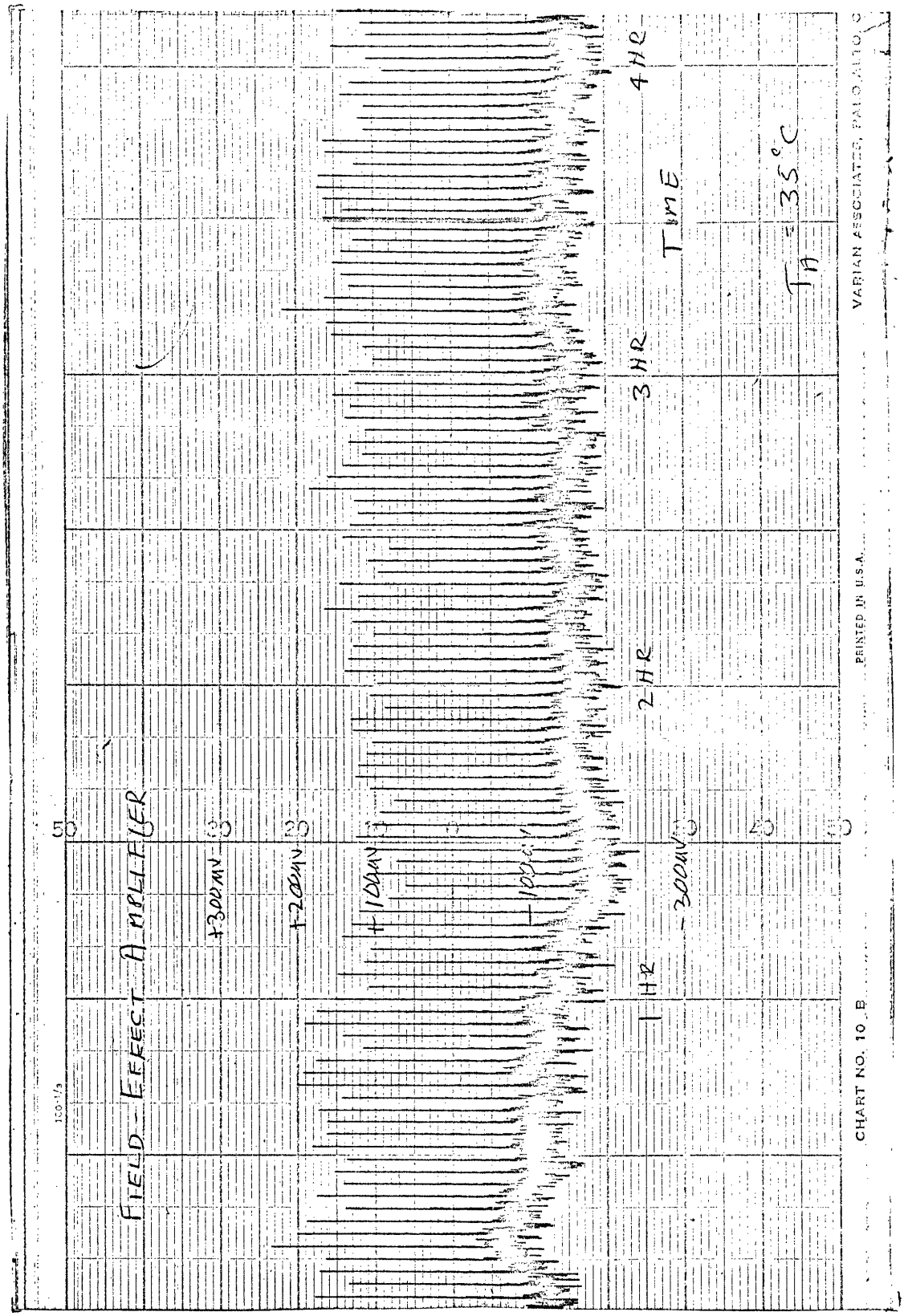

FIELD-EFFECT AMPLIFIER
+300mV
+200mV
+100mV
-100mV
-200mV
-300mV
1 HR
2 HR
3 HR
4 HR
TIME
Tf = 35°C
CHART NO. 10_B
PRINTED IN U.S.A.
VARIAN ASSOCIATES, PALO ALTO, C

Figure 6.6

Chapter VII

Conclusions

7.1 Conclusions

The objective of this paper was to investigate the most recent semiconductor devices on the market and evaluate their use in a low-drift direct-current amplifier. All three techniques investigated have met with some measure of success.

The FSP-2 straight d.c. amplifier has presented the simplest answer to the problem. The design itself is not critical and components are limited to only those necessary to achieve acceptable performance. The two-in-one approach has shown that a "straight" d.c. amplifier can be constructed with as low as 5 microvolts per °C temperature drift without any special temperature compensating circuits and without close tolerance selection of transistors. If transistors are to be selected for stability with temperature variations, it appears that a comparison of the base characteristics along with h_{FE} matching might result in very good temperature stability of a differential amplifier.

The field-effect transistor has also proven its feasability for d.c. amplifier design. The major source of difficulty is the temperature dependency of the transcenductance and the drain current. Although it was thought that matching of these parameters for transistors used in the first stage of a differential amplifier might improve the temperature coefficient of the amplifier, this was not found to be the answer. As pointed out previously, the mechanisms controlling the temperature dependency of the conductivity are complicated, so that the solution to this problem is not completely evident. It is expected that as the state of the art advances for the field-effect transistor, better temperature stability will be achieved. Nevertheless, the amplifier can be compensated for these temperature variations, and good performance can be the result.

It is also felt that the high input impedance of the field-effect transistor is an important factor, and for this reason the device is superior to a conventional transistor for many d.c. amplifier applications.

The chopper amplifier was the poorest of the three amplifiers but not because of the chopper transistors. It was found that the two-in-one approach works very well for minimization of offset errors. Because of its complexity it is believed that the chopper approach is reasonable only when size is not a problem.

Appendix A

A.1 Analysis of a Single-Stage D.C. Amplifier

Figure A.1 is a schematic representation of a single-stage amplifier along with its associated signal flow graph.

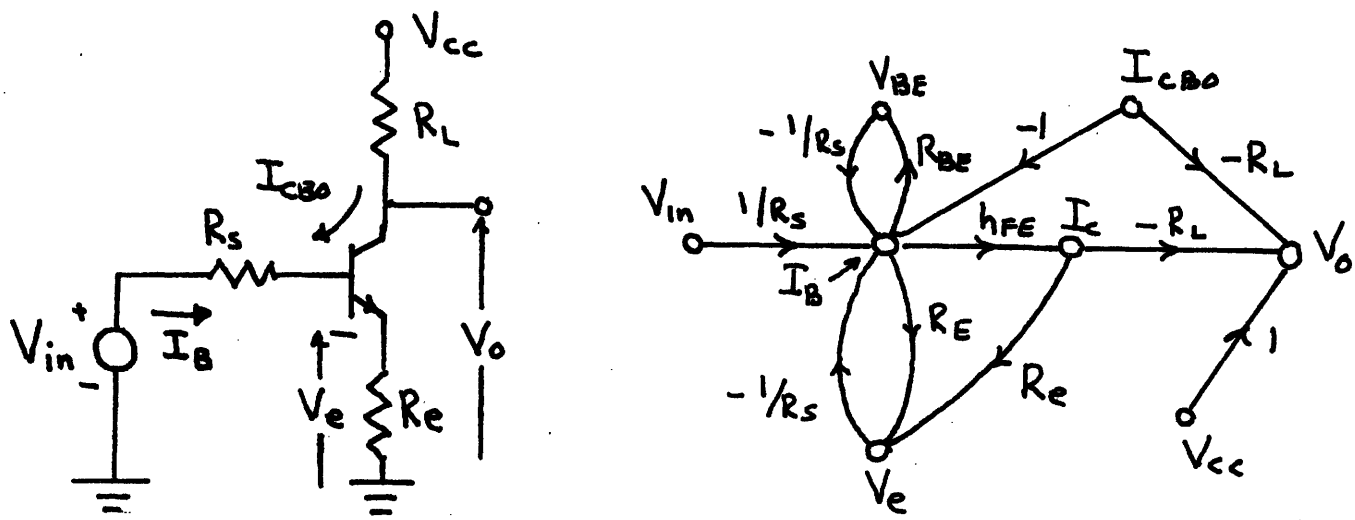


Figure A.1

If V_{BE} is considered an independent source, the output is

$$V_o = V_{CC} - \frac{\frac{h_{FE}\frac{R_L}{R_S}}{1+\frac{R_e}{R_S}(1+h_{FE})}}{}V_{in} + \frac{\frac{h_{FE}R_L}{R_S}}{1+\frac{R_e}{R_S}(1+h_{FE})}V_{BE} + \frac{\frac{h_{FE}R_L I_{CBO}}{}}{\frac{R_e}{R_S}(1+h_{FE})[-I_{CBO}R_L]} \quad (A.1)$$

Considering V_{BE} to be a dependent variable adds another loop in the flow graph as shown by the dotted branch R_{BE}. With this addition the third term on the right side of equation (A.1) vanishes and the determinent of the network changes, so that

$$\Delta = 1 + \frac{R_e}{R_S}(1+h_{FE}) + \frac{R_{BE}}{R_S} \quad (A.2)$$

A.2 Analysis of a Differential D.C. Amplifier

Figure A.2 is the schematic representation of a differential D.C. amplifier along with its associated signal flow graph. The effects of I_{CO} have been neglected, as has the output impedance of the transistors. If V_{BE} is considered to be independent, solution of the flow graph for V_3 results in the following equation.

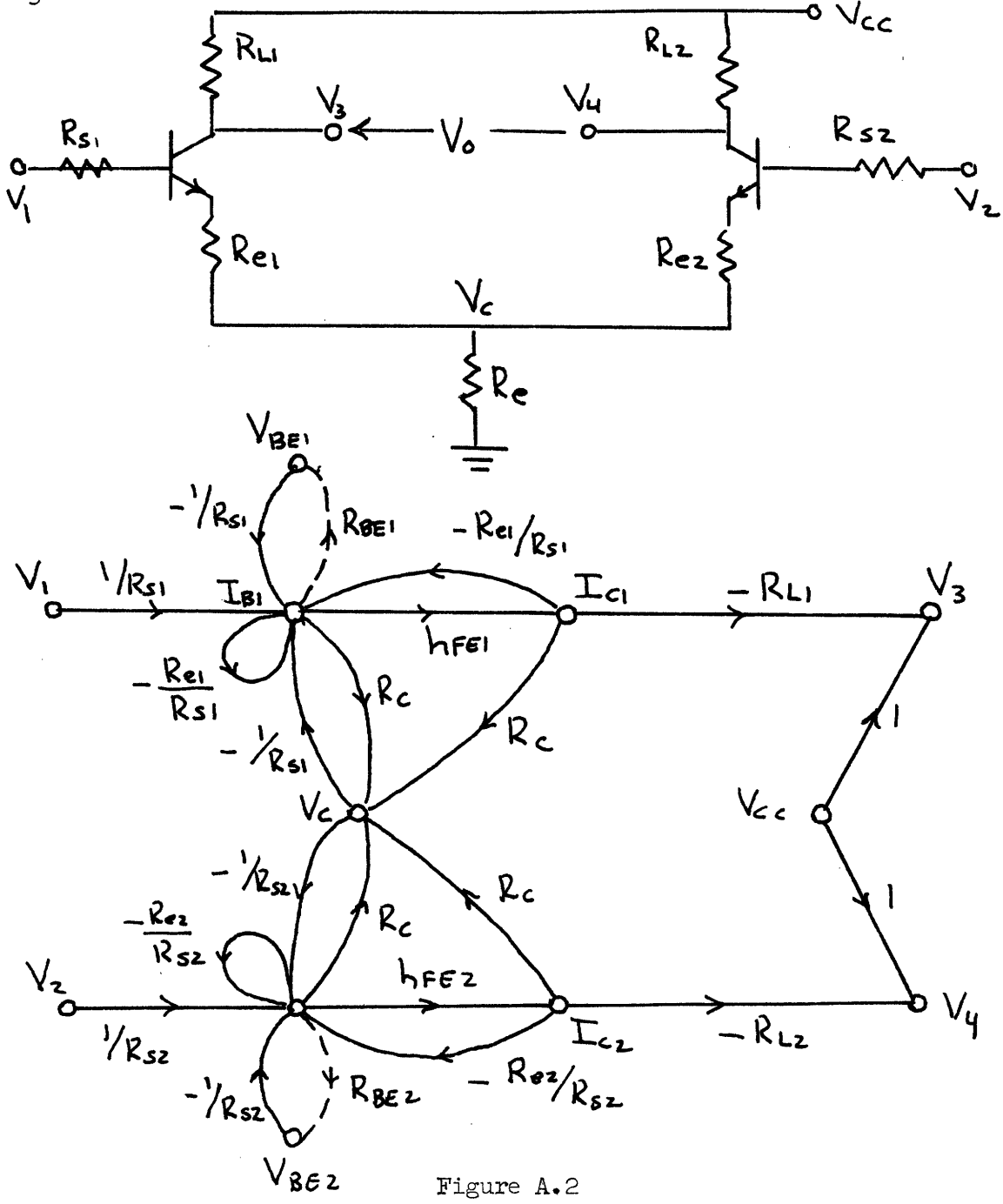


Figure A.2

$$V_3 = V_{CC} - \frac{h_{FE1}\frac{R_{L1}}{R_{S1}}(V_1 - V_{BE1})}{\Delta}\left[1 + \frac{R_C + R_{e2}}{R_{S2}}(1 + h_{FE2})\right]$$

$$+ \frac{h_{FE1}(1 + h_{FE2})\frac{R_C R_{L1}}{R_{S1} R_{S2}}}{\Delta}(V_2 - V_{BE2}) \qquad (A.3)$$

where

$$\Delta = 1 + \frac{R_C + R_{e1}}{R_{S1}}(1 + h_{FE1}) + \frac{R_C + R_{e2}}{R_{S2}}(1 + h_{FE2})$$

$$+ \frac{R_{e1}}{R_{S1}}(1 + h_{FE1})\left[\frac{R_C + R_{e2}}{R_{S2}}(1 + h_{FE2})\right]$$

$$+ \frac{R_C R_{e2}}{R_{S1} R_{S2}}(1 + h_{FE1})(1 + h_{FE2}) \qquad (A.4)$$

If $h_{FE} \gg 1$, $R_C \gg R_{e1}$, $R_C \gg R_{e2}$, then equation (A.3) can be reduced to

$$V_3 = V_{CC} + \frac{h_{FE1} h_{FE2} R_{L1}(V_2 - V_1 + V_{BE1} - V_{BE2})}{h_{FE1} R_{S2} + h_{FE2} R_{S1} + h_{FE1} h_{FE2}(R_{e1} + R_{e2})} \qquad (A.5)$$

In a similar matter the expression for V_4 can be derived, so that

$$V_o = V_3 - V_4 = \frac{h_{FE1} h_{FE2}(R_{L1} + R_{L2})(V_2 - V_1 + V_{BE1} - V_{BE2})}{h_{FE1} R_{S2} + h_{FE2} R_{S1} + h_{FE1} h_{FE2}(R_{e1} + R_{e2})} \qquad (A.6)$$

If the transistors are perfectly matched and if $R_{L1} = R_{L2} = R_L$, $R_{S1} = R_{S2} = R_S$, $R_{e1} = R_{e2} = R_e$, then $V_o = \frac{h_{FE} R_L (V_2 - V_1)}{R_S + h_{FE} R_e}$ (A.7)

If V_{BE} is considered to be a dependent variable, then the two additional loops of the flow-graph in Figure A.2 are added. If this is done it can be found that

$$V_o = \frac{h_{FE} R_L (V_2 - V_1)}{R_{BE} + R_S + h_{FE} R_e} \qquad (A.8)$$

where $R_{BE1} = R_{BE2} = R_{BE}$.

Appendix B

B.1 Analysis of a Single-Stage F.E. Amplifier

Figure B.1 is a schematic representation of a single-stage field-effect amplifier and its associated small-signal equivalent circuit. The flow-graph for this circuit is shown in Figure B.2. In order to simplify the analysis the impedance from source to drain has been neglected along with the input and output capacitances. In the flow graph $R_1 = R_S + R_i$.

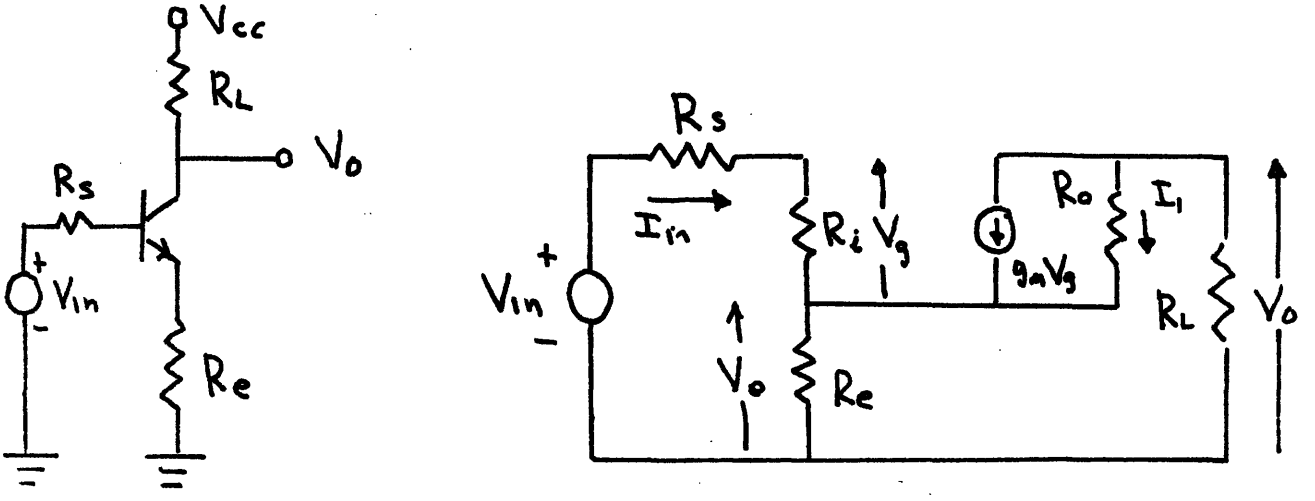


Figure B.1

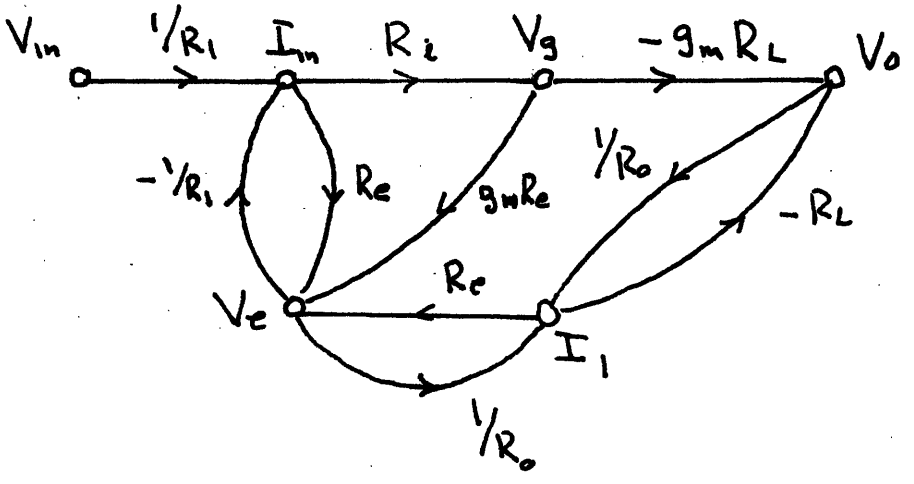


Figure B.2

Solution of the flow-graph for the output voltage leads to

$$V_o = \frac{-\frac{g_m R_L R_i}{R_1}\left(1 + \frac{R_e}{R_o}\right) + \frac{R_e R_L}{R_o R_1}}{\Delta} V_{in} \qquad (B.1)$$

where

$$\Delta = 1 + \frac{R_e(1 + g_m R_i)}{R_1} + \frac{R_L + R_e}{R_o} + \frac{R_e R_L (1 + 2g_m R_i)}{R_o R_i} \qquad (B.2)$$

If both R_i and R_o are large compared to all other resistors in the circuit, then equation (B.1) reduces to

$$V_o = -\frac{g_m R_L}{1 + g_m R_e} \qquad (B.3)$$

B.2 Analysis of a Differential F.E. Amplifier

The equivalent circuit of the field-effect transistor shown in Figure B.3 neglects all impedances of the transistor since these are all large compared to the circuit impedances. The signal flow graph is shown in Figure B.4. Solving for V_3, it is found that

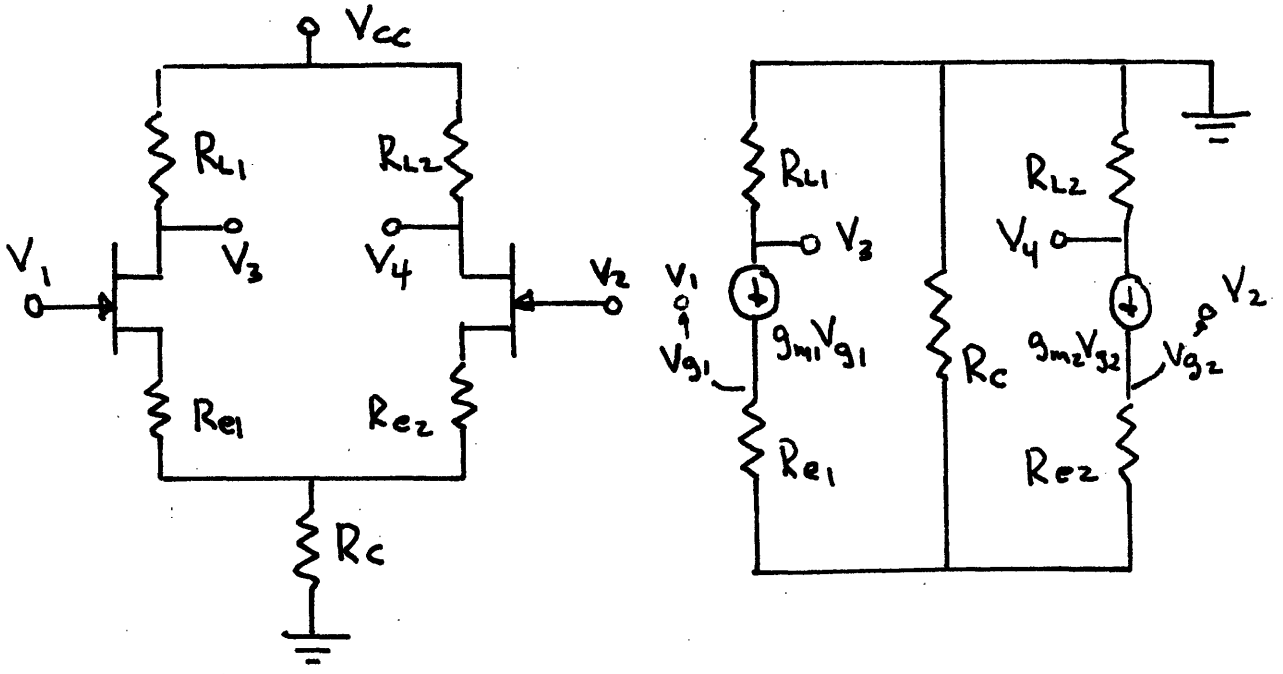


Figure B.3

$$V_3 = - \frac{g_{m1} R_{L1} [\, 1 + g_{m2} (R_c + R_{e2})]\, V_1 + g_{m1}\, g_{m2}\, R_{L1}\, R_c\, V_2}{\Delta} \qquad (B.4)$$

where

$$\Delta = 1 + g_{m1} (R_{e1} + R_c) + g_{m2} (R_{e2} + R_c)$$

$$+ g_{m1}\, g_{m2}\, R_{e1}\, R_{e2} + 2 g_{m1}\, g_{m2}\, R_{e2}\, R_c \qquad (B.5)$$

Similarly, V_4 can be solved for so that the differential output voltage is

$$V_o = V_3 - V_4 = \frac{g_{m2} R_{L2} V_2 - g_{m1} R_{L1} V_1 + g_{m1}\, g_{m2} R_c (R_{L1} V_2 - R_{L2} V_1)}{\Delta}$$

$$+ \frac{g_{m1}\, g_{m2} [R_{L2} (R_c + R_{e1}) V_2 - R_{L1} (R_c + R_{e2}) V_1]}{\Delta} \qquad (B.6)$$

If the circuit is balanced so that $R_{L1} = R_{L2} = R_L$, $R_{e1} = R_{e2} = R_e$ then

$$V_o = \frac{R_L (g_{m2} V_2 - g_{m1} V_1) + g_{m1}\, g_{m2} R_L (2R_c + R_e)(V_2 - V_1)}{1 + (R_e + R_c)(g_{m1} + g_{m2}) + g_{m1}\, g_{m2} R_e (2R_c + R_e)} \qquad (B.7)$$

Also, if $g_{m1} = g_{m2} = g_m$ is substituted into equation (B.7), then it can be factored so that

$$V_o = \frac{-g_m R_L [1 + g_m (2R_c + R_e)]}{(1 + g_m R_e)[1 + g_m (2R_c + R_e)]} (V_1 - V_2) \qquad (B.8)$$

which is simply

$$V_o = - \frac{g_m R_L}{1 + g_m R_e} (V_1 - V_2) \qquad (B.9)$$

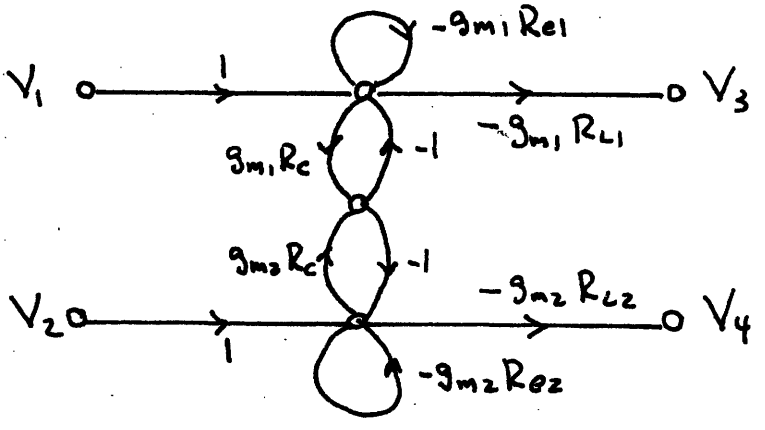


Figure B.4

Appendix C

C.1 Important Characteristics of Fairchild FSP-1 Matched Transistors

Maximum offset voltage 100 V at $I_{B1 \text{ and } 2} = \frac{300 \text{ a}}{}$ $I_{E1 \text{ and } 2} = 0.$
Typical emitter to base cutoff current 0.6 m a at $V_{EB1 \text{ or } 2} = 5V$ $I_C = 0.$
Typical collector to base cutoff current 0.6 m a at $V_{CB1 \text{ or } 2} = 25V$ $I_E = 0.$
Collector to emitter voltage 20V $I_{CE1 \text{ or } 2} = 1$ ma $I_B = 0.$
D.C. Beta ratio between 0.9 and 1.1 at $I_{CE1 \text{ and } 2} = 1.0$ma $V_{CE} = 5V.$

C.2 Important Characteristics of Fairchild FSP-2 Matched Transistors

Minimum D.C. current gain 30 at $I_C = 1$ m.a. $V_{CE} = 10V.$
Typical collector cutoff current 0.8 m a at $V_{CB} = 25V$ $I_E = 0.$
Maximum base voltage differential 30 mv at $I_C = 1$ m.a. $V_{CE} = 5V.$
D.C. beta ratio between 0.9 and 1.1 at $I_C = 1$ m.a. $V_{CE} = 10V.$

C.3 Important Characteristics of Crystalonics C 610 Field-Effect Transistors

Maximum pinch-off voltage 20 volts.
Transconductance between 100 and 400 micromhos at drain voltage of of 24 volts.
Maximum saturated drain current 1 m.a. at drain voltage of 24 volts.
Maximum gate current 0.1 microamps at gate to source voltage of -40 volts.

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