A RADIO FREQUENCY DC-TO-DC RESONANT POWER CONVERTER

by

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ABSTRACT

A 10 MHz dc-to-dc resonant power converter has been designed, constructed, and experimentally evaluated. This converter, which incorporates newly available power MOSFET and Schottky diode technologies, is composed of a current mode sine wave inverter whose output is rectified by a full wave bridge. Linear regulation of the output current is achieved through variation of the switch gating frequency. Radio frequency operation permits the converter, constructed on a printed circuit board, to be smaller, lighter, and cheaper than conventional choppers.

Power MOSFET technology is examined and design constraints are developed. Factors limiting efficiency, switching speed, and power rating are determined. Parasitic elements are identified and a large signal model is developed. This model is used to select an appropriate circuit topology. One major innovation is the incorporation of the parasitic, nonlinear output capacitance of the power MOSFETs into the capacitances of the resonant tank of the power circuit.

The experimental circuit was constructed on a glass epoxy printed circuit board. Parasitic elements were quantified and included in the simulation. The simulation was used to estimate device currents, which could not be measured directly in the experimental circuit. These estimates were used in a power dissipation analysis whose validity was confirmed by experimental temperature measurements.

The experimental converter delivers a peak power of 50 W to a resistive load. The efficiency at that power level, disregarding gate drive losses, is 85%. The results of this thesis suggest that further advances in switching device and magnetic materials technologies may well permit the fabrication of dc-to-dc converters as integrated circuits.

Thesis Supervisor: Dr. John G. Kassakian
Title: Professor of Electrical Engineering

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Chapter One: Introduction

Although the trend in electronics is towards cheaper, smaller, and more modular components, power conditioning equipment remains relatively expensive, large, and heavy. One extremely useful power module would be an inexpensive, lightweight dc-to-dc converter with a wide range of output voltage.

A promising approach to this problem employs a radio frequency dc-to-ac resonant inverter. The output dc level is produced by rectifying the load current and controlled by varying the driving frequency. This scheme provides an output dc level with an easily filtered high frequency ripple, unlike the discontinuous waveforms of conventional choppers. The size and cost of the resonant tank components decrease with increasing frequency, so one would design the resonant inverter to operate at the highest frequency that the switching devices could tolerate.

This limiting frequency is much higher than one would expect with conventional pulse width modulated inverters, since the waveforms in a resonant converter are sinusoidal (or semi-sinusoidal) and continuous, thereby easing the rise and fall time requirements. In addition, the sinusoidal waveforms make the circuit much less prone to ringing and overshoot due to parasitic inductances and capacitances.

The principal disadvantage of resonant circuits is the need for switching devices whose peak voltage and current ratings are higher than the peak output voltages and currents. This requirement may be understood by considering the basic resonant circuit of figure 1.1.

The capacitor is initially charged to a voltage V_p. When switch S1 is open, it must support the full capacitor voltage. When the switch is closed, it must eventually withstand the peak inductor current.

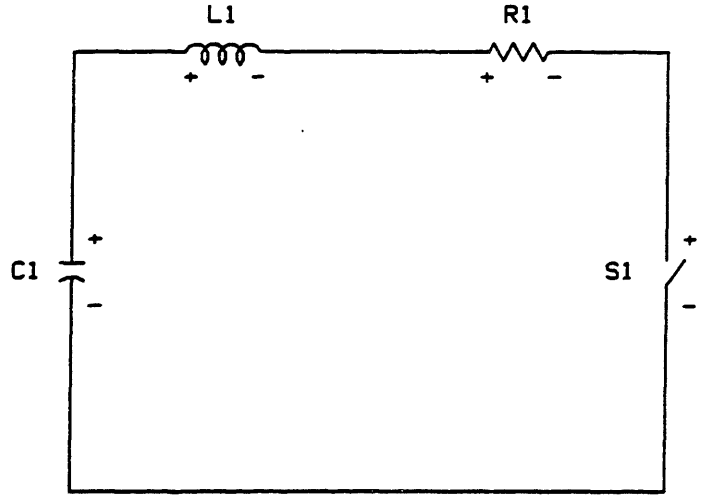


Figure 1.1: Basic Resonant Circuit

After the switch closes, the capacitor voltage obeys

$$v_C(t) = V_p \frac{\omega_o}{\omega_d} e^{-\alpha t} \cos(\omega_d t - \varphi) \tag{1.1}$$

and the inductor current behaves as

$$i_L(t) = -V_p \frac{\omega_o^2 C}{\omega_d} e^{-\alpha t} \sin(\omega_d t) \tag{1.2}$$

where

$$\omega_d = \sqrt{\omega_o^2 - \alpha^2} \tag{1.3}$$

$$\alpha = \frac{R}{2L} \tag{1.4}$$

$$\omega_o = (LC)^{-\frac{1}{2}} \tag{1.5}$$

and

$$\sin \varphi = \frac{\alpha}{\omega_o} \tag{1.6}$$

Equations 1.1 and 1.2 assume that the tank is underdamped, that $\omega_o > \alpha$. This condition is necessary for continuous operation of the inverter.

Neglecting the exponential decay, the peak switch current is therefore

$$I_p = \frac{V_p \omega_o^2 C}{\omega_d} \tag{1.7}$$

The quality factor Q may be defined as

$$Q = \omega_o \frac{W_p}{P_d} \tag{1.8}$$

where W_p is the peak stored energy and P_d is the power dissipated in the resistor. One may combine equations 1.3 through 1.8 to yield an expression for the switch VA rating

$$V_p I_p = \frac{4Q^2 P_d}{\sqrt{4Q^2 - 1}} \tag{1.9}$$

This function reaches its minimum at

$$Q_{crit} = \frac{1}{\sqrt{2}} \tag{1.10}$$

which corresponds to a minimum switch VA rating of

$$V_p I_p = 2P_d \tag{1.11}$$

This approximate analysis suggests that the switch VA rating must be at least twice the rated power of the inverter.

The purpose of this thesis is to investigate the issues involved in radio frequency power conversion and to design, construct, and evaluate a dc-to-dc converter. The specific goal was to develop a converter that, driven around 10 MHz, could deliver at least 25 W. More general goals included determining which factors control maximum efficiency and gating frequency, investigating issues of circuit construction and device behavior, and developing design procedures.

Chapter Two: Resonant Circuit Topologies

2.1: Overview

Several different resonant circuit topologies are examined. A particular circuit and rectification scheme are chosen.

2.2: Resonant Dc-to-Ac Inverters

One representative resonant power circuit is the voltage mode sine wave inverter (fig. 2.1), described in 1967 by Mapham [1]. This double-ended inverter, essentially a series resonant tank tuned closely to the desired output frequency, produces a sinusoidal output voltage with excellent load regulation.

A qualitative description of the circuit operation follows. Both switches, S_1 and S_2, are initially open. Switch S_1 closes, and current flows from the voltage source through the switch, charging the tank capacitor C_1 to a voltage sinusoidally approaching $2V_1$. As the ringing current reverses direction, it flows back to the source via diode D_1 as S_1 commutates, producing the positive half cycle of the output voltage sine wave. Next, S_2 is closed and the other half of the circuit repeats the process, producing the negative half cycle of the output sine wave.

This particular circuit has three major drawbacks with respect to radio frequency operation. First, the resonant tank contains one capacitor and switches between two inductors. A more efficient circuit would contain one inductor and switch between two capacitors, since magnetic components are generally larger, more expensive, and less efficient than their electric duals.

Second, the grounds of the switch drives must float with respect to the power circuit. This is a disadvantage for radio frequency operation, since coupling devices, such as transformers or optoisolators, possess

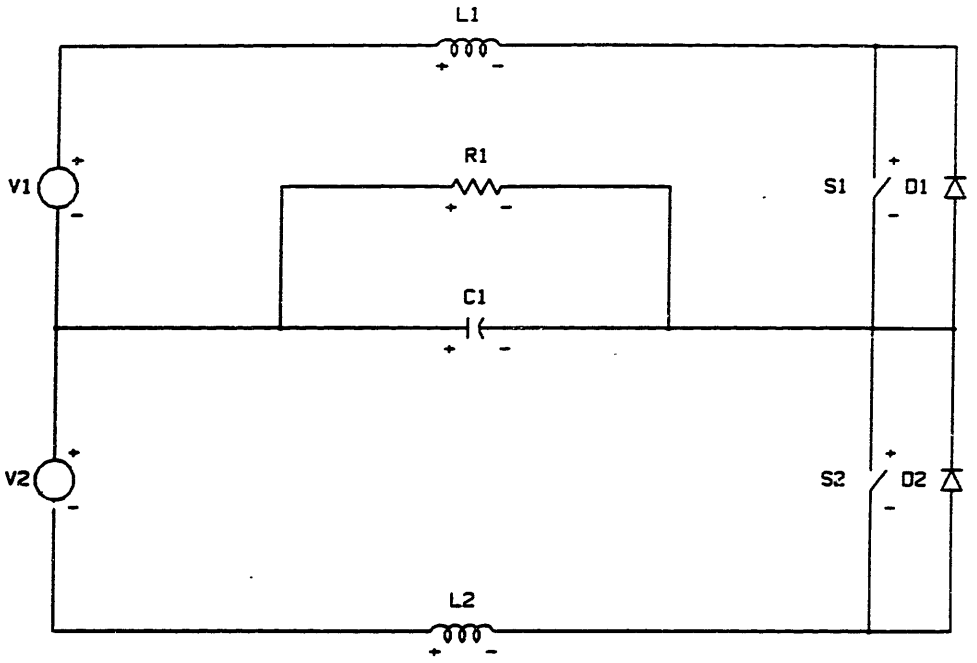


Figure 2.1: Voltage Mode Sine Wave Inverter

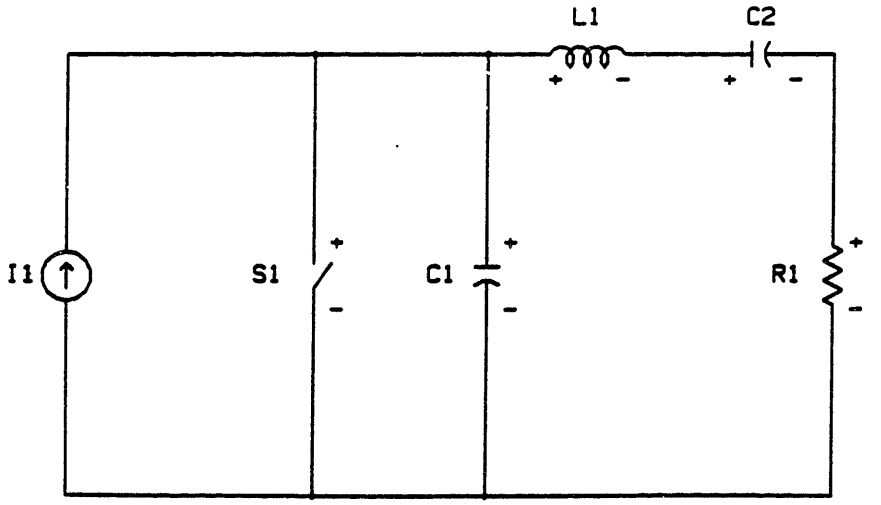


Figure 2.2: Single Ended Current Mode Inverter

large parasitic inductances or capacitances that limit switching speed.

And third, the reverse recovery time of the diodes in the circuit must be extremely short compared to the period of excitation. At radio frequencies this mandates use of Schottky barrier diodes, which are majority carrier devices that do not display reverse recovery. Schottky diodes, however, can not withstand large reverse voltages. Since the diodes are antiparallel with the switches, the maximum forward switch voltage would be determined by the reverse voltage rating of the Schottkies. Since large switch voltages are inherent in a resonant circuit, power output would be severely restricted.

Resonant power circuits were rediscovered in 1975 as "Class E Amplifiers" [2]. The single ended current mode inverter described by the Sokals (fig. 2.2) avoids the disadvantages of the voltage mode circuit. The gate drive can share the power circuit ground, there is only one inductor, and there are no diodes. Although the current source may be realized as a voltage source with a large inductor, the hysteresis losses in this choke inductor are minimal and are determined by the current ripple.

The electrical dual of the voltage mode inverter is the current mode sine wave inverter described by Kassakian [3] and shown in figure 2.3. This circuit also obviates the disadvantages of the voltage mode circuit. This circuit, like its dual, provides excellent load regulation [4]. In addition, both tank capacitors may well be realized as the output capacitances of the switching devices.

The basic operation of the inverter circuit can be understood by considering figure 2.3. Initially, both switches are conducting, constraining the initial capacitor voltage and inductor current to be zero. Switch S_1 is opened, giving the equivalent circuit of figure 2.4, and the state

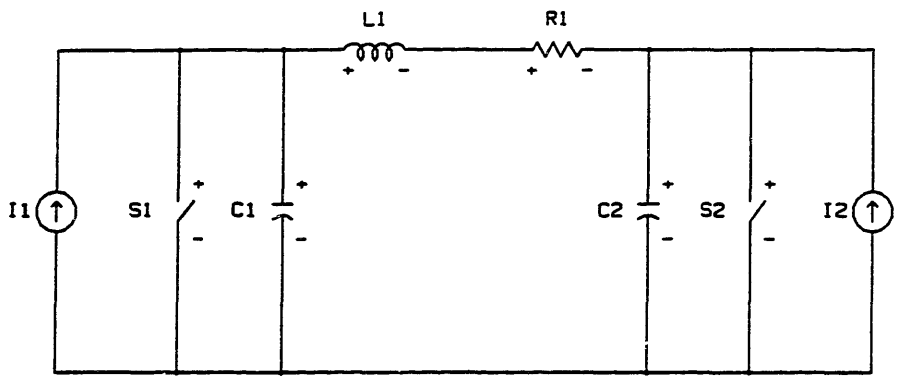


Figure 2.3: Current Mode Sine Wave Inverter

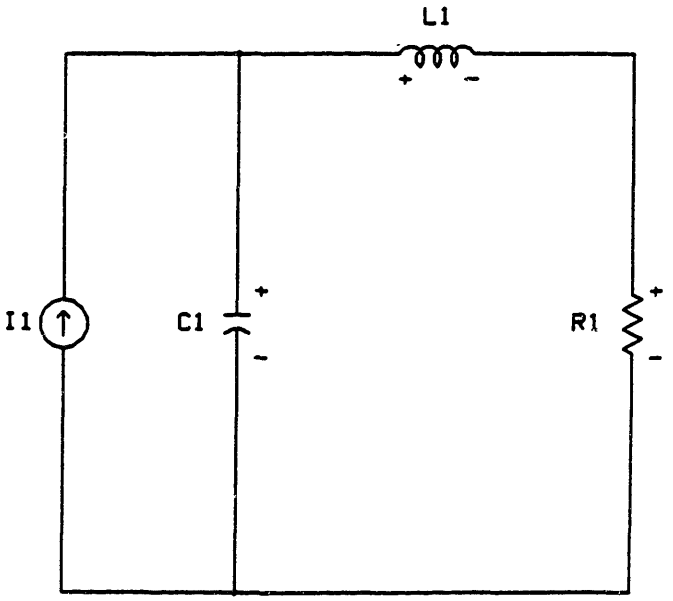


Figure 2.4: Equivalent Circuit

equations are

$$\frac{dv_C}{dt} = \frac{I_{DC} - i_L}{C} \qquad \frac{di_L}{dt} = \frac{v_C - Ri_L}{L} \qquad (2.1\ a,b)$$

where v_C is the capacitor voltage and i_L the inductor current. The solution to this system is

$$v_C(t) = I_o \left[R + \frac{e^{-\alpha t}}{\omega_d C} \sin(\omega_d t - 2\varphi)\right] \qquad (2.2\ a,b)$$

$$i_L(t) = I_o \left[1 + e^{-\alpha t} \left[\frac{\alpha}{\omega_d} \sin(\omega_d t - 2\varphi) - \cos(\omega_d t - 2\varphi)\right]\right]$$

where ω_o, ω_d, α, and φ are defined by equations 1.3 through 1.6.

After the capacitor voltage executes its first decaying semi-sinusoidal cycle, S_1 is closed again. Then S_2 is opened and a complementary cycle occurs. The resultant waveforms are shown in figure 2.5.

A sinusoidal inductor current is achieved by overlapping the times during which both switches are open. Note that the switches are gated when their voltage is near zero. Switching losses, therefore, are low.

2.3: Output Rectification

Radio frequency operation of inverters, however, is impractical, since parasitic inductances or capacitances associated with the load will disrupt the resonant tank. Gutmann [5] suggested the application of microwave circuit techniques to rectify the output of resonant inverters operating in the 10 MHz range. Delivering dc power would insulate the circuit from parasitic inductances and capacitances associated with the load.

At microwave frequencies energy storage elements are easily fabricated with striplines. The gallium arsenide Schottky diodes commonly employed, however, possess significant parasitic resistances and capacitances. Rectification schemes therefore minimize the number of diodes, at the

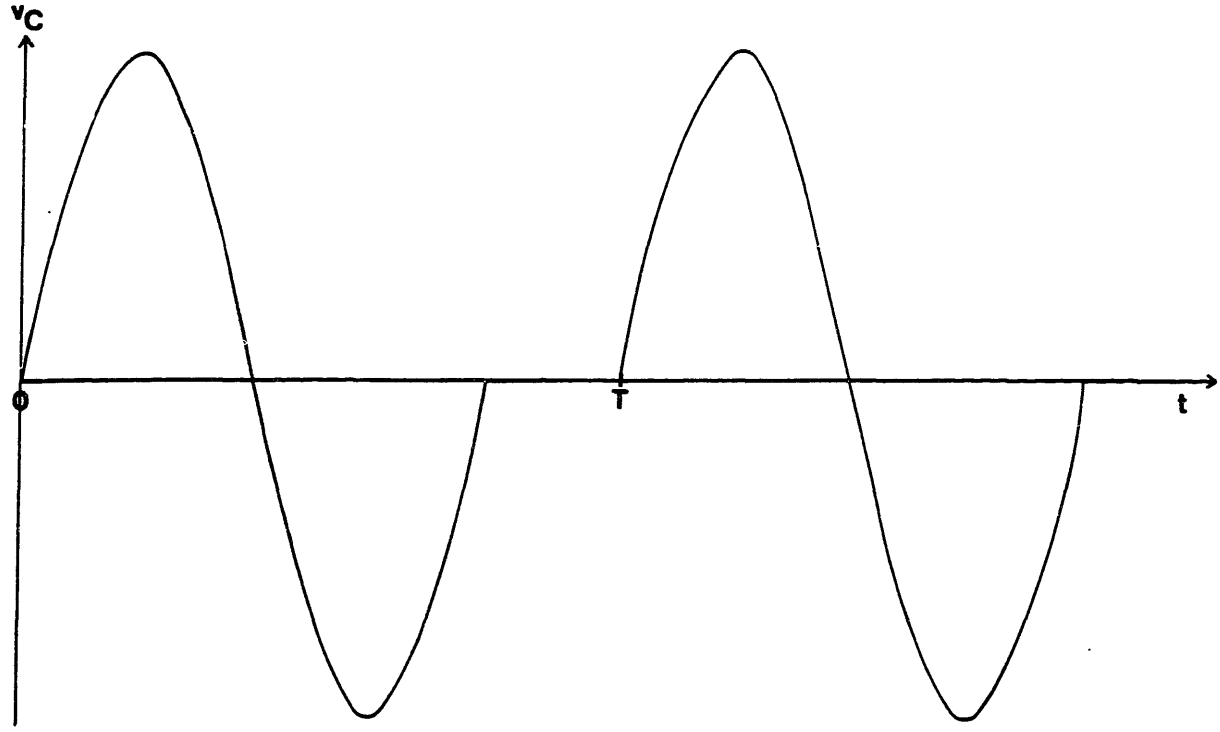


Figure 2.5a: Capacitor Voltage

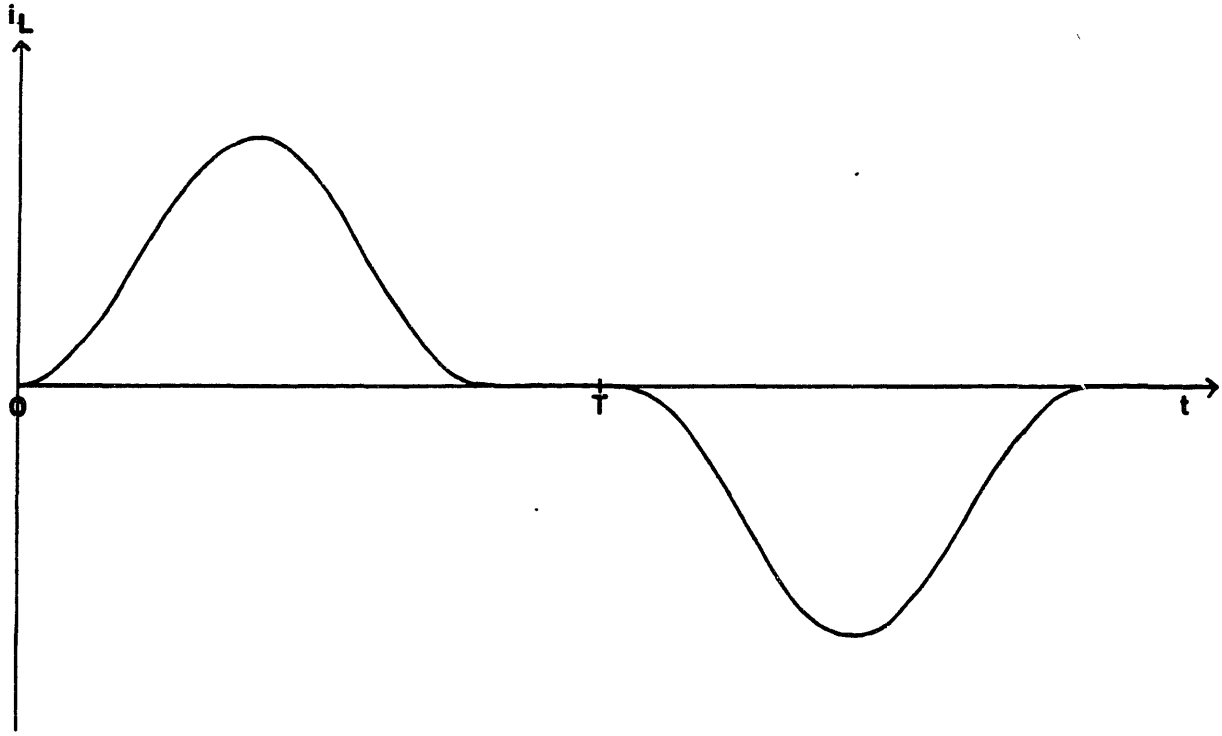


Figure 2.5b: Inductor Current

expense of larger inductors and capacitors.

This tradeoff may be understood by comparing the half wave rectifier, which requires one diode, and the full wave rectifier, which reqires four. The fundamental frequency of the full wave rectifier's output is twice that of the half wave rectifier. Although the full wave rectifier requires four times as many diodes as the half wave circuit, equation 1.5 reveals that the LC product of a tuned harmonic output filter is only one-fourth the size.

Gutmann combined a class E inverter with a lumped parameter version of a microwave power rectifier circuit [6]. The resulting dc-to-dc converter, shown in figure 2.6, employs only one diode and smoothes the output with harmonically tuned filters.

But the practical value of true RF techniques at 10 MHz is limited for two reasons. First, wavelengths are on the order of 3 m, too long for the practical use of striplines. The harmonic filters must be fabricated with many discrete capacitors and inductors. Second, while air core inductors are practical at low power levels, at high power their magnetic fields must be contained in order to prevent coupling to other sections of the circuit. This containment can be accomplished with either ferrites or metal shields. Either approach will introduce power loss and reduce circuit efficiency.

Progress in Schottky diode technology since Gutmann's work further shifts the balance, at 10 MHz, away from energy storage elements and towards diodes [7]. The dc-to-dc converter of figure 2.7 rectifies the output of the current mode inverter with a full wave bridge and smoothes the output with one capacitor [8].

The output dc level is proportional to the switch gating frequency. The slower the gating frequency, the higher the voltages and currents can

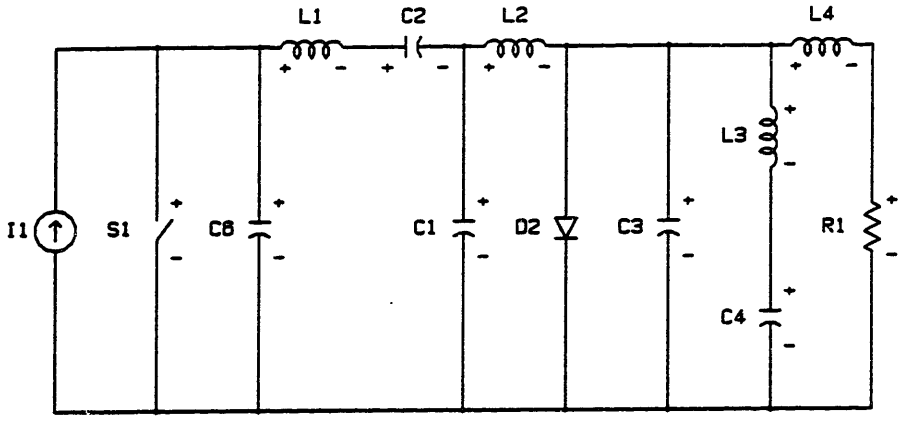


Figure 2.6: Rectified Class E Inverter

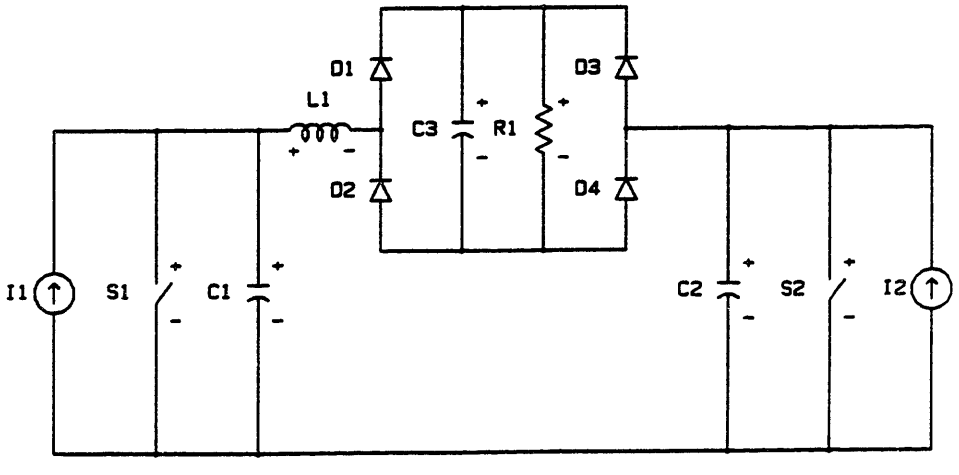


Figure 2.7: Rectified Current Mode Inverter

ring, and the higher the output power. If the circuit is gated too slowly, however, the switch voltage begins to ring positive before the switch is gated, and switching losses are high. If the circuit is gated too quickly, the switch voltage will not have rung all the way to zero at switch turn-on.

The dc-to-dc converter of figure 2.7 was chosen as the topology for this design. This double-ended circuit, which contains only one ac inductor and a simple rectification scheme, promised reasonable power handling ability, efficiency, and linear regulation.

Chapter Three: Power MOSFET Technology

3.1: Overview

MOSFET technology is examined with respect to the high frequency, high efficiency requirements of the power circuit. A switching device is chosen and modeled in order to facilitate the power circuit design.

3.2: Evolution of the MOSFET

Traditional minority carrier devices, such as thyristors and bipolar transistors, can not switch power in the radio frequency range. Thyristors limit the operating frequency to about 25 kHz and power bipolar junction transistors restrict operation to below 100 kHz. Power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETS), on the other hand, are majority carrier devices, and low power MOSFETs can switch at microwave frequencies [9].

The signal level planar double-diffused MOSFET (DMOS) is shown in figure 3.1. In the n-channel device shown, electrons can flow from source to drain when an applied electric field inverts the p-region to n-region. Inversion is initiated by raising the gate-to-source voltage to a threshold voltage, which for this n-channel device is

$$v_T = v_{FB} + \frac{2kT}{q} \ln \frac{N_A}{n_i} + \left(4\frac{N_A kT}{\varepsilon_s} \ln \frac{N_A}{n_i} \right)^{\frac{1}{2}} \qquad (3.1)$$

where kT/q is the thermal voltage, N_A is the channel doping concentration density, n_i is the intrinsic carrier concentration density, ε_s the dielectric permittivity of the semiconductor, and v_{FB} the flat-band voltage [10]. The inversion layer begins to form in the p-region when the conduction band energy falls to the Fermi energy at the oxide-semiconductor interface. The energy band diagram is shown in figure 3.2 [11].

The switching speed of the device is dominated by the charging time of

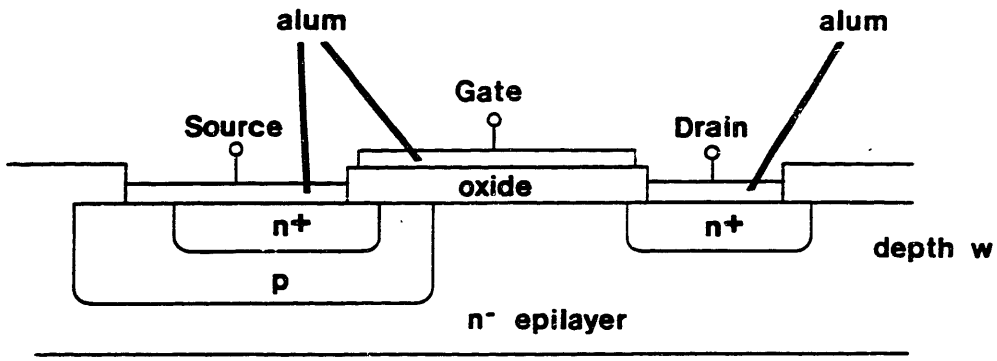


Figure 3.1: Planar MOSFET

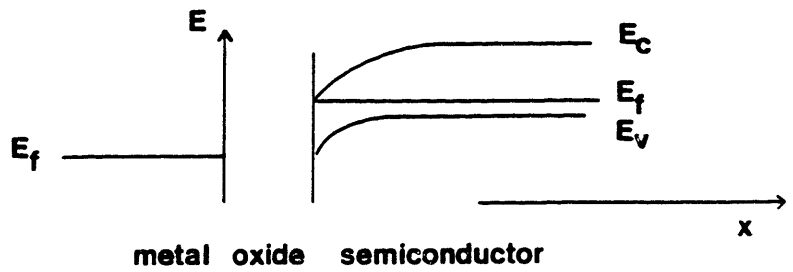


Figure 3.2: Energy Band Diagram

the gate-to-source capacitance. Once this capacitance is charged to the threshold voltage and the inversion layer begins to form, the switch begins to conduct. The channel resistance, however, is very high and power dissipation in the device is severe. Once the gate-to-source voltage is raised far enough to ensure strong inversion in the channel, power dissipation is greatly reduced.

The gate-to-source capacitance has two components. One component is associated with the gate oxide layer, which separates the positive charge on the gate electrode from the negative charge on the semiconductor surface. The magnitude of this oxide capacitance is

$$C_{ox} = \frac{\varepsilon_{ox} LW}{d_{ox}} \tag{3.2}$$

where ε_{ox} is the dielectric permittivity of the oxide layer, L is the channel length, d_{ox} is the thickness of the oxide layer, and W is the channel width in the direction perpendicular to the page in figure 3.1.

When the gate voltage is raised from zero, a depletion region is created at the semiconductor surface as the holes of the p-region drift away from the oxide-semiconductor interface. The depletion capacitance is associated with this separation of charge, and its approximate magnitude is

$$C_{depl} = \frac{\varepsilon_{ox} LW}{d_{depl}} \tag{3.3}$$

where d_{depl} is the width of the depletion region. This width increases with the applied gate-to-source voltage until the inversion layer begins to form. The electric field originating on the gate can then terminate on the mobile electrons available in the inversion region, and any increase in the gate-to-source voltage does not appreciably increase the depletion layer width. The depletion capacitance, therefore, decreases in magnitude until

the gate-to-source voltage reaches the threshold voltage, and then the capacitance remains constant.

The total gate-to-source capacitance is the series combination of the oxide and depletion capacitances. By expressing d_{depl} in terms of device parameters, the gate-to-source capacitance below the threshold voltage can be written as

$$C_{gs} = \frac{\varepsilon_{ox}}{d_{ox}} LW \left[1 + \frac{2\varepsilon_{ox}{}^2 v_{GS}}{qN_A \varepsilon_s d_{ox}^2} \right]^{-\frac{1}{2}} \tag{3.4}$$

where v_{GS} is the gate-to-source voltage [12]. Above the threshold voltage, the capacitance is

$$C_{gs} = \frac{\varepsilon_{ox}}{d_{ox}} LW \left[1 + \frac{2\varepsilon_{ox}{}^2 v_T}{qN_A \varepsilon_s d_{ox}^2} \right]^{-\frac{1}{2}} \tag{3.5}$$

In addition to the gate-to-source capacitance, there is a gate-to-drain capacitance created by the intentional extension of the gate electrode over the drain region. When the device is turned on, the electric field originating on the extended gate electrode terminates in the drain region, enhancing the carrier concentration and decreasing the on-state resistance of the MOSFET.

The power loss of this planar DMOS device is dominated by the channel resistance. When the switch is on, the resistance is

$$R_c = \frac{Ld_{ox}}{\mu_e \varepsilon_s W v_{GS}} \tag{3.6}$$

where μ_e is the electron mobility [13].

In order to minimize the switching time and the power loss, the capacitance and the channel resistance must be minimized. Comparison of equations 3.4, 3.5, and 3.6 show that this can be achieved by minimizing the channel length L. Short channel planar DMOS, however, is not appropriate

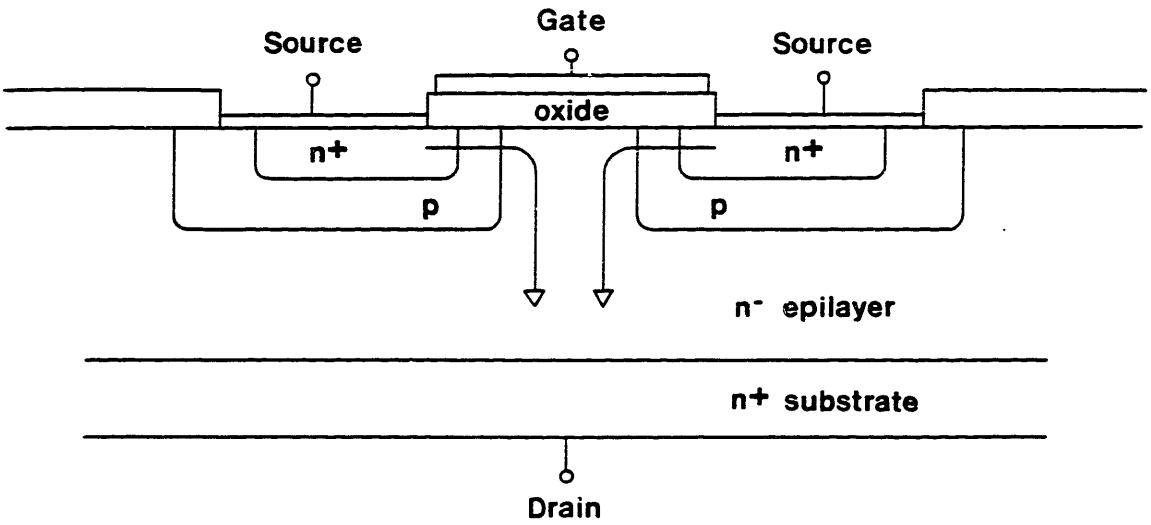


Figure 3.3: Vertical DMOS

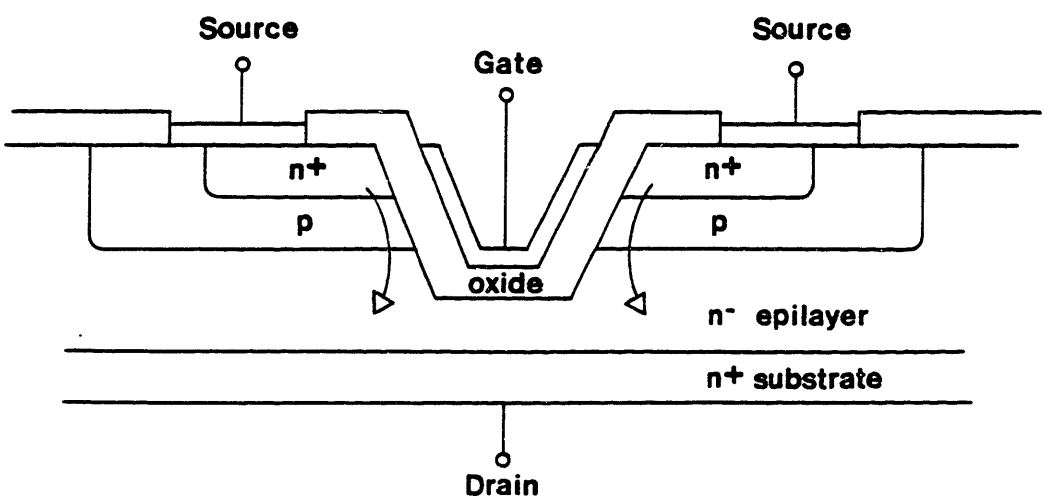


Figure 3.4: VMOS

for power devices, since when the device is blocking forward voltage, the drain-channel depletion region may expand all the way through the epilayer to the drain and cause device breakdown [14].

The two major topologies that overcome this problem are the vertical DMOS device, shown in figure 3.3, and a vertical V-groove structure, VMOS, illustrated in figure 3.4 [15]. These two devices are very similar and their operation can be understood by considering figure 3.3. In the n-channel cell pictured, electrons flow from each of the two sources through the two channels and down through the epilayer to the drain. The channel is short, as required, and the depletion layer forms primarily in the lightly doped epilayer. Hence a large voltage can be supported by extending the epilayer, at the cost of additional series resistance. The resistance of the FET can be reduced at the cost of increasing the capacitance by paralleling cells on a single substrate. The VMOS device is almost identical, except that the gate has been distended in order to spread the current, as shown by the arrows in figure 3.4, and thus reduce the series resistance. The larger gate, however, means a larger gate-to-source capacitance.

One possible method of greatly reducing both on-resistance and switching time would be to fabricate the vertical DMOS device from gallium arsenide, rather than silicon [16]. Experimental attempts to construct such devices, however, have so far failed to achieve inversion [17].

3.3: Device Selection and Modeling

The MOSFET selected for the power circuit was the Motorola MTP8N10. The data sheets appear in the appendix. This device, selected for its particular balance of on-resistance, 0.5 ohms, and its gate-to-source capacitance, about 400 pF, has a vertical DMOS structure and polysilicon

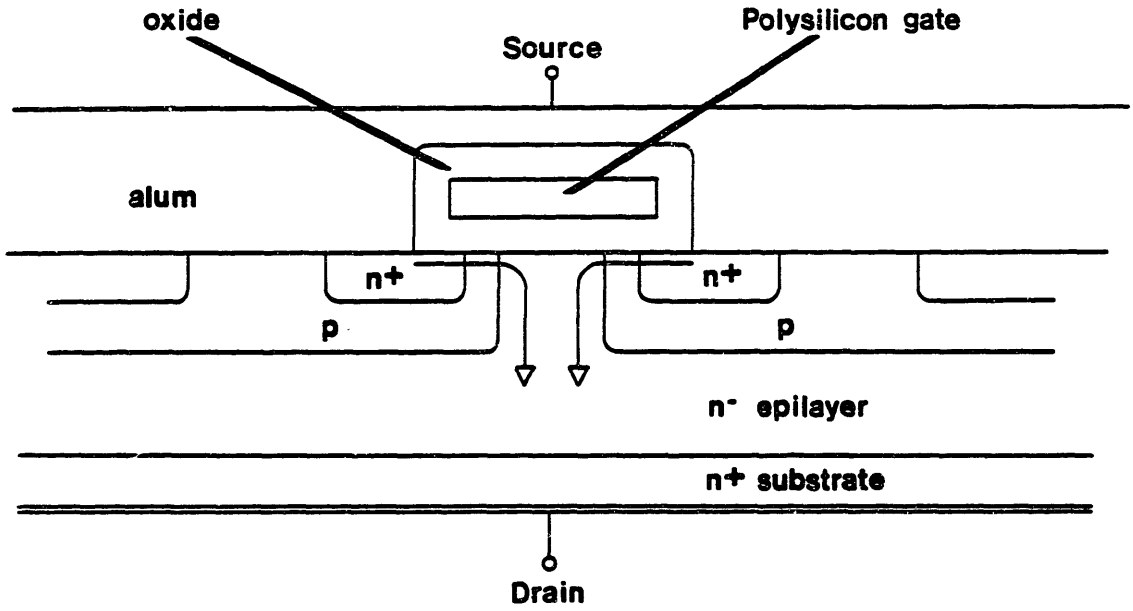


Figure 3.5: Motorola TMOS

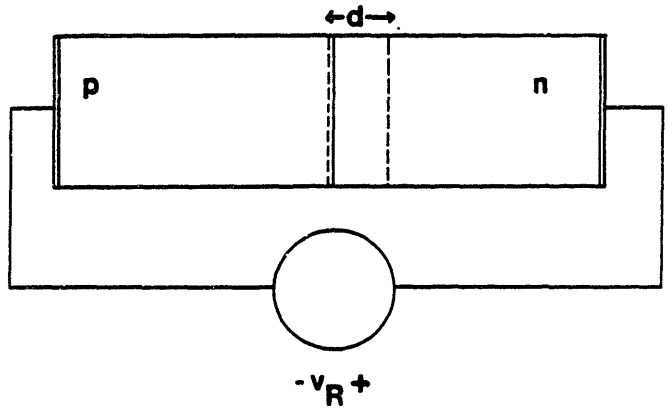


Figure 3.6: Reverse Biased PN Junction

gate, as shown in figure 3.5. The cells are packed in a square array and the source aluminization extends over the surface of the chip [18].

Although polysilicon has a higher resistance than aluminum, and therefore contributes a larger RC time constant to the gate voltage rise time than an equivalent metal gate would, it is easier to align [19]. This alignment is crucial, since any overlap of the gate with the source increases the input capacitance. The metallization of the entire surface, however, greatly increases the gate-to-source capacitance. An interdigitated topology has been proposed where the source metallization does not cover the gate [20].

The overlap of the source metallization with the p-region of the body is of great importance, as this shorts out the base-emitter junction of a parasitic bipolar transistor that appears in parallel with the device. This overlap, however, creates a parasitic pn junction diode anti-parallel with the MOSFET. This switch, therefore, can not support reverse voltage. This is an attribute of all currently manufactured power MOSFETs. The depletion capacitance associated with this parasitic diode dominates the output drain-to-source capacitance of the switch. The magnitude of this capacitance must be determined empirically, due to the complicated geometry, but the functional dependence of the capacitance can be estimated by considering a planar pn junction.

The depletion capacitance of the diode shown in figure 3.6 is

$$C_{depl} = \frac{\varepsilon_s A}{d} \tag{3.7}$$

where A is the cross-sectional area of the device and d is the width of the depletion region. Since the p-region of the FET is much more heavily doped than the n-epilayer, most of the depletion layer extends into the n-region.

Assuming in this diode model that the p-region is much more heavily doped than the n-region, the depletion region width is

$$d = \left\{ \frac{2\epsilon_s}{qN_D} \left[\frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} + v_R \right] \right\}^{\frac{1}{2}} \tag{3.8}$$

where N_A and N_D are the p and n-region dopant concentration densities and v_R is the applied reverse voltage as shown in figure 3.6 [21]. For a reverse voltage whose magnitude is much greater than a volt, the voltage dependence of the capacitance is

$$C(V) \approx K\, V^{-1/2} \quad ; \quad K = A \left[\frac{qN_D\epsilon_s}{2} \right]^{\frac{1}{2}} \tag{3.9}$$

When the drain-to-source voltage of the FET is large, equation 3.9 is a good approximation for the output capacitance. The constant K may be determined from the manufacturer's data sheets.

Finally, there is a capacitance between gate and drain, formed by the overlap of the gate with the epilayer. This capacitance may be reduced by reducing the distance between the p-diffusions. If this separation distance is too small, however, the depletion regions associated with each $p\text{-}n^-$ junction will meet, forming a parasitic junction field effect transistor.

The large signal power MOSFET model is shown in figure 3.7, incorporating a gate controlled switch Q, the nonlinear gate-to-source capacitance C_{gs}, the nonlinear gate-to-drain capacitance C_{gd}, the nonlinear drain-to-source capacitance C_{ds}, and the on-state resistance R_{on}. Manufacturers usually specify the capacitances in terms of C_{iss}, C_{oss}, and C_{rss}, where these are defined as

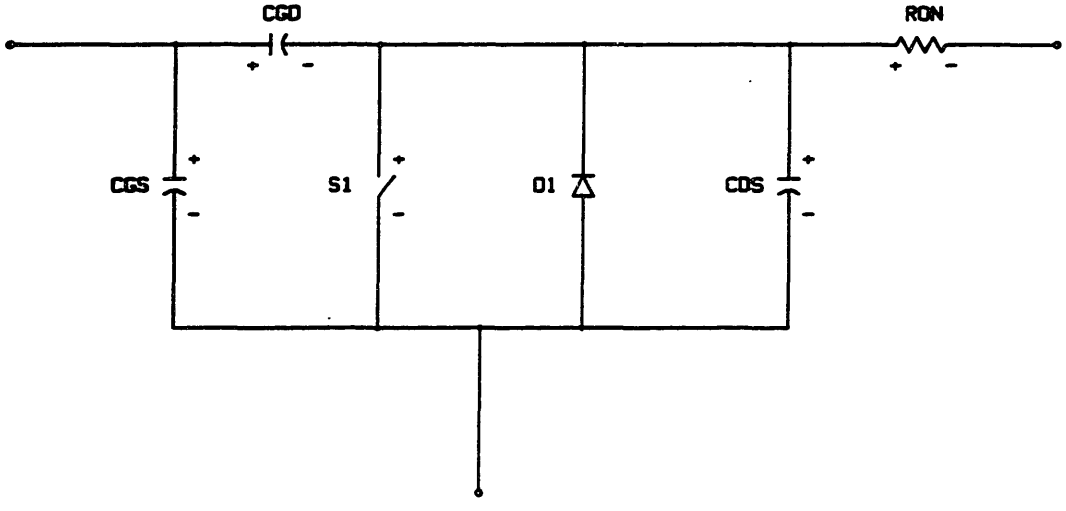


Figure 3.7: Large Signal Power MOSFET Model

$$C_{iss} = C_{gs} + C_{gd} \tag{3.10}$$

$$C_{oss} = C_{ds} + C_{gd} \tag{3.11}$$

$$C_{rss} = C_{gd} \tag{3.12}$$

The input capacitance C_{iss} is, in practice, increased by the Miller effect. This effect, caused by the feedback capacitance C_{gd}, may be understood through the following qualitative description. When the gate-to-source voltage is raised from zero to its maximum value, the channel progresses from weak to strong inversion. Since the channel resistance is modulated by the gate voltage during this progression, the MOSFET effects a voltage gain A_v, such that

$$v_{ds} = A_v \, v_{gs} \tag{3.13}$$

The change in voltage across the gate-to-drain capacitance for a change in input voltage is therefore

$$\Delta v_{gd} = [1 - (-A_v)] \, \Delta v_{gs} \tag{3.14}$$

In some incremental time Δt the additional charge the driver must supply to C_{gd} is

$$\Delta q = C_{gd} \, \Delta v_{gd} = (1 + A_v) \, C_{gd} \, \Delta v_{gs} \tag{3.15}$$

The Miller effect, therefore, multiplies the input capacitance by approximately the gain of the circuit. An analogous analysis holds for turn-off.

3.4: Summary

The DMOS device chosen for the design, the Motorola MTP8N10, is limited in switching speed by its input capacitance and in power handling by its on-resistance. These limitations are reflected in the large signal model of figure 3.7.

Chapter Four: Power Circuit Design

4.1: Overview

The nonlinear nature of the converter of figure 2.7, repeated here as figure 4.1, makes circuit analysis extremely difficult. The design was iterated, with each analysis more exact than the one before.

First, the inverter of figure 2.3 was considered as an ideal resonator and approximate relations were derived. The next iteration used the MOSFET model of chapter three and incorporated the drain-to-source capacitances as the resonant capacitors of the circuit. The circuit was analysed with numerical techniques, as well as Parity Simulation [22]. Finally, the full wave bridge was added to the design and the full converter was simulated.

4.2: Approximate Relations

Approximate formulae for the value of the circuit components of figure 2.3 can be derived as follows. Considering the circuit as a resonator, one can equate the peak electric energy stored in each capacitor with the peak magnetic energy stored in the inductor.

$$\tfrac{1}{2}Li_{L,peak}^2 = \tfrac{1}{2}Cv_{C,peak}^2 \tag{4.1}$$

This can be cast in the form

$$\frac{i_{L,peak}^2}{v_{C,peak}^2} = \frac{L}{C} = Y_o^2 \tag{4.2}$$

where Y_o is the characteristic admittance of the resonator. The peak current in the switch is approximately the total current from one dc current source plus the peak inductor current.

$$i_{switch,peak} = I_{DC} + (Y_o\, v_{C,peak}) \tag{4.3}$$

Approximating the switch current as a rectangular pulse, the rms current can be expressed as

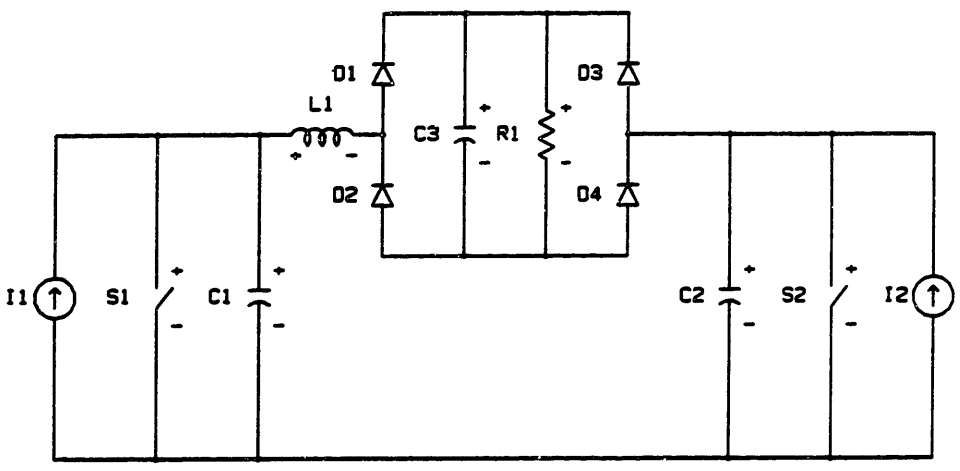


Figure 4.1: Dc-to-Dc Converter

$$i_{switch,rms} = \sqrt{T_{on}/T_{total}}\,[I_{DC} + (v_{C,peak}\,Y_o)] \qquad (4.4)$$

Equations 2.3, 4.3, and 4.4, together with the peak voltage, current, and rms current ratings of the switches, as well as the maximum frequency of the gate drive, give design criteria for the resonant inductor and capacitors.

The Q of the resonant tank should be minimized, as this minimizes the peak device currents and voltages. If the load resistance is too large, however, the switch voltage does not ring to zero. The devices would, in that case, be gated on while still supporting a large forward voltage. Switching losses would be large. The Q of this circuit is

$$Q = (Y_o R)^{-1} \qquad (4.5)$$

and for this circuit was empirically determined to be optimal at about 3.0.

Additional constraints arise from the non-ideality of the physical components. Parasitic inductances and capacitances mandate minimum values of the tank components, and the on-state resistance of the FETs reduces the allowable load resistance.

4.3: Including the MOSFET Model

The dominant parasitic effect in the power circuit is the drain-to-source capacitance of the MOSFET. One major innovation of this design was to use this capacitance as the resonant capacitor of the tank circuit. This reduces the size and cost of the circuit, as well as eliminating any lead inductance between the switch and capacitor. Such inductance would cause potentially disastrous voltage ringing.

This resonant capacitance, however, is a nonlinear function of voltage, as given by equation 3.9. For such a capacitor the charge Q is

$$Q = Cv_C = Kv_C^{-\frac{1}{2}}v_C = Kv_C^{\frac{1}{2}} \qquad (4.6)$$

and the current i is

$$i_C = \frac{dQ}{dt} = K \frac{dv_C^{\frac{1}{2}}}{dt} \qquad (4.7)$$

Making the substitutions

$$x_1 = v_C^{\frac{1}{2}} \quad ; \quad x_2 = i_L \qquad (4.8\,a,b)$$

the state equations for the circuit of figure 2.4 can be written in a form very similar to equations 2.1(a,b):

$$\frac{dx_1}{dt} = \frac{I_{DC} - x_2}{K} \quad ; \quad \frac{dx_2}{dt} = \frac{x_1^2 - Rx_2}{L} \qquad (4.9\ a,b)$$

These equations are valid for the positive voltage ring of the capacitor, since the body-drain diode will clamp the reverse voltage. The x_1^2 term in equation 4.9(b) renders this system both nonlinear and insoluble. The equations were numerically integrated using a fourth order Runge-Kutta algorithm [23].

The input current I_{DC} was assumed to be 1 A. The constant K was evaluated using the data sheets in the appendix as 950×10^{-12} coulombs/volt$^{\frac{1}{2}}$, and the resistance, 20 Ω, and the inductance, 0.5 μH, were determined by iterating the previously derived expressions, the numerical integration, and a Parity Simulation employing linear capacitors. The Parity Simulator, a digitally controlled analog simulator of power electronic circuits, can model circuits with linear elements and ideal switches, and can provide approximate real-time simulations of this nonlinear circuit.

The results of the numerical integration are plotted in figures 4.2 and 4.3. Figure 4.2 shows the predicted positive voltage ring of the nonlinear MOSFET output capacitance. Also plotted is the curve for a linear capacitance, 111 pF, that results in a sinusoidal ring of the same period. Using this value of capacitance in equation 2.3 yields a resonant

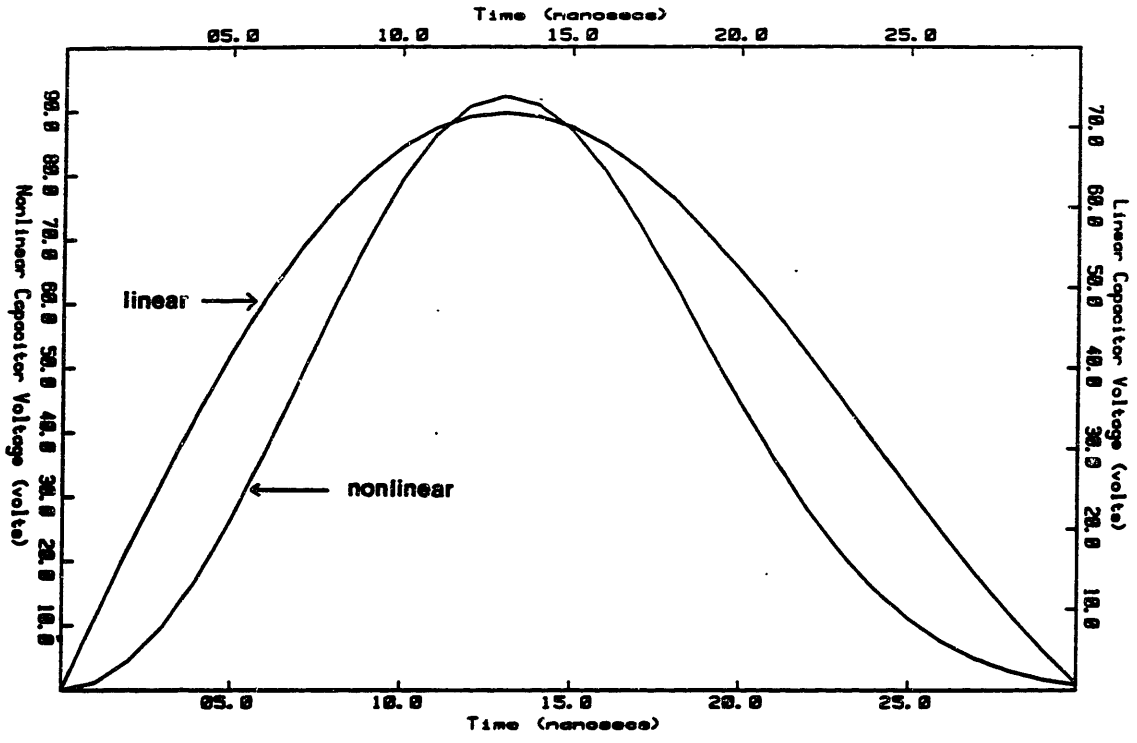


Figure 4.2: Estimated Capacitor Voltages

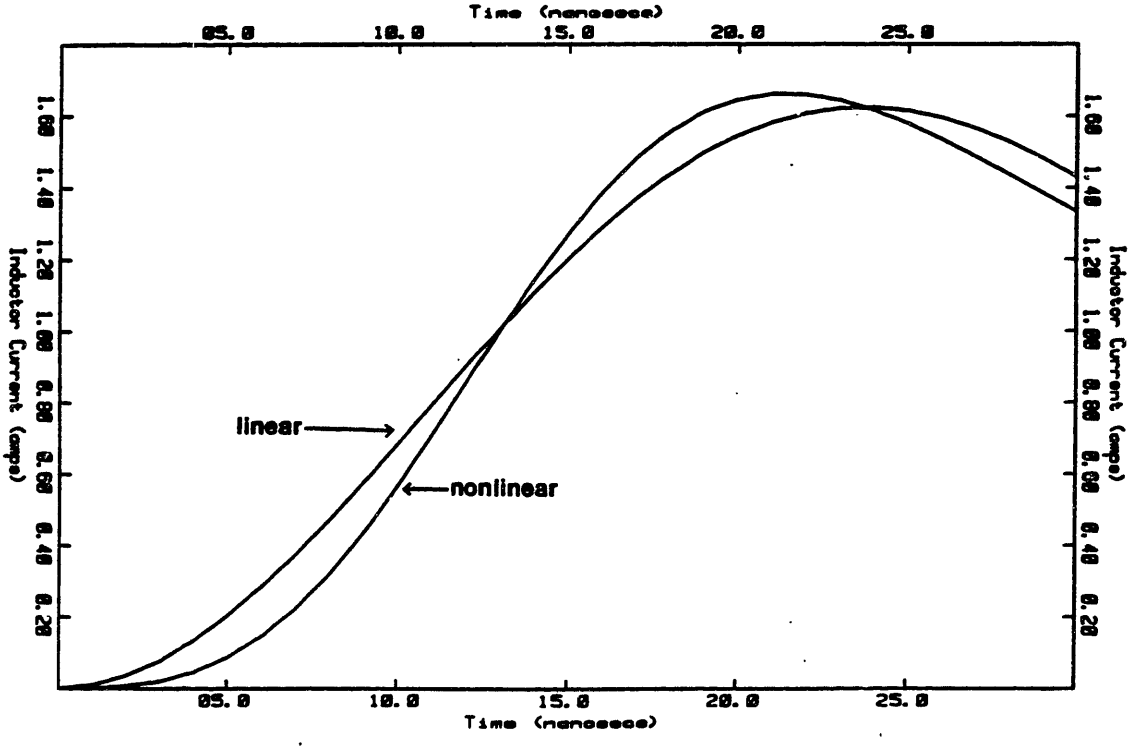


Figure 4.3: Estimated Inductor Currents

frequency of about 21 MHz. The squashed-in peak of the nonlinear capacitance voltage waveform is due to the reduced capacitance at higher voltages. Figure 4.3 shows the predicted inductor current for both the linear and nonlinear cases.

Figure 2.5, however, demonstrates that both switches are required to block reverse voltage. One solution might be to introduce, with added expense and reduced efficiency, series blocking diodes in the drain leads [24]. These diodes, however, will prevent the drain-to-source FET capacitance from discharging, and the FETs will be gated on while still supporting a large forward voltage, with the attendant large switching losses.

A better solution is to permit the body diode to conduct. The resulting circuit, shown in figure 4.4, incorporates the equivalent MOSFET circuit of figure 3.6 and models the ideal current sources as a voltage source with two large dc inductors.

The circuit of figure 4.4 was then modeled by Parity Simulation. Since the simulation does not permit nonlinear elements, the resonant capacitors were taken to be 111 pF. The on-state resistances are modeled by R_2 and R_3, whose values of 0.35 Ω were estimated from the data sheets. Simulated waveforms are shown in figures 4.5-4.7. The input voltage has been set to 21.5 V, since that voltage resulted in a current of 1 A through each source inductor, as in the numerical analysis. Note that the voltage across the load resistor, R_3, is not purely sinusoidal. This distortion could be reduced by raising the 12.5 MHz gating frequency closer to the 21 MHz resonant frequency.

The distortion is not significant, since the output current will be rectified, as shown in figure 4.8. The simulated waveforms for this cir-

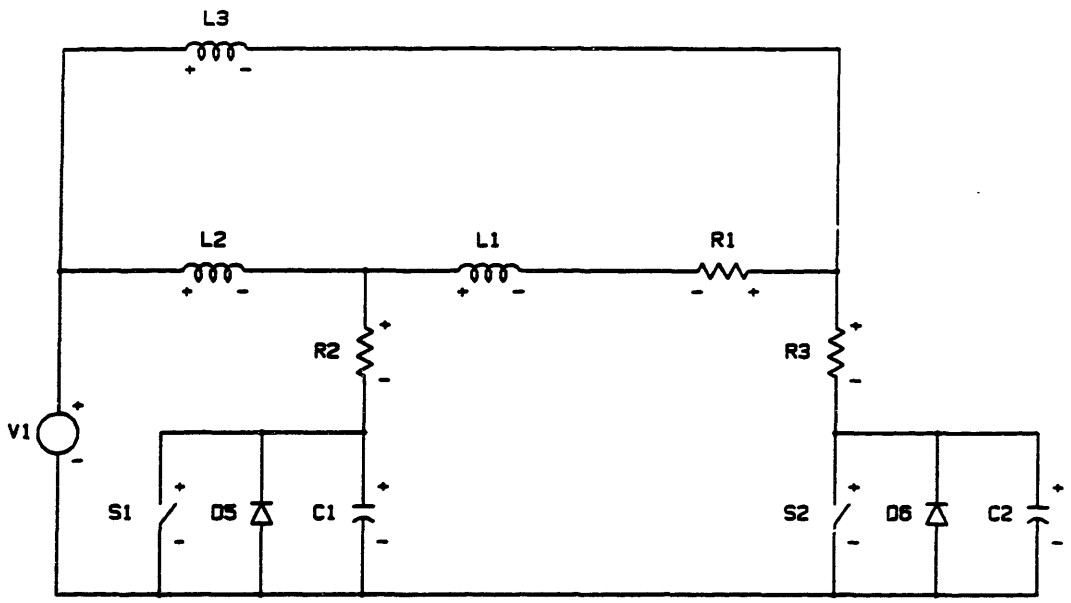
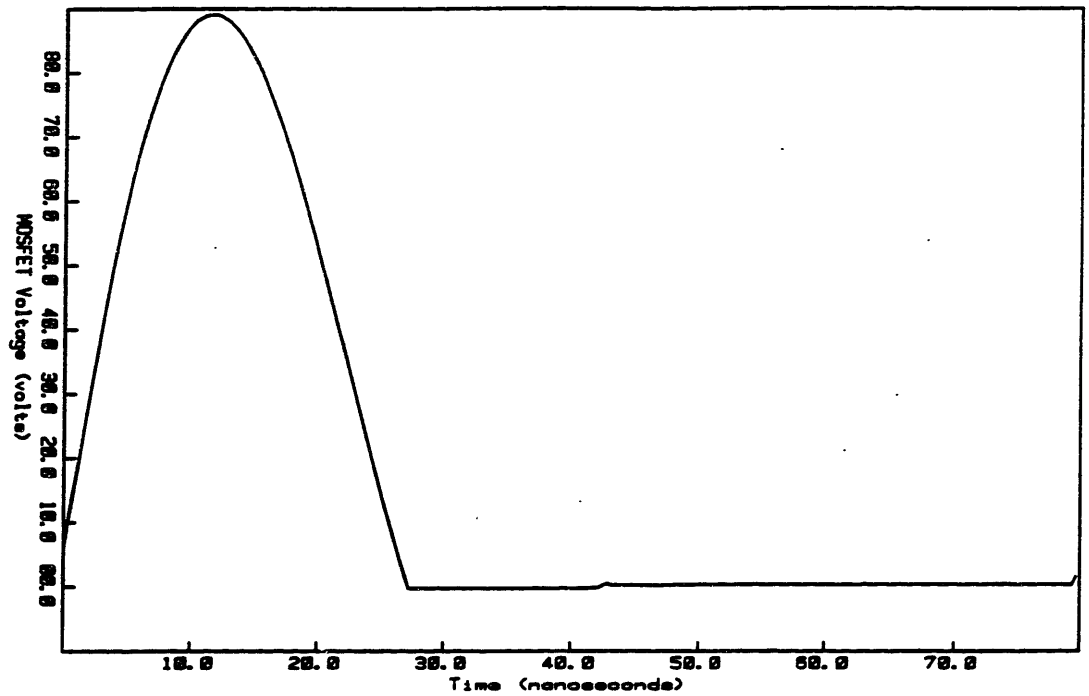


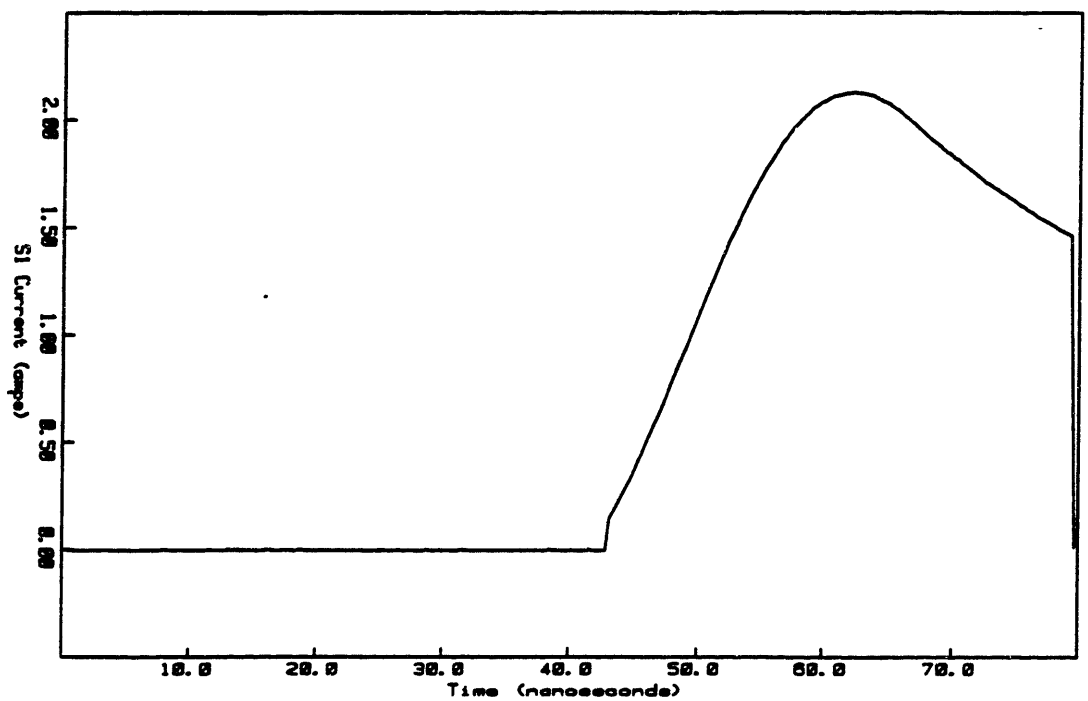
Figure 4.4: Parity Simulation Model of Current Mode Inverter

L1 = 0.5 μH
L2 = L3 = 120 μH
C1 = C2 = 111 pF
R1 = 20 Ω
R2 = R3 = 0.35 Ω



Maximum 80.0 volts
Minimum -293 millivolts
Average 19.1 volts
RMS 36.3 volts

Figure 4.5: Simulated Switch Voltage at 12.5 MHz (v_{in} = 21.5 V)



Maximum 2.13 amps
Minimum -4.09 milliamps
Average 708 milliamps
RMS 1.11 amps

Figure 4.6: Simulated Switch Current at 12.5 MHz (v_{in} = 21.5 V)

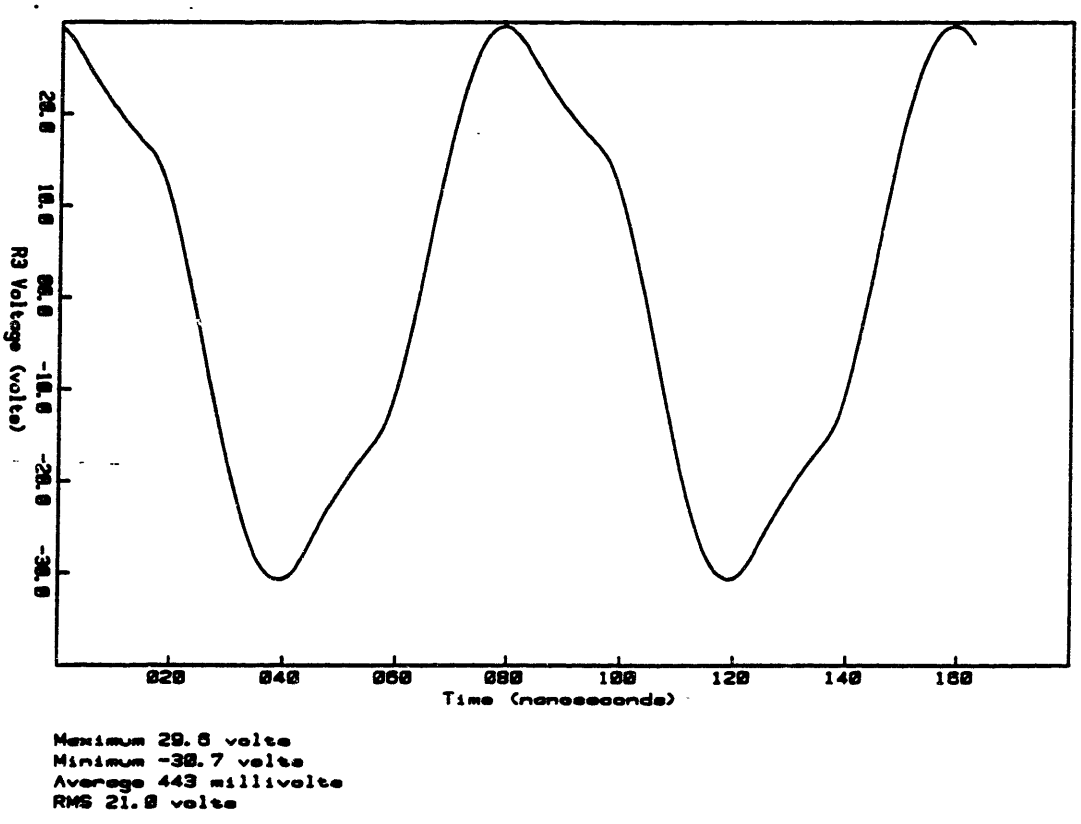


Figure 4.7: Simulated Output Voltage at 12.5 MHz (v_{in} = 21.5 V)

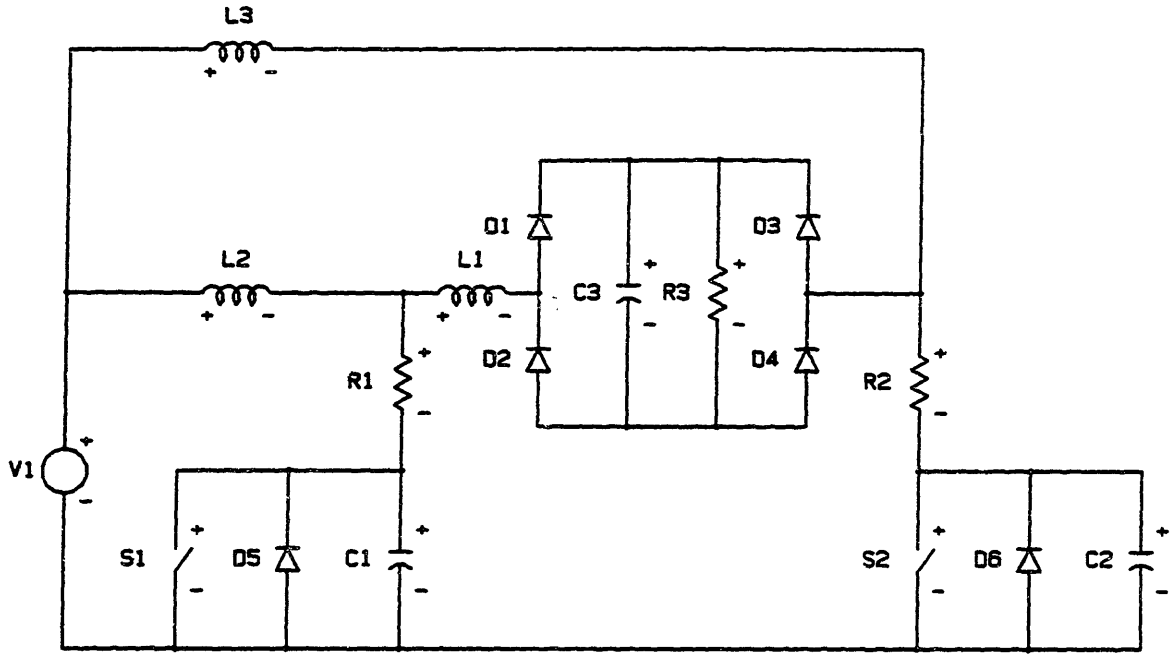


Figure 4.8: Parity Simulation Model of Dc-to-Dc Converter

L1 = 0.5 μH
L2 = L3 = 120 μH
C1 = C2 = 111 pF
C3 = 10 μF
R1 = R2 = 0.35 Ω
R3 = 20 Ω

cuit were not significantly different from those of figures 4.5-4.7.

In practice, the antiparallel body-drain diode is not the ideal diode of the simulation. But since the diode turns on as the charge store in its depletion capacitance has rung to zero, and then turns off through voltage commutation as the MOSFET turns on, its switching speed need not be extremely fast. So although the parasitic diode is typically slow compared to the maximum switching frequency of the actual MOSFET, it does not prevent the proper operation of the circuit.

4.4: Use of Schottky Diodes

At radio frequencies the forward and reverse recovery transients of pn junction diodes degrade the operation of a full wave bridge. Schottky diodes, therefore, were employed. Their limited voltage blocking ability, however, limits the output voltage of the converter. In addition, the diodes have an associated depletion capacitance that is not negligible; at the metal-semiconductor interface a depletion region that is similar to the depletion region of a one-sided pn junction extends into the semiconductor. This nonlinear capacitance can also be modeled by equation 3.9 [25].

The effect of this depletion capacitance can be determined by analysing figure 4.9, which shows the full wave bridge driven by a sinusoidal current source. Each of the Schottky diodes are assumed to be ideal and identical. When a diode is reverse biased, it is replaced by a depletion capacitance C_j, which is approximated as linear. The filter capacitor C1 holds the output constant at V_{dc}.

This situation is analogous to the more familiar voltage driven full wave bridge with commutating series inductance, and may be analysed similarly. When the current is positive, diodes D_1 and D_4 are conducting and the depletion capacitances of D_2 and D_3 are charged to the output voltage.

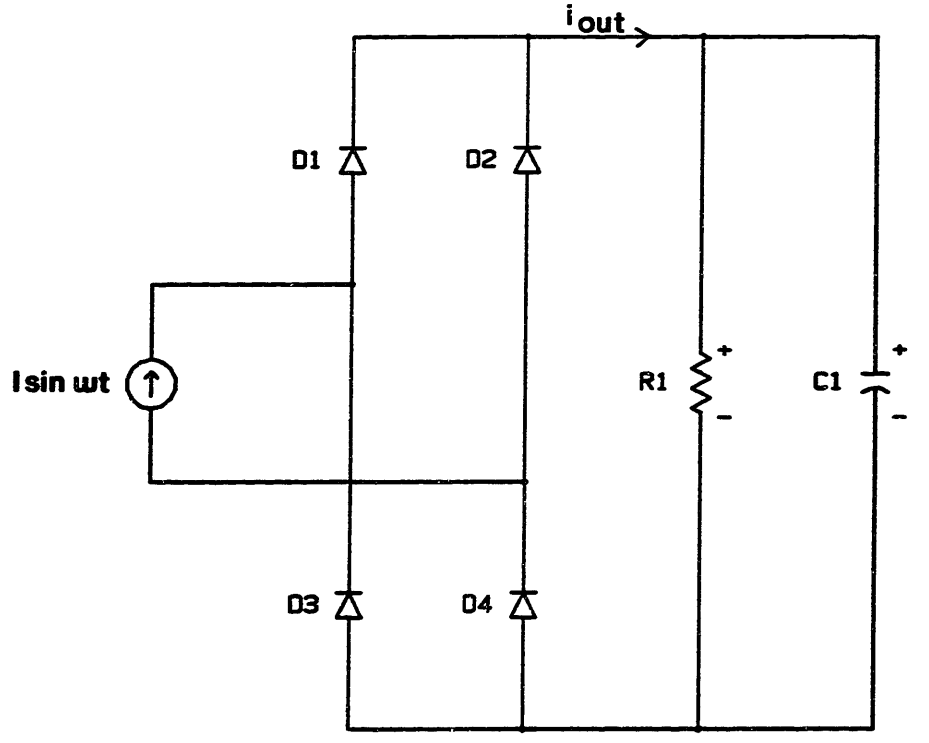


Figure 4.9: Full Wave Diode Bridge

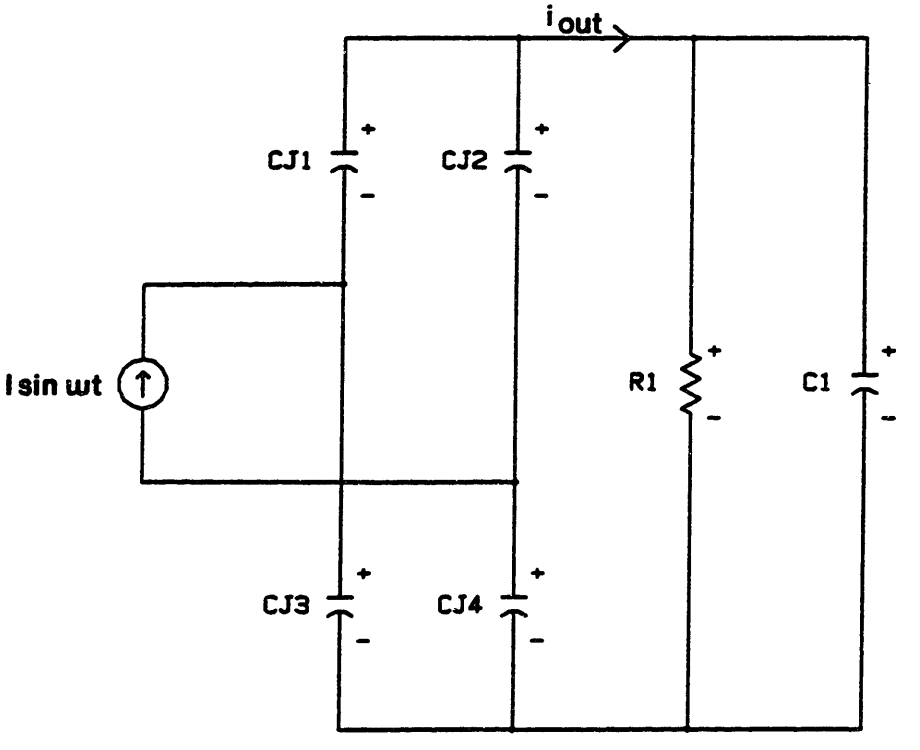


Figure 4.10: Diode Bridge Equivalent Circuit

When the current reverses direction, D_1 and D_4 turn off. D_2 and D_3, however, can not turn on until their depletion capacitances have discharged. This intermediate situation, where all four diodes are off, is modeled by the equivalent circuit of figure 4.10. The voltage v_1 across capacitor CJ1 is given by

$$v_1 = \frac{I_o}{2C_j} \int_o^t \sin \omega t' \, dt' \tag{4.10}$$

whose solution is

$$v_1 = \frac{I_o}{2\omega C_j} [1 - \cos \omega t] \tag{4.11}$$

the diodes D_2 and D_3 turn on when v_1 is charged to the output voltage V_{DC}. This occurs at a time t_o such that

$$\cos \omega t_o = 1 - \frac{2\omega C_j V_{DC}}{I_o} \tag{4.12}$$

The output current i_{out} is sketched in figure 4.11, and its average value $\langle i_{out} \rangle$ may be calculated as

$$\langle i_{out} \rangle = \frac{I_o}{\pi} \int_{\omega t}^{\pi} \sin \varphi d\varphi = \frac{I_o}{\pi} [1 + \cos \omega t_o] \tag{4.13}$$

Combining equations 4.12 and 4.13(b) and using the fact that

$$v_{DC} = R \langle i_{out} \rangle \tag{4.14}$$

gives an expression for the output voltage in terms of circuit parameters

$$v_{DC} = \frac{2RI_o}{\pi} [1 + \frac{2R}{\pi} \omega C_j] \tag{4.15}$$

The effect of the depletion capacitance, therefore, is to reduce the output voltage by the factor in square brackets. For a depletion capacitance of 200 pF, typical for the Schottky diodes used in this circuit, a load resistor of 20 Ω, and a frequency of 10 MHz, the depletion capacitance

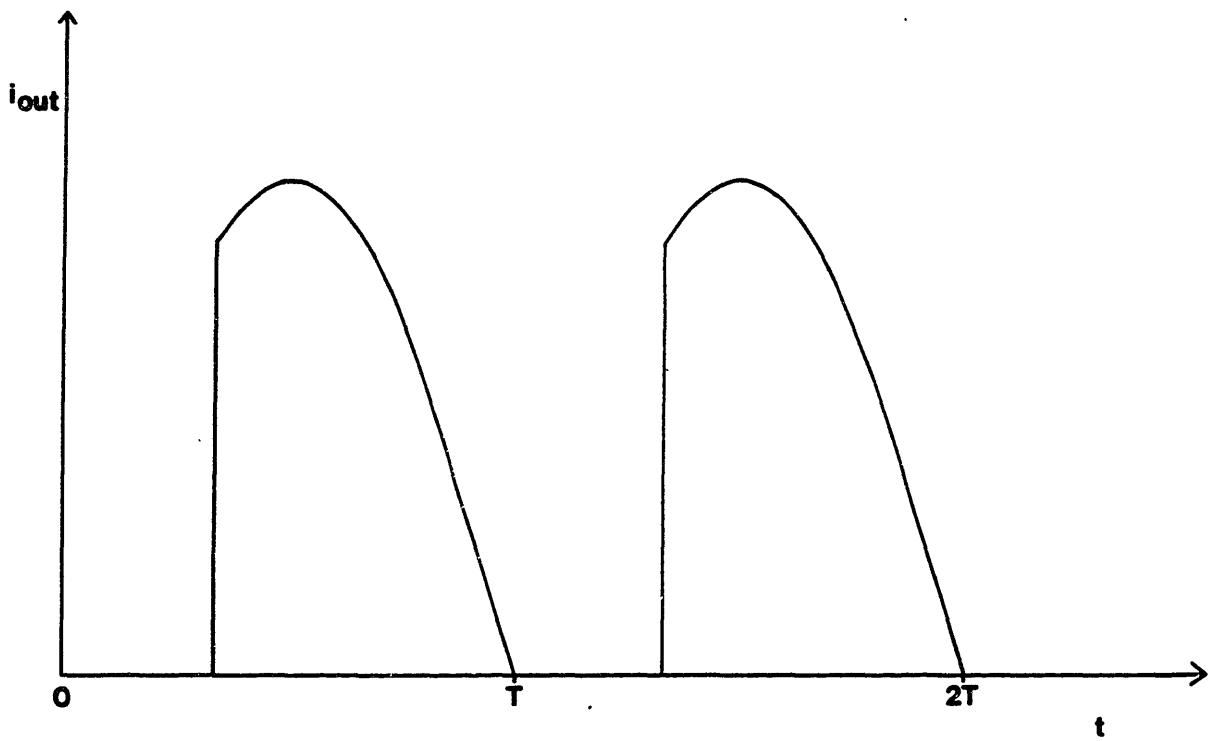


Figure 4.11: Rectifier Output Current

reduces the output voltage by 14%.

4.5: Projected Power Output

Since Parity Simulation does not model switching losses or the non-linear capacitances of the FETs and diodes, the simulated output voltage of the dc-to-dc converter is approximate. The simulation suggested that the maximum output power level would be in the vicinity of 50 W.

Chapter Five: Gate Drive Design

5.1: Overview

The gate drive requirements of the MOSFET switches are analysed, and the gate drive circuit is developed.

5.2: Gate Drive Requirements

The switching speed of the MOSFETs is determined primarily by the ability of the gate drive to charge and discharge the gate-to-source capacitances, thereby creating and destroying the inversion layers necessary for conduction. Once the channel is strongly inverted, the dominant resistance is in the epilayer and conduction losses can not be reduced appreciably by further increases in the gate-to-source voltage.

In this particular power circuit, v_{DS} is near zero at turn-on, as shown in figure 2.5. Most of the switching losses take place at turn-off, since the current is interrupted as v_{DS} begins rising sinusoidally. As described in chapter two, if the circuit is gated at too fast or too slow a frequency, v_{DS} will be non-zero at turn-on and switching losses will be large there also.

Ideally, therefore, the gate drive should be capable of sourcing and sinking large capacitive currents, so that the FET can traverse the high channel resistance domain as quickly as possible. If the input capacitance and the current drive are approximated as constant, and the gate resistance neglected, the current required to switch a FET within a time interval Δt is

$$i = \frac{C_{gs} (v_S - v_T)}{\Delta t} \qquad (5.1)$$

where v_T is the gate-to-source voltage at the onset of inversion, and v_S is the gate-to-source voltage at strong inversion. According to the data

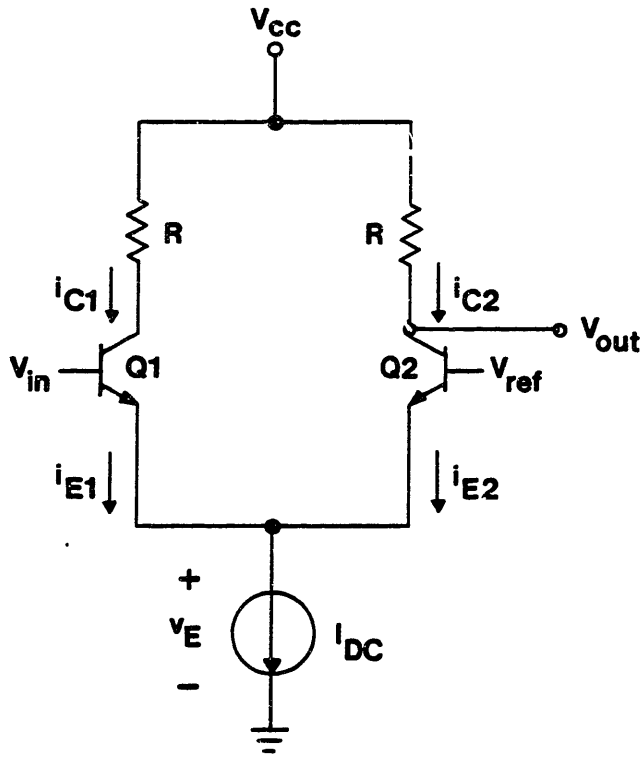


Figure 5.1: Canonical Emitter Coupled Pair

sheets for the MTP8N10, the input capacitance is approximately 400 pF, v_S is about 8 V, and v_T is about 2 V. In order to switch the FET within 10 nsec, the device must source and sink at least 240 mA.

This calculation underestimates the current required, since it ignores the Miller effect, described in chapter three, that increases the effective input capacitance. In this circuit, the Miller effect at turn-on is negligible, as v_{DS} is clamped at zero.

The minimum energy that must be stored each cycle in the input capacitance is approximately

$$W = \tfrac{1}{2} C_{gs} (v_S - v_T)^2 \qquad (5.2)$$

Assuming that the gate drive circuit does not recover any of the energy stored in the input capacitance, and that an equivalent amount of energy is expended in any series resistance between driver and gate, the average power dissipated is then

$$P_d = (2) (\tfrac{1}{2}) C_{gs} (v_S - v_T)^2 f \qquad (5.3)$$

where f is the driving frequency. Switching the MTP8N10 at 10 MHz, therefore, requires at least 0.14 W per transistor.

5.3: Emitter Coupled Pairs

The gate drive controller was implemented with emitter coupled logic (ECL). For proper operation of the power circuit, the two 10 MHz gate drive signals must be 180° out of phase. ECL, with its short gate delays and fast switching speeds, was the obvious choice of logic family.

But ECL dissipates more power than any other logic family. This may be understood by considering the canonical emitter-coupled pair, shown in figure 5.1. From the Ebers-Moll equations for bipolar transistors [26] in the forward active region, one can write

$$i_{E1} = I_{ES1}\,[e^{q(v_{IN} - V_E)/kT} - 1] \qquad (5.4\ a)$$

$$i_{E2} = I_{ES2}\,[e^{q(v_{REF} - V_E)/kT} - 1] \qquad (5.4\ b)$$

where I_{ES} is the reverse saturation current of the emitter-base junction. By Kirchoff's Current Law,

$$i_{E1} + i_{E2} = I_{DC} \qquad (5.5)$$

Assuming for each transistor that $i_E >> I_{ES}$, one can solve equations 5.4(a,b) and 5.5 for the emitter currents

$$i_{E1} = I_{DC}\,[e^{q(v_{REF} - V_{IN})/kT} - 1]^{-1} \qquad (5.6\ a)$$

$$i_{E2} = I_{DC}\,[e^{-q(v_{REF} - V_{IN})/kT} - 1]^{-1} \qquad (5.6\ b)$$

These expressions can be recast as

$$i_{E1} = \frac{I_{DC}}{2}\left[\,1 - \tanh\frac{v_{REF} - v_{IN}}{2kT/q}\,\right] \qquad (5.7\ a)$$

$$i_{E2} = \frac{I_{DC}}{2}\left[\,1 + \tanh\frac{v_{REF} - v_{IN}}{2kT/q}\,\right] \qquad (5.7\ b)$$

From equations 5.7(a,b) and the identity

$$\tanh^{-1} r = \frac{1}{2}\ln\frac{1 + r}{1 + r} \qquad (5.8)$$

one can compute that at 25°C, 99% of the current is switched from one transistor to the other when the difference between the input and reference voltages is only 0.12 V. Since the total current I_{DC} is not varied, but merely steered through one transistor of the pair by very small changes in voltage, the output voltage can change state extremely rapidly. Also, in any ECL circuit both the output and its complement are immediately available, eliminating inverter gate delays.

Power dissipation in ECL circuits is high, therefore, because one

transistor of each pair is always on. In addition, high speed switching transistors are heavily gold doped [27] in order to create many recombination-generation centers. This drastically reduces minority carrier lifetime and switching time, but at the cost of drastically reducing the current gain. The resulting large base currents further increase the power requirements.

ECL can not drive power FETs directly. An output stage is required to amplify the small ECL voltage signal, and to source and sink the large charging currents. A conventional approach, such as the circuit shown in figure 5.2, would also employ emitter-coupled pairs. When the logic signal goes high, the current in Q_3 switches to Q_4. Transistor Q_2 is turned off, so all of Q_4's collector current charges the FET input capacitance. At turn-off the logic signal falls and the current in Q_1 switches to Q_2. Now Q_4 is turned off and the collector current of Q_2 is provided by the discharge of the FET input capacitance. The diodes around the collector-base junctions of Q_2 and Q_4 ensure that those transistors do not saturate, and diodes set the reference voltages at the bases.

This output stage consumes too much power. If the charging currents are 0.5 A, each output stage must dissipate at least 15 W. This estimate ignores the substantial base currents and the power consumed by the emitter follower Q_5. The power circuit employs two FETs, so the two drives would consume at least 30 W. This is, according to the design analysis of chapter four, comparable to the maximum output power of the converter.

Building low power, high speed gate drives using conventional topologies with discrete components may well be impractical. One promising proposal, however, would take advantage of the fact that unlike the base drive of a bipolar transistor, which must feed recombination and reverse

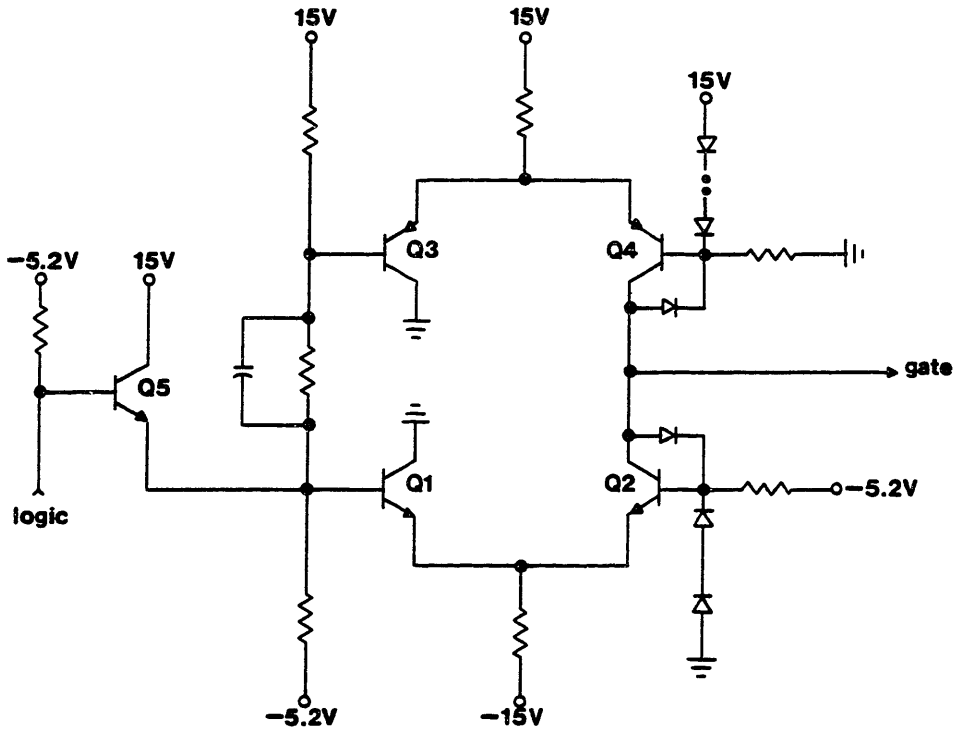


Figure 5.2: Representative ECL Gate Drive

injection, the gate drive of a FET need only store energy in the input capacitance. A gate drive might incorporate the FET input capacitance as part of a resonant tank, and thereby recover most of the energy at the end of each cycle [28].

5.4: Gate Drive Implementation

The gate drive output stage employed in this design was an integrated circuit MOS clock driver, the National Semiconductor DS0026. The data sheets appear in the appendix. This chip, designed for capacitive loads, is capable of delivering up to 1.5 A peak current and can charge and discharge the MTP8N10 input capacitance in less than 10 nsec, while dissipating about 3.5 W. The actual gate drive behavior is documented in chapter seven.

The gate drive logic, in order to facilitate both experimentation and possible future closed loop control, permits voltage control of both period and on-time. The block diagram is shown in figure 5.3. An input voltage sets the frequency of a voltage controlled oscillator (VCO), which sends a square wave of frequency f_o to the monostable multivibrator. The monostable triggers on both rising and falling edges of the square wave and produces a stream of pulses of frequency $2f_o$. The width of the pulses is set by a second control voltage. These pulses are gated with the VCO output to produce two signals, 180° apart, of frequency f_o.

Figure 5.4 shows the actual schematic. The circuit was implemented using the Motorola MECL 10K series. The frequency of the VCO is set by varying the reverse bias of the MV1401 varactor, which serves as the capacitance of a resonant tank. The pulse width is controlled by varying the charging current of the 10 pF capacitor in the timing circuit of the monostable.

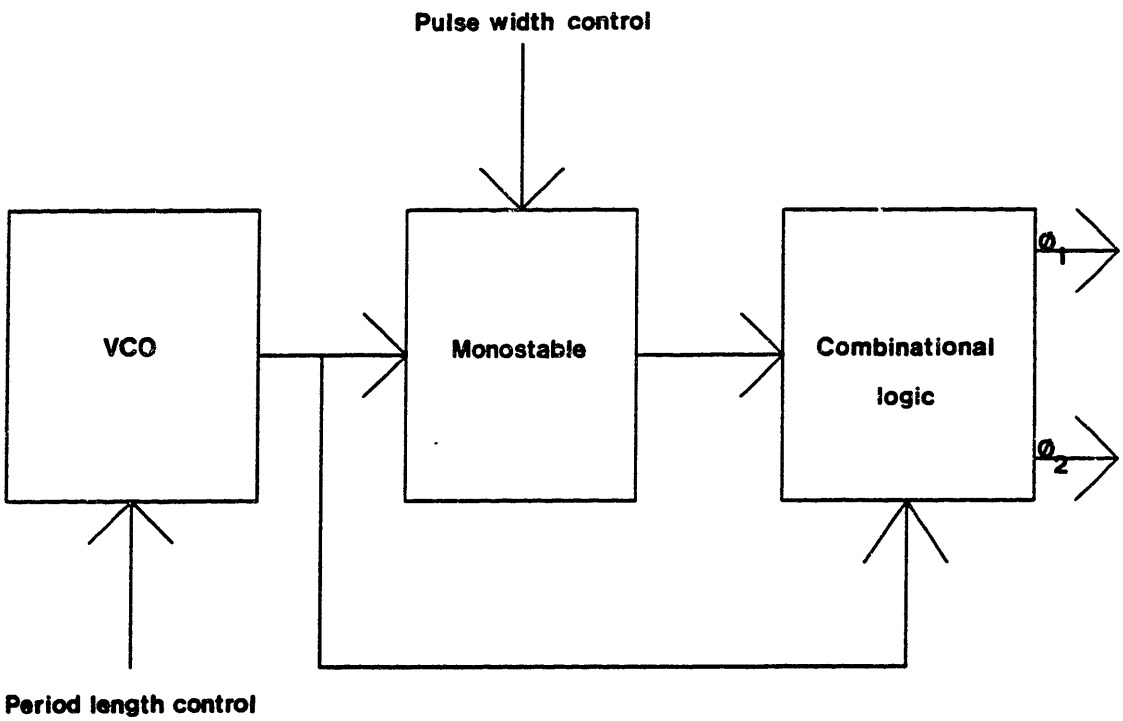


Figure 5.3: Gate Drive Block Diagram

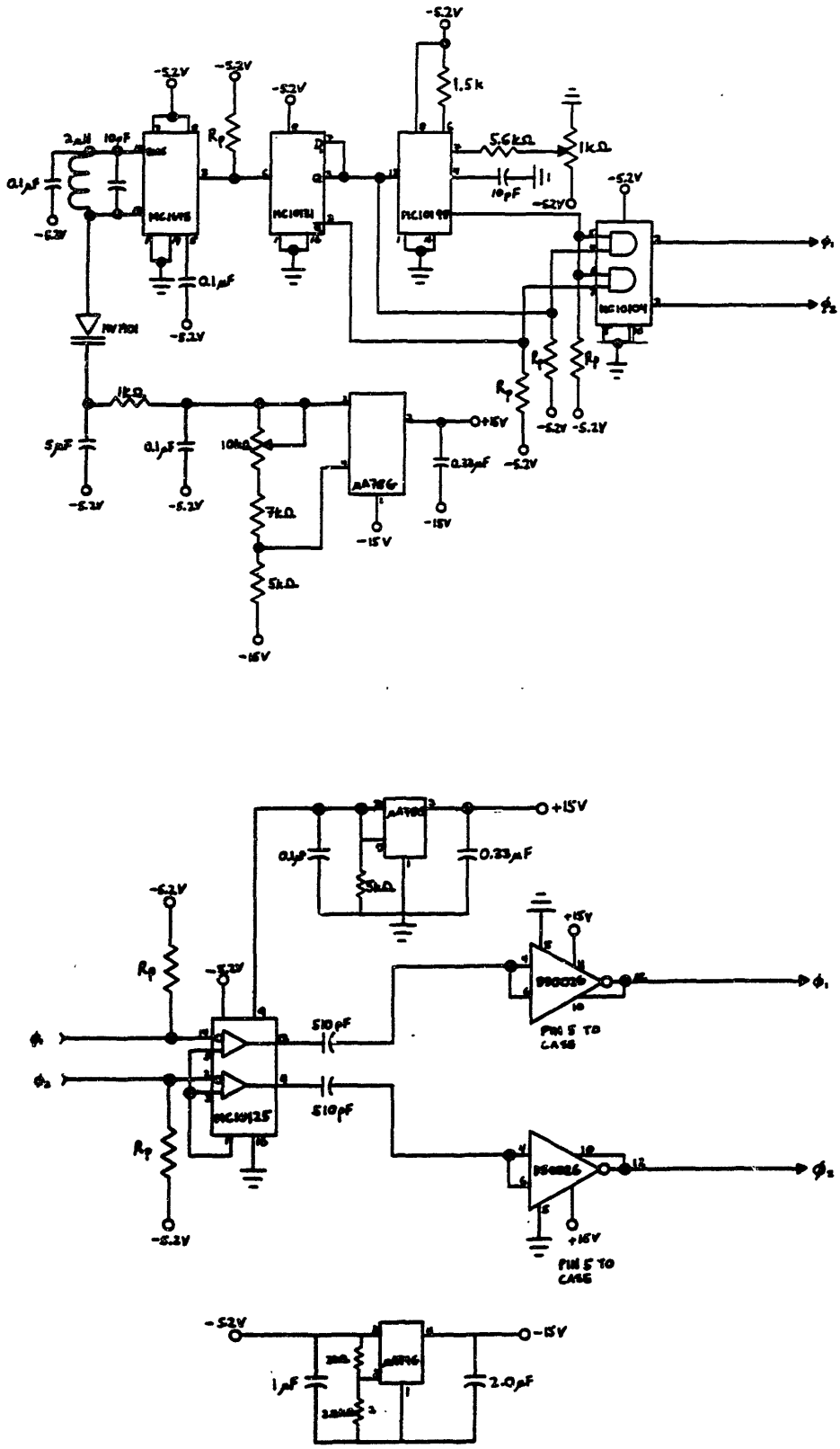


Figure 5.4: Gate Drive Schematic
(R_p = 270 Ω, each chip has 0.1 μF to ground)

In this design, the gate drive switches between 0 and 15 V. Although strong inversion takes place at 8 V, the additional voltage swing was necessary to reduce the 2 to 8 V switching time. The minimum power that must be dissipated in each gate drive is, according to equation 5.3, 0.9 W at 10 MHz. The actual power dissipated in the gate drive was a function of MOSFET input capacitance and driving frequency, and will be discussed in chapter seven.

The voltage regulators on the logic supplies permit the maximum gate voltage to be controlled by simply adjusting the positive voltage supply to the gate drive circuit.

5.5: Summary

The gate drivers were integrated circuits MOS clock drivers. The control signal was generated by ECL, and two control voltages permitted variation of period and pulse width. Photographs of the actual output are shown in chapter seven, as well as an analysis of the power dissipation.

Chapter Six: Printed Circuit Board Design

6.1: Overview

The experimental circuit is laid out on a printed circuit board. Parasitic elements are modeled, adequate heat sinking is provided, and the energy storage elements are designed.

6.2: Modelling the Printed Circuit Board

The experimental circuit was constructed on a 7" by 10" double-sided printed circuit board. The component side was used as a ground plane, since ground plane construction permits the quantification and control of parasitic inductances and capacitances. This, for the copper traces, could have been achieved simply by routing return traces on the other side of the board, but the presence of such large, metallic objects as heat sinks and chip packages necessitated a full ground plane.

The traces were modeled with lumped parameter elements as shown in figure 6.1. This analysis treats the printed circuit board as a quasi-static system, since the physical dimensions are much smaller than the 30 m wavelength at 10 MHz. This model neglects the shunt conductance, since the glass epoxy board is an excellent insulator. Its dielectric constant is about $5\varepsilon_0$ and its conductivity σ is on the order of $10^{-10}\ \Omega^{-1}m^{-1}$ [29]. The loss tangent for the board material,

$$LT = \frac{\sigma}{\omega\ \varepsilon} \tag{6.1}$$

is on the order of 10^{-8} at 10 MHz, indicating that the shunt conductance is indeed negligible.

In order to calculate the trace resistance, one must first calculate the skin depth at the fundamental driving frequency of 10 MHz. The skin depth is [30]

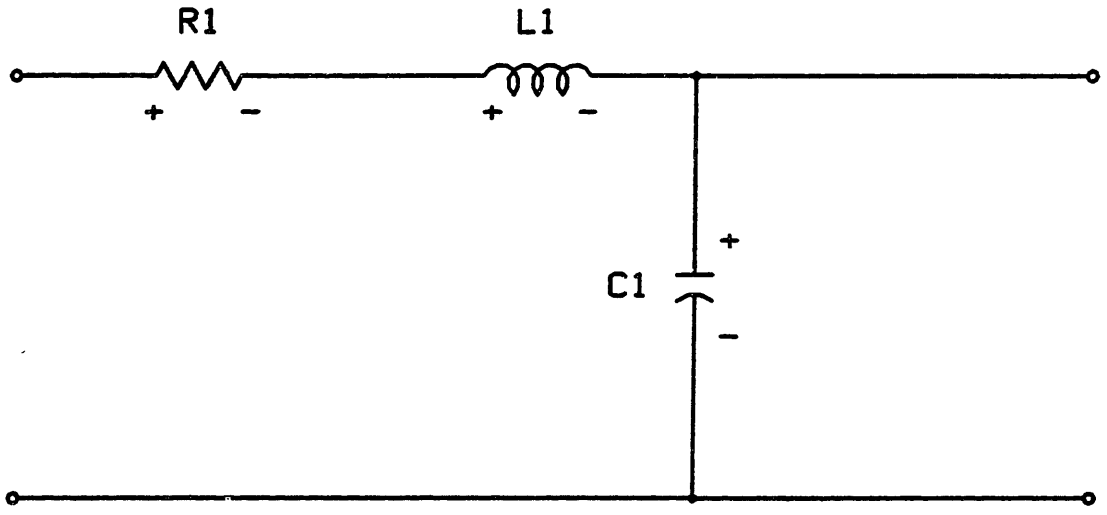


Figure 6.1: Lumped Parameter Model of Printed Circuit Trace

$$\delta = \sqrt{\frac{2}{\omega\mu_o\sigma}} \tag{6.2}$$

where μ_o is the magnetic permeability of the glass epoxy, essentially that of free space, $4\pi \times 10^{-7}$ H/m, and σ is the conductivity of the copper, which is approximately 5.8×10^7 mho/m [31]. The skin depth may therefore be evaluated as 20.9 μm. The resistance per inch may then be approximated as

$$R = \frac{2}{\sigma w \delta} \tag{6.3}$$

where w is the width of the trace. The factor of two takes into account the return current in the ground plane. For a trace width of 0.2", which was used for the power traces, the resistance is 8.2 mΩ/inch, which is small enough to neglect.

The actual resistance is smaller, for two reasons. First, this analysis assumes that the current flows inside one skin depth. The 2 oz copper board is 68.6 μm thick [32], about three skin depths, so that only about (100/e)% of the current is contained in one skin depth. Second, it ignores the spreading of the current in the ground plane.

The inductance of the trace above the ground plane can be computed by the method of images. The boundary condition at the surface of the ground plane, which for a perfect conductor would be the cancellation of the normal H-field, can be satisfied by replacing the ground plane with another trace. This ficticious trace lies the same distance below the ground plane as the real trace is above, and contains a current flowing in the opposite direction. This situation can be considered as a one turn inductor closed at infinity, and its inductance per inch, assuming that the width and length of the trace are large compared to the thickness of the

glass epoxy, is

$$L = \frac{\mu_o 2d}{w} \tag{6.4}$$

where d, the board thickness, is 0.0625". For the trace width of 0.2", the inductance is 20.0 nH/inch, which suggests that trace lengths be kept as short as possible.

Finally, the capacitance of the trace can be computed by considering the trace and its image in the ground plane as a parallel plate capacitor, with the printed circuit board glass epoxy material as the dielectric. The resulting expression is

$$C = \frac{5\varepsilon_o w}{2d} \tag{6.5}$$

This is about 1.8 pF/inch. This again suggests that lead lengths should be kept as short as possible.

In chapter seven the lead inductance will be found to be the dominant parasitic effect. This result will be confirmed by both experiment and Parity Simulation.

6.3: Heat Sinking

Four devices, the two power FETs and their two DS0026 drivers, required heat sinking. This design provided for adequate cooling through natural convection. The resultant large heat sinks necessitated a much larger printed circuit board than would have been required had cooling fans been used. The heat sinks also had to be separated far enough from each other to prevent electrostatic coupling.

The steady state equivalent heat dissipation circuit shown in figure 6.2 obeys an analogue to Ohm's Law,

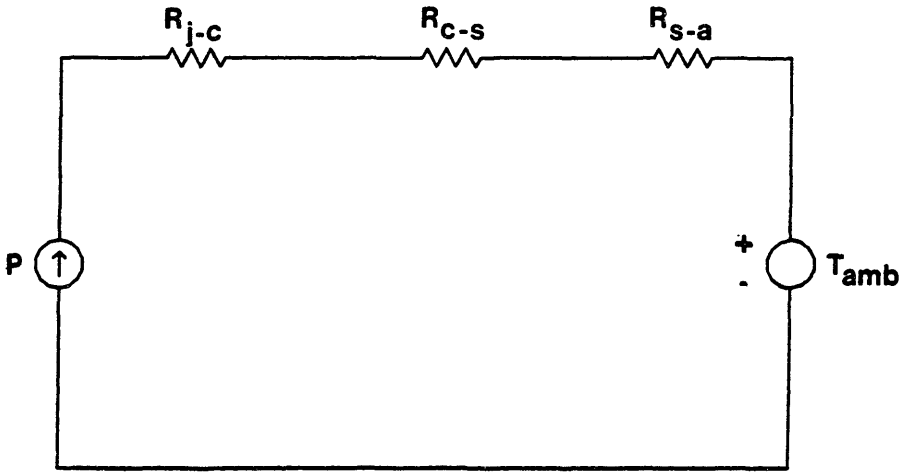


Figure 6.2: Power Dissipation Circuit Analog

$$T = P\,R \tag{6.6}$$

The R_{j-c} of figure 6.2 is the thermal resistance between junction and case, R_{c-s} the resistance between case and heat sink, and R_{s-a} the resistance between the sink and the surrounding air. T_{amb} is the ambient temperature, T_j the junction temperature, and P the average power dissipated in the device.

The maximum rms current that the FETs would handle was estimated as 3 A, and the maximum T_j desired was 100°C. The maximum on-state resistance for the MTP8N10 is 0.5 Ω, resulting in a maximum on-state loss of 4.5 W. The heat sink employed for this TO-220 package was the IERC HP-1, which has an R_{s-a} of 7.5 °C/W. The R_{j-c} was 1.67 °C/W and the R_{c-s} about 1.0 °C/W, for a maximum case temperature, with the ambient temperature at 25°C, of about 65°C and a maximum T_j of about 70°C. Each FET could dissipate an additional 3 W in switching losses before T_j would rise above 100°C.

A similar analysis for the drivers, which are packaged in TO-8 metal cans with a R_{j-s} of 15.3 °C/W and a maximum power dissipation of about 3 W each resulted in the selection of the IERC UP-TO8, which has an R_{s-a} of 11.8 °C/W.

The manufacturer ties the metal tab of the FET's TO-220 case to the drain. In order to avoid large capacitance between the case and the heat sink, the heat sink was electrically tied to the case. In order to reduce the resulting capacitance between the heat sink and the ground plane, the heat sink was raised on insulating spacers. The capacitance, of the form of equation 6.5, was calculated as less than 5 pF. If a linear resonant capacitor were required in the power circuit, control of the distance between the heat sink and the ground plane would be one inexpensive way to realize it.

Capacitance from one FET heat sink to the other would disrupt circuit operation; the 1" separation reduces this capacitance to less than 1 pF.

The driver cans, which are normally electrically isolated, were grounded and placed in electrical contact with their heat sinks. The heat sinks were separated from the FET heat sinks by at least 0.5" in order to reduce the inter-sink capacitance to at most 1 pF.

6.4 Energy Storage Elements

The three inductors were made using Ferroxcube ferrite pot cores in order to prevent the magnetic fields from coupling to the rest of the circuit. The tank inductor of 0.5 μH was made with 3.5 turns in an 1811PA40-4C4 pot core, and has a Q of 215 at 10 MHz, as computed from the data sheets in the appendix. This Q, which in the neighborhood of 10 MHz has the form

$$Q = \frac{\omega L}{R} \tag{6.7}$$

corresponds to a frequency dependent equivalent series resistance of

$$R = \frac{\omega L}{Q} = (14.6 \times 10^{-9})\ f \tag{6.8}$$

This high Q is achieved, as shown below, by keeping the magnetic flux density in the core extremely low. Assuming that the current flows uniformly to one skin depth in the #18 magnet wire, and that the mean length of turn is 3.7 cm, the wire resistance is about 34 mΩ. The total power dissipated in the inductor, therefore, is

$$P_d = (I_{rms})^2\ [33.9 \times 10^{-3} + (14.6 \times 10^{-9})\ f] \tag{6.9}$$

where P_d, the dissipated power, is in watts, I_{rms}, the rms current, is in amperes, and f, the fundamental frequency, in Hz.

The magnetic field in the core can be estimated from two of Maxwell's equations,

$$\oint H \cdot dl = \int J \cdot d\bar{a} \quad ; \quad \oint B \cdot d\bar{a} = 0 \qquad (6.10\ a,b)$$

Assuming that the fields in the core are constant in space, one can apply these equations to the magnetic circuit, and get

$$H_g l_g + H_m (l_m - l_g) = Ni \quad ; \quad \mu_m H_m = \mu_o H_g \qquad (6.11\ a,b)$$

where H_g and H_m are the components of the magnetic fields in the gap and the ferrite, l_g is the gap length, l_m the mean magnetic path length, and μ_m and μ_o are the magnetic permeabilities in the ferrite and in the gap. Together with the constitutive relation

$$B_g = \mu_o H_g \qquad (6.12)$$

these equations can be solved for the magnetic flux density B_g as

$$B_g = \mu_o Ni \left[l_g + (\mu_o/\mu_m)(l_m - l_g) \right]^{-1} \qquad (6.13)$$

Using the values from the data sheet in the appendix, and assuming a peak inductor current of 4 A, B_g can be estimated as

$$B_g = \frac{(4\pi \times 10^{-7}\ H/m)(3.5\ turns)(4.0\ A)(10^4\ Gauss/T)}{[0.08" + 0.008(1.02" - 0.08")](0.0254\ m/")} = 80\ Gauss$$

which, as seen from figure 6.3, is far from saturating the core.

The two 120 μH dc inductors were each constructed with twenty turns of #20 wire on 2616PL00-4C4 ungapped cores. Using a similar analysis to the tank inductor, the magnetic field in the core material can be calculated as

$$B_m = \frac{\mu_m Ni}{l_m} \qquad (6.14)$$

which for this core, assuming a dc current of 2 A, is

$$B_m = \frac{(4\pi \times 10^{-7}\ H/m)(20\ turns)(2.0\ A)(10^4\ Gauss/T)}{.0376\ m} = 1600\ Gauss$$

which makes good use of the core. Any resistance will be due to copper

losses in the magnet wire and is approximately

$$R_w = \frac{l_t}{\pi r^2 \sigma} N \tag{6.15}$$

where l_t is the mean length of turn and r the radius of the wire. For the 2616 core, l_t is 5.3 cm and for #20 wire, r is 406.4 μm. The resistance of each core is therefore 35 mΩ, and is negligible.

Finally, the 8.8 μF output capacitor is composed of four 50 V Centralab Mono-Kap ceramic capacitors CY30C225Z. These capacitors were selected for their high capacitance and miniature size, as well as their wide frequency range and low dissipation.

Chapter Seven: Experimental Circuit Analysis

7.1: Overview

The experimental circuit was constructed with the components shown in figure 7.1. Several modifications of this original design were required. The final circuit configuration was modeled by Parity Simulation in order to assist analysis of power dissipation. This simulation included the parasitic lead inductances present in the experimental circuit. The power dissipation analysis was confirmed by temperature measurements.

7.2: Gate Drive

In order to achieve the full range of output current regulation, the switches of the dc-to-dc converter must be gated at rates approaching the resonant frequency of the tank circuit. The resonant frequency of the original power circuit design of chapter four was 21 MHz. The actual gate drive circuit was not able to switch the MOSFETs quickly enough to permit efficient operation of the original power circuit design throughout the required frequency range.

Figure 7.2 shows the gate drive signal at 7.0 MHz with v_{DS} clamped at 0 V. The ringing of the waveform at switching transitions is caused by the interaction of the MOSFET input capacitance with the lead inductance of the printed circuit board trace connecting the output of the driver to the gate of the FET. The length of the trace between the driver output and the FET gate is about 4" and the trace width is 0.1". The lead inductance, by equation 6.4, is about 160 nH. This value of inductance, together with the FET input capacitance of 400 pF, corresponds to a period of 50 nsec, which is close to the 45 nsec ring period observed.

Ringing at turn off, however, can retrigger the MOSFET if the amplitude of the gate-to-source voltage exceeds the threshold voltage discussed

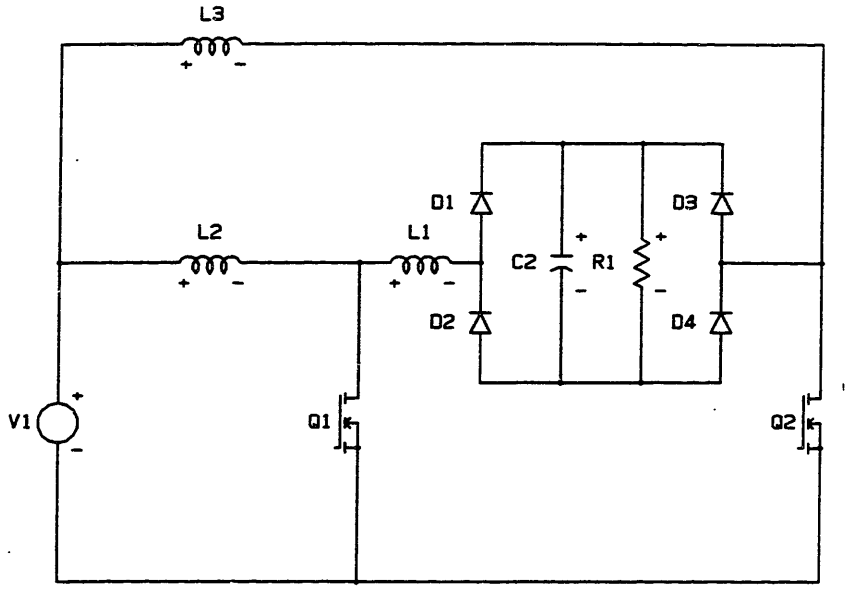


Figure 7.1: Experimental Circuit

L1 = 0.5 μH
L2 = L3 = 120 μH
C2 = 8.8 μF
R1 = 18.2 Ω
Q1 = Q2 = Motorola MTP8N10
D1 ... D4 = Motorola MBR340P

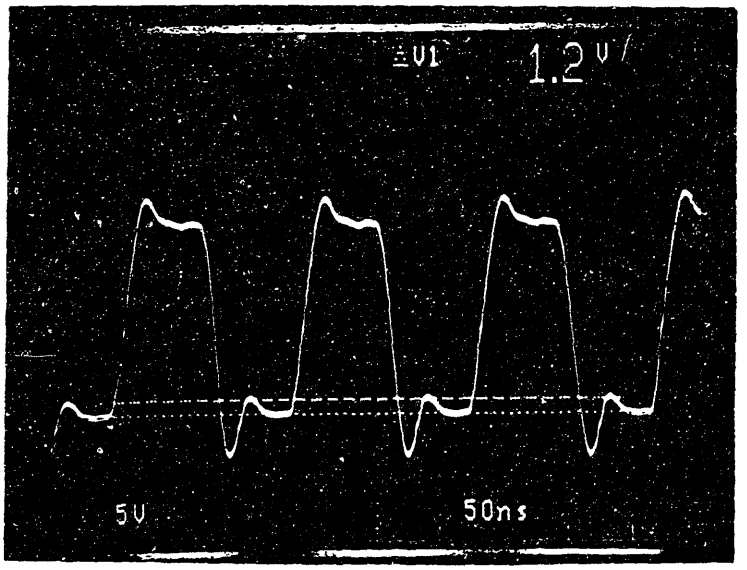


Figure 7.2: Gate Drive (v_{GS}) at 7.0 MHz
(v_{DS} = 0 V)
5 V/div, 50 nsec/div

(Bottom cursors indicate ground)

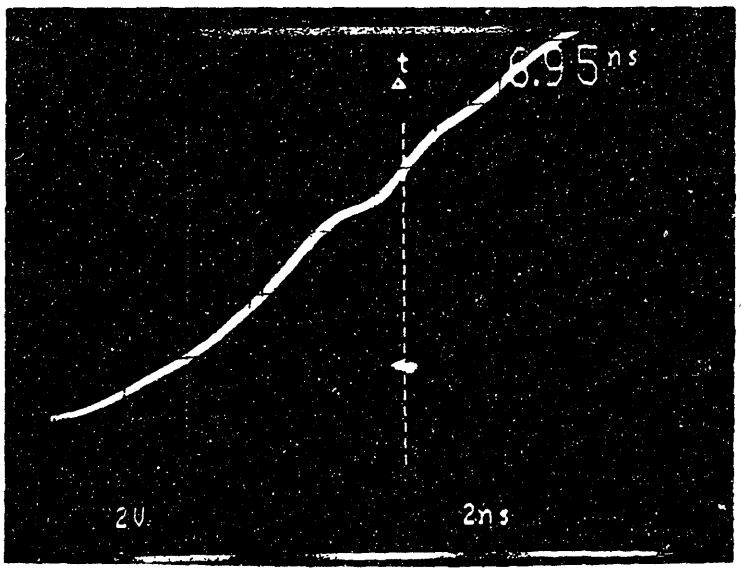


Figure 7.3: Gate Drive Turn-On (v_{GS})
(v_{DS} = 0 V)
2 V/div, 2 nsec/div

(Bottom cursors indicate ground)

in chapter three. In order to control the amplitude of this ringing, the trace is terminated with a 3.7 Ω resistor (not shown in figure 5.4).

As in chapter five, the rise and fall times of the gate drive waveform are defined as the intervals between weak and strong inversion of the MOSFET channel. For the MTP8N10 this is the time the gate-to-source voltage takes to switch between 2 V and 8 V. Figures 7.3 and 7.4 show that the rise and fall times, with v_{DS} clamped at zero, are 6.95 nsec and 7.05 nsec, respectively.

With increasing frequency the gate drive waveform loses the rectangular shape of figure 7.2. Figure 7.5 shows the gate drive signal at 12.0 MHz, again with v_{DS} clamped at zero. The waveform is beginning to look sinusoidal, because the gate drive is unable to deliver the current required to charge and discharge the MOSFET input capacitance fast enough to maintain the sharp gate-to-source voltage transitions. As the frequency is increased, and the sum of the switching times approaches the total desired conduction time, the MOSFET channel is not strongly inverted during a significant portion of the conduction time. This conduction through only moderately inverted channels results in high power losses and lowered efficiency.

The gate drive's limited ability to provide capacitive charging currents restricts the maximum frequency at which the circuit can operate efficiently. The power circuit was therefore modified so that the tank resonates at a lower frequency.

7.3: Modifying the Power Circuit

Although the modification of the resonant tank required the addition of circuit components, the modified design is capable of delivering more than twice the power of the original circuit.

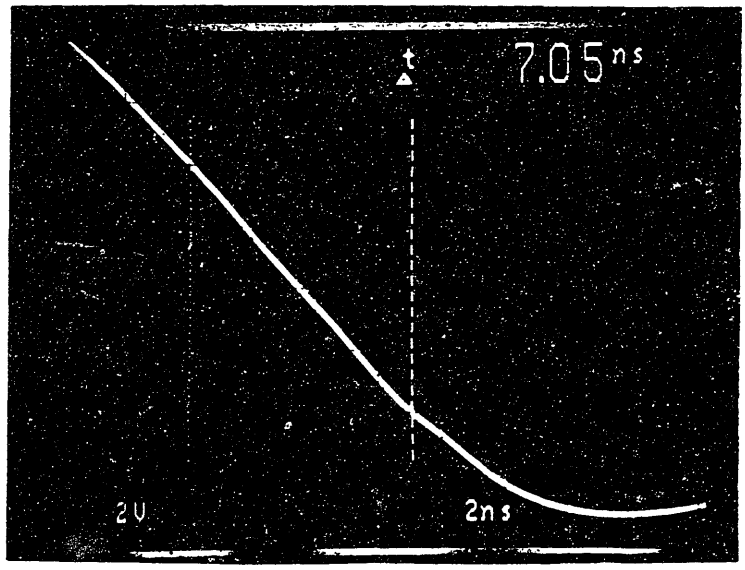


Figure 7.4: Gate Drive Turn-Off (v_{GS})
(v_{DS} = 0 V)
2 V/div, 2 nsec/div

(Bottom cursors indicate ground)

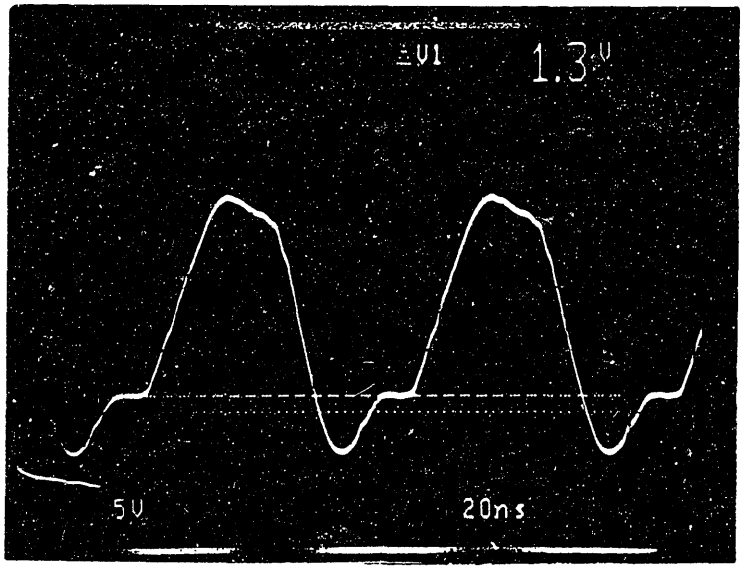


Figure 7.5: Gate Drive (v_{GS}) at 12.0 MHz
(v_{DS} = 0 V)
5 V/div, 20 nsec/div

(Bottom cursors indicate ground)

The resonant tank was slowed down by adding two 75 pF mica capacitors, a total of 150 pF, in parallel with each FET. The total resonant capacitance was then approximately 261 pF, the sum of the 150 pF mica capacitance and the 111 pF effective output capacitance of each FET. This capacitance, together with the 0.5 μH tank inductor, corresponds to a resonant frequency of 13.9 MHz.

The Q of the resonant tank, as computed from equation 4.5, decreased with the increased capacitance. According to equations 4.2 and 4.5, as the Q of the circuit is reduced, the peak switch voltage and current decrease, easing the requirements for the MOSFET. If the Q is too low, however, the capacitor voltage never rings to zero and the circuit does not function properly. The 18.2 Ω load resistance of the original circuit was empirically found to be the maximum that allowed the circuit to function properly. The optimal load resistance for the modified circuit was found empirically to be 16.4 Ω. The modified circuit is shown in figure 7.6.

Slowing down the tank has the advantage of increasing the maximum power that can be delivered by the circuit. In both the original and the modified circuits the maximum power is limited by the peak voltage across each switch, since the voltage reaches its design limit, 90 V peak, before the switch current reaches its design limit, 3 A rms. Since the peak switch voltage and rms current are related by equation 4.4, increasing the capacitance while holding the peak switch voltage constant will increase the rms switch current and, therefore, the maximum load power. This assertion was verified experimentally by comparing the operation of the original and the modified circuit. The maximum power that the original design could deliver was 26.9 W at 10.0 MHz. The modified circuit can deliver 56.7 W at 6.5 MHz.

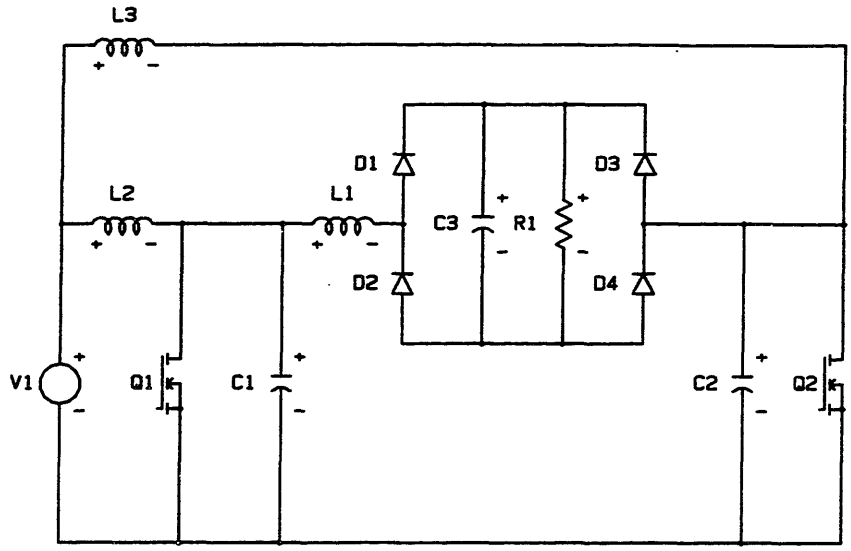


Figure 7.6: Modified Experimental Circuit

L1 = 0.5 μH
L2 = L3 = 120 μH
C1 = C2 = 150 pF
C3 = 8.8 μF
R1 = 16.4 Ω
Q1 = Q2 = Motorola MTP8N10
D1 ... D4 = Motorola MBR340P

The original design avoided the need for explicit capacitors by using the output capacitances of the power MOSFETs as the resonant tank capacitors. The limited current sourcing ability of the gate drive required the addition of external capacitors. Although additional circuit components had to be added, the power rating of the resulting circuit is double that of the original design.

7.4: Refining the Parity Simulation

The use of a printed circuit board precluded measurements of all currents except the input and output currents. Currents were estimated from the Parity Simulation, which was refined by matching experimentally measured voltages to those observed on the Simulator. The simulated currents were assumed to be an accurate reflection of the currents in the actual circuit, and were then used to estimate the distribution of power dissipation in the experimental converter.

The introduction of external capacitors in the resonant tank introduced substantial ringing into the MOSFET voltage and current waveforms. This ringing is caused by the interaction of the mica capacitors and the FET output capacitances with the inductance associated with the physical separation of the mica capacitors and the FET package leads. Figure 7.7 shows a sample drain-to-source voltage waveform from the original experimental circuit, while figure 7.8 shows a sample drain-to-source voltage waveform from the modified experimental circuit. The trace connecting the capacitors with the MOSFETs is 2.15" long and the theoretical analysis would therefore predict a value of 43 nH.

The refined Parity Simulator model is shown in figure 7.9. Inductors L_1 and L_3 model this lead inductance. The value of lead inductance which resulted in the best match of the simulated v_{DS} with the waveform of figure

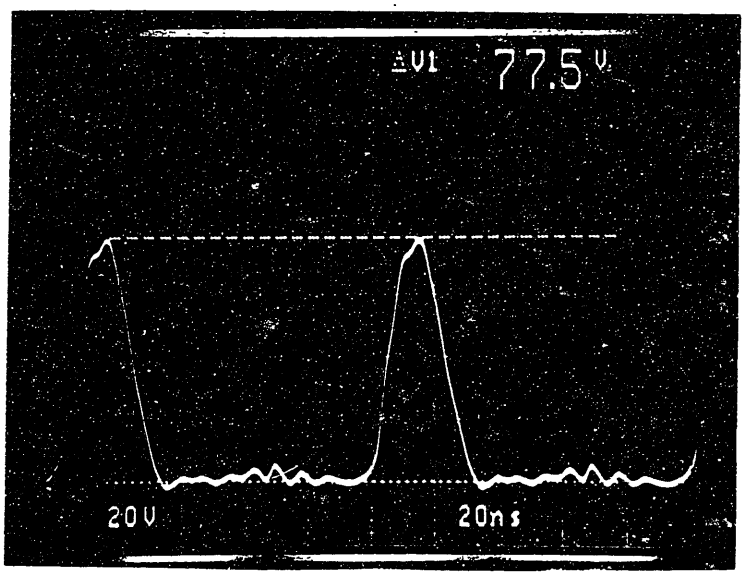


Figure 7.7: v_{DS}, Original Circuit
(f_d = 10.0 MHz, v_{in} = 15 V)
20 V/div, 20 nsec/div

(Bottom cursors indicate ground)

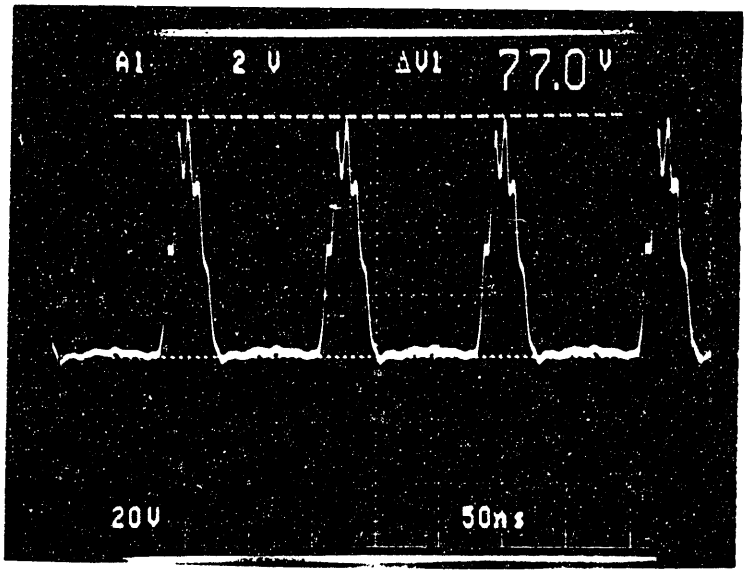


Figure 7.8: v_{DS}, Modified Circuit
(f_d = 8.0 MHz, v_{in} = 15 V)
20 V/div, 50 nsec/div

(Bottom cursors indicate ground)

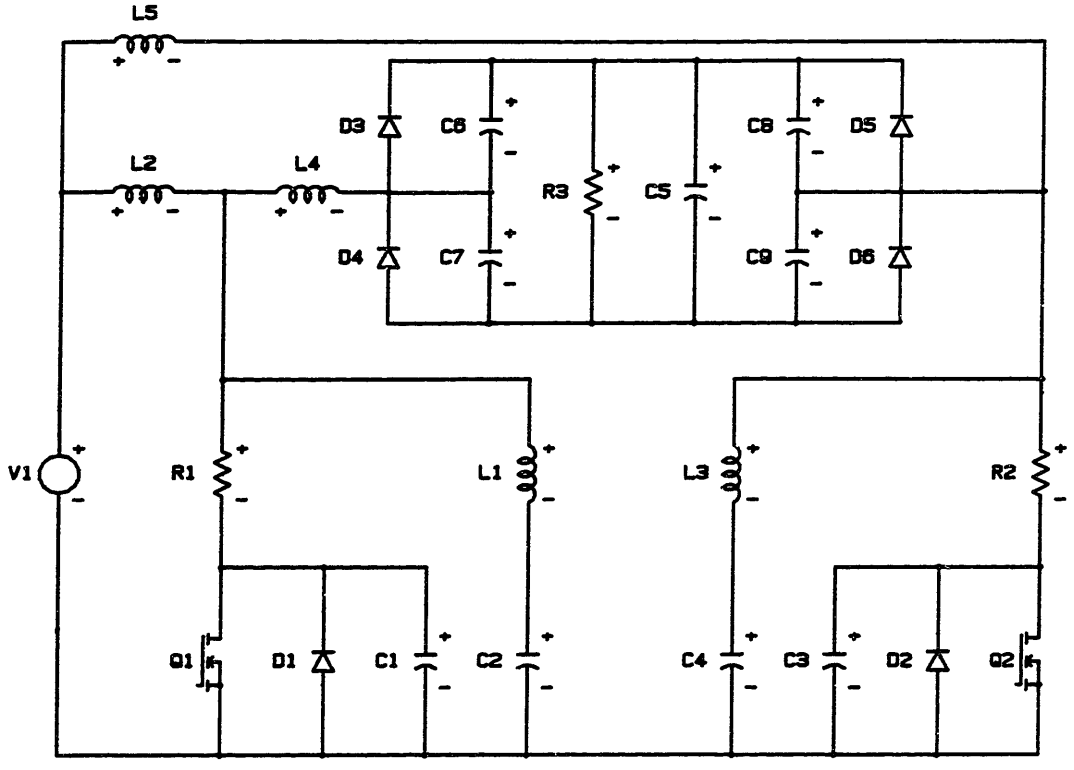


Figure 7.9: Refined Parity Simulation Model

L1 = L3 = 30 nH
L2 = L5 = 120 μH
L4 = 0.5 μH
C1 = C3 = 111 pF
C2 = C4 = 150 pF
C5 = 8.8 μF
C6 ... C9 = 200 pF
R1 = R2 = 0.35 Ω
R3 = 16.4 Ω

7.8 was 30.0 nH. The 13 nH difference between theoretical prediction and Parity Simulation can be accounted for by the inaccuracies of the theoretical analysis as well as the Parity Simulation. The theoretical analysis assumed an infinite ground plane, whereas the actual ground plane is not only finite, but interrupted by component leads. Moreover, the lumped parameter analysis is itself only an approximation. The Parity Simulation, for its part, does not model the nonlinear FET output capacitance.

Capacitors C_6 through C_9 model the depletion capacitance of the Schottky diodes. Their value of 200 pF was also found by matching the simulated to the experimental waveforms.

The experimental voltage waveform is expanded in figure 7.10 and is quite similar to the simulated waveform of figure 7.11. This close correspondence between simulation and experiment in the voltage waveforms is the basis for confidence in the simulated current waveforms.

7.5: Regulation and Efficiency of the Converter

In this section experimental data is presented to demonstrate the linear regulation and the efficiency of the converter. This data is found to be consistent with expectations.

The gate drive and the power circuit represent two different, though interrelated, problems. Therefore, unless otherwise noted, the efficiency calculations in this chapter do not include the power loss of the gate drive.

The input and output currents were measured with a Tektronix A6302 Hall effect current probe with an AM503 modular amplifier. Input voltage was measured with a Fluke 8020A digital multimeter. The input power was calculated from these measurements as

$$P_{in} = I_{in} V_{in} \qquad (7.1)$$

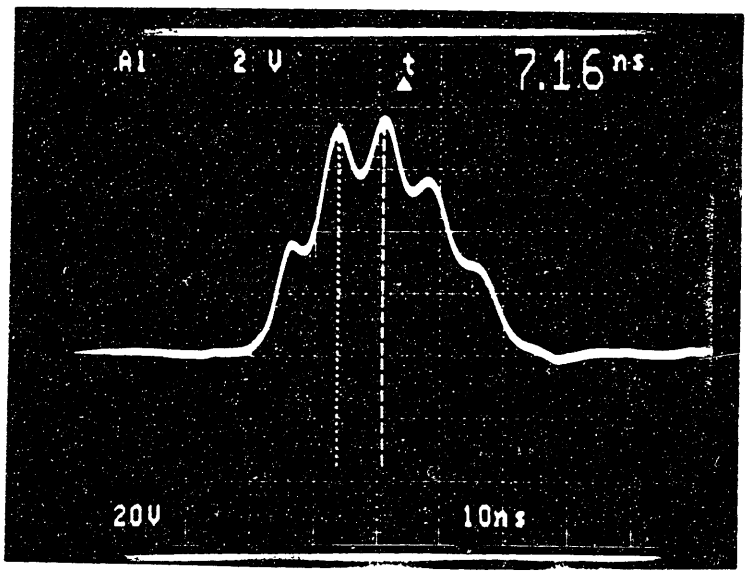


Figure 7.10: Experimental v_{DS}
(f_d = 8.0 MHz, v_{in} = 15 V)
20 V/div, 10 nsec/div

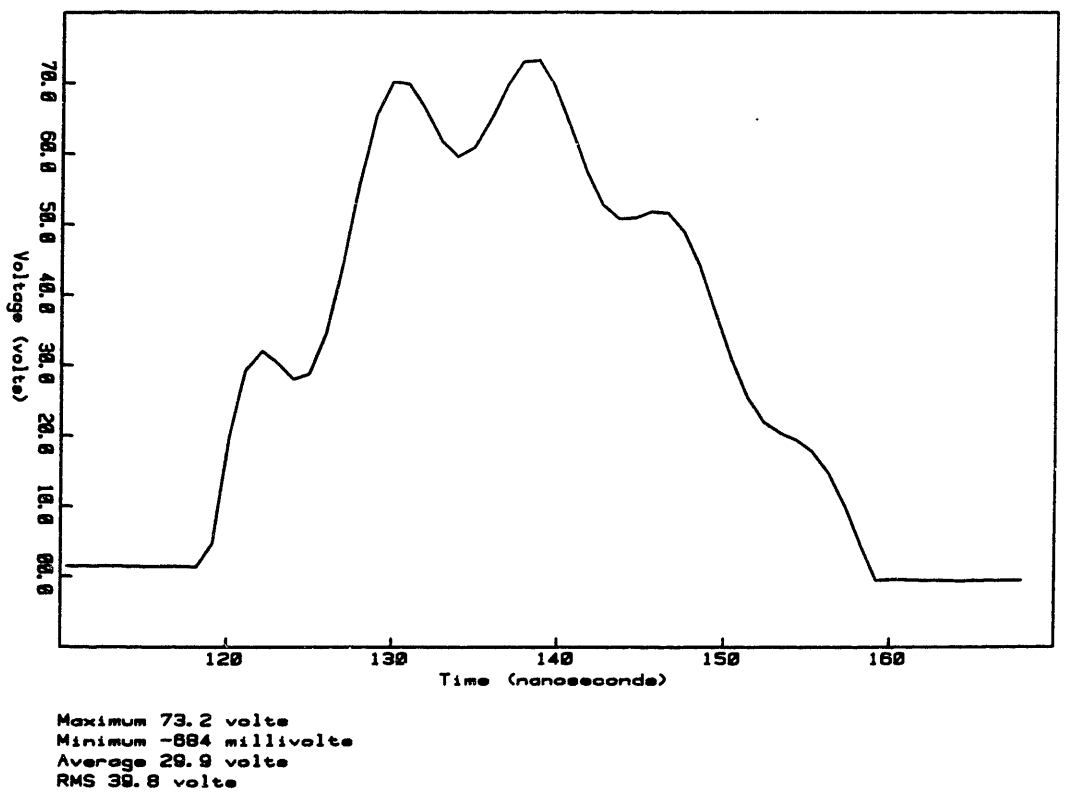


Figure 7.11: Simulated v_{DS}
(f_d = 8.0 MHz, v_{in} = 15 V)

The output power was calculated as

$$P_{out} = I_{out}^2 R_{load} \tag{7.2}$$

since the current ripple was negligible. The load resistance was measured with the Fluke meter. The efficiency was then simply defined as

$$\text{efficiency} = 100 \, (P_{out} / P_{in}) \tag{7.3}$$

The output voltage was not measured directly for two reasons. First, stray magnetic fields caused the Fluke meter to display erroneously high readings. Second, the large common mode voltage across the load resistor prevented use of an oscilloscope. The floating oscilloscope could not track the common mode signal, resulting in large ground currents that distorted the displayed waveform.

Figures 7.12 and 7.13 show input current and output voltage plotted as functions of gating frequency, for a constant input voltage of 15 V. Note the linear regulation curve of the output voltage, which is proportional to the output current. Representative input and output current waveforms are pictured in figures 7.14 and 7.15.

The efficiency, plotted as a function of frequency in figure 7.16, ranges from a peak of 85.9% at 7.0 MHz to lows of 81.2% at 12.0 MHz and 81.8% at 6.0 MHz. As discussed in section 7.2, the limited current sourcing ability of the gate drive degrades the efficiency at the high end of the frequency range. In addition, if the frequency is too high, the drain-to-source voltage does not ring to zero before the switch is gated, resulting in higher losses.

At the low frequency extreme the drain-to-source voltage begins to ring positive again before the switch is gated. Again, the non-zero drain-to-source voltage at the time of switching causes additional switching losses.

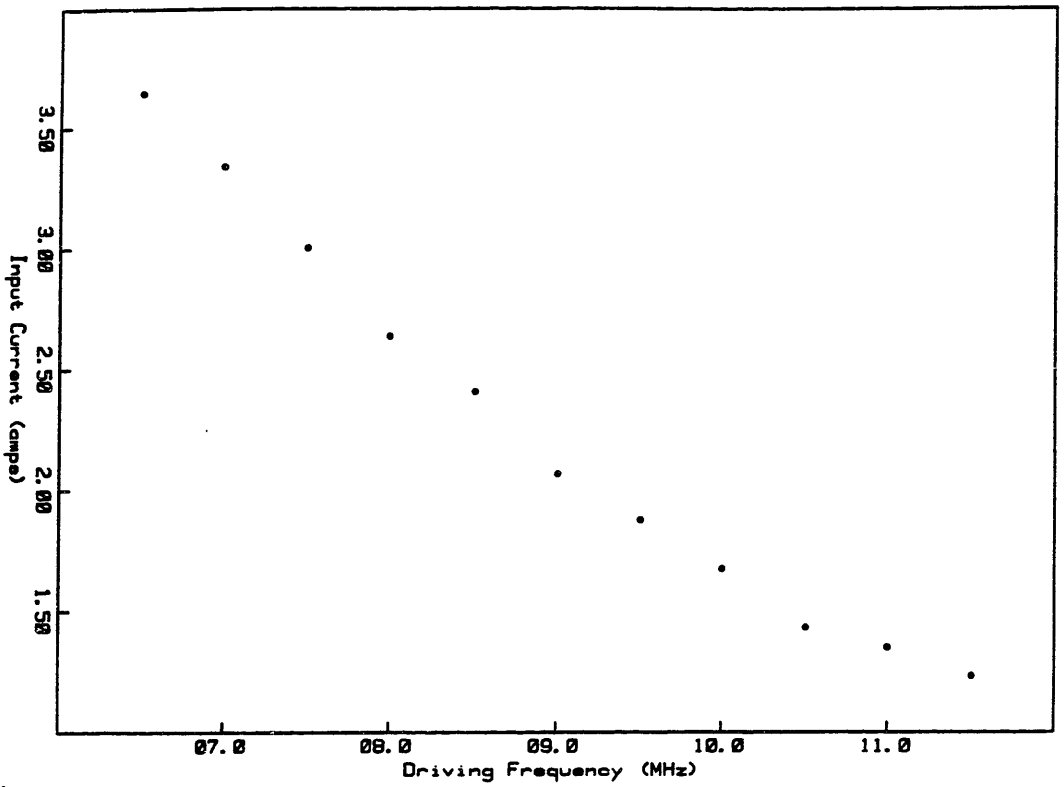


Figure 7.12: Input Current vs Frequency (V_{in} = 15 V)

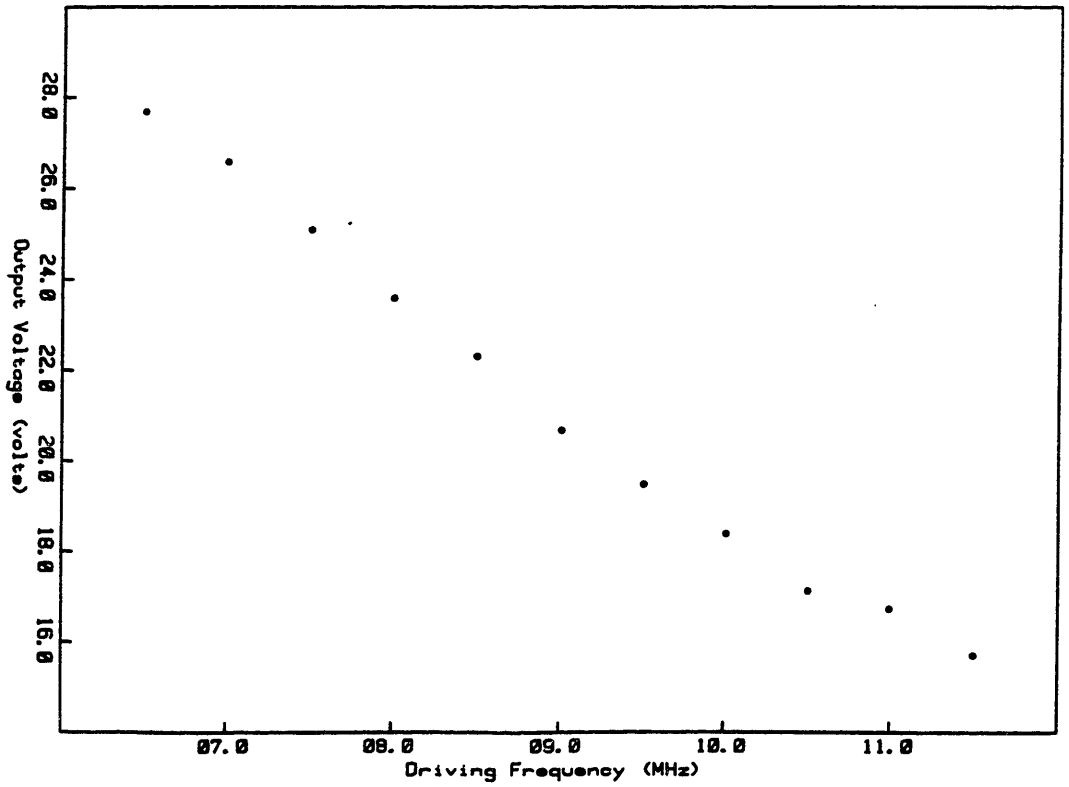


Figure 7.13: Output Voltage vs Frequency (V_{in} = 15 V)

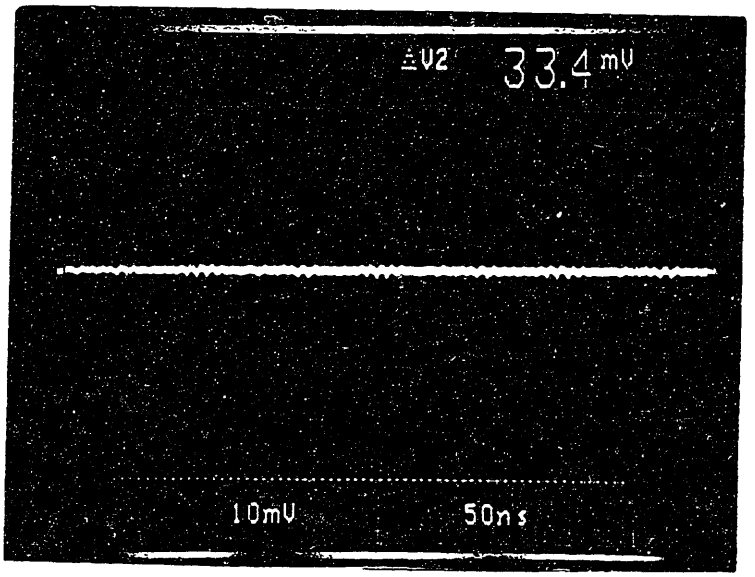


Figure 7.14: I_{in}
(f_d = 7.0 MHz, v_{in} = 15 V)
1 A/div, 50 nsec/div

(Bottom cursors indicate zero current)

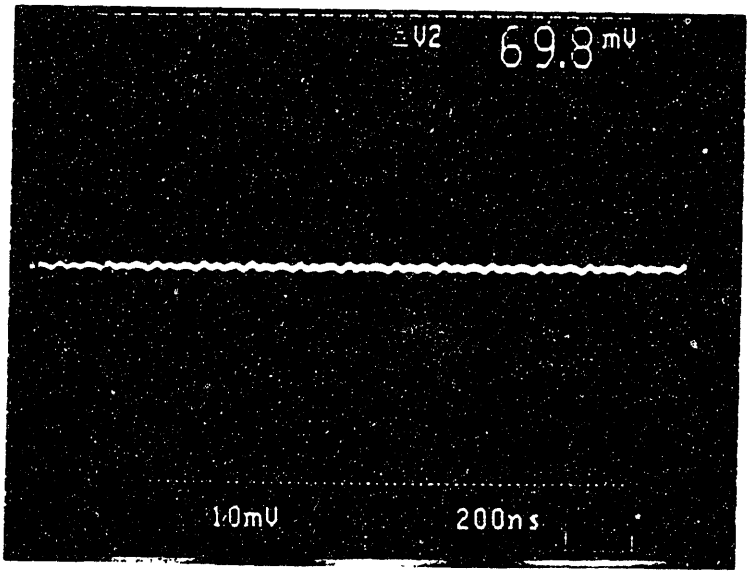


Figure 7.15: I_{out}
(f_d = 7.0 MHz, v_{in} = 15 V)
0.5 A/div, 200 nsec/div

(Bottom cursors indicate zero current)

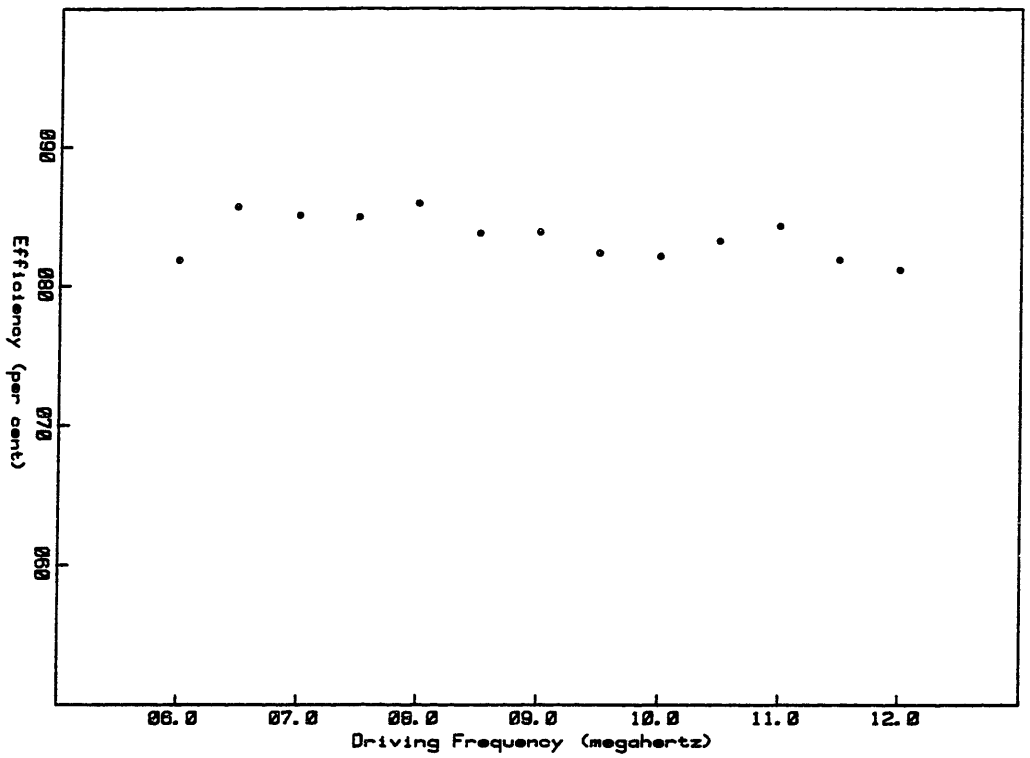


Figure 7.16: Efficiency vs Frequency (V_{in} = 15 V)

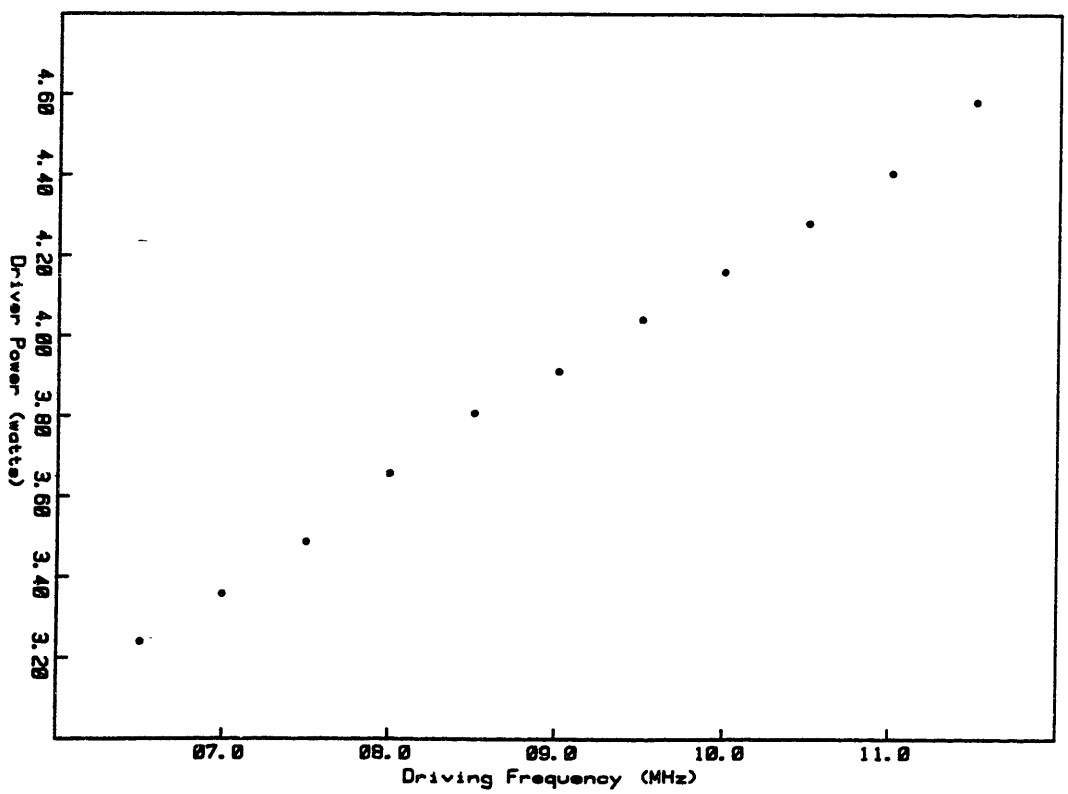


Figure 7.17: Driver Power vs Frequency (V_{in} = 15 V)

As predicted, this converter demonstrates the linear regulation curve of the current mode sine wave inverter. The variation in efficiency is consistent with expectations.

7.6: Power Dissipation in the Gate Drive

The power dissipation in the gate drive can be divided into two components. The -15 V supply provides power to the ECL controller. The controller dissipates about 4.6 W. The power sourced by the +15 V supply, which provides power to the DS0026 drivers, is plotted as a function of frequency in figure 7.17. The minimum power dissipated is 3.05 W at 6.0 MHz, and the maximum is 4.74 W at 12.0 MHz. At 10 MHz the +15 V supply provides 4.16 W, or about 2 W per transistor. This is only twice the minimum power that must be supplied in order to achieve the 0 to 15 V gate-to-source voltage swing, as calculated in chapter five. It is, however, more than an order of magnitude greater than the minimum power needed to switch the device between the threshold voltage and strong inversion, which was calculated as 0.14 W per transistor. Clearly, there is room for improvement.

7.7: Power Dissipation in the Power Circuit

Power loss is analysed below near each extreme of the gating frequency range; one analysis was performed at 6.5 MHz, the other at 12.0 MHz. At each operating point, the input voltage was adjusted so that 35.4 W would be delivered to the 16.4 Ω load resistor. Four loss mechanisms were identified: bridge diode losses, tank inductor core and winding losses, MOSFET conduction losses, and MOSFET switching losses. Losses in the low dissipation mica capacitors were not considered since their temperature rise was negligible.

Current measurements were made with the Tektronix 2465 oscilloscope

and the Tektronix AM503 current probe assembly. Voltage and resistance measurements were performed with the Fluke 8020A meter. Temperature measurements were also made with the Fluke meter in conjunction with its 80T-150 temperature probe. Tables 7.1 and 7.2 list the instrument accuracies specified by the manufacturers and derive error estimates for the input and output power measurements.

Tank inductor, diode, and MOSFET currents could not be measured directly and were therefore estimated from Parity Simulation. MOSFET on-state resistance values and diode forward voltage drops were estimated from the manufacturer's data sheets. Tank inductor core and winding losses were computed according to equation 6.9.

Tables 7.3 and 7.4 list the input and output powers measured at the two operating points. Approximately 6.1 W were lost during 6.5 MHz operation, about 15% of the total input power. The loss increased to 20% at 12.0 MHz.

Figures 7.18 through 7.23 show the experimental v_{DS} and v_{GS} waveforms at each frequency. In figures 7.20 and 7.23 v_{DS} and v_{GS} are superimposed in order to clarify their relative positions. A non-inductive probe tip was used for figures 7.18, 7.19, 7.21, and 7.22, while a standard probe tip was used to observe v_{GS} in figures 7.20 and 7.23. This accounts for the slight differences in the waveforms.

Certain features of the experimental waveforms require elaboration. The gate drive displays a great deal of ringing at turn-off, but not at turn-on. This is caused by the building up of a large v_{DS} following turn-off, which reduces the input capacitance of the MOSFET and therefore reduces the damping ratio, as well as shifting the ringing frequency. In figure 7.2 there is little ringing at either turn-on or turn-off, since v_{DS}

Table 7.1: Accuracy of Measuring Equipment

Parameter	Device	Accuracy
Current	Tektronix 2465 Oscilloscope	±2.0%
	Oscilloscope Cursor Accuracy	±1.25%
	Tektronix AM503 Current Probe	±3.0%
	Total	±6.25%
Voltage Resistance	Fluke 8020A Digital Multimeter	±0.1%

Table 7.2: Experimental Error Estimates

Parameter	Error Algorithm	Error
$P_{in} = I_{in}V_{in}$	$100[1 - (1\pm0.0625)\ (1\pm0.001)]$	±6.36%
$P_{out} = I_{out}^2R$	$100[1 - (1\pm0.0625)^2\ (1\pm0.001)]$	±13.0%

Table 7.3: Power Dissipation Error Analysis at 6.5 MHz

Parameter	Algorithm	Result
P_{in}	$(V_{dc,in})$ $(I_{dc,in})$	
	(12.94 V) (3.21 A)	41.5 W
Error, P_{in}	$\pm$(0.0636) (41.5 W)	$\pm$2.64 W
P_{out}	$(I_{dc,out})^2$ (R_{load})	
	$(1.47\ A)^2$ (16.4 Ω)	35.4 W
Error, P_{out}	$\pm$(0.13) (35.4 W)	$\pm$4.60 W
ΔP	$P_{in} - P_{out}$	
	(41.5 - 35.4) W	6.1 W
Error, ΔP	$\pm$(4.60 - 2.64) W	$\pm$1.94 W

Table 7.4: Power Dissipation Error Analysis at 12.0 MHz

Parameter	Algorithm	Result
P_{in}	$(V_{dc,in})$ $(I_{dc,in})$	
	(24.68 V) (1.79 A)	44.2 W
Error, P_{in}	$\pm$(0.0636) (44.2 W)	$\pm$2.81 W
P_{out}	$(I_{dc,out})^2$ (R_{load})	
	$(1.47\ A)^2$ (16.4 Ω)	35.4 W
Error, P_{out}	$\pm$(0.13) (35.4 W)	$\pm$4.60 W
ΔP	$P_{in} - P_{out}$	
	(44.2 - 35.4) W	8.8 W
Error, ΔP	$\pm$(4.60 - 2.81) W	$\pm$1.79 W

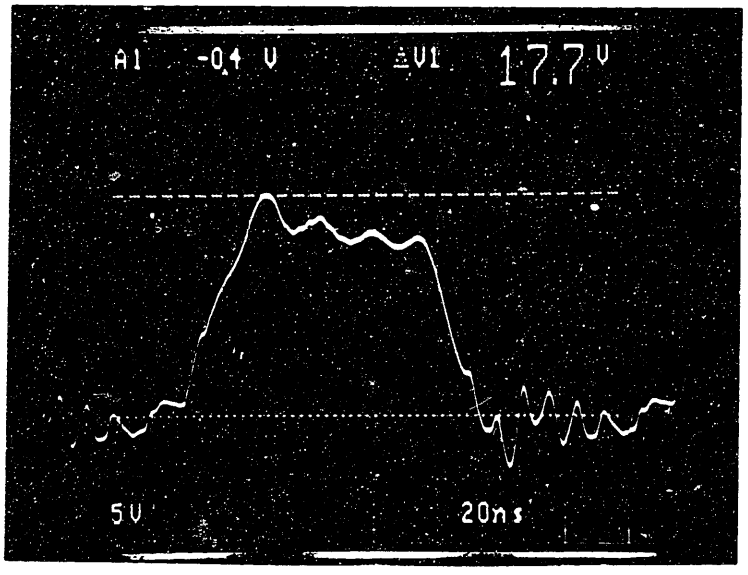


Figure 7.18: v_{GS} at 6.5 MHz
(f_d = 6.5 MHz, v_{in} = 12.9 V)
5 V/div, 20 nsec/div

(Bottom cursors indicate ground)

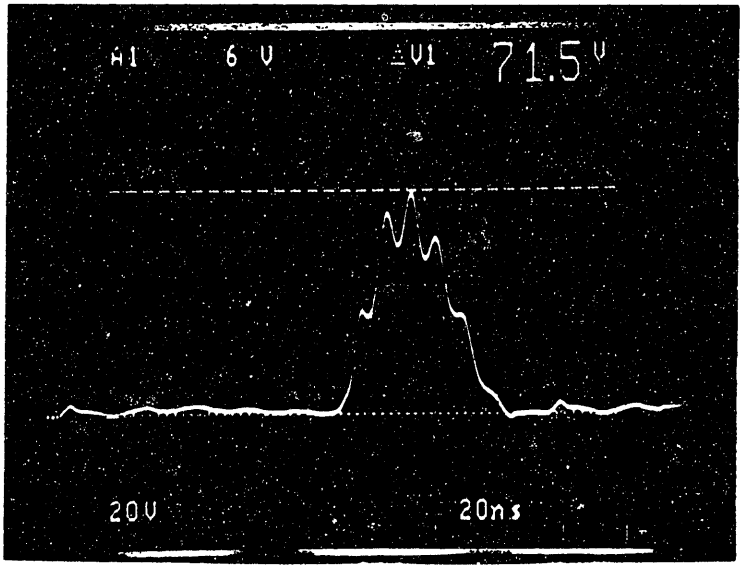


Figure 7.19: v_{DS} at 6.5 MHz
(f_d = 6.5 MHz, v_{in} = 12.9 V)
20 V/div, 20 nsec/div

(Bottom cursors indicate ground)

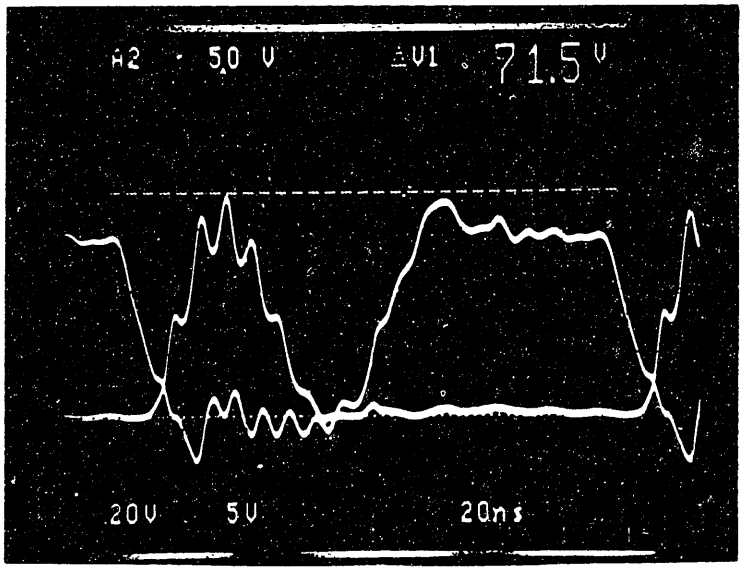


Figure 7.20: v_{GS} and v_{DS} at 6.5 MHz
(v_{in} = 12.9 V)
5 V/div (v_{GS}), 20 V/div (v_{DS}), 20 nsec/div

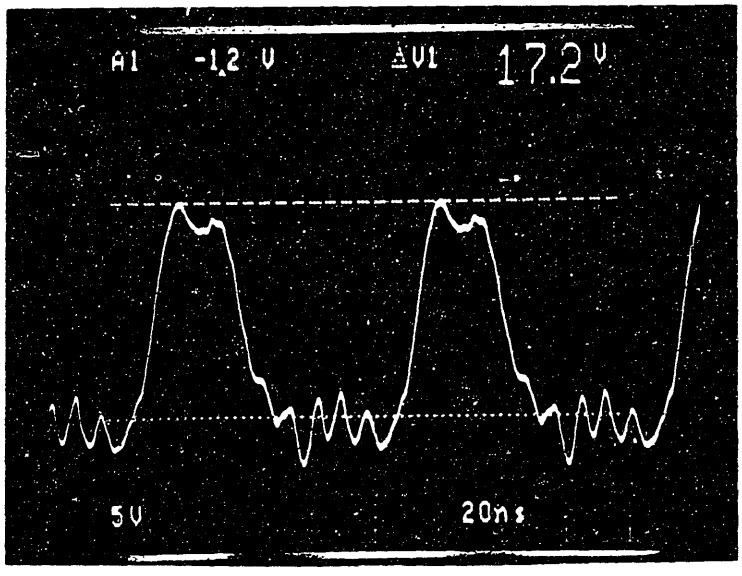


Figure 7.21: v_{GS} at 12.0 MHz
(f_d = 12.0 MHz, v_{in} = 25 V)
5 V/div, 20 nsec/div

(Bottom cursors indicate ground)

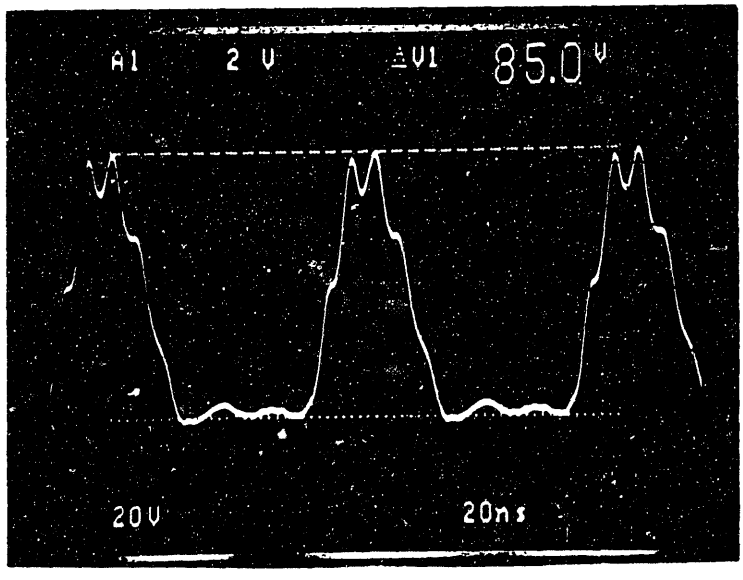


Figure 7.22: v_{DS} at 12.0 MHz
(f_d = 12.0 MHz, v_{in} = 25 V)
20 V/div, 20 nsec/div

(Bottom cursors indicate ground)

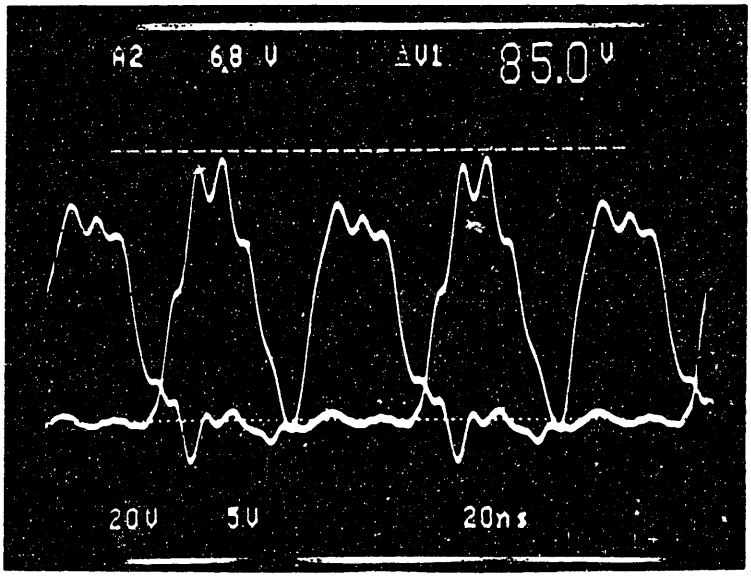


Figure 7.23: v_{GS} and v_{DS} at 12.0 MHz
(v_{in} = 25.0 V)
5 V/div (v_{GS}), 20 V/div (v_{DS}), 20 nsec/div

is clamped at zero and the input capacitance is large, resulting in a large damping ratio and a slower ring.

As predicted in chapter five, the Miller effect is manifest only at turn-off. In figures 7.20 and 7.23 the plateau in v_{GS} that occurs as the device tries to turn off is coincident with the sinusoidal rise of v_{DS}.

Tables 7.5 and 7.6 show the distribution of the power dissipation. The simulated circuit waveforms used in this analysis are shown in figures 7.24 through 7.31. The power loss unaccounted for by diode, inductor, or MOSFET conduction losses is assumed to be dissipated during switching. This analysis suggests that each FET dissipates about 2.5 W at 6.5 MHz and 3.3 W at 12.0 MHz.

This analysis was confirmed by measuring the temperature rise of the MOSFET cases and relating this measurement to the power dissipated by means of the thermal resistance of the heat sink. These results are presented in tables 7.7 and 7.8. Electromagnetic interference prevented the temperature probe from functioning properly during circuit operation, so the following procedure was used. While the power circuit was operating, the thermistor probe tip was brought into contact with the FET case. After the probe reached thermal equilibrium with the FET case, the power was interrupted and the measurement was immediately made.

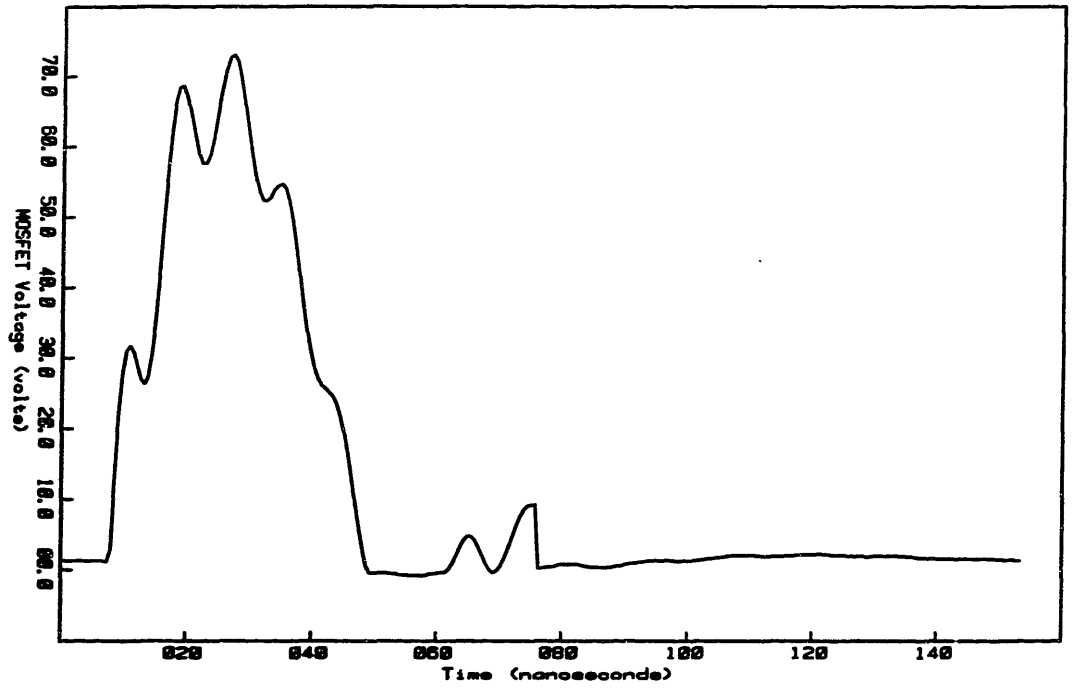
The case-to-air thermal resistance of the MOSFET on its heat sink was experimentally determined by mounting another MTP8N10 MOSFET on another HP-1 heat sink in a fashion similar to that of the converter. A constant gate potential was applied so that the FET conducted a dc drain current through a load resistor. By measuring v_{DS} and the drain current, the power dissipated in the device was calculated. The current was determined with the Fluke meter by measuring both the voltage across the load resistor, and the

Table 7.5: Power Dissipation Composition Analysis at 6.5 MHz

Parameter	Algorithm	Result
P_d, Bridge Diodes	(# of Diodes) $\langle I_{diode} \rangle$ ($V_{forward}$)	
	(4) (0.63 A) (0.3 V)	0.76 W
P_d, Tank Inductor	eq. 6.9 evaluated at I_{rms} = 1.57 A	0.32 W
P_d, FET Conduction	(# of FETs) $(I_{rms,FET})^2$ (R_{on})	
	(2) $(2.03\ A)^2$ (0.35)	2.88 W
P_d, FET Switching	(6.1 - 0.76 - 0.32 - 2.88) W	2.14 W
Total Power Dissipated in Each FET	[(2.88 + 2.14) / 2 ± (1.94 / 2)] W	2.51 ± 0.97 W

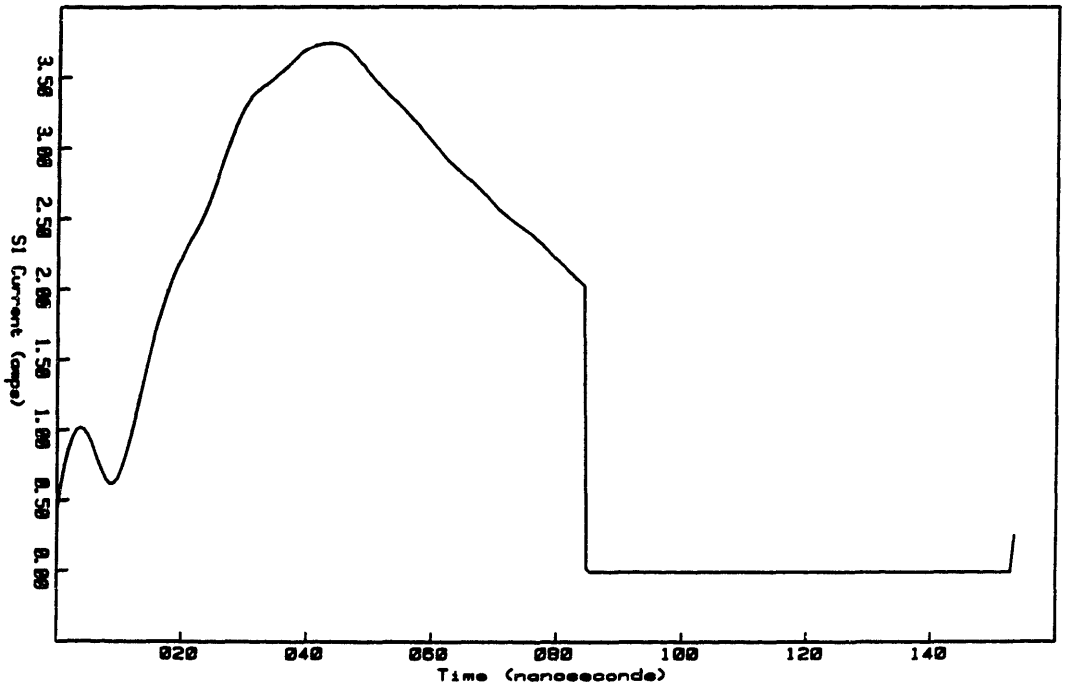
Table 7.6: Power Dissipation Composition Analysis at 12.0 MHz

Parameter	Algorithm	Result
P_d, Bridge Diodes	(# of Diodes) $\langle I_{diode} \rangle$ ($V_{forward}$)	
	(4) (0.63 A) (0.3 V)	0.76 W
P_d, Tank Inductor	eq. 6.9 evaluated at I_{rms} = 1.65 A	0.57 W
P_d, FET Conduction	(# of FETs) $(I_{rms,FET})^2$ (R_{on})	
	(2) $(1.48\ A)^2$ (0.35)	1.53 W
P_d, FET Switching	(8.8 - 0.76 - 0.57 - 1.53) W	5.94 W
Total Power Dissipated in Each FET	[(1.53 + 5.94) / 2 ± (1.79 / 2)] W	3.74 ± 0.90 W



Maximum 73.1 volts
Minimum -782 millivolts
Average 12.7 volts
RMS 24.7 volts

Figure 7.24: Simulated v_{DS} at 6.5 MHz (v_{in} = 12.9 V)



Maximum 3.74 amps
Minimum -4.89 milliamps
Average 1.41 amps
RMS 2.03 amps

Figure 7.25: Simulated Drain Current at 6.5 MHz (v_{in} = 12.9 V)

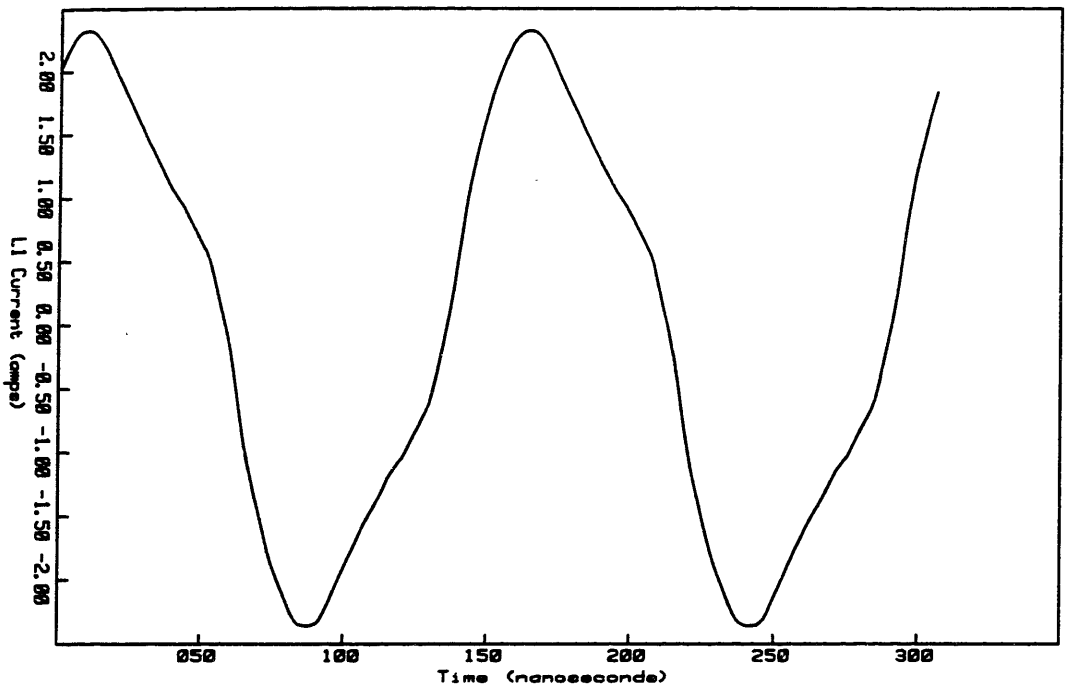


Figure 7.26: Simulated Tank Inductor Current at 6.5 MHz (v_{in} = 12.9 V)

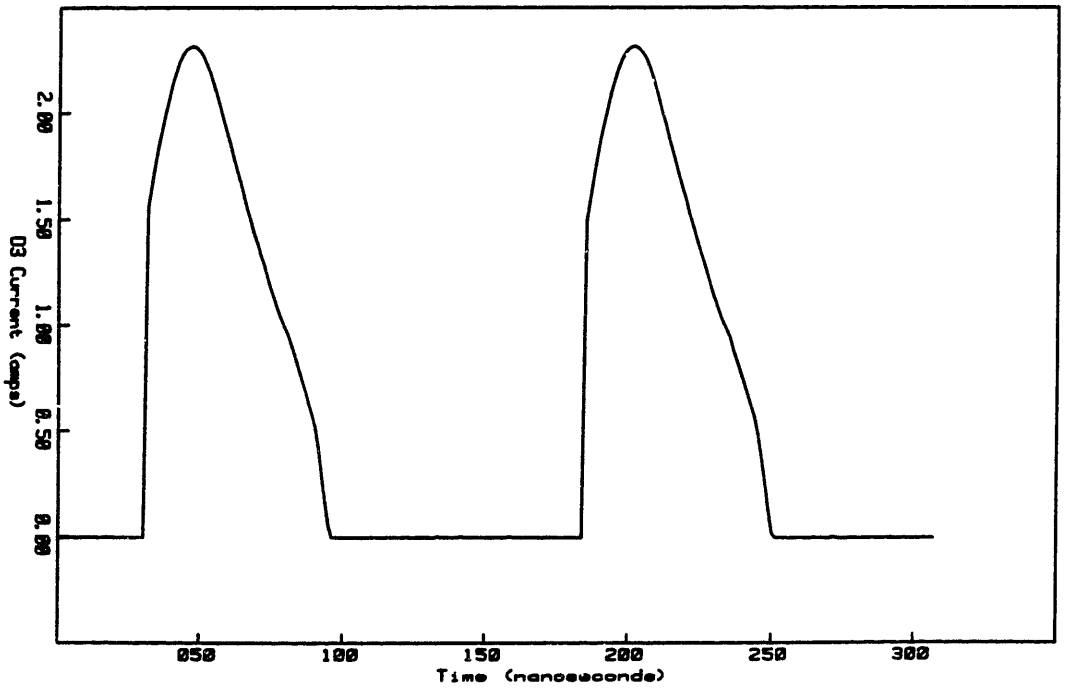
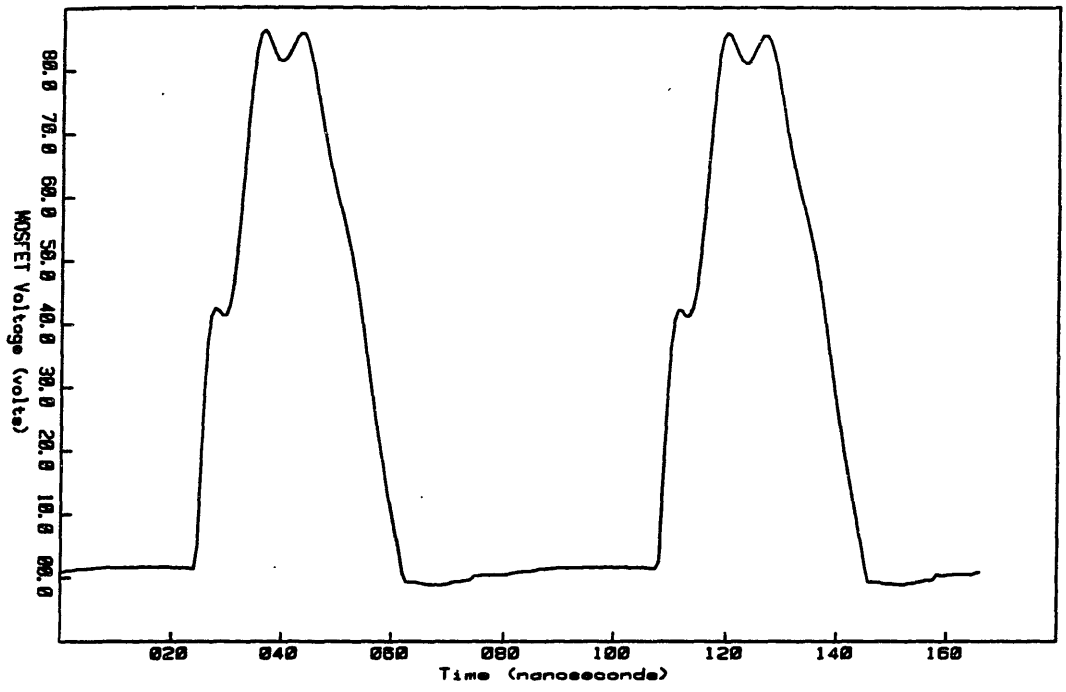
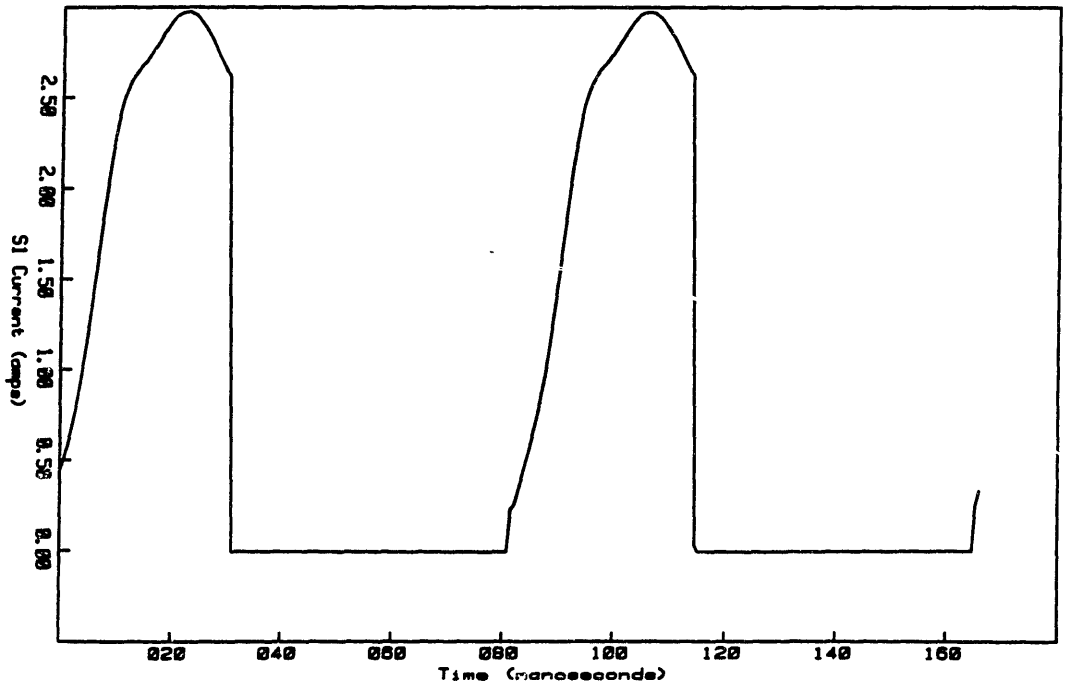


Figure 7.27: Simulated Diode Current at 6.5 MHz (v_{in} = 12.9 V)



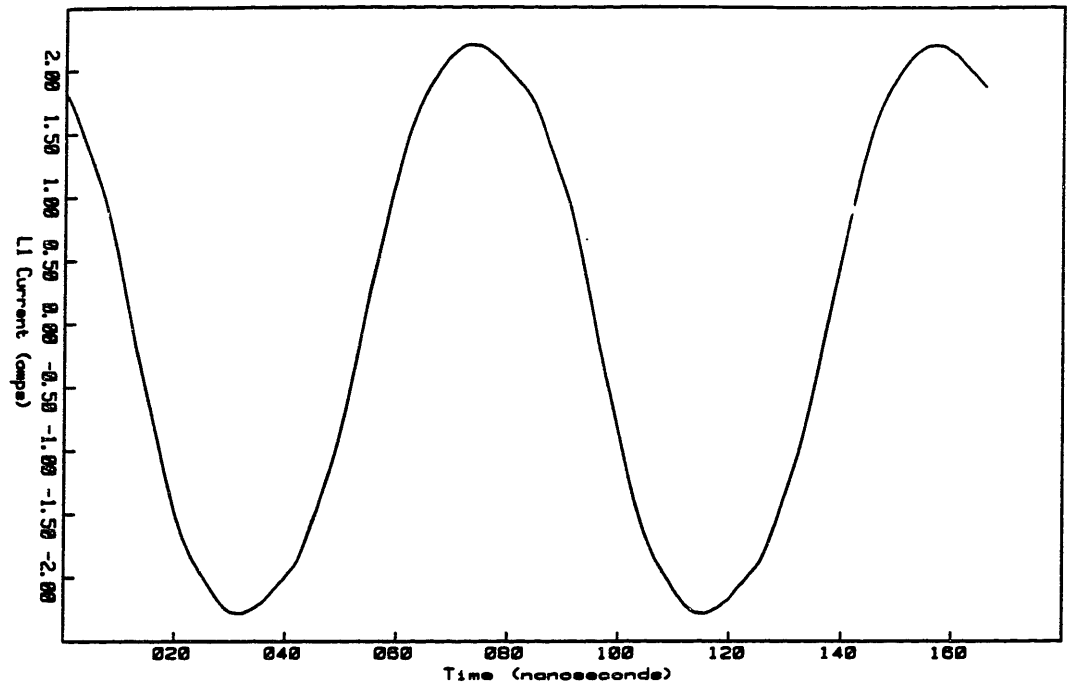
Maximum 80.4 volts
Minimum -1.17 volts
Average 24.9 volts
RMS 40.4 volts

Figure 7.28: Simulated v_{DS} at 12.0 MHz (v_{in} = 25 V)



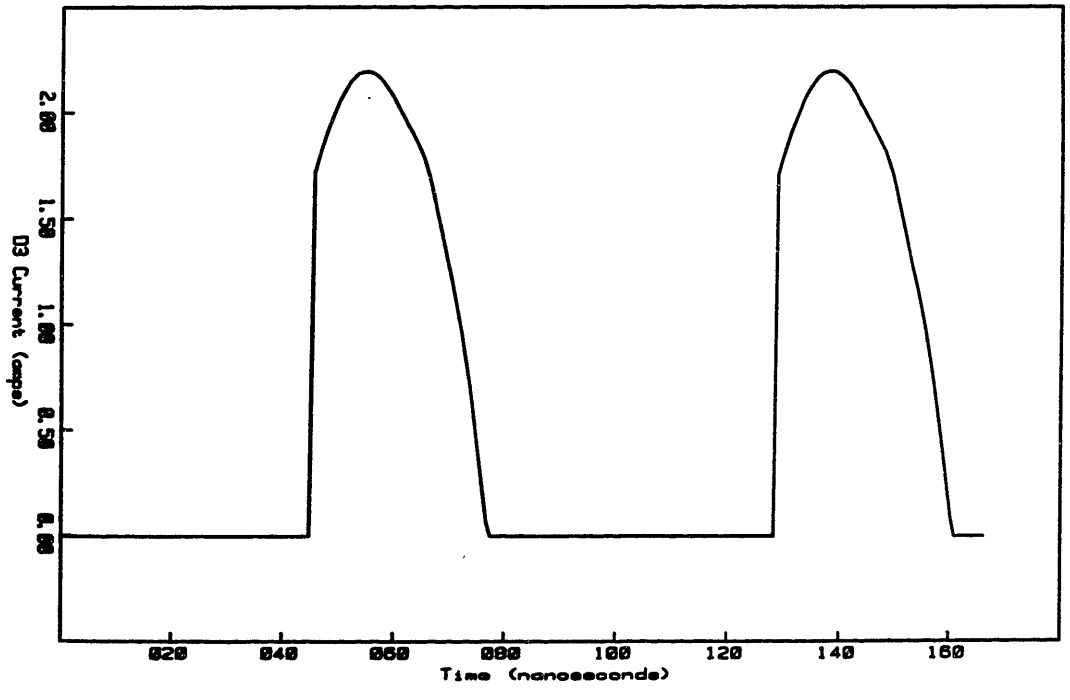
Maximum 2.98 amps
Minimum -4.89 milliamps
Average 853 milliamps
RMS 1.48 amps

Figure 7.29: Simulated Drain Current at 12.0 MHz (v_{in} = 25 V)



Maximum 2.20 amps
Minimum -2.28 amps
Average -27.4 milliamps
RMS 1.65 amps

Figure 7.30: Simulated Tank Inductor Current at 12.0 MHz (v_{in} = 25 V)



Maximum 2.19 amps
Minimum -4.89 milliamps
Average 632 milliamps
RMS 1.00 amps

Figure 7.31: Simulated Diode Current at 12.0 MHz (v_{in} = 25 V)

Table 7.7: Experimental Determination of FET Power Dissipation at 6.5 MHz

Parameter	Algorithm	Result
Power Dissipation per FET	$\frac{[(T_f = 43.1°) - (T_i = 23.3°)]}{(R_{c-a} = 8.2\ °C/W)}$	2.42 W

Table 7.8: Experimental Determination of FET Power Dissipation at 12.0 MHz

Parameter	Algorithm	Result
Power Dissipation per FET	$\frac{[(T_f = 50.3°) - (T_i = 23.1°)]}{(R_{c-a} = 8.2\ °C/W)}$	3.32 W

value of resistance. Hence each individual measurement was within the 0.1% accuracy of the Fluke meter. The temperature rise of the case from ambient corresponded to an R_{c-a} of 8.2 °C/W. This value is within 4% of the value of 8.5 °C/W predicted in chapter six.

The power circuit dissipation analysis did not consider the effect of power supplied by the gate drive. With the power circuit off, v_{DS} equal to zero, and the gate drive set to 6.5 MHz, the temperature of each FET case rose by 1.2°C, which corresponds to 0.15 W dissipated per FET. At 12.0 MHz the temperature rise corresponded to 0.31 W dissipated per FET. When the power circuit was fired up, the gate drive power consumption did not increase by any measurable amount. The assumption was therefore made that the power dissipation in the FET due to the gate drive remains constant as the current switched by the FET increases.

The total expected power dissipation in each FET at 6.5 MHz would therefore be the sum of the 2.51 W computed in table 7.5 and the 0.15 W due to the gate drive. This expected dissipation of 2.66 W per transistor agrees well with the measured power dissipation of 2.42 W listed in table 7.7. The 0.24 W difference between the expected and measured values is within the uncertainty of 0.97 W.

Similarly, the expected power dissipation in each FET at 12.0 MHz, including the power supplied by the gate drive, was 4.05 W. This also agrees well with the measured power dissipation of 3.32 W listed in table 7.8. The 0.73 W difference is within the uncertainty of 0.90 W.

7.8: Summary

The experimental observations verify the conclusions of the theoretical analysis. The circuit is less efficient at the high extreme of the gating frequency range, and the additional power is dissipated primarily

during switching transitions in the MOSFETs. This loss is due to the long gate-to-source voltage switching times relative to the period.

These results confirm the predictions of chapters three and five. As expected, the efficiency of the circuit is dominated by the switching device. Low input capacitance is necessary for low switching losses, and low on-state resistance is necessary for low conduction losses.

Chapter Eight: Conclusion

This thesis has demonstrated that 50 W dc-to-dc converters may indeed be composed of rectified radio frequency resonant inverters employing power MOSFETs and Schottky diodes. The parasitic output capacitances associated with the MOSFETs have been successfully incorporated into the resonant tank, and Parity Simulation has been demonstrated to be a useful tool not only for design, but also for analysis. The course of the research highlighted several issues that need to be addressed in order to further develop radio frequency switching converters.

First, circuit switching speed and efficiency were shown to be inversely related to switch input capacitance. Commercially available MOSFETs are not designed with low capacitance as a primary goal, and are therefore not optimized for radio frequency operation. Such approaches as interdigitated topologies, improved gate alignment, and use of gallium arsenide could reduce input capacitance. In addition, replacing the polysilicon gate with metal would reduce the gate series resistance, thereby reducing the voltage transition times and tne gate power dissipation.

Work is required on a better gate drive circuit, since the switching speed and efficiency of the circuit are restricted by the ability of the gate drive to deliver and remove the capacitive charging current. And a lossless gate drive could improve circuit efficiency by recovering the energy stored in the input capacitance.

Different circuit topologies could be explored with the aid of Parity Simulation. The value of the Parity Simulation would be greatly enhanced with the development of models of nonlinear capacitors. Parity Simulation would then permit more accurate investigation of currents and voltages that can not be observed directly in the experimental circuit.

Finally, the physical size of the circuit could be greatly reduced by improved heat sinking of the MOSFET die. The size could be further reduced by integrating a lossless drive circuit on the same chip as the switch. This would also eliminate the parasitic lead inductance between drive and gate that causes potentially destructive gate voltage ringing.

Radio frequency resonant dc-to-dc converters may well provide high efficiency, low cost power conditioning. As device technology improves and switching speeds increase, these converters could become available as integrated circuits.

APPENDIX

Manufacturers' Data Sheets

MTM8N05, MTP8N05
MTM8N10, MTP8N10
MTM10N05, MTP10N05
MTM10N06, MTP10N06

MOTOROLA

C

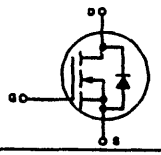
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

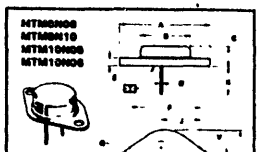
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



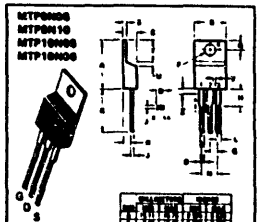
8.0 and 10 AMPERE
N-CHANNEL TMOS
POWER FET
$R_{DS(on)}$ = 0.5 OHM
50 and 100 VOLTS
$R_{DS(on)}$ = 0.30 OHM
50 and 60 VOLTS

MTM8N05
MTM8N10
MTM10N05
MTM10N06



CASE 1-05
TO-204AA
(TO-3 TYPE)

MTP8N05
MTP8N10
MTP10N05
MTP10N06



CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP				Unit
		10N05	10N06	8N05	8N10	
Drain-Source Voltage	V_{DSS}	50	60	50	100	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	60	50	100	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current — Continuous / Pulsed	I_D / I_{DM}	10 / 28		8.0 / 20		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C / Derate above 25°C	P_D	75 / 0.6				Watts / W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.5 mA)	MTM10N06/MTP10N06	$V_{(BR)DSS}$	60	—	Vdc
	MTM10N05/MTP10N05		50	—	
	MTM8N06/MTP8N06		60	—	
	MTM8N10/MTP8N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(T_J = 100°C)			—	2.5	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)	MTM10N06/MTM10N06 MTP10N06/MTP10N06	$r_{DS(on)}$	—	0.28	Ohms
(V_{GS} = 10 Vdc, I_D = 4.0 Adc)	MTM8N05/MTM8N10 MTP8N05/MTP8N10		—	0.50	
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 10 Adc)	MTM10N06/MTM10N06 MTP10N06/MTP10N06		—	3.4	
(I_D = 8.0 Adc, T_J = 100°C)	MTM8N06, MTM8N10 MTP8N06/MTP8N10		—	2.8	
(I_D = 8.0 Adc)	MTM10N05, MTM10N05 MTP10N05/MTP10N05		—	4.8	
(I_D = 4.0 Adc, T_J = 100°C)	MTM8N05/MTM8N10 MTP8N05/MTP8N10		—	4.0	
Forward Transconductance (V_{DS} = 15 V, I_D = 5.0 A)	MTM10N06/MTM10N06 MTP10N06/MTP10N06	g_{fs}	2.5	—	mhos
(V_{DS} = 15 V, I_D = 4.0 A)	MTM8N06/MTM8N10 MTP8N06/MTP8N10		1.5	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms, See Figures 1 and 2)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		t_f	—	60	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Characteristic		Symbol	Typ	Unit	
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0, See Figures 1 and 2)	V_{SD}	1.9	Vdc	
Forward Turn-On Time		t_{on}	200	ns	
Reverse Recovery Time		t_{rr}	300	ns	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 — SWITCHING TEST CIRCUIT

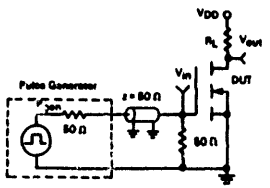
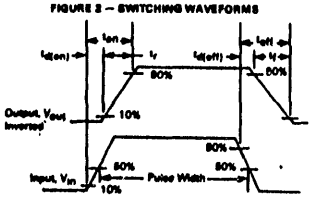


FIGURE 2 — SWITCHING WAVEFORMS



C

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TYPICAL CHARACTERISTICS

ON-REGION CHARACTERISTICS

FIGURE 3 — MTM8N08, MTM8N10
MTP8N08, MTP8N10

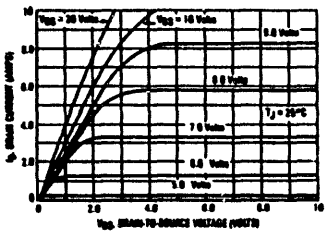
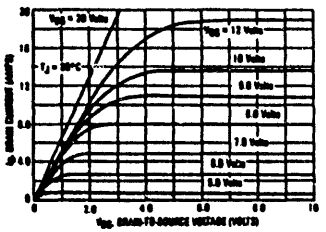


FIGURE 4 — MTM10N05, MTM10N06
MTP10N05, MTP10N06



TRANSFER CHARACTERISTICS

FIGURE 5 — MTM8N08, MTM8N10
MTP8N08, MTP8N10

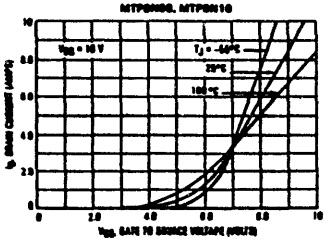
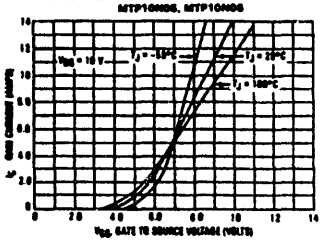


FIGURE 6 — MTM10N05, MTM10N06
MTP10N05, MTP10N06



ON-RESISTANCE versus DRAIN CURRENT

FIGURE 7 — MTM8N08, MTM8N10
MTP8N08, MTP8N10

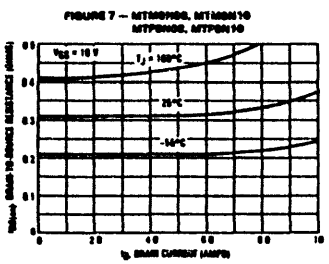
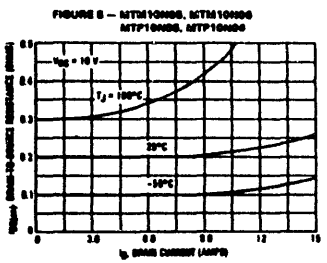


FIGURE 8 — MTM10N05, MTM10N06
MTP10N05, MTP10N06



C

TYPICAL CHARACTERISTICS

FIGURE 9 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

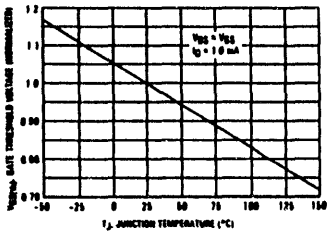
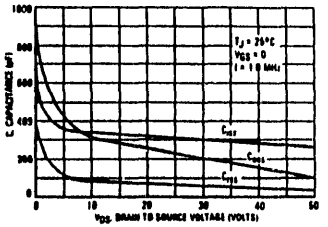


FIGURE 10 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 11 — MTM8N08, MTM8N10, MTM10N05, MTM10N06

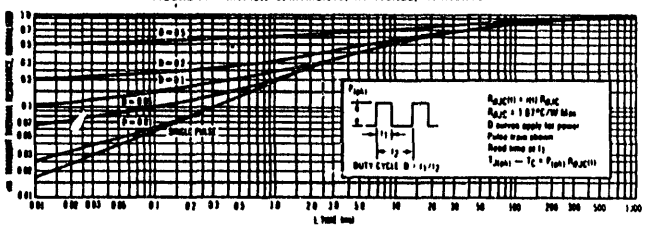
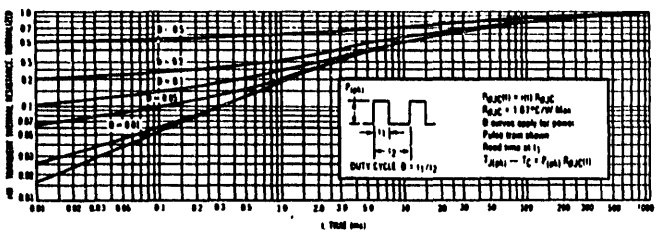


FIGURE 12 — MTM8N08, MTM8N10, MTM10N05, MTM10N06



C

SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 13 — MTM8N08, MTM8N10
MTP8N08, MTM8N10

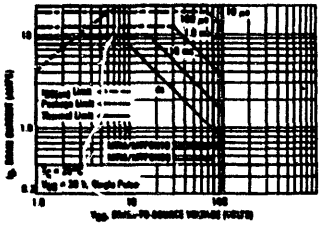
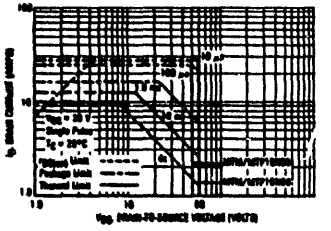


FIGURE 14 — MTM10N08, MTM10N06
MTP10N08, MTM10N06



FORWARD BIASED SAFE OPERATING AREA

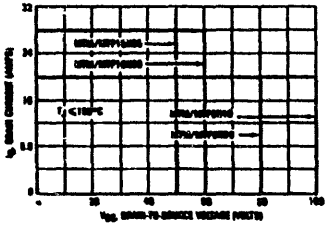
The dc data of Figures 13 and 14 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 13 and 14.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
$r(t)$ = normalized thermal response from Figures 11 or 12.

FIGURE 15 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 15 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 15 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

MOTOROLA

1N5820 MBR320P
1N5821 MBR330P
1N5822 MBR340P

Designers Data Sheet

AXIAL LEAD RECTIFIERS

employing the Schottky Barrier principle in a large area metal-to-silicon power diode. State-of-the-art geometry features epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low-voltage, high frequency inverters, free wheeling diodes, and polarity protection diodes.

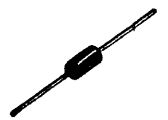
- Extremely Low v_F
- Low Power Loss/High Efficiency
- Low Stored Charge, Majority Carrier Conduction

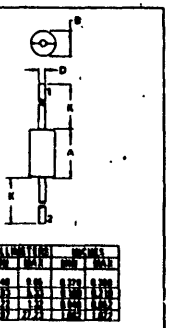
Designer's Data for Worst-Case Conditions

The Designer's Data sheets permit the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate worst-case design.

SCHOTTKY BARRIER RECTIFIERS

3.0 AMPERES
20, 30, 40 VOLTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.46	9.65	0.333	0.380
B	3.30	3.94	0.130	0.155
D	1.27	1.40	0.050	0.055
F	2.79	3.30	0.110	0.130
K	34.93	37.21	1.375	1.465

CASE 267-01

MECHANICAL CHARACTERISTICS

CASE	Transfer molded plastic
FINISH	All external surfaces corrosion-resistant and the terminal leads are readily solderable
POLARITY	Cathode indicated by polarity band
MOUNTING POSITIONS	Any
SOLDERING	220°C 1/16" from case for ten seconds

*MAXIMUM RATINGS

Rating	Symbol	1N5820 MBR320P	1N5821 MBR330P	1N5822 MBR340P	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	V
Non-Repetitive Peak Reverse Voltage	V_{RSM}	24	36	48	V
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	28	V
Average Rectified Forward Current (2) ($V_{R(equiv)} \le 0.2\ V_{R(DC)}$, T_L = 95°C, $R_{\theta JA}$ = 28°C/W, P.C. Board Mounting, see Note 2)	I_O	3.0			A
Ambient Temperature (Rated $V_{R(DC)}$, $P_{F(AV)}$ = 0, $R_{\theta JA}$ = 28°C/W)	T_A	80	85	80	°C
Non-Repetitive Peak Surge Current (Surge applied at rated load conditions, half wave, single phase 60 Hz, T_L = 75°C)	I_{FSM}	80 (for one cycle)			A
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}	−65 to +125			°C
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	150			°C

*THERMAL CHARACTERISTICS (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	28	°C/W

*ELECTRICAL CHARACTERISTICS (T_L = 25°C unless otherwise noted) (2)

Characteristic	Symbol	1N5820	1N5821	1N5822	MBR...P	Unit
Maximum Instantaneous Forward Voltage (1) i_F = 1.0 Amp i_F = 3.0 Amp i_F = 9.4 Amp	v_F	0.370 0.475 0.860	0.380 0.500 0.900	0.390 0.525 0.950	0.400 0.550 0.980	V
Maximum Instantaneous Reverse Current @ Rated dc Voltage (1) T_L = 25°C T_L = 100°C	i_R	2.0 20	2.0 20	2.0 20	2.0 20	mA

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Lead Temperature reference is cathode lead 1/32" from case.
*Indicates JEDEC Registered Data for 1N5820-22.

NOTE 1 – DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating the rectifier at reverse voltages above 0.1 $V_{R(rated)}$. Proper derating may be accomplished by use of equation (1).

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where $T_{A(max)}$ = Maximum allowable ambient temperature
$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest)
$P_{F(AV)}$ = Average forward power dissipation
$P_{R(AV)}$ = Average reverse power dissipation
$R_{\theta JA}$ = Junction-to-ambient thermal resistance

Figures 1, 2, and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2).

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2, and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2, and 3 is based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design, that is:

$$V_{R(equiv)} = V_{(FM)} \times F \quad (4)$$

The factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

EXAMPLE: Find $T_{A(max)}$ for 1N5821 operated in a 12-volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 2.0 A ($I_{F(AV)}$ = 1.0 A), $I_{(FM)}/I_{(AV)}$ = 10, Input Voltage = 10 $V_{(rms)}$, $R_{\theta JA}$ = 40°C/W.

Step 1 Find $V_{R(equiv)}$. Read F = 0.86 from Table 1,
$\therefore V_{R(equiv)} = (1.41)(10)(0.86) = 9.2$ V.

Step 2. Find T_R from Figure 2. Read T_R = 105°C
@ V_R = 9.2 V and $R_{\theta JA}$ = 40°C/W

Step 3 Find $P_{F(AV)}$ from Figure 6 **Read $P_{F(AV)}$ = 0.86 W
@ $\frac{I_{(FM)}}{I_{(AV)}}$ = 10 and $I_{F(AV)}$ = 1.0 A.

Step 4 Find $T_{A(max)}$ from equation (3)
$T_{A(max)}$ = 105 − (0.86)(40) = 74°C.

**Values given are for the 1N5821. Power is slightly lower for the 1N5820 because of its lower forward voltage, and higher for the 1N5822. Variations will be similar for the MBR-prefix devices, using $P_{F(AV)}$ from Figure 7.

TABLE 1 – VALUES FOR FACTOR F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.2	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

*Note that $V_{R(PK)} \approx 2.0\ V_{in(PK)}$. †Use line to center tap voltage for V_{in}.

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE
1N5820/MBR320P

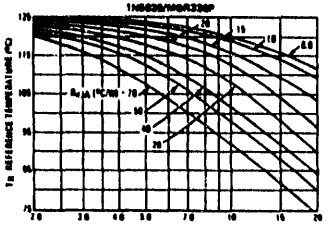


FIGURE 2 – MAXIMUM REFERENCE TEMPERATURE
1N5821/MBR330P

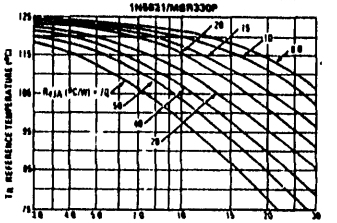


FIGURE 3 – MAXIMUM REFERENCE TEMPERATURE
1N5822/MBR340P

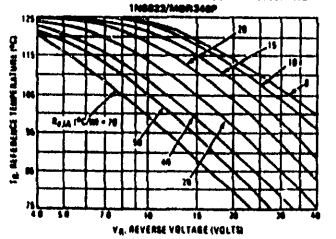


FIGURE 4 – STEADY STATE THERMAL RESISTANCE

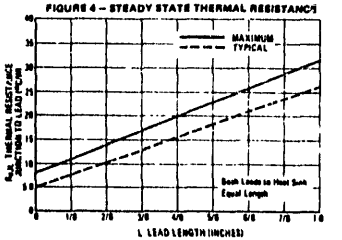


FIGURE 5 – THERMAL RESPONSE

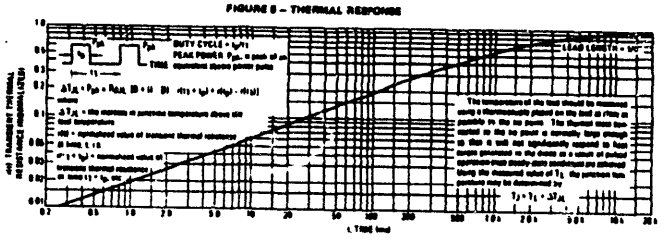


FIGURE 6 – FORWARD POWER DISSIPATION
1N5820-22

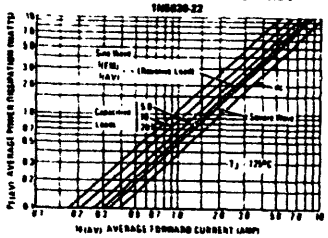
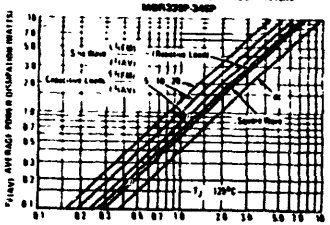


FIGURE 7 – FORWARD POWER DISSIPATION
MBR320P-340P



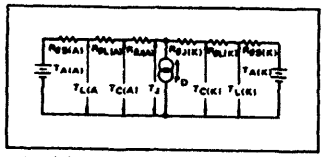
NOTE 2 – MOUNTING DATA

Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

Mounting Method	Lead Length, L (in)				
	1/8	1/4	1/2	3/4	
1	52	57	67	80	°C/W
2	65	70	81	92	°C/W
3		35			°C/W

NOTE 3 – APPROXIMATE THERMAL CIRCUIT MODEL



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heat sink. Terms in the model signify:

T_A = Ambient Temperature
T_C = Case Temperature
T_L = Lead Temperature
T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heat Sink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heat Sink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Total Power Dissipation = $P_F + P_R$
P_F = Forward Power Dissipation
P_R = Reverse Power Dissipation
(Subscripts (A) and (K) refer to anode and cathode sides, respectively.) Values for thermal resistance components are:
$R_{\theta L}$ = 42°C/W/in typically and 68°C/W/in maximum
$R_{\theta J}$ = 10°C/W typically and 16°C/W maximum

The maximum lead temperature may be found as follows:

$$T_L = T_{J(max)} - \Delta T_{JL}$$

where $\Delta T_{JL} = R_{\theta JL} \cdot P_D$

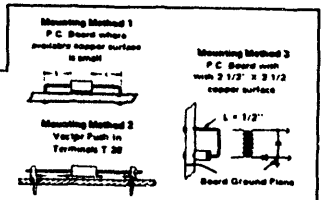


FIGURE 8 – TYPICAL FORWARD VOLTAGE

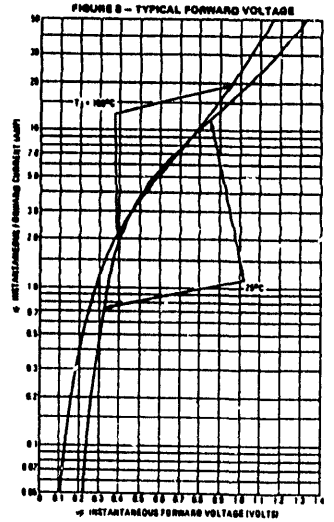


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

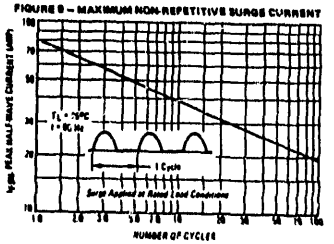


FIGURE 10 – TYPICAL REVERSE CURRENT

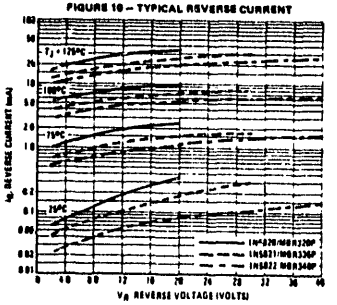
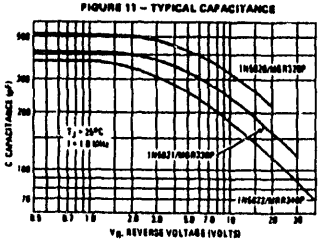


FIGURE 11 – TYPICAL CAPACITANCE



NOTE 4 – HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 11.)

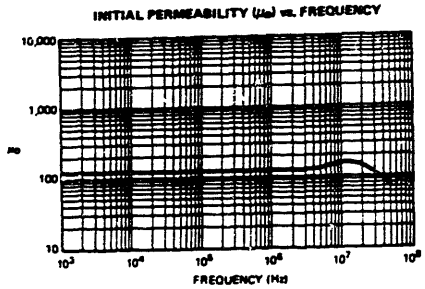
4C4 FERRITE

4C4 MATERIAL

This Nickel Zinc ferrite was developed for filter coil applications for the 1 to 20 MHz frequency range. Also a suitable material for high-frequency wide-band and pulse transformers.

Available in:
POT CORES
TOROIDS

INITIAL PERMEABILITY (μ_o) vs. FREQUENCY



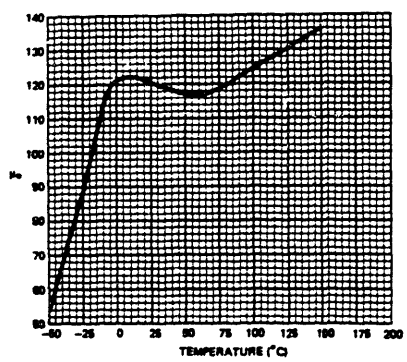
4C4 CHARACTERISTICS

Parameters shown are typical values, based upon measurements of a 1" toroid.

Initial Permeability at 25°C	μ_o	125 (±20%)
Saturation Flux Density at 25°C, H = 10 oersteds	B_s	3000 gauss*
Coercive Force	H_c	3.0 oersted*
Loss Factor at B ≤ 1 gauss	$\frac{\tan\delta}{\mu_o}$	
100 KHz		35×10^{-6} *
500 KHz		35×10^{-6} *
1 MHz		$\leq 40 \times 10^{-6}$
5 MHz		$\leq 80 \times 10^{-6}$
10 MHz		$\leq 100 \times 10^{-6}$
Temperature Factor (+5° to +55°C)	TF	-8.0×10^{-6} MIN. $+8.0 \times 10^{-6}$ MAX.
Disaccommodation Factor (10-100 minutes)	DF	$< 15 \times 10^{-6}$
Curie Temperature	T_c	≥300°C

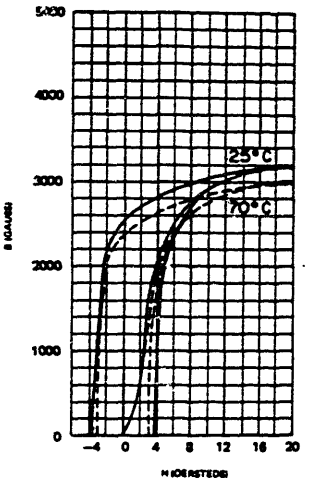
*Typical values

INITIAL PERMEABILITY (μ_o) vs. TEMPERATURE

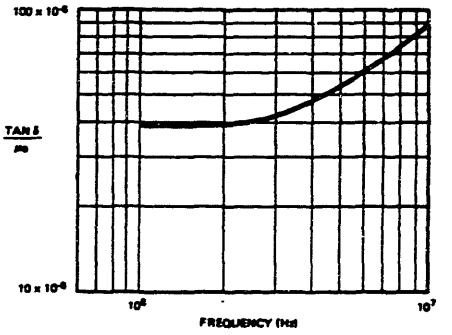


4C4 FERRITE
CHARACTERISTIC CURVES

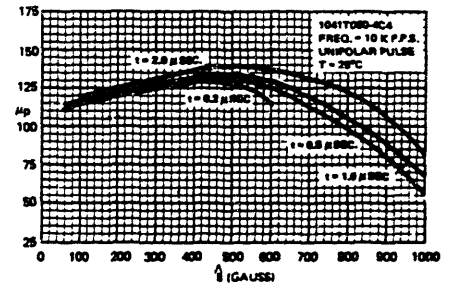
HYSTERESIS CURVE

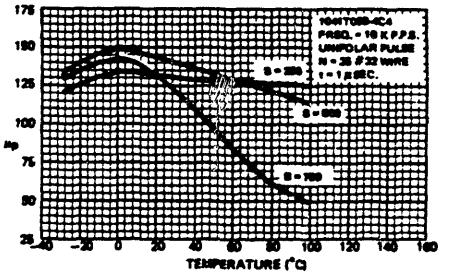


LOSS FACTOR ($\frac{TAN\ \delta}{\mu_p}$) vs. FREQUENCY



PULSE CHARACTERISTICS





SERIES 1811 POT CORES

1 This core type is

- manufactured in the following ferrite materials:
  3B7 3B9 3C8 3D3 3E2A 4C4
- available in the following types:
  ungapped; fixed gap; adjustable gap.
  (3E2A ferrite available only in ungapped type.)
- available with the following optional accessories:
  Single, Dual, and Triple-Section Standard Bobbins; and Printed Circuit Bobbins. Styles H, H1, H2, HD and HPC Hardware.

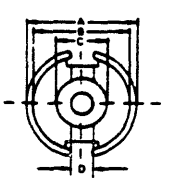
2 Electrical parameters are expressed in the MKS System.

3 All terms and symbols used are defined in the Glossary at the rear of the catalog.

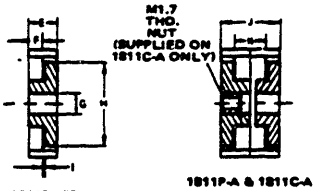
4 Characteristics of the ferrite materials used are described in the Materials section at the front of the catalog.

ACTUAL SIZE

MECHANICAL CHARACTERISTICS & DIMENSIONS



1811P-L00



1811P-A & 1811C-A

MECHANICAL CHARACTERISTICS

NOTE: Values given apply to a core set.

MAGNETIC PATH LENGTH	ℓ_e	1.02 in. 2.59 CM
CORE CONSTANT	$\frac{\Sigma \ell_e}{A_e}$	15.22 in.$^{-1}$ 5.91 CM^{-1}
EFFECTIVE CORE AREA	A_e	.067 in.^{2} .433 CM^2
EFFECTIVE CORE VOLUME	V_e	.068 in.^{3} 1.12 CM^3
WEIGHT		.226 oz. 6.4 Grams

NOTE: MINIMUM CORE AREA .337 CM^2

POT CORE DIMENSIONS

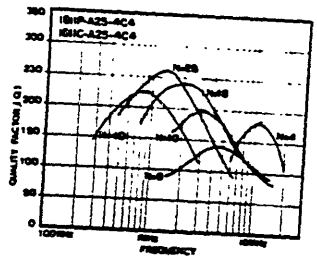
All dimensions are in inches.

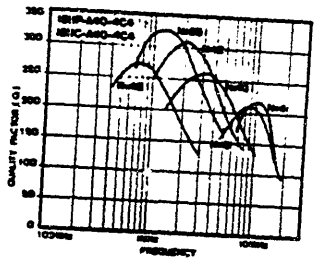
	MINIMUM	MAXIMUM		MINIMUM	MAXIMUM
A	.693	.717	G	.118	.126
B	.386	.606	H	.516	.540
C	.257	.299	I	.015	.025
D	.126	.174	J	.410	.422
E	.206	.211	K	.284	.300
F	.142	.150			

PERFORMANCE CURVES

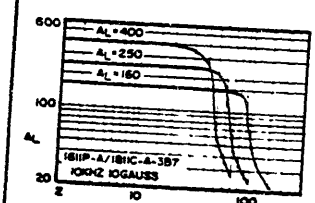
Q vs. FREQUENCY

4C4

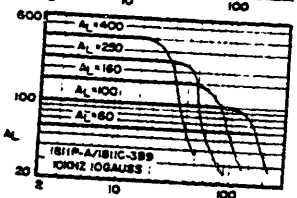




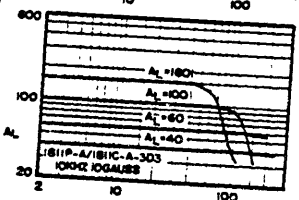
A_L vs. BIAS



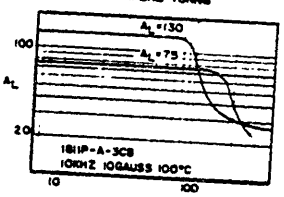
3B7



3B9



3D3



3C8

WINDING INFORMATION FOR Q CURVES

TYPICAL FULL-BOBBIN WINDINGS	
TURNS	WIRE
4*	18
6*	80/46
10*	80/46
16*	80/46
25*	80/46
25**	80/46
40	80/46
63	80/44
100	30/44
160	19/46
250	7/44
250	32
400	34
630	36
1000	38

*4C4 only.
**3D3 only.

ELECTRICAL CHARACTERISTICS

UNGAPPED POT CORES

CORE PART NUMBER*	CORE MATERIAL	A_L† (mH PER 1000 TURNS) (±25%)	μ_e† (REF.)
1811P-L00-3E2A	3E2A	7500	3570
1811P-L00-3C8	3C8	4000	1930
1811P-L00-387	387	3680	1740
1811P-L00-389	389	2630	1250
1811P-L00-3D3	3D3	1550	735
1811P-L00-4C4	4C4	265	125

*Part number for a core half. †Per pair of cores.

GAPPED POT CORES

• NON-ADJUSTABLE GAPPED POT CORE PART NO.	•• ADJUSTABLE-GAP POT CORE ASSEMBLY PART NO.	CORE MATERIAL	A_L† VALUE	μ_e (REF.)	APPROX. GAP LENGTH (IN.)	TEMPERATURE COEFFICIENT PPM/°C	
						MIN-MAX	TEMP. RANGE
1811P-A160-387	1811C-A160-387 White Adjustor	387 (To 300 KHz)	160 ±1.5%	76	.013	−46 to +46	+20° to +70°C
1811P-A250-387	1811C-A250-387 Brown Adjustor		250 ±2%	119	.0075	−71 to +71	
1811P-A400-387	1811C-A400-387 Gray Adjustor		400 ±3%	190	.004	−114 to +114	
1811P-A60-389	1811C-A60-389 Red Adjustor	389 (To 300 KHz)	60 ±1%	28	.047	+25 to +53	−30° to +70°C
1811P-A100-389	1811C-A100-389 Yellow Adjustor		100 ±1%	46	.024	+41 to +87	
1811P-A160-389	1811C-A160-389 White Adjustor		160 ±1.5%	76	.013	+68 to +144	
1811P-A250-389	1811C-A250-3C9 Brown Adjustor		250 ±2%	119	.0075	+107 to +226	
1811P-A400-389	1811C-A400-389 Gray Adjustor		400 ±3%	190	.004	+171 to +361	
1811P-A40-3D3	1811C-A40-3D3 Green Adjustor	3D3 (200 KHz to 2.5 MHz)	40 ±1%	19	.080	+19 to +67	
1811P-A60-3D3	1811C-A60-3D3 Red Adjustor		60 ±1%	28	.047	+28 to +361	
1811P-A100-3D3	1811C-A100-3D3 Yellow Adjustor		100 ±1%	46	.024	+46 to +138	
1811P-A160-3D3	1811C-A160-3D3 White Adjustor		160 ±1.5%	76	.013	+76 to +288	
1811P-A25-4C4	1811C-A25-4C4 Red Adjustor	4C4 (1 MHz to 20 MHz)	25 ±1%	12	.140	−72 to +72	+5° to +55°C
1811P-A40-4C4	1811C-A40-4C4 Green Adjustor		40 ±1%	19	.080	−114 to +114	

*Part number is for a core set (2 cores). **Part number is for a core set (2 cores), nut, and specified adjustor.
†The A_L values are based on a fully wound bobbin without adjustor: mH/1000 turns. See later page for partial bobbin winding.

GAPPED POT CORES FOR POWER APPLICATIONS

• NON-ADJUSTABLE GAPPED POT CORE PART NO.	CORE MATERIAL	A_L† VALUE	μ_e (REF.)	APPROX. GAP LENGTH (IN.)
1811PA75-3C8	3C8	75 ± 3%	36	037
1811PA130-3C8		130 ± 3%	62	018

*Part number is for a core set (2 cores)
†The A_L values are based on fully wound bobbin, mH/1000 turns.
See later page for partial bobbin winding.

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