Characterization and Modeling of Pattern Dependencies in Copper Interconnects for Integrated Circuits

by

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S.B., Electrical Engineering and Computer Science, MIT, 1998
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Abstract

Copper metallization has emerged as the leading interconnect technology for deep sub-micron features, where electroplating and chemical mechanical polish (CMP) processes have a vital role in the fabrication of integrated circuits. The processes both suffer from a similar problem: the copper electroplated profiles and the polished surface exhibit pattern dependent topography. In this thesis, a methodology for the characterization and modeling of pattern dependent problems in copper interconnect topography is developed. For the electroplating process, the methodology consists of test structure and mask design to examine feature scale copper step height and the height of copper array regions as a function of underlying layout parameters. Semi-empirical response surface models are then generated with model parameters extracted from conventional and superfill plating processes. Once the models are calibrated, layout parameters including pattern density, line width distributions, and line length are extracted for each cell in a 40 μm by 40 μm discretization of any random chip layout. Then, a chip-scale prediction is achieved by simulating generalized average heights for each grid cell across the entire chip. The prediction result shows root mean square errors of less than 1000 Å for array height and around 500 Å for step height. This methodology provides the first known chip-scale prediction of electroplated topography.

For pattern dependencies in copper CMP, this thesis focuses on the development of test structures and masks (including multi-level structures) to identify key pattern effects in both single-level and multi-level polishing. Especially for the multi-level studies, electrical test structures and measurements in addition to surface profile scans are seen to be important in accurately determining thickness variations. The developed test vehicle and characterization of copper dishing and oxide erosion serve as a basis for further pattern dependent model development. Finally, integration of electroplating and CMP chip-scale models is illustrated; the simulated step and array heights as well as topography pattern density are used as an input for the initial starting topography for CMP simulation of subsequent polishing profile evolution.

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Chapter 1

Introduction

With ever-decreasing dimensions and ever-increasing complexity of layout patterns in integrated circuits (IC), semiconductor manufacturing is continually faced with great challenges and difficulties. Over the years, tighter constraints have been imposed on process margins and specifications, and this kind of limitation on process window is projected to be even more severe for later generations of chips [1]. Furthermore, introduction of new materials such as copper and low dielectric constant films for back-end interconnects creates even greater challenges in terms of development of new processes and integration of different materials.

Copper metallization, which has replaced traditional aluminum technology for the state-of-the-art IC's, is expected to have ten levels of metal with as small as 50 Å of copper thickness loss for minimum feature arrays and less than 150 Å of wide copper line loss by year 2010. This is a challenging future requirement for the current chemical mechanical polish (CMP) process, especially when current planarization technology often exceeds 1000 Å of copper loss in dense regions. The constraint on copper planarization is made more difficult by the incoming topography variation from copper electroplating where large bulge or recess may be present depending on the size of feature arrays, as this incoming topography variation is known to impact CMP performance directly by causing varying removal rates of copper on different pattern regions [2].

The Semiconductor Industry Association (SIA) roadmap calls for a full CMP model in near future with 10% topography accuracy of specification limits. Thus, it is critical to have a systematic methodology for the characterization and modeling of pattern dependent issues and problems in both copper electroplating and subsequent CMP processes, and

this is the focus of this thesis work. The research presented here enables rapid and effective development and optimization of each process, and the modeling work for chip-scale topography prediction capability also enables development of relevant layout design rules to limit topography variations.

This chapter is organized into five sections. An overview of copper metallization is given in Section 1.1 with a review of the damascene process used for copper metallization. In Section 1.2, the principles and mechanisms of the electroplating and CMP processes for copper metallization are described. Then, key pattern dependent problems and issues are examined in Section 1.3. Finally, the goal of this thesis is described in Section 1.4, and the thesis organization is given in Section 1.5.

1.1 Introduction to Copper Metallization

Aluminum has enjoyed over three decades usage as the preferred choice of interconnect in integrated circuits. However, due to performance and process limitations of aluminum metallization (e.g. inherent resistivity, electromigration limitations, and increasing challenge to etch very fine aluminum lines), copper metallization has emerged as the leading interconnect technology for deep sub-micron features. Unlike traditional metallization, where aluminum is deposited on top of inter-level dielectric (ILD), patterned, and etched, copper metallization uses a damascene process. In a damascene process as shown in Figure 1.1, ILD is first deposited and patterned to define "trenches" where the metal lines will lie. Then, a thin layer of barrier material (e.g. tantalum or tantalum nitride with thickness of around 200 Å) is deposited typically using a physical vapor deposition (PVD) process on the entire surface to act as a barrier since copper can readily diffuse into silicon and destroy devices. After the deposition of the barrier layer, a copper seed layer (around 1000 Å thick) is deposited, which serves as a base for the subsequent deposition of copper

using electroplating. Once the patterned trenches and field regions are filled with copper as shown in step 5 in Figure 1.1, the CMP process is used to remove the excess metal outside the desired lines.

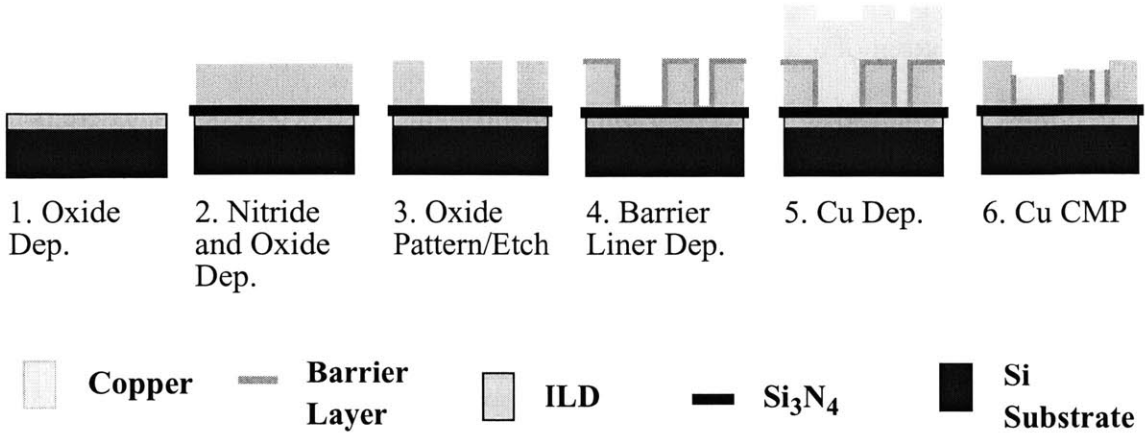


Figure 1.1: Copper Metallization: Damascene Process

As illustrated above, the copper metallization process involves many integrated processing steps, and two of the key enabling technologies are copper deposition by electroplating and copper removal/planarization by CMP. The underlying barrier material must have strong adhesion to the dielectric material and continuos step coverage across deep trenches with good electrical and electromigration performance. Furthermore, the copper seed layer, which is typically deposited by a PVD process, must be also continuous with high step coverage for adequate sidewall and bottom fills, especially for high aspect ratio trenches.

Once a wafer is coated with the copper seed layer, bulk copper is deposited by electroplating. Many techniques exist for the deposition of copper material on patterned wafers [3]; however, electroplating, which is the same technology used for printed circuit board (PCB) metallization, has become the widely accepted choice for copper deposition [4].

One of the key driving forces for the adoption of electroplating for copper deposition is that this technique enables void-free fills in narrow trenches which is a key requirement for sub-micron feature sizes and high aspect ratios. This void-free fill is often achieved with added chemistries in the copper plating solution so that a higher deposition rate occurs on the bottom of a trench, thus avoiding voids in trenches. Once copper is deposited, it must be removed so that copper only remains in the designed trenches. There is no viable solution for plasma etching of copper, and industry has adopted CMP for copper removal and planarization of the damascene structures.

CMP has emerged as the leading planarization technique in silicon integrated circuit fabrication processes and has been extensively applied for planarization requirements of back-end interlayer dielectrics (ILD) as well as for the front-end shallow trench isolation (STI) process. While other planarization techniques exist, such as spin-on-glass with etch back or other novel deposition and processing, CMP satisfies both the local and global planarity requirements, imposed by lithography depth-of-focus limitations and integration issues for current silicon technologies [5]. In addition, current CMP applications also include polishing of metals such as tungsten [6] and other novel materials which are currently under active research [7, 8]. Finally, CMP has been a key enabler for copper interconnects; one of the first commercial fabrication processes to use copper is pictured in Figure 1.2 [9].

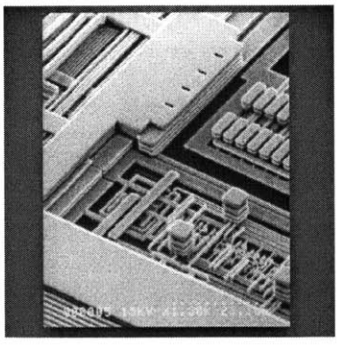


Figure 1.2: Copper Interconnect (6 Levels, Source: IBM)

1.2 Review of Electroplating and CMP: Principles and Mechanisms

We begin with a brief review of the principles and mechanisms in copper electroplating and CMP. In Section 1.3, we then discuss in more detail a key challenge in the processes related to pattern dependencies. A schematic view of the electroplating tool is shown in Figure 1.3. A wafer surface coated with a thin electrically continuos layer of copper (the seed layer) is immersed in a solution containing copper ions, and the wafer surface is electrically connected to an external power source. Deposition of copper onto the wafer surface occurs by copper ions reacting with electrons to form copper at the wafer surface when current is passed through. The following equation describes the chemical reaction mechanism on the wafer surface which acts as a cathode where cupric ions are reduced to copper atoms.

$$Cu^{2+} + 2e^{-} \rightarrow Cu(O) \tag{1.1}$$

The depleted cupric ions in the solution are replenished by the anode which is another active electrical surface in the electroplating system that completes the electrical circuit. The anode, where an oxidation reaction occurs that balances the current flow in the system, is composed of a bulk copper material.

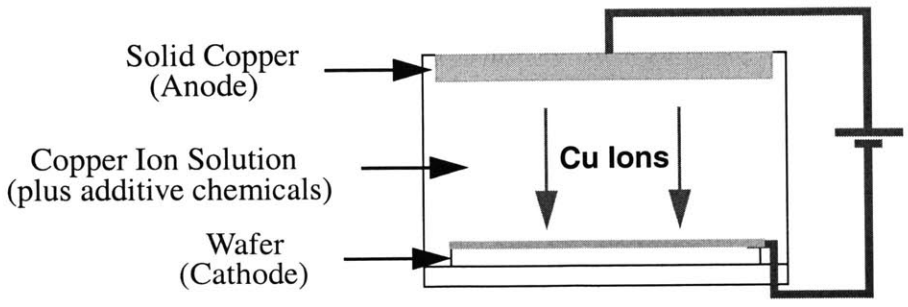


Figure 1.3: Basic Mechanism of Copper Electroplating

The basic governing principle of deposition is Faraday's law of electrolysis which relates the amount of copper deposited to current density [9]. However, this mechanism is complicated by added chemistry in the copper solution. Typically, these added chemicals are called suppressors and accelerators that are designed to suppress the deposition rate on raised regions while accelerating the deposition rate on the bottom of trenches to achieve void-free fills [10, 11, 12]; such electroplating processes are referred to as bottom-up fill or superfill.

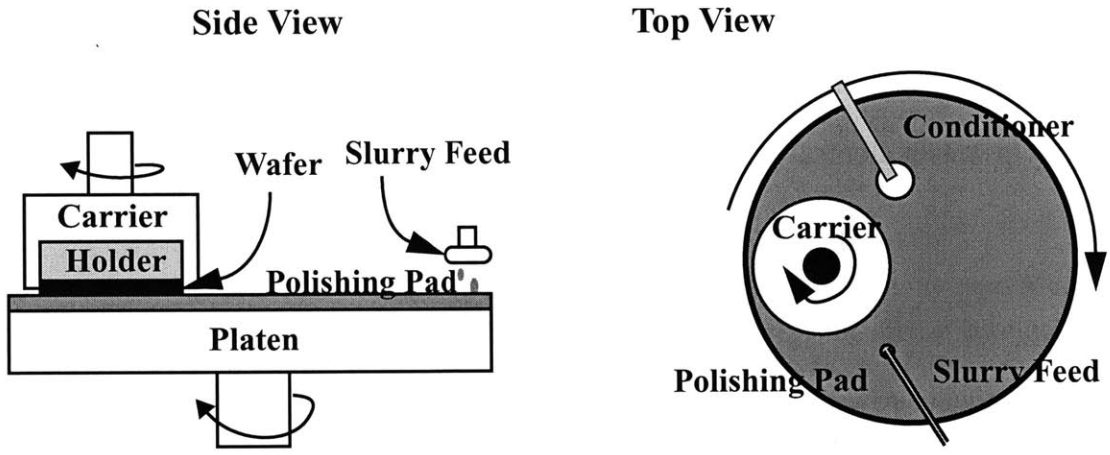


Figure 1.4: CMP Machine

A schematic view of a CMP machine is shown in Figure 1.4. A wafer is held on a carrier typically with a back pressure with the surface to be polished facing down towards a polishing pad. A retainer ring on the outer edge of the carrier head prevents the wafer from slipping out of the carrier during polishing. The wafer is then pressed onto a porous polyurethane polishing pad that is attached to a platen. Both the wafer carrier and the platen are rotated, typically in the same direction with the carrier also having a lapping motion across the pad, and slurry composed of suspended particles in a chemical solution is delivered to

the polishing platform. The removal mechanism has two parts. First, the slurry chemically reacts with the wafer surface film to enhance or inhibit removal of particular materials. Second, mechanical abrasion from the relative movements and pressure of pad and wafer with the slurry particles results in the removal of material [13]. Over time, the pad surface becomes glazed and the removal rate decreases resulting in poor polishing performance. In order to keep the integrity of the pad surface and maintain a reliable polish rate, a conditioning head typically with a diamond tip is used to refresh the surface of the pad to maintain the surface characteristics. Other variants of this rotating platform exist such as linear polishing machines, orbital machines, or machines in which the wafer is facing up with a small (smaller than the size of the wafer) polishing pad facing down on a wafer; in all of these tools the basic polishing mechanisms are similar [14].

1.3 Key Problems in Electroplating and CMP

Due to the layout patterns of the underlying trenches to be filled, non-uniform topography exists after electroplating. The resulting topography can be characterized by two height parameters: a feature scale step height (SH) and an array height (AH) — either recess or bulge — as shown in Figure 1.5 for a superfill electroplating. SH is defined as the height associated with each copper line where copper may stick up or recess depending on the feature size, and the AH is measured from the top of the raised features in an array to the flat copper field region over wide oxide. The magnitude of bulge or recess and step heights are dependent on feature sizes including both line width and space. For large features, conformal plating is observed, indicating that there is no impact on large features from the added chemistries to cause superfill. However, for fine arrays of lines, copper is filled above the field level nearby, and for large lines with fine spaces, a recess may be present in the copper surface topography. Also, it is possible to have copper sticking up

above a trench when the trenches are narrow and spaces are large. The step and array height trends will be thoroughly examined in Chapter 4.

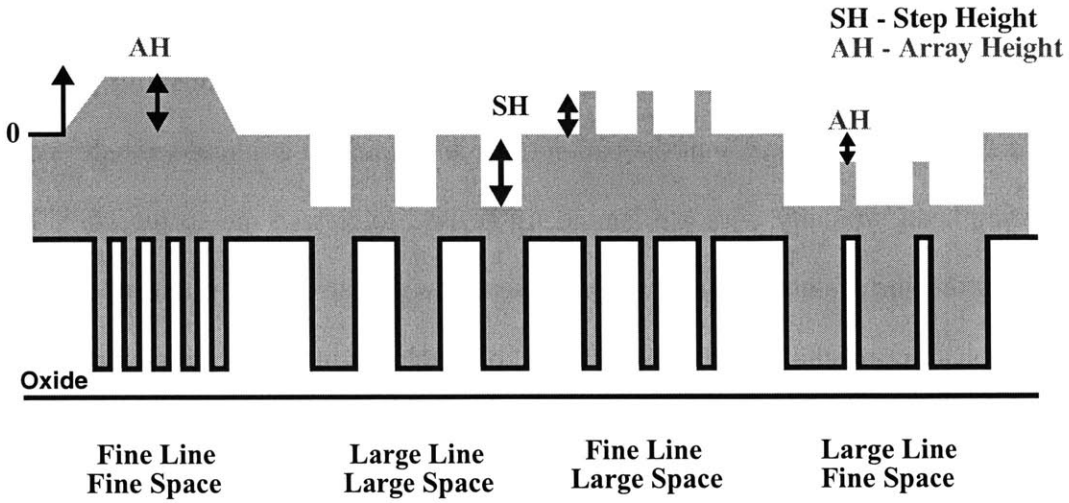


Figure 1.5: Non-Uniform Topography in Copper Electroplating (Superfill)

Once a wafer is deposited with copper which exhibits these non-uniform thickness variations, the next step is the CMP process. A copper CMP process is best viewed as having three intrinsic stages [15]. Stage 1 is the removal of bulk copper on top of a barrier layer, and stage 2 is the removal of the barrier layer. In stage 1, we have homogenous (single material) polishing where the copper removal rate on different parts of a die is influenced by the as-plated initial copper topography created by layout patterns and plating characteristics. For example, Figure 1.6 shows two sample regions: a fine array region and a large pitch region. The fine array region has a bulge and polishes roughly at a blanket copper polish rate. Thus, it achieves a relatively flat surface in that local region later than in the large pitch region where raised features with a 50% pattern density see an accelerated copper removal rate compared to the blanket rate. Due to the initial topography, there are differences in removal rates across a die, and thus different parts of a die complete the

removal of excess copper overburden and expose the underlying barrier layer at different polish times. Continued polish beyond barrier removal or overpolish phase is the third intrinsic stage, where additional differential polish rates occur to due material removal selectivity.

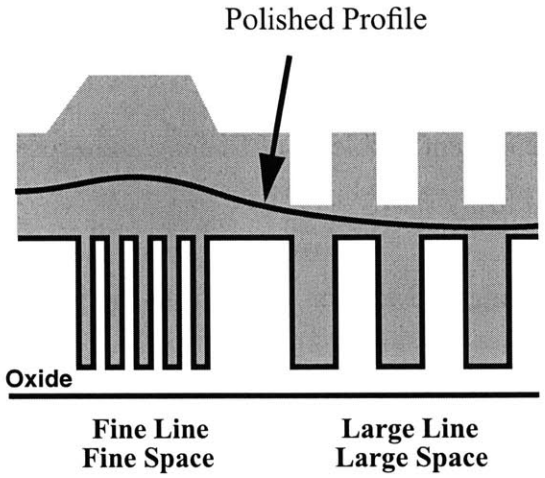


Figure 1.6: Initial Copper Profile and Influence on Copper Removal

Ideally, the polished copper wafer surface should be perfectly flat; unfortunately, an important non-ideality is that copper lines suffer from dishing and erosion due to CMP. Figure 1.7 shows a cross sectional schematic view of a realistic case suffering from dishing and erosion. Dishing is defined as the recessed height of a copper line compared to the neighboring oxide, erosion is defined as the difference between the neighboring field region and the post-polish oxide height, and field oxide loss is defined as the difference between the original oxide thickness and the post-polish oxide thickness in wide field area as illustrated.

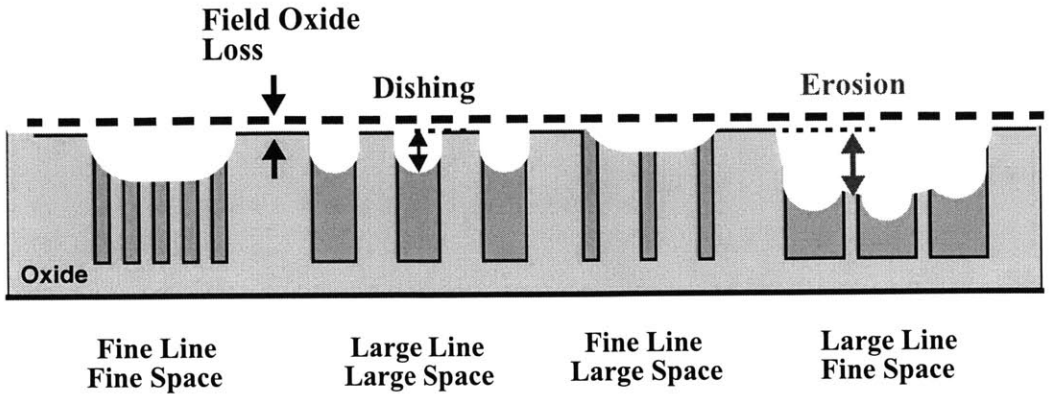


Figure 1.7: Pattern Dependent Problems of Dishing and Erosion In Copper CMP.

These problems of dishing and erosion come from the inherent overpolish stage in copper CMP, and the degree of overpolish depends on two components. First, due to the initial non-uniform topography, there are differences in bulk copper removal rates and thus different regions have different clearing times to the underlying barrier layer. Thus, using the example illustrated above, the region with fine arrays which starts out with a bulge would see a slower clearing time exposing the barrier layer later and thus receive less overpolish. This will result in decreased dishing and erosion for that structure. The second component that adds to the total degree of non-uniformity is the fact that during the barrier and overpolish, we are again polishing pattern regions created by copper trenches and oxide spacings. Thus, these regions will now again see differences in removal rates of copper and oxide and cause added dishing or erosion on top of what is already caused by the differences in clearing time due to the initial copper topography. Thus, the plated topography strongly affects CMP performance, and it is important that we develop an integrated methodology for understanding these pattern dependent issues of both electroplating and CMP.

Beyond the non-uniformity problems in single-layer CMP processes, we must also consider multi-level copper metallization and its non-uniform topography and thickness variation. Figure 1.8 illustrates the processing sequence of multi-level copper metallization in a schematic format (excluding the via layer for the sake of simplicity). (1) After metal 1 polish, there is a certain amount of oxide recess across a structure region. (2) Because of this starting recess on the metal 1 layer, conformally deposited metal 2 oxide has a similar recess shape as the metal 1 recess. (3) The pattern and etch of the uneven oxide makes the bottom of the copper trenches uneven, and the copper deposition profile is also influenced by the uneven profile shape in addition to any non-uniform depositions from electroplating itself. (4) After copper deposition, the wafer is planarized by CMP.

What we are interested in are the metal 2 recess and the remaining line thickness in both an overlap region and non-overlap region, and understanding how these are affected by the propagation of non-uniform topography created in the lower level. The topography non-uniformity in the polished metal 2 surface exhibits the similar dishing and erosion problems seen in a single-level polish. However, different degrees of erosion, for example, exist for an uniform array of lines depending on whether a portion of it lies over already-recessed metal 1 region since that region would see higher amounts of recess due to its recessed level even before metal 2 CMP. Another problem in multi-level polishing is that the topography map, often gathered using a surface profiler does not give a complete picture of thickness variation. We have found that electrical measurements of the copper thickness and surface scans are an effective complementary approach to fully characterize multi-level polish behaviors.

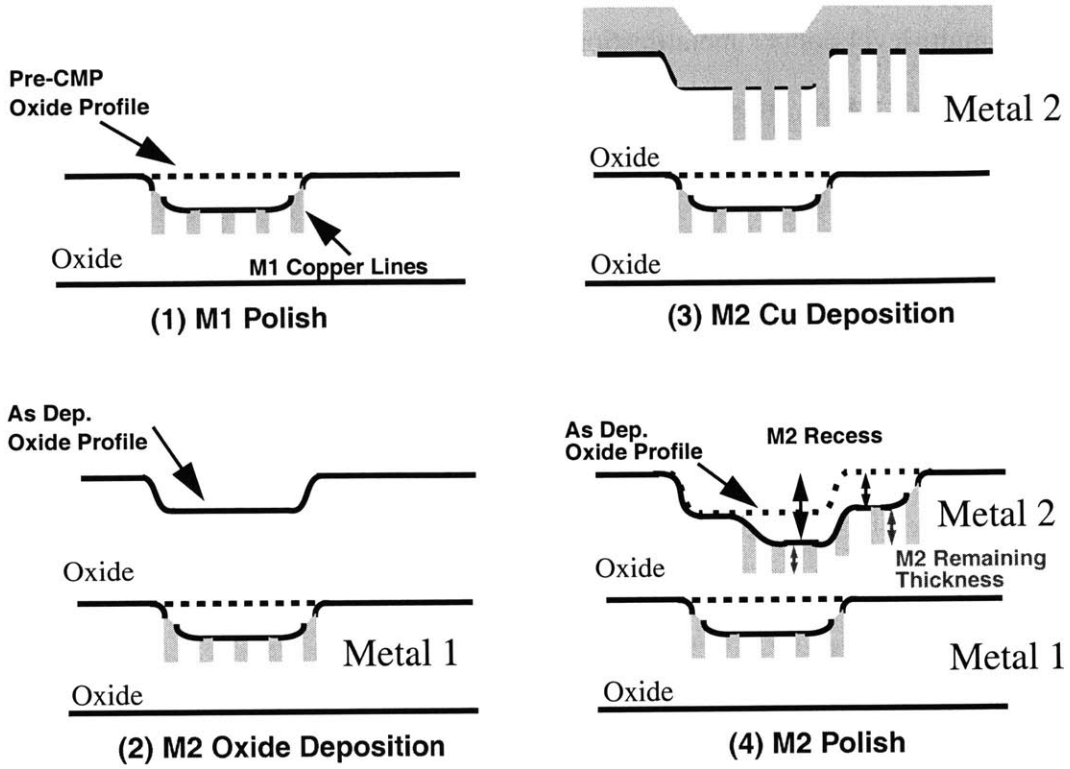


Figure 1.8: Multi-Level Process Sequence

These problems of copper thickness variation due to copper dishing, oxide erosion, and field loss are major challenges in advanced copper metallization processes. Such problems can affect chip performance by introducing variable differences in resistance and capacitance depending on line locations within a chip, and the different amount of dishing and erosion also leads to considerable surface non-planarity with consequent manufacturability and process integration difficulties. These problems are seen to largely depend on underlying layout patterns such as pattern density or pattern pitch. Understanding the initial as-plated topography pattern dependencies is a critical first step for modeling of integrated deposition and polish results.

1.4 Thesis Goals

Copper metallization is becoming a main stream process with tight constraints on thickness variations after CMP. The complexity of copper planarization is increased by the incoming topography variation from copper electroplating where large bulge or recess may be present depending on the underlying features. Thus, it is critical to have a systematic methodology for the characterization of pattern dependent issues and problems in both copper electroplating and CMP. This characterization methodology must also be coupled to a model that captures these pattern effects for prediction of plating and CMP results for arbitrary product patterns.

The basis of the methodology includes identifying key layout and process parameters that cause variations in electroplated step heights and CMP dishing/erosion. The identification of the key pattern dependent factor is possible by design of test structures that consist of various pattern factors combining a wide range of line widths and spaces. The design of the test structures is also closely tied with measurement and analysis techniques so that we can effectively capture these dependencies.

Using the same test mask as the vehicle of characterization for both electroplating and CMP, we can study and understand pattern dependent behaviors in each process and furthermore understand how the electroplated topography affects the CMP process. As described earlier, different array heights are possible for an electroplated die depending on the size of features and spacings, and thickness variations of dishing and erosion are present after CMP due to layout patterns. Based on the trends of these non-uniformities, a pattern dependent model can be formulated. With characterization and model formulation, one can understand the fundamental limitations of these thickness variations for a specific process.

In addition to experimentally inducing and characterizing pattern dependent thickness variations, a model is needed capable of predicting thickness variations across an entire chip by relating layout parameters such as pattern density and line width with calibrated model coefficients. Thus, a layout parameter extraction algorithm needs to be developed so that an extracted layout result can be efficiently used with the model in predicting chip-level variations. Furthermore, when chip-scale prediction is possible based on layout parameters, relevant layout design rules can be generated to limit thickness variations after the copper electroplating and CMP process.

In summary, the main goals and objectives of this thesis are as follows:

1. Develop test structures and masks to explore key pattern effects in both electroplating and CMP processes.
2. Characterize pattern dependent problems in electroplating as a function of underlying pattern features and develop a model to capture the variation.
3. Develop layout parameter extraction procedures and apply the electroplating model in chip-scale simulation and prediction for arbitrary layouts.
4. Characterize both single level and multi-level CMP pattern dependent effects as a function of underlying pattern features.
5. Illustrate the integration of electroplating topography prediction and CMP modeling for predictive chip-scale simulation of final interconnect topography.

1.5 Thesis Organization

This thesis is organized into seven chapters. Chapter 2 outlines the overall methodology for both electroplating and CMP characterization and modeling and highlights different parts of the overall method with an emphasis on how they integrate to form a coherent methodology for characterizing and modeling interconnect topography.

Once the overall methodology is presented, the subsequent chapters discuss in detail each part of the methodology. Chapter 3 covers the test structure and mask design which is

the key first step in experimentally exploring pattern dependencies in a process. Design issues and structure descriptions are presented for a single-level mask. Then, a multi-level mask description is given to study polishing effects in multi-level interconnect processes. In Chapter 4, electroplating characterization is presented and followed by modeling of electroplated non-uniform surface topography. Trends are observed and various proposed physical and superfill mechanisms are examined to formulate model variables. Then, Chapter 5 describes layout parameter extraction and chip-scale simulation using the developed model, and a chip-scale plating prediction result is presented.

Understanding of pattern dependent electroplating non-uniformity is essential for the subsequent CMP process since the initial topography directly impacts the planarization of the CMP process. In Chapter 6, CMP characterization is presented for both single-level and multi-level pattern dependencies. The use of electrical test structures and their analysis are also presented. The ability to gather electrical data, especially for fine lines which are often hard to measure with surface profile tools, is shown to complement surface height measurement. Then, an overview of the pattern dependent CMP model is described followed by the integration of the electroplated topography simulation result and a CMP chip-scale model. Finally, Chapter 7 summarizes the key results and contributions of this thesis and concludes with directions for future research in this area.

Chapter 2

Comprehensive Characterization and Modeling Methodology

Characterization of the pattern dependent non-uniformities in copper electroplating and CMP is needed to understand the fundamental limitations of each process and assist in new process development efforts. For the characterization work to be meaningful and valid, it must be carried out in a systematic and methodical way. This chapter first gives an overall methodology to characterize an electroplating process to understand the plated thickness variations such as step height and array height. The development and application of a pattern dependent electroplating model coupled to the characterization method is presented with an overall goal of chip-scale thickness simulations for any random layouts. Then, a similar methodology is illustrated for the characterization and modeling of the CMP process, with an emphasis on the integration of electroplating and CMP simulations. This chapter is intended to give an overall picture of all the pieces involved in the characterization and modeling work to illustrate how they are interrelated, and the subsequent chapters give details of each individual part of the methodology.

2.1 Electroplating Characterization and Modeling

The overall methodology for electroplating characterization and modeling is summarized in Figure 2.1. To characterize as-plated copper topography variation for a particular electroplating process, a wafer patterned with a dedicated test mask is processed. The test mask consists of various combinations of line widths and line spaces to cover a wide range of pattern densities and features. The designed test patterns are used with measurement and analysis techniques to capture and identify key layout dependencies in the plating pro-

cess. Once a wafer is electroplated, step height and array bulge or recess are measured across many test pattern arrays and isolated features using a surface profiler. Also, field areas (e.g. large region without any copper lines) are measured for the absolute copper thickness so that we can translate relative surface height measurements into absolute thickness throughout the chip. The direct measurement of copper film thickness has become possible due to emerging tools such as the Metapulse system by Rudolph Technologies, or the Impulse 300 system by Philips Analytical.

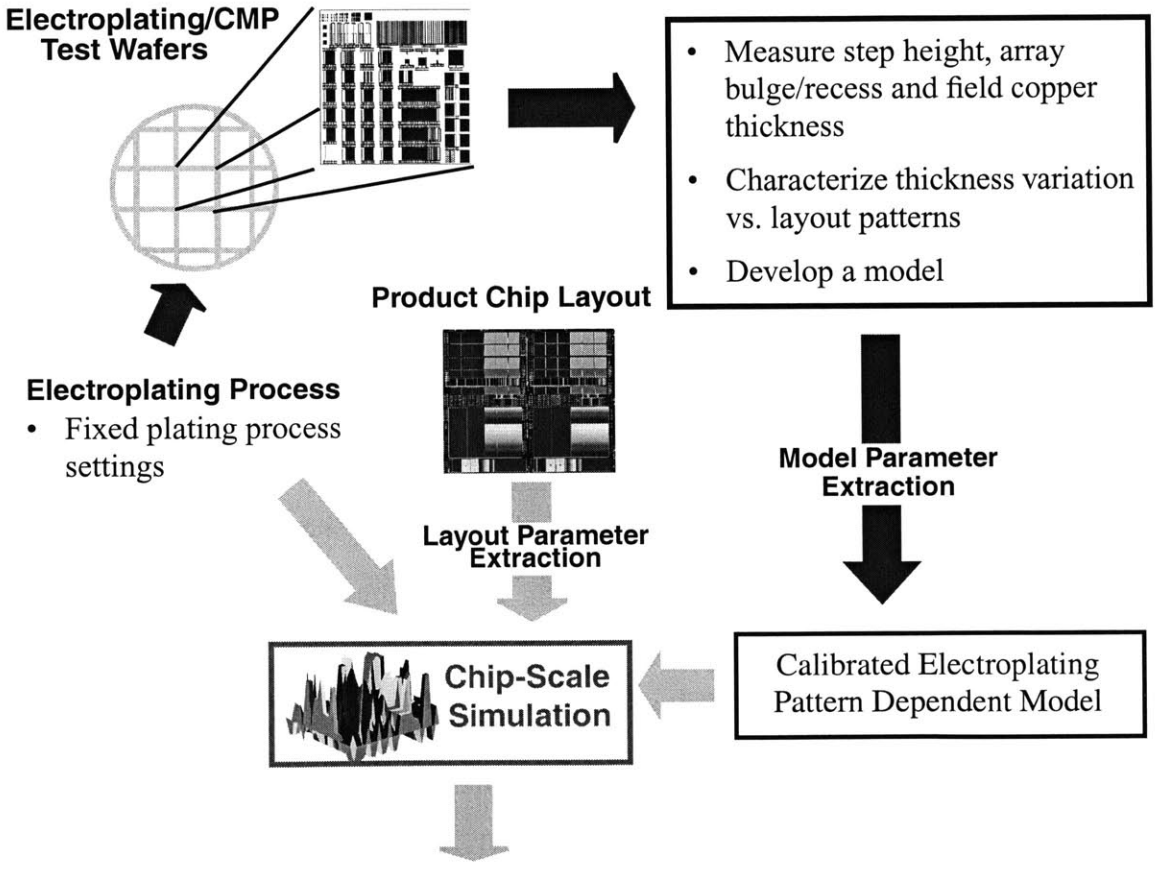


Figure 2.1: Overall Methodology for Characterization and Modeling of Thickness Pattern Dependency in Copper Electroplating

The measured data is analyzed to assess and identify key pattern dependencies, and their trends are examined as a function of specific layout features. This characterization serves as a powerful tool to understand the plating behavior and can help an engineer to identify and resolve any non-uniformity issues before they cause any difficulties in manufacturing or create yield problems. Once a process is fully characterized for its pattern induced thickness profiles, a semi-empirical model is developed incorporating the macrophysics of electroplating; this model captures the key pattern effects as a function of underlying layout patterns. The model can be calibrated for different electroplating recipes.

The model parameters are then extracted, and the calibrated electroplating pattern dependent model can be used to perform chip-scale simulations for the thickness variation for other chips fabricated using the calibrated electroplating process. The chip-scale simulation can be done for any arbitrary layout; to accomplish this, the relevant layout parameters must be extracted before the simulation can be performed. The result of the simulation is step height and array height across an entire chip for the given electroplating process. The simulation result can be used to determine overall non-uniformity as well as to check for any regions on the chip with excess copper bulge or recess. Furthermore, the model-based simulation can be used to develop intelligent design rules for layout patterns: for example, once any possible trouble spots are determined, the layout can be modified to alleviate the problem by inserting dummy fills to equalize the pattern effects.

Detailed descriptions for each part of the methodology, including the test mask design, non-uniformity characterization and model development, chip-scale simulation and prediction, are presented in Chapters 3, 4, and 5, respectively.

2.2 CMP Characterization and Modeling

Characterization and modeling of pattern dependent variations of copper dishing and oxide erosion for CMP process is shown in Figure 2.2 and has similar flow as the method used for electroplating. A patterned wafer deposited with copper is polished using a particular process. Then, dishing of copper lines are measured for isolated lines and array lines, and erosion of oxide is measured for array lines using a surface profiler. In addition to these surface measurements, optical field area measurements of dielectric thickness are done to obtain the absolute remaining film thicknesses at various locations such as at either ends of each surface trace. Also, electrical measurements are performed to gather line resistance, which are later converted to copper thickness for comparisons with the surface profile data and optical dielectric film thickness. This electrical data analysis has been found to be particularly useful for multi-level CMP characterization where surface profile scan does not necessarily indicate the remaining copper thickness profile. It has been found that the use of both surface profiles and electrical measurements is necessary to get a complete picture of the polished thickness/surface variations. All of these measurements are done across various pattern regions to ensure that we have a data set that covers wide range of pattern features.

Based on the characterization of the pattern effects and incorporating polishing fundamentals such as blanket removal rates and material removal selectivities, a semi-empirical pattern dependent CMP model is developed. The calibrated copper CMP model can be used for chip-level simulation of any arbitrary layout (e.g. a product chip) using relevant layout parameters extracted from the layout. The chip-scale simulation gives prediction of dishing and erosion and can be used for layout design rules such as assessing the effectiveness of dummyfication. This thesis is not to cover all aspects of this methodology to understand and model CMP variations. Rather, this thesis focuses on the development of

the test mask that serves as the foundation for all characterization and modeling work. Then, the thesis presents characterization methodology and result for single layer and multi-layer CMP thickness variations. The modeling and simulation aspects of the methodology are developed by a research colleague, Tamba Tugbawa. Please refer to his Ph.D thesis for the complete description of the modeling work for CMP [16].

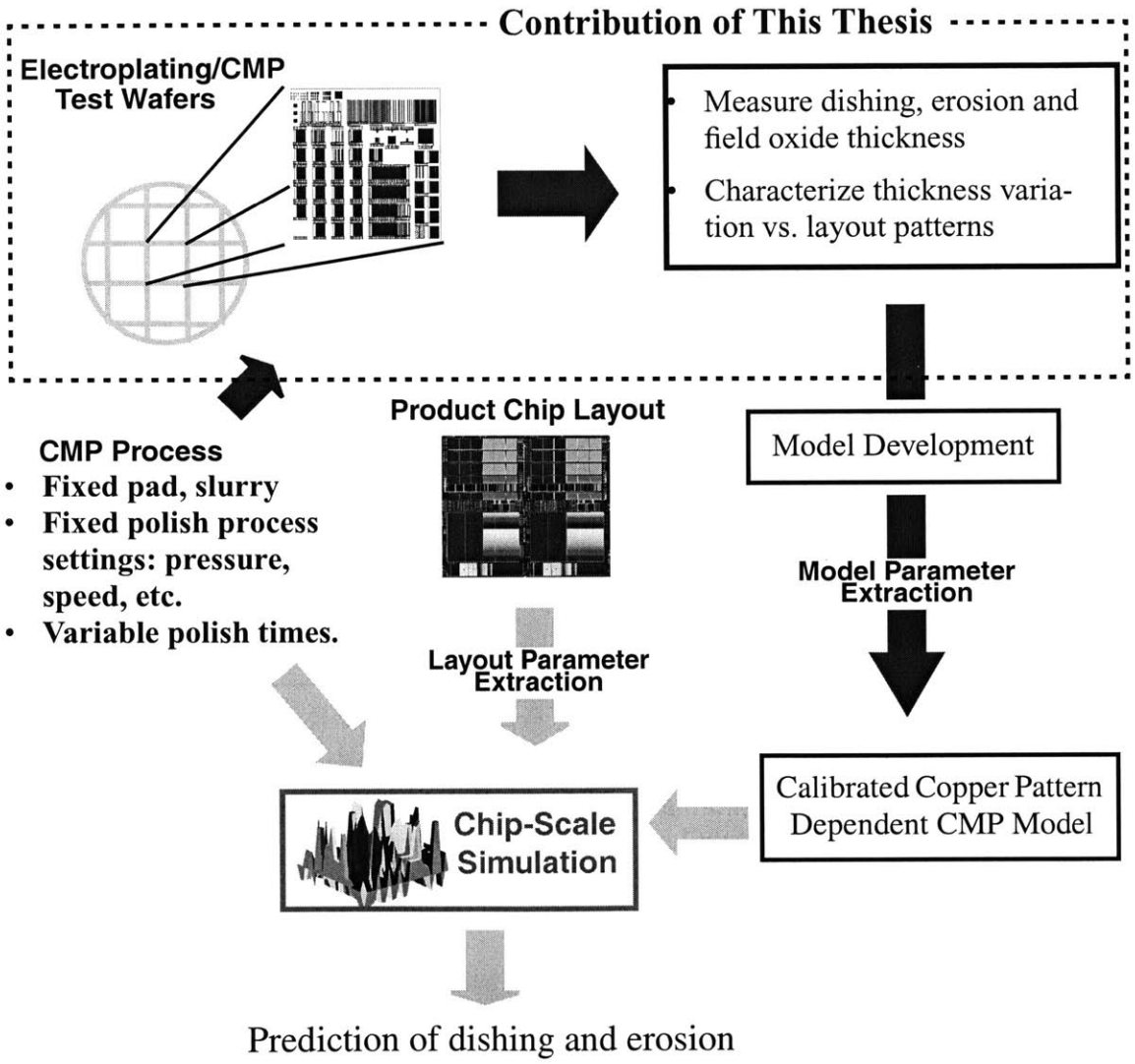


Figure 2.2: Overall Methodology for Characterization and Modeling of Thickness Pattern Dependency in Copper CMP

2.3 Overview of Integration for Electroplating and CMP Chip-Scale Simulations

As discussed in Chapter 1, the initial non-uniform topography has a directly impact on the CMP polishing behavior and this topography is created by the pattern dependency in copper deposition in electroplating. Thus, we need to define what topography information is transferred to CMP model so that it can make an effective use of the plating information. The plating topography information needed by CMP is dictated by CMP simulation needs as the calibrated CMP model uses the electroplated topography as the initial condition of the die surface. Specifically, CMP uses the electroplated topography information of final thickness, step height, and as-plated pattern density to calculate removal rates at various locations across a whole chip in bulk copper removal stage. Subsequently, CMP model uses extracted layout parameters of a chip to predict copper dishing and erosion in the third stage of polishing. Figure 2.3 summarizes how the electroplated topography information is fed-forward to the CMP modeling methodology.

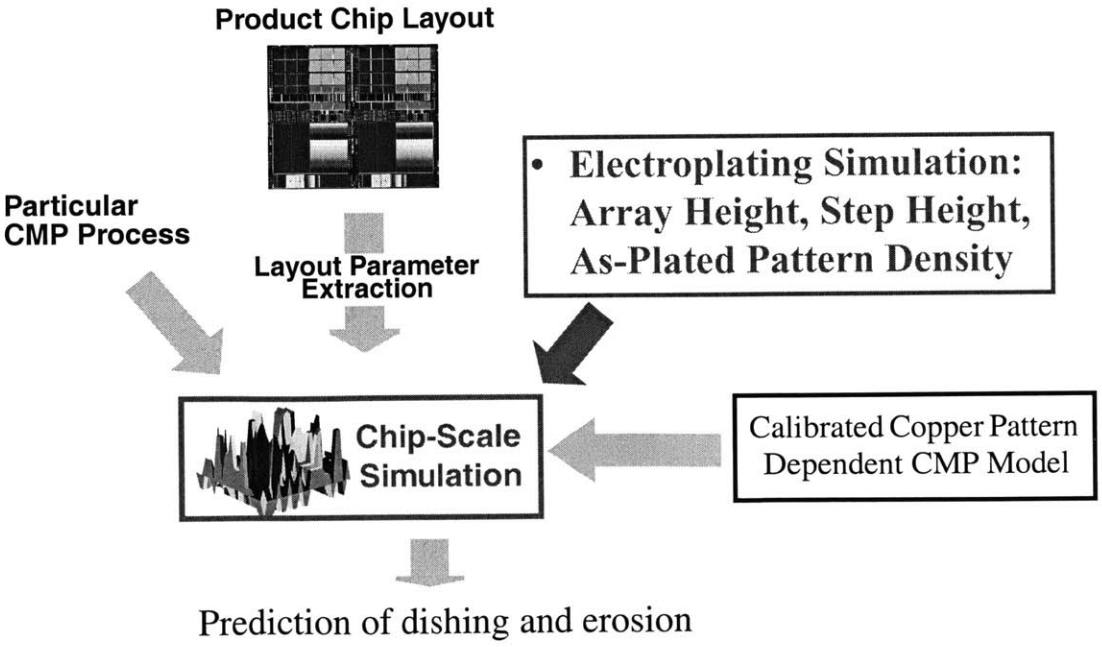


Figure 2.3: Integration of Electroplating Model and CMP Model for Complete Chip-Level Simulation

How the electroplated topography is used in the CMP model is summarized in Chapter 6. As it can be seen, each characterization and modeling methodology for electroplating and CMP does not change for the purpose of the integrating the two models for chip level simulation. The integration is efficiently done through three electroplated topography information, array height, step height, final thickness, and pattern density, that are fed-forward to the CMP simulation. This information transfer is done for each discrete unit of grid cells where the grid cells are common in both electroplating and CMP simulations. Thus, all information from electroplating can serve as an input to the CMP model as it is without any alteration or manipulation of the data.

Chapter 3

Test Structure and Mask Design

The key underlying vehicle that enables characterization and modeling of copper interconnect pattern dependency is a test mask. In this chapter, we present descriptions of test structures for a single level test mask. Measurement requirements and issues are also illustrated. The test mask described here has evolved from the original copper CMP test mask version 1.0 [17] through many experimental studies and subsequent enhancements of mask designs.

The test mask can be used for rapid characterization of electroplating and CMP characteristics such as consumable/tool comparisons, and process dependencies. Furthermore, these test masks can serve as a vehicle for calibrating and validating physical or semi-empirical models. There exist many process and integration issues in copper metallization, some of which are void-free electroplating especially for high aspect ratio trenches, barrier reliability, and CMP endpoint controls. However, the test masks presented in this thesis, including the multi-level mask design presented in Appendix B, are specifically designed to target layout pattern dependent behavior and related studies for copper electroplating and subsequent CMP planarization.

This chapter is organized as follows. First, structure design issues and principles are described including the relevant characteristic length scales in electroplating and CMP processes. Then, a single level mask is described followed by measurement descriptions.

3.1 Structure Design Philosophy and Issues

The fundamental issue in designing a test mask is understanding what kinds of patterns do actually matter in causing non-uniform topography after processing. Having a

wide range of patterns does not necessarily mean that the key pattern problems can be identified. A test reticle should contain relevant pattern factors, such as pattern density, that a process of interest has dependency on. Identifying these pattern factors typically occurs through previous studies or results in similar processes; for example, studies of tungsten CMP process pattern effects can help in assessing the copper process since they are both in-laid processes. In addition to the types of patterns, it is also critical that the designed patterns have a structure size that accounts for a characteristic length of a process so that each structure or pattern does not get confounded pattern effects from neighboring structures.

For example, if a structure region is only 500 μm wide when a characteristic length is 5 mm for a particular process, then the pattern effect from this particular structure has a significant amount of confounded influence from surrounding regions, complicating analysis especially when understanding of pattern interactions is not clear. Thus, each structure size should be big enough to attain a uniform local pattern environment. In addition, a structure design needs to remain simple, as complicated designs often cause measurement and analysis difficulties.

The placement of each pattern structure on the mask, also known as floorplanning, is the next critical factor in a test mask design. Floorplanning offers designers the flexibility of being able to place structures in strategic locations to either minimize or to cause possible structure to structure interactions. For instance, we have found that a field area of at least 100-200 μm is needed between structures for each structure to be considered "isolated" from other structures in the overpolish phase of the copper CMP process [18]. The designed structures and their placements must also offer strategic and easy measurement plans for efficient and effective data gathering. For example, if a structure size is too big or if two structures are side by side, then a surface profile scan would contain excess noise

from leveling by the profiler or distortions from wafer warp that would make it hard to distinguish what is noise and what is actual behavior. We encountered this measurement difficulty due to having structures side by side in an early test mask design (version 1.0), and all the subsequent designs have eliminated the problem by inserting field area separations between structures.

All of the issues described above – pattern factors, structure size, and placement – are critical in a test mask design to capture key pattern effects in a process. These design issues are described in detail in test structure designs in the following sections.

3.1.1 Characteristic Length Scales in Electroplating and CMP

As discussed in the previous section, structure design must take into account characteristic length scales in a process. This section thus summarizes key length scales observed in the electroplating and CMP processes so that structure design principles are better understood. Since we want to use the same test mask to characterize both electroplating and CMP, the design must meet the characteristic length scales for both processes. This section first summarizes the relevant length scales in electroplating. Design of test structures is a iterative process where findings from experiments enable improvements in design. Thus, in discussing electroplating and CMP length considerations, we refer to early studies and experimental results; in may cases these results are presented later in more detail for electroplating in Chapter 4, and for CMP in Chapter 6.

In the electroplating process, our studies have found that the plated profile depends primarily on the details of the local feature itself. To first order, electroplating is a localized process where the plating depends on the line and its surroundings including the spacing and the nearest neighbors [19]. Thus, the characteristic length scale is equal to the feature size including the nearest neighbors within 2-5 μm of the feature. Thus, if there are

more than several lines in a test structure, a uniform and self-contained local pattern environment is formed. Also, it is observed that if a line is positioned away from other lines by more than 5-10 μm, then the line can be considered as an isolated line where it is not influenced by other lines.

The test mask design described later has a line/array structure with an isolated line that is hundreds of microns away from other structures, and this is far greater than the 3-5 μm transition region length scale seen in electroplating. Thus the line structure can be effectively treated as an isolated line. For an array region consisting of sequences of lines and spaces, the test structure size is on the order or millimeters containing regular arrays of many lines. Thus the array size of the array region is large enough for use of the structures in studies of pattern effects in electroplating. We find that the constraining characteristic length scale governing the test mask design is imposed by the CMP process, rather than by the electroplating process. Thus, the designed test structures can be used effectively for an integrated studies of pattern effects in both processes if they satisfy the more difficult CMP imposed design challenges.

In oxide CMP, one length scale has been found to dominate: a "planarization length" on the order of 3-7 mm effectively averages the density of raised topography within that range, determining the relative rates of polish [20]. In copper polishing, on the other hand, three different length scales appear to be at work. First, an analogous long-range (e.g. 6 mm in [21]) pattern density dependence appears to be important during the initial planarization of the bulk copper. Second, a relatively sharp and short range transition of approximately 50-200 μm is observed between a field oxide region and the dishing/erosion profile in an array region as shown in Figure 3.1, or between two different density/pitch array regions [18, 22]. We have also found that field area of at least 100-200 μm is needed between structures for each structure to be considered "isolated' from other struc-

tures in the overpolish phase of copper CMP process [18]. Finally, very short range dependencies on the order of the individual line width or space (feature length scale) can substantially accelerate or limit dishing and erosion [22].

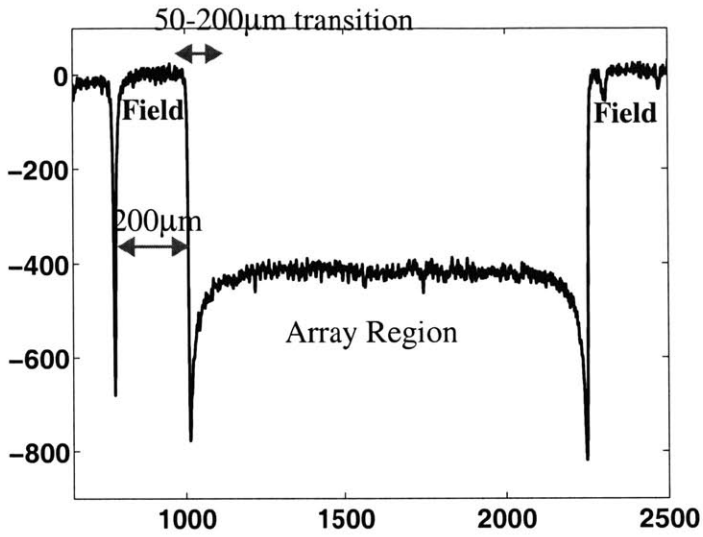


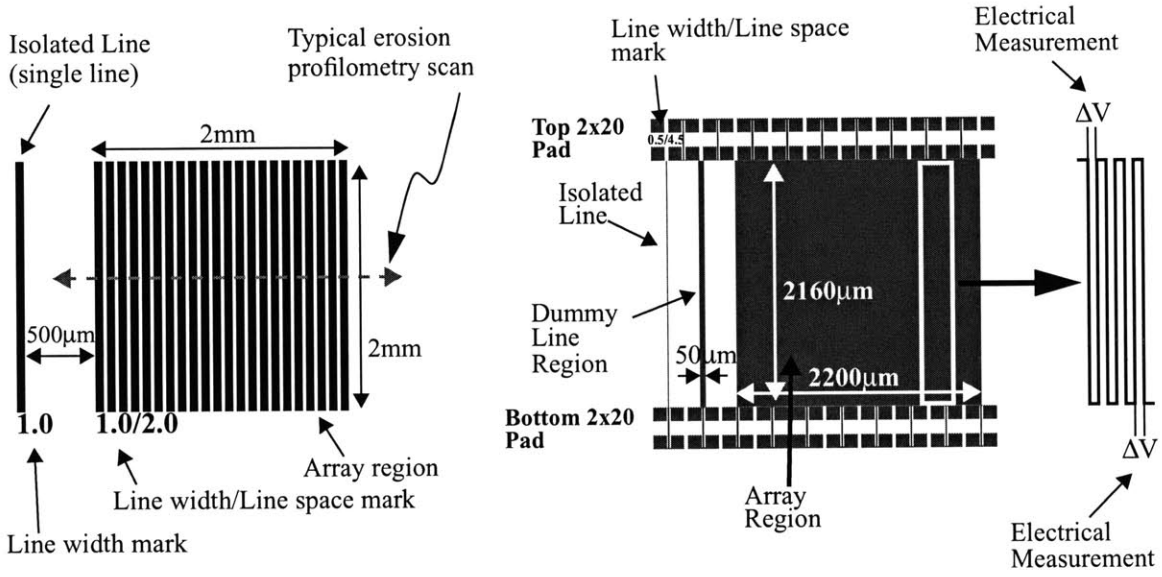
Figure 3.1: Sample Erosion Profile Across an Array Region

The variety of these length scales and their influences must be accounted for in the design and layout of test structures for copper interconnect pattern dependency characterization, as well as in the measurement and analysis of topography data.

3.1.2 Basic Test Structure Design: Line/Array

In this section we first describe the basic line/array structure used to explore array and step height in electroplating fill, and dishing and erosion in the CMP process. We then discuss the key principles and guidelines for structure design and layout to address the length scales discussed above, as well as how these structures support physical and electrical measurement of key pattern dependencies.

As discussed earlier, the pattern dependent problems in plating and CMP have been found to depend on both line width and line space. To mimic interconnect, arrays of lines and spaces form the fundamental test structure for the study of pattern dependencies. Shown in Figure 3.2a is a test structure that incorporates two regions or elements. The "isolated line" on the left gives pattern effect due to an isolated line with minimal surrounding influence, and this is used to obtain isolated feature plating step height and CMP dishing information. The "array" region gives information about array bulge or recess in electroplating and array erosion in CMP across a series of lines, as well as feature step height and dishing within array lines.



a. Physical Test Structure **b. Electrical Test Structure**

Figure 3.2: Line and Array Test Structures

For a line to be considered "isolated" its electroplating and polishing behavior should not be influenced by nearby array region. For CMP, we have seen that oxide spaces greater than 200 μm or so erode relatively little [18, 22, 23], so that separation of 300 to 500 μm

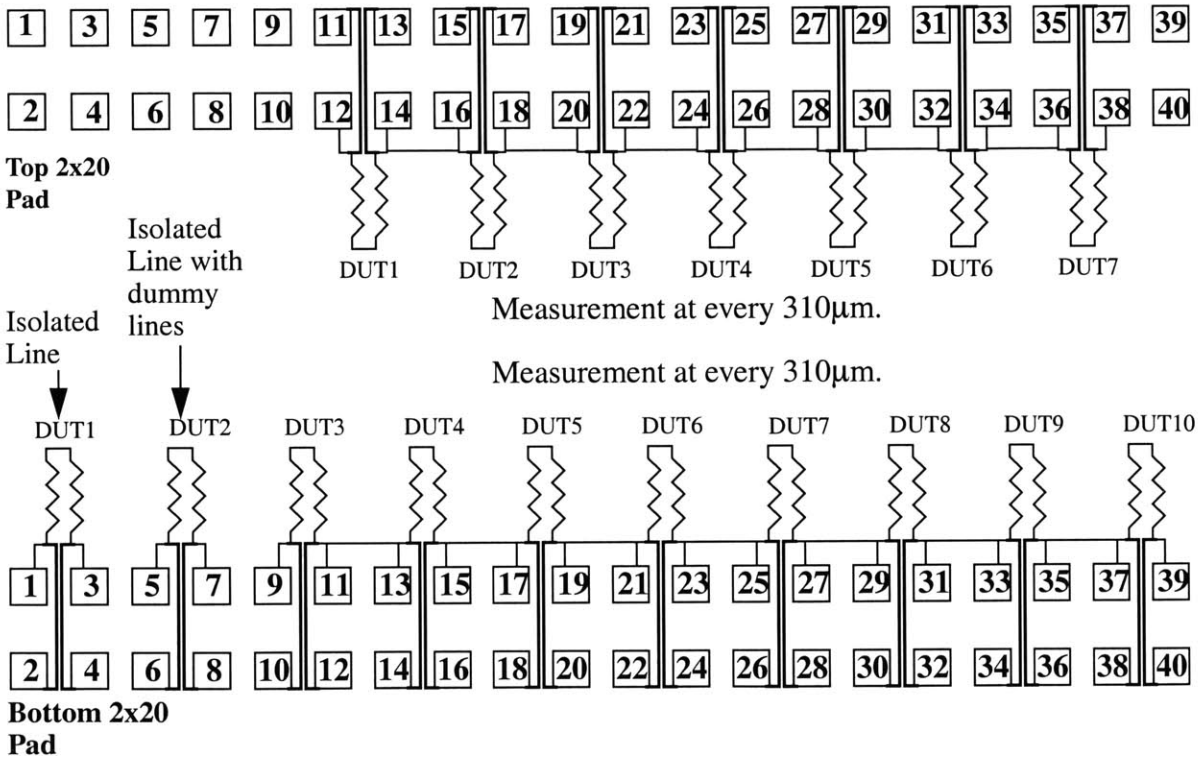
between the isolated line and the associated array region should minimize the impact of erosion on the isolated line. Also, this separation distance is large enough for the isolated line to be electroplated without array region influence.

The entire array structure is relatively large in size (~2000 x 2000 μm or more), and is separated from neighboring structures (including the associated isolated line) by substantial oxide spacing of 500 μm to decouple interactions among structures to give a large field area to serve as measured surface profile reference points. The array region size of 2-3 mm is selected to be an appreciable fraction of the bulk copper planarization length and significantly more than the transition length in CMP erosion profile (50-200 μm), so that a relatively constant effective pattern region is established within the structure. Furthermore, this choice of array size is large enough for an electroplating process as well since only an array size of tens of micron is required to maintain a uniform local pattern environment.

It should be remembered, however, that in CMP the bulk copper polish interacts over several mm; by keeping the isolated line relatively near to the corresponding array structure, both should experience similar long range averaged pattern densities. Considering the other extreme, dishing within the array will depend on both line width and line space. Typically, the dishing of a line in this case 'sits' on top of the erosion profile where the array erosion profile has a rather sharp transition from the field oxide region to the structure region. This length is on the order of 100 μm, and thus we want the structure size to be several times larger than this so that a series of lines across the array can be examined without any influence from the transition region.

This basic structure is also extended with electrical bond pads for electrical testing as shown in Figure 3.2b. Such electrical testing is only applicable in post-CMP characterization after the copper and barrier have been sufficiently cleared to produce electrically well-defined copper lines and structures. Each structure consists of an isolated line, a dummy

line region, and a pattern region with electrical bond pads on both the top and bottom of the structure. The "isolated line" consists of two line segments with a bend so that the measurement can be taken from the same set of bottom pads. Second, a dummy line region is added for electrical test structure design and consists of a line surrounded by a small region (50 μm wide) containing similar lines. The dummy line region is away from the isolated line and the array region by 200-300 μm so that structure influence is minimized.



Note: Although not explicitly shown, the lines connected to the bottom 2x20 pad and the lines connected to the top 2x20 pad are all connected since all lines are designed in a serpentine fashion.

Figure 3.3: Density Structure Circuit Representation

The array region is made up of serpentine lines providing resistance measurements based on a 4-point Kelvin structure. The use of both top and bottom pads is to increase the number of measurements that can be made on each structure: a spatial sampling along the array is thus possible. As the circuit representation shown in Figure 3.3 indicates, the electrical line resistance measurements are sampled evenly across the whole array region at every 155 μm. This is done by interleaving top and bottom measurement taken at every 310 μm. Serpentine lines also allow simultaneous resistance measurement on one loop of a line or an array for thickness extraction and continuity test of lines in the density structures. The spatial electrical measurement can also be used with the surface profile measurement as a complementary analysis.

3.2 Single-Level Copper Test Mask V1.2

Using the basic test pattern, a broad range of feature sizes, spanning typical IC designs from lower to upper metal layers, is used to form pattern structures for a test mask. This section contains the description for the single-level copper test mask version 1.2 evolved from the original test mask version 1.0. This mask is designed to understand and characterize pattern dependent variation of dishing and erosion on a wide range of density and pitch structures (thus, different line width and line space combinations), and further to model them for better process optimization and integration. As discussed previously, the test mask also provides the range of features and pattern environments needed for characterization of copper electroplating process pattern dependencies. This mask consists of the basic line/array test pattern with a wide range of pattern features such as pattern density and pitch (thus, different line width and line space combinations).

The mask is a single level mask of die size 20 mm x 20 mm with a minimum geometry of 0.25 μm for line width and 0.25 μm for line space, and a maximum geometry of 500 μm lines. The floorplan of the test mask is shown in Figure 3.4.

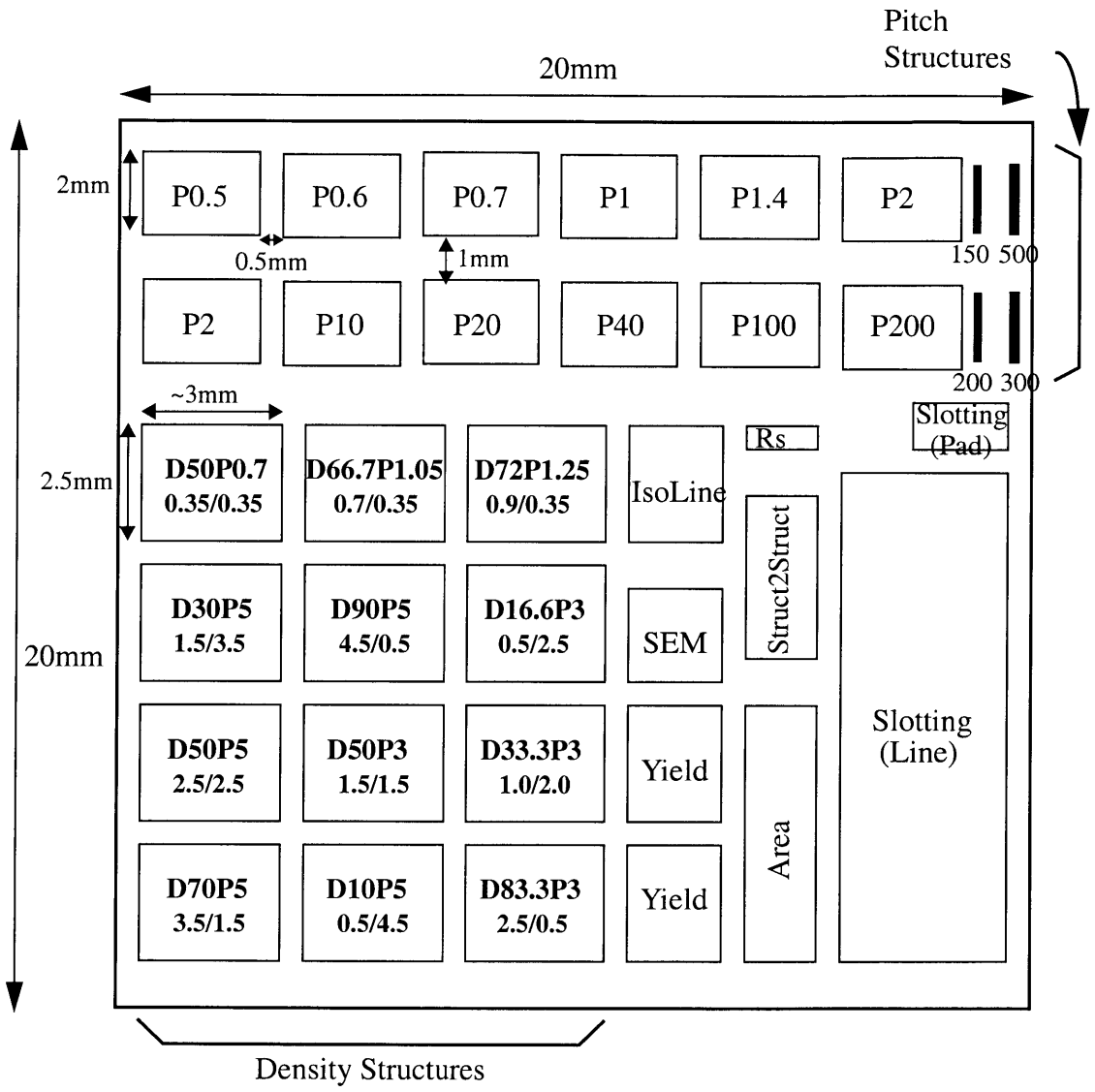


Figure 3.4: Single-Level Mask Floorplan

In the floorplan, pitch structures (top two rows) are marked with "Pxx" where xx is the associated pitch value in microns. Pitch is defined as the sum of line width and line space. If no density is indicated, the default density of 50% is used (e.g. same line width and line

space). For example, a structure designated with "P0.5" has a pitch of 0.5 μm, or a line width and space of 0.25 μm, respectively. To the right of the pitch structures are some wide lines having line widths of 150, 200, 300, and 500 μm without associated array regions. The density structures are marked with "DyyPxx" where yy is the associated percentage density of copper lines for the given pitch of xx microns. The density is defined as the ratio of line width to pitch, and the range of density for these structures are from 10% to 90% for fixed pitch of 5 μm, and from 16.6% to 83.3% for fixed pitch of 3 μm. For example, "D90P5" indicates 90% density for pitch of 5 μm, and this structure has 4.5 μm lines and 0.5 μm spaces. Likewise, 100% pattern density is solid copper and 0% pattern density is just oxide.

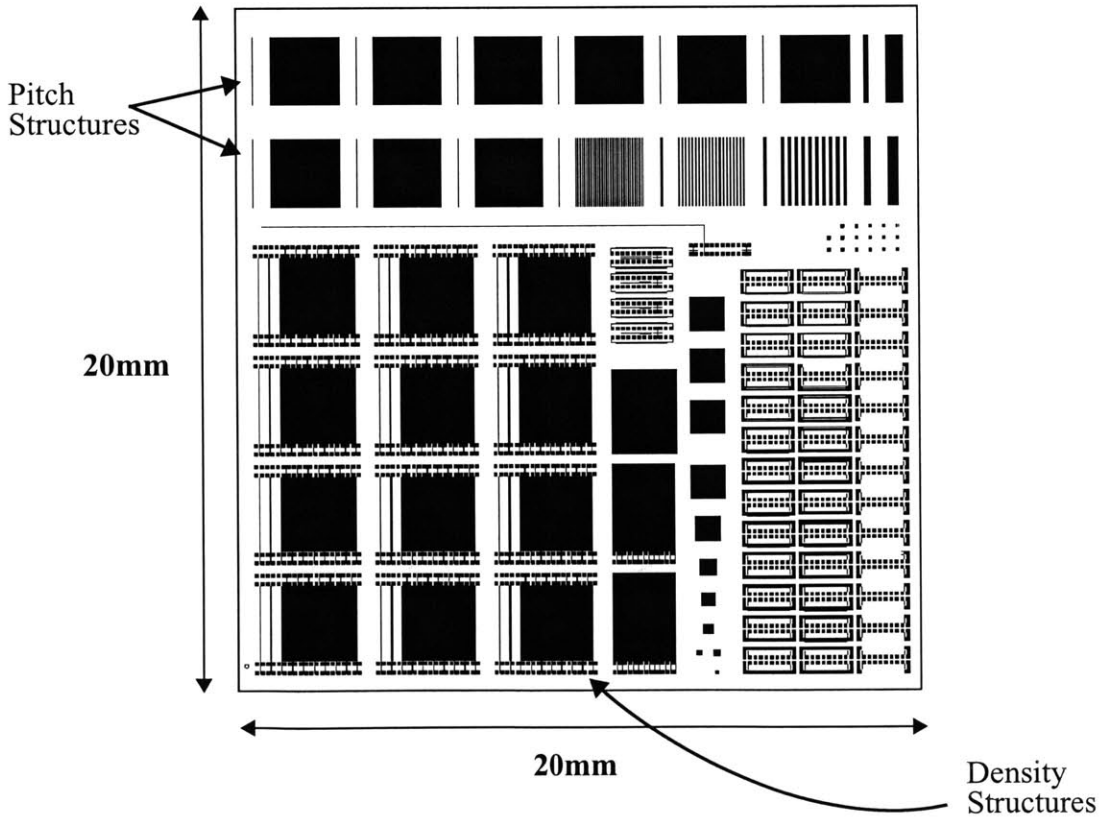


Figure 3.5: Single-Level Copper Test Mask V1.2

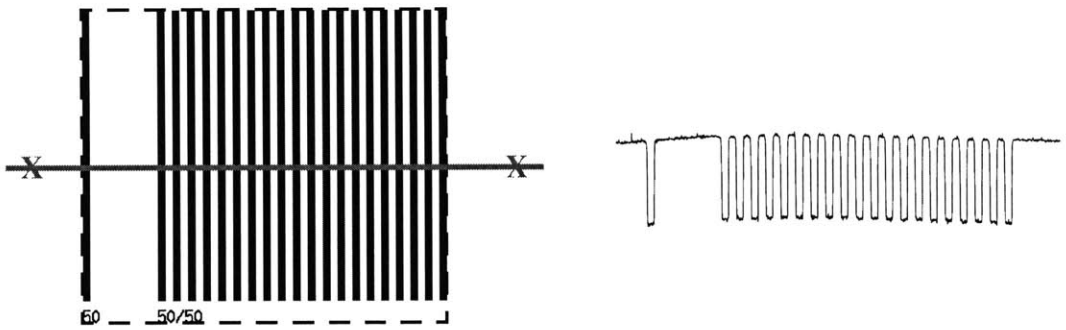
The layout of the test mask is shown in Figure 3.5, and the shaded areas (e.g. shaded lines) correspond to the test structures. Some parts of the layout are not printed due to the resolution of the picture. The top two rows of structures are pitch structures where the pitch is varied from 0.5 μm to 200 μm at a fixed pattern density of 50% (e.g. same line width and line space). The other main pattern structures are density structures. A density region is made up of serpentine style lines with the size of 2200 μm x 2160 μm as described earlier in Figure 3.2b. There are additional structures in this mask design and they are found in Appendix A and in the mask documentation [24].

3.3 Measurements

The main measurements for the test structures are surface profile scans and film thickness measurements of copper and oxide. For a relative height measurement of the line/ array test structures, a surface profile scan is made across each structure containing both the isolated line and the corresponding array region with optional film thickness measurements at each end of the scan (e.g. indicated by X) as illustrated in Figure 3.6. The surface profile scan should extend at least 200 μm to the left and right of the structure so that the trace can be leveled referenced to the field region. Film thickness measurements can be also used to level surface profile scans by forcing the ends of the scan to match the film thickness measurements.

Surface profile scans are made by tracing across a pattern region with a small stylus tip actually touching the wafer surface, and recording relative surface heights. Surface profilers used in this thesis work are the KLA-Tencor HRP (High Resolution Profiler) and P10 tool, and a Veeco profilometer (Dimension Vx Atomic Force Profiler) which has integrated atomic force microscopy (AFM) and long range scan capability. The HRP or Veeco profilers are used whenever possible since its sub-micron stylus tip size enables the mea-

surement of fine lines down to the geometries of our interest (e.g. 0.25 μm or 0.18 μm). The P10 profiler has a rather large tip size of about 2 μm and is limited to measuring large features or array heights. Some of these machines, especially the HRP, have automatic pattern recognition capability so that automatic measurements of many structures are possible once a recipe is set up. One possible drawback of a profile scan is that when a relatively long scan is taken, typically greater than 3-4 mm in our experience, the profile traces suffer from non-linear leveling problems and it is often hard to analyze the scans. To minimize this leveling issue, the test structures are designed so that scan lengths do not go beyond 3 mm or so.



Line/Array Structure with Profile and Film Thickness Measurement Plan

Sample Profile Scan

Figure 3.6: Sample Measurement Plan

For measurement of dielectric oxide, KLA-Tencor Assert-F5 is used. This tool is based on optical interferometry and ellipsometry to measure absolute film thicknesses. It offers faster throughput than surface profile scans, and it also has pattern recognition capability. It has a measurement spot size of 5-40 μm and has 50-100 Å of accuracy for typical dielectric films (e.g. silicon dioxide). One drawback in this kind of tool is that it cannot measure copper thicknesses which is a major limitation for our studies of copper intercon-

nects. However, direct copper thickness measurement has become possible with new emerging tools such as the Impulse 300 from Philips Analytical and the MetaPULSE 200X from Rudolph Technologies. For the study presented here, we use the MetaPULSE 200X which uses picosecond ultrasonic laser sonar for a non-contact and non-destructive measurement technique based on laser-induced ultrasound [25]. It has a measurement spot size of around 20 to 30 μm and offers excellent accuracy and repeatability of measurements taken in wide field regions. The measurement is within 150-200 Å of accuracy compared to SEM measurement for 3000 Å thick bond pad, and its repeatability is typically better than 0.5% standard deviation (e.g. roughly 60 Å of standard deviation for copper thickness of around 12400 Å).

In addition to these "physical" measurements, electrical measurements are possible for obtaining line resistances which then can be converted to line thicknesses. The HP4062, an automatic parametric system, is used for electrical testing and can be programmed to collect a large amount of data. The main advantage of using an electrical measurement is that it enables measurement of fine features and complements the profile measurements, which is especially important in the multi-level studies presented in Chapter 6.

3.4 Summary

In this chapter, test masks have been described that support the measurement, characterization, and modeling of pattern dependencies in both copper electroplating and CMP. Multilevel effects are also important in CMP; extensions of the test mask structures described in this chapter are presented in Appendix B and multilevel experimental results are shown in Chapter 6. In the next chapter, we examine various pattern dependent trends in electroplated topography using the test mask described in this section.

Chapter 4

Characterization and Modeling of Surface Topography in Electroplating

As noted in Chapter 2, careful characterization of the pattern dependent electroplated topography variation is critical to understand the fundamental limitations of the process and to assist in new process developments. This chapter corresponds to the second part of the overall methodology outlined in Chapter 2 and presents characterization of as-plated copper topography variation as a function of various underlying layout parameters such as line width and line space using the test mask as the vehicle. First, a wafer is electroplated with a baseline process and various height differences are measured. Then, the data is analyzed to capture topography variation trends while identifying key layout parameters that influence such trends. Once such observation is made, a semi-empirical model is formulated based on the empirical data. This empirical model is informed by consideration of physical electroplating mechanisms; these help determine the model structure and model variables that are semi-physically based. This chapters ends with a summary of the model fit to the data capturing both the superfill trend and conformal fill trend.

4.1 Surface Topography Definitions

The as-plated pattern dependent surface topography variation has been introduced in Chapter 1 and is revisited here to remind us of the definitions of different height variations in electroplated surface topography. The as-electroplated topography can be characterized by two height parameters: a feature scale step height (SH) and an array height (AH) as shown in Figure 4.1 for a superfill (also known as bottom-up fill) electroplating process. Step height is defined as the height associated with each copper line. If copper sticks up

due to superfill effect, then the height is assigned a positive number, whereas if the copper line recesses, then the step height is assigned a negative number. This notation of positive and negative is to distinguish whether a line fill is superfill or conformal fill. Array height is defined as the height difference between the top of the raised features in an array and the flat copper field region over wide oxide. Similar to the step height definition for positive and negative assignment, array height is referenced to the field area which is defined to be at zero. Thus, when a bulge is present (as for the case of fine line and fine space), we have a positive array height, whereas when the overall array region is recessed with respect to the field area, we have a negative array height. Thus, if we add the array height to the nominal field area thickness, we get the total copper thickness.

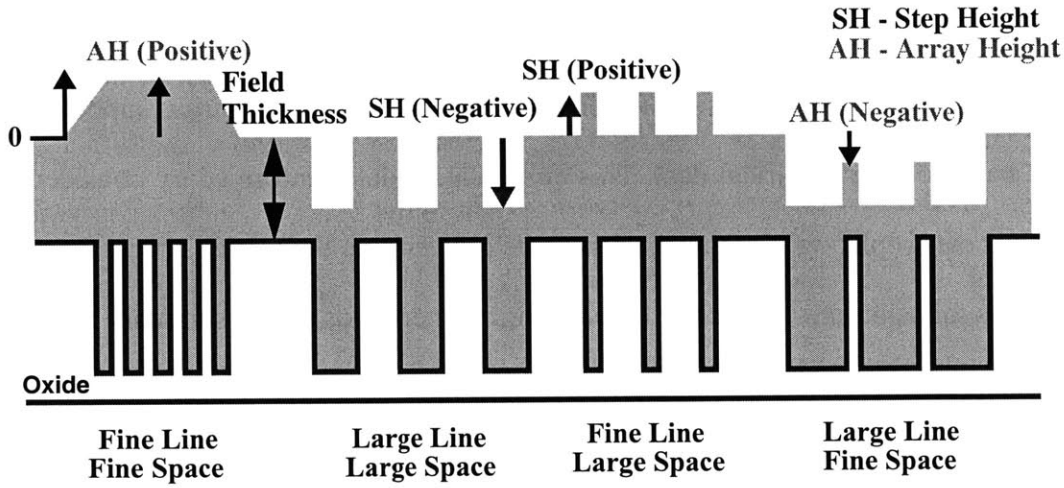


Figure 4.1: Non-Uniform Topography in Copper Electroplating (Superfill)

4.2 Experimental Setup and Measurement

For this study, we use the MIT Copper Test Mask Version 1.2 which has minimum feature size of 0.25 μm for line width and line space. Full description of the mask is found in Chapter 3. A short flow process is used where an 8" wafer is deposited with oxide, pat-

terned and etched with a nominal trench depth of 5500 Å. Then, a tantalum based barrier layer is deposited followed by copper seed deposition and electroplating using a Novellus tool. The nominal target thickness of 15500 Å over wide field area (e.g. region without any trenches) is electroplated on the wafer surface. We will refer to this as plating experiment A.

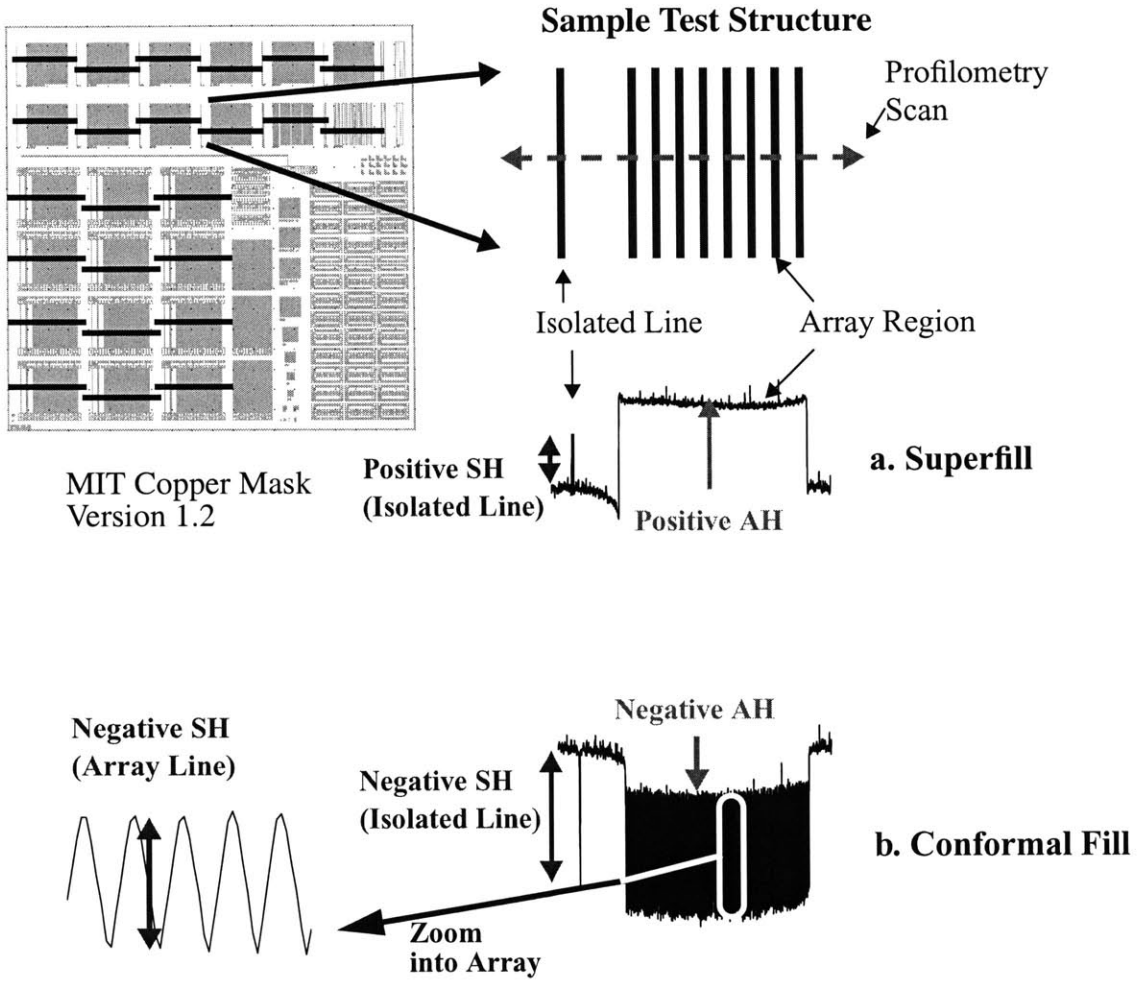


Figure 4.2: Test Pattern and Sample Profile Scans for (a) Superfill Plating, and (b) Conformal Fill

Once the wafer is electroplated, we measure the relative surface heights using a KLA-Tencor HRP (High Resolution Profiler) machine. As illustrated in Figure 4.2, for each of

the test patterns, we make a surface profilometry scan to obtain the step height for the isolated line and the array line, and the array height in the array region. Two example scans are shown in Figure 4.2 which exhibit different electroplating characteristics. The first shows a case where a superfill plating is performed, and the second scan shows an example of a more conformal fill plating process.

4.3 Characterization and Trends

For our characterization, we want to quantitatively examine both the step height and array height as a function of various underlying layout parameters and identify key trends. First, the surface profile scans are examined to observe qualitative trends in electroplating. Quantitative evaluation of these trends are then considered.

4.3.1 Surface Profile Trends for Various Patterns

The wide range of pattern induced surface topography variation is seen in Figure 4.3 and Figure 4.4. The surface profile scans shown in Figure 4.3 are for pitch structures from 0.25 μm width and space to 100 μm width and space as marked above each plot. In these structures, the line width is equal to the line space, so that all structures in this figure have 50% pattern density. Bulging of the array region can be seen for most of the structures in the top half of the figure, and greater bulge is observed for narrower lines and spaces. However, the bulge decreases as feature size increases, and it is observed that the bulging effect becomes negligible for the arrays having 1μm width and space. For the surface profile scans for the still larger pitch structures, the bulging effect is gone, and conformal deposition becomes more dominant with some recess seen for 2 μm to 10 μm array lines. Furthermore, varying degrees of step height are observed: small features have practically no or very small step height, and large features show a step height saturated at approximately the designed trench depth.

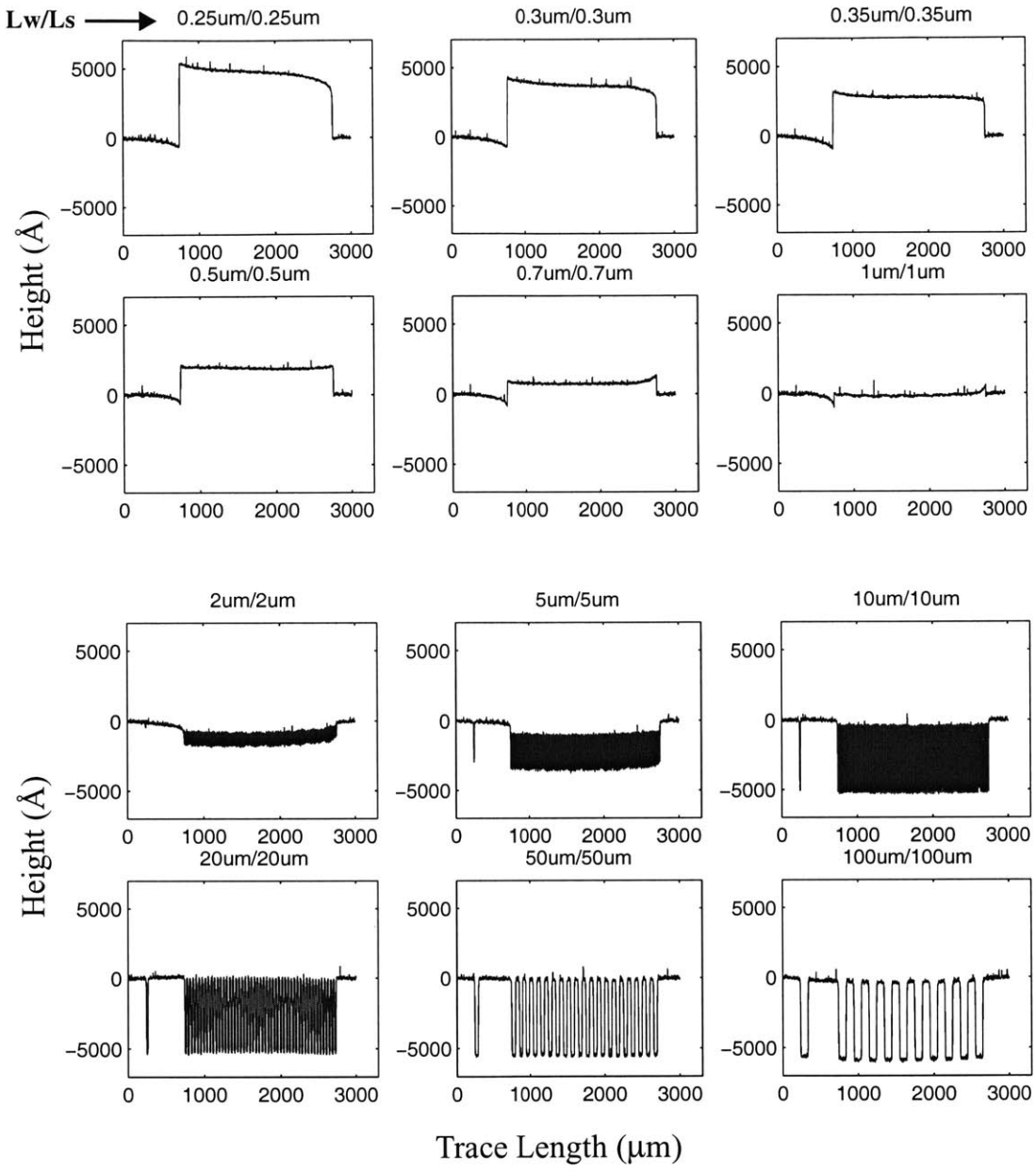


Figure 4.3: Surface Topography Profiles for Pitch Structures (50% Pattern Density): Plating Experiment A

Figure 4.4 shows the surface profiles for a range of density structures. The top row, which are structures where line width is changing from 0.35 to 0.9 μm for a fixed space of 0.35 μm, shows that the amount of bulging decreases as the line width increases, and indicates that there is a line width effect present that causes bulging of copper above the field

level. The middle and bottom rows are structures from 10% to 90% copper densities for fixed pitch of 5 μm (thus, 10% density array has 0.5 μm lines and 4.5 μm spaces). The 10% density array shows some bulging, and as the density increases the fill becomes more conformal in nature.

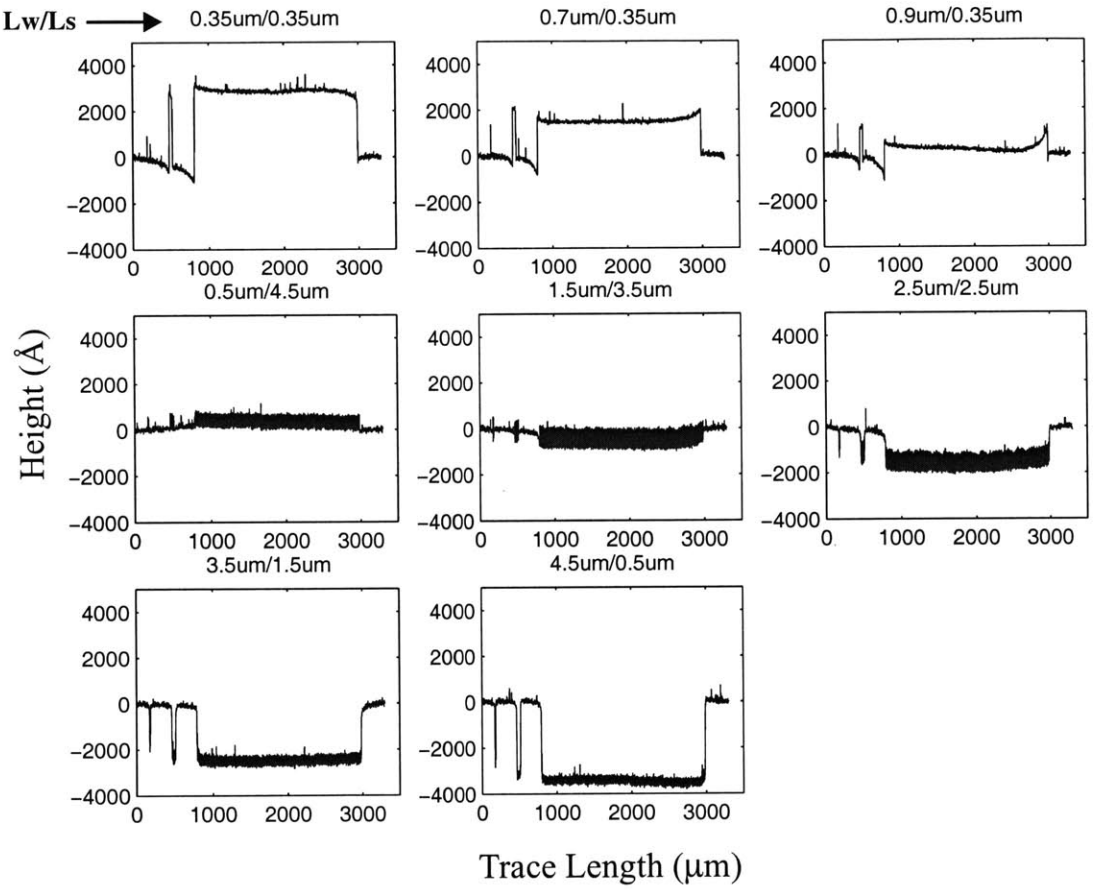


Figure 4.4: Surface Topography Profiles for Density Structures (Varying Pitch): Plating Experiment A

4.3.2 Step Height and Array Height Trends

The profiles examined above provide qualitative insight into trends for various patterns. In this section, the step and array heights are plotted as a function of underlying layout pattern factors based on extraction from the surface profile scans.

Figure 4.5 shows the step height as a function of the underlying line (copper trench) width. The top graph shows step height obtained from the isolated lines and the bottom graph shows step height obtained from the array lines. We can see from the top graph that step height is positive for small isolated features, indicating a regime of superfill up to a line width of 1 to 2 μm. Step height then becomes negative in Figure 4.5 as line width increases further. The negative step height indicates that lines are filled in a more conformal fashion as illustrated schematically in Figure 4.6(b). It can be noted that after about 10 μm (marked by L_W), the step height saturates at the trench depth of around 5500 Å, corresponding to the case of Figure 4.6(c). The saturation indicates that even if lines become wider, the step height remains at the trench depth showing that conformal deposition is dominant for large feature sizes. A similar behavior is observed for the array lines, where step height again depends strongly on line width. Since the test mask contains structures with the same line width but different line space, multiple data points are seen for a particular line width in these plots. The different step height values at these line widths indicate that, in addition to a line width dependence there is also a line space dependence in the plated step height.

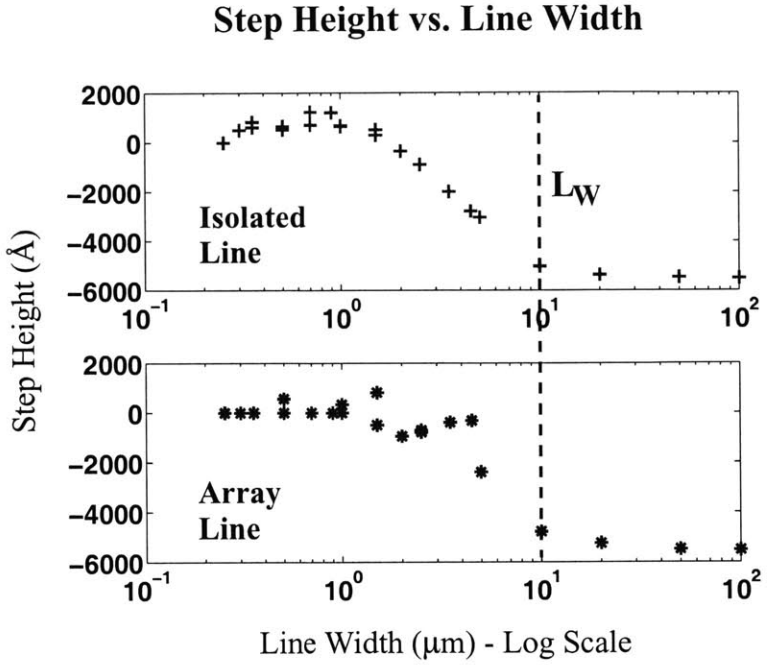


Figure 4.5: Step Height vs. Line Width for Isolated Lines and Array Lines: Plating Experiment A

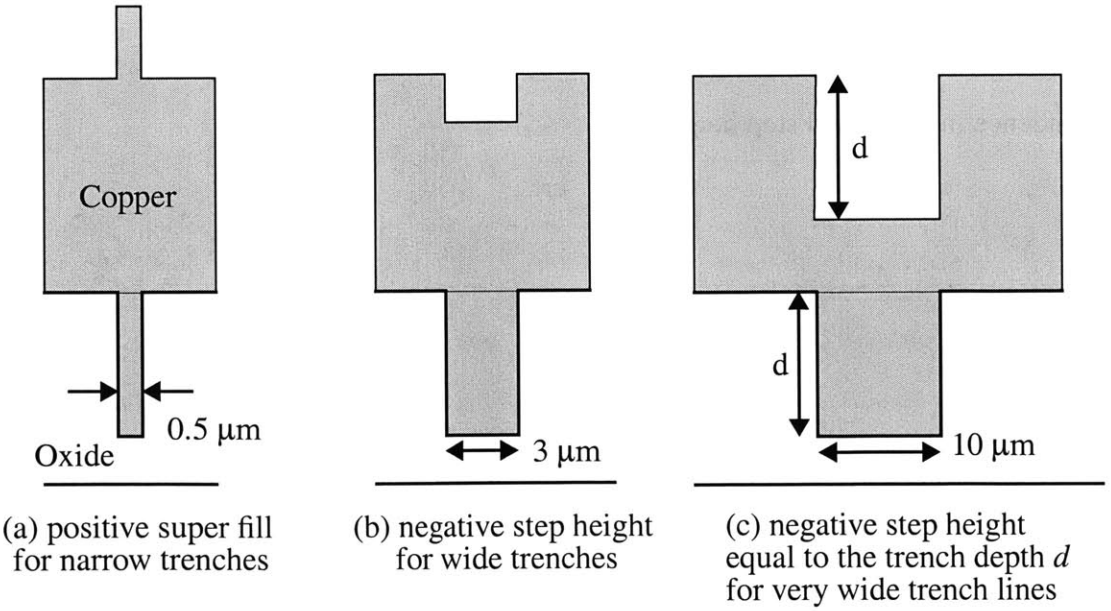


Figure 4.6: Fill Characteristics for Different Trench Widths

Next, we examine step height as a function of line space. Since the isolated lines do not have a notion of line space, we only examine the step heights obtained from the array lines. Figure 4.7 shows the observed dependence on line space. The trend is similar to the line width dependence: positive step height for small features is observed; the step height becomes negative as line space increases with a saturation beginning at around 10 μm (marked by L_S). The step height data can alternatively be examined as a function of pattern pitch or density to determine if there is a clear relationship between step height and these pattern factors. However, no clear trends in terms of these factors are seen; rather, trends in step height are more clearly seen as a function of the feature layout parameters of line width and space, rather than as a function of derived pattern factors such as pattern density and pitch.

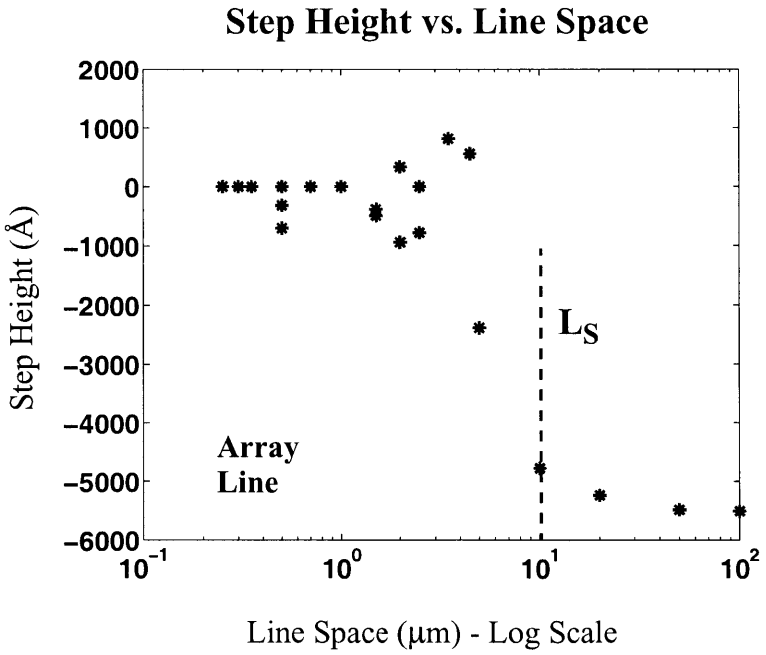


Figure 4.7: Step Height vs. Line Space for Array Lines: Plating Experiment A

For the case of array height, we also find that the trends are best captured as functions of line width and space. Figure 4.8 shows the array height dependence on line width. It is

observed that the array height is positive for small features, indicating bulging of copper due to superfill behavior, as pictured schematically in Figure 4.9(a),. The bulging effect is larger for small features and increases as line width decreases. As line width becomes larger (between 1 μm and 10 μm), the array height decreases and becomes negative, which indicates array recess as pictured in Figure 4.9(b). Then, as the line width increases further, the array height saturates and reaches zero beyond the line width of 10 μm (marked by L_W) as illustrated in Figure 4.9(c). In Figure 4.9(a) through (c), a hypothetical case of zero feature step height is shown in order to emphasize the array height effect. In reality, both parameters are varying. For example, Figure 4.9(d) schematically illustrates the surface topography for very wide trenches, where the array height is zero and the step height is equal to the trench depth. Returning to Figure 4.8, we again note that multiple data points are shown for the same line width since there are several test structures on the chip with different line spaces but with the same line width.

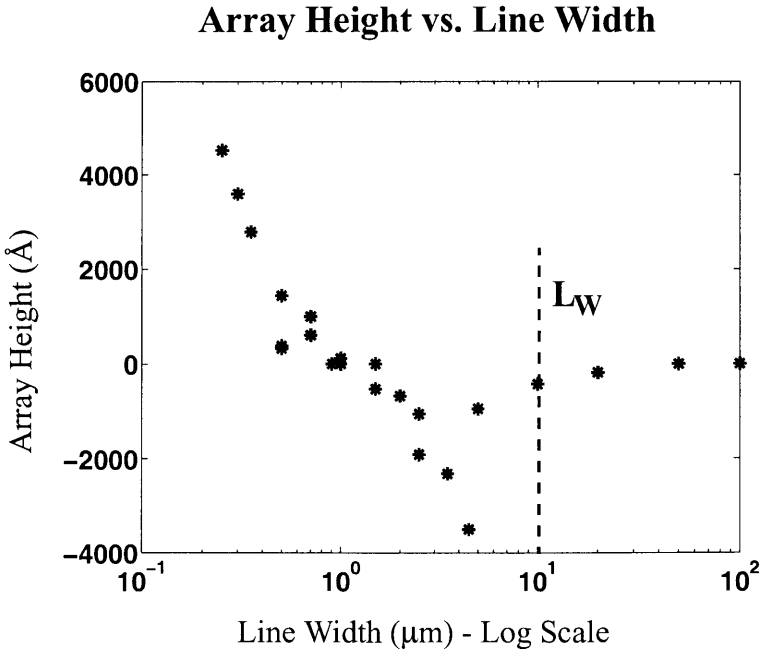
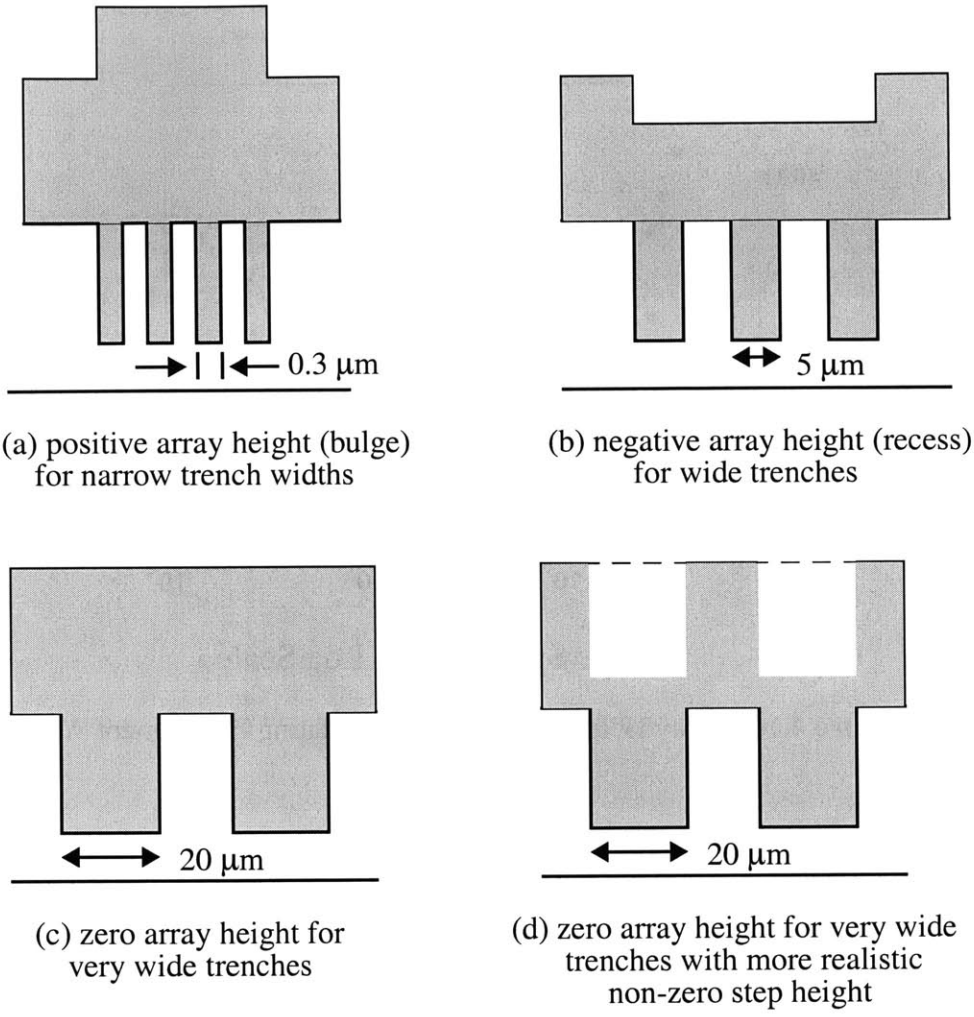


Figure 4.8: Array Height vs. Line Width in Log Scale: Plating Experiment A



(a) positive array height (bulge) for narrow trench widths

(b) negative array height (recess) for wide trenches

(c) zero array height for very wide trenches

(d) zero array height for very wide trenches with more realistic non-zero step height

Figure 4.9: Array Height: Bulge and Recess

The dependency of array height on line space is shown in Figure 4.10. For small feature sizes (thus small line space), the array height is positive (bulging), then becomes negative (recess) before saturating to zero at around 10 μm (marked by L_S). The saturation to zero array height for large line spaces indicates that beyond 10μm of line space, the region can be treated as field area.

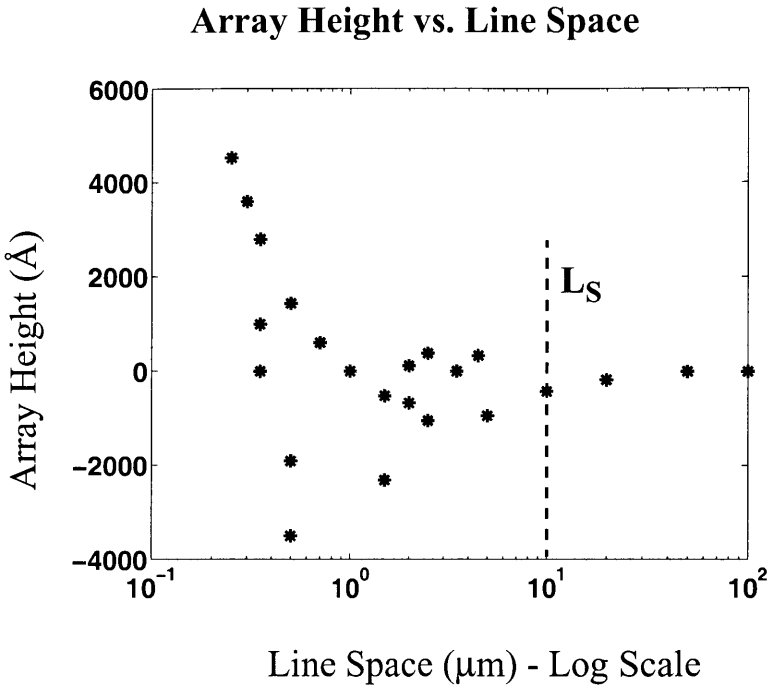


Figure 4.10: Array Height vs. Line Space: Plating Experiment A

Using the range of test structures in the test mask, the impact on both the step height and array height can thus be quantified, and trends as a function of feature layout parameters of line width and line space are identified. Overall, small features (small line width and spaces) show a superfill effect where the step height and array height are large and positive. In contrast, large features show conformal deposition where the electroplated profile resembles the underlying trenches and spaces. The saturation width (L_W) and space (L_S) for the step height are found to be approximately 10 μm, and the same value is also observed as the saturation point in the array height trends.

4.3.3 Characteristic Length Scales in Electroplating

The saturation width and space of 10 μm indicate a length scale for the degree of conformal deposition on the feature size. As noted, greater than 10 μm line width and space will result in simple conformal deposition for this particular electroplating process. This

observation of saturation feature size is important when we extract relevant layout parameters of a given layout for chip-scale simulation. However, this length scale for the conformity of within line deposition must not be mistaken with another characteristic length scale – that governing the influence of neighboring regions on electroplating – which we examine next.

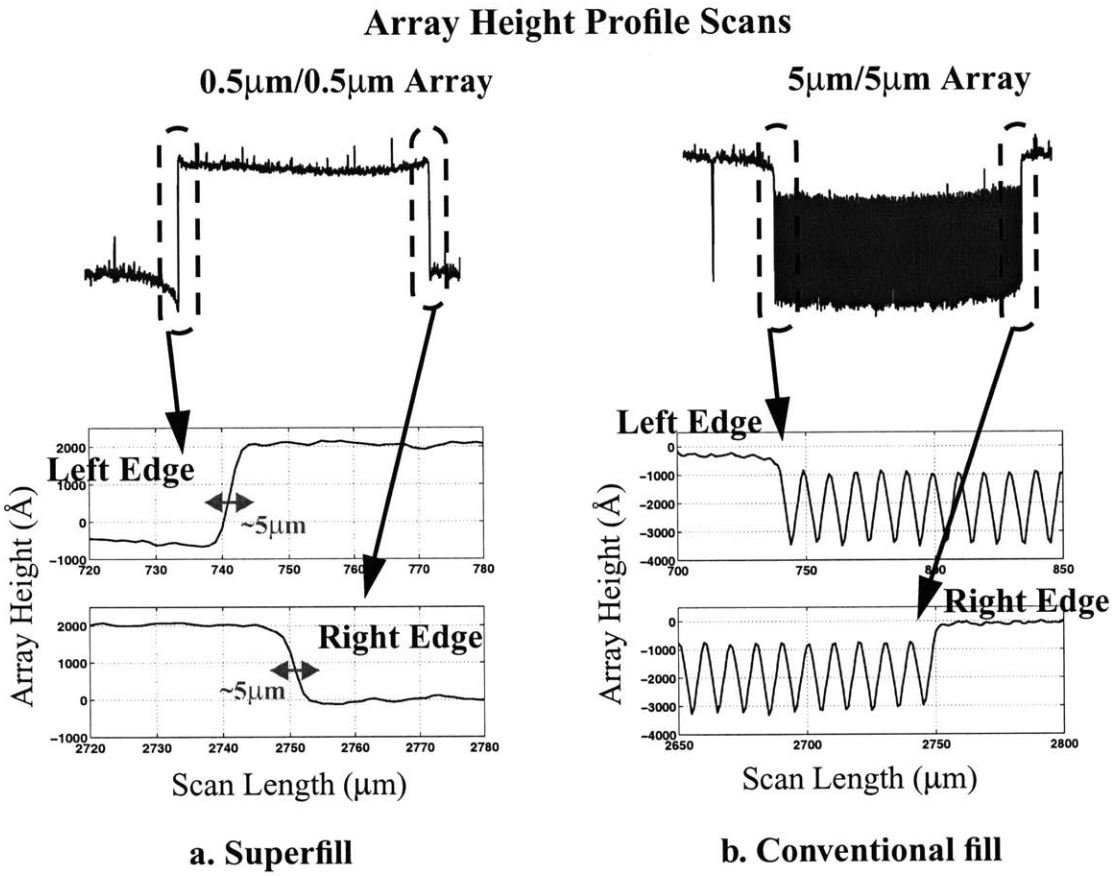


Figure 4.11: Sharp Transition from Field to Array Region: Plating Experiment A

Figure 4.11 shows array height profile scans for two array structures that exhibit superfill and conformal fill, respectively. Figure 4.11a shows the transition region at the edge of the array zoomed in and replotted. We see a rather sharp transition from field to the array. In contrast to the "saturation lengths" discussed earlier, we will refer to the width of the

transition in array or step height near the edge of the array as the "transition length." This transition length appears to be approximately 5 μm in Figure 4.11a. Similarly in Figure 4.11b, showing the recessed profile scan for 5 μm line and spaces, we se that the transition occurs within a single line width or within 5 μm. We can thus se that nearby structures can influence the array or step height of a neighboring structure, but only within a relatively short distance of 5 μm or less.

The short distance neighboring effect is also seen in a scan made across two neighboring arrays as shown in Figure 4.12 (as opposed to the scan from field regions into a single structure shown earlier). From one array region to the next, the transition is abrupt; again, the transition length appears to be well under 5 μm, and the fill changes from the edge line of one array to the edge line of the next array. This indicates that the electroplating length scale is rather short and depends primarily on the local features themselves (as opposed to the millimeter interaction distances seen in CMP). Thus, consideration of only a local "nearest neighbor" (or a few neighbors for very fine lines and spaces) should be sufficient to capture or predict the plating topography for a given set of features.

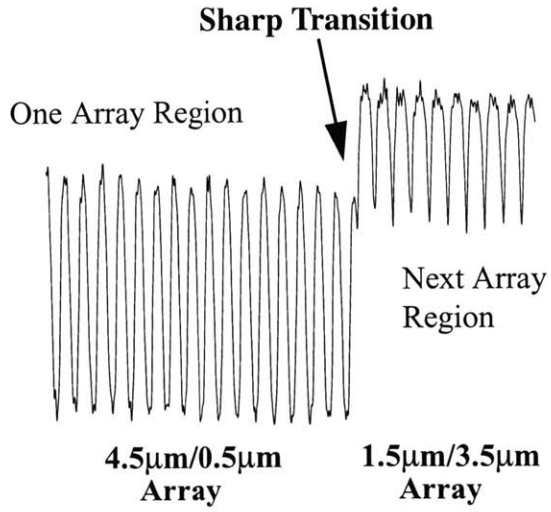


Figure 4.12: Nearest Neighbor Effect in Electroplating: Plating Experiment A

4.3.4 Interaction of Line Width and Space

Electroplating fill depends on more than just the dimension of the line being filled; rather, line space has an effect on the deposition rate and may cause varying degrees of step and array heights. Figure 4.13 shows the step height data obtained from a second plating experiment, which we will refer to as plating experiment B.

In this case, a different plating tool and process are used (provided by SEMATECH). Test wafers are patterned with the first layer of the MIT multi-level mask version 2.1 as described in Appendix B; this mask has minimum feature sizes of 0.18 μm for line width and line space, and the test structures are similar to the single-level mask version 1.2 described in Chapter 3. A short flow process is used where an 8" wafer is deposited with oxide, patterned, and etched with a nominal trench depth of 6500 Å. Then, a tantalum based barrier layer is deposited followed by copper seed deposition and electroplating using a Novellus machine. The version 2.1 mask is especially useful for studying the joint dependency on line width and line space, as it contains structures with fixed line width and varying line space. In the earlier version 1.2 mask, there are only a few such combinations, as seen in the previous trend plots.

The step height trend for superfill experiment B is similar to that observed in the experiment A data, but also reveals the line width and line space interaction more clearly. This interaction is shown in Figure 4.13b, where a range of step height values for a fixed line width of 1 μm are shown as a function of line space. As the line space increases, step height increases and saturates at about 2400 Å, which is close to the step height for isolated lines of 1 μm. This space interaction is also shown in the array line step height (in Figure 4.13a) for the 50 μm and 100 μm line width features: the step height is different for line spaces of 1 μm and 100 μm. For the 100 μm space, both 50 μm and 100 μm lines are filled conformally and the step height is equal to the initial trench depth of around 7000 Å.

For the 1 μm line space on the other hand, the step height is slightly less than the initial trench depth. These observations indicate that indeed there is space effect as well as width and space interactions in the electroplating process.

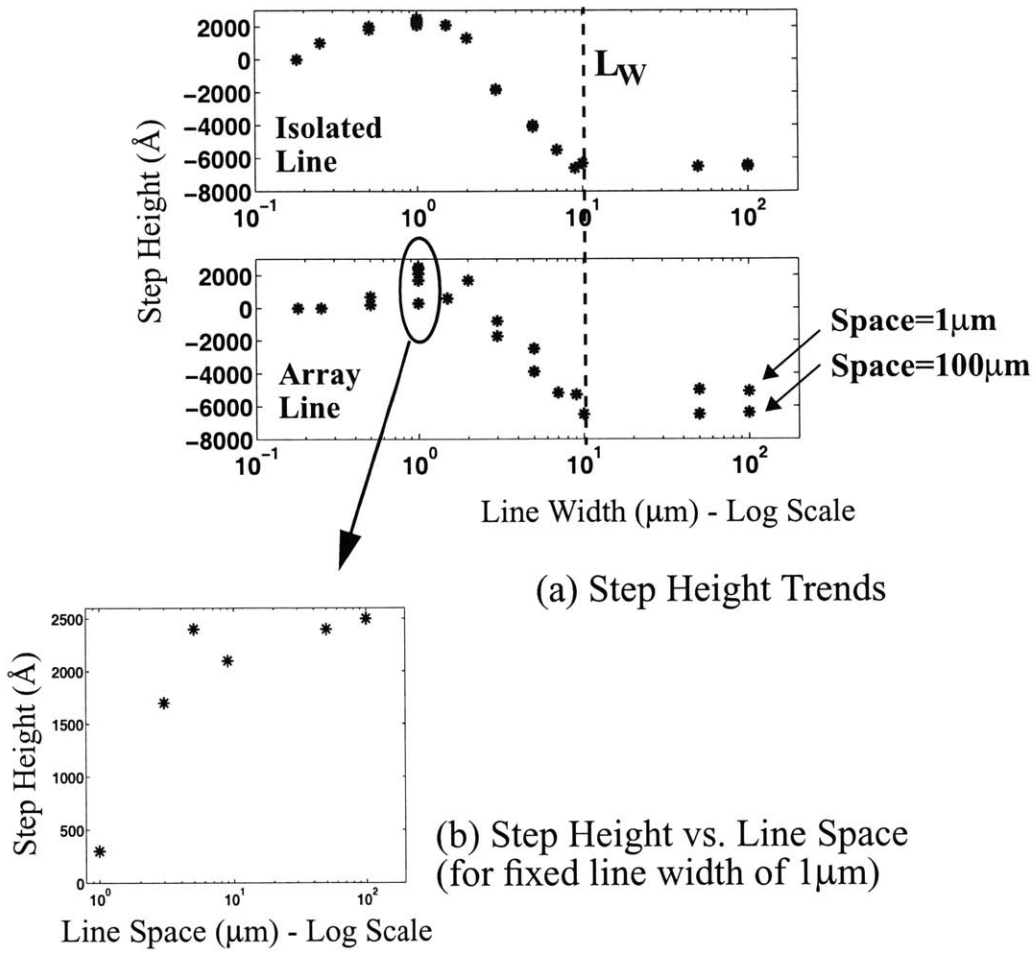


Figure 4.13: Line Space Effect and Interactions with Line Width: Plating Experiment B

In addition to the two experimental data sets described here, we also have examined plating profile trends using additional alternative electroplating recipes and processes. Trends for step and array height as functions of line width and line space are seen in all of these processes. A summary of these additional results can be found in [19].

4.4 Pattern Dependent Model Development: Incorporating Physical Effect

We have seen that indeed there are trends in electroplating that depend on the underlying layout parameters of line width and space. The next step is to develop a model that captures the surface topography variation. Instead of developing a physical model, our approach is to develop a response surface regression model that captures the variation of step height and array height as a function of line width and line space. This approach enables us to achieve the goal of chip-scale simulation; a first-principles physics based numerical simulation approach would not be practically feasible for chip-scale simulations, given the current state of the development of these models. In addition, there is considerable debate in the literature regarding the physics of the electroplating, as noted in the following sections.

In previous work, we attempted to capture the plating topography variation using a purely empirical polynomial fit [19] using the following formulas for step height and array height:

$$SH = a_S W + b_S S + c_S W^2 + d_S W^3 + e_S W \times S + Const_S \tag{4.1}$$

$$AH = a_A W + b_A S + c_A S^2 + d_A S^3 + e_A W \times S + Const_A \tag{4.2}$$

where SH is step height, AH is array height, W is line width, and S is line space. This formulation captures the basic trends and gives reasonable results in terms of fitting to data. However, there is no physical basis for choosing model parameters such as W^3. The model is also found to give somewhat poor performance in capturing the superfill effect for fine features.

Thus, in the next section, we examine the current literature on copper electroplating mechanisms, especially on superfill, to derive response surface model parameters that are more physically motivated and that can better capture the observed plating behavior. The intent is not to make judgements as to the validity of any proposed physical mechanisms or models, nor to extend these models, but rather to survey existing models and mechanisms of physical/chemical behavior in electroplating so that we can derive response surface model variables with better compatibility to the underlying physics. We term the resulting plating model a "semi-physical" model for this reason.

4.4.1 Basic Governing Principles in Electroplating

The electroplating process has been in practice for many decades for plating various metals such as gold, silver, aluminum, nickel, and copper on a wide variety of substrates or work pieces. The basis of the electroplating process, the law of electrolysis, was formulated by Faraday in 1833 and still serves as the basic governing mechanism in electroplating. As described in Chapter 1, the product of plating time and current density determines how much copper is deposited on the wafer surface. The governing equations can be stated as follows:

$$J = \sigma E \tag{4.3}$$

$$J = -\sigma \nabla \phi \tag{4.4}$$

$$\nabla^2 \phi = 0 \tag{4.5}$$

where J is current density, σ is conductivity, E is electric field, and ϕ is electric potential. Current density is directly proportional to electrical field which can be expressed as the gradient of the electric potential. Using the poisson equation in Equation 4.5 and necessary boundary conditions, the electrical potential can be determined and the current den-

sity can be found. Then, the amount of copper deposited is simply found using Faraday's law which states that the amount of copper deposited on the cathode electrode is directly proportional to the current delivered through the system.

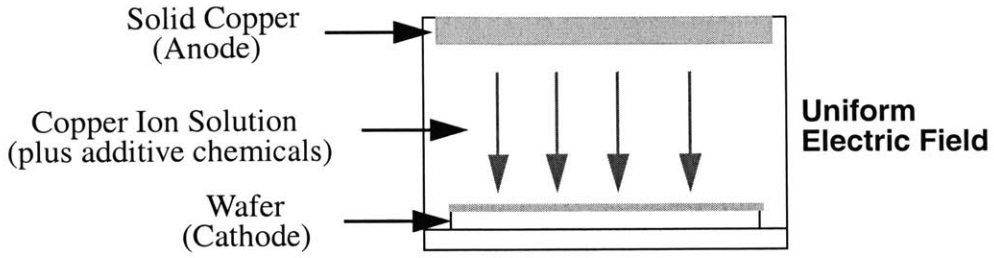


Figure 4.14: Basic Mechanism for Blanket Wafer

Let us examine different cases of trench features to identify what layout parameter may influence the deposition rate. Shown in Figure 4.14 is a simplified drawing of an ideal electroplating system for the case of a blanket wafer. Since the conduction surface at the wafer is flat, there is uniform electrical field across the wafer, and thus there would be the same rate of copper deposition everywhere. In the case of a patterned wafer as shown in Figure 4.15, the electric field is not uniform across a trench feature and causes varying deposition rate at different locations. There is a convergence of electric field near the top corners of the trench and the higher electric field causes higher deposition rate at the top corners. While the electric field converge at the top corners of the trench, the bottom of the trench sees a divergence of electric field and has slower deposition rate compared to the top of the trench. Furthermore, the possible depletion of copper ion species inside a trench may reduce the deposition rate further as one goes deeper into the trench. This depletion is more likely in a narrower trench.

A key concern in plating is void formation in trenches; the faster deposition rate at the top corners compared to the (possibly reduced) rate within the trench closes the trench

even before the trench is completely filled. If the trench width is wider, as seen in Figure 4.15b, the bottom of a trench receives more electric field with less chance of copper ion depletion, and is deposited similarly to the field region. Thus for a wide feature, conformal deposition occurs and the as-plated step height is close to the initial trench depth.

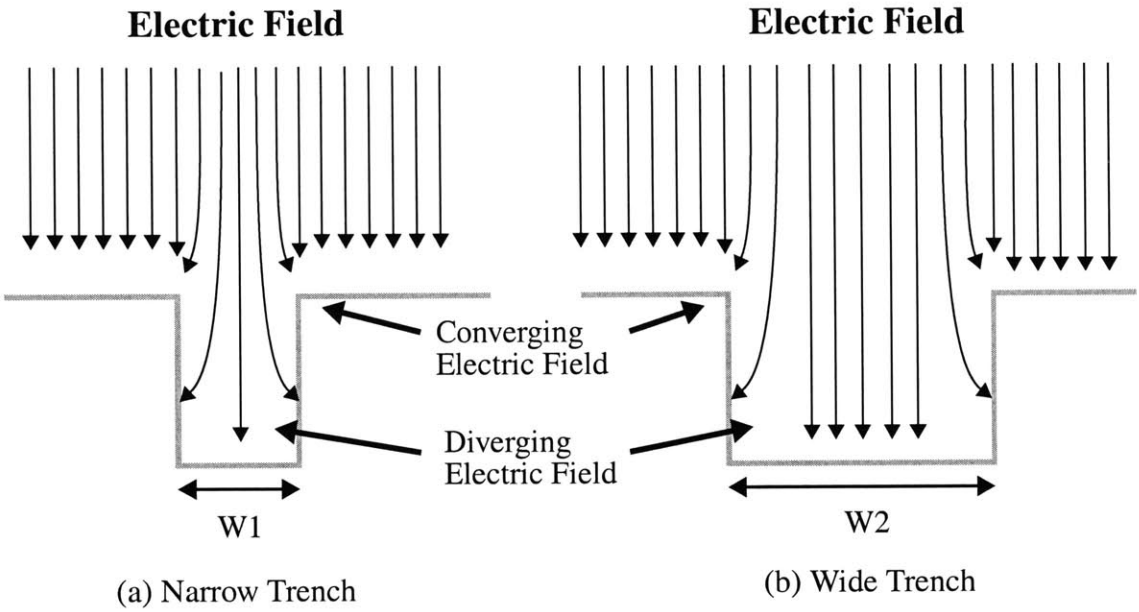


Figure 4.15: Basic Mechanism for Different Trench Width

We can infer from the behavior of electric fields within different feature sizes that the deposition rate will depend on the line width as illustrated in Figure 4.16. Qualitatively, the deposition rate on the bottom of the trench is reduced as the width of the trench is decreased. In addition to the line width effect, a line space effect can also be inferred by observing that the electric field converges more strongly on the sharp angle of a narrow space than on a wide space where the field lines are more uniform across.

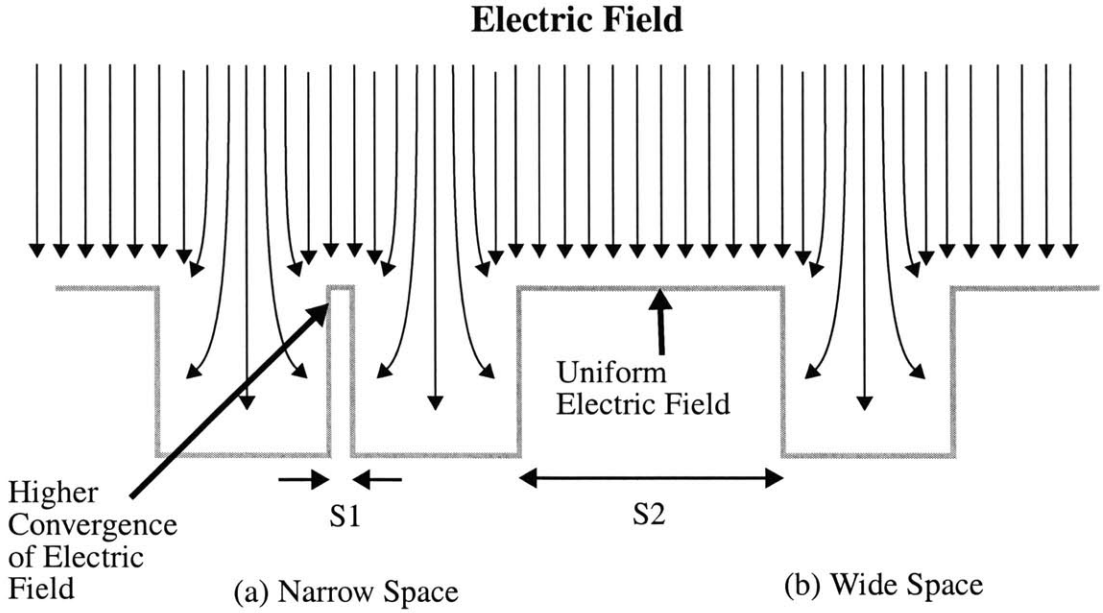


Figure 4.16: Basic Mechanism for Different Spacing Width

The examination of the basic electric field dependence of electroplating indicates that indeed the plating should depend on both the line width and space, as we have seen in our data for step height and array height variations as a function of line width and line space. Thus, we will include line width and line space as fundamental variables in our model. The next step is to examine the superfill effect, in which the trenches fill more quickly than the tops of the features, to identify what layout factors influence this mechanism.

4.4.2 Superfill Electroplating Mechanisms

The current copper electroplating requirement to fill sub-micron features (e.g. 0.13μm) without any voids in trenches is not achieved with traditional electroplating method dependent primarily on the electric field effects and possible depletion of copper ions in trenches described in the previous section. The traditional plating recipes are found to cause void problems in sub-micron features. To resolve this problem, the industry has developed bottom up fill or superfill behavior in electroplating where deposition starts at

the bottom of the trench and moves upward, thus eliminating any voids [4]. This superfill behavior is engineered by introducing additive chemicals in the plating solution known as accelerators and suppressors. Accelerators are catalytic molecules that contain pendant sulfur atoms [10] (e.g. sulfactants) that are adsorbed on the surface and increase the local deposition rate. Suppressors are polymers such as polyethylene glycol that reduce the local deposition rate when adsorbed to surface. Another class of suppressors are known as levelers, and these act to suppress the current density, and thus modify deposition rate.

The concentration of each additive in the plating bath solution determines whether superfill is achieved or not, and the degree of superfill. The exact mechanism by which the additive chemicals modify the deposition rate is not well understood; there are many theories and proposed mechanisms regarding electroplating physics and the bottom up fill of trenches [4, 10, 11, 12, 26-30]. However, the various proposed mechanisms fall into two general categories. One set of theories is based on diffusion-adsorption, and the other set is based on additive-accumulation. Our goal is not to propose or develop a physical model of electroplating mechanisms, but rather to examine the available and proposed models in the literature so that we can relate the physical mechanisms to our empirical model and derive appropriate model parameters for use in an efficient chip-scale pattern dependent model.

A simple pictorial representation of the diffusion-adsorption mechanism is shown in Figure 4.17. In the proposed diffusion-adsorption mechanisms [4, 11, 26, 27, 31], there are numerous assumptions and observations, but the key assumed mechanism is that suppressors reduce the kinetic rate of copper deposition at the wafer surface, and thus any suppressor concentration gradients due to diffusion of the suppressor also affect the deposition rate of copper. Since the bottom of a trench is less accessible to the bulk solution compared to the top of the trench, the trench bottom is "less" suppressed and filling starts from the bottom. We can infer from this proposed mechanism that the suppressors

are less accessible for trenches with higher aspect ratios, where aspect ratio is the trench depth divided by trench width. For deeper trenches or narrower lines, the suppressors will have more difficulty in diffusing into the trenches. West [27] and Cao [11] also state that the prediction of copper deposition depends on the aspect ratio of the trench.

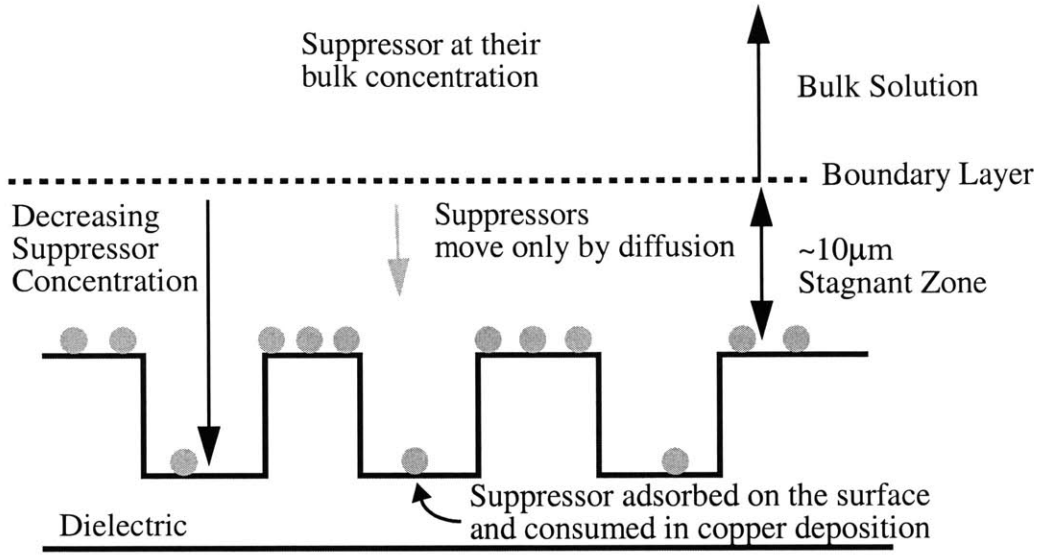
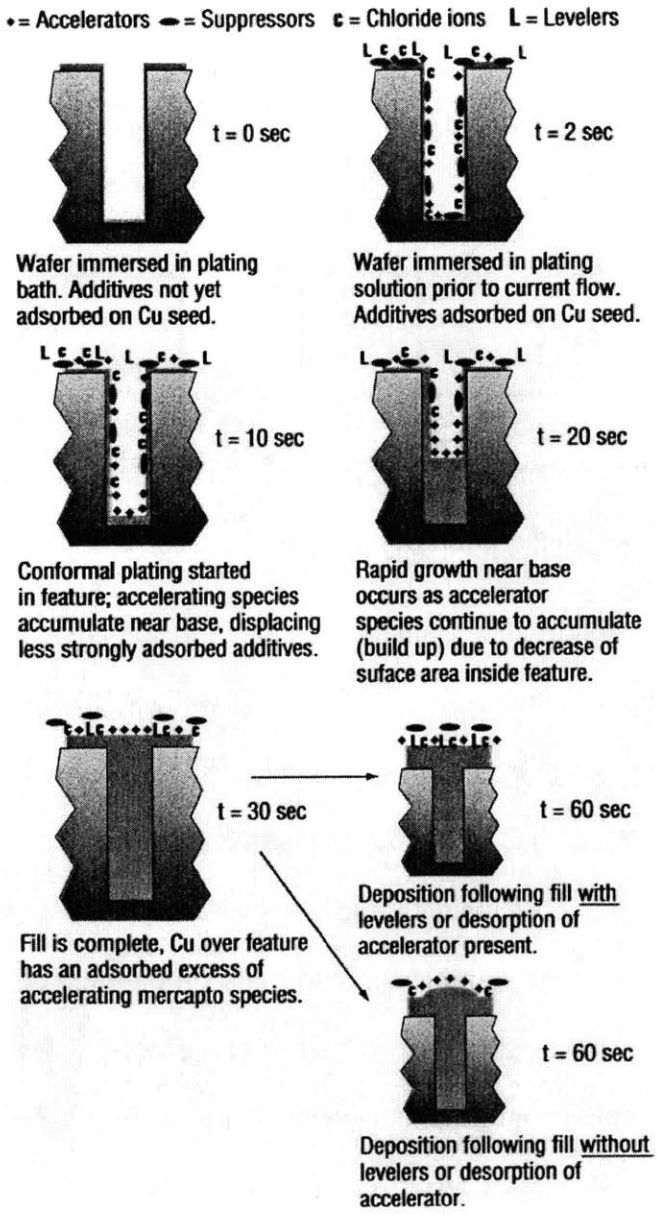


Figure 4.17: Diffusion-Adsorption Based Model Proposed by IBM [4]

An alternative to the diffusion limited mechanism in the diffusion-adsorption theory is an additive-accumulation theory, which argues that the diffusion-adsorption theory is not sufficient to explain the dynamics of overfill (e.g. bulging effect) after a trench is filled to the top [12, 28]. Reid [10], from one of the leading suppliers of copper electroplating tools, explains the general additive-accumulation mechanism with a pictorial diagram as shown in Figure 4.18. Once a wafer is immersed into the solution bath, an equilibrium condition is achieved where additives are adsorbed on the surface before voltage or current is applied. As plating starts with a conformal deposition of copper, accelerators accumulate on the bottom of trench and displace less strongly adsorbed suppressors. Then, since we have more accelerators and less suppressors in the bottom of trench, deposition rate

increases on the bottom, and as more copper is deposited from the bottom, more accelerators accumulate due to decreasing surface area inside the trench. Once the trench is filled up, the accumulated accelerators cause the continued copper deposition resulting in the bump or bulging effect. One of the key assumptions for this mechanism is that, unlike in the diffusion-adsorption theory, there is no consumption of additives on the surface of wafer.



Source: Solid State Technology, July 2000 [10]

Figure 4.18: Illustration of Additive Adsorption-Accumulation Behavior During Electroplating Fill

Other literature [12, 28, 29, 30] also propose similar accelerator-accumulation mechanisms with slightly different emphasis and treatment of the role of accelerators and suppressors on the overall deposition kinetics. Still, the variants of the accelerator-accumulation mechanism indicate that the increase of the accelerators is directly related to the decrease of the surface area within a trench, which is related to the aspect ratio of a feature as shown in Figure 4.19. If a trench is deep, there are more accelerators that can accumulate from the side walls as the trench is filled, and if a trench is narrow, there is a faster percentage decrease in the trench width which causes higher accelerator concentration relative to displaced suppressor concentration on the bottom of the trench.

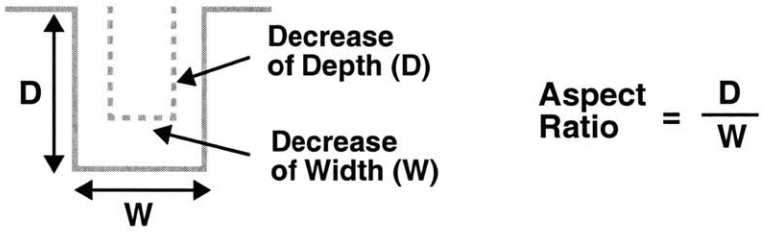


Figure 4.19: Accelerator-Accumulation: Dependence on Aspect Ratio

In both of these proposed mechanisms – diffusion-adsorption and additive-accumulation – the aspect ratio (depth/width) is found to have a dominant impact on the superfill effect. Since trench depth is typically fixed for a given process, we find that 1/(width) has a direct influence on the deposition rate and thus on the final surface profile. We will thus also explore the use of the term 1/w in our semi-empirical model development to capture as-plated surface topography.

4.5 Semi-Empirical Pattern Dependent Model

In this section, we combine the findings of key layout parameters and their forms to develop a semi-empirical model. It is conceivable to derive a model based on the first prin-

ciples of electroplating including superfill to capture the resulting surface topography of step height and array height. However, this physics-based model approach, which typically uses numerical simulations to determine profile evolutions of copper deposition, is presently too time-consuming and not practical for the wide range of pattern combinations (line width or line space) possible in realistic circuits.

Rather, what we are proposing in the model development is a multivariate response surface model that captures the surface topography variation for an electroplating process as a function of underlying layout parameters. A response surface model is appropriate in our case since our goal is to capture the surface topography variation in an effective manner and apply the model to any arbitrary layout across an entire chip for a chip-scale simulation. Previous descriptions of both physical mechanisms of electroplating and the observed data indicate that line width and line space both play an important role in determining the degree of step height and array height. However, the physical mechanisms of the basic principles in electroplating process and the superfill models (e.g. diffusion-adsorption and additive-accumulation) highlight competing kinetic explanations for the deposition, where the former hinders the filling of small trenches and the latter enhances the fill for such features. Thus, to capture surface profiles that result from these two competing processes, we make use of the forms of the layout parameters that are found dominant in both mechanisms: width, space, 1/width, and width*space interactions. The second order terms (W^2 and W^{-2}) are added to capture any higher order effects that may not be captured by W and W^{-1} terms only. Thus our starting form of the model is as follows:

$$Height \sim W + W^2 + W^{-1} + W^{-2} + S + W \cdot S + Const \tag{4.6}$$

where *Height* is either step height and array height, W is line width, and S is line space. Using Splus statistical analysis software, the significance of each model factor is deter-

mined across five different data sets; the following response model is found to be most effective at capturing array height and step height variations:

$$AH = a_A W + b_A W^{-1} + c_A W^{-2} + d_A S + e_A (W \cdot S) + Const_A \tag{4.7}$$

$$SH = a_S W + b_S W^{-1} + c_S W^{2} + d_S S + e_S (W \cdot S) + Const_S \tag{4.8}$$

where AH is array height and SH is step height as defined earlier. As W becomes small, the superfill effect is dominant and we see that the $1/W$ and $1/W^2$ terms become dominant. As W increases, conformal fill is dominant, and we see that $1/W$ and $1/W^2$ terms become small and the W, S, and $W \cdot S$ terms become dominant to capture the conformal trend. A superfill electroplating process typically used for current copper metallization exhibits both superfill and conformal regimes depending on the feature size, as seen in the data of Section 4.3, and both regimes are captured in the model form instead of modeling for two regimes separately.

When compared to the original polynomial form, the new model form does significantly better at capturing data and trends. In particular, the new model form for the array height shows reduction of RMS error by half. This response surface model is tested over many sets of data from different plating recipes and different tools, and all fits are generally under 500 Å of RMS error. Kelly [32] also found by empirical testing that the 1/w term is more effective in capturing superfill effect. Statistical analysis and model fits are considered in the next section to demonstrate model parameter significance and overall data fits.

4.6 Model Fit and Model Coefficient Extraction

Before a regression analysis is performed on the step height and array height data, the associated line width and line space for some data points must be filtered. The data trends in Section 4.3 shows that beyond the critical line width of L_W and critical line space of L_S, which in our case is 10 μm for both, the step height and array height behavior remain constant; specifically, the step heigh is equal to the trench depth, and the array height is zero. Thus, any line widths that are greater than L_W are assigned the value of L_W as the line width, and likewise, any line spaces that are greater than L_S are assigned the value of L_S as the line space. A step height data that is obtained from 50 μm line width and 50 μm line space array region is assigned an equivalent line width of 10 μm and line space of 10 μm. The regression is performed using the adjusted line width and sapce, and an example of the line width and line space transformation is shown in Table 4.1.

Table 4.1: Example of Line Width and Line Space Transformation

Line Width	Line Space	Transformed: Line Width	Transformed: Line Space
0.5	0.5	0.5	0.5
2	2	2	2
20	5	10	5
20	20	10	10
50	50	10	10

Table 4.2 summarizes the result of the regression for the step height data from the plating experiment A; the model coefficients as well as a RMS error and the significance, are indicated. As the step height model fit is shown in Figure 4.20 as a function of line width, the overall trend is well captured with a model R^2 of 0.9793 and a fitting RMS error of

around 330 Å. Also, the significance test (Pr(>|t|)) indicates that the model coefficients are all seem to be highly significant (to greater than 99.99% confidence).

Table 4.2: Step Height (SH) Fit

SH Model Coefficients	Extracted Values	Standard Error	t value	Pr(>|t|)
a_S	-663.18	108.05	-6.14	0.0000
b_S	-357.23	80.74	-4.42	0.0001
c_S	60.45	10.50	5.76	0.0000
d_S	115.56	17.26	6.69	0.0000
e_S	-69.11	9.16	-7.54	0.0000
$Const_S$	1075.22	245.02	4.39	0.0001
RMS Error = 327Å R^2 *= 0.9793* *Overall Significance: P Value = 0*				

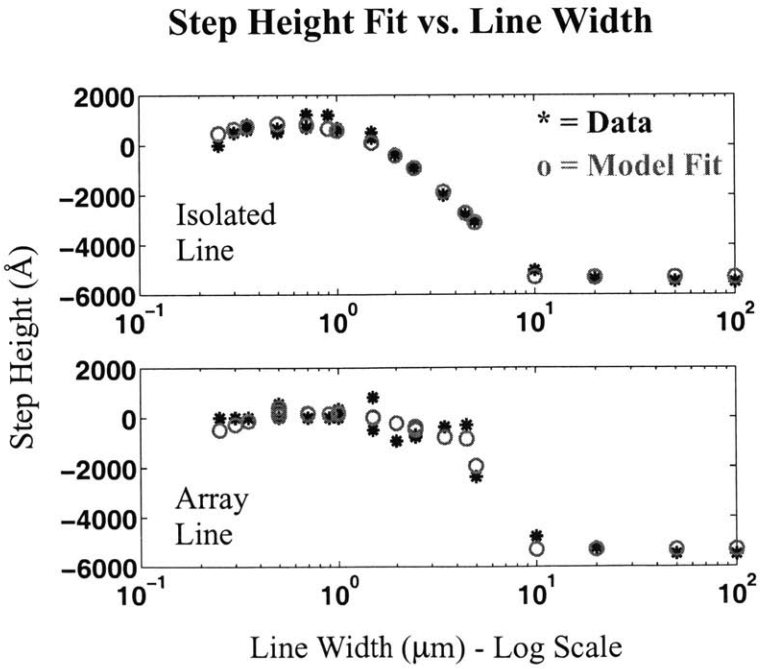


Figure 4.20: Step Height Model Fit vs. Line Width: Plating Experiment A

In the array height fit of Table 4.3, the constant and S (d_A) terms are only marginally significant, and the $1/W$ (b_A) term is not significant. Thus, in this particular case, coefficient b_A is set to zero, and the model is refitted to data using the simplified model form:

$$AH = a_A W + c_A W^{-2} + d_A S + e_A (W \cdot S) + Const_A \tag{4.9}$$

The obtained new set of model parameters, summarized in Table 4.4, shows that the simplified model form is more significant and still captures the trend well. Our general model framework can be simplified in some cases depending on the electroplating process, and the model fit discovers this simplification as a natural part of the regression.

The model fit vs. data is shown in Figure 4.21 with the "better" simplified model. The fit for the array height vs. line width captures both the superfill trends for small features and the conformal fill trends for large features. The RMS error for the model fit is about 424 Å, and the R^2 value is 0.9546.

Table 4.3: Array Height (AH) Fit

AH Model Coefficients	Extracted Values	Standard Error	t value	Pr(>|t|)
a_A	-1015.55	195.57	-5.19	0.0001
b_A	-476.05	601.45	-0.79	0.4390
c_A	360.38	125.58	2.87	0.0102
d_A	-135.79	92.51	-1.47	0.1594
e_A	102.09	17.48	5.84	0.0000
$Const_S$	1259.97	742.70	1.70	0.1070
RMS Error = 428Å *R^2 = 0.9561* *Overall Significance: P Value = $1.41*10^{-11}$*				

Table 4.4: Array Height (AH) New Model Form (without 1/w term) Fit

AH Model Coefficients	Extracted Values	Standard Error	t value	Pr(>|t|)
a_A	-887.3203	108.4705	-8.1803	0.0000
b_A	0	NA	NA	NA
c_A	263.8060	29.4506	8.9576	0.0000
d_A	-128.2050	91.1012	-1.4073	0.1755
e_A	93.4935	13.5594	6.8951	0.0000
$Const_S$	717.0528	281.9886	2.5428	0.0199
RMS Error = 424Å R^2 *= 0.9546* *Overall Significance: P Value =* $1.773*10^{-12}$				

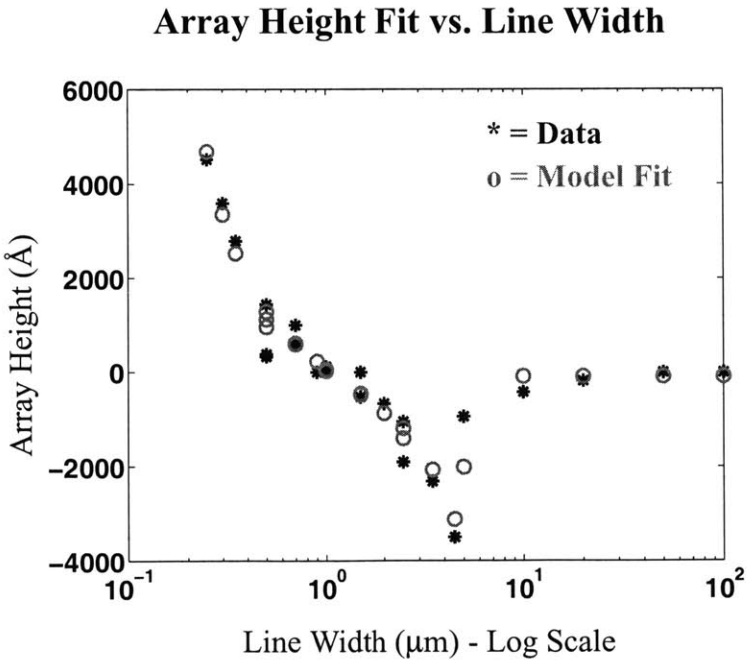


Figure 4.21: Array Height Model Fit vs. Line Width: Plating Experiment A

The array height and step height models are tested across various data sets from different tools and recipes, and have found to be able to capture overall trends with about 500-600 Å of RMS errors or less. We show one additional regression result for step and array height model fits for plating experiment B. The step height fit result is summarized in Table 4.5, and shows all model variables are significant with a RMS error of 564 Å and the R^2 value of 0.9769. The model fit vs. data is shown in Figure 4.22, and the trend is well captured by the model fit.

For the array height model, the $1/W^2$ (c_A) term is found to be insignificant while the $1/W$ (b_A) term is significant. This is unlike the previous case of the experiment A where the opposite was true. In addition, the $W \cdot S$ (e_A) term is found to be insignificant as well. Thus, these coefficients are set to zero, and the model is refitted to data, and the result is summarized in Table 4.6. The RMS error for the model fit is 556 and the R^2 value is 0.9634. The model fit vs. data using the simplified model form is shown in Figure 4.23 as a function of line width, and shows a good correspondence between the two.

Table 4.5: Process B: Step Height (SH) Fit

SH Model Coefficients	Extracted Values	Standard Error	t value	Pr(>|t|)
a_S	-2056.2462	152.3671	-13.4953	0.0000
b_S	-853.9300	97.2350	-8.7821	0.0000
c_S	118.3951	12.9004	9.1776	0.0000
d_S	116.9125	29.7870	3.9249	0.0003
e_S	-29.6537	5.5414	-5.3513	0.0000
$Const_S$	4067.0828	392.8965	10.3515	0.0000
RMS Error = 564Å *R^2 = 0.9769* *Overall Significance: P Value = 0*				

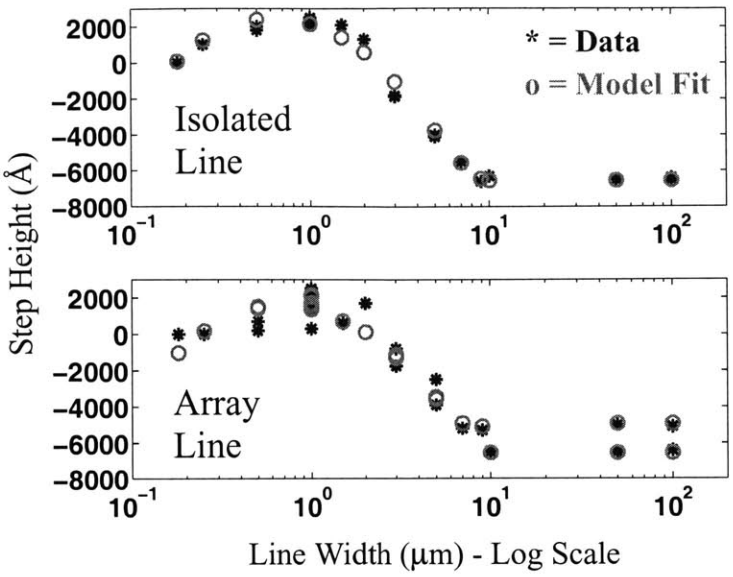


Figure 4.22: Step Height Model Fit vs. Line Width: Plating Experiment B

Table 4.6: Process B: Array Height (AH) Fit

AH Model Coefficients	Extracted Values	Standard Error	t value	Pr(>|t|)
a_A	-53.8966	37.5853	-1.4340	0.1678
b_A	1975.7463	112.7834	17.5181	0.0000
c_A	0	NA	NA	NA
d_A	151.6045	32.1776	4.7115	0.0002
e_A	0	NA	NA	NA
$Const_S$	-1074.7376	301.2698	-3.5674	0.0021
RMS Error = 556Å $R^2 = 0.9634$ *Overall Significance: P Value =* $7.983*10^{-14}$				

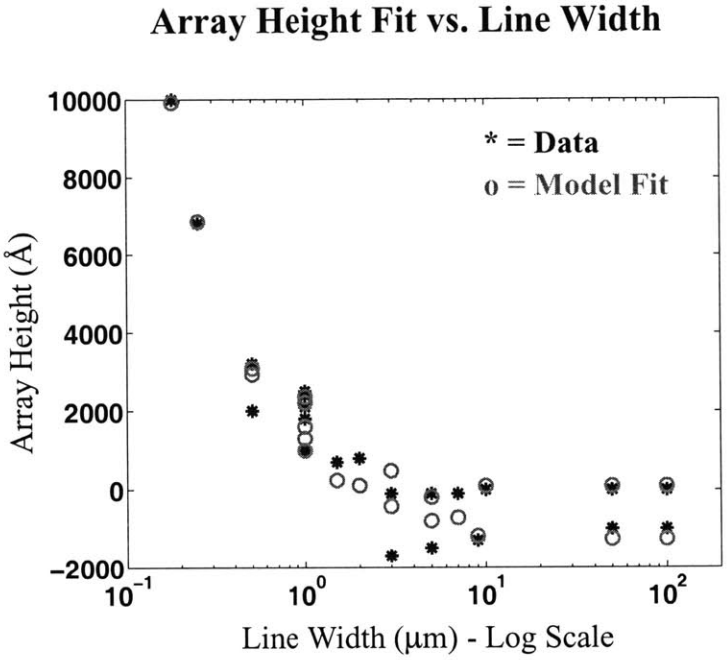


Figure 4.23: Array Height Model Fit vs. Line Width: Plating Experiment B

In this chapter, we have shown the pattern dependent behavior of as-plated surface topography, capturing the basic trends and making key observations of the dependence on line width and line space. In an attempt to capture the trends through surface regression model, basic principle and various proposed superfill mechanisms are examined to identify key layout factors that cause non-uniform deposition rates for patterned features, and the examination of the topography dependency helped determine the relevant form (e.g. *W* or *1/W*) of model variables. The identified layout parameters and the variants of their forms are used to formulate an optimal set of model variables by fitting across various sets of data from different recipe settings and tools. The model shows good correlation between the data and the fit, and captures both the superfill effect for fine features and conformal fill for large features. The use of the model and the extracted model coefficients enables us to perform chip-level simulations which is the focus of the next chapter.

Chapter 5

Chip-Scale Simulation and Prediction of Surface Topography in Electroplating

This chapter describes how the semi-empirical plating model presented in Chapter 4 is applied to perform chip-scale simulation for surface topography variation. To perform the step height and array height simulations across an entire chip, we need line width and line space information across an entire chip. It would not be practical or computationally efficient to make use of each individual line and space in an entire chip. Thus, we need a methodical way to obtain appropriate layout parameters for the purpose of chip-scale simulation. Once we obtain the relevant layout information for a particular chip, the chip-scale simulation procedure is carried out to obtain the surface topography variation for that chip. The chip scale simulation is demonstrated for a complex layout (different than that used to calibrate the plating model) to predict chip-scale topography variations, which is the goal of our overall characterization and modeling methodology overviewed in Section 2.1.

This chapter first describes a calculation method used to obtain average topography on a coarsely discretized grid through the concept of average array height and average step height. Then, the layout parameter extraction is illustrated where distributions of feature sizes are extracted from the layout within this grid. The use of the extracted layout parameters and the chip-scale simulation procedure for step and array height are outlined, followed by the field region thickness variation modeling, which is a major extension to the feature model of Chapter 4. Finally, we demonstrate the chip-scale simulation results for the same layout used to calibrate the model and for another random layout. An evaluation of errors introduced by this averaging approximation is also presented.

5.1 Overview of Average Step and Array Height Calculation

The chip-scale simulation of electroplated topography is done by computing a generalized "average" array height and step height for a grid cell, where grid cells are equally divided small regions on a die. The procedure for obtaining relevant layout information and using this information to perform chip-scale simulation is explained in detail in the next two sections. In this section, an example is first used to illustrate the calculation of the average or effective array height and step height for a given grid cell. This method is the key enabler for efficient chip-scale simulation.

In this work, we choose a grid discretization using 40 μm x 40 μm cells. This is a trade-off between several considerations. First, we would prefer to discretize the chip surface as finely as is reasonable to do, approaching the size of features of relevance to the electroplating model previously discussed. Second, however, this discretization should not be too fine, as we need to average across enough features to account for transition or near-neighbor effects. Third, a typical chip may be 20 mm x 20 mm in size, so a 40 μm cell edge length results in a 500 x 500 array for the entire chip. It is feasible to maintain information for each cell without extraordinary memory requirements at this level of discretization. Finally, the 40 μm x 40 μm discretization is compatible with the needs of subsequent CMP simulation.

An example cell is shown in Figure 5.1, consisting of two regions with different copper line widths and spaces. Region *A* occupies the left 24 μm wide portion of the cell, and region *B* occupies the right 16 μm portion of the 40 μm wide grid cell. In the electroplated profile labeled "Case 1" shown in the lower part of Figure 5.1, region *A* has a plated AH of -2000 Å and SH of -3000 Å, and region *B* has an AH of 0 Å and SH of -5000 Å.

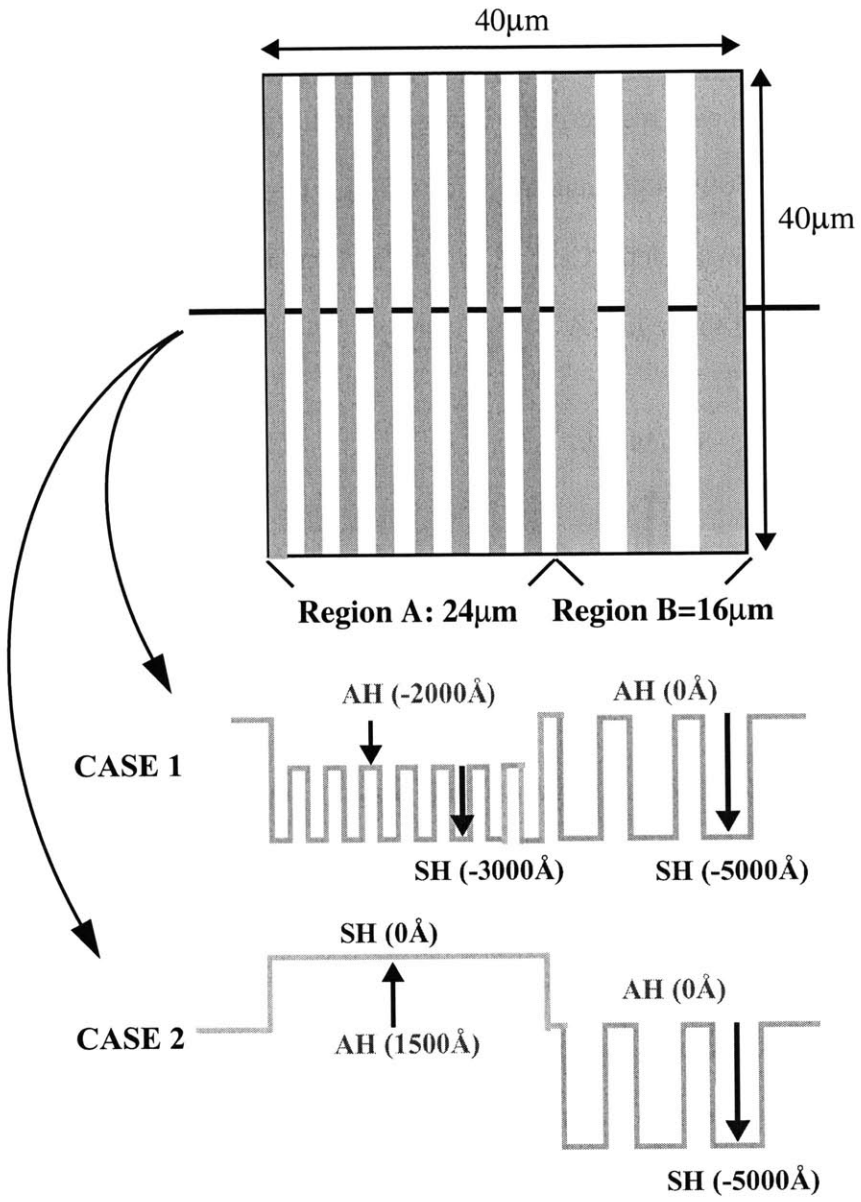


Figure 5.1: Example Grid Cell and Cross Sectional View of Plated Profile

In the simplest approach, we might find an "average" array height and step height for this grid cell by computing the area-weighted averages as follows:

$$AH_{Avg} = (-2000Å \times 24\mu m + 0Å \times 16\mu m) / 40\mu m = -1200Å \quad (5.1)$$

$$SH_{Avg} = (-3000Å \text{ x } 24\mu m + -5000Å \text{ x } 16\mu m) / 40\mu m = -3800Å \quad (5.2)$$

Thus for Case 1, the AH_{Avg} of -1200 Å and SH_{Avg} of -3800 Å are the average array height and step height for this grid cell, respectively. Using the similar method, we can find a positive AH_{Avg} of 900 Å (= 1500x24/40) and SH_{Avg} of -2000 Å (= -5000x16/40) for the alternative electroplated profile labeled "Case 2" at the bottom of Figure 5.1 which has a pronounced array bulge for the region *A*.

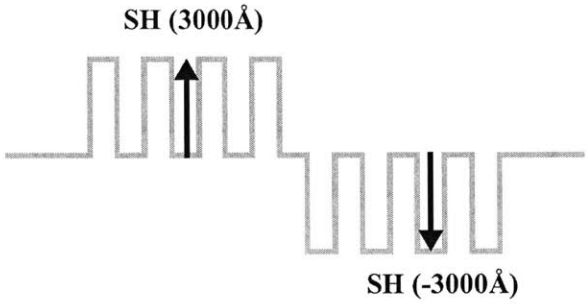


Figure 5.2: Positive and Negative Step Height Cancellation Effect

This simple average must be generalized in an important way, however, to account for positive and negative step heights. A scenario where the effective step height is calculated to be zero even from existing step height topography helps to illustrate the problem. Figure 5.2 shows a situation where half of the grid cell has a positive step height of 3000 Å and the other half has a negative step height of the same amount. Because the two regions cover the same area, the average step height is computed to be zero. A step height of zero suggests that the surface is flat or smooth, but this is not the case here. Thus, we generalized the "average" step height calculation to the following:

$$SH_{Avg} = (|SH_A| \text{ x } Area_A + |SH_B| \text{ x } Area_B) / Total\ Area \quad (5.3)$$

where we take the absolute step height value of each region *A* and *B*, weight by the area occupied by each respective region, and divided by the total area.

5.2 Layout Parameter Extraction

The next challenge is to extract meaningful information from layout geometry data for each cell. As mentioned earlier, a given layout is divided into smaller regions or cells. Figure 5.3 shows an example grid cell for a "random" layout which is seen to contain a variety of feature sizes. In each grid cell in a layout, an arbitrary number of lines and vertical or horizontal line orientations can exist. We are interested in extracting the line width and line space information for each cell.

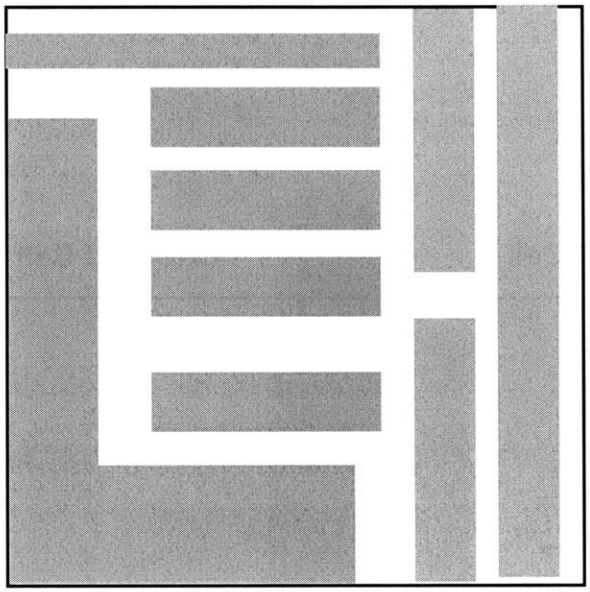


Figure 5.3: Example "Random Layout" Grid Cell

For any given rectangle in a grid cell, it could represent either horizontally or vertically running line. Regardless of its direction, for consistency we require that the shorter dimension of the rectangle be taken as the line width (W) and the longer dimension be taken as the line length (L) as shown in Figure 5.4 for various lines. In a case where the layout object is a polygon, the polygon is split into a set of rectangles, and the same rule applies

in determining which dimension is W and which dimension is L for each rectangle. Some ambiguity remains, as it is possible for a polygon to be subdivided to rectangles in more than one way. For our purposes, any "reasonable" subdivision produced by a layout extraction tool will be considered adequate, given the averaging and other approximations entailed in the chip scale simulation.

It is also possible that a line occupies two neighboring grid cells. In that case, we still use the same definition of width and length, but use the full width and length of the layout object and not the object cut off at the grid box boundaries. If the object is cut off at the grid boundaries of the box, then incorrect line widths are reported which can hinder the simulation result.

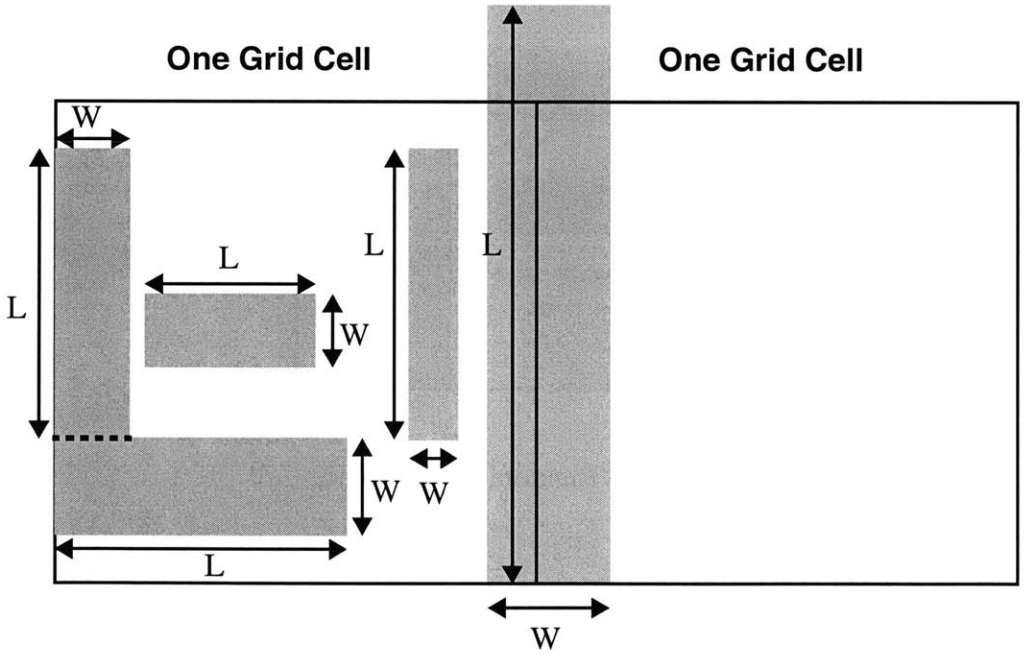


Figure 5.4: Definition of Line Width and Line Length

Using this definition of line width and line length, layout parameter extraction is done for each cell and eventually both step height and array height simulation are performed on

a cell by cell basis. A further comment can be made regarding the size of the grid cell, relative to important electroplating length scales. If the "transition length" of the electroplating process (discussed in Section 4.3.3) is greater than the size of the grid, and if we perform our simulations on a cell by cell basis without accounting for any neighbor cells, then our simulation may suffer as a result. Essentially, the influence of any neighboring environment would be ignored in this case. As stated in the previous chapter, we find that electroplating depends mostly on the feature level and nearest neighbor interactions, and the characteristic "transition length" in electroplating is relatively small, being only a few microns in length. The grid size of 40 x 40 μm is considered to be large enough so that neighboring influence from external cells can be neglected. Within the cell, the averaging procedure will naturally incorporate the effect of nearby structures. Alternative approaches (e.g. using a window larger than the discretization cell for computing feature effects) add complexity but might be useful to consider as future work.

Using the definition of line width and space given above, a layout extractor gives the following layout information for each cell:

- X and Y location of the cell center
- Minimum line width
- Average line width
- Maximum line width
- Average line length
- Copper pattern density

where copper pattern density is defined as the ratio of the area occupied by copper lines within the grid cell (excluding any portion of a line that extends out of the grid of interest) to the total area of the grid cell. In a typical layout, there are many lines of different width within a cell. A simple approach might be to use the average line width and average line space (derived from the copper pattern density and average line width) to perform the

electroplating simulation. If the plating step height and array height were to depend linearly on line width, then an average line width might result in reasonable results. However, the result would be a poor approximation when a cell contains a wide range of line widths, because the array and step heights are found to depend in a non-linear fashion on line widths in Chapter 4.

In this work, we propose to use a binning approximation to the distribution of line widths reported from the layout extractor, and then to use this information to further generalize the computation of "average" array and step heights within the cell. In this method, the layout extractor gives a count of the number of lines having a line width in each bin of the line width distribution. We illustrate this using an example shown in Figure 5.5 having a regular array of lines for simplification. Let us assume that the grid cell has two different pattern regions: region *A* contains eight lines of width 1.5 μm and space 1.5 μm, and region *B* contains three lines of width 4 μm and space 2 μm. Thus, the minimum width is 1.5 μm and maximum width is 4 μm. The average width is (8*1.5 + 3*4)/11 which is 2.182 μm. For our example, the total area occupied by copper is (8*1.5*40 + 3*4*40) which is 960 μm^2, and the total area of the grid cell is 40*40 which is 1600 μm^2. Thus the copper pattern density reported from the layout extractor is 960/1600 which is 0.60 or 60%.

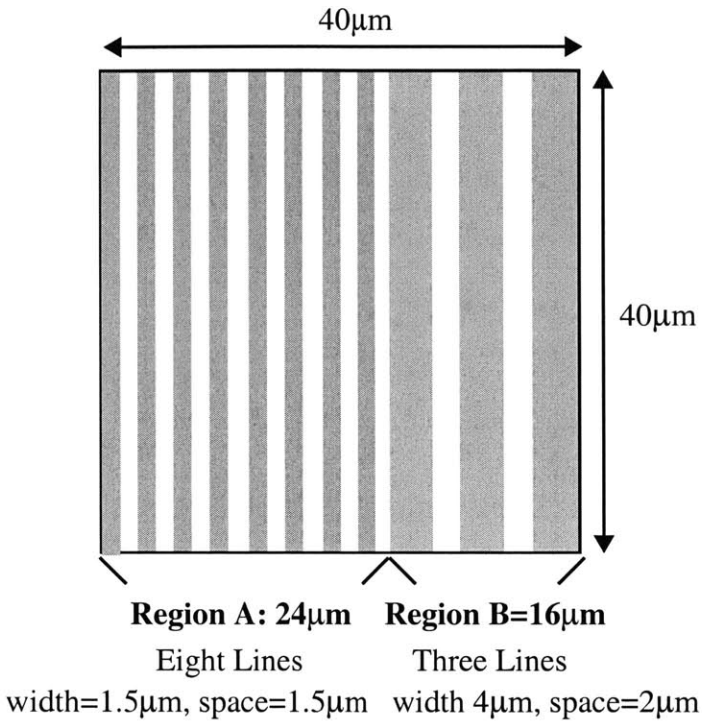


Figure 5.5: Example Grid Cell for Binning Calculations

The number of bins to use to represent the distribution of line widths, as well as the cut off line widths between bins, are obtained by observing the step and array height trends as a function of line width. The trend is replotted in Figure 5.6 with the cutoff values used in this work shown with vertical dotted lines. The cutoff values of line width are chosen so that the non-linear trends can be approximately linearized within each bin. Fine features are sampled more frequently since this is the regime where superfill causes a significant bulging effect. The last bin starts at a line width of 10 μm, which is equal to the critical line width, L_W, found earlier. Since lines with widths greater than L_W behave the same way, all lines wider than this are reported in the last bin.

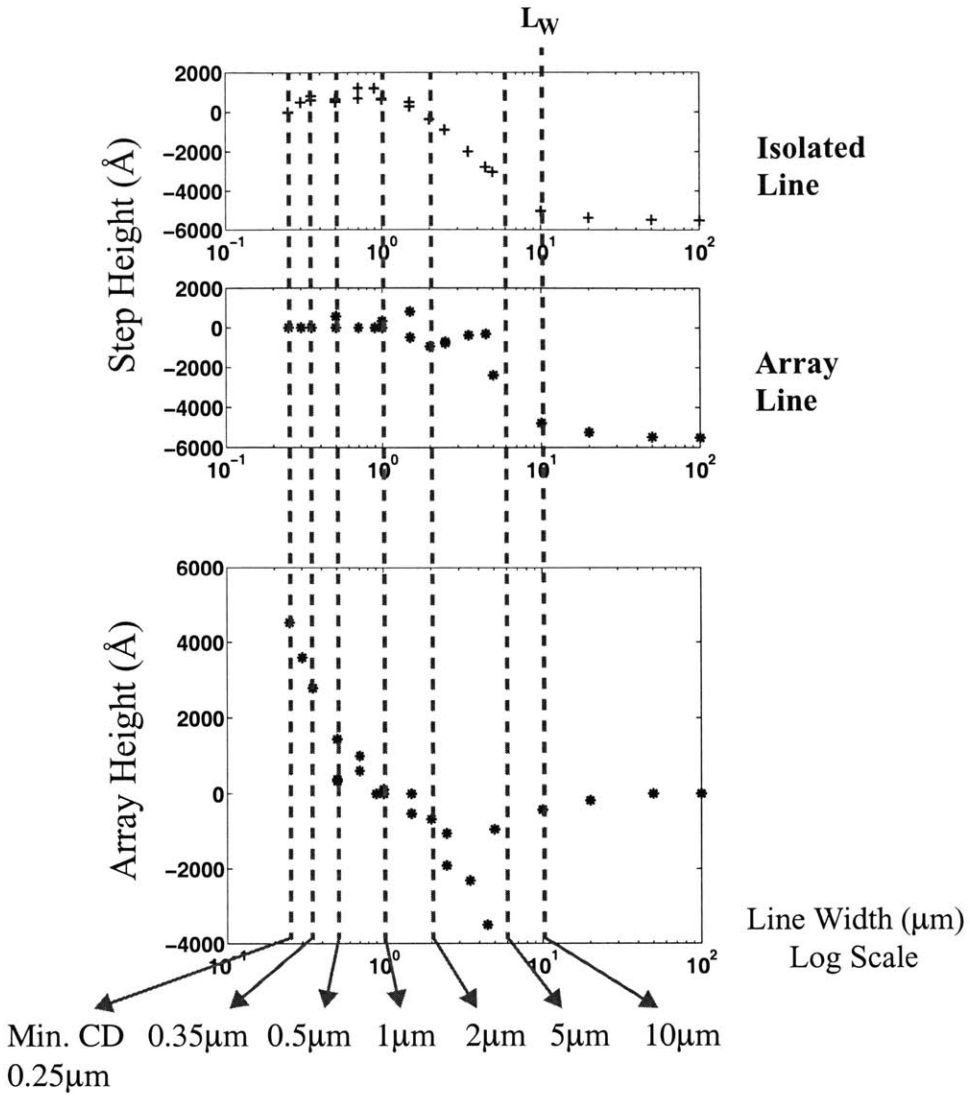


Figure 5.6: Step Height and Array Height vs. Line Width and Bin Cutoffs

For the line width bins, the cut-off line widths are specified below:

- Minimum critical dimension (CD) in design <= Bin 1 < 0.35 μm
- 0.35 μm <= Bin 2 < 0.5 μm
- 0.5 μm <= Bin 3 < 1 μm
- 1 μm <= Bin 4 < 2 μm
- 2 μm <= Bin 5 < 5 μm
- 5 μm <= Bin 6 < 10 μm
- 10 μm <= Bin 7

The result of the layout extraction for our example cell in Figure 5.5 is summarized in Table 5.1. It should be noted that the current layout tool is limited in only calculating information on the line width, but not on the line space. Thus, line space distributions are not explicitly reported. However, using the line width and copper pattern density, an average line space can be derived for each bin. This is reasonable approximation, in the case of line space, as the array and step heights are linear functions of S (Equations 4.7 and 4.8), unlike the strongly nonlinear dependence on W which motivated the use of bins for line width. In Table 5.1, we see that eight lines are reported in Bin 4, and three counts in Bin 5 for our example, in addition to other layout information.

Table 5.1: Example Layout Extraction

Layout Parameter Extracted	Values
Min. W	1.5μm
Avg. W	2.182μm
Max. W	4μm
Avg. Length	40μm
Layout Copper Density	60%
Bin 1	0 Count
Bin 2	0 Count
Bin 3	0 Count
Bin 4	8 Counts
Bin 5	3 Counts
Bin 6	0 Count
Bin 7	0 Count
Total Count (of lines in all bins)	11
X, Y Location of the Grid Cell	X_o, Y_o

5.3 Chip-Scale Simulation of Array Height and Step Height

The extracted bin layout parameters are input to the semi-empirical plating model to perform the simulations for each grid cell in the chip. This section describes the procedure

for performing chip-scale simulation based on the binned extracted layout information. The key idea is to generalize the "average" step and array height as a weighted average of plating heights across the binned layout information.

First, we assign one representative value for the line width for each bin, as shown in Table 5.2, by using the mean of the low and high cutoff values for that bin. For example, since our second bin is from a line width of 0.35 μm to 0.5 μm, 0.425 μm is used as the representative value of the width for that particular bin. One exception to this rule is the assigned width for Bin 7 where the characteristic length, L_W, is used as the representative line width.

Table 5.2: Assigned Line Width for Each Distribution

Assigned Width (μm)	Assigned Line Width
W1	(Min_CD + 0.35)/2 = 0.3μm
W2	0.425μm
W3	0.75μm
W4	1.5μm
W5	3.5μm
W6	7.5μm
W7	L_W = 10μm

As stated earlier, the current extractor tool is limited to calculating information on line width only, but not on line space. Thus, we need to derive an average line space from the layout extraction result given. This is done by using the definition of copper patter density, ρ_c, for arrays of lines as indicated in Equation 5.4.

$$\rho_c = \frac{W}{W + S} \tag{5.4}$$

This can be rearranged to give line space S in terms of the available copper pattern density and width:

$$S_i = \frac{W_i(1-\rho_c)}{\rho_c} \tag{5.5}$$

where S_i is the space for i^{th} bin derived from ρ_c and W_i, the i^{th} bin line width. Before the simulation can be performed we need one more piece of information, and that is the area occupied by the lines in each bin as indicated in Equation 5.6:

$$A_i = W_i \cdot N_i \cdot \bar{L} \tag{5.6}$$

where W_i is the assigned line width for the i^{th} bin, N_i is the number of lines in the i^{th} bin, and $\bar{L}$ is the average line length in the grid cell.

Given this preparation, the array height (AH) and the step height (SH) simulations can now be performed. First, the array and step heights are calculated for each bin i as described in Equation 5.7 and Equation 5.8:

$$AH_i = a_A W_i + b_A W_i^{-1} + c_A W_i^{-2} + d_A S_i + e_A(W_i \cdot S_i) + Const_A \tag{5.7}$$

$$SH_i = a_S W_i + b_S W_i^{-1} + c_S W_i^{2} + d_S S_i + e_S(W_i \cdot S_i) + Const_S \tag{5.8}$$

where a_A through e_A and a_S through e_S are the empirically extracted model coefficients for AH and SH, respectively. Once individual array and step heights are found for each bin, the generalized AH and SH are determined by an area-weighted average similar to the method used in the example illustrated in Section 5.1 as follows:

$$AH = \begin{cases} 0 & TotalCount = 0 \quad or \quad \rho_c < 0.01 \\ -H_o & \rho_c > 0.99 \\ \dfrac{\sum_i (AH_i \cdot A_i)}{A} & Otherwise \end{cases} \tag{5.9}$$

$$SH = \begin{cases} 0 & TotalCount = 0 \quad or \quad \rho_c < 0.01 \\ 0 & \rho_c > 0.99 \\ \dfrac{\sum_i (|SH_i| \cdot A_i)}{A} & Otherwise \end{cases} \tag{5.10}$$

where the total area A is the sum of each bin area A_i, or $A = \sum A_i$, as computed in Equation 5.6. The absolute value of SH_i for each bin is used for the reason described in Figure 5.2. A number of special cases must be considered. When the copper pattern density is near zero, or the total count is zero, then there are no lines in that grid cell, and the cell represents a field region on the chip. Thus, the array height is zero and step height is zero. Another boundary case is when the copper pattern density is close to 1 (100%). This indicates that the grid cell is nearly all trench fill, as if the grid region comes from a middle of a large line or pad on the chip which would be filled conformally. Thus, the array height is set to $-H_o$, where H_o (a positive number) is the initial trench depth, and the step height is set to zero. The computation of AH and SH as expressed in Equations 5.9 and 5.10 (including the special cases discussed above) is then repeated for all grid cells in the chip to yield a complete chip-scale simulation of the electroplated topography.

Based on the step height result, a "topography density," or ρ_T, is defined as follows:

$$\rho_T = \begin{cases} \rho_c & SH > 0 \\ 1 - \rho_c & SH < 0 \\ 1 & SH = 0 \end{cases} \tag{5.11}$$

where ρ_c is the layout copper pattern density as computed by the layout extractor. The topography density ρ_T represents the area fraction of "raised" features, in each grid cell, accounting for both negative and positive step heights. If the step height is positive, the topography density is the same as the layout pattern density, and if the step height is negative, then the topography density is one minus the layout density as illustrated in Figure 5.7.

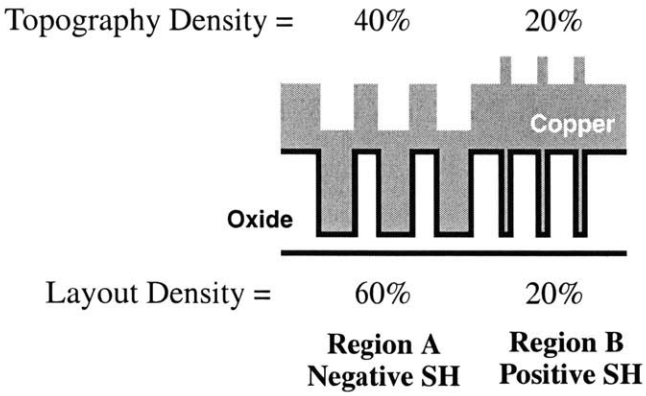


Figure 5.7: Topography Density vs. Layout Density

5.4 Field Thickness Variation: Extraction and Simulation

Up to this point, we have dealt with array height and step height variations, and have assumed that the nearby wide field regions without any patterned trenches are flat. Experimental results, however, indicate that there is non-negligible field thickness variation, where we consistently observe a thinner field thickness near fine array regions that have a large array bulge, than in regions near wide features or wide field areas that have no bulge. In this section, we extend the plating model of Chapter 4 to account for this "chip scale" effect, and describe extension of the chip scale simulation to incorporate this additional field thickness variation.

For this study, measurements are taken using the Metapulse tool by Rudolph Technologies on field regions between array structures, on wafers from plating experiment A discussed in Chapter 4. The measurement sites are marked by numbers indicated on the test mask v1.2 as seen in Figure 5.8a. The measured data is shown in Figure 5.8b, where the range of field thickness is about 1400 Å, and the average is 15325 Å which is close to the nominal target thickness of 15500-16000 Å. A simplified approach might be to treat the field thickness variation seen in this data as random "noise", and use the average value of 15325 Å throughout the chip in calculating absolute copper film thicknesses. This simplified approach would contribute an RMS error of 374 Å, and the use of the average value might be acceptable since it gives an RMS error of only about 2.5%.

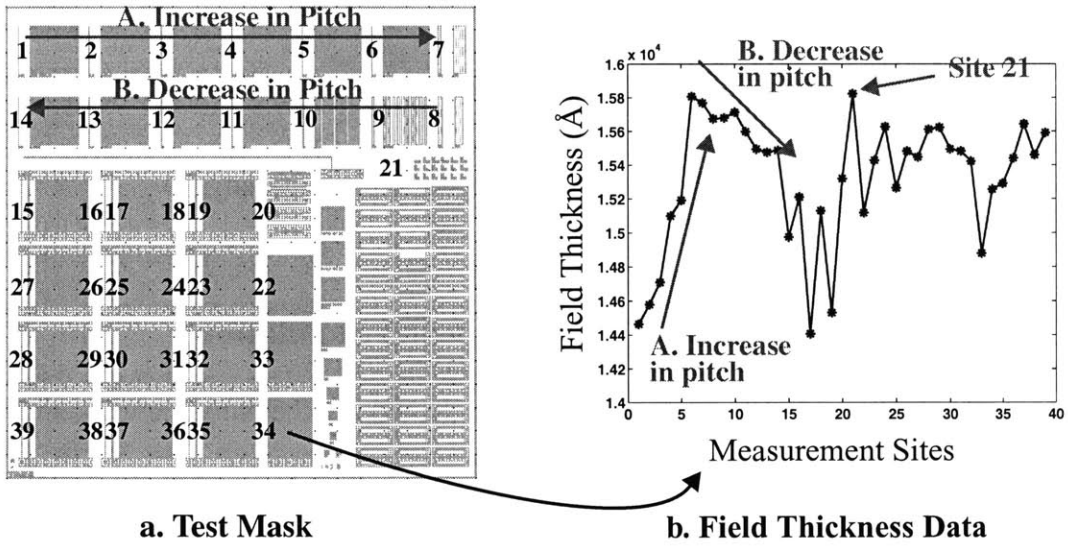


Figure 5.8: Field Thickness Measurement and Data

Upon careful observation, however, the data is found not to be random, but rather to have a systematic trend. For the measurement sites 1 through 7, the array regions next to each site increase in pitch, and for the measurements sites 8 through 14, the array regions next to each site decrease in pitch, where pitch is defined as the sum of line width and line

space. The top two rows (where measurements from 1 through 14 are made) are pitch structures having a fixed pattern density of 50% (equal line width and line space) with varying pitch values. The data indicates that there is an increase in field thickness if there are array regions nearby with large pitch values, and there is a decrease in field thickness if there are array regions nearby with smaller pitch values. Also, it is observed that measurement site 21, which is surrounded by larger field region, has one of the largest field thickness. This observation of a systematic trend indicates that a third length scale may be at work related to field thickness variation. In this case, the field thickness depends on nearby structures in a region on the order of hundreds of microns if not millimeters around the field region of interest since the distance from a field measurement site to a nearby array region is around 0.5 to 1 mm.

It is not clear what the physical origins of this effect are. One possibility is that field thinning might be influenced by the nearby bulged regions as pictured in Figure 5.9. As a wafer is electroplated, a bulge starts to form in regions where there are fine lines and spaces. As the region is protruded above nearby field regions, there is a divergence of electrical fields in the field area near a bulged region. Thus, the field area may see a somewhat slower deposition rate. Another possibility is that a microloading effect is taking place, in which depletion of copper species and additive chemistries may occur depending on neighboring regions [33].

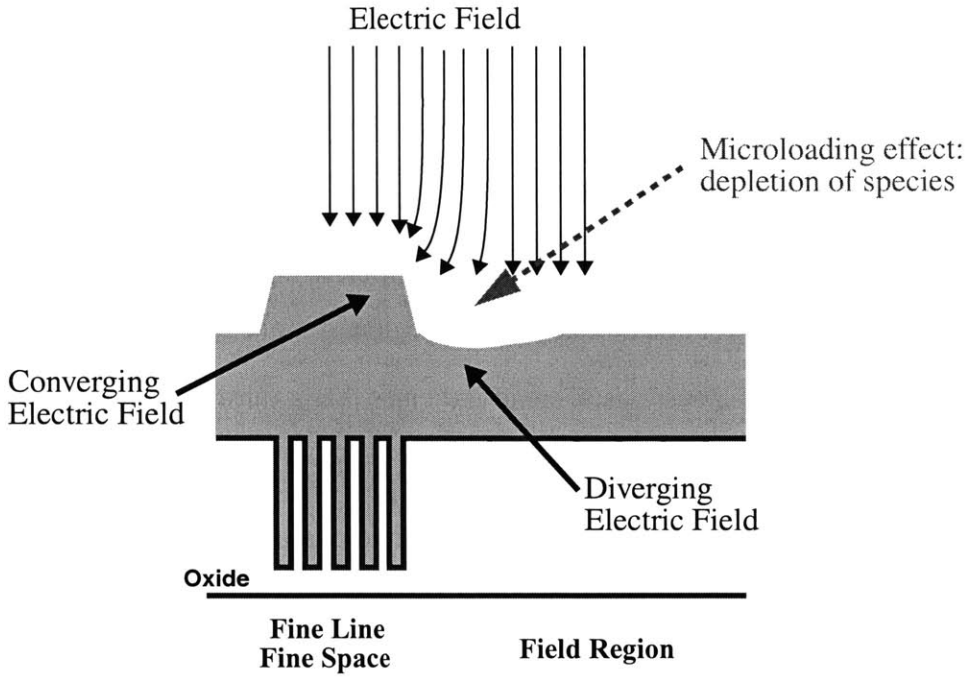


Figure 5.9: Initial Copper Profile and Influence on Copper Removal

In the work here, we seen again to generate a semi-empirical model to capture the observed effect, and leave physical investigation to future work. We note that the nearby pitch regions have different degrees of bulging or recess, and hypothesize that this is related to the thinning in nearby field regions. We thus propose a first order model in which the field thickness is related to copper fill in surrounding regions as indicated in Equation 5.12.

$$FT\,(x, y) = f(\textit{copper fill in surrounding region}) + \textit{Constant} \qquad (5.12)$$

where *FT* is the field thickness of position x, y on the chip. One approach to computation of the "total fill" needed in Equation 5.12 would be to use the results of the array height calculation in the previous section. We propose an alternative approach in which we frame the field thickness variation as a function of the underlying layout patterns (rather than as the derived *AH* values) as shown in Equation 5.13.

$$FT(x, y) = f(\text{layout pattern}, P) \tag{5.13}$$

Here P is a model parameter that specifies the size of the region that influences a particular point of interest, and is used to determine the number of grid cells to use in calculating *FT*.

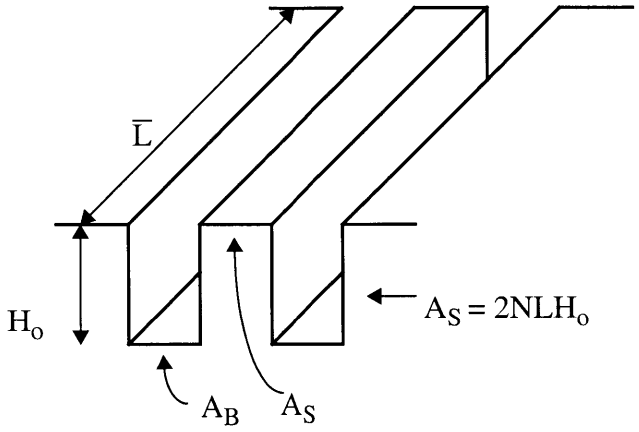


Figure 5.10: Surface Area Calculation

To capture the field thickness variation, we find an average "surface area" computed over a region of size P on the chip. This surface area parameter, or *SA*, is a derived layout factor which tracks both line width and space simultaneously, and is conceptually based on a total "exposed" surface area accounting for sidewalls as well as the tops and bottoms of features, as illustrated in Figure 5.10. The surface area increases for smaller line width and/or space where a larger bulging effect is present. The surface area is defined as follows:

$$SA_g = A_W + A_B + A_S \tag{5.14}$$

$$A_S = N \cdot \bar{L} \cdot 2H_o \tag{5.15}$$

$$A_B + A_S = G^2 \tag{5.16}$$

where SA_g is the surface area for grid cell g, A_W is the side wall area, A_B is area of the bottom of trench, A_S is the area of spacing, N is the total number of lines in the cell, L is the average line length, and H_o is the patterned trench depth. Here G is the grid size, in our case 40 μm.

Based on the surface area SA_g, we formulate the following relationship from Equation 5.13 to capture field thickness variation for grid each cell g:

$$FT_g = \alpha\langle \overline{SA}_g - C_o \rangle + F_o \tag{5.17}$$

where α, C_o, and F_o are common model parameters for all of the grid cells. Here C_o is a constant surface area offset term, and F_o is a field thickness constant term. $\overline{SA}_g$ is the average surface area computed over a distance P. Thus, $\overline{SA}_g$ is an averaged value of the underlying cell SA_g values, where the average is taken across a substantial number, $(P/G)^2$, of nearby cells. In determining the model parameters, $\overline{SA}_g$ is computed for a range of values of P up to 10mm which is the half the size of die. Then, for each candidate P and resulting $\overline{SA}_g$, the model is fit to the data to determine the fit error. The optimal field thickness model parameters are selected for the case with lowest fit error. The model parameter extraction result for plating experiment A is summarized in Table 5.3 and Figure 5.11. The field thickness model produces a chip-scale prediction of film thickness by computing the average surface area surrounding each grid cell in a die. This long-range averaging computation of field thickness is similar to the "planarization length" averaging used in pattern density-based CMP models [34], and produces a smoothly or slowly varying field thickness across the entire chip.

Table 5.3: Field Model Fit

Field Model Parameters	Extracted Values	Standard Error	t value	Pr(>|t|)
α	-1.1056	0.1178	9.4	0.0000
C_o	1628.1	24	67.8	0.0000
F_o	15720	211	74.5	0.0000
P	4680 μm			
RMS Error = 203Å $R^2 = 0.704$ *Overall Significance: P Value =* $2.547*10^{-11}$				

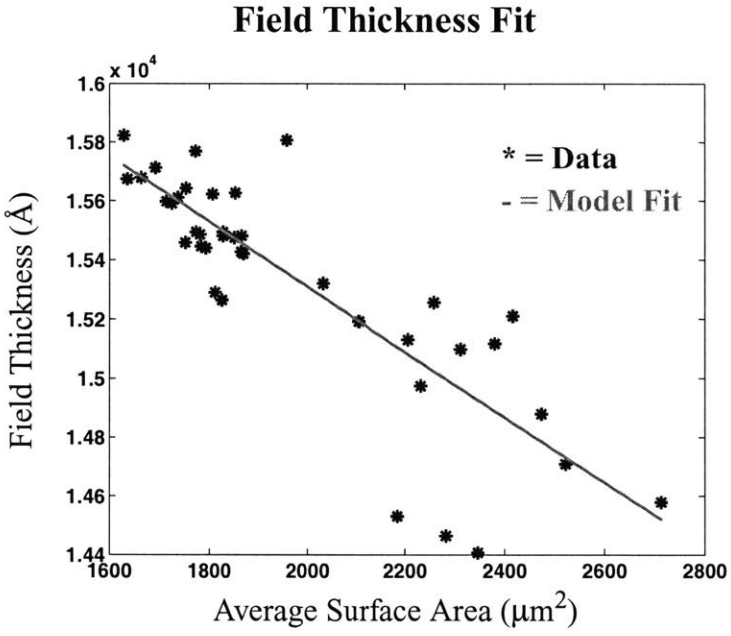


Figure 5.11: Field Thickness Fit

Using the field thickness variation predicted by this model, instead of the nominal or uniform average for field thickness, the final copper thickness, TT_g, can be found as the sum of field thickness and the array height in each grid g:

$$TT_g = AH_g + FT_g \tag{5.18}$$

5.5 Chip-Scale Simulation and Prediction Results

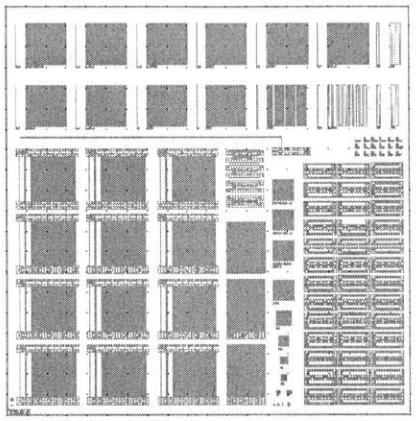
The procedure for chip-scale simulation using the semi-empirical feature and field thickness plating models, coupled to layout distribution information, has been described in the previous section. In this section, we present simulation results for step height, array height, final thickness, and as-plated topography density. First, results will be shown to evaluate how well the model is able to fit a set of calibration experiments. Second, prediction results will be shown to understand how well the fitted model applies to a different "random" layout.

5.5.1 Chip-Scale Simulation Calibration Results

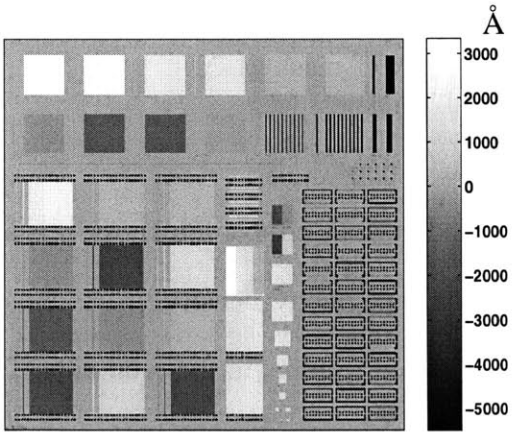
In accordance with the semi-empirical modeling approach described in Chapter 2, we first determine values for our model parameters using experimental data for a given plating process. Here we use data from plating experiment A presented in Chapter 4. Approximately 25 structures are measured for *AH* and *SH*, and 40 field region areas are measured for total copper film thickness *TT*. These values are used in the empirical fits described on Chapter 4 for *AH* and *SH*, and on Section 5.4 for field thickness. Chip-scale simulation is then performed for the test chip layout.

Figure 5.12 shows the result of the chip-scale simulation of array height and step height on the test mask (MIT mask version 1.2) that is used to calibrate the model. Qualitatively, the array and the step height maps resemble the structures on the test mask. For instance, the top two rows are the pitch structures where the top most left corner is a structure with the smallest feature size on this mask, and as we have seen in the array height trend, the array height simulation is the highest in that array region. When the simulation result is compared to the data used to calibrate the model, the root-mean-square (RMS) errors of array height and step height are 440 Å and 420 Å, respectively. These values are

slightly larger than the fitting RMS errors of 430 Å and 330 Å for array height and step height models, respectively, in the underlying feature level models. The small increase in the error is due to the fact that we are now dealing with distribution and derived layout parameter values rather than true values of line width and space in the layout. The closeness of the chip-scale values to the fit errors appears to confirm that the generalized averaging approach proposed in Section 5.3 is a good approximation.

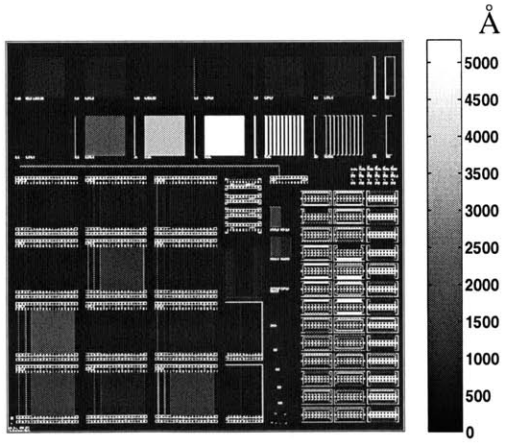


Test Mask



Array Height

RMS Error = 440Å

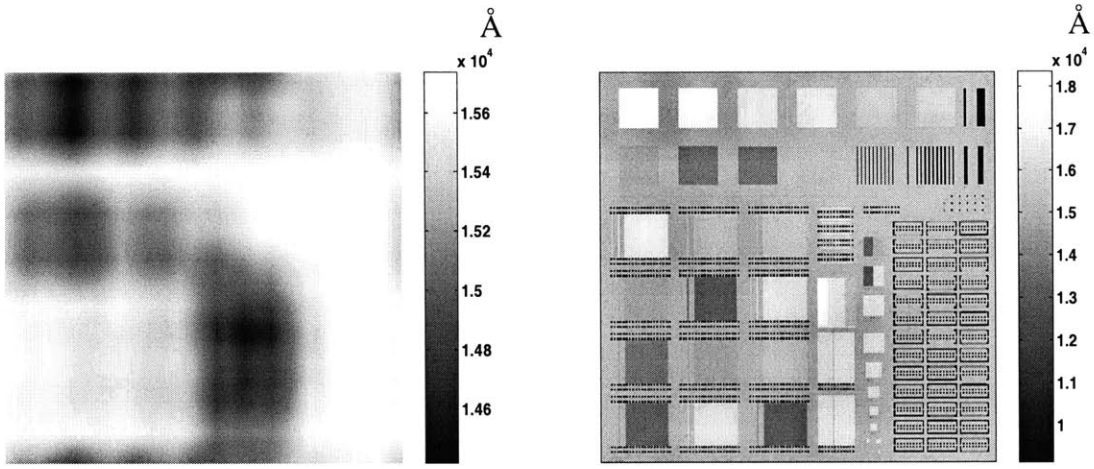


Step Height

RMS Error = 420Å

Figure 5.12: Chip-Scale Simulation for MIT mask v1.2:
Array Height and Step Height

The chip scale simulation of the field thickness variation is shown in Figure 5.13a. We see that the field is thin in areas of large array height (or bulge), as along the top left and center vertical region of the array height map in Figure 5.12. In the case of field thickness, RMS error for the chip simulation fit is the same as that during the model extraction, equal to 203 Å. To produce the total thickness map, the field thickness is added to the array height, and the result is shown in Figure 5.13b.



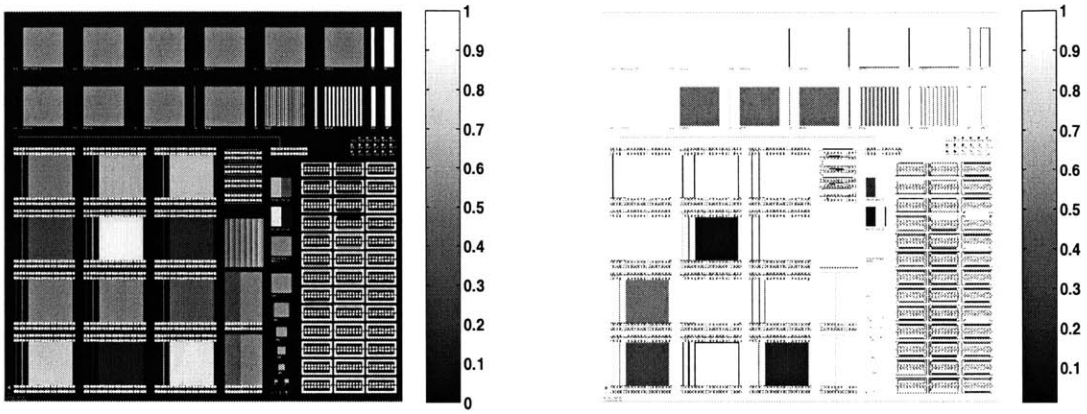
a. Field Thickness Variation

b. Total Copper Thickness

Figure 5.13: Chip-Scale Simulation for MIT mask v1.2:
Field Thickness Variation and Total Thickness Maps

In addition to the surface topography variation and the total copper thickness, it is also important to determine the topography density. The topography density, ρ_T, is the as-plated feature density corresponding to the ratio of raised features to the total area. This result is important since the topography density is directly used in the simulation of CMP profile evolution where raised feature density plays a major role in determining the rate of removal rate of copper. Figure 5.14 shows the simulated topography density. When compared to the layout density, which is the density determined using the layout geometries, the topography density is different at many locations. For instance, the top row in the mask

layout contains relatively fine pitch structures with 50% pattern density. Thus, the layout density shows 0.5 for those array regions. However, since the small features result in small plated step heights, the surface is flat or blanket-like in each array region. Thus, these array regions are interpreted as 100% topography density in the map to the right of Figure 5.14.



Layout Density Topography Density

Figure 5.14: Chip-Scale Simulation for MIT mask v1.2:
Layout Density and Topography Density

5.5.2 Chip-Scale Prediction and Verification Result for Arbitrary Layout

The previous section demonstrated good matching between the extracted model and the data used to fit that model. This section presents simulation results and the verification for predicting the surface topography for a different complex layout as desired in the methodology pictured in Figure 5.15. For this verification of the chip-scale prediction, a patterned wafer containing both test structures and product like regions is electroplated with the same process used to calibrate the model. After the wafer is electroplated, measurements of array height, step height, and copper field thickness are taken at about 60

locations in a representative die, and compared to the prediction result from the chip-scale simulation.

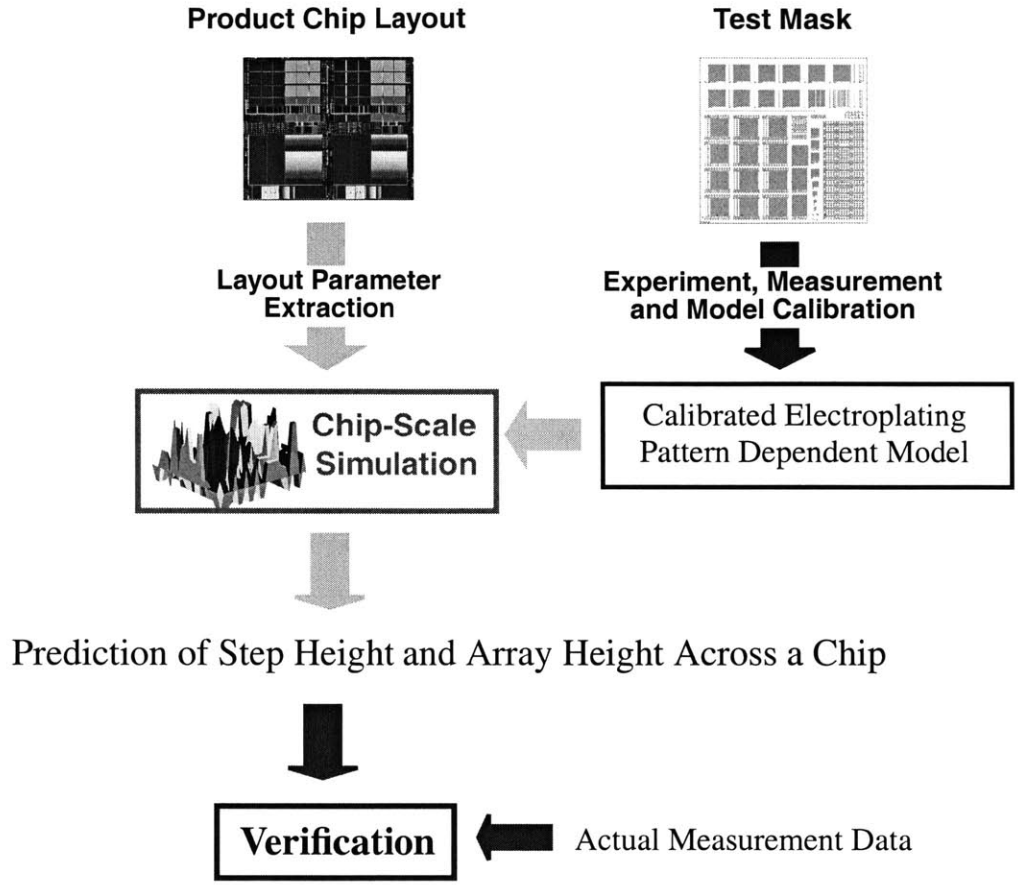


Figure 5.15: Prediction and Verification of Chip-Scale Simulation

A sample surface profile measurement is shown in Figure 5.16 for the complex layout. We can identify regions in the scan where the surface profile is relatively flat corresponding to large array regions; we take array and step height measurements in these regions whenever possible to avoid having to average heights for a region smaller than our discretization length of 40 μm. This sample scan shows that our notion of array height and step height is still applicable for random layouts. The field level is estimated by leveling the scan to regions consisting mostly of field area.

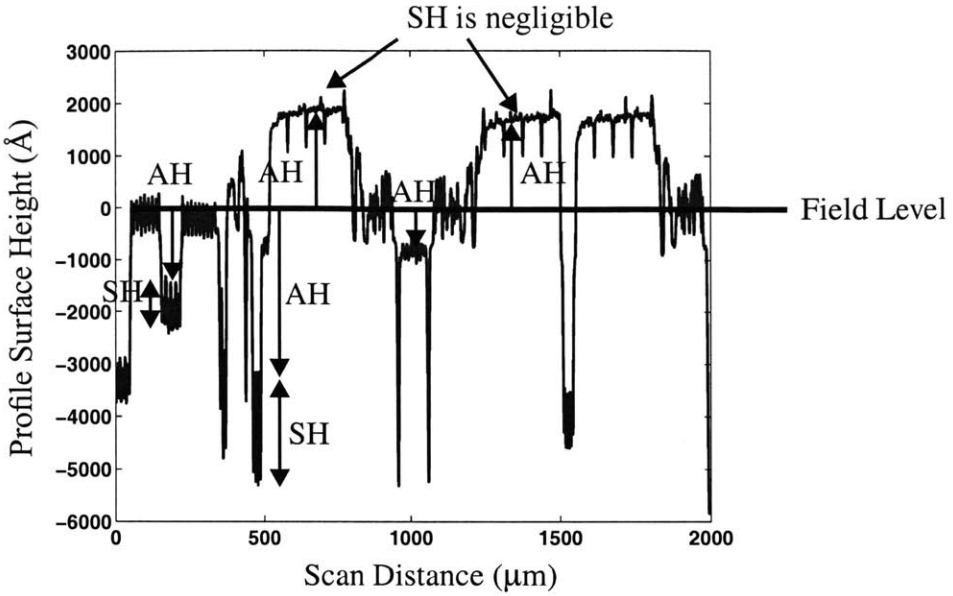
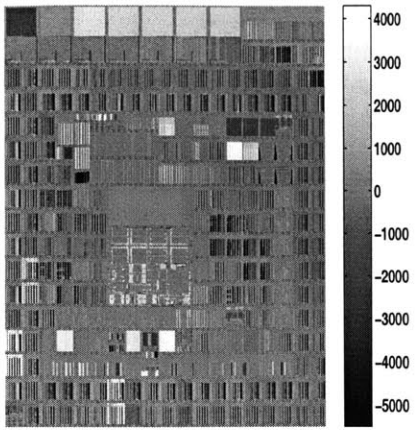
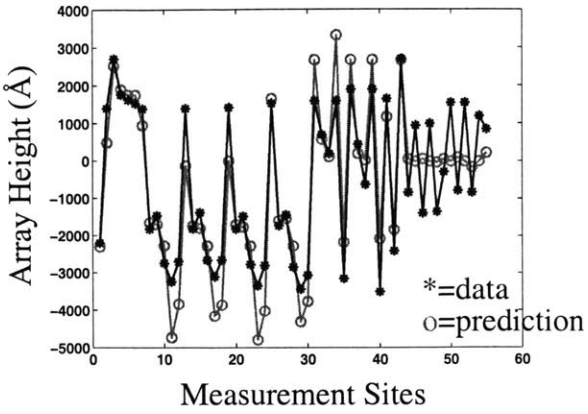


Figure 5.16: Sample Profile Scan of Verification Data

Figure 5.17 shows the prediction result of the chip-scale simulation for the array height and the comparison to actual measurement data. The comparison shows that root-mean-square (RMS) error is about 870 Å; for a nominal copper thickness of 15000 Å, this corresponds to about 5.8% error. We note that in some regions (sites 10 to 40), the model over predicts the magnitude of array height. This is believed to be caused by nearby dummy fills around the measured region consisting of lines that span about 10-20 μm wide; the simulation accounts for these dummy fills in its 40 μm wide cell whereas our measurement is done for the array height created by the lines excluding the nearby dummy fills. In other regions that are more product chip like (sites 40 to 55), the model predicts relatively little array height, while ±1000 Å is observed. This may be due to difficulties and errors in the measurement of array height where there are no clearly defined field areas to level profile surface traces.

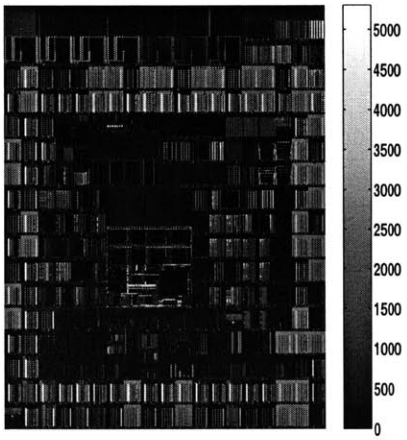


Array Height

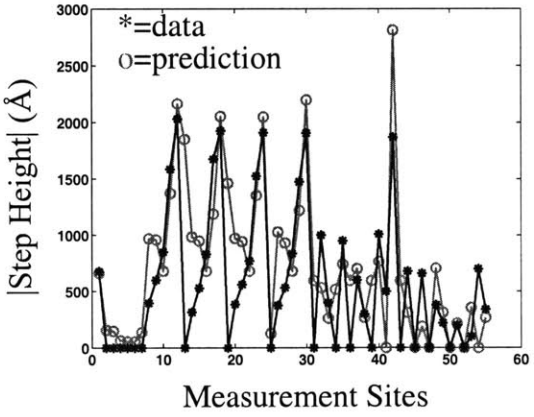


Prediction RMS Error = 870Å

Figure 5.17: Chip-Scale Prediction and Verification: Array Height



Step Height



Prediction RMS Error = 479Å

Figure 5.18: Chip-Scale Prediction and Verification: Step Height

The chip-scale result of the step height prediction is shown in Figure 5.18 along with the comparison between the simulated result and measurement data. The step height prediction is done based on absolute values to avoid the positive and negative height cancellation effect described in Section 5.1, and an RMS error of 479 Å is obtained. The range of

observed step height is about 2100 Å, and the model captures the spatial dependency fairly well. We conjecture that the averaging and die-scale discretization contribute to larger errors in truly random layouts, compared to relatively large and uniform test structures used in model extraction.

The field thickness variation across the entire chip is shown in Figure 5.19 with the comparison to data shown on the right of the figure. The field thickness model is seen to produce a good first order prediction; further work could seek to identify additional second order effects giving rise to field thickness variation around the smooth averages predicted by the model. The plot of field thickness vs. average surface area shows that the electroplated field copper is thinner in regions with higher average surface area of the layout patterns; these cause a greater bulging effect, and this bulged region reduces the field thickness nearby.

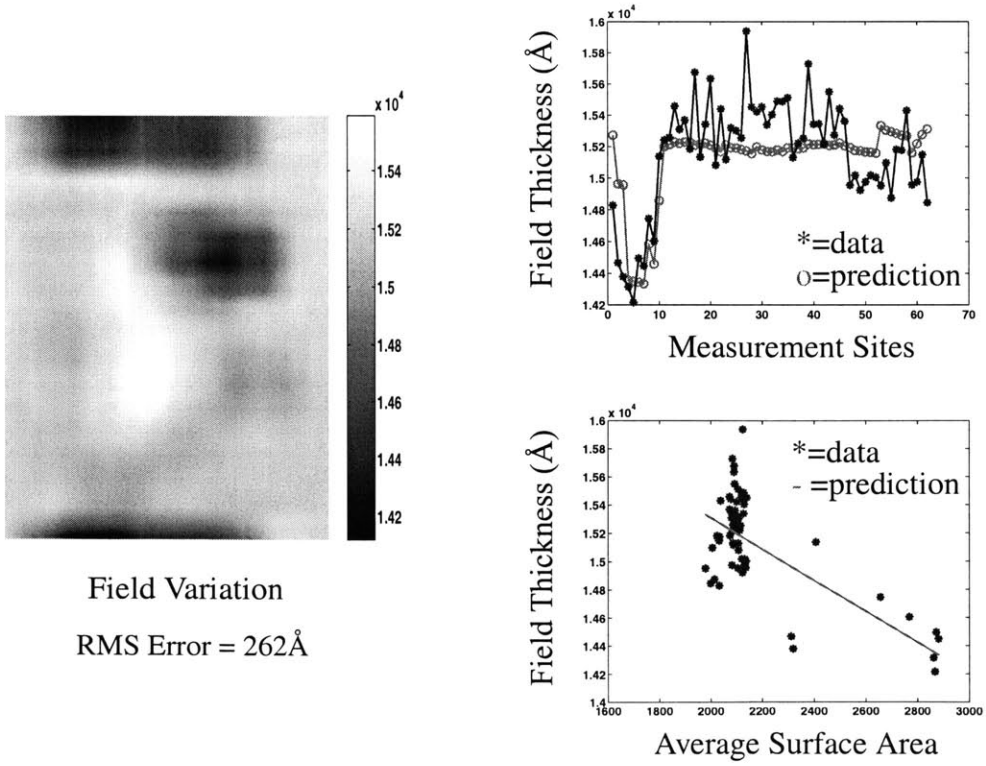


Figure 5.19: Chip-Scale Prediction and Verification: Field Thickness

By adding the field thickness result to the array height, the total copper thickness is obtained as shown in Figure 5.20. The prediction indicates that the thickness varies from 0.9 μm to almost 2 μm, which gives a range of more than 1 μm thickness difference across the chip. In addition to thickness and relative height predictions, the as-plated topography density is shown in Figure 5.21, together with a layout density map for comparison. Similar to the result for the test mask version 1.2, there is great amount of difference between the layout density and the topography density. As stated earlier, the topography density is an important input to the subsequent CMP process modeling which relates removal rate to pattern density of raised features.

We have described the result of the chip-scale prediction for a complex layout and verified with actual data. There is a good match between the prediction result and measured data, and the approach of the methodology provides the first known chip-scale prediction of electroplated topography.

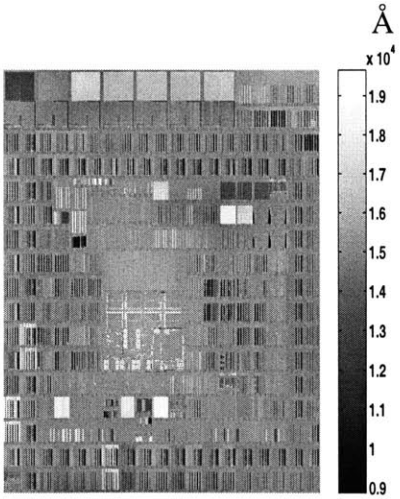
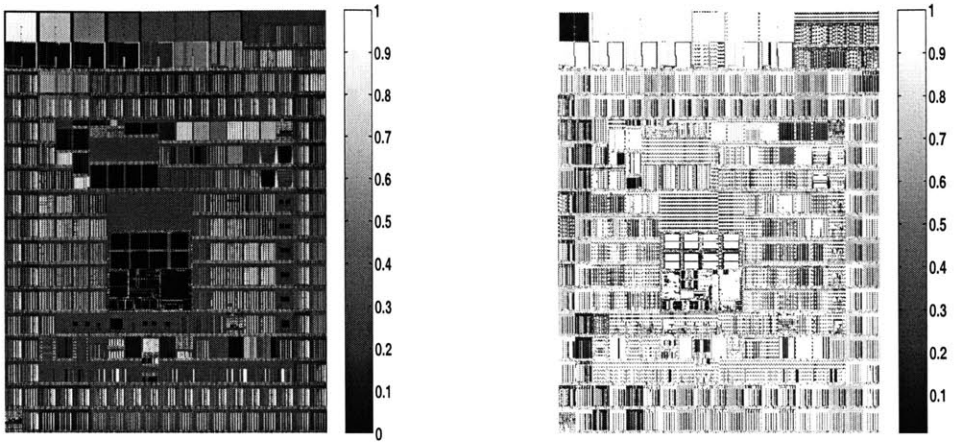


Figure 5.20: Chip-Scale Prediction: Final Thickness



Layout Density Topography Density

Figure 5.21: Chip-Scale Prediction:
Layout Density and Topography Density

5.6 Wafer to Wafer Variability of SH/AH and Field Thickness

The calibration of the model and prediction of step height, array height, and field thickness is done for a particular die from one wafer in a lot. If there is variability from wafer to wafer, the prediction of surface profiles may not be accurate. Thus, in this section we examine the wafer to wafer variability of SH, AH, and field thickness, and its implication for model prediction.

In verification experiment discussed in the previous section, 12 wafers were processed through the electroplating tool. Among the 12 wafers electroplated, we measure SH and AH at several different locations on the same center die for wafers 1, 3, 5, 7, 9 11, and 12 (Wafer 5 is used in the previous section for prediction/verification). The variability of the data across different wafers are plotted in Figure 5.22. The top graph shows SH data for seven different wafers, indicating little variability of SH from wafer to wafer. The measured standard deviations are 10, 34, and 31 Å for site 1, site 2, and site 3, respectively, as

summarized in Table 5.4. The AH trend also shows little variability from wafer to wafer, as the standard deviations for each site are all under 100 Å.

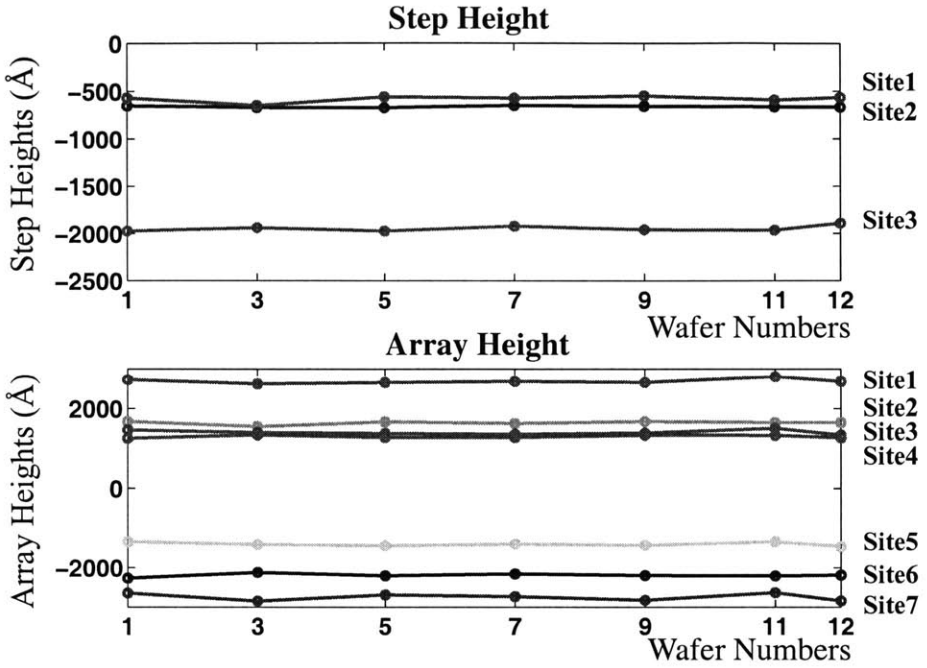


Figure 5.22: Step Height & Array Height Variability from Wafer to Wafer

Table 5.4: Standard Deviations and Range for Wafer to Wafer

Site No.	Step Height: Standard Deviation, Range	Site No.	Array Height: Standard Deviation, Range
1	10, 25	1	45, 145
2	34, 104	2	35, 87
3	31, 82	3	59, 182
		4	44, 126
		5	59, 166
		6	46, 120
		7	92, 215

The wafer to wafer variability for SH and AH is well controlled in this process. All of the variability assessment of SH and AH – the standard deviations and range of the data from wafer to wafer – compared to the prediction RMS errors (~500 Å for SH and ~900 Å for AH) indicates that the wafer to wafer variability should not limit plating model accuracy, for feature and array heights.

We next consider the overall copper thickness variability from wafer to wafer in field regions. For this examination, we use all 12 wafers in our experiment, where 57 of field area sites are measured for the same die location on each wafer. Shown on the left of Figure 5.23 is the mean thickness for each wafer, with a grand mean thickness of 15301 Å across all wafers. The standard deviation is around 121 Å, giving a wafer to wafer non-uniformity of about 0.788% (defined as standard deviation divided by mean of the thickness). If the first wafer in this lot is excluded from this data set, an even narrow variation in the data is seen: a standard deviation of 97 Å (thus, a non-uniformity of 0.634%) and range of 246 Å are obtained. The first wafer appears to add more variability in the data, perhaps due to a first wafer or process idle effect. In any case, the mean copper field thickness is found to fluctuate relatively little from wafer to wafer.

The plot on the right of Figure 5.23 shows the copper thickness for each measurement site averaged across all 12 wafers to filter out noise that may be present for a single wafer data set. This graph shows that there is standard deviation of 321 Å with the data range of almost 1400 Å and the same mean value of 15301 Å. This gives within die field non-uniformity of around 2.1%. The variation within a die for field thickness is more than three times that of wafer to wafer variability for field thickness, and motivates our effort to model within die field thickness variation.

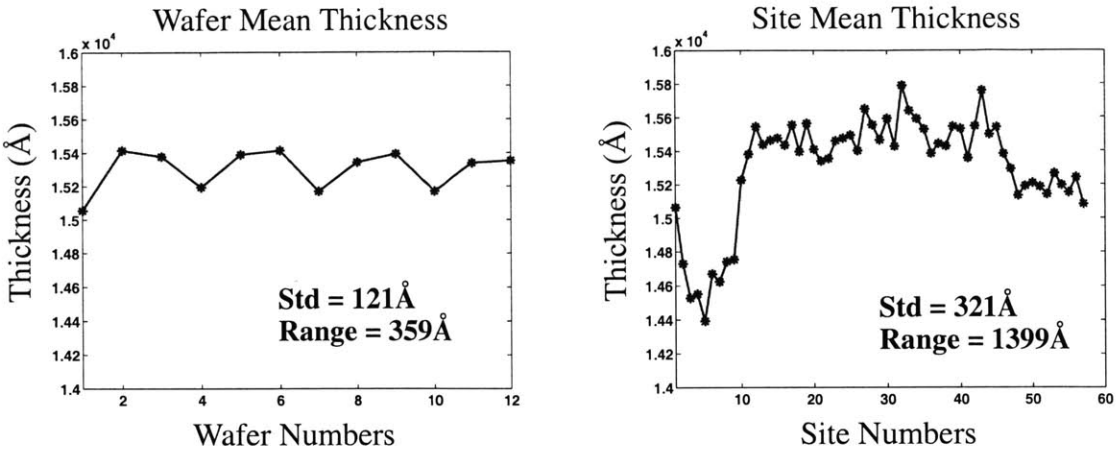


Figure 5.23: Field Thickness Variability from Wafer to Wafer

5.7 Summary

This chapter has described how the semi-empirical plating model is applied to perform chip-scale simulation for surface topography variation. Chip-scale simulation is based on average topography on a 40 x 40 μm discretized grid through the concept of average array height and average step height. This averaging within each grid cell is appropriate because the subsequent CMP process has a planarization length scale on the order of millimeters; any small "spike" of copper height that may not be captured by the average array or step height is rapidly polished away in the CMP process. To perform the step height and array height simulations across an entire chip, layout parameters are extracted based on distributions of line sizes from the layout within this grid. Then, the chip-scale simulation procedure is carried out to obtain the surface topography variation for that chip; we demonstrate successful simulation for a complex layout (different than that used to calibrate the plating model) for prediction of chip-scale topography variations including the field region thickness variation across the chip. We have found a good match between the prediction result and measured data. This methodology provides the first known chip-scale prediction of electroplated topography.

Chapter 6

Pattern Dependencies in Chemical Mechanical Polishing

A critical step in copper technology is the use of chemical mechanical polishing (CMP) to remove excess copper outside the desired metal lines and to planarize the surface. This chapter describes the pattern dependent copper thickness variation in chemical mechanical polish. As illustrated in Chapter 1, CMP is a subsequent process after electroplating to remove the excess copper and planarize the surface in a damascene process, and CMP is known to suffer from copper dishing and oxide erosion. These problems lead to a loss in final copper thickness and also leave a non-uniform surface after polishing. Just as with electroplating, characterization of these pattern dependencies is needed to identify the degree of variations in various patterns and to understand fundamental limitations of each process. In Section 6.1, we first describe the bulk polishing behavior with a given superfill electroplated profile. The thickness variation in the overpolish stage is also described and characterized for single-layer metal CMP processes. Section 6.2 then examines dishing and erosion effects arising from CMP of multi-layer interconnect structures. A pattern-dependent model for CMP proposed by Tugbawa is reviewed in Section 6.3. Finally, Section 6.4 discusses the integration of electroplating and CMP topography simulation.

6.1 Single-Level Characterization

Copper CMP interacts strongly with pattern dependent topography. In this section, we describe empirical characterization of these dependencies using the patterned test masks presented in Chapter 3. First, in Section 6.1.1, bulk copper polish behavior is described by showing the profile evolution over polish time for different test structures, and consider

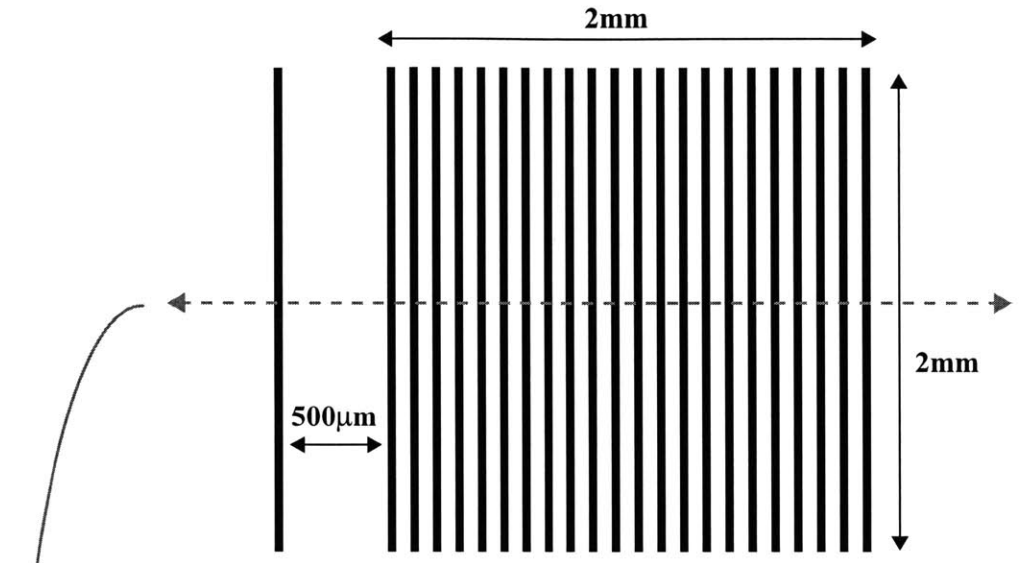
how planarization is affected by the initial topography. In Section 6.1.2, the subsequent overpolish profile evolution is examined to study copper dishing and oxide erosion. Finally in Section 6.1.3, three different studies are presented to illustrate key pattern and process effects in copper CMP processes.

6.1.1 Bulk Copper Polish Evolution

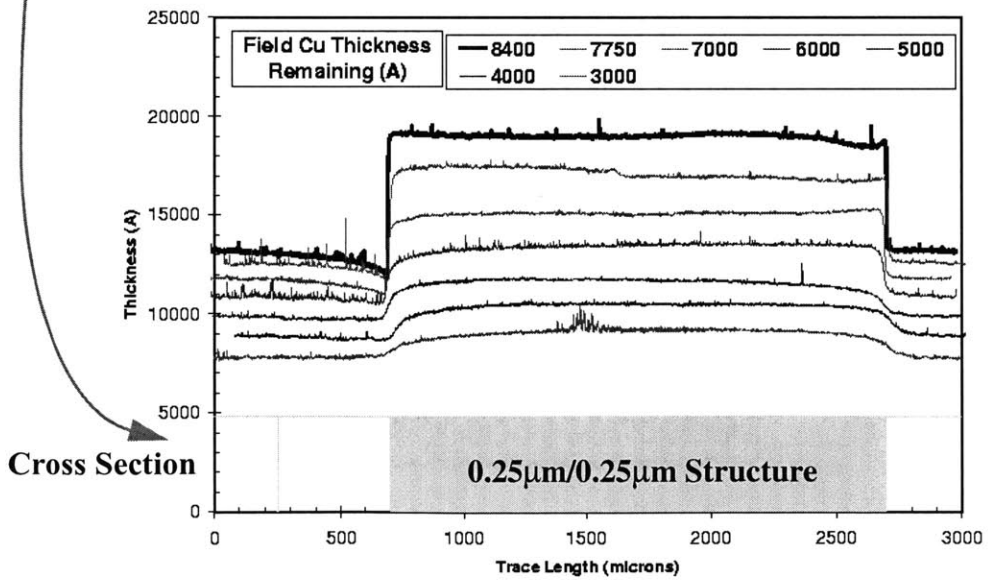
We have emphasized the importance of electroplated topography and its influence on CMP. In this section, we show a polishing sequence of different structures with various polishing characteristics. Wafers 8" in diameter are patterned with the copper test mask v1.2 with a trench depth of 5000 Å and then electroplated for a nominal copper thickness of 8500 Å using a superfill recipe similar to that used in the electroplating profile studies presented in Chapter 4. For polishing, an Applied Materials Mirra CMP tool is used, with 5 psi down force and 63 rpm table speed, and a consumable set consisting of Rodel IC1000/Suba4 stacked pad and Cabot EPC-5001 slurry. Each wafer is polished to a different target thickness in field regions (we refer to this phase as "step 1"), and HRP scans are made across each structure as shown in Figure 6.2a.

Figure 6.2b shows a cross sectional view of the test structure (isolated line and array region) on the bottom of the graph with 5000 Å of trench depth. The corresponding profile scans for each remaining copper target thickness are shown above the cross sectional view of the test structure, and the targeted remaining copper thicknesses in the field region in each successful polish split are: 8400, 7750, 7000, 6000, 5000, 4000, and 3000 Å. The profile shown for 8400 Å constitutes the initial profile. Since this is a fine array structure (0.25 μm width and space), the initial electroplated surface topography shows a large array height. As we would expect, this bulge region is polished faster than the nearby field regions, thus effectively decreasing the magnitude of the bulge over time. The profile cor-

responding to 3000 Å field thickness remaining shows that about 5000 Å of copper has been removed in the field region while about 10000 Å has been removed in the bulge area.



a. Test Structure



b. Profiles Across the Middle of the Test Structure

Figure 6.1: Bulk Copper Polishing: Fine Feature

The polishing evolution for the as-plated starting topography for a different structure having line width and space of 50 μm is shown in Figure 6.2. The starting profile shows about the same step height for the isolated line and the array lines since these are rather large features. Initially, only the up areas are polished and the down areas (corresponding to trenches) receive little removal. As the step height decreases, the down area starts to polish, and eventually at the field copper remaining thickness of 3000 Å, there is little step height left. This behavior shows a copper removal rate dependence on the step height; models for this effect will be described in Section 6.3. In the array region, the top of the array is at the same level as the field initially, but as polishing progresses a slight recess across the array region compared to the nearby field level becomes apparent. This accelerated polish for a patterned region is a well known effect where the characteristic length scale of neighbor influence is typically in the range of 4 to 8 mm [21, 35, 36]. Figure 6.3 shows the profile evolution for a large trench of 200 μm that also highlights the step height dependent polish rate. As expected, there is little removal of the down area initially, and after the step is reduced to a certain height the down area starts to polish [15, 21].

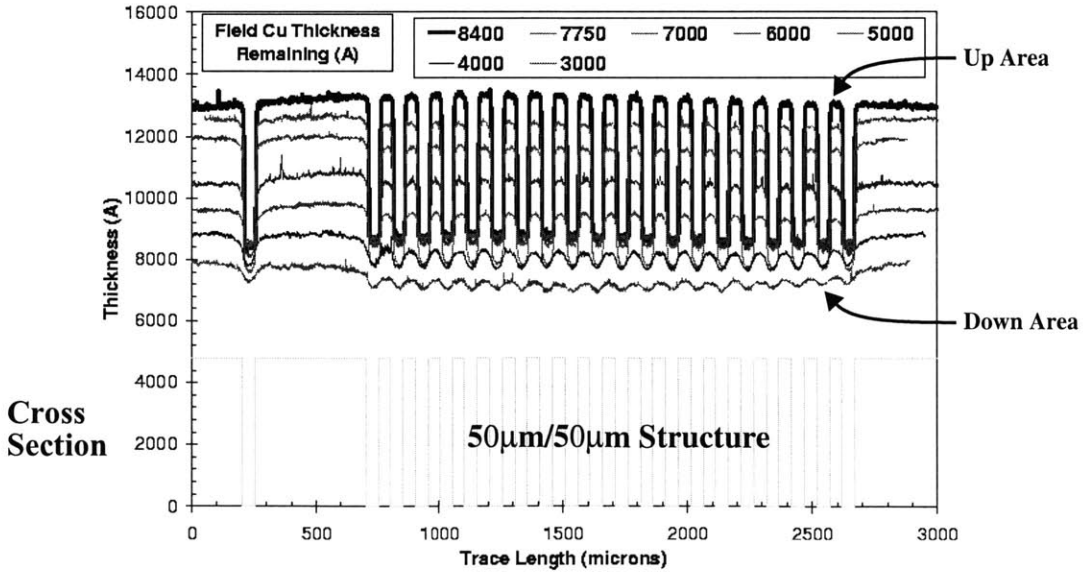


Figure 6.2: Bulk Copper Polishing: Large Feature

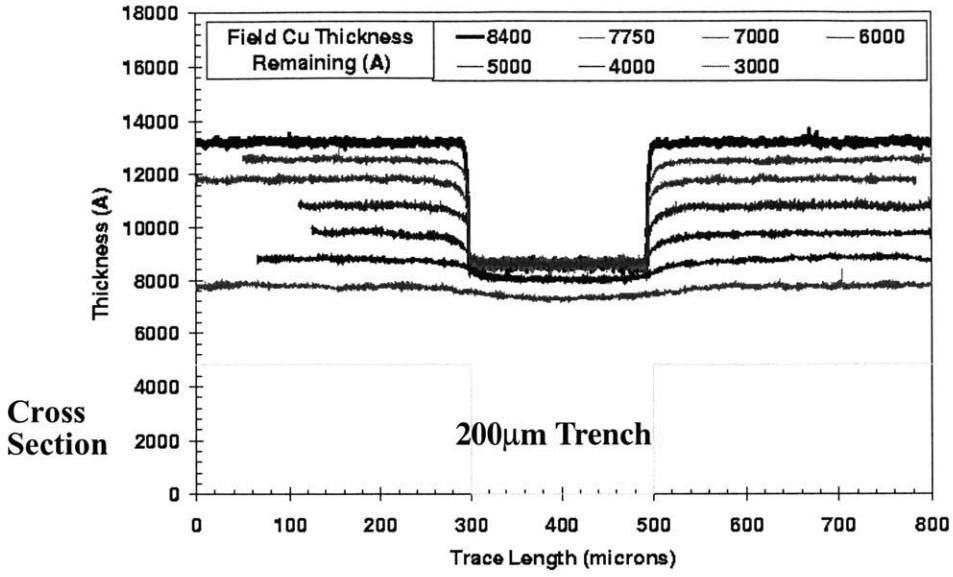


Figure 6.3: Bulk Copper Polishing: Large Trench

The previous figures show polishing profile evolution over time; it is also interesting to observe the trend as a function of various patterns at different polishing phases. Shown in Figure 6.4 are the initial as-plated copper profiles across different pitch structures leveled to zero on the field region. As discussed in Chapter 4, the plating profiles depend on the underlying layout patterns. A thick bulge (positive array height) is observed for the 0.25μm/0.25μm (line wdith/line space) structure, while conformal deposition is observed for large features. Shown in Figure 6.5 are similar initial profile trends for density structures. The figures in the top row are structures with line widths of 0.35, 0.7, and 0.9 μm, all with a fixed line space of 0.35 μm. As we would expect, the degree of bulge decreases with wider trenches. The next two row of figures contains varying density structures with a fixed pitch of 5 μm. The 0.5μm/4.5μm structure shows a significant bulge, while the 4.5μm/0.5μm structure shows a large recess (negative array height). In both figures, the

transition from bulge (superfill) to recess (conformal fill) happens between line widths of approximately 1 μm and 2 μm.

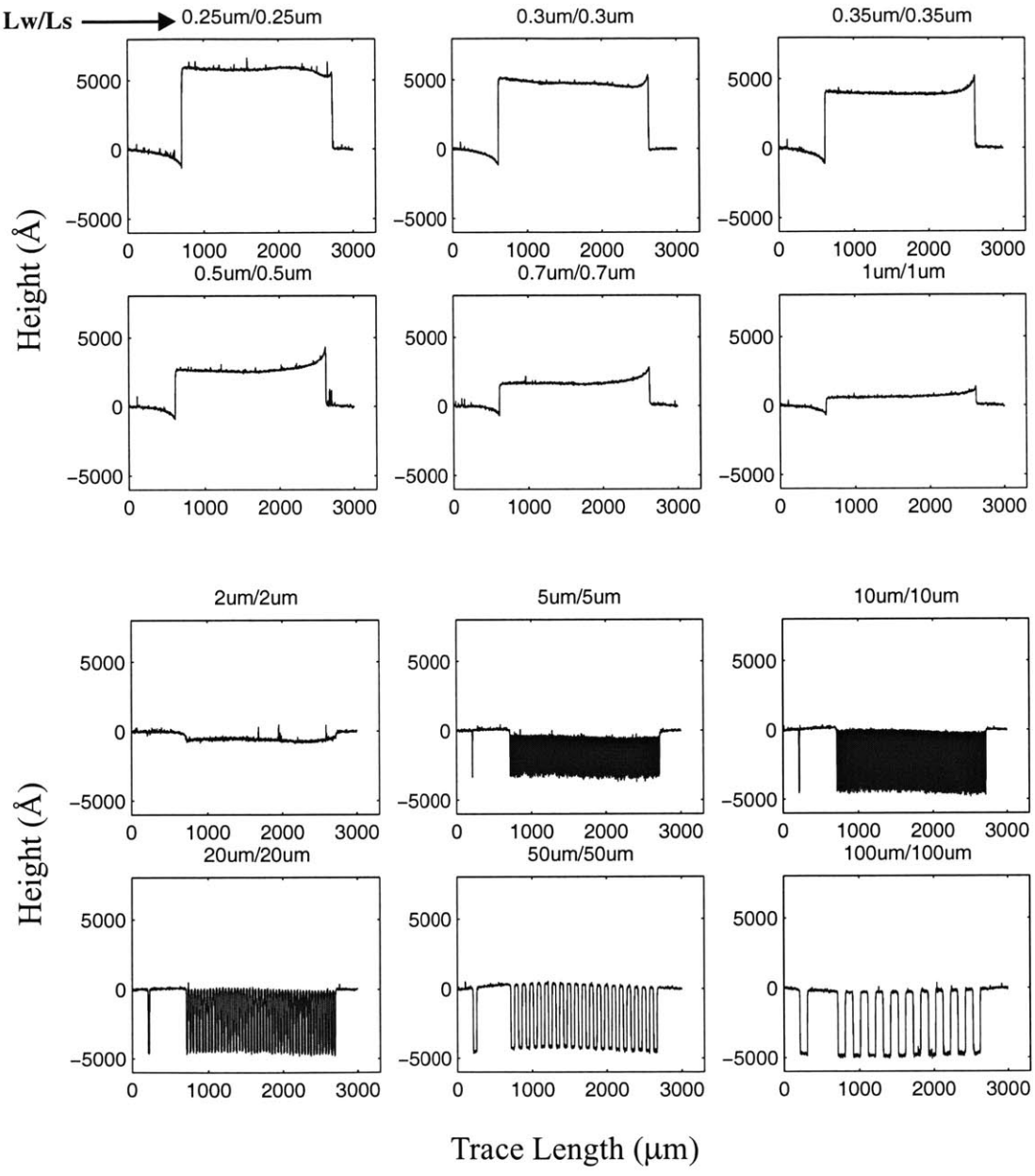


Figure 6.4: Initial Surface Heights for Pitch Structures

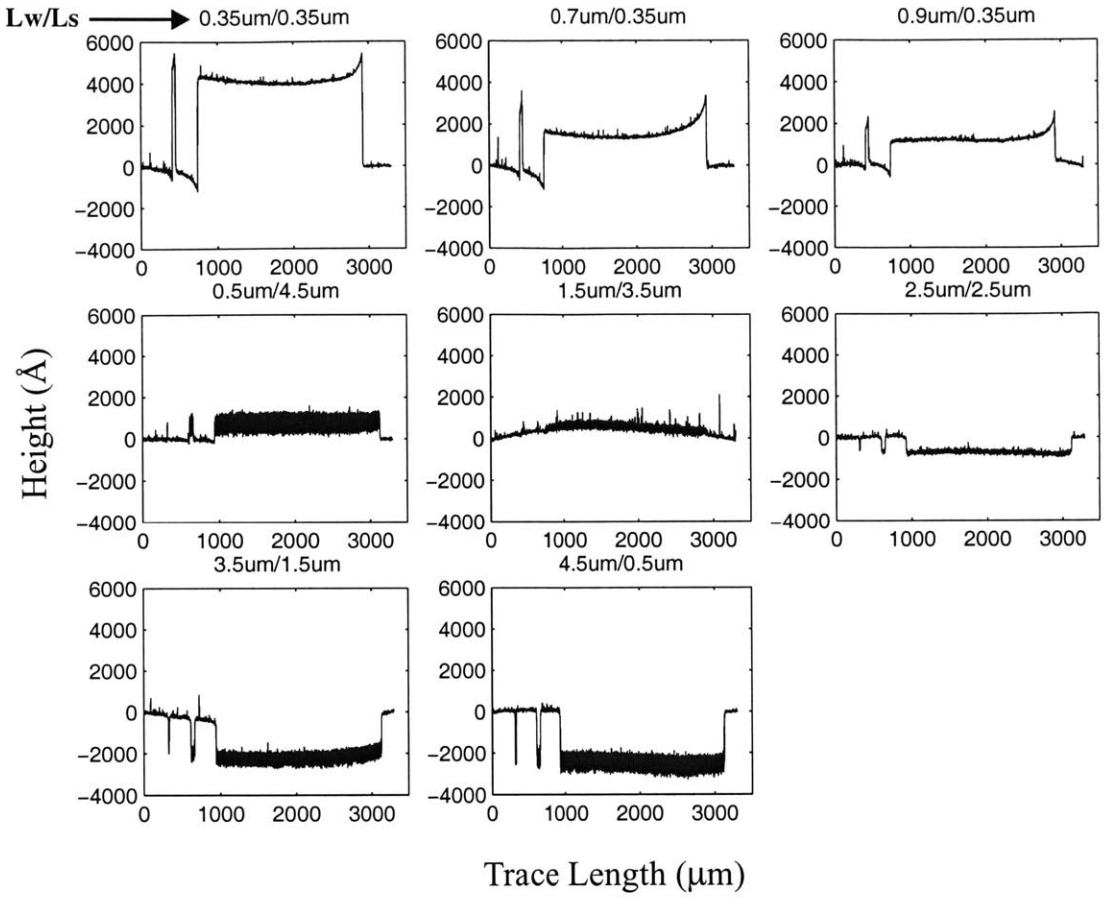


Figure 6.5: Initial Surface Heights for Density Structures

As polishing progresses, each structure receives different degrees of removal. Figure 6.6 shows the profiles across each pitch structure leveled at zero for the field remaining target thickness of 5000 Å. The bulge is still seen for small feature structures, but a relatively flat surface is observed for 0.7 and 1 μm pitch structures. For large features, the step height is reduced to about half the initial height, and a higher degree of array recess is seen for structures with 5, 10, and 20 μm lines and spaces. For the density structures shown in Figure 6.7, a similar polish-induced array recess increase is present in high density structures in the bottom row of the figure, and a relatively flat profile is achieved for low to

medium density arrays shown in the middle row of the figure. Also, a relatively flat surface is seen for the 0.9μm/0.35μm density structure indicating that most of the bulge has been removed. The structure labeled 0.35μm/0.35μm is a repeated structure on a different location on die and shows similar removal of bulge for the same structure present in the pitch structure in Figure 6.6.

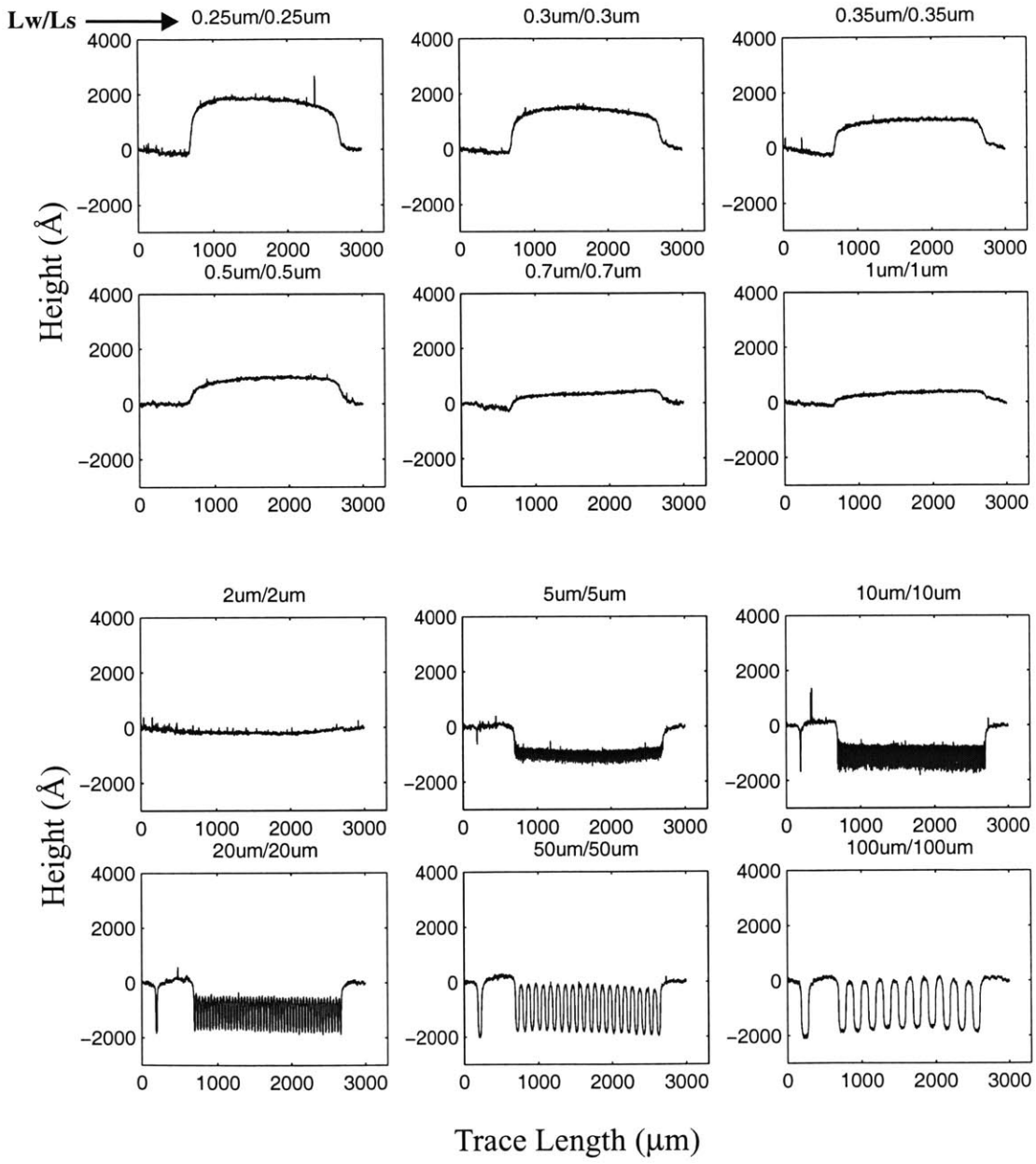


Figure 6.6: Surface Heights for Pitch Structures for Target Field Thickness of 5000Å

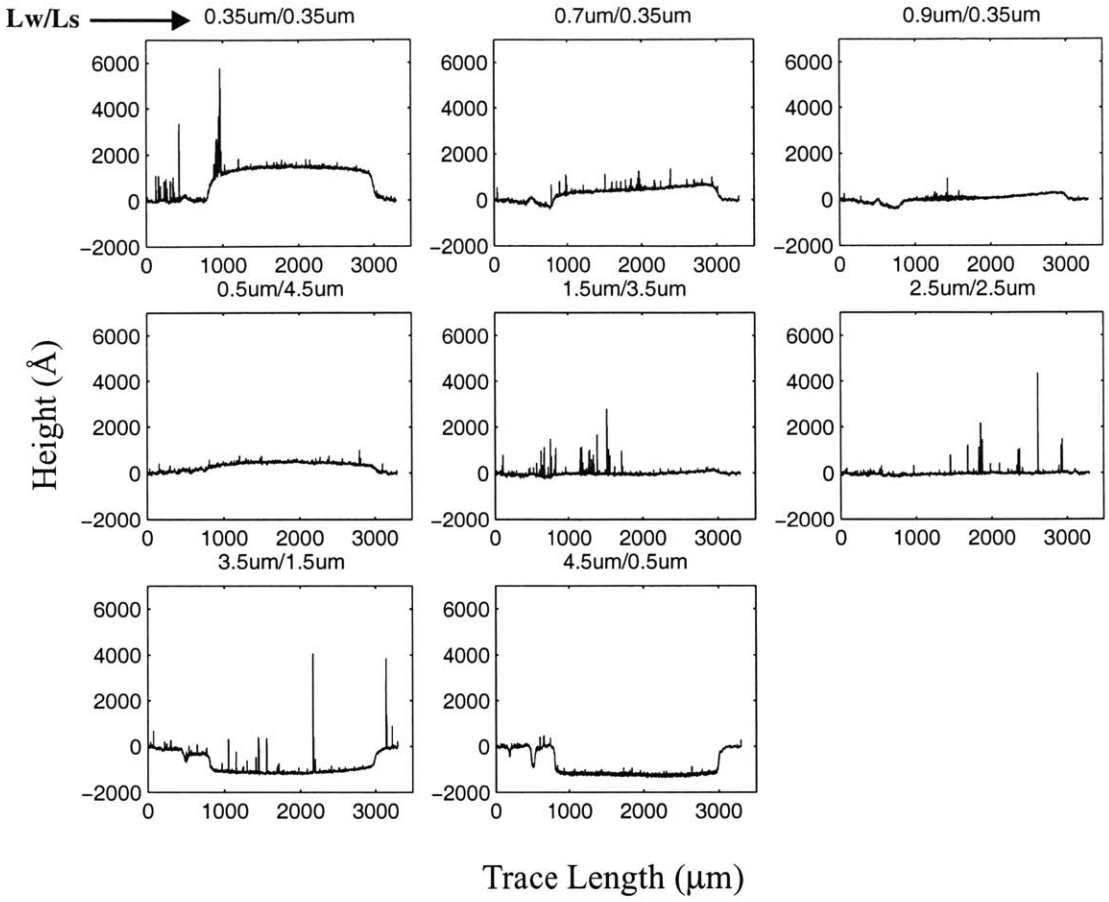


Figure 6.7: Surface Heights for Density Structures for Target Field Thickness of 5000Å (the spikes are noise in the surface trace)

As polishing further progresses, most of the structures are planarized but as much as 1000 Å of bulge can be still seen for the 0.25μm/0.25μm structure when the field has been polished down to 3000 Å as shown in Figure 6.1. The observations of the data and trends for various polish times and many pattern structures indicate that polishing has strong dependency on the initial topography in its ability to planarize the surface, and motivates our effort to model the electroplating surface topography.

6.1.2 Overpolish Evolution of Dishing and Erosion

After the copper wafers in this study are polished down to a field remaining copper thickness of about 3000 Å, the process is changed to step 2 where a low down force of 2 psi is used so that "soft landing" can be achieved. Soft landing refers to a step in which the pad "lands" slowly on the underlying barrier layer after clearing of bulk copper so that end point signals are more effective in detecting the clearing of copper. The tool and consumable set in this step is the same as for the bulk copper polish. A reflectance sensor on the tool is used for endpoint detection. To obtain absolute barrier/oxide film thicknesses, a KLA-Tencor F5 tool is used to measure thicknesses in field regions around the structures, and the surface profiles are leveled and referenced to the absolute thicknesses.

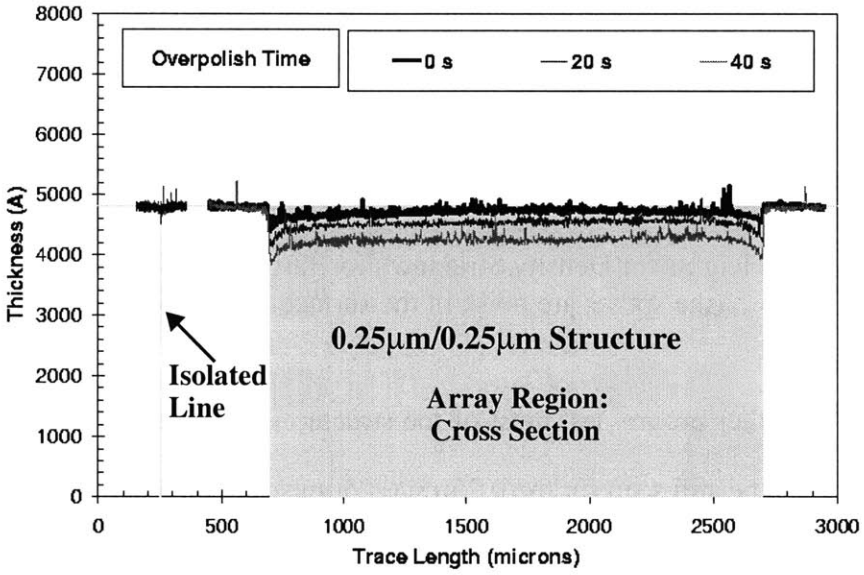


Figure 6.8: Copper Clearing and Overpolish: Fine Feature

Figure 6.8 shows the surface profile of the 0.25μm/0.25μm pitch structure for different degrees of overpolish. In this figure, "0 s" or 0 second corresponds to the endpoint time, and the wafers are further polished for the specified additional time. The surface profile

across the array region shows that even at the endpoint there is about 400 Å of recess or erosion, and this increases with further polish up to about 800 Å of recess. Since the copper slurry has high selectivity with a higher copper removal rate than barrier removal rate, there is little removal in field regions. A small amount of the isolated line dishing is also observed.

Wafers polished to endpoint in step 2 are further polished to remove the barrier layer in step 3. Step 3 uses a process condition similar to step 2 but with a different slurry. Wafers are polished for different times and the resulting profiles are plotted in Figure 6.9. Oxide film thickness measurements are also made for this step and all profile scans are referenced to these thickness values. The top-most trace shows considerable removal of oxide in the field region, about 1000 Å, and shows increased erosion of about 600 Å. The profiles for the longer polish times show an overall increase in thickness loss. Also some copper dishing is present for the isolated line.

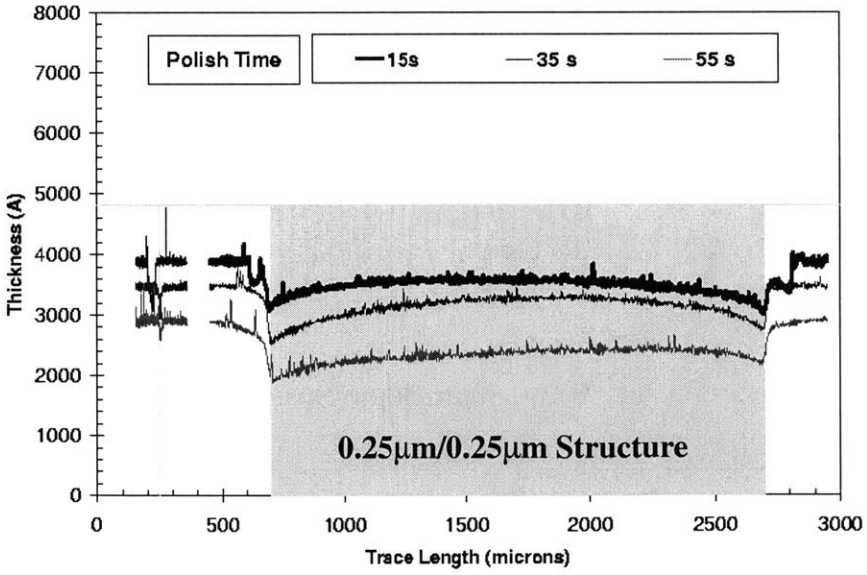


Figure 6.9: Copper Overpolish: Fine Feature

Profiles for the 50μm/50μm structure (previously examined for the bulk polish in Figure 6.2) are plotted for the step 2 process endpoint time ("0 s") and for additional polish times in Figure 6.10. The profile for the endpoint marked by "0 s" shows almost no erosion, but significant dishing for both the array line and the isolated line is observed. Dishing further increases with polish time whereas the field region maintains its thickness. The same structure is shown for the step 3 (barrier removal) polish in Figure 6.11. More erosion is now present in the array, while the array line dishing shows a decrease and finally a reversal in this process step. This reversal of dishing is commonly seen when the slurry selectivity of oxide to copper has a higher removal rate for oxide than for copper. Thus, as polishing progresses, oxide is polished faster, and the copper-recessed dishing from step 2 of the process is reduced and eventually makes the copper lines more recessed compared to neighboring oxide spaces. Also, significant field area thickness loss is shown in the figure.

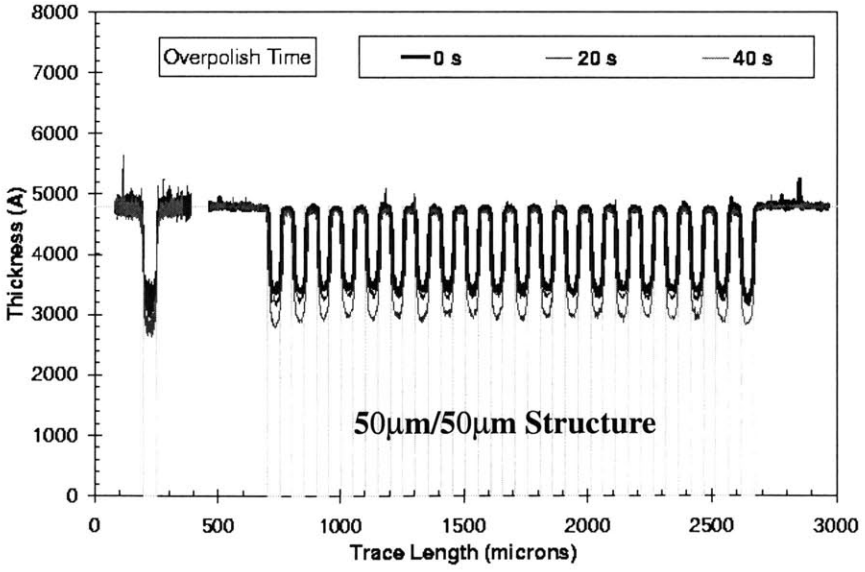


Figure 6.10: Copper Clearing and Overpolish: Large Feature

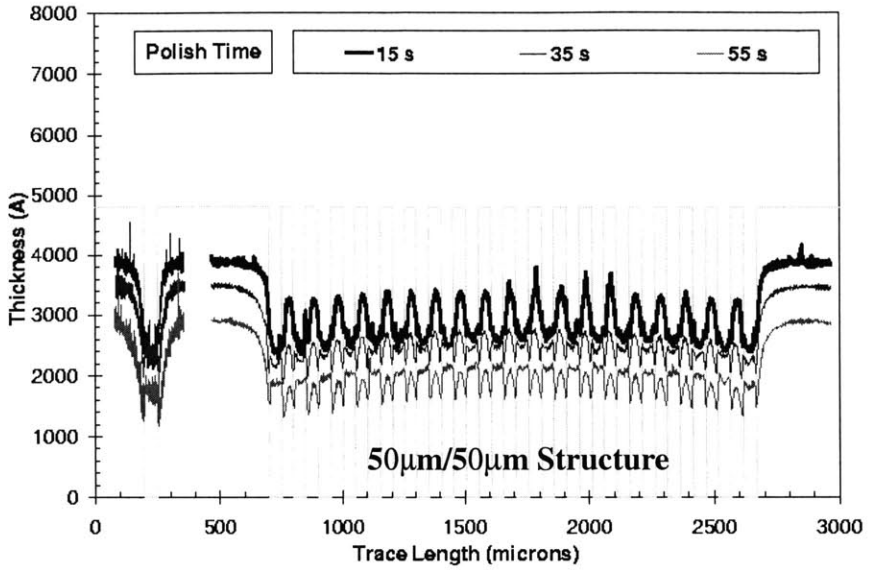


Figure 6.11: Copper Overpolish: Large Feature

The time evolution of surface profiles for various pattern structures shows that the initial starting topography from electroplating influences CMP planarization performance and the degree of dishing and erosion in overpolish. In the next section, we quantitatively examine the dishing and erosion as a function of various layout patterns.

6.1.3 Characterization of Dishing and Erosion

Ultimately, characterization data should be coupled to a physically based copper CMP model, so that key model parameters can be extracted and the resulting model then applied to arbitrary layouts as described in Chapter 2. The analysis methodology consists of careful study of the trends and dependencies identified by dishing and erosion data as a function of layout patterns, polish time or recipe, consumable selections, tool design alternatives, or other parameters of interest. These analyses can be applied to process development and optimization, to guide design rule generation (e.g. minimum/maximum rules on density, line width, and line space), as well as dummy fill or slotting strategies. In

this section, we show three different studies from different copper CMP processes, and describe their dependencies on pattern factors including pitch and density. The characterization of these variations are based on both physical measurements such as surface profiles, and film thickness measurements, and electrical measurements focused on line resistance.

A. Study1: Reverse Dishing

The first data set corresponds to the profile evolutions shown in the previous section. Array erosion and dishing are extracted from the scans and plotted against polish time and patterns. Positive and negative dishing is defined as shown in Figure 6.12. Figure 6.13 shows array line dishing vs. polish times after step 2 endpoint for different pitch structures. As we previously observed, there is significant dishing (negative step height) for large features as shown on the left, and the step height decreases in magnitude and becomes positive as more polishing is done. This happens because of the change in slurry chemistry from process step 2 to step 3: the large initial negative dishing remaining at the end of step 2 is reduced due to faster polish rate of oxide in process step 3, thus causing the magnitude of dishing to become smaller and eventually resulting in copper lines which stick up referenced to nearby oxide spaces. For the small features on the right plot of Figure 6.13, positive dishing is already present at the start of the step, and with more overpolish does not change and stays at its steady-state dishing value [37].

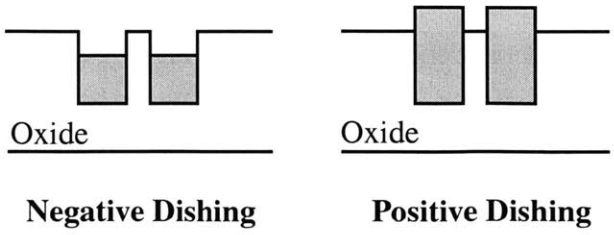


Figure 6.12: Positive and Negative Dishing

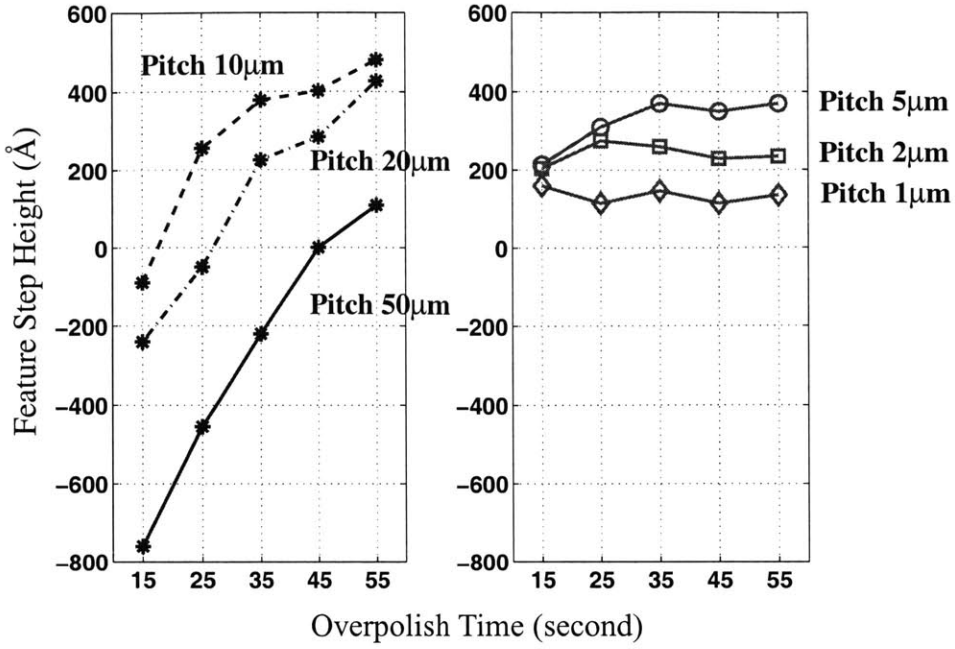


Figure 6.13: Array Dishing vs. Overpolish Time

Figure 6.14a shows the same array line dishing data plotted against pitch values. As the pitch increases from 0.5 μm (0.25 μm width and 0.25 μm space) to about 10 to 20 μm, the amount of dishing increases and becomes more positive. Then, the trend is a higher magnitude of negative dishing as the pitch becomes larger. Figure 6.14b shows the array recess (corresponding to oxide erosion) referenced to nearby field regions. Overall, higher recess is shown for larger pitch values except for 100 to 200 μm where the recess suddenly becomes less. This is because the spacing associated for large pitch structures are becoming wide enough to be polished as if it is a field region, not a patterned pitch environment. The remaining oxide field thickness is shown in Figure 6.14c, indicating that there is significant oxide loss in this particular study. As expected, there is a linear decrease in the field thickness for larger polish times. The total copper loss (field loss + recess + dishing) is plotted in Figure 6.14d, showing an overall decrease in copper thickness for all features

as polishing time increases. Large pitch structures show the greatest loss primarily because of their relatively high array dishing.

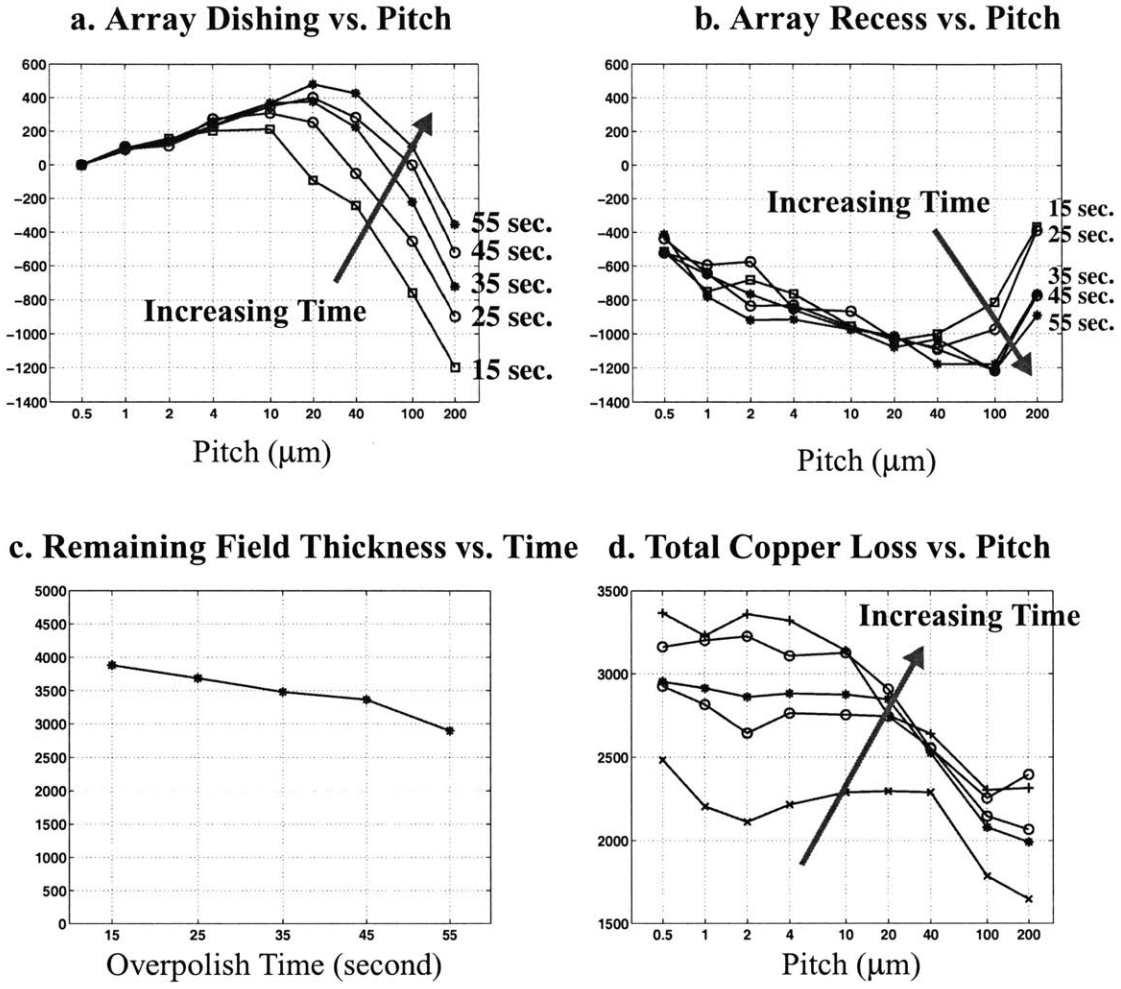


Figure 6.14: Array Dishing vs. Pitch

These trends show the peculiar behavior of reversal of copper dishing for array lines whereas the isolated line dishing does not show such a trend. The behavior is attributed to the high selectivity oxide slurry plus the accelerated oxide removal in array regions thus undoing the negative array line dishing caused by the previous step that has high selectivity copper slurry. Small pitch structures typically show more erosion, but this is not the

case in this study where less erosion occurs for smaller pitch structures. This behavior is believed to be caused by the initial copper bulge; fine array regions are cleared later than are the larger features, and thus suffer less net erosion.

B. Study 2: Minimal Set of Structures for Typical Pattern Effects

In this section, we show a "minimal" set of data that provide for rapid evaluation of CMP dishing and erosion trends. As a minimum set of structures to evaluate dishing and erosion, a line/array structure as described in Chapter 3 is needed for a small feature (e.g. 0.5 μm line), a medium feature (e.g. 5 μm line), and a large feature (e.g. 100 μm line). These measurements provide "corners" for minimum and maximum dishing and erosion for a typical process. Field oxide thickness measurements are also needed for field oxide loss near array regions, especially if a process suffers from significant field oxide loss. The acquired data then are plotted against the chosen pattern factors and can be compared among different processes or parameter settings.

In this study, wafers (8 inch) are patterned with multi-level copper mask v2.0 (nearly identical to the v2.1 mask described in Appendix B and similar structures to those in the single-level mask v1.2). After patterning, wafers are electroplated using a conventional rather than superfill plating process on a Semitool machine, and polished using an Applied Materials Mirra CMP tool with a slurry where the removal selectivity between copper, barrier, oxide is similar.

Figure 6.15 shows data taken on three pitch structures with the indicated line width and line space. The structure consists of an array region and two isolated lines of the same line width, and a profile scan is made across the middle of each structure as shown with the dashed line. The dishing for the isolated lines is all greater than the associated array line, except in the large feature case where a similar amount of dishing is shown. Thus, it

is important to indicate whether reported dishing comes from an isolated line or from an array line. We observe that the three profiles can be classified into three regimes according to the array region behavior: erosion dominant, dishing dominant, and dishing/erosion dominant. The small feature array shows erosion across the structure but negligible array line dishing, and the opposite is shown for the large feature array where dishing dominates the thickness loss with minimal recess across the array. The combined effect of dishing and erosion is seen for a medium size feature where both erosion and dishing is present across the array region. This illustrates the dominant effect for different feature sizes and indicates that a process must be tuned to reduce erosion for lower device layers that contain relatively small features, and tuned to reduce dishing for upper layers where large features such as bond pads are present.

The magnitude of dishing and erosion are extracted from profiles, and are plotted in Figure 6.16. The plot on the left shows the dishing trend for both isolated line and array line, and the erosion trend as a function of feature sizes. Total copper line loss is shown on the right, computed as the sum of erosion and dishing. There is minimal field loss in this case. Because more dishing is seen for a large feature than erosion for small features, the total copper loss is greater for large pitch arrays.

Study 2 thus illustrates two points. First, a substantially different CMP process behavior compared to that in study 1 is observed, without the unusual "reverse dishing." This conventional CMP process shows more commonly reported dishing, erosion, and total copper loss trends as functions of feature size. Second, this study also demonstrates that rapid evaluation of key pattern trends can be achieved with a small number of judiciously selected test structure measurements.

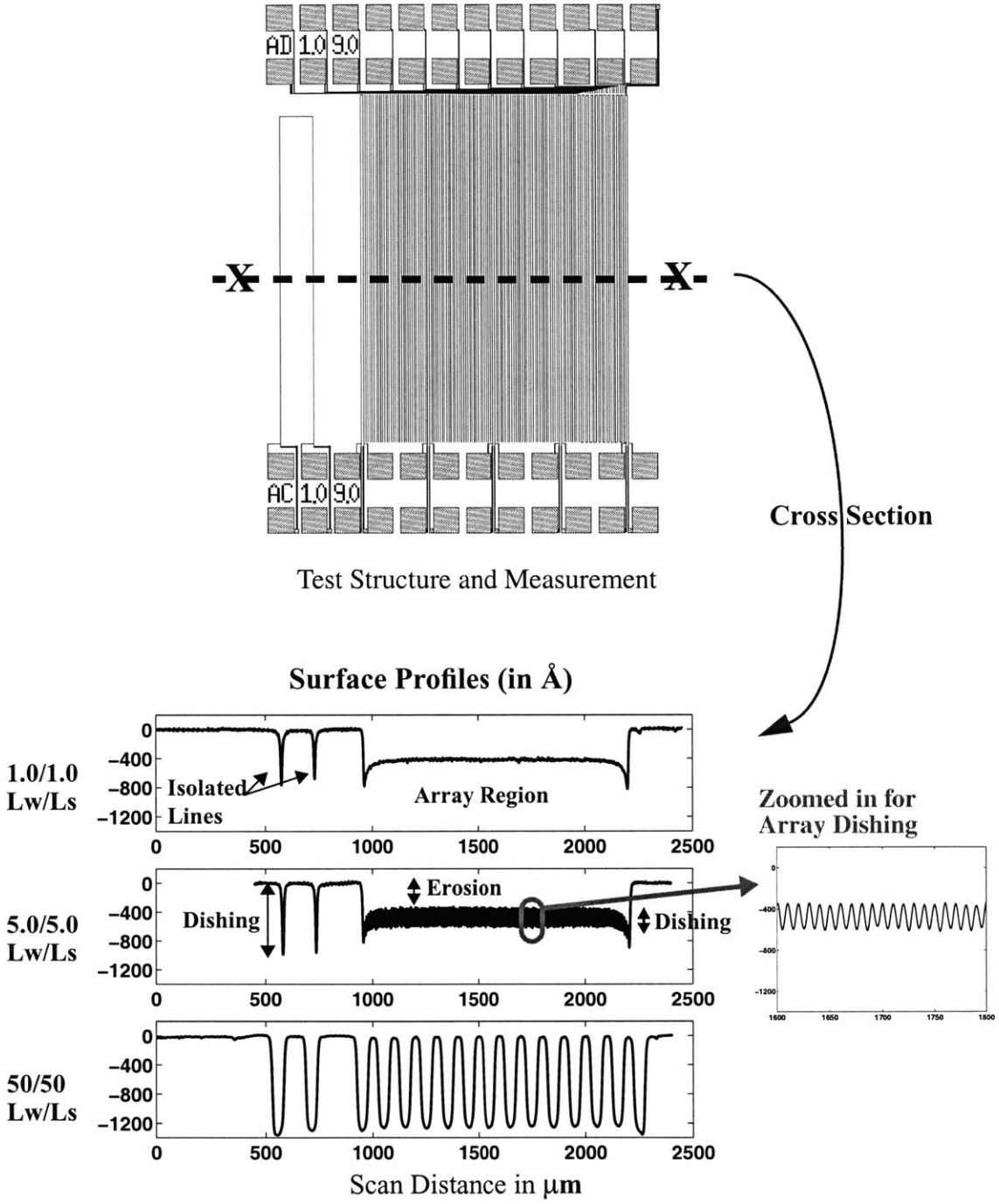


Figure 6.15: Surface Profiles Showing Dishing and Erosion Trends in the Line/Array Structures

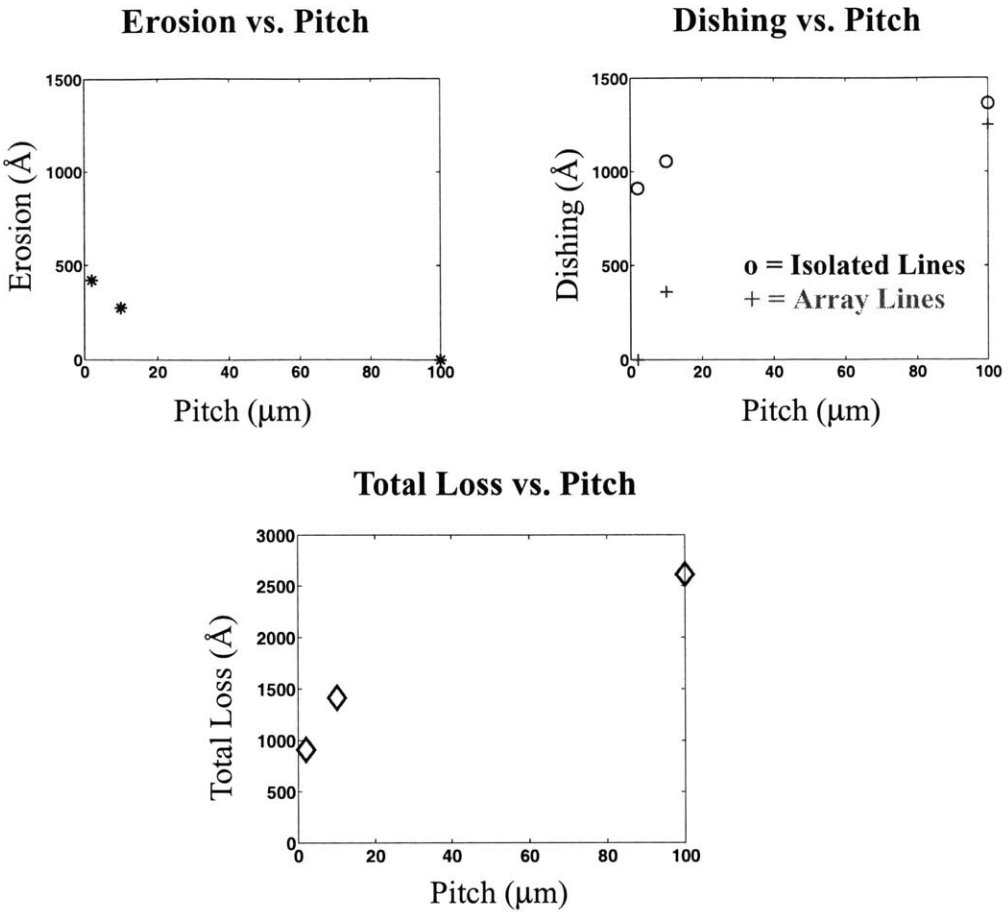


Figure 6.16: Surface Topography and Copper Thickness Variation vs. Pitch

C. Study 3: Detailed Pattern Trends and Pad DOE

In this study, we show detailed pattern effects, including a line width effect for a fixed line space, and a line space effect for a fixed line width. We also examine dishing and erosion for two different pads. Wafers are patterned with the metal 1 layer of the multi-level test mask v2.1 described in Appendix B where the basic pattern structure is similar to the one used in the single-level mask v1.2. Patterning of the wafers is followed by barrier deposition, copper seed deposition, and electroplating using a superfill chemistry. For polishing, an Applied Materials Mirra CMP tool is used with down force of 3 psi and table speed of 93 rpm with Cabot 5001 slurry. Two different pads are considered: Pad A is a standard

IC1000/Suba4 with K-groove, and Pad B is an IC1000 pad (no subpad) with XY groove without subpad. Wafers are polished to endpoint for the bulk copper removal and subsequent overpolish is done for a time estimated to remove about 500, 1000, and 2000 Å of copper in field areas.

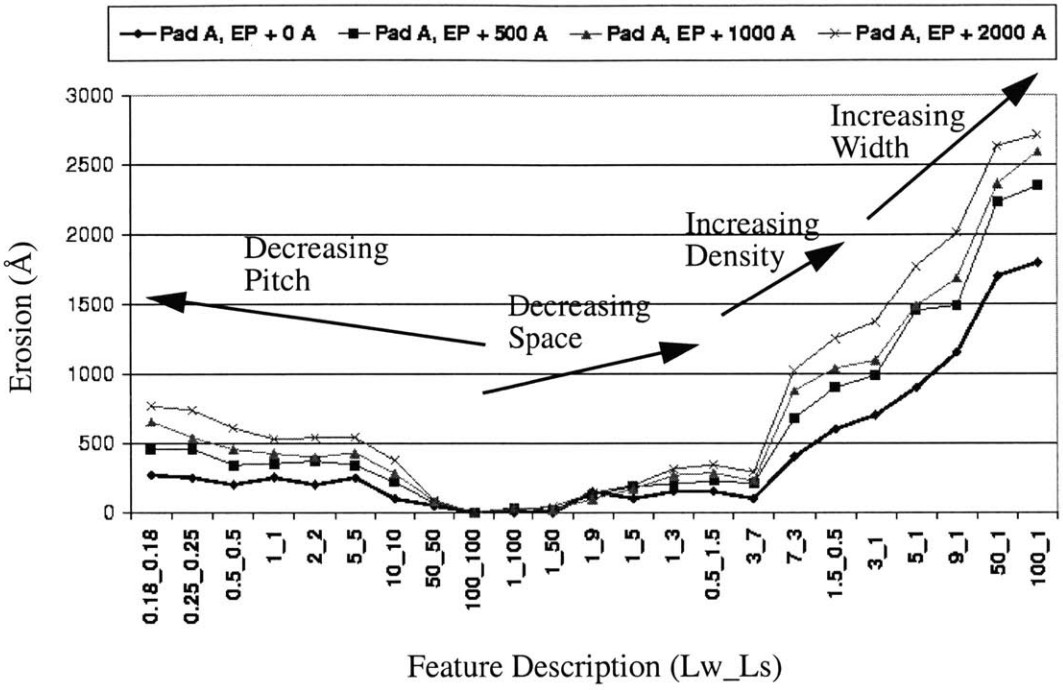


Figure 6.17: Erosion for Pad A vs. Features

Figure 6.17 shows erosion across each array region for various pattern structures (labeled as "Width_Space" on the horizontal axis) for Pad A. The test pattern features can be divided into four sets. The first set shows an increase of recess as pitch values decrease. The next set, having new test patterns where line space is varied for a fixed width of 1 μm, shows a slight increase in erosion once the line space becomes relatively small. The third set are density structures where two different density environments are formed for two different pitch values of 2 μm and 10 μm. Data indicates higher erosion for higher copper pattern density. The forth set consists of structures with a fixed space of 1 μm and varying line width. As the graph shows, there is a significant amount of recess when the width

increases. The accelerated erosion is due to both small line space and high density formed by large line width. The erosion trend also indicates that there is increased erosion with more overpolish. The erosion trend for Pad B shown in Figure 6.18 is similar to that observed for Pad A but shows generally less erosion.

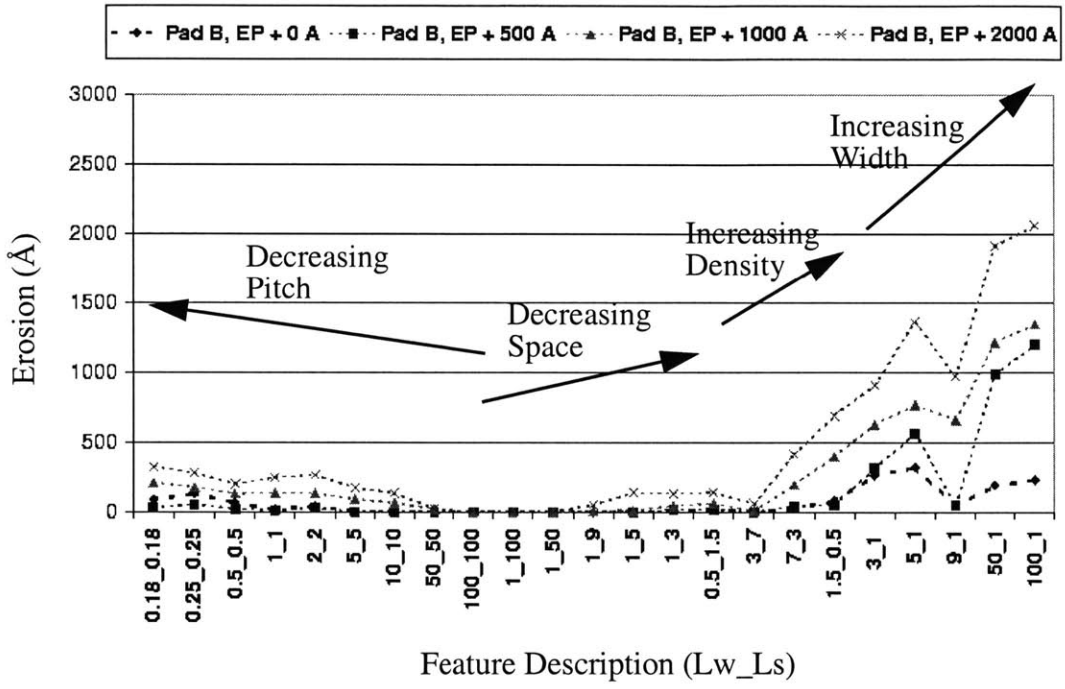


Figure 6.18: Erosion for Pad B vs. Features

Figure 6.19 and Figure 6.20 show array line dishing for Pad A and Pad B, and Figure 6.21 and Figure 6.22 show isolated line dishing for Pad A and Pad B, respectively, for the same set of features. In general, dishing is seen to increase as line width increases, and decrease as the line space increases. Although there are similar trends of dishing for the array lines and isolated lines, there are also definite differences. Especially notable is the fourth set of structures with increasing line width and fixed line space where substantial dishing is observed for isolated lines. Similar to the erosion behavior, smaller dishing is observed for Pad B for both isolated and array lines. It is hypothesized that the higher stiff-

ness of Pad B compared to Pad A planarizes over a longer length scale due to less pad bending and causes less erosion and dishing.

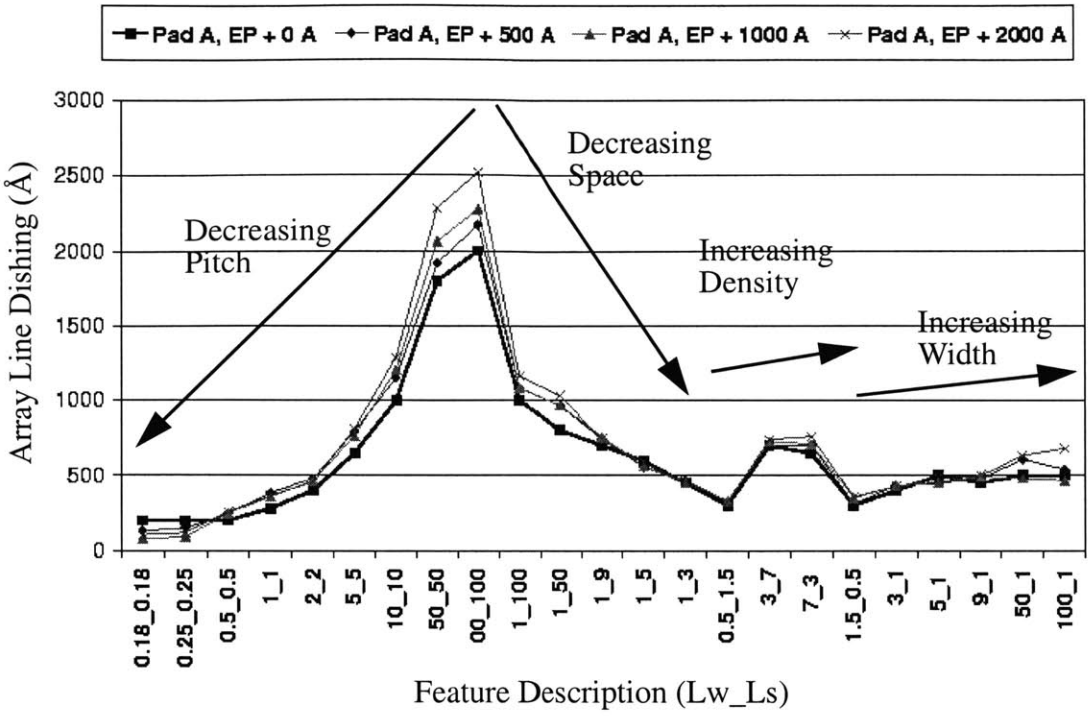


Figure 6.19: Array Line Dishing for Pad A vs. Features

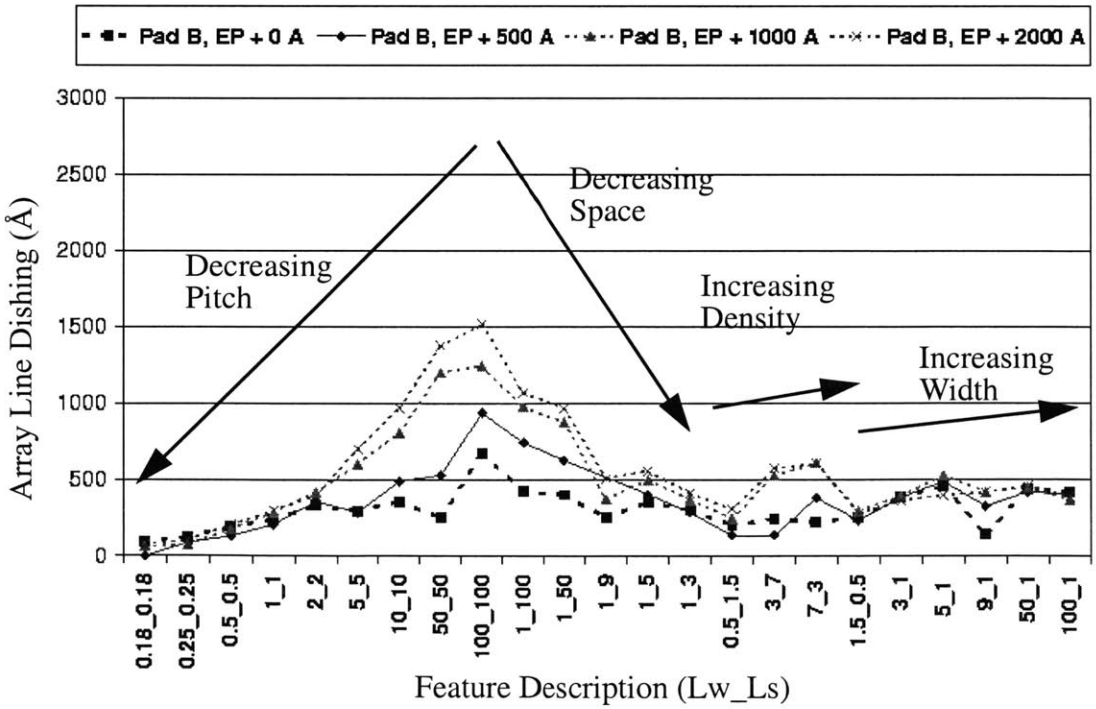


Figure 6.20: Array Line Dishing for Pad B vs. Features

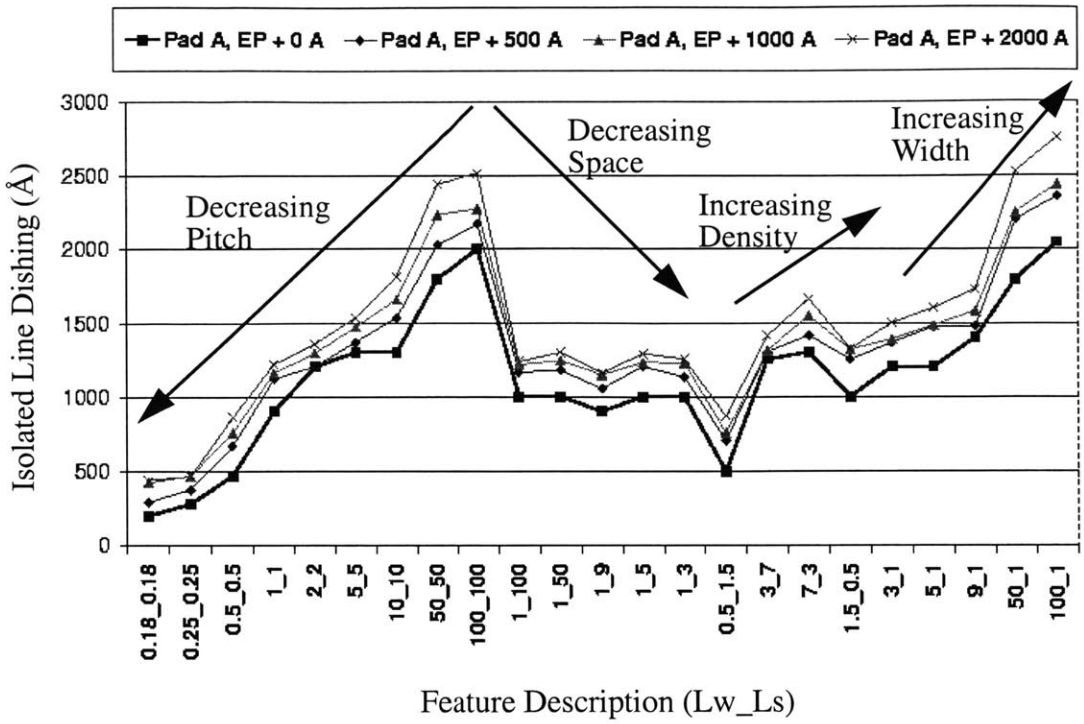


Figure 6.21: Isolated Line Dishing for Pad A vs. Features

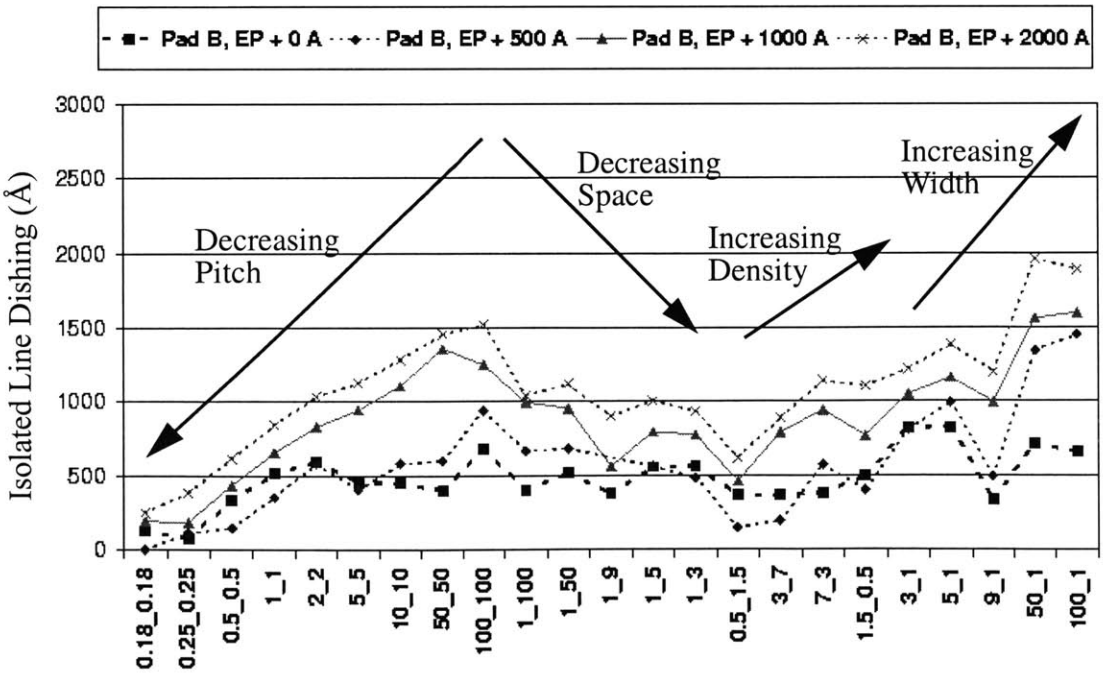


Figure 6.22: Isolated Line Dishing for Pad B vs. Features

As we have observed in all three data sets, the test masks enable exploration of key pattern effects in the copper CMP process across various tool settings and conditions. Furthermore, these observed trends show that there are additional effects beyond pattern pitch and density as once originally assumed, and Study 3 shows line space and line width effects that have a significant influence on dishing and erosion. The characterizations themselves are important for understanding process limitations, and aid monitoring or optimizing processes. In addition, the developed test masks and characterization of pattern effects are the basis for semi-empirical or physical modeling of the CMP process so that the pattern effects can be simulated and predicted for other kinds of layout through calibrated model parameters.

6.2 Multi-Level Pattern Effects and Propagation

Characterizing and modeling of metal 1 polish with a uniform underlying oxide topography, as presented in Section 6.1, is crucial in understanding copper CMP. However, we also need to understand multi-level polishing issues to complete our picture of how copper CMP behaves and how it can be modeled. For this purpose, we use the developed two level mask set dedicated to studying the multi-level pattern effects in polishing of copper. The test masks utilize electrical test structures and the analysis framework discussed in Chapter 3 and presented in [22]. The electrical data analysis has been found to be particularly useful for multi-level CMP characterization where surface a profile scan does not necessarily indicate the remaining copper thickness profile. It has been found that the use of both surface profiles and electrical measurements are necessary to obtain a complete picture of the polished thickness and surface variations.

6.2.1 Review of Multi-Level Structure and Mask Description

The test vehicle used in this study is a multi-level mask set (metal 1, via, and metal 2) designed with electrical test structures. The full description is found in Appendix B, and the key structures are highlighted in this section. The goal of the mask set is to understand multi-level effects of metal 1 (M1) on metal 2 (M2) with a wide range of density and pitch structures as shown in Figure 6.23. Since this mask is more complicated than the single level studies we have shown so far, a review of the key structures is given in this section.

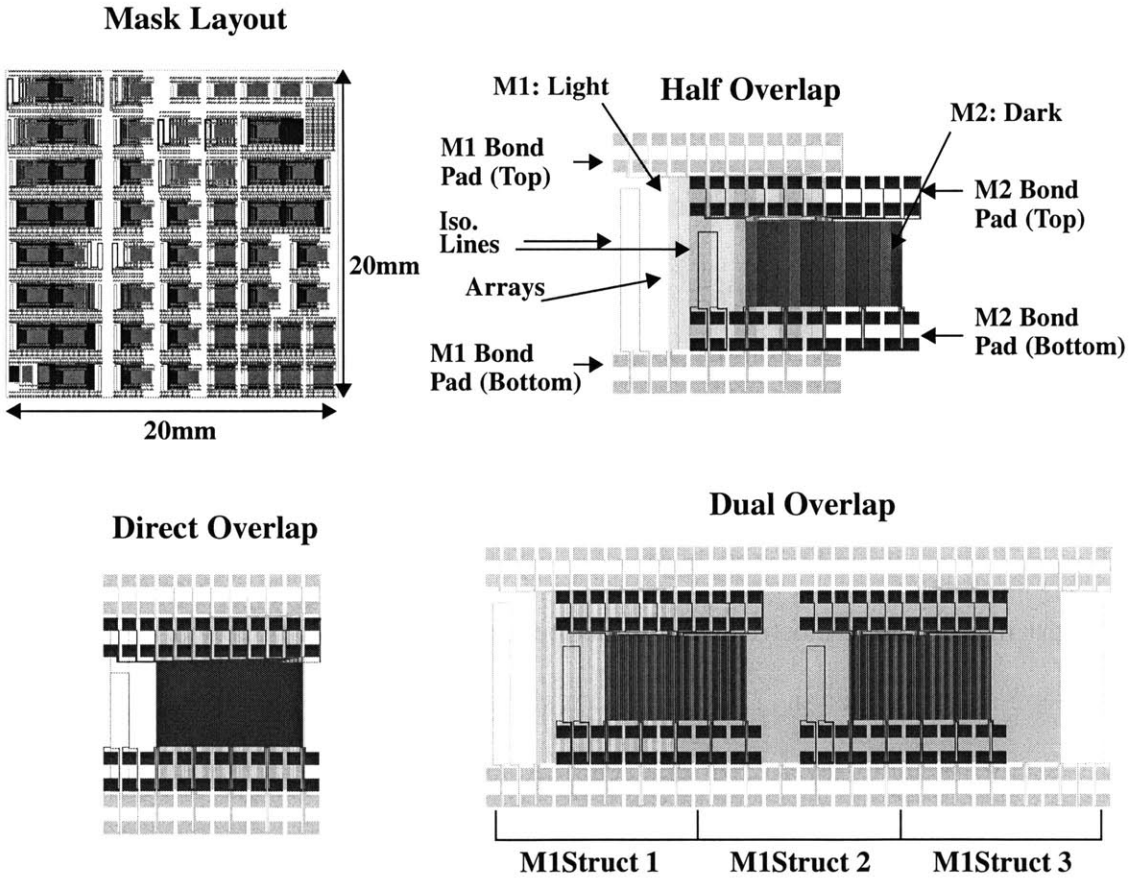


Figure 6.23: Mask and Test Structure Layout

Metal 1 and 2 contain test structures (isolated line and an array of lines) forming various overlap cases: direct, half, and dual overlaps. In the direct overlap case, the M2 struc-

ture is directly over an M1 structure, and in the half overlap case the M2 structure is half-over the M1 structure and half-over the oxide. In the dual overlap case, there are two different M1 structures right next to each other (with different density or layout parameters), and the M2 structure is half-over one M1 and half-over the other M1 structure.

All of the M1 and M2 structures (except the middle structure in the dual overlap case) consist of an isolated line pair and an array of lines forming different pitch and density regions by varying line widths and spaces. The line width of the isolated line pair is the same as that used in the corresponding array. The array region for each M1 structure is about 1250 x 1610 μm and two sets of bond pads (one at the top and one at the bottom of the array region) are used to measure the line resistance. The bottom set of pads is used for the measurement of the isolated line as well as to sample from the array of lines at equal distances from the left edge of the array to the right edge. The top set of pads are used to measure lines at finer increments near the transition regions.

The array region of the M2 structure is about 1250 x 800 μm and is placed within the M1 structure so that M2's polishing behavior is influenced by M1 non-uniformity only. Each M2 structure has the same bond pad and measurement configuration as the M1 structure. However, the transition regions on M2 are created both by the M2 structure itself as well as by the underlying M1 structure. Thus, depending on the overlap case, some M2 structures are measured only at one edge of the array or some are measured both at the edge and center of the array where the M2 center is directly over the edge of M1 structure. A via layer is used to connect M1 pads to M2 pads, which are placed directly over the M1 pads, so that test structures on M1 could be measured also after M2 polish.

6.2.2 Experimental Setting

The experiment considered here was carried out at SEMATECH using 8 inch wafers in a single level damascene process where each metal layer (M1, via, and M2) has its own dielectric deposition, pattern and etch, barrier layer and copper deposition, and polishing. The nominal designed metal thicknesses are 0.8 μm for both M1 and M2.

M1 polish is done with a given process for the purpose of creating non-uniform topography and M2 polish is done with different process settings. The surface profiles are measured using a Tencor P10, and electrical testing was done on an HP4062. SEM cross sections are also used to verify data. The copper thickness extraction procedure outlined in [22] is used to obtain remaining copper thickness from electrical line resistance.

Figure 6.24 illustrates the processing sequence in a schematic format (excluding the via layer for the sake of simplicity). (1) After metal 1 polish, there is a certain amount of oxide recess across a structure region. (2) Because of this starting recess on the metal 1 layer, conformally deposited metal 2 oxide has a similar recess shape as the metal 1 recess. (3) The pattern and etch of the uneven oxide makes the bottom of the copper trenches uneven, and the copper deposition profile is also influenced by the uneven profile shape. (4) After copper deposition and polishing, additional metal 2 recess and dishing occurs, and the remaining line thickness varies in a complex fashion in both an overlap region and non-overlap region. Our goal in this work is to understand the basic effect of CMP and metal 1 topography on metal 2 surface heights and line thicknesses. Modeling of the metal 2 polish effects, based on extensions of the CMP model summarized in Section 6.3, remains a topic for future research.

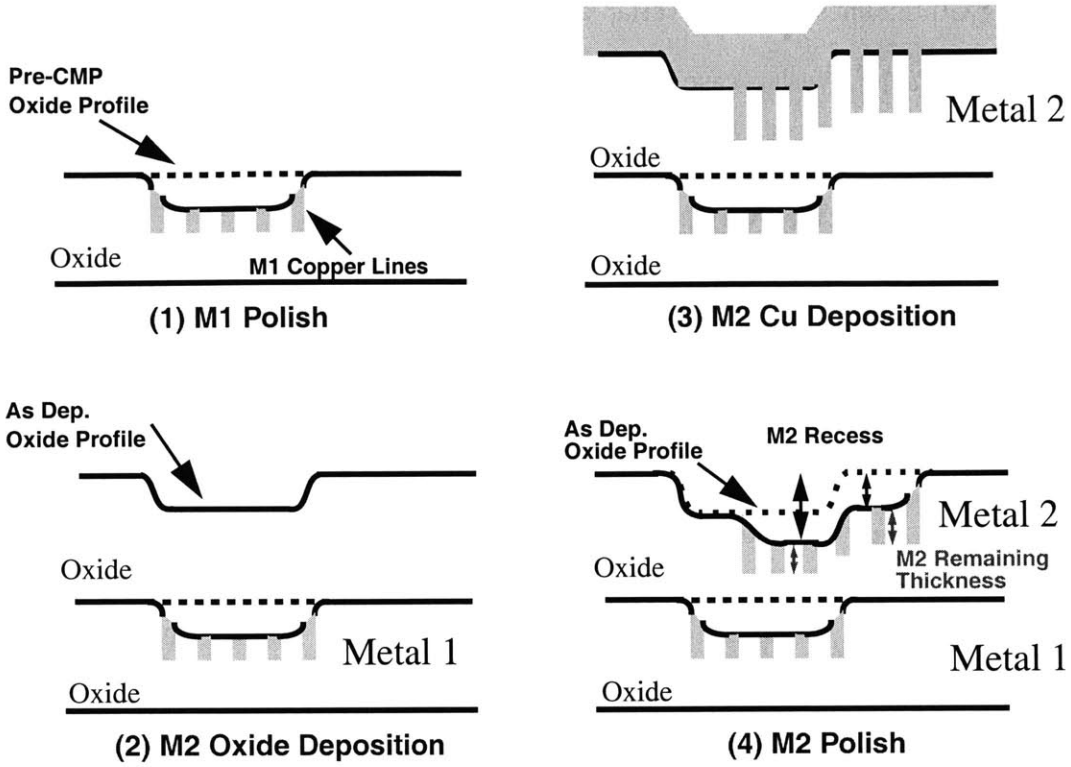


Figure 6.24: Multi-level Process Sequence

6.2.3 Experimental Result And Discussion

Figure 6.25 through Figure 6.27 show surface scans and electrically extracted remaining Cu thicknesses of M2 and M1 for three different overlap cases with M1 and M2 cross sections for one process setting. Note that the cross sectional schematic view and all data plots are aligned vertically. Also shown is data for a reference "no overlap" M2 structure without any underlying M1 topography (no structure on M1). The the direct overlap case is shown in Figure 6.25 with a schematic view of both M1 and M2 on the bottom of the figure. M1 recess is present due to the erosion across an array region, and also shown are dishing from two isolated lines. In M2, the whole structure region is recessed, and the M2 overlap structure shows *more* surface recess than in the reference structure. The electri-

cally extracted Cu thickness profiles follow the surface scan profiles and show higher remaining Cu thickness for the overlap compared to the no overlap (reference or no M1) case. Although the overlap case has a higher amount of accumulated recess, since the starting topography on M1 is also recessed due to M1 erosion, the final effective M2 Cu thickness is greater in the overlap case.

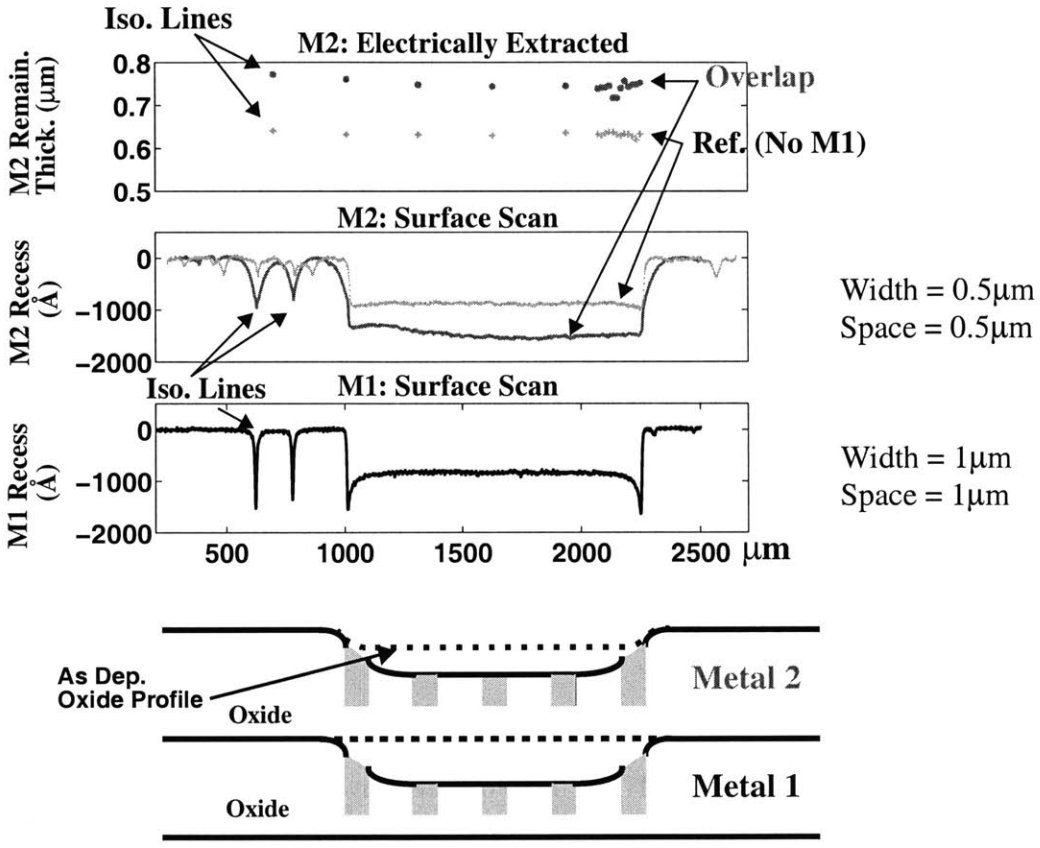


Figure 6.25: Direct Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

In the half overlap test structure results shown in Figure 6.26, the surface scan shows the most recess in the structure overlap region and slightly less in the oxide overlap region. Because the initial polished M1 profile is not flat due to M1 erosion, M2 electrical thicknesses do not identically follow the surface recess scans. Rather, M2 Cu line thickness depends on both the M1 recess and the M2 polish behavior: it is essential to measure both

the line thickness and the surface profile to construct an accurate picture of the resulting M2 structure. Even though the structure overlap region has higher M2 recess, the remaining Cu thickness is greater in that region. In the dual overlap case of Figure 6.27, the M1 surface profile is constructed from electrical measurements ("o" are electrical data points), showing the recess difference between two neighboring structures: one structure having line width and space of 0.5 μm and the neighboring structure having line width of 2.5μm and line space of 7.5 μm. Similar to the half overlap case, the final M2 Cu thickness is greater over the more recessed region on the surface scan. Also seen in both the half and dual overlap cases, the remaining Cu thickness changes from one overlap to another overlap region, more so than the amount of erosion.

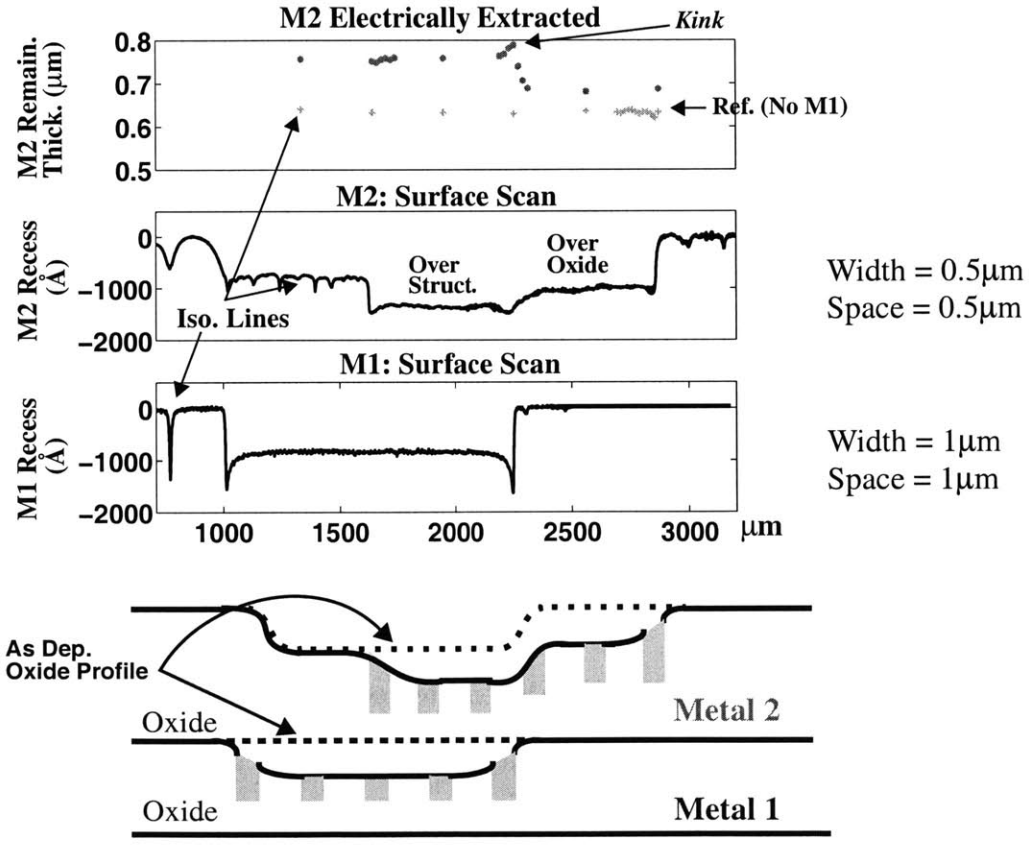


Figure 6.26: Half Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

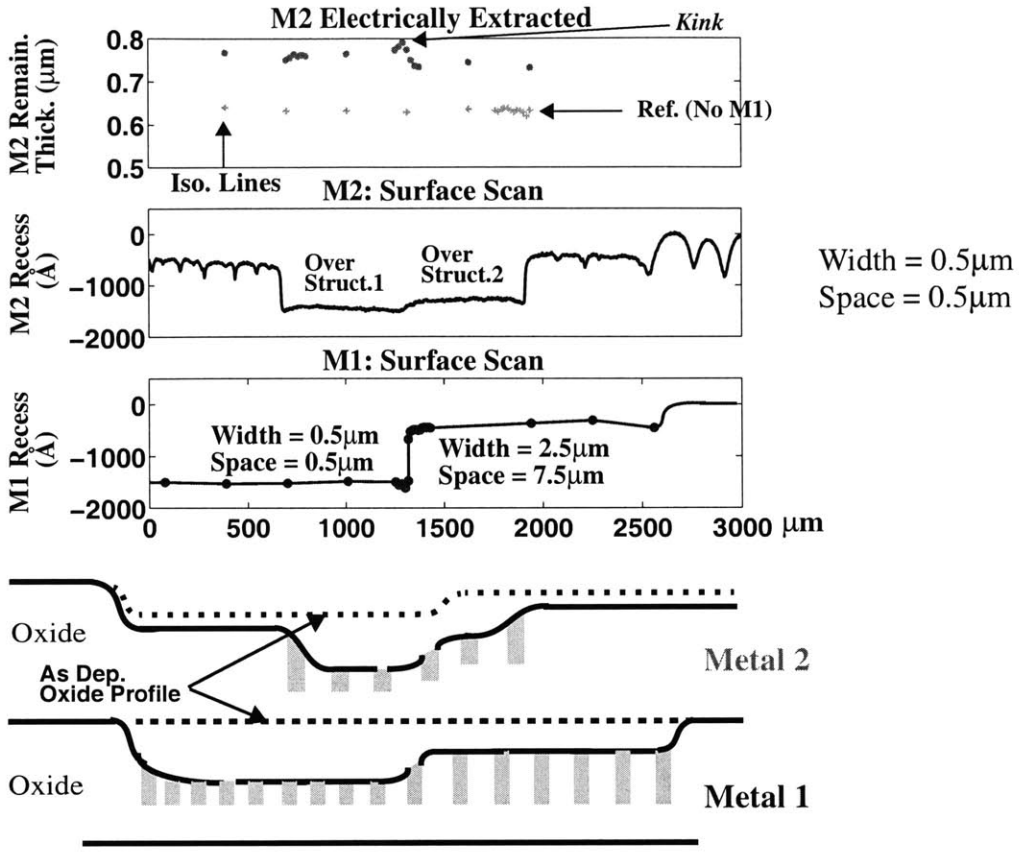


Figure 6.27: Dual Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

In terms of M2 recess vs. M1 recess, we can investigate how much recess on M2 is introduced by the M1 recess. The observed trend is that more total recess on M2 results as the amount of M1 recess increases. However, the M2 remaining thickness increases even though the total surface recess on M2 increases. Thus, the M2 recess is primarily due to the initial starting recess on M1 and that is causing M2 recess to appear greater. Thus, the *additional* recess created during M2 polish is decreased somewhat when the M2 structure already resides with an M1 recessed region. This is consistent with a notion of reduced pad pressure on low areas of the chip caused by M1 recess. We also note a slight "kink" on the M2 remaining thickness right at the transition region for the half and dual overlap

cases. This effect is due to the edge effect on M1 where there is slightly more recess (or edge dip) at structure transitions.

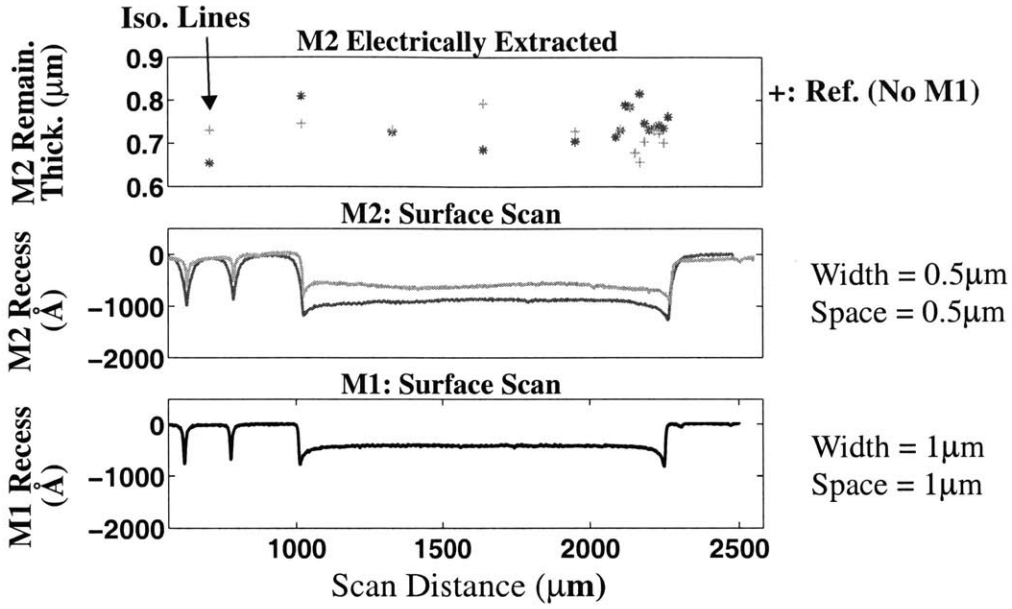


Figure 6.28: Direct Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

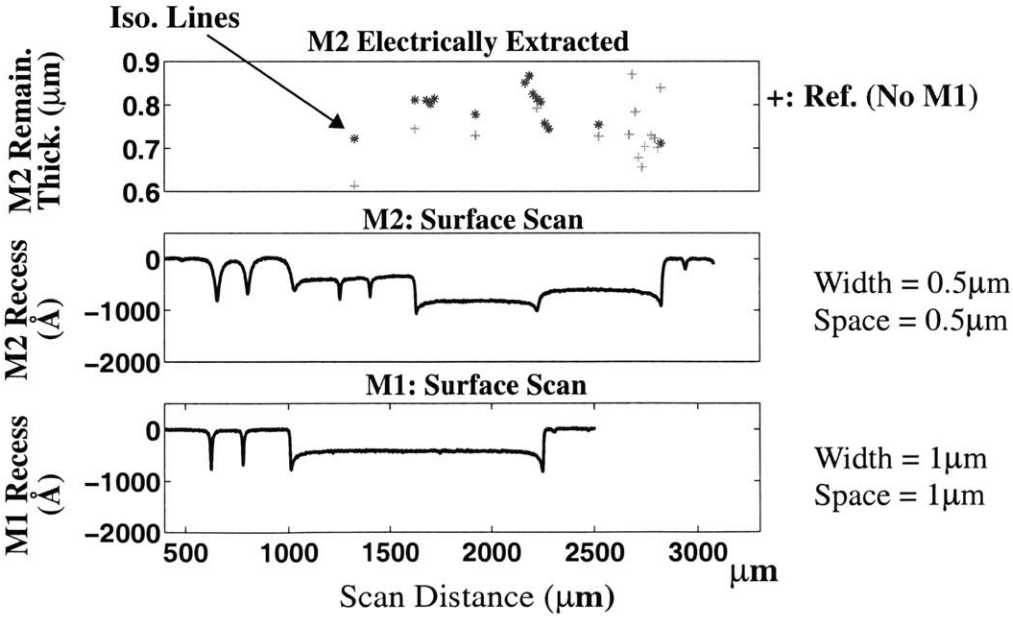


Figure 6.29: Half Overlap: M1 and M2 Surface Profile and Extracted Cu Thickness

Shown in Figure 6.28 and Figure 6.29 are similar thickness and surface plots for a different consumable and process setting. For this process, the difference in the M2 recess and the M2 remaining thickness between the overlap case and no overlap case (reference structure with no M1) is small in contrast to the earlier observation. However, the half overlap case in Figure 6.29 shows higher remaining line thickness in the overlap region compared to the region over metal 1 oxide, and this is consistent with what we observe in the previous case.

Finally, we are also interested in multi-level structure impact of copper dishing. Figure 6.30 shows propagated M1 dishing on M2, and the degree of the propagated dishing is less in the overlap region compared to the no overlap region. Figure 6.31 shows propagated M1 recess on M2 with M2 structure dishing where the dishing is constant in both the overlap and no overlap regions. We would expect the dishing to be constant in both regions, assuming dishing occurs on a local length scale and depends primarily on line width.

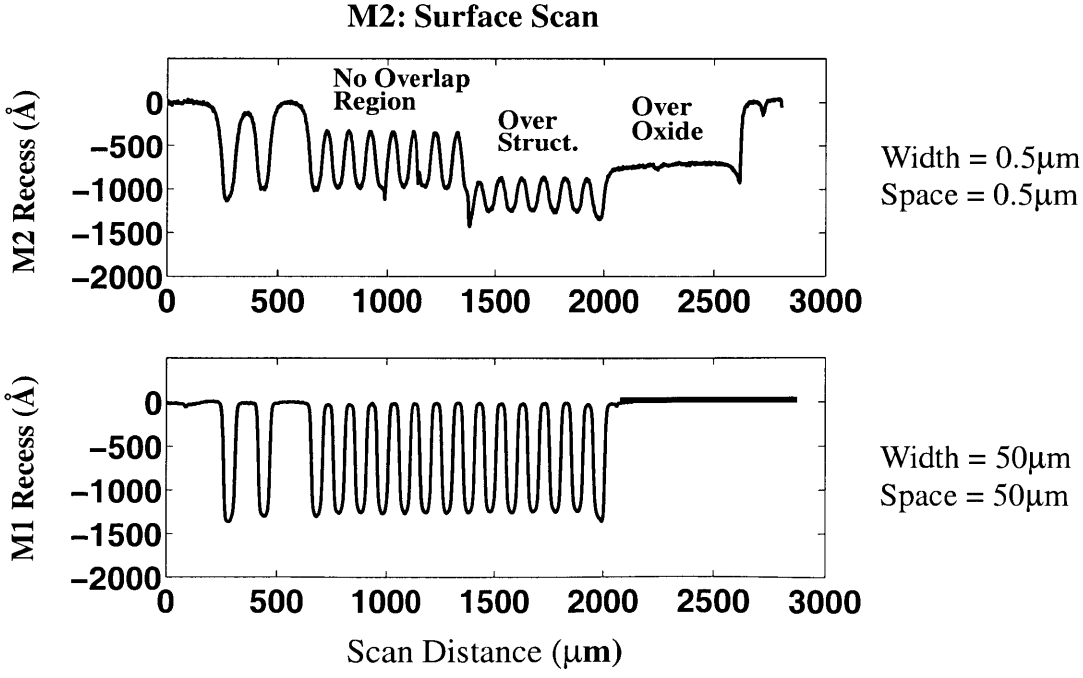


Figure 6.30: Surface Profiles for Half Overlap: Propagation of M1 Dishing to M2 Profile

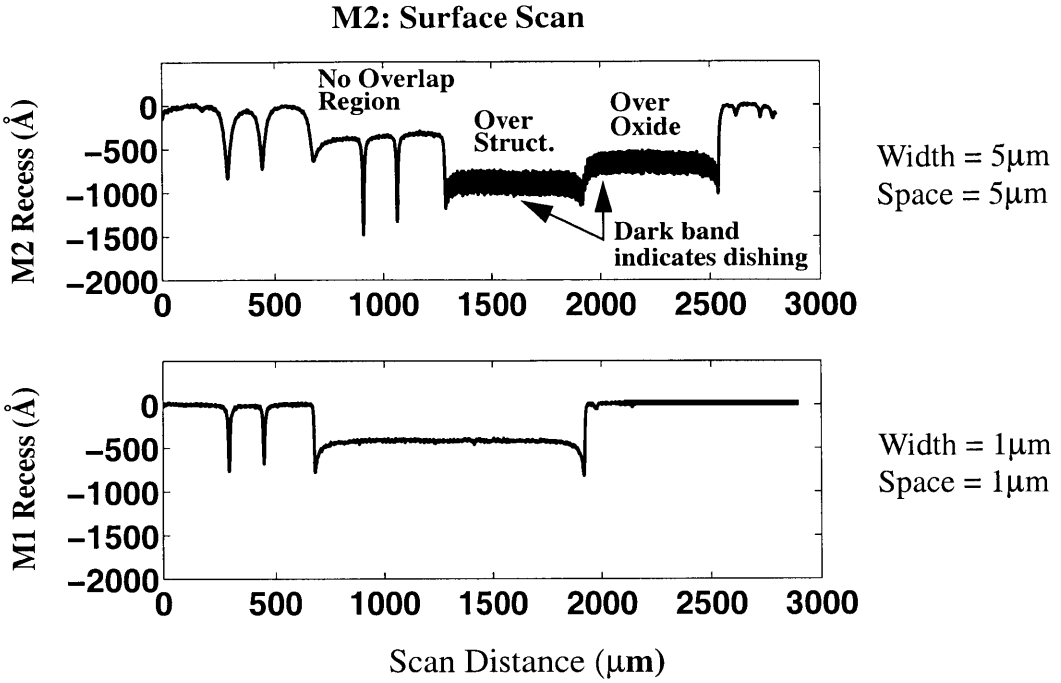


Figure 6.31: Surface Profiles for Half Overlap: Propagation of M1 Recess to M2 Recess and Dishing

Characterization of multi-level pattern effects have been presented to gain a qualitative understanding of how layout pattern and initial non-uniform topography influence metal 2 polish. This understanding is crucial for improved process development, optimization, and integration. The qualitative data from these studies will be helpful in future multilevel model development to capture the CMP dependencies and to predict such multilevel polishing characteristics on other kinds of layouts. In the next section, an existing CMP model for prediction of single level CMP effects is presented, based on the quantitative experimental data presented in Section 6.1.

6.3 Modeling of Pattern Dependency in CMP Process

We have presented so far how the developed test masks are used for the characterization of pattern dependent CMP problems of dishing and erosion. In this section, we

present a review of an existing CMP model, developed elsewhere, that relates removal rates of different regions and materials through the combined interactions of contact mechanics, pattern density, and step height. This model is provided as background, and to illustrate how the characterization work presented in Section 6.1 is used in calibrating such a CMP model. In addition, a basic understanding of the CMP model is necessary to understand the integration of plating and CMP models presented in Section 6.4.

Various CMP models have been reported [37, 38, 39, 40, 41]; here we focus on the integrated contact mechanics and density-step-height model developed by Tugbawa et al. [37, 41]. First, contact mechanics can accommodate the long range initial thickness variation caused by copper electroplating, and also accounts for the evolution of surface topography as polishing progresses. A polishing pad is treated as an elastic body as shown in Figure 6.32. The displacement of the pad, w, is related to the contact pressure p [42, 43]:

$$w(x,y) = \frac{(1-\upsilon^2)}{\pi E}\iint_A \left(\frac{p(x,y)}{\sqrt{(x-\xi)^2+(y-\eta)^2}} \right) d\xi d\eta \tag{6.1}$$

where discretized boundary elements are considered with boundary conditions. When the pad contacts the wafer, p is unknown but w is set by the wafer surface:

$$w_{i,\,known} = W_{Ref} - W_{i,\,wafer} \tag{6.2}$$

When pad is not in contact, w is unknown but p is known by:

$$p_{i,\,known} = Q_{Ref} \tag{6.3}$$

where Q_{Ref} is the reference pressure exerted by the tool on the pad. Using these equations, one can solve for pressures and displacements at each point in time, and compute removal rate for each location. For example, if a region has a thickness at the reference level (field

level), then the region would polish at a blanket removal rate. If a region has a bulge, then it would see higher pad pressure and the removal rate would increase.

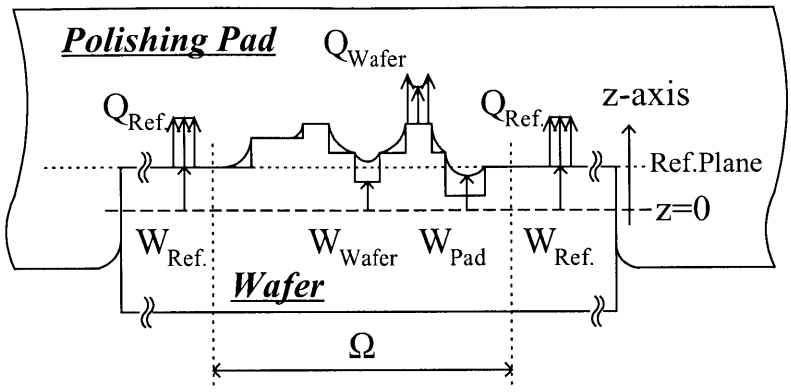


Figure 6.32: Contact Mechanics from Yoshida [43]

Second, the density-step-height model [37, 41] accounts for the removal rate dependency of pattern density and step height as pictured in Figure 6.33 and Figure 6.34 for stage 1 and stage 3 polishing, respectively. Here stage 1 is the bulk copper polish, stage 2 is barrier polish, and stage 3 is the overpolish. In bulk copper polishing as shown in Figure 6.33, if the step height is greater than some critical value, H_{ex}, then it is assumed that there is no contact in the down area and thus no removal in the down area. All pad pressure is distributed on the up area, and the up area is polished inversely proportionate to the up area pattern density. If the up area pattern density, ρ_{Cu}, is high, there are more regions supporting the pad and thus the removal rate is low, whereas the removal rate is high if the pattern density is low as there is less raised copper (above oxide spaces) to remove. As a result, the up area is initially polished at the blanket copper polish rate, R_{Cu}, divided by ρ_{Cu}. As the step height is decreased to below H_{ex}, the pad is assumed to touch both the up and down areas so that there is pressure distribution between the two. This would cause the up area removal rate to decrease linearly while the down area removal rate to increase

linearly. As the step height further decreases and approaches zero, the wafer surface becomes blanket-like, and the up and down area removal rates converge to the blanket removal rate.

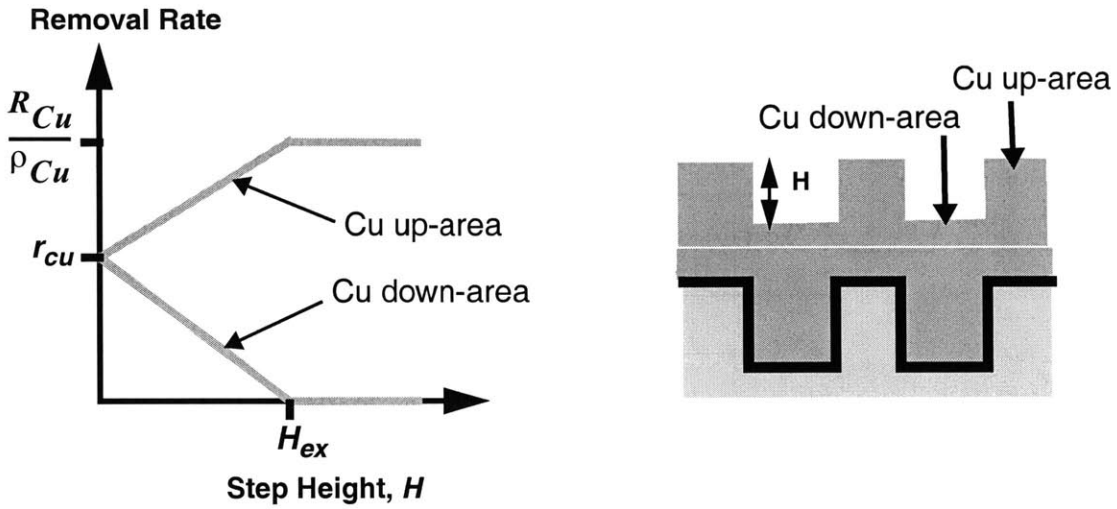


Figure 6.33: Stage 1: Removal Rate Diagram

In the overpolish stage, we are polishing two materials, copper and oxide, but the general pattern density and step height dependency is the same as shown in Figure 6.34. Initially, the two materials are flat and polish at their respective blanket rates. As a step height is created by copper dishing, the removal rate of the up area, which is the oxide, increases, while the removal rate of the down area, which is copper, decreases. As the dishing increases to its hypothetical maximum value, D_{max}, the removal rate of the oxide saturates to the blanket rate divided by the oxide density, Φ_{ox}, and the removal rate of copper becomes zero. D_{max} is a model parameter and is defined as the dishing at which the pad exerts no pressure on the copper (down area) in the case where the oxide material is infinitely hard [37]. Thus, in this case of maximum dishing, all pressure is on the up area and the oxide is polished inversely proportional to Φ_{ox}. However, this maximum dishing case is never reached; rather the steady state dishing, D_{ss}, is reached where the removal rate of

the up area and the down area is the same. The modeling of the stage 2 for barrier layer polish is analogous to the stage 3 modeling, where we replace oxide for barrier and the model follows in a similar fashion.

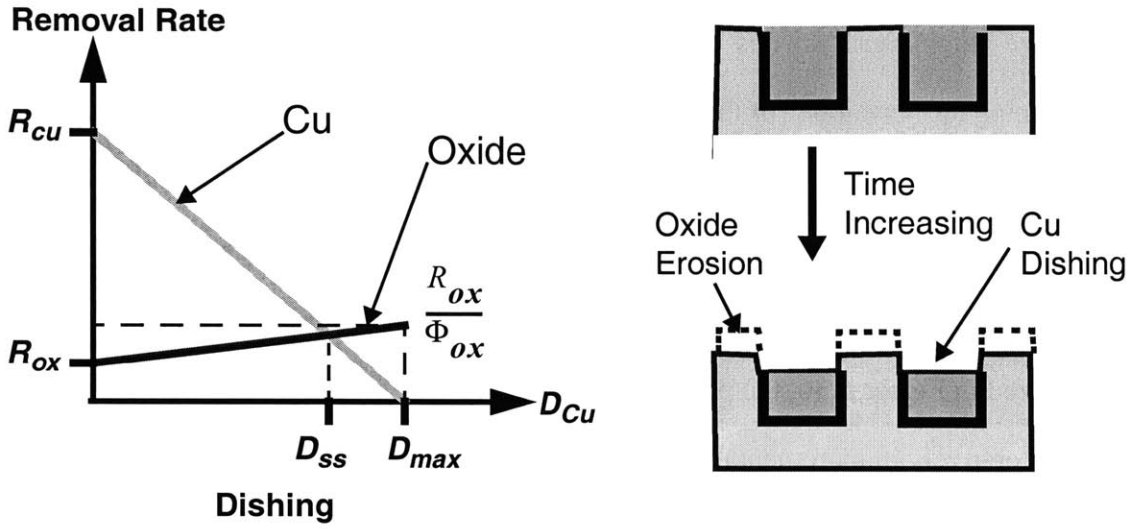
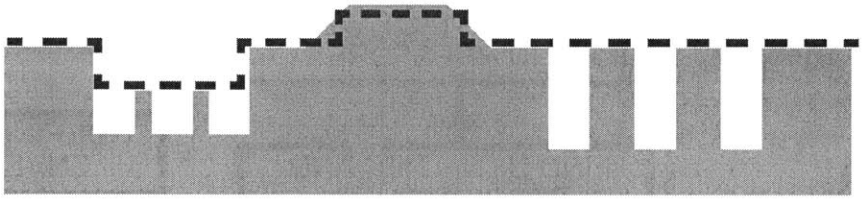
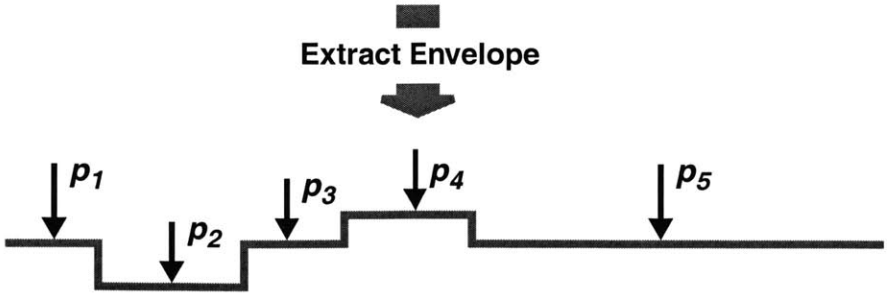


Figure 6.34: Stage 3: Removal Rate Diagram



a. Cross-Sectional View of Electroplated Topography



b. Envelope and Pressure at Various Locations

Figure 6.35: Sample Electroplated Topography and the Associated "Envelope"

The density-step-height model is excellent for capturing local pattern effects but does not take into account global height variations. The contact wear model is excellent for long-range pressure apportionment but could be computationally prohibitive if discretization is down to the feature level. Thus, these two models are integrated to capture both the long-range height variations as well as local pattern effects. The implementation begins with defining an "envelope" of the initial electroplated copper surface, which gives the relative heights of the local "up-areas" as shown in Figure 6.35. Then, the contact wear model is used to determine pressures across each of these large scale regions. The density-step-height model is used to determine up/down area removal rates within each region. As summarized in Figure 6.36, the process of finding pressure, density, and step height is carried out iteratively in incremental time, δt, while updating the profiles until the total polish time is reached.

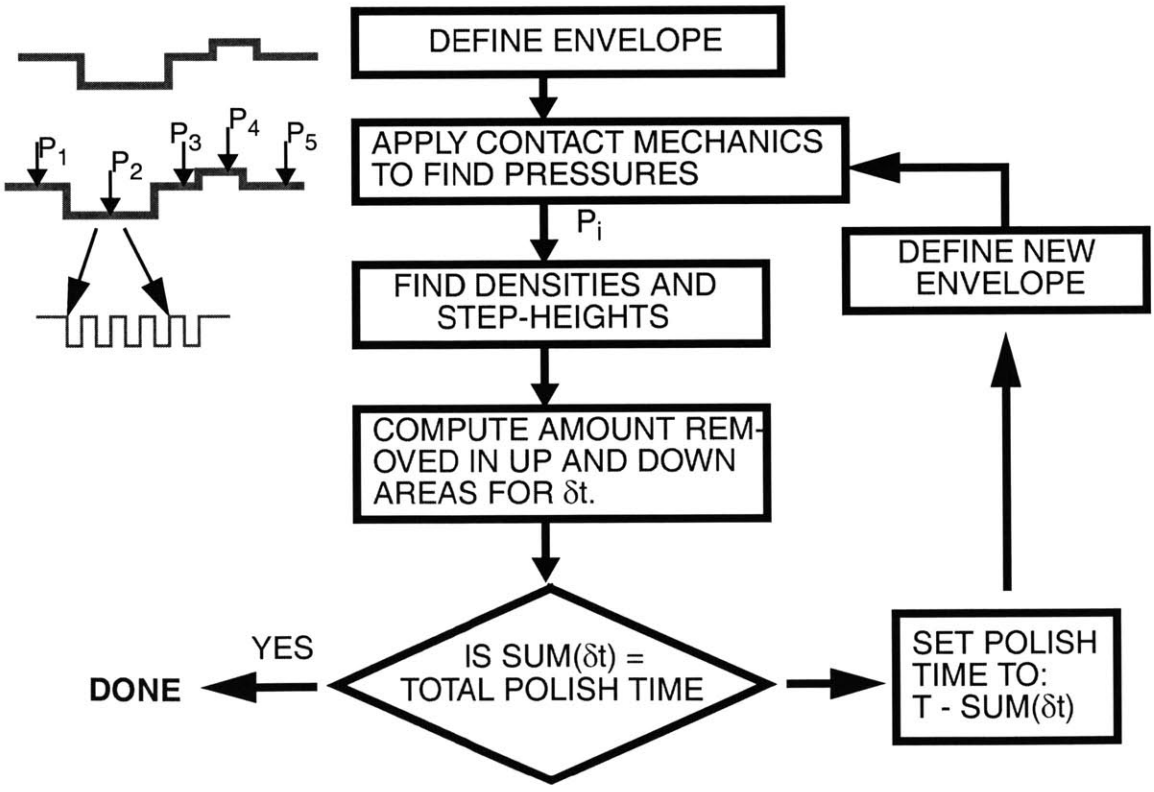
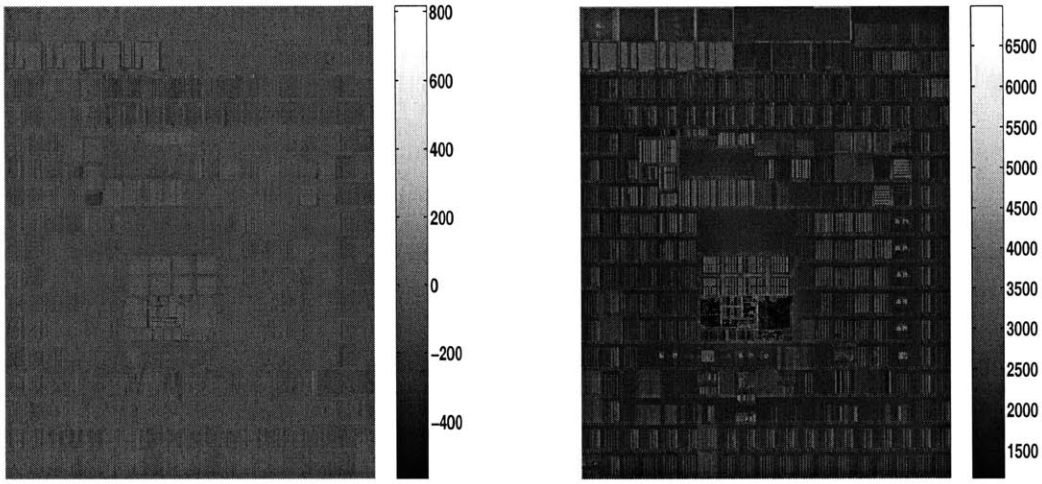


Figure 6.36: Integrated Implementation of Contact Mechanics and Density-Step Height Model

This integrated model of contact wear and density-step-height is used for chip-scale prediction of dishing and erosion for an arbitrary layout, in keeping with the overall methodology for CMP characterization and modeling as described in Chapter 2. Here we show examples of the prediction result for dishing and erosion for the same layout used for experiment A of our electroplating study presented in Chapter 5. Figure 6.37 shows such an example after the CMP process, highlighting the large range of dishing and erosion values within a single chip.



a. Dishing b. Erosion

Figure 6.37: CMP Prediction Result of Dishing and Erosion for an Arbitrary Layout

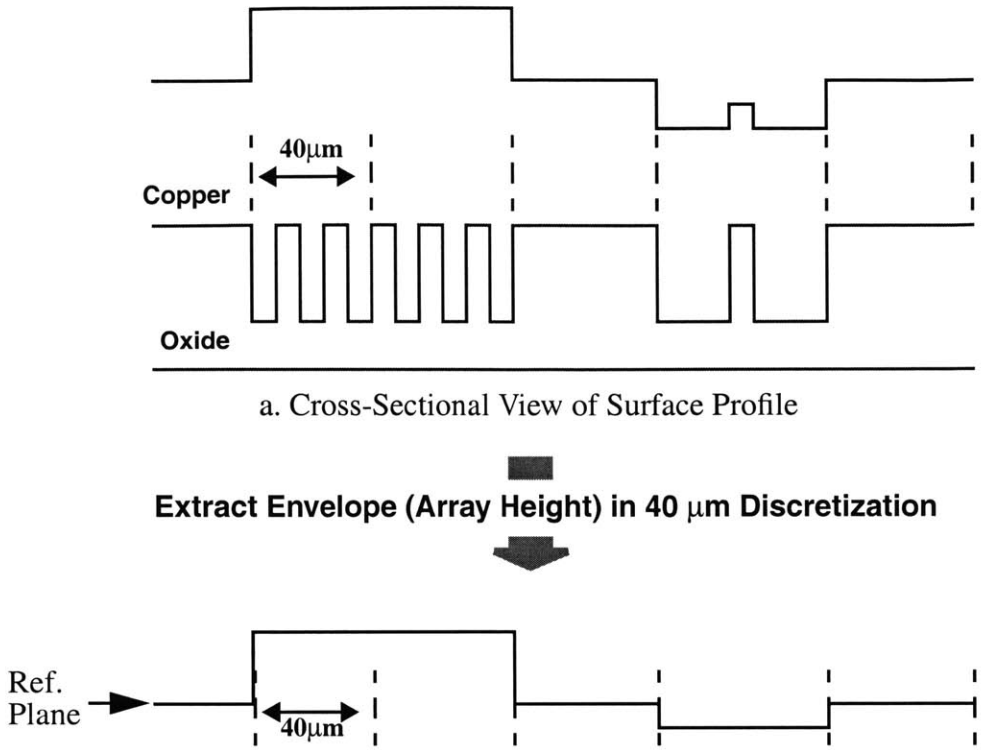
6.4 Integration of Plating and CMP Models

The overall goal of the characterization, modeling, and simulation methodology in this thesis is the efficient prediction of interconnect topography variation related to layout pattern effects. Chapter 4 has presented characterization of electroplating dependencies, and Chapter 5 has shown new methods for chip-scale prediction of surface topography varia-

tions in electroplating. Chapter 6 has presented a similar characterization of CMP pattern dependencies, and has reviewed a chip-scale CMP model which is calibrated based on characterization with test mask data.

As discussed in the previous section, the electroplated non-uniform topography has a direct impact on the CMP polishing behavior by causing differences in removal rates at different locations on a die, depending on height variations and pattern environment. Without a complete picture of the starting topography, CMP simulation does not yield adequate results because removal rates are miscalculated. This starting topography is what the electroplating topography simulation provides. In this section, we present how the topography information from the electroplating model is integrated with the CMP model, and summarize how the electroplated topography is used in the CMP model for a chip-scale simulation. Finally, an example pair of simulations is presented to show the importance of integrated plating and CMP models.

The integrated contact mechanics and the density-step-height model treats a polishing pad in a CMP process as an elastic material that deforms when pressed against the wafer surface. We note that the pad deforms and touches the top surface of the electroplated profile, and the magnitude of the displacement is determined by the relative height of the topography surface. This topography surface is the envelope and is equal to the definition of the array height which gives relative up area heights of copper referenced to field region as shown in Figure 6.38. In particular, the purpose of the envelope is to give the "overall" array height of a region, while the details of feature step heights are not important for the long-range pressure distribution. In both the CMP model and the plating model, the envelope and array height, respectively, are calculated on 40 μm x 40 μm discretized cells, as shown in Figure 6.38. Thus, array height is one of the key results from the electroplating topography simulation that is passed to the CMP simulation.



a. Cross-Sectional View of Surface Profile

b. Envelope (Array Height) in 40 μm Discretization

Figure 6.38: Envelope (Array Height) in Discretized Cells

In addition to the polishing dependence on the relative array or region heights, we have also seen that polishing has a strong dependence on pattern density and feature step height. The pattern density and step height are thus another input required by the CMP simulation. These correspond directly to the results of the "topography density" and step height simulations in the electroplating model. The topography density is often different than the layout density as noted in Section 5.5, and this as-plated density is what CMP simulation uses to correctly capture the pattern density dependent rate of polish. The CMP model uses the electroplated topography information of total thickness (field thickness + array height), step height (SH), and as-plated density (topography density, ρ_T) to calculate removal rates at each grid cell across a whole chip during the bulk copper removal stage.

Figure 6.39 summarizes how the electroplated topography information is fed-forward to the CMP modeling methodology.

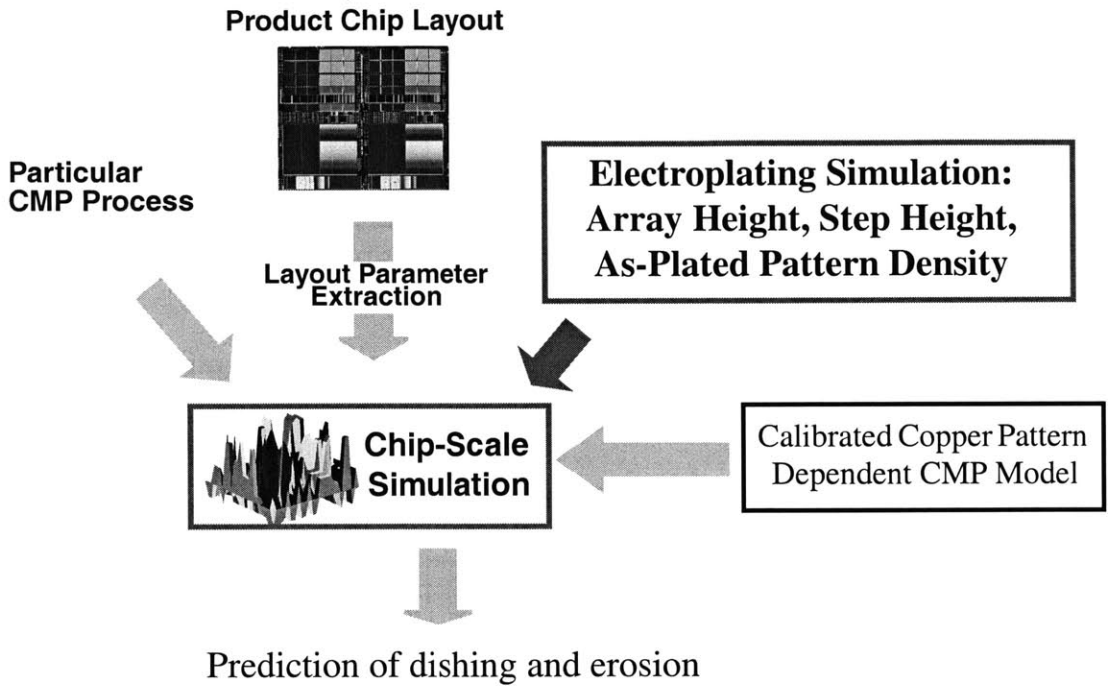


Figure 6.39: Integration of Electroplating Model and CMP Model for Complete Chip-Level Simulation

All information from the electroplating model is based on 40 x 40 μm grid cells, and this is also the simulation discretization for CMP. The total copper thickness from the electroplating simulation result is used to determine the pressure distribution for each grid cell across an entire chip using the contact mechanics portion of the CMP model. Then, for each discrete cell, the removal rate is found using the combination of the pressure on the surface, the electroplated pattern density, and the topography step height using the density-step-height portion of the CMP model. This procedure of finding removal rates and thus the amount removed within each cell is iteratively carried out for each incremen-

tal polish time, where the copper thickness, step height, and topography density after each time increment is updated until the specified polish time is complete. This stage 1 bulk copper polish part of the CMP simulation is critical in determining the clearing time of copper to the underlying barrier, as this impacts to overpolish experienced in each region on the chip during the subsequent simulation of copper dishing and erosion.

We have emphasized the importance of initial plating topography in CMP performance. To conclude our discussion of the integrated plating and CMP models, we present a simulation result showing a comparison between a realistic electroplated surface case and an "ideal" case. The realistic case uses the electroplated result from experiment A as presented in Chapter 5, and the ideal case assumes that the initial profile is flat everywhere without any local step heights. Figure 6.40 shows the simulation results for erosion for the realistic and ideal cases. We see from the erosion profile across the top row of the test mask, that significant differences in erosion result in the various pattern regions. In this case, the difference is about 200-300 Å. As a final observation, this example also illustrates that erosion may continue to be a concern in future CMP processes, even if a "perfect" plating process can be developed.

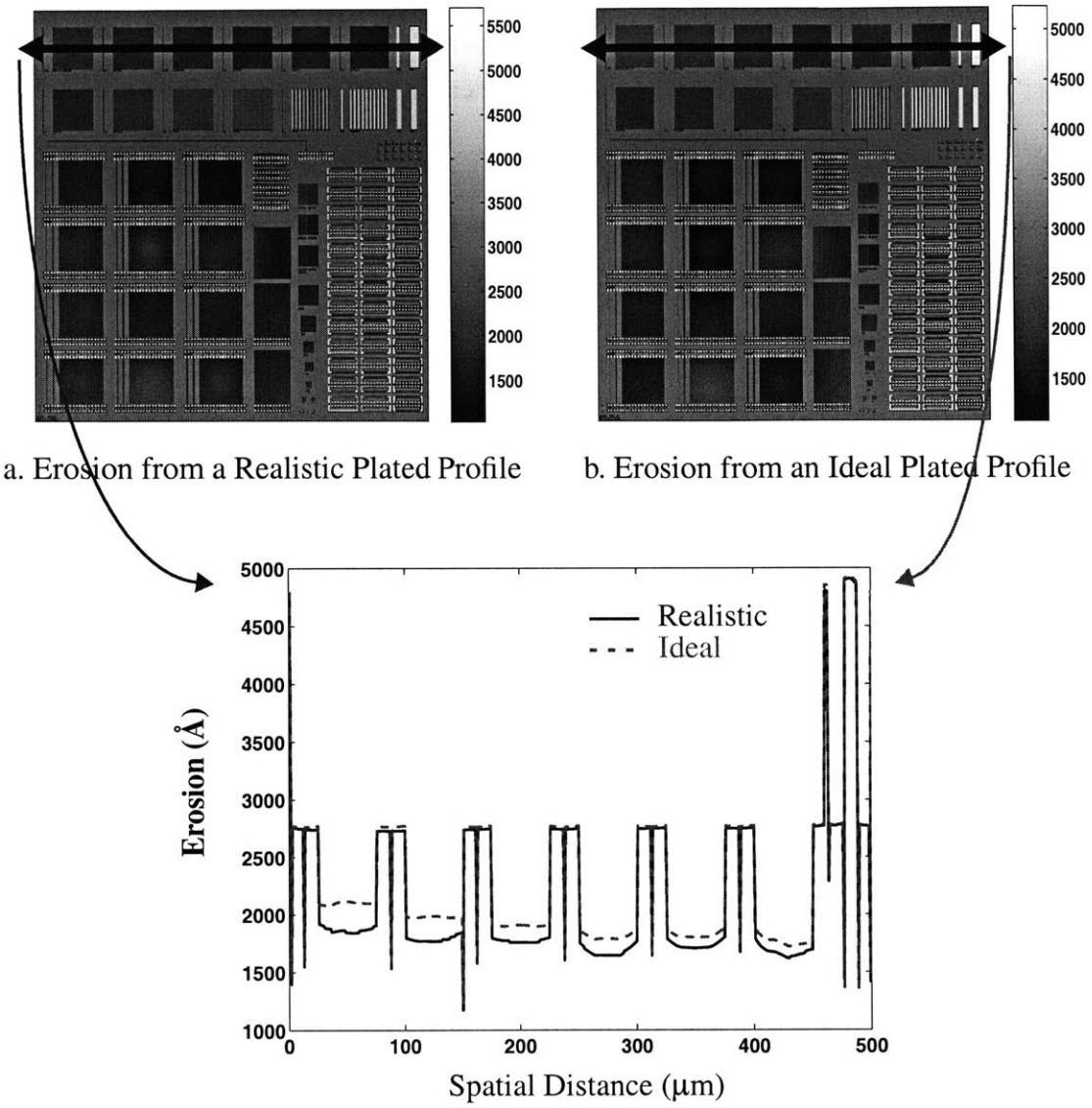


Figure 6.40: Impact of Plating Topography on CMP Erosion

Chapter 7

Conclusion

In this chapter, we summarize the key results of this research and review the key contributions of the thesis. Two areas of future work are then suggested. First, applications of the electroplating and CMP characterization and modeling methodology are suggested. Second, possible extensions to the electroplating model are discussed.

7.1 Summary and Conclusion

The research presented in this thesis has examined pattern induced topography variations in electroplating and CMP process for creating copper interconnects, and developed a comprehensive characterization and modeling methodology for topography and thickness variation in copper electroplating. This methodology consists of test mask development, characterization of data trends, model development, and simulation/prediction for other layouts.

The test masks consist of various combinations of line width and line space, forming various pattern environments. A basic structure consists of an isolated line and a pattern array region, and typical measurements include surface profile scans and copper thickness measurements in open field regions. The test masks serve as the characterization vehicle for determining key non-uniform behavior of a process. Once wafers are processed, various surface topography variations are characterized as a function of underlying layout patterns, and we have found that the electroplated topography exhibits strong pattern dependency on both line width and line space. Thus, these two layout parameters are chosen for the development of a surface regressional model whose structure is motivated by consideration of key physical effects in both conventional and superfill electroplating. In

particular, we use the aspect ratio term or 1/width term in our model to better capture the superfill or bulging effect compared to the original polynomial model form.

Then, in order to perform a chip-scale simulation with the calibrated model, layout parameter extraction for random features is described. A layout is divided into 40x40μm grid cells and all layout extraction is done for each grid. The core of the procedure is the extraction based on line width distributions rather than average line width so that better accuracy can be achieved in the model prediction. Furthermore, the distribution idea helps us to work with manageable layout information; it would not be practically feasible to use or retain the feature-level detailed geometry information for a layout. The layout parameter extraction procedure is closely tied to the chip-scale simulation where we use the distribution information to perform area-based averaging of simulations for each bin.

The calibration error of the step height and array height is less than 500 Å, and the model prediction captures the topography trends including field thickness variation with RMS errors of roughly 1000 Å for the electroplating process with about 15000 Å of copper thickness in field region. A part of the prediction error comes from using the distribution of lines rather than actual line geometries, but the overall error is within a reasonable bound.

The chip-scale simulation and prediction capability can be used to help determine whether a new product chip can meet the specification even before a single wafer is polished. Instead of performing actual electroplating work on each and every new product wafer which is costly and often hard to characterize due to their inherent nature of random features, the test mask can be relatively easily made and the characterization performed a single time to capture and model the process interactions with layout patterns.

In addition to the characterization and modeling methodology for electroplated surface profiles, a similar method is developed to characterize pattern dependent problems of cop-

per dishing and oxide erosion in CMP processes. This thesis contributes the development of the test masks and characterization procedures for both single-level and multi-level CMP pattern effects, and we advocate the systematic study and characterization of these pattern dependencies through the use of electrical and physical test structures and measurements.

In addition to a single-level mask, a dedicated multi-level test mask is designed that incorporates various overlap cases between metal 1 and metal 2 structures. We show CMP polished surface profiles and electrically determined metal thicknesses that describe how non-uniformity on M1 (i.e. erosion and dishing) affects M2 polishing behavior. The amount of erosion on M1 as well as what type of overlap is created on M2 both affect M2 polish. We find that the M2 polish creates additional array recess, but the amount of additional recess is smaller when the M2 array resides in a previous M1 array recess region. In addition, the resulting M2 line thickness depends not only on the M2 pattern and polished surface profile, but also on the M1 recess. Thus, determination of final M2 line thickness cannot be inferred from the M2 polish surface profile alone; knowledge of the M1 profile or direct electrical or physical measurement of M2 line thickness as enabled by the developed test masks is necessary. Understanding and characterization of these single-level and multi-level pattern effects are critical for successful and efficient process development as well as optimization and integration, and supports modeling of these variations in a systematic method.

In summary, this research has made the following contributions:

1. Developed test structures and masks to explore key pattern effects in both electroplating and CMP processes.
2. Characterized pattern dependent problems in electroplating as a function of underlying pattern features and developed a model to capture the variation.

3. Developed layout parameter extraction procedures and applied the electroplating model in chip-scale simulation and prediction for arbitrary layouts.
4. Characterized both single level and multi-level CMP pattern dependent effects as a function of underlying pattern features.
5. Illustrated the integration of electroplating topography prediction and CMP modeling for predictive chip-scale simulation of final interconnect topography.

7.2 Future Work – Applications of the Methodology

In addition to being able to predict the resulting surface topography and thickness variation in electroplating, the overall methodology can be used for various applications. One application is screening for problem areas on a candidate chip layout. Given the range of line widths and spaces for a given layout, the resulting simulations for profile and thickness variation can be used to check possible "thick" or "thin" spots and to verify that all regions satisfy some process specification. The opposite flow is also possible where intelligent design rules can be developed to impose a limit on the range of line width and line space for a given layer or a part of a layout so that a required thickness specification can be satisfied for a given process. This can be done by generating a family of curves for step height and array height as a function of line width and space, and examining the prediction results.

Another application is optimization of the copper deposition thickness. For instance, if a lower level metal layer contains all small features where superfill is present, then the electroplating deposition thickness can be optimized to be thinner than nominal target thickness so that higher throughput and better planarization can be achieved in the subsequent CMP process.

Another key model application involves the use of dummy fills. To minimize pattern effects, dummy fills are often used, and the developed model can be used to specify the

size of dummy fills and fill pattern environment (e.g. density or pitch) to balance out pattern effects. If the dummy fill size is too small, then unwanted excess bulge may be introduced, or if the dummy fill size is too big, then large conformal step heights are created. Proper size of the fill, and their distance from each other and to active layout, can be formulated by examining the topography response to these introduced features.

For our studies, we have mainly focused on the line/array test pattern for electroplating and CMP pattern effects. The study of additional test patterns described in Appendix A may be helpful in design of dummy fill or slotting strategies to reduce copper thickness loss. In addition, the capacitance structures described in Appendix B may be useful for obtaining valuable information for electrical characterization of interconnect capacitances, especially for materials with low dielectric constant.

7.3 Future Work - Model Extensions

Due to the limitations of the layout extraction tool, only line width information is extracted and used in our chip-scale simulation procedure, with the line space derived from pattern density. It is suggested that line space information also be extracted for each grid cell for better representation of the layout. The proposed method for getting line space information is as follows. Effective line space is computed for each line width bin, where for each line in a bin, its average space to its nearest neighbors is obtained and this is again averaged for all lines within the same bin to obtain the effective line space for that bin. Thus, one number for the effective space is reported for each line width bin. Since there could be hundreds of possible combinations of line width and space, this method efficiently captures spacing information for a given distribution of lines. One underlying assumption is that lines in a given line width bin have similar line spaces, where this is typical of actual circuit layout practices.

The electroplating characterization and modeling of topography variation presented in this thesis is based on measurements of a single center die. We have shown wafer to wafer variability in Section 5.6, but did not explicitly deal with non-uniformity across the wafer. One possible approach to deal with wafer-level non-uniformity is to produce model fits for several die across the wafer, and use these to produce "worst case corner" models for the pattern dependent plating. Other possible approach is to develop a wafer-scale model to account for such a long-range variation.

The developed methodology is limited to a given process, and when a new process is formulated, it must be characterized first to obtain the necessary model coefficients for simulations on other layouts for the new process. A future extension of our methodology is to integrate it with a physical electroplating model. A physical model can produce simulations of surface topography variation for a set of lines and spaces, and give a sample data set for a new process. Then, this data set can be used to calibrate our model to perform chip-scale simulations as we have done here with an actual data set. Another direction for future research is to extend or integrate the model to account for wafer-scale variation and for macroscopic variation such as the copper field thickness variation we have seen. The integration of the chip-scale model with both feature-scale and macro/wafer-scale models, including process parameter as well as layout pattern dependencies, would be the ultimate challenge in the modeling of thickness variations present in electroplating.

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Appendix A

Single-Level Test Mask Description: Version 1.2

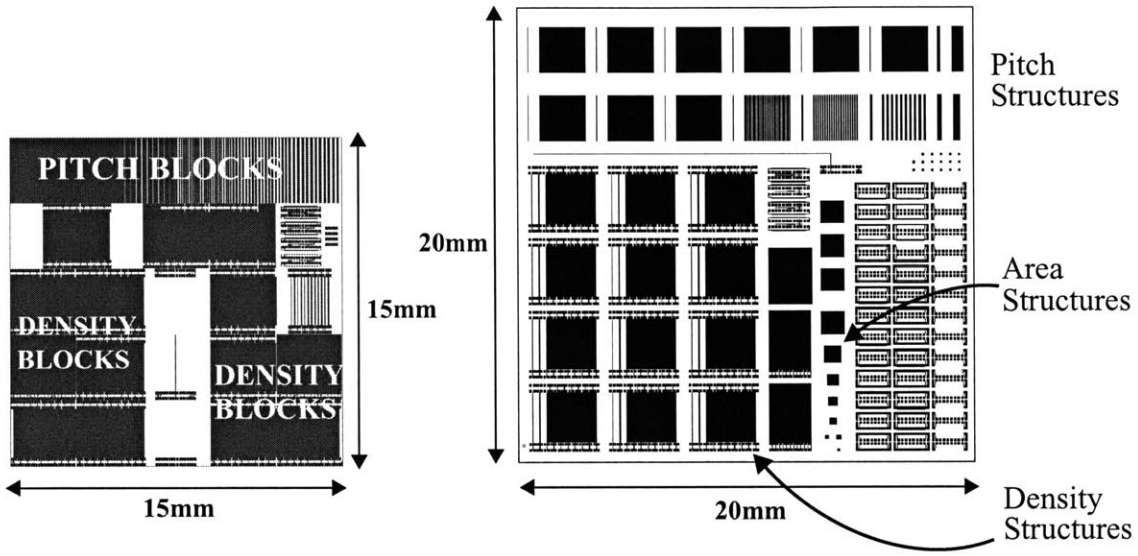
In this appendix, we present additional information of the single level test mask v1.2 whose main test pattern structures are described in Chapter 3. Here we first give a brief historical background of the mask design; some of the design issues are highlighted while comparing this test mask to a previous one. Then, additional test structures are described in detail, which are often useful for specific purposes of examining pattern effects or electrical yield.

A.1 Historical Background in Mask Designs

It is worthwhile to review the historical background in copper CMP test mask evolution by considering two generations of single-layer copper CMP test masks as shown in Figure A.1 At the left of the figure is an original design of a test chip (version 1.0) having 15 mm x 15 mm die size that is based on collaboration with SEMATECH, and is also known as the "SEMATECH 931 mask". The test mask shows physical pitch blocks of size 2.5 mm x 3.0 mm at the top, a variety of 3 mm x 3 mm electrically probed density blocks, a number of serpentine and combs to characterize clearing and yield (at 0.35 μm line width and line space), and an assortment of additional structures including control lines, oxide filled pads, and van der Pauw structures.

By comparison with a more recent generation mask design at right that is described in Chapter 3, a number of lessons learned should be noted. First, the revised chip is larger (20 mm x 20 mm) enabling simplified floor planning and isolation between structures: separations of 500 to 1000 μm between structures (rather than abutting structures as in the earlier mask) ensure that a "field oxide" reference can be identified for leveling profilome-

try scans, and shorter scans can be used. Second, the test structures (both physical and electrical) incorporate isolated and dummy regions in close proximity to the corresponding array region, ensuring better correspondence between the observed dishing and erosion. These improvements have proved to be valuable for an effective use of measurement and analysis.



a. First Generation Mask ("SEMATECH 931 Mask")

b. Later Generation Mask (Copper Test Mask V1.2)

Figure A.1: Evolution of Single-Layer Copper Masks

A.2 Additional Structures

In addition to the line/array structures used to form pitch and density structures, there are other structures that are often useful in examining pattern dependent issues as well as other yield related problems in copper interconnect. For testing of leakage current and line shorting problems after a CMP process, a yield structure is designed with comb and serpentine lines as shown in Figure A.2. 0.35 μm lines and spaces are used for the comb and serpentine combined region, and 0.35 μm lines with 0.7 μm and 0.9 μm spaces are used

for the region with only comb patterns. The main measurement for this structure is an electrical current leakage test.

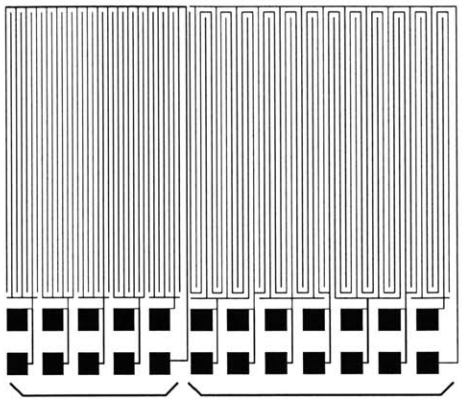


Figure A.2: Comb and Serpentine Yield Structure

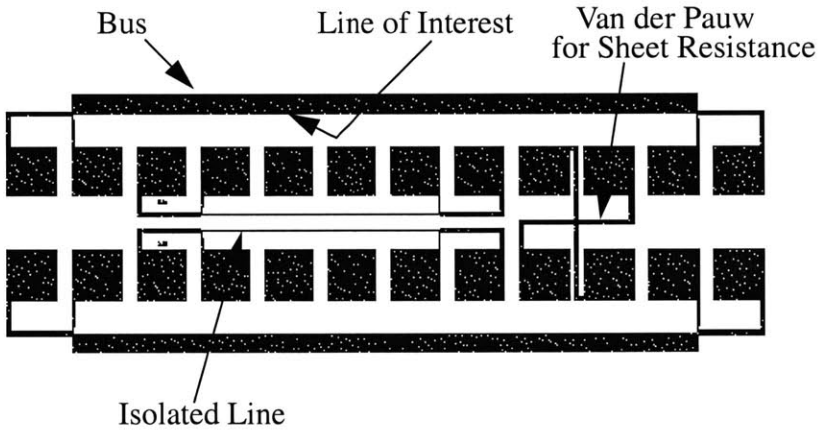


Figure A.3: IsoLine Structure: Isolated Line with Bus and with & without Dummy Lines

The Figure A.3 shows a sample structure to examine the effect of CMP on a line beside a wide bus and beside dummy lines by considering three design factors: bus width (20 μm and 40 μm with linewidth and linespace of 0.5 μm), width of line in examination (0.5 μm and 5 μm), and the space between the line and the bus (0.5 μm and 5 μm). In the

middle of the pads along with a Van der Pauw structure are isolated lines to serve as a reference data. The Van der Pauw structure is included for sheet resistance measurement after CMP process is complete.

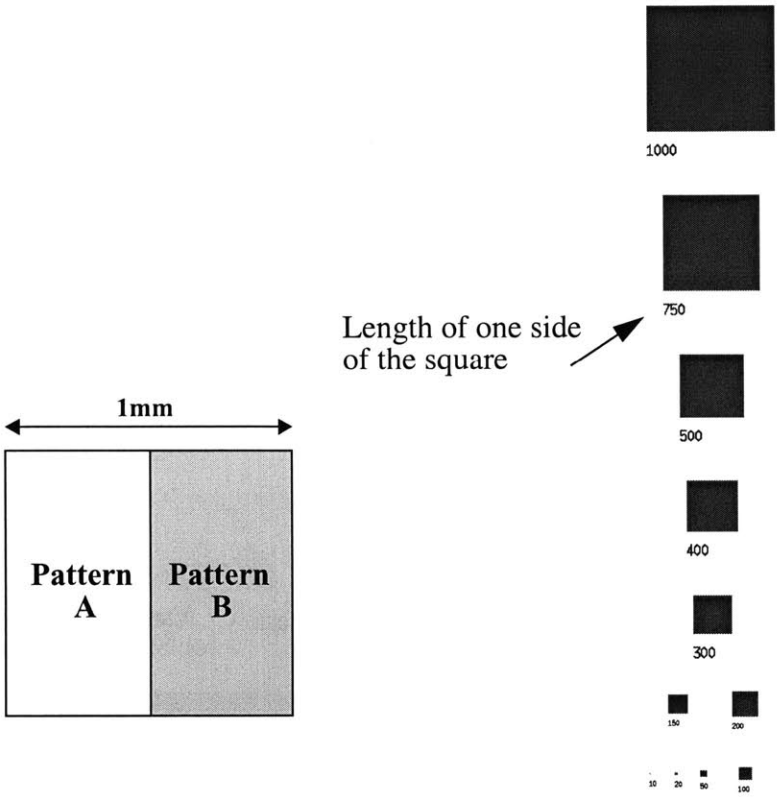


Figure A.4: a: Structure to Structure, b: Area

For a study of interaction in neighboring pattern regions, a test structure is designed with each block of 1 mm x 1 mm in size with two different 0.5 mm x 1 mm regions of different density and/or pitch as shown in Figure A.4a. For a study of process behavior on the size of an array region, a set of structures is designed in a square shape ranging from 10 μm x 10 μm to 1000 μm x 1000 μm with vertical lines of 0.35 μm line width and 0.35 μm line space as pictured in Figure A.4b. There is a label in the layout to indicate the

size of each structure. This is structure is used to examine electroplated array height or CMP erosion as a function of structure size, and surface profile measurement can be used to gather the data by scanning across the middle of each block with long enough field area for leveling of the data. Shown in Figure A.5 is a slotting structure designed for a typical bond pad and interconnect lines where oxide pillars are inserted into the copper for the purpose of minimizing severe copper dishing often present with large features.

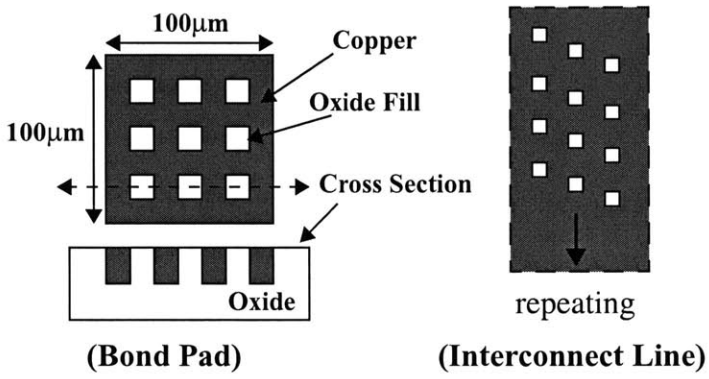


Figure A.5: Slotting Test Structures

Appendix B

Multi-Level Test Mask Description

Multilevel CMP effects can be troublesome: topography can accumulate across multiple levels in successive copper patterning and CMP steps. Here we describe extensions to the test structures and mask designs which have been developed to enable study of these effects.

A multilevel test structure is created by using a line/array structure on metal 1 to induce pattern dependent topography in the first level, and then overlaying another line/array structure in metal 2 on top of (nested within) this topography. The dishing and erosion in the metal 2 line/array structure as a function of the underlying topography can then be studied. Shown in Figure B.1a is a basic structure which consists of an isolated line (the segments of this line forms a loop with a wide oxide spacing in this case between the lines for better isolation) and an array region; the dummy line regions are not used in this layout. Electrical bond pads and an optional via mask level enable probing of both the metal 1 and metal 2 structures after fabrication by using stacked pads to reach metal 1.

One of the key concerns in multilevel polishing is the ability to fully clear upper level structures residing within recesses created by lower level metal polishing. To study this issue, as well as to map out the transition in polish behavior from one underlying topography to another, a number of "overlap" test structure cases are designed. As shown in Figure B.1b, the "half overlap" offsets the metal 2 structure laterally, and Figure B.1c shows a "direct overlap" where the metal 2 structure sits fully within the metal 1 topography. The more complicated "dual overlap" structure in Figure B.1d enables study of the transition from one pattern to another (rather than from one pattern region to field oxide) in metal 1 and the impact of that transition on metal 2 polish.

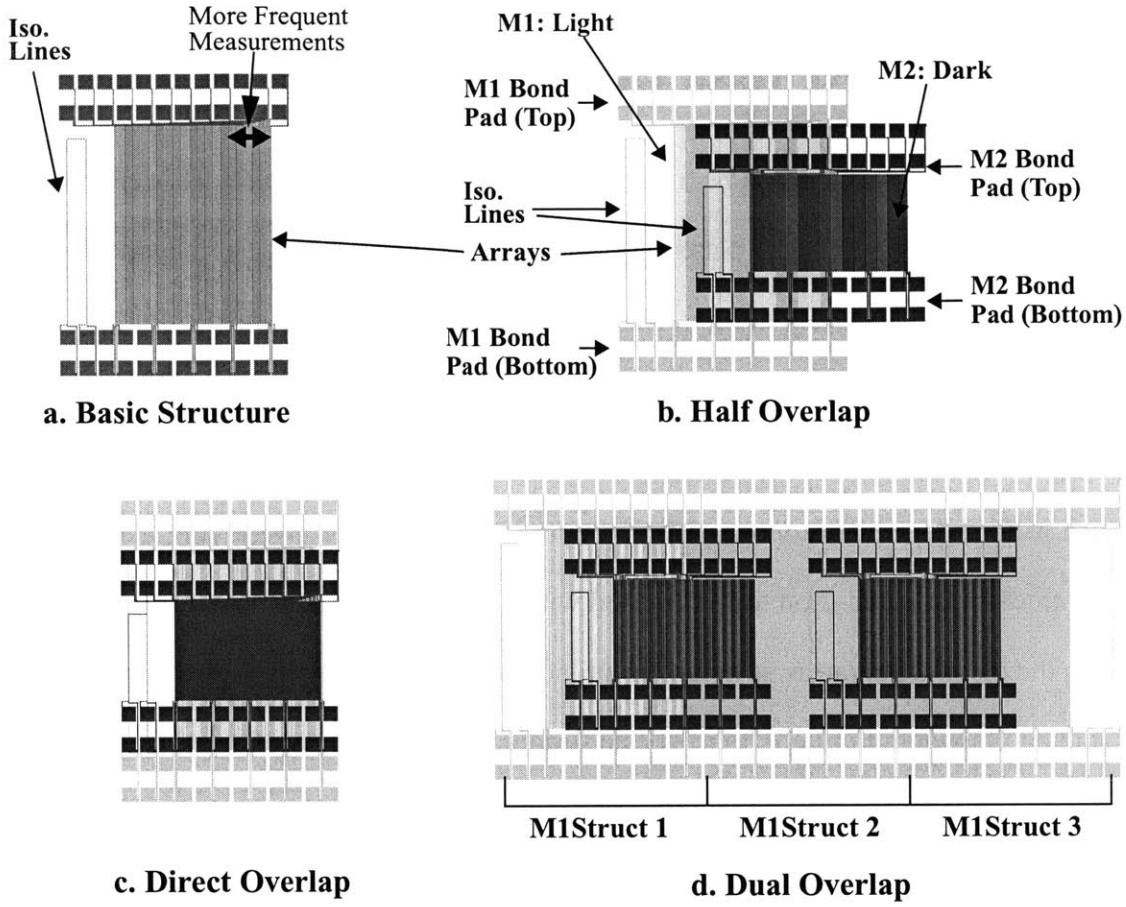


Figure B.1: Multi-Level Mask and Test Structure Layout

Additional minor improvements are made to the metal 1 structures (of size 1250 x 1610 μm) compared to the earlier single level masks. Specifically, a nonuniform spatial sampling of resistances along the line array is used. In each array, the bottom set of pads is used for the measurement of the isolated line as well as to sample from the array of lines at equal distances from the left edge of the array to the right edge. The top set of pads, however, is used to measure lines at finer increments in the transition region near the field oxide. This frequent sampling allows measurement of the pattern topography using electrical data as an alternative to physical surface profile scan data. In a similar fashion, the

metal 2 structures (of size 1250 x 800 μm) are spatially sampled to provide more refined information near transitions of interest (depending on the type of overlap).

B.1 Overall Description for Multi-Level Mask V2.1

This test mask is an evolution of earlier copper CMP test masks. These include the previously described single layer test mask, and a version 2.0 multi-level test mask set (metal 1, via, and metal 2). Version 2.0 has a 20 mm x 20 mm die size and is also known as the "SEMATECH 954 mask". The latest version 2.1 multi-level test mask set is also referred to the "SEMATECH 854 mask". Valuable understanding of copper CMP polishing dependencies and behaviors from these earlier masks made it possible for improved and enhanced structure designs and to focus on key pattern dependencies in copper CMP. Most of the structures are again designed with electrical testing for fast data gathering, electrical characterization and extraction. In this case, both resistance and capacitance measurement is enabled for characterization of interconnect topography as well as evaluation of interconnect electrical performance.

This test mask design is concerned with the following aspects of copper CMP with either conventional oxide (e.g. SiO_2) or low k dielectrics:

1. Intra-level metal 1 polishing pattern effects due to various pattern factors created by different line width and line space combinations (e.g. density and pitch) and combination of structures (e.g. step density and step pitch).
2. Inter-layer multi-level effects of polishing pattern effects with non-uniform topography on a layer below: effects on metal 2 polishing due to metal 1 surface topography generated by metal 1 polishing.
3. Intra-layer and inter-layer capacitance and resistance variations due to polishing non-uniformities such as dishing and erosion, and combined RC variation for circuit impact study.
4. Yield issues with via chains, serpentine lines, and comb structures that include continuity and leakage test.
5. Slotting (oxide island filling in a copper line) structures for optimization of design rule to reduce copper dishing for wide lines.

This copper CMP test mask set consists of three layers and thus three masks: metal 1 mask (hereafter referred to as M1), via mask, and metal 2 (hereafter referred to as M2) mask, and enables study of multi-layer issues in copper CMP. However, the M1 mask itself is purposely designed such that it can be efficiently used for characterization of single layer polishing behaviors. This M1 single mask contains all of the relevant structures and also probing electrical bond pads on the same M1 layer. The M2 mask is also designed with electrical probing capability for both M1 and M2 structures, as well as combined M1 and M2 structures (e.g. inter-layer capacitance structures and via chains). Vias are used to connect M1 bond pads to M2 bond pads (stacked pads).

As with the description of the single-level mask in the previous section, pitch is defined as the line width plus line space, and density is defined as the ratio of copper line width to pitch. Density always refers to copper pattern density, not oxide pattern density, unless otherwise specified. Also, whenever possible, shorthand notations are used where 'Lw' indicates line width or the trench width and 'Ls' indicates line space. We have previously used density and pitch structures as the main pattern factors in the design of the test masks. Density structures are designed so that the pattern environment changes in copper density with fixed pitch value; pitch structures are designed with fixed density of 50% (same line width and space) for varying pitch values. However, in this test mask design we have introduced additional pattern factors where we keep line width fixed and vary line space, and vice versa. This is done to examine line width or line space dependencies without being confounded by each other as was the case for the density and pitch structures.

The minimum feature size of this mask is 0.18 μm line width and 0.18 μm line space which is the current technology node for IC's, and the maximum geometries are 100 μm lines and 100 μm spaces which are large enough to cover the wide spectrum of feature

sizes. Figure B.2 shows the floorplan of the test mask, and Figure B.3 shows the corresponding layout for both metal 1 and metal 2 layers.

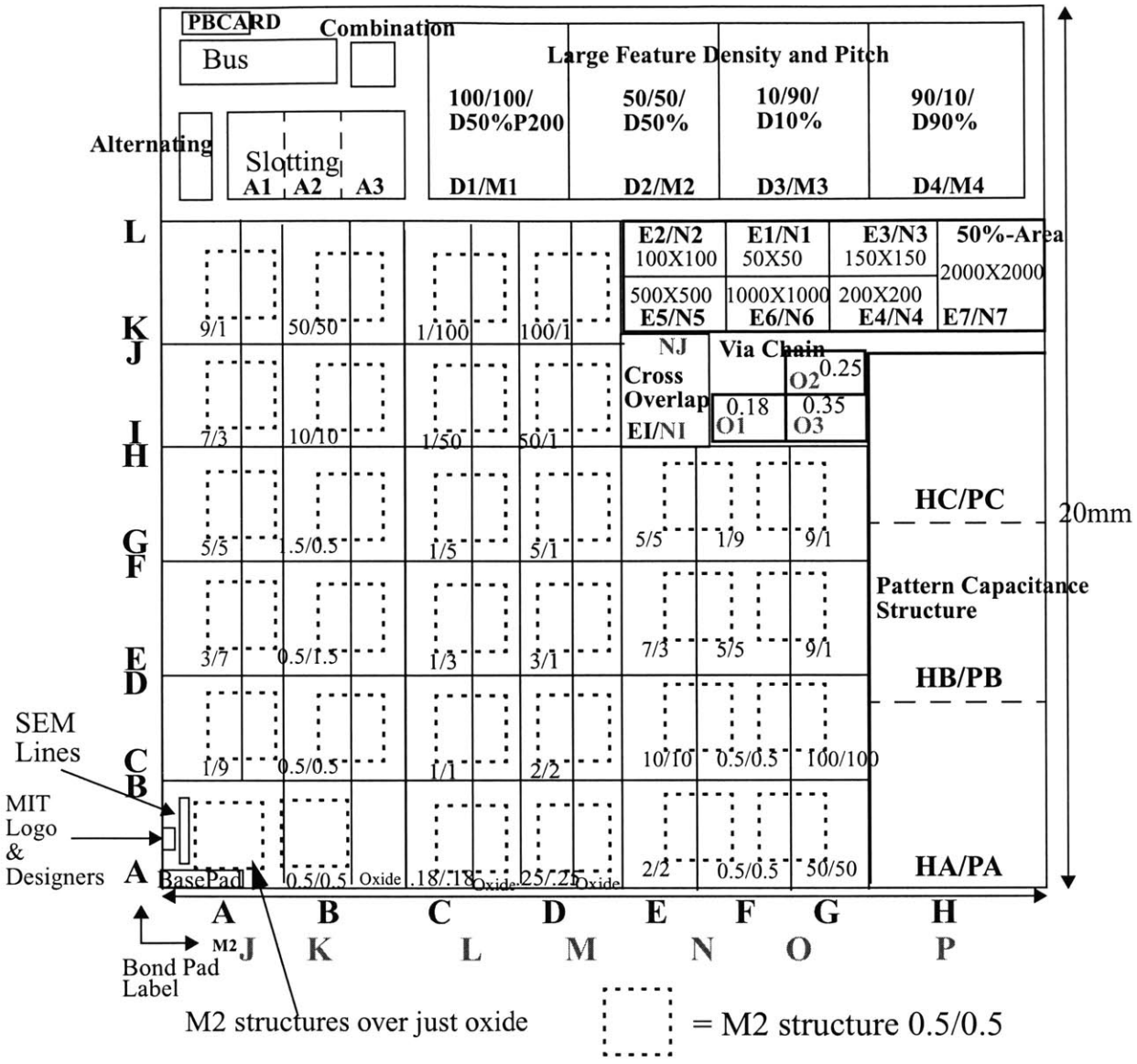


Figure B.2: Multi-Level Test Mask Floorplan

For the key pattern structures in the floorplan, which are various overlap patterns that will be described in detail in the following sections, the line widths and line spaces are marked with the designed M2 overlap structure. For other remaining structures, only

structure names or module names are given. A module name is given for each test structure to uniquely designate it using the column alphabet character followed by row alphabet character. Thus, from the module name, the location of a structure can be determined as well.

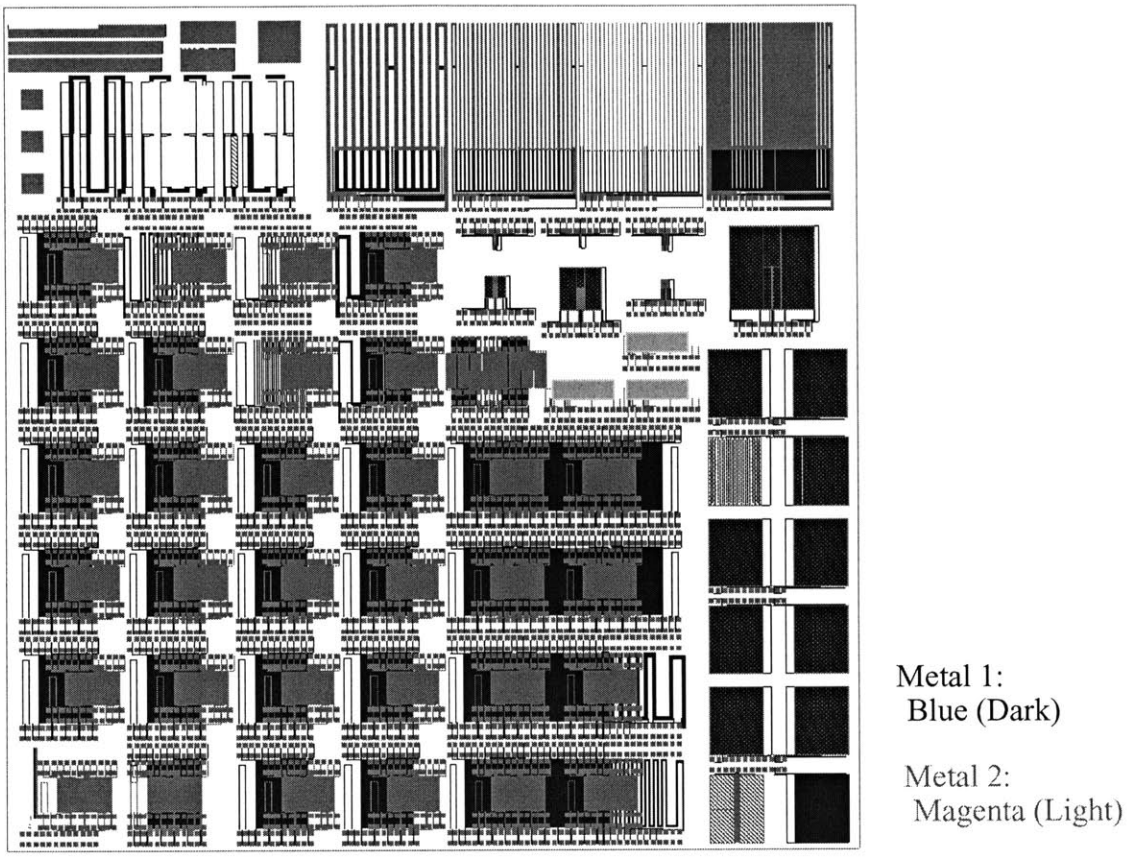


Figure B.3: Multi-Level Test Mask Layout

Near the lower left corner of the mask as shown in Figure B.4 are the mask copyright mark and list of people involved in the design of this mask. Also shown are two pattern recognition masks: one is a solid box within a box and the other one is shaped like a 'cactus'. The pattern recognition mark is used to align the wafer for automatic measurement of

surface profile scans or for automatic thickness measurement recipes. Two letter module label refers to column and row.

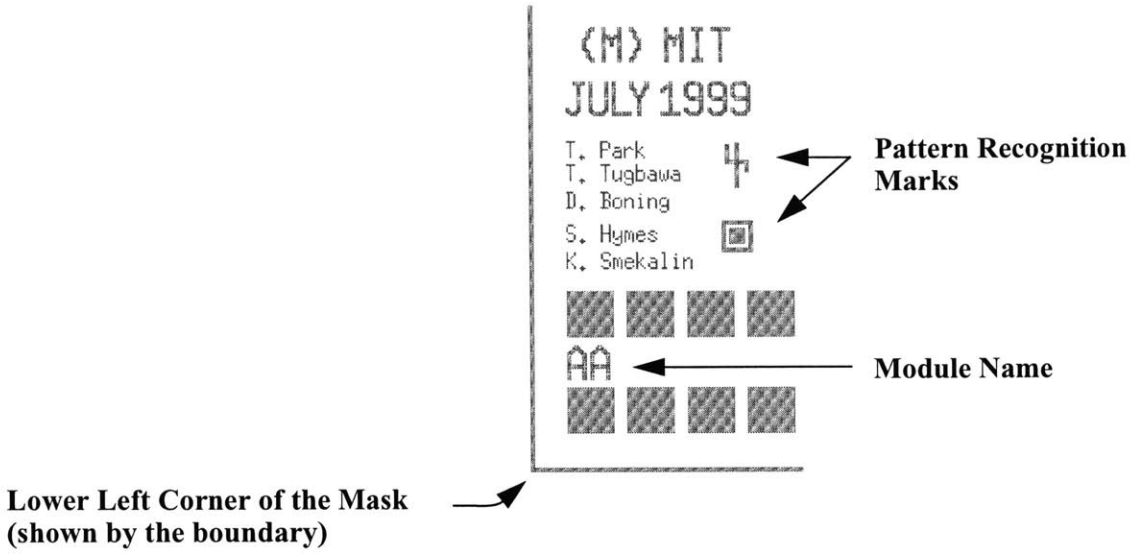


Figure B.4: Mask Copyright Mark and Pattern Recognition Marks

B.2 M1 Pattern Structures and M1-M2 Overlap Structures

This section contains structure descriptions for all of the M1 and M2 structures used to create different overlap cases as mentioned earlier: direct, half, dual, and cross overlaps with no overlap case for a reference. First, the basic design of M1 and M2 structures used to form various overlap case is described. Then, a direct overlap case is described followed by half, dual, and cross overlap structure descriptions.

B.2.1 M1 Structure Design

The basic M1 structure design for creating various overlap cases is shown in Figure B.5 with the circuit representation in Figure B.6. The structure consists of 1250 μm x 1610 μm array region with specified line width and space, and an isolated line (actually two lines) of the same line width used in the array. Both the isolated line and the array of

lines are measured electrically for line resistance using both the top 2x12 bond pads and the bottom 2x12 bond pads.

The bottom bond pads measure the isolated line and the five lines (each line actually consisting of two lines since the line has to go up, bend, and come down to the bottom pads) across the array of lines: the center of the array, the left edge, the right edge, half way between the center and the left edge, and half way between center and the right edge of the array. The top 2x12 bond pads are used for more frequent measurements near the right edge.

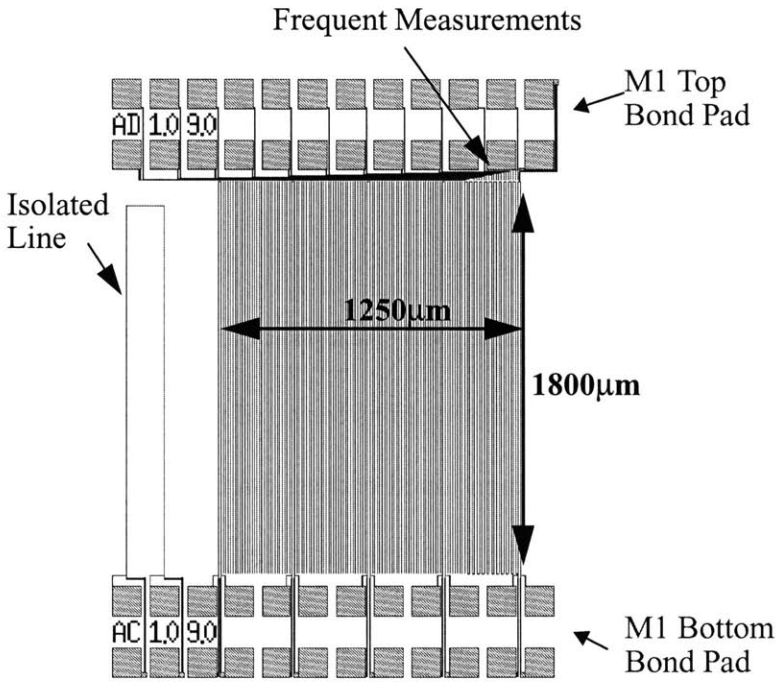


Figure B.5: Metal 1 Baseline Structure

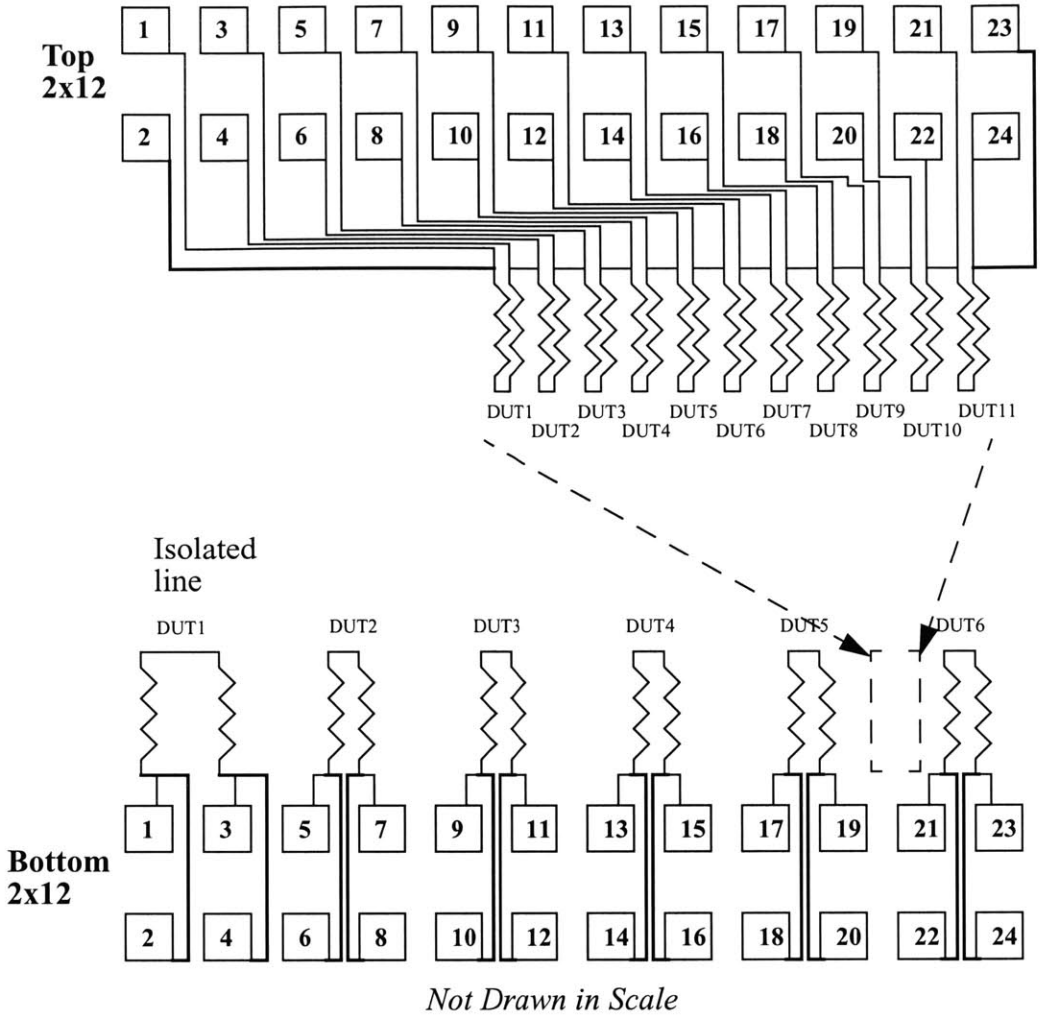


Figure B.6: Metal 1 Baseline Structure: Circuit Representation

B.2.2 M2 Structure Design

The 1250 μm x 800 μm M2 structure array region consists of 0.5 μm line width and 0.5 μm line space as shown in Figure B.7. On the left of the array structure is an isolated line (actually two lines) of 0.5 μm line width. Both the isolated line and the array of lines are measured electrically for line resistance using both the top 2x12 bond pads and bottom 2x12 bond pads. The bottom bond pads measure the isolated line and the four lines (each line again consisting of two lines for electrical continuity) across the array of lines: one at

the center of the array, one at the right edge, one half way between the center and the left edge, and one half way between center and the right edge of the array. The top 2x12 bond pads are used for more frequent measurements near the left edge (starting at the very left edge line thus giving a data point for the left edge of the array) and near the center of the array (both to the left and right of the center of the array measured using the bottom pads). In addition, there are two split comb structures located as shown in the figure. These two split combs are used to test for leakage for possible under-clearing of the overlap region. The circuit representation of the M2 baseline structure is in Figure B.8.

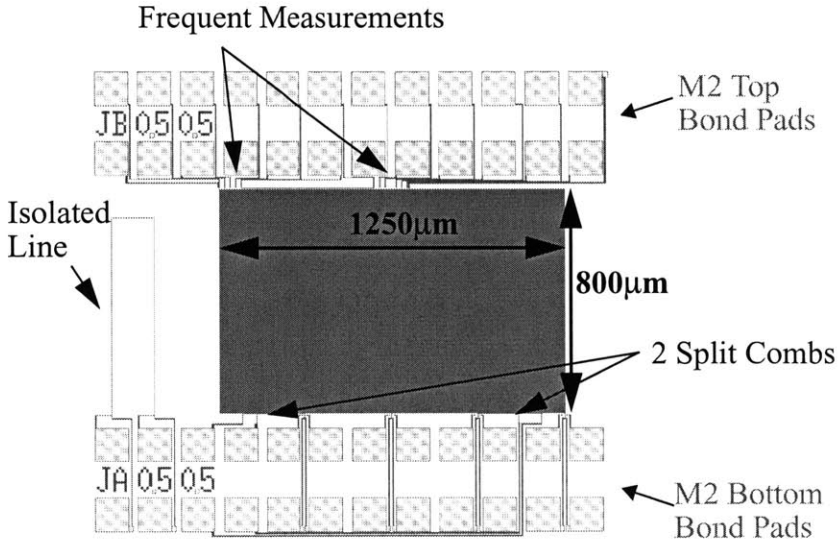


Figure B.7: Metal 2 Baseline Structure

There is one M2 structure over field oxide on M1 that does not form any M1-M2 overlap case. Therefore, this M2 structure serves as a baseline structure for M2 structures having various overlap cases.

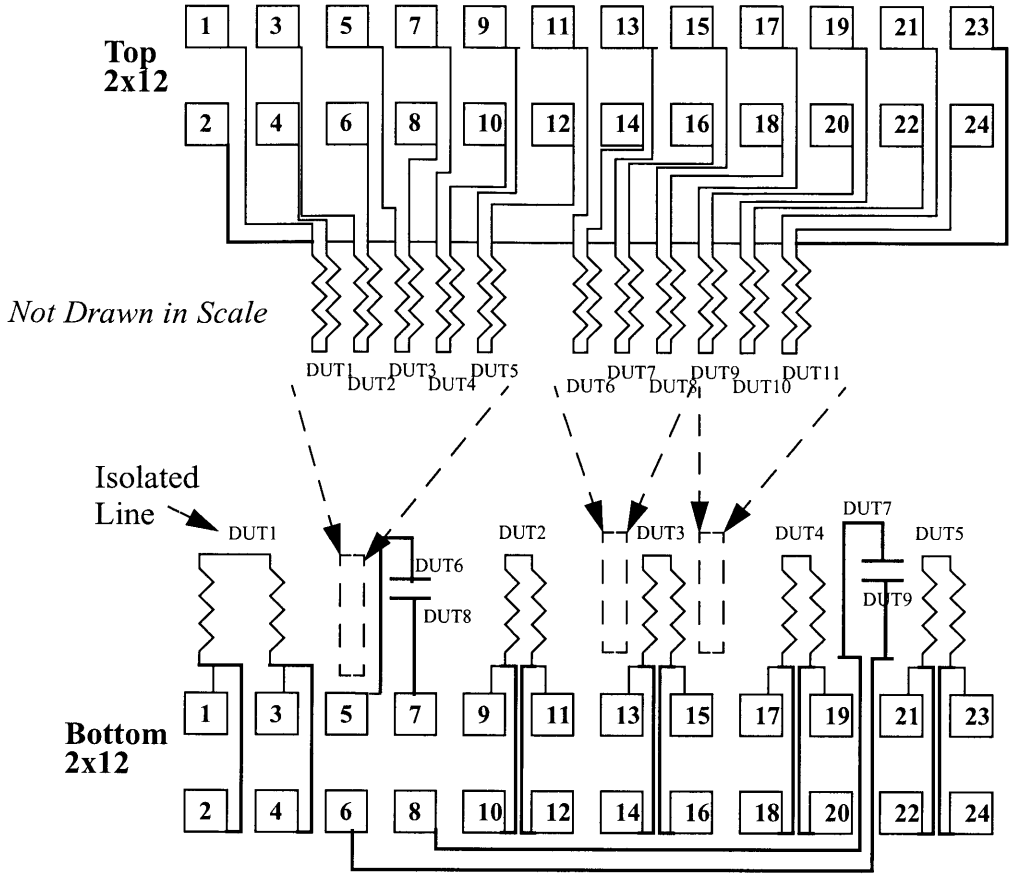


Figure B.8: Metal 2 Baseline Structure: Circuit Representation

B.2.3 Direct Overlap Structure

There is only one direct overlap structure created by the described M1 and M2 structures where they both have line width and space of 0.5 μm. Figure B.9 illustrates the direct overlap structure, which is created by aligning the M2 structure directly over the M1 structure so that the left and the right edges of M2 structure align directly on top of M1 structure. The M1 structure is vertically larger than the M2 structure so that bond pads can be brought up directly to M2 (stacked) from M1 for M1 structure resistance measurements on

metal 2, and also so that the M2 structure can fit within the M2 bonds pads used to measure the underlying M1 structure.

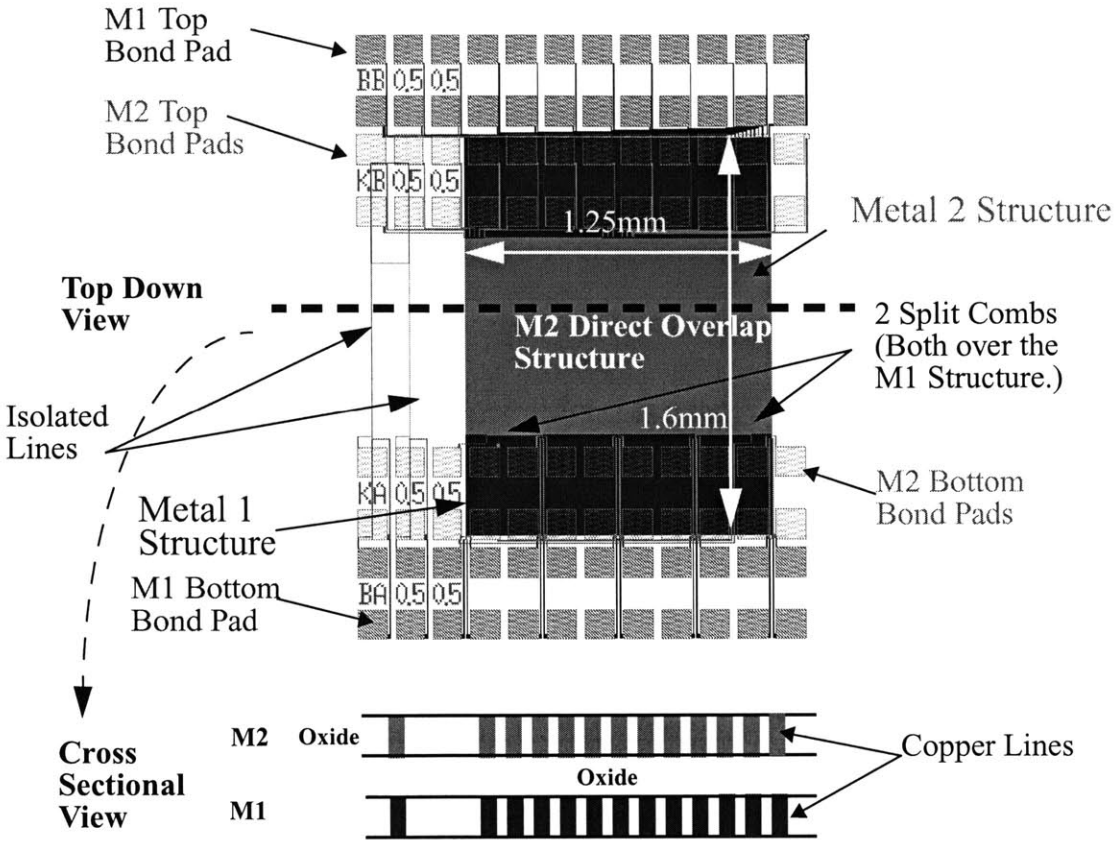


Figure B.9: Direct Overlap Structure

B.2.4 Half Overlap Structure

This section describes half overlap structures on M2 with M1 structures as shown in Figure B.10. The half overlap case is created by aligning the M2 structure half way between M1 structure and oxide so that the center of the M2 is directly over the right edge of the M1 structure. Note that each of the two split combs on metal 2 is now in different metal 1 environment: one is over the half overlap region and the other is over oxide. The

serpentine lines used for resistance measurements are also in two different regions, and the center line is right over the transition between a structure region and oxide. In this way, a good comparison of polish differences can be observed depending on the overlap case and non-overlap (oxide) case.

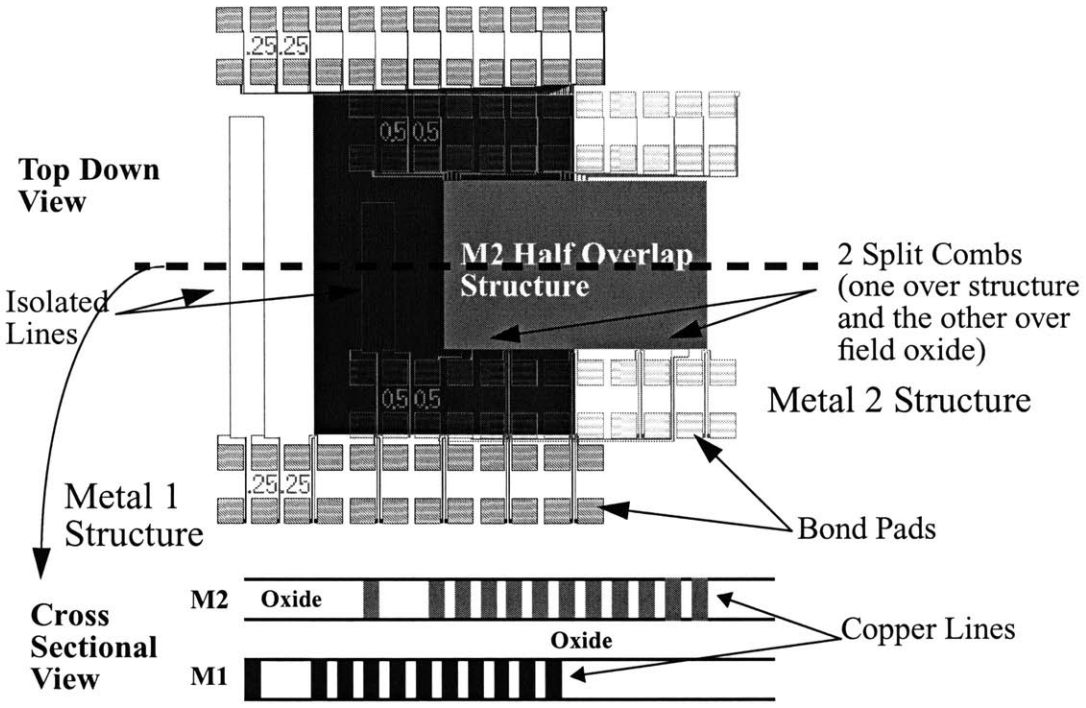


Figure B.10: Half Overlap Structure

B.2.5 Dual Overlap Structure

The dual overlap case is created on M2 with M1 step density structures, consisting of different density structures with constant pitch side by side, and step pitch structures, consisting of different pitch structures with constant density of 50% side by side, as shown in Figure B.11. Each M2 structure is half over one M1 structure and half over the neighboring M1 structure as shown in Figure B.11. The dual overlap structure is similar to the half

overlap structure, but instead of one region being field area, both of the regions that the M2 structure overlaps are patterned regions. In addition to studying the multi-level effects, the M1 structure can be used to study structure to structure interactions, especially the transition region between two neighboring structures.

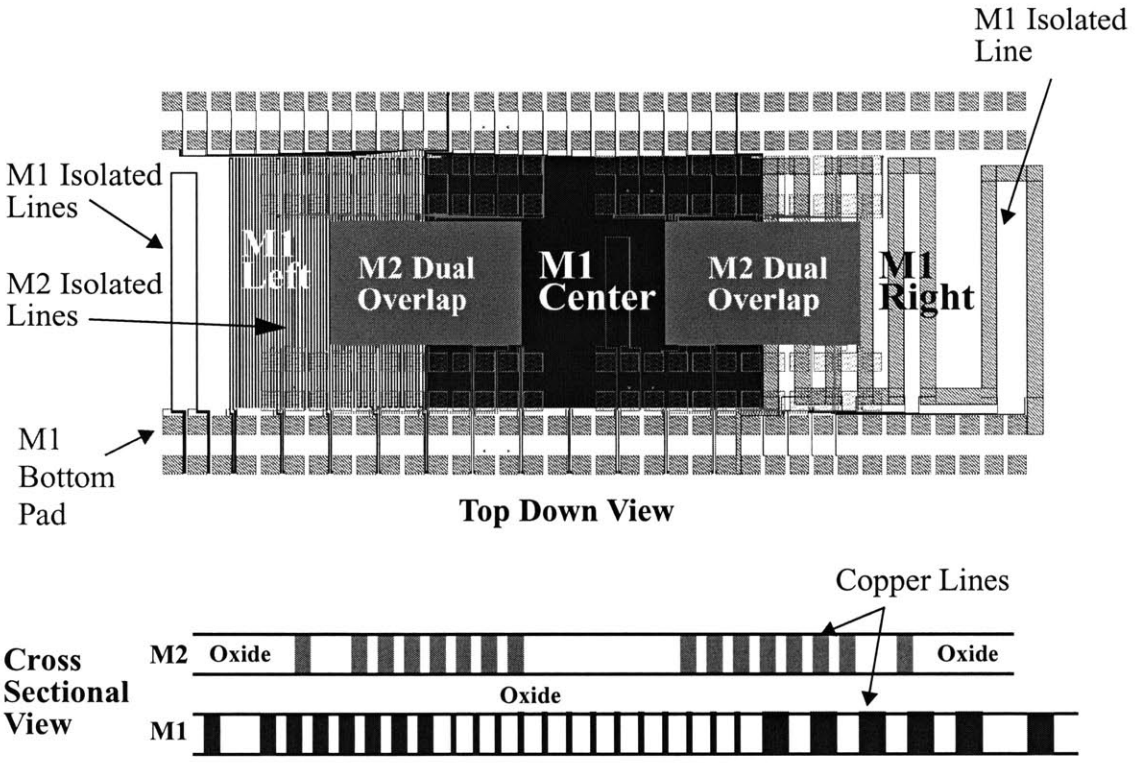


Figure B.11: Dual Overlap Structures

B.2.6 Cross Overlap Structure

There is one cross overlap structure where various sub-structures form various cross overlap cases, and the design is shown in Figure B.12. The idea is to examine how cross-running lines on metal 2 (as opposed to same-directional lines as is the case for all other overlap cases) are polished in terms of surface topography and e-test yield. The metal 1

consists of basically three different sub-structures (each sub-structure is 600 μm x 1600 μm):

- left one third with 1.5 μm line width and 0.5 μm line space to create a large amount of erosion with minimal dishing
- center one third with 10 μm line width and 90 μm line space to create dishing only environment
- the right one third with 5 μm line width and 5 μm line space to create both erosion and dishing environment

There are eight main topography environments that can be created on metal 1, and corresponding metal 2 structures are also shown:

- No Topography (no erosion and no dishing) to Erosion – Region A
- Erosion Only – Region B
- Erosion to Dishing – Region C
- Dishing Only – Region D
- Dishing to Erosion and Dishing – Region E
- Erosion and Dishing – Region F
- Erosion and Dishing to No Topography – Region G
- No Topography (no erosion and no dishing) – Region H

For each sub-structure, the left edge line, the center line, and the right edge lines are measured for resistance. The metal 2 structure is a typical serpentine and comb combined structure where there is a serpentine line in the middle of the two fingered combs, and the size is 240 μm x 800 μm. This metal 2 structure is repeatedly placed over each environment as mentioned above to create different cross overlap cases.

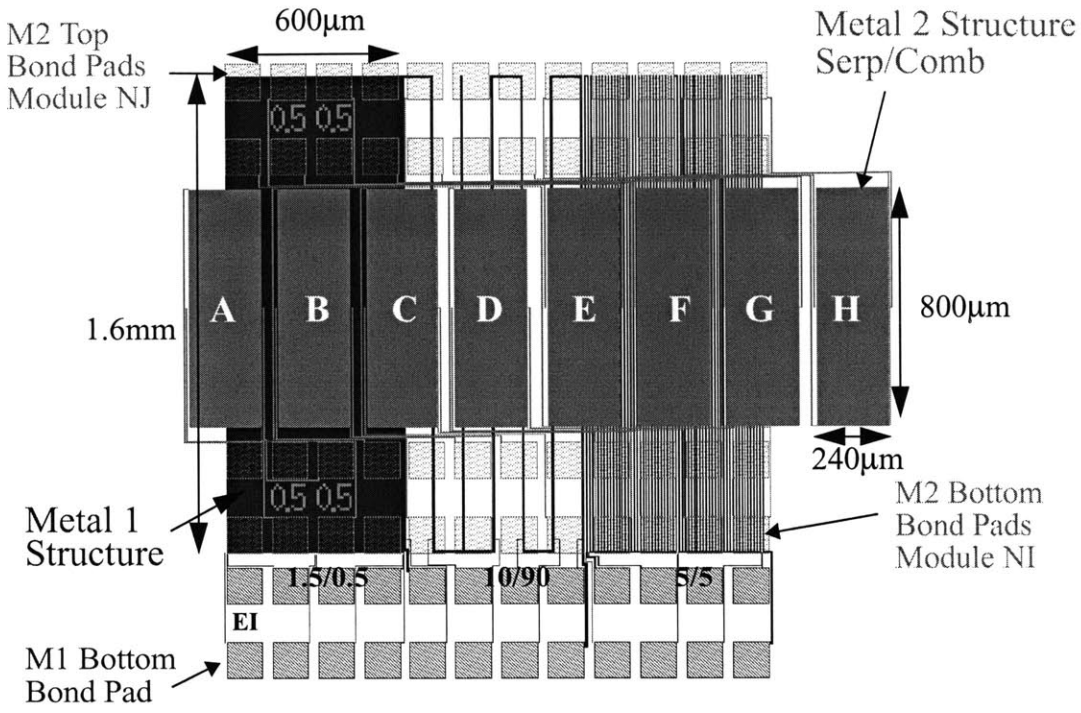
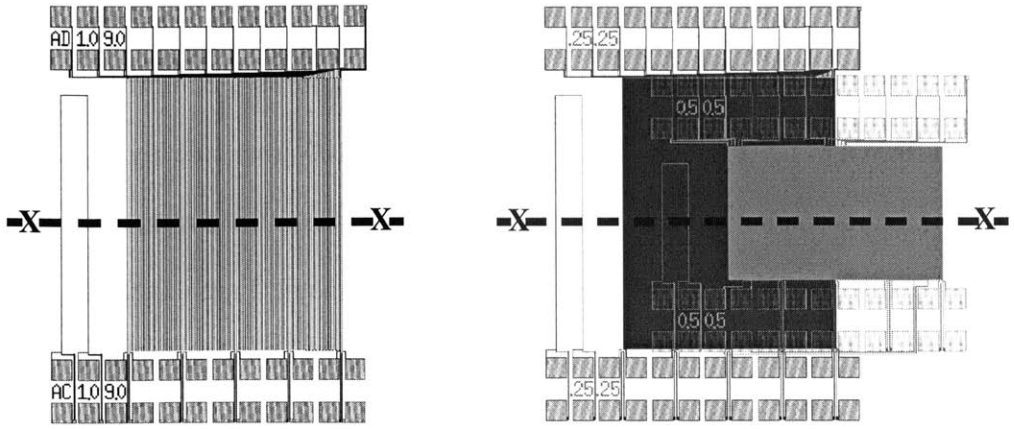


Figure B.12: Cross Overlap Structure

B.2.7 Measurements and Analysis

In addition to the electrical tests that have been outlined with each structure description, surface profile scans are also necessary especially on the metal 2 layer. A surface profile scan is done similarly for all overlap cases as illustrated in Figure B.13. For the measurement of metal 1 polishing behavior, a scan is made in the middle of a test structure that contains the both the isolated line and the array region. It is also advised that enough dielectric field region is contained in the scan for data leveling. Furthermore, dielectric film thickness can be made at each end of the scan to examine field loss as well as to use the data for surface data leveling.



Metal 1 Measurement Overlap Measurement of M1 and M2

Figure B.13: Measurement of M1 and Overlap Structures

For the measurement of metal 2 structures in conjunction with the metal 1 overlaps, similar surface profile scans are made across the metal 2 structure. However, the scan is made that covers both the M1 structure and metal 2 structure so that one can clearly see the propagation of M1 topography on metal 2 layer. Direct overlap, dual overlap, and cross overlap structures are measured the same way for the surface profiles as illustrated for the half overlap case.

B.3 Miscellaneous Structures

There are a number of additional structures designed on this test mask to study process effects on the size of a structure and for different types of measurement capabilities such as intra-level and inter-level capacitances. Each of the following sections gives a brief description of the design.

B.3.1 Large Feature Density and Pitch Structures

M1 structures are created by step pitch and step density structures as shown in Figure B.14. Step pitch structure is a combination of structures with different pitch blocks (at constant 50% density) side by side. The step density structure is a combination of structures with different density blocks (at constant pitch of 100 μm) side by side. The M2 structure is the same replicated M1 structure with a vertical shift of 1mm, thus forming a vertical half overlap. The measured lines on metal 1 and metal 2 are exactly at the same location within each structure and thus they directly overlap with vertical shift.

The analysis for metal 1 layer is to examine density/pitch effects of polishing in copper bulk removal phase, especially focusing on step height reduction and remaining copper thicknesses in different pattern structures. The idea is to examine this initial copper polishing behavior to find out the length scale of polishing (i.e. planarization length or distance). Several measurements across the array of lines are required for each structure (e.g. edge vs. center line resistance). The same analysis used for metal 1 is performed for metal 2 which has added topography effect from metal 1 structures.

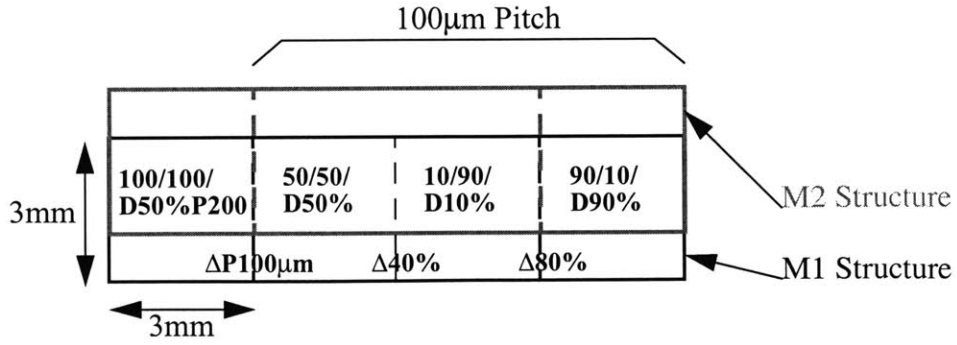


Figure B.14: Large Feature Density and Pitch Structure

B.3.2 Pattern Capacitance Structure

As copper interconnect becomes more fully integrated with low k dielectrics, it will be important to examine capacitances on both the intra-layer and inter-layer levels, and for this purpose a new test structure as shown in Figure B.15 has been designed. The structure consists of fingered comb lines on metal 1 for lateral capacitance measurement, and has a solid metal 2 plate for layer to layer capacitance measurement. Each M1 structure consists of two split combs (two edge combs connected together and the center comb) as shown in Figure B.15. Two edge combs (50 μm wide at each edge) are connected to increase (or double) the resolution of measurements.

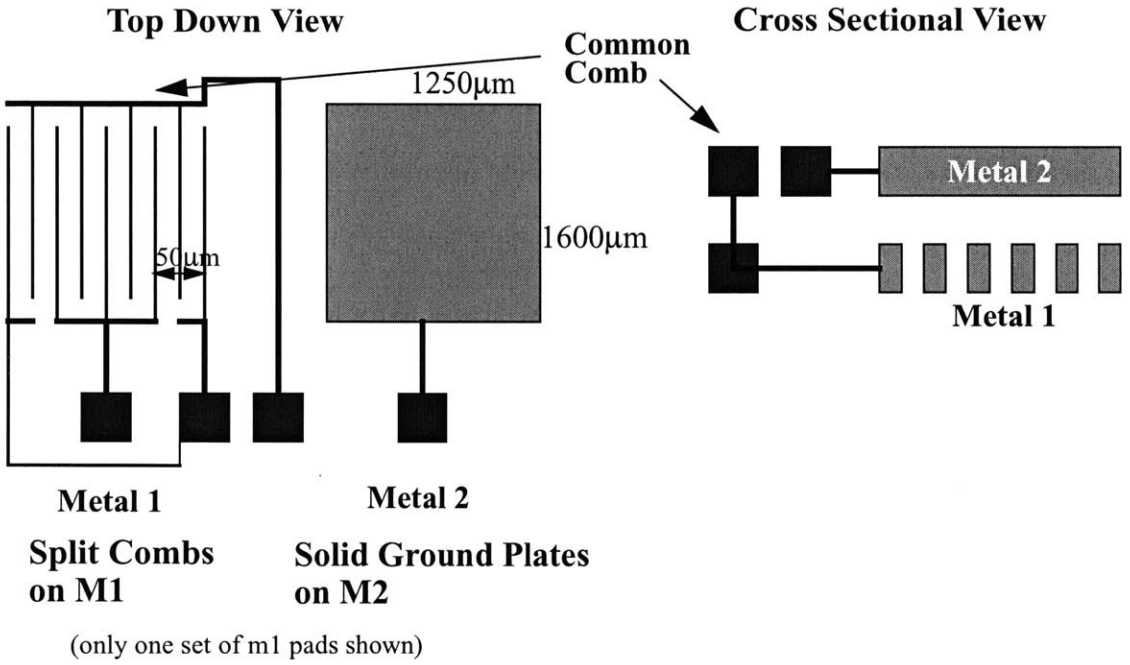


Figure B.15: Pattern-Capacitance Structure

There are two main analyses for this structure. First is the M1-M1 lateral (intra-layer) capacitance measurements for both the edge arrays and the center arrays of lines, and the second is the M1-M2 inter-layer capacitance measurements: a solid metal plate on M2 is used directly on top of the all M1 comb structures. Also included are large Lw and Ls

structures (e.g lines and spaces up to 50 μm) on M1 for inter-layer capacitance study due to dishing on M1.

B.3.3 50% Density-Area Structure

This structure is designed to study process effects based on the size of the patterned structure, instead of the patterns themselves. The structure size varies from 50 x 50 μm to 2000 x 2000 μm with M1 Lw/Ls of 1/1μm (e.g. 50% metal density). This line width and space dimension was chosen to be large enough to be insensitive to possible line width variation. Each M1 structure consists of array of lines with five serpentine lines (two at each edge and one at the middle of structure) and two split combs as shown in Figure B.16. Each two edge serpentines (one at the very edge that consists of two lines connected at the top of the structure, and the other one right next to it) and the center line are measured for resistance, and the rest of the two middle array of lines (separated by the center resistance measurement line and edge lines) are measured for lateral and inter-layer capacitance.

The M2 structure is a solid metal plate with a small line resistance measurement in the center of the solid plate. The line length is horizontally 1/5 of the size of the metal plate, and there are a total of five lines connected in a serpentine fashion for one resistance measurement. The line width is 0.5 μm and separated from the solid plate by 0.5 μm. The serpentine line is designed such that the metal 2 plate remains as a whole plate. This is achieved by using left and right 'slabs' of metal to force current through the center line and having two slabs of measurement leads. The left and right slabs are connected by the line that we are trying to measure and so are the measurements leads. This is to electrically measure dishing of the metal plate.

The analysis used for this structure is to study erosion/dishing vs. structure size during overpolish phase. For the metal 2, the analysis is to study erosion/dishing vs. structure size, pad bending and planarization length/efficiency.

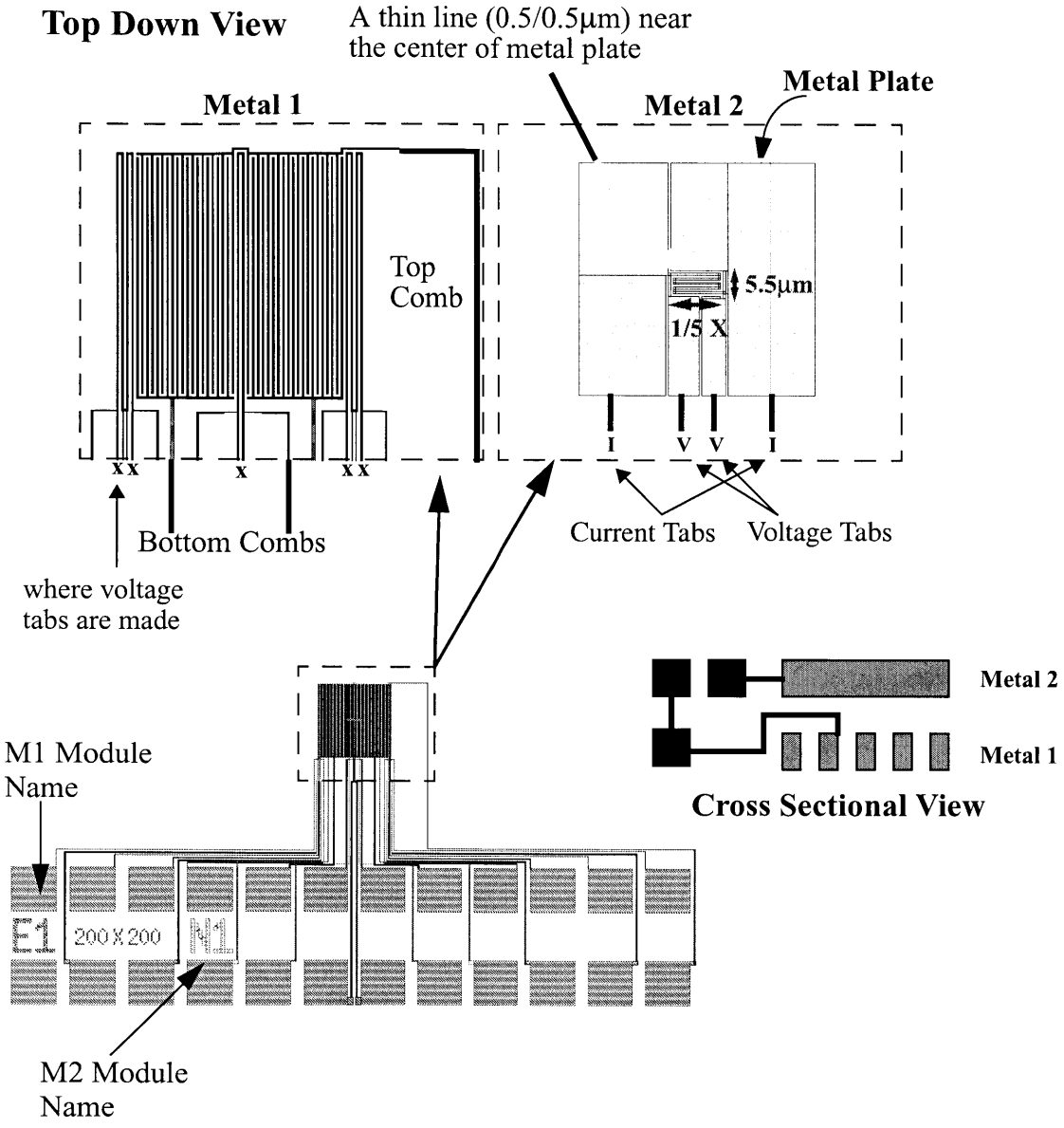


Figure B.16: 50% Density-Area Structure: 200 x 200 μm structure shown

B.3.4 Other Structures

In addition to these structures described, there are additional test patterns and structures designed on this mask set. These are via chains to study pattern effects on via yield, slotting to study how oxide inserts in a line reduce copper thickness loss, and bus-like structures instead of large arrays. The complete description of these structures are found in the mask documentation [44].

B.3.5 Multi-Level Extensions

It is possible to extend this mask set (M1, via, and M2) to higher metal layers for added multi-layer effect study, using the following process sequence. Once M1 and M2 are processed, the via layer between M2 and M3 is omitted, and M3 and M4 layers are then processed in the same way as M1 and M2. Then, all information can be gathered at M2 for M1 and M2, and at M4 for M4 and M3. Thus, we have information for each layer and can identify any pattern dependencies between layers except the inter-layer capacitance between layer 2 and 3. The pictorial representation for this extension is shown in Figure B.17.

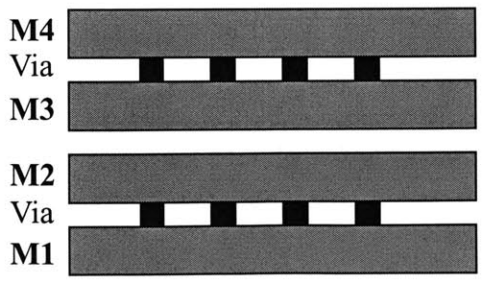


Figure B.17: Multi-Level Extension for Metal 3 and 4