Characterization of Optical Interconnects

by
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B.S., Electrical Engineering
University of Maryland at College Park, 1998

Submitted to the Department of Electrical Engineering
and Computer Science
in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering and Computer Science
at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
May 2000
[June 2000]

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Abstract

Interconnect has become a major issue in deep sub-micron technology. Even with copper and low-k dielectrics, parasitic effects of interconnects will eventually impede advances in integrated electronics. One technique that has the potential to provide a paradigm shift is optics. This project evaluates the feasibility of optical interconnects for distributing data and clock signals. In adopting this scheme, variation is introduced by the detector, the waveguides, and the optoelectronic circuit, which includes device, power supply and temperature variations. We attempt to characterize the effects of the aforementioned sources of variation by designing a baseline optoelectronic circuitry and fabricating a test chip which consists of the circuitry and detectors. Simulations are also performed to supplement the effort. The results are compared with the performance of traditional metal interconnects. The feasibility of optical interconnects is found to be sensitive to the optoelectronic circuitry used. Variation effects from the devices and operating conditions have profound impact on the performance of optical interconnects since they introduce substantial skew and delay in the otherwise ideal system.

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Acknowledgments

I would like to thank Professor Boning and Professor Chandrakasan for their time and effort in guiding and motivating this work. Their encouragement and trust were crucial to the completion of the project.

I would also like to thank Kush for his willingness and selflessness in providing insights and enlightening suggestions whenever I encountered problems along the way. I am grateful to Desmond and Andy for imparting their knowledge of device physics and for assisting in the design and testing of the detector. In addition, I want to thank Paul-Peter for his assistance in building the prototype. Heartfelt appreciation is extended to Jim and Illiana for offering invaluable help during the layout of the chip.

I want to thank Rong-Wei for his constant support, be it emotional or technical, and for his belief in my ability, more so than myself.

Lastly, I would like to thank my family for their love, support, and sacrifices. My father, for offering insights and inspirations; my mother, for the loving care and gentle encouragements; my little brother, for the mysteriously timed phone calls and laughter that we share.

This research was supported in part by the Interconnect Focus Center under MARCO and DDRE funding and by an NSF Graduate Fellowship.

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Chapter 1

Introduction

1.1 Background

As technology continues to scale into deep sub-micron regions, there is a corresponding increase in chip size and device speed. Whereas transistor scaling provides simultaneous improvements in both density and performance, interconnect scaling improves interconnect density but generally at the cost of degraded interconnect delay, as illustrated in Figure 1-1. Results of theoretical modeling indicate that below 1μm minimum feature size, interconnect delay due to parasitic capacitance, including both fringe and inter-wire coupling capacitance, will have a strong impact on circuit performance [2]. As a result, effects of interconnects, which previously have been regarded as trivial, are becoming more prominent. These effects include bus delays, clock skews, coupling signal noise, and power and ground noise. To address these problems, active research has resulted in the following technological trends [14].

- Increasing the aspect ratio
- Increasing the number of metal layers

- Reducing dielectric constant
- Reducing resistivity of metal lines

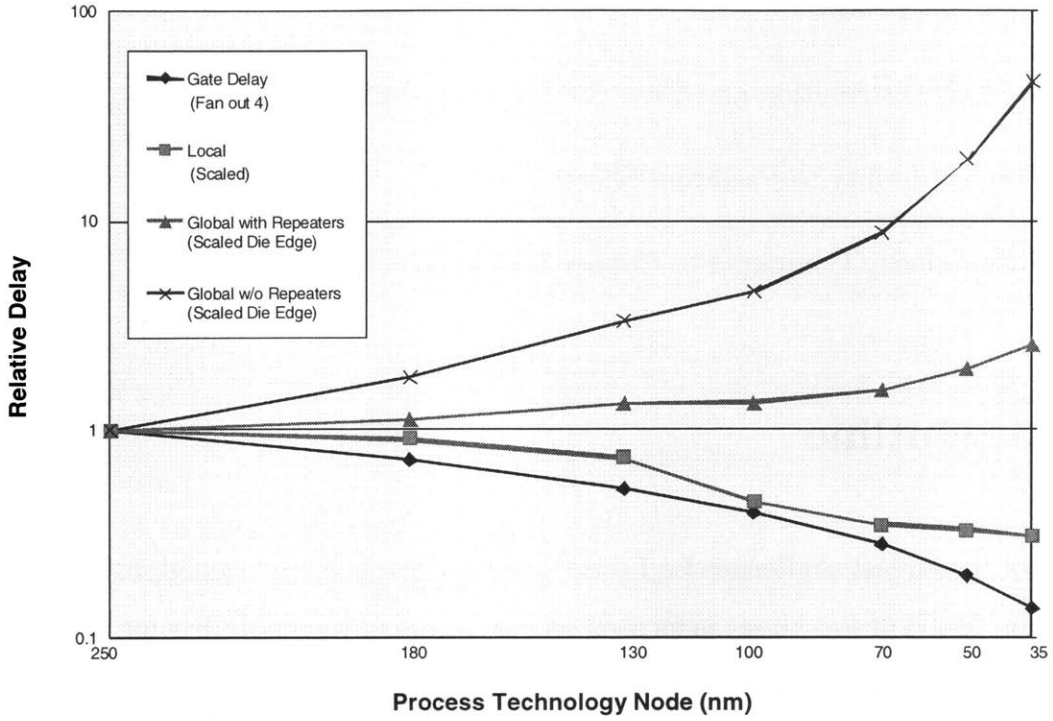

Figure 1-1: Delay for Local and Global Wiring versus Feature Size [26].

Yet, studies have shown that even with copper and low-k dielectrics, these approaches will eventually encounter limits and may impede advances in integrated electronics [18]. New, revolutionary techniques are needed to provide a paradigm shift to continue the progress in integrated electronics. One technique that has the potential to solve many of the underlying physical problems while continuing to scale is optics. However, there are many practical challenges awaiting to be addressed. The technology is still in its infantile stage and the systems that could benefit most from optics are likely to be different from the architectures of today, which are optimized around the strengths and weaknesses of electrical interconnects [18]. Moreover, there are many technical challenges in implementing dense optical interconnects in silicon CMOS chips. These include circuit issues, integration techniques, and development of appropriate optical technology to allow low-cost optical modules.

In this work, we attempt to evaluate the feasibility of optical interconnects from the following perspectives:

- Circuit Issues
- Clock Distribution and Data Routing Applications
- Susceptibility to Variation Effects
- Superiority Compared to Copper Interconnects

1.2 Outline

One of the largest challenges for future interconnects is high-speed global clock distribution. Much of this thesis is focused on evaluation of the feasibility for use of optical interconnect to meet this challenge. In Chapter 2, we describe the component architecture for global optical clock distribution with local electrical distribution. The optoelectronic circuitry required to interface to the global clock is also presented. Next, in Chapter 3, the effects of variation from various components in the optical clocking scheme are discussed, along with the presentation of simulation results. The sensitivity of the combined optical-electronic clock to these variations is a key concern; these variations and sensitivities will introduce skew and limit the clock speed achievable. Chapter 4 illustrates the comparison between optical and conventional metal interconnects, including global data communication as well as clock distribution. Chapter 5 presents the physical realization of the baseline optoelectronic receiver circuit and measurement results. Chapter 6 details suggestions and revision ideas for the receiver circuit. Chapter 7 concludes with possible future work and research directions.

Chapter 2

Optoelectronic Circuitry

Conventional clock distribution falls into two categories, equipotential clocking and H-tree clocking. Equipotential clocking entails distributing a global clock signal to the chip as a regular signal line, as illustrated in Figure 2-1. Since equipotential clocking assumes that the resistance in the wires is negligible and that the entire net is a uniform voltage, this clocking method causes skew when the RC time constant of the nets become significant due to the scaling of feature sizes. In order to achieve the same performance as clock speed increases, the 300MHz and 600MHz Alpha chips used two drivers and subsequently four top level buffers [1]. This is done because only smaller sections of the chip can be modeled as equipotentials at higher frequencies.

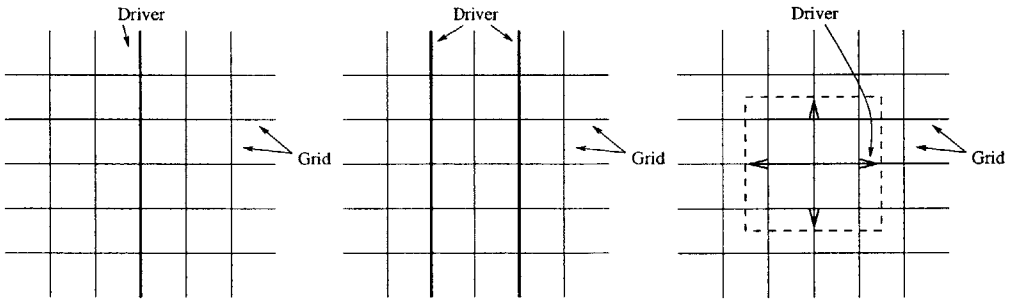

Figure 2-1: One-driver Grid, Two-driver Grid and Windowpane grid

H-trees, on the other hand, are based on the symmetry of the clock net, as shown in Figure 2-2. The clock distribution system is laid out in a way such that the distance between the center of the net to each of the tips is always the same. This would result in the signals arriving at the tips at the same time. H-trees, however, are affected by intra-die variations. Line-width variations and temperature gradients, for example, will result in skew.

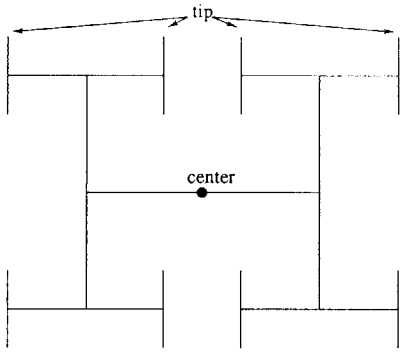

Figure 2-2: H-tree Clock Distribution.

A more novel approach consists of using an array of synchronized Phase-Lock Loops (PLL) [12]. Independent oscillators generate the clock signal at multiple points across a chip; each oscillator distributes the clock to only a small section of the chip. Phase detectors (PD) at the boundaries between the tiles produce error signals that are summed in each tile and are used to adjust the frequency of the node oscillator. This approach is currently still being researched and tested.

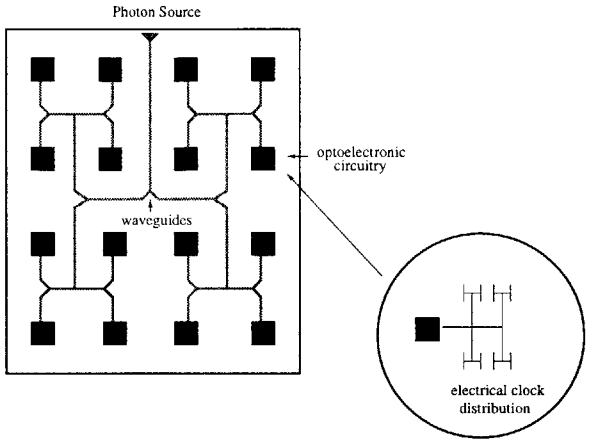

Figure 2-3: Global Optical Clock Distribution.

In this work, we consider optical clocks. Optical clocks can be transmitted in a tree using waveguides or in freespace. The limitation of optical interconnects, in both cases, is their inability to operate as a stand alone module. In order to utilize optics for on-chip communications, optoelectronic circuitry is required to serve as an interface. In this thesis, we focus on developing a baseline optoelectronic circuit for use with waveguide transmission. Figure 2-3 illustrates the component architecture for global optical clock signal distribution with local electrical distribution. The chip is divided into smaller sections, and each section consists of a detector and a receiver module. The global clock is distributed from the photon source (the most popular choice being a laser for its ease of use) through waveguides with splitters and bends to each of the sections. Once reaching the detector in each section, the global clock optical pulses are converted into current pulses. These current pulses feed into the transimpedance amplifier of the optoelectronic circuitry and are amplified into voltage signals, which are distributed through conventional metal interconnects as electrical clock signals. The motivation behind such a hybrid clock distribution system is that smaller areas on chip are exposed to less intra-die variation due to locality. Thus, as long as a skew-free signal is distributed to the nodes, conventional H-tree distribution can be used within the smaller region. Figure 2-3 illustrates 16 smaller sections, but the optimal number of sections depends on the chip size and variation effects. A similar scheme can also be employed for routing data on chip. In the case of clock

distribution, clock skew is the parameter of concern; however, for data distribution the absolute delay is much more important than skew.

Receiver designs generally break down into the block diagram in Figure 2-4. Incoming current pulses from the detector are amplified into voltage pulses through the preamplification stage, depicted as a transimpedance amplifier in the figure. Due to amplification and bandwidth requirements, voltage amplifiers usually follow as the next stage in the design. Some designs incorporate a decision circuit as the final stage for converting the signal into a rail-to-rail digital circuit. Others use buffers to achieve the same purpose. The designs for each module can be implemented as either a single-ended or a double-ended topology.

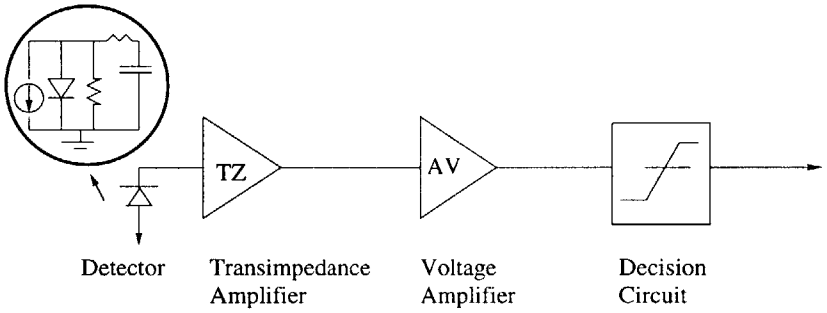

Figure 2-4: Receiver Circuitry Block Diagram.

Woodward et al. [27] has implemented a single-ended receiver design that operates up to 500MHz. The design consists of an inverter-based transimpedance amplifier, followed by a second stage voltage amplifier implemented as an inverter with a diode-connected device, and a buffer before the output. The output of the preamplifier is fed into digital logic elements designed to generate zero skew differential output signals. These signals are applied to off-chip driver circuits.

Ingels et al. [8] designed a single-ended receiver circuitry using a feedback resistor around a string of modified inverters. It uses a replica biasing circuit in order to accurately bias the inverters. The system achieves a gain of 18THzΩ, which makes it capable of amplifying current in the μA region at the expense of a lower bandwidth of 120MHz.

Tanabe et al. [5] approached the design using a differential-ended circuit. The design consists of a preamplifier, an automatic gain control, a PLL and demultiplexers. The design was implemented in a 0.15μm process and achieves a bandwidth of 1.2GHz.

In this work, we develop a baseline optoelectronic circuit [13] to investigate the feasibility of optical interconnects. In order to integrate dense optical interconnects on-chip, the optoelectronic circuitry power dissipation is kept in the mW range. The circuitry operates at a bandwidth of 1GHz on a single power supply voltage in order to facilitate integration with a standard CMOS process without the use of analog extensions. Figure 2-5 provides a block diagram illustration of the optoelectronic circuitry consisting of a preamplification and a postamplification stage. The preamplifier is required in order to convert the current generated by the photodetector upon receiving optical excitation into a voltage signal. It amplifies a 10μA current from the photodetector into a voltage signal with a 10mV amplitude. This voltage signal is further amplified through the postamplification stage into a rail-to-rail voltage swing of 3.3V, which serves as the on-chip clock. The circuit details are presented in the following sections. The photodiode is modeled as a current source in parallel with a diode capacitance and diode resistance.

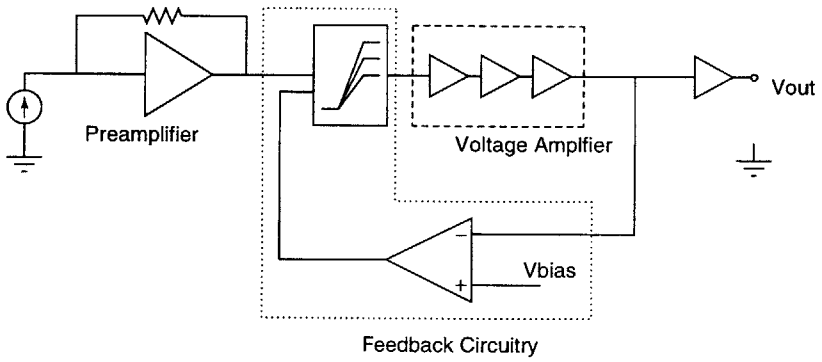

Figure 2-5: Optoelectronic Circuitry Block Diagram.

2.1 Transimpedance Amplifier

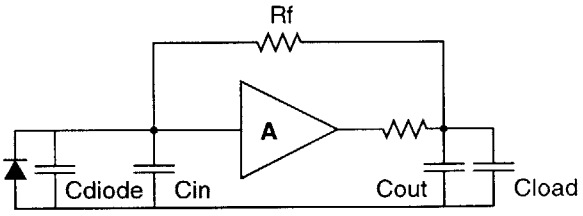

Figure 2-6: Generalized Transimpedance Amplifier.

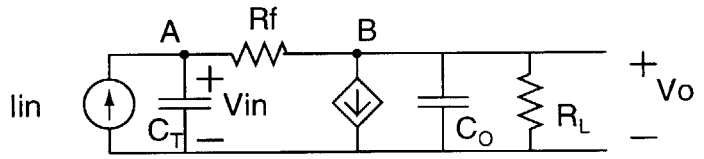

Figure 2-7: Small Signal Model of Transimpedance Amplifier.

A generalized transimpedance amplifier and its small signal model are shown in Figure 2-6 and 2-7. R_L includes the output resistance of the transimpedance amplifier and the load resistance. C_{out} is the output capacitance of the amplifier and C_{load} is the load capacitance. C_{diode} represents the diode of the capacitance and C_{in} denotes the input capacitance of the transimpedance amplifier. R_f is the feedback resistor used in the preamplifier. The C_T shown in the small signal model is the summation of C_{diode} and C_{in}, where C_O includes C_{out} and C_{Load}.

Summing currents at node A in the small signal model, we obtain the following

$$I_{in} = V_{in} s C_T + \frac{(V_{in} - V_O)}{R_f} \tag{1}$$

At node B,

$$G_m V_{in} + \frac{V_O}{R_L} + V_O s C_O + \frac{V_O - V_{in}}{R_f} = 0 \tag{2}$$

Simplifying Equation 2,

$$V_{in} = -V_O \left(\frac{\frac{1}{R_f} + sC_O + \frac{1}{R_L}}{G_m - \frac{1}{R_f}}\right) \tag{3}$$

Substituting Equation 3 into Equation 1,

$$I_{in} = -V_O(\frac{\frac{1}{R_f} + sC_O + \frac{1}{R_L}}{G_m - \frac{1}{R_f}})(sC_T + \frac{1}{R_f}) - \frac{V_O}{R_f} \tag{4}$$

$$\frac{V_O}{I_{in}} = \frac{R_L R_f(\frac{1}{R_f} - G_m)}{1 + G_m R_L + s(C_O R_L + C_T R_L + C_T R_f) + s^2(C_O C_T R_f R_L)} \tag{5}$$

Thus, the transfer function at DC value, Z_f, and pole, p_1, are

$$Z_f = \frac{R_L R_f(\frac{1}{R_f} - G_m)}{1 + GmR_L} \tag{6}$$

$$p_1 = \frac{1 + G_m RL}{C_T(R_L + R_f) + C_O R_L} \tag{7}$$

The following assumption

$$C_T > C_O \tag{8}$$

results in $\omega_{3_{dB}}$ given by the following:

$$\omega_{3_{dB}} = \frac{1 + G_m R_L}{C_T(R_L + R_f)} \tag{9}$$

Looking at Equation 6, we notice that with a high G_m, the absolute gain of the transimpedance amplifier can be estimated as the value of the feedback resistor, R_f. $\omega_{3_{dB}}$, as shown in Equation 9, is a function of the gain, $1 + G_m R_L$ and the RC time constant of the circuit.

The CMOS implementation of the 1GHz transimpedance amplifier [13] is presented in Figure 2-8. It is based on a gm/gm amplifier with a feedback resistor implemented as a PMOS transistor operating in linear region (M4 in the figure), with the resistance given by

$$R_f = \frac{1}{g_{ds} + g_m} \tag{10}$$

The well, being connected to the drain, results in only a small degradation in bandwidth as the well capacitance is added to the input node. The transimpedance amplifier takes a current input of 10μA and converts it into a voltage signal with an amplitude of $10m$V. M1 and M3 form an inverter configuration. M2 is added in order to increase the bandwidth of the preamplifier.

Using the approximation that the gain can be estimated as the value of the feedback resistor, we designed for R_f to be around $1k\Omega$. C_T was estimated to be $100fF$ (the diode capacitance) and R_L was estimated to be the load resistance of the next stage, which is a level shifter. These parameters were used as a starting point in the design of the 1GHz transimpedance amplifier and further iterated with simulations.

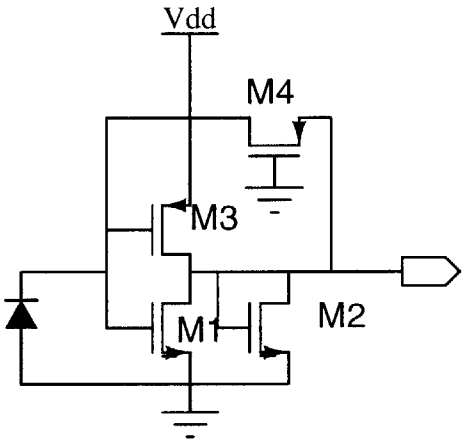

Figure 2-8: Preamplifer, based on [13].

2.2 Postamplifier

The signal has to be further amplified through postamplifiers into the desired rail-to-rail signal due to the insufficient gain from the preamplifier. This can be accomplished through a string of inverters biased at their threshold voltages. The first inverters act as linear amplifiers due to the small input signal. Closer to the final stages, clipping occurs at the rails. Thus, a larger input will merely result in a shift forward of the

first clipping. As a result, we have avoided automatic gain control at the expense of accurately biasing of the inverters. This is accomplished through replica biasing [13], as shown in Figure 2-12.

Conventional inverters are unable to achieve a high bandwidth due to their inherent gain. Thus, modified inverters are used. Figure 2-9 illustrates such an inverter. The diode connected NMOS shifts the second-order pole to higher frequencies by reducing the small-signal impedance on the inverter's output node. The gain is also limited as a result. The small signal circuit is shown in Figure 2-10; using the source-absorption theorem, a simplified small signal model is obtained, shown in Figure 2-11.

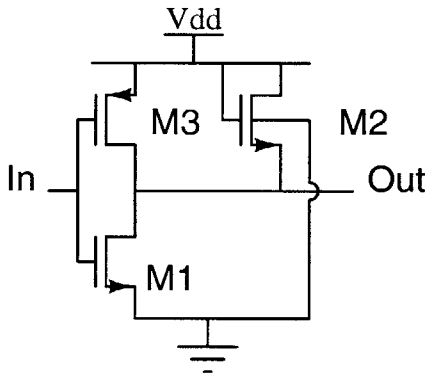

Figure 2-9: Voltage Amplifier.

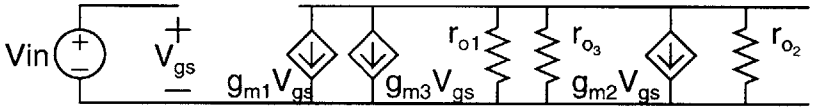

Figure 2-10: Small Signal Model of Voltage Amplifier.

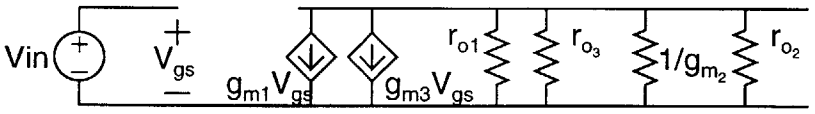

Figure 2-11: Simplified Small Signal Model of Voltage Amplifier.

From the model, we can derive the gain of the amplifier:

$$V_{in} = V_{gs} \tag{11}$$

$$V_{out} = (g_{m1} + g_{m3})V_{gs}(g_{ds1} + g_{ds2} + g_{ds3} + g_{m2}) \tag{12}$$

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} + g_{m3}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m2}} \tag{13}$$

Assuming

$$g_{m2} \gg g_{ds2} + g_{ds1} + g_{ds3}$$

Equation 13 simplifies to

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} + g_{m3}}{g_{m2}} \tag{14}$$

Where without M2, the gain would be

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} + g_{m3}}{g_{ds1} + g_{ds2} + g_{ds3}} \tag{15}$$

The $\omega_{3_{dB}}$ is given by the following:

$$\omega_{3_{dB}} = \frac{1}{R_{out}C_{out}} \tag{16}$$

where, in the case where M2 is included, R_{out} is approximately

$$R_{out} = \frac{1}{g_{m2}} \tag{17}$$

and C_{out} is given by

$$C_{out} = C_{load} + C_{gd1} + C_{db1} + C_{gs3} + C_{sb3} + C_{gs2} + C_{sb2} \tag{18}$$

Thus, $\omega_{3_{dB}}$ is increased by the transconductance of M2 while the gain is reduced simultaneously. In this design, three of these modified inverters are cascaded together in order to obtain sufficient gain for a single stage. A single stage was designed to have a gain of $20dB$ with a cutoff frequency of 1GHz.

2.3 Feedback Circuitry

One critical issue in using the above circuitry is accurate biasing. Inaccurate biasing of the inverter strings will lead to a degraded duty cycle. In this work, replica biasing, as shown in Figure 2-12, is used.

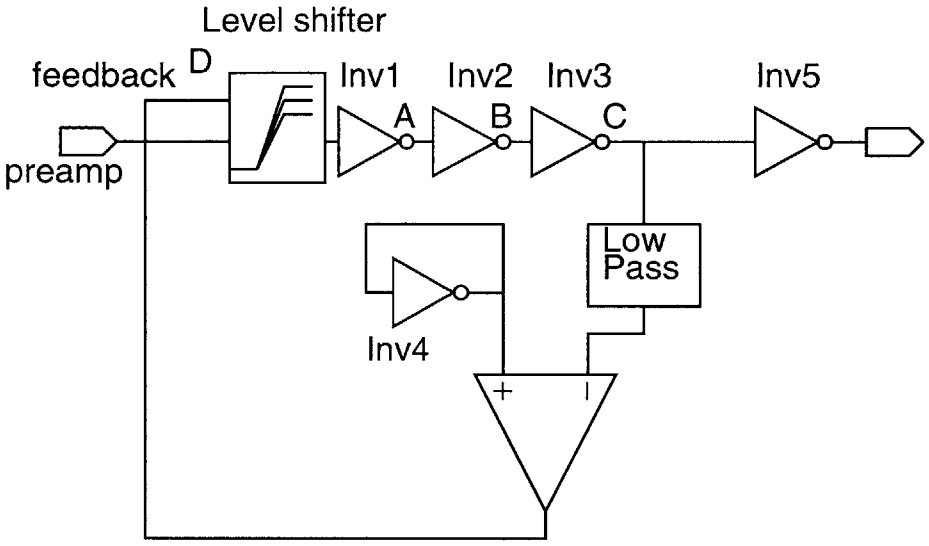

Figure 2-12: Replica Biasing.

The feedback circuitry consists of a level shifter (Figure 2-13), a comparator (Figure 2-14) and a low pass filter. The low pass filter obtains the DC value of the string of inverters at node C. This DC value is compared (through the comparator) to the threshold voltage of Inverter 4, which is a replicate of the string of inverters. The output of the comparator will adjust the level shifter accordingly. The output of the level shifter increases with decreasing input value and vice versa. For example, when node C a has DC value greater than the threshold of the inverter, the comparator will have a voltage smaller than the nominal value. This will cause the DC voltage at the output of the level shifter to increase. As a result, the DC voltage at node A will decrease while the value at node B will increase and the value at node C will decrease. This negative feedback will result in the convergence of the DC biasing for the inverters.

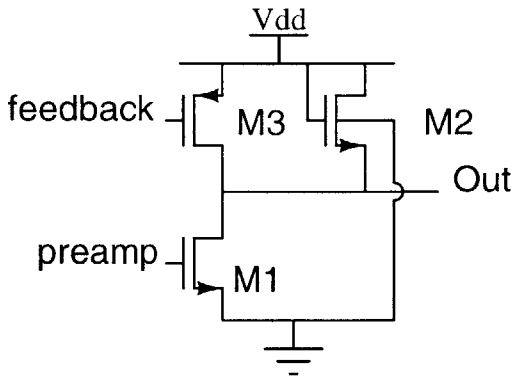

Figure 2-13: Shifter Circuit.

Since the shifter is in the signal path, it is designed with a bandwidth comparable to the modified inverters, with only a small gain, given by the following equation. It results from an analysis similar to that of Equation 14, but with g_{m3} removed as M3 is feedback connected:

$$A_V = \frac{g_{m1}}{g_{m2}} \tag{19}$$

The comparator, as shown in Figure 2-14 has a DC gain of 120, with a bandwidth of around 45KHz. To obtain the low pole, a capacitor is placed in Miller configuration. The zero introduced by the Miller capacitor is nulled by a resistor, a technique widely used in operational amplifier designs. In order to ensure stability of the feedback circuitry, a low corner frequency is used.

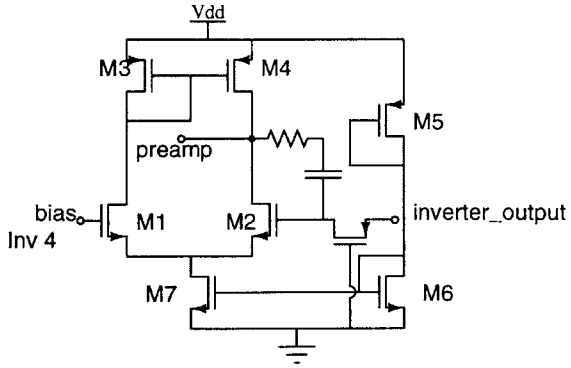

Figure 2-14: Comparator Integrated with LP Filter.

2.4 Complete Receiver

The complete receiver [13] is shown in Figure 2-15. The input current is converted into a voltage signal through the preamplifier, it is further amplified by $20dB$ through the second stage, which consists of a level shifter, three modified inverters and a feedback system for DC biasing. Since a single post amplification stage is insufficient for the input current that we are considering, a second post amplification stage, identical to the first, is added. The final output is buffered into a rail-to-rail voltage swing. The transient simulation results are shown in Figure 2-16.

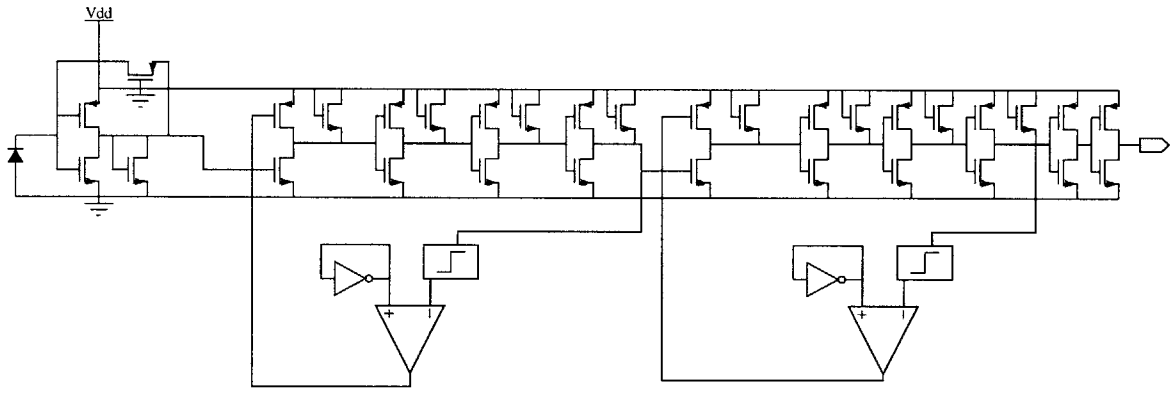

Figure 2-15: Complete Receiver Circuitry.

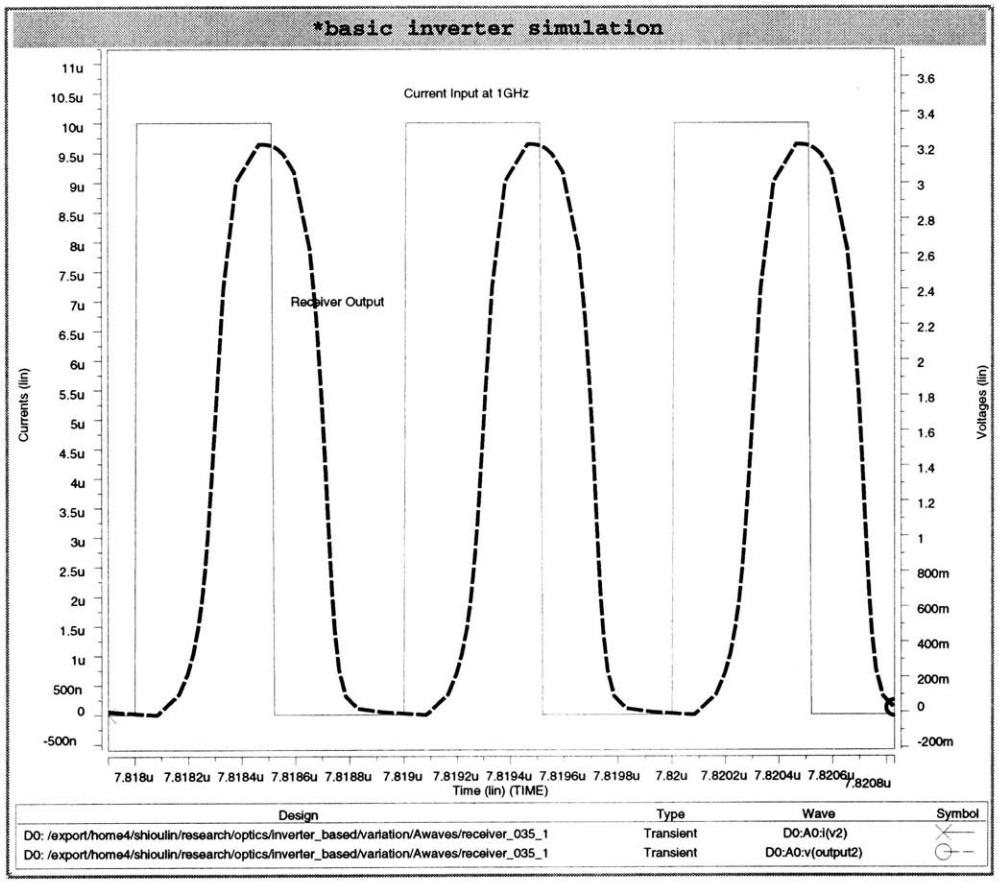

Figure 2-16: Simulation Results at 1GHz.

Chapter 3

Variation Effects

As devices continue to scale down, variation effects are becoming more prominent and are causing substantial performance degradation in designs. In large chips, spatial pattern dependent interconnect and device variations result in clock skew and delay [16]. In analog designs, much effort has been concentrated on device matching since mismatch will sometimes reduce design yield.

In conventional interconnects, spatial dependent interconnect variation and device variation results in clock skew and data bus delay. In implementing the clocking scheme suggested in Chapter 1, variation stems from three sources: the waveguide, the detector and the receiver circuitry. We will study the individual contributions of these aforementioned sources to the total clock skew.

In this chapter, we first review several approaches currently being used to understand effects of variation, and then present our methodology and results for analyzing variation effects on the optical module and the circuitry.

3.1 Statistical Modeling

Several approaches have been used to model process variations. In the following sections, we present a brief overview of some of the approaches.

3.1.1 Process Oriented Approach

A process oriented approach to variation analysis uses a process simulator, a device simulator, and a circuit simulator, as shown in Figure 3-1. The process simulator takes in the process description along with an IC layout and generates physical and geometry characteristics such as dopant profiles and thicknesses of various layers. These outputs are fed into a device simulator which produces device results suitable for device parameter extraction; these device models then form the inputs to the circuit simulator. Variations can be introduced into the process description in order to understand the effects, resulting in the scheme shown in Figure 3-2 [19].

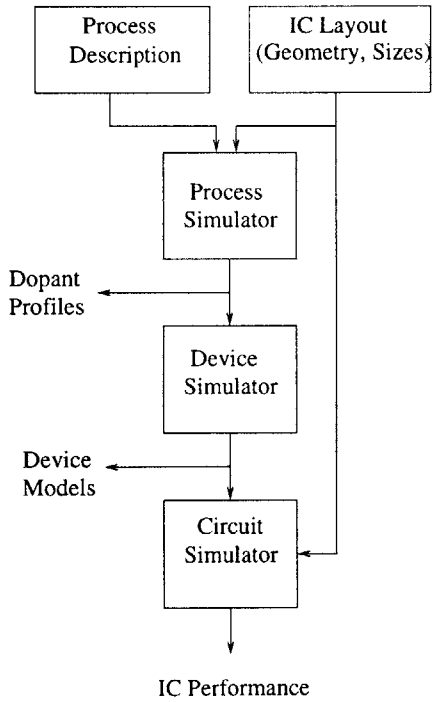

Figure 3-1: Process Oriented IC simulation.

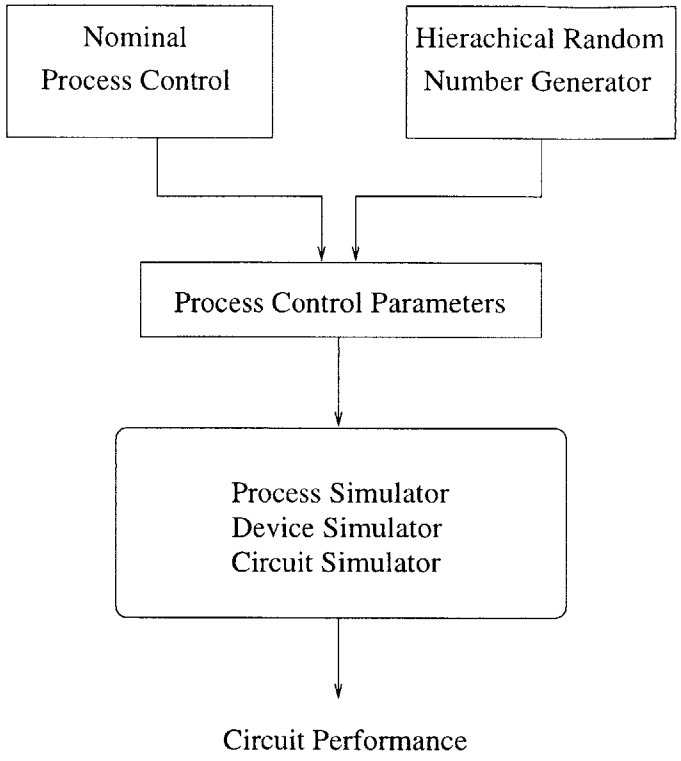

Figure 3-2: Simulation Scheme for Process Level Variation.

3.1.2 Device Oriented Approach

A device-oriented approach to variation analysis, on the other hand, is based on device model parameter extraction from measured I-V curves, as shown in Figure 3-3. Measurements for different sets of transistors taken from different areas on the chip are conducted and plotted. The model parameters extracted from the I-V curves will exhibit statistical variations and correlations. In using this approach, it is often assumed that independent variation occurs between the model parameters and that the circuit would be operational over an arbitrary combination of the variations of parameters such as threshold voltage, body effect and oxide thickness. This will lead to inaccurate characterization of the IC process variations. For example, independent variation between V_{tn} and V_{tp} would overestimate the variability of a transistor since the correlation of V_{tn} and V_{tp} is usually strong.

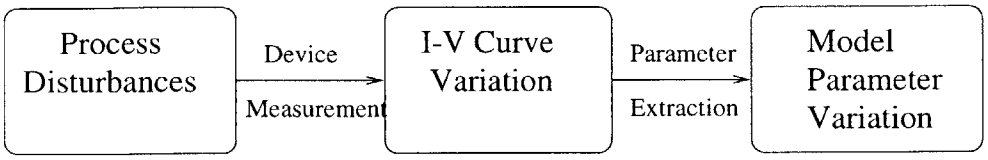

Figure 3-3: Device Oriented Approach.

3.1.3 Inter-Die Variations Approach

Statistical analysis using inter-die variation usually assumes that process disturbances affect devices within the same chip in the same way, i.e., intra-die variations are negligible. In using this approach, one would need to choose a set of model parameters (for forming a parameterized inter-die statistical model) to characterize the device variations. This lends utmost importance to identifying the critical model parameters. All other parameters can then be generated from this set using regression dependencies.

The parameters are generally chosen using factor analysis and principle component analysis [4], which account for the correlations between the different device parameters (e.g., between V_{tp} and V_{tn}). A regression model is then built from these parameters.

3.1.4 Intra-Die Variations Approach

The above approximation approach would be acceptable for digital circuits, but in cases where device matching is important, it would lead to significant error. The most common example is matching in analog circuit blocks, where mismatch would cause an offset in the output. The research on intra-die variation has mostly focused on the mismatch variance [17], [11], [22]. One approach taken by [17], as shown in Figure 3-4, is most interesting because it is capable of generating statistically significant models from intra- and inter-die parameters. It uses statistical parameter analysis to obtain parameter means, correlations and standard deviations as a function of device size and spacing. Principal component analysis and σ-space analysis are performed on these parameters. In using PCA, correlations within transistor are preserved while

σ-space analysis preserves variance between transistors. The output from PCA and σ-space form the input for generation of model decks. The model decks and circuit description are then used for circuit simulation.

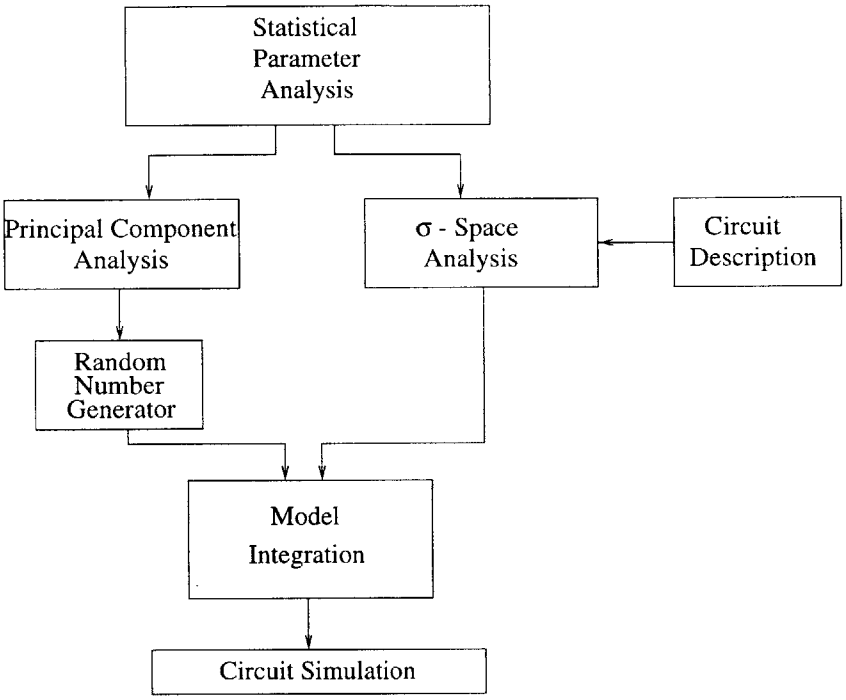

Figure 3-4: Simulation Flowchart.

The initial phase of our work closely resembles the inter-die variation approach, where circuit parameters are assumed to be independent of each other. We perform a sensitivity analysis on poly length and threshold voltage. We also look at environmental variation, including power supply and temperature. The results of our sensitivity analysis are used to create a regression model, either linear or quadratic, depending on the goodness of fit. This approach may overestimate the variation effects, but gives the worst case bound, which provides sufficient information for comparison purposes.

We follow the methodology depicted in Figure 3-5 to perform sensitivity analysis for the receiver circuitry. The script takes three input files - the parameters file, the transistor model template and the receiver circuit template. The parameters file contains the model parameters and the range over which they should be varied; this results in different model files which are used with the circuit templates to generate

Spice files. The Spice simulations are performed in batches and the delay and skew numbers are extracted from the output. In cases where there are no device variations but only operating variations, the methodology follows the bypass route as depicted in Figure 3-5.

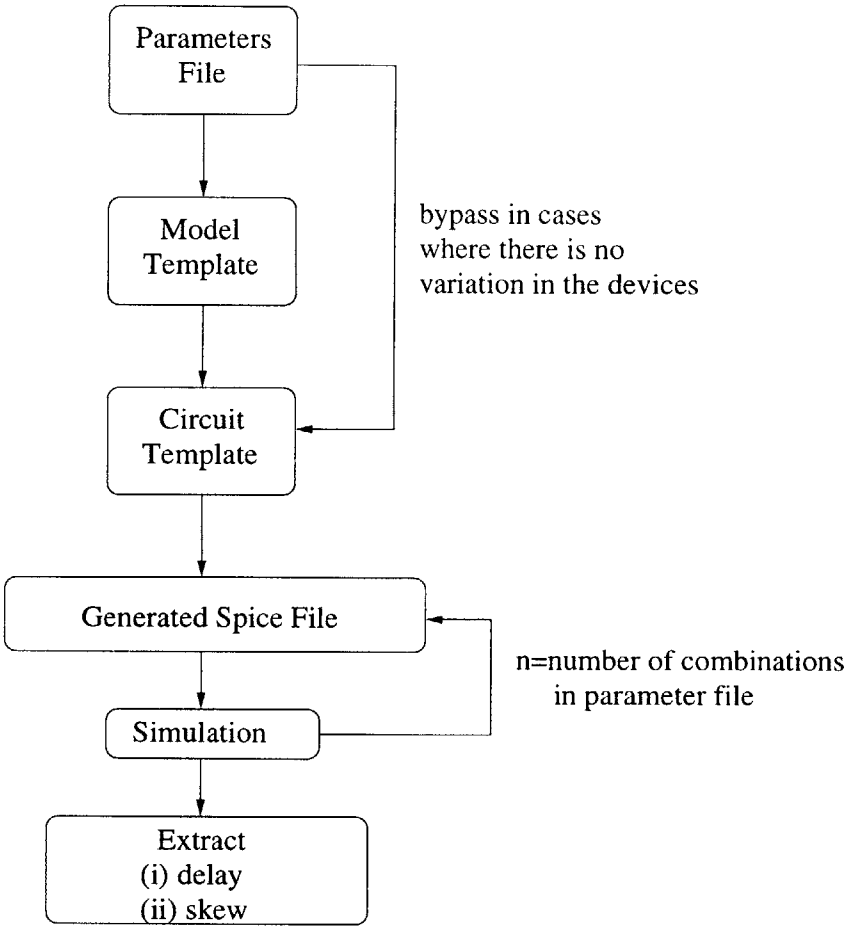

Figure 3-5: Flow Chart for Variations Effect Simulation.

A different methodology is used for simulating the effects of variation in the optical modules. For the waveguides, we consider the effects of varying the waveguide dimensions as these will affect clock skew in the system. For the detector, we follow the methodology illustrated in Figure 3-6. Variations from optical power and dark current are simulated as input current variation. This perturbs the Spice template. Clock skew and delay numbers are extracted from Spice simulations performed with the perturbed templates. The next sections present the effects of variation in the waveguide, the detector and the receiver module.

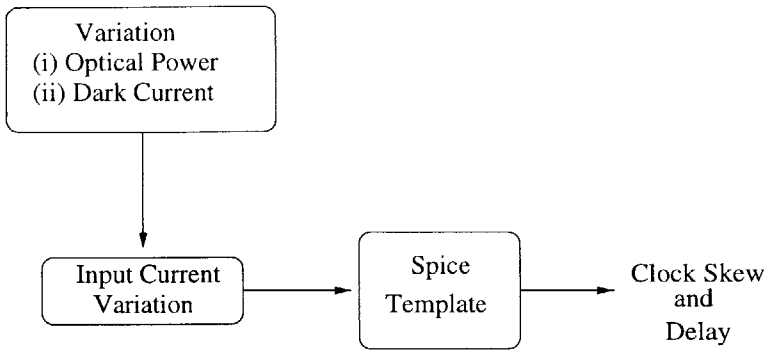

Figure 3-6: Methodology for Simulating Variation Effects in Detector.

3.2 Waveguide

Waveguides on chip, as illustrated in Figure 3-7, are fabricated using Si/SiO_2. The high dielectric contrast confinement shrinks the wavelength of the light to dimensions of $\frac{\lambda}{n}$. Smaller sized devices are preferred because they enable faster optoelectronic transduction, higher local fields to drive non-linear interactions and higher levels of integration which provides new functionality at lower costs.

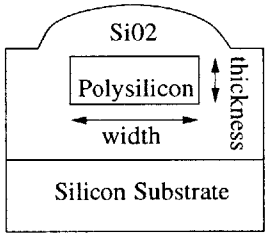

Figure 3-7: Polysilicon Waveguide.

The variation in waveguide dimensions will result in skews at different branches. From simulations, the dimensions in waveguide will vary around 10% [15], which will result in a skew of $2ps$ in arrival of light pulses.

3.3 Detector

Variations from the detector are by the varying amounts of detector current at the output. Detector current is a function of the dark current (I_{dark}), also known as

leakage current, and photocurrent (I_{photo}). Photocurrent, in turn, is a function of optical power ($P_{optical}$) and detector efficiency ($E_{detector}$).

$$I_{detector} = I_{photo} + I_{dark}$$

$$I_{photo} = P_{optical} + E_{detector}$$

Photocurrent that a detector can generate varies depending on the optical coupling between the detector and waveguide. In addition, optical power will also vary up to a worst case bound of 10% [15]. These two factors combine to cause a varying detector current at the output, which results in clock skew and databus delay.

Since dark current is inherent to photodetectors and is a fixed constant, a larger input current will be less susceptible to the variation caused by dark current because dark current will have a much smaller impact proportionally. A larger input current would also reduce the number of stages required in the receiver circuitry, which would result in less clock skew in the system.

One research direction is to investigate the effects of different levels of optical power on clock skew and propagation delay in the receiver. This can also be viewed as investigating the tradeoff in power requirements for the two modules, the electrical module and the optical module. To capture the effects of optical power variation, simulations are performed here by varying the input current. Three points, 10μA, 100μA and 1mA, are chosen to obtain a snapshot of the trends.

With higher levels of input current, the receiver circuitry can be trimmed due to less required gain. With an input of 100μA current, the gain stages of the voltage amplifiers can be reduced, resulting in the circuit shown in Figure 3-8. Another order of magnitude increase in current implies that the preamplifier itself is sufficient to obtain the gain required, with the resulting circuit shown in Figure 3-9.

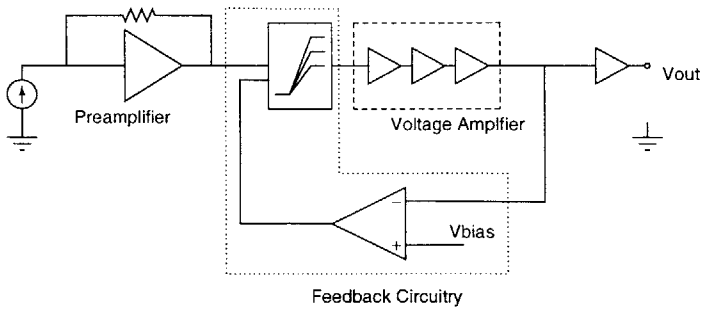

Figure 3-8: Receiver Circuitry for 100μA Input Current.

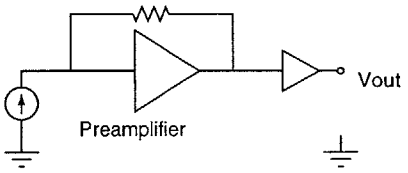

Figure 3-9: Receiver Circuitry for 1mA Input Current.

Results from these circuits are tabulated in Table 3-1 and Table 3-2. They illustrate the effects of varying levels of input power on skew and delay for each of the three design alternatives.

Input Current	Receiver Power	Skew
8μA	60mW	8ps
10μA	60mW	nominal
12μA	60mW	4ps
89μA	35mW	4ps
100μA	35mW	nominal
111μA	35mW	2ps
900μA	11.5mW	22ps
1000μA	11.5mW	nominal
1100μA	11.5mW	14ps

Table 3-1: Impact of Input Current on Skew

Looking at the impact of input current on skew, we notice that for an input current of 100μA, the skew is almost reduced in half compared to the case where the input current is 10μA. This is because the receiver circuitry for the higher input current has one less amplification stage, thus it is less susceptible to the impact of input current variation. On the other hand, for the case where input current is 1000μA, clock skew effects are very pronounced. This is due to the nature of the design coupled with the

Input Current	Receiver Power	Delay
10μA	60mV	1.23ns
100μA	35mV	0.868ns
1000μA	11.5mV	.658ns

Table 3-2: Impact of Input Current on Delay

huge absolute magnitude of the variation. The design used for an input current of 1000μA consists of only the preamplification stage and buffers. Such a design is very susceptible to any variation effects.

The relationship between input current and delay, shown in Table 3-2, is as expected. As we increase the input current, the delay is reduced substantially.

Reducing the skew and delay is thus circuitry dependent and is also a direct tradeoff with the amount of current, i.e., the amount of optical power required. With the appropriate circuitry, both skew and delay decrease as optical power is increased, and the circuit power requirements are also shifted to the optical module. The decision thus hinges on the circuit and its response to the varying level of current. In this case, the best design point of these considered would be at 100μA. With this level of optical power, we obtain the smallest amount of skew with less power consumed in the circuit. If we were only concerned about absolute delay, then the best design point would be at 1mA. One would also need to evaluate the cost function of the optical modules and the feasibility of providing a higher optical power.

3.4 Receiver Circuitry

The receiver circuitry is subjected to varying degrees of variation from the devices and the environment, some stemming from the sources below:

- Systematic Process Variation

- Power Supply Variation
- Operating Temperature Variation

3.4.1 Process Variation

There are two components in process variation, systematic and random. Random variation includes doping densities, implant doses, variation in width and thickness of active diffusion, oxide layer and passive conductors, masking and etching effects, and parasitic capacitance values. Recent studies have shown that systematic within-die variation is a significant concern [3]. Most of the variation resulting from chemical mechanical polishing (CMP) of the inter-layer dielectric (ILD) is based on systematic spatial effects and varies substantially within die.

In this work, we focus on random variation effects that cause device mismatches; we consider here the effects that L_{poly} and V_T variations have on the receiver circuitry.

Threshold variation

The difference in threshold voltages, ΔV_T, between two transistors is assumed to be normally distributed with zero mean and standard deviation [24], [11]:

$$\sigma_{\Delta_{VT}} = \frac{A_{VT}}{\sqrt{WL}} = \frac{qt_{ox}\sqrt{2N\,t_{depl}}}{\epsilon_0\epsilon_{ox}\sqrt{WL}}$$

This is based on the assumption that mismatch is caused by independent random disturbances and that the correlation distance of the statistical disturbance is small compared to the active device area. These assumptions lead to a proportionality of the standard deviation with the inverse square root of the area. For a feature size of .35μm, A_{VT} is found to be 8mVμm. [22]. A plot of $\sigma_{\Delta_{VT}}$ is shown in Figure 3-10.

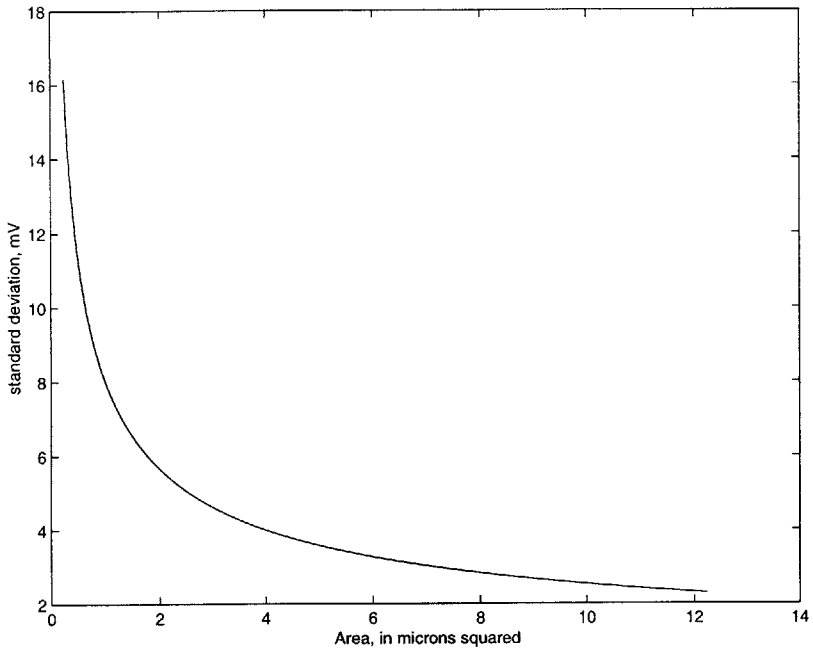

Figure 3-10: Standard Deviation of V_T mismatch, $\sigma_{\Delta Vt}$, versus Area for a .35μm process.

Using a one-sided alpha risk of 0.001, which translates to a 99.9% confidence level that the threshold voltages fall within the limits, the upper and lower bounds of the threshold voltages are given as follows:

$$V_T = \mu_{VT} \pm 3.09\sigma_{VT}$$

Since $\Delta_{VT} = V_{T1} - V_{T2}$, the standard deviations are related as the following:

$$\sigma^2_{\Delta VT} = \sigma^2_{VT1} + \sigma^2_{VT2}$$

Assuming the distributions have the same mean and variance,

$$\mu_1 = \mu_2$$

$$\sigma_{VT1} = \sigma_{VT2} = \sigma_{VT}$$

Thus,

$$\sigma^2_{\Delta VT} = 2\sigma^2_{VT}$$

V_T can then be expressed as

$$V_T = \mu_{VT} \pm \frac{3.09}{\sqrt{2}}\sigma_{\Delta VT}$$

The resulting threshold voltage bounds are shown in the Figures 3-11 and 3-12. Upon looking at the plots, 99.9% of the V_T variations for both NMOS and PMOS devices fall within 7% of the mean value. Simulation results for effects of V_T variation of $\pm 15\%$, are shown in Figure 3-13.

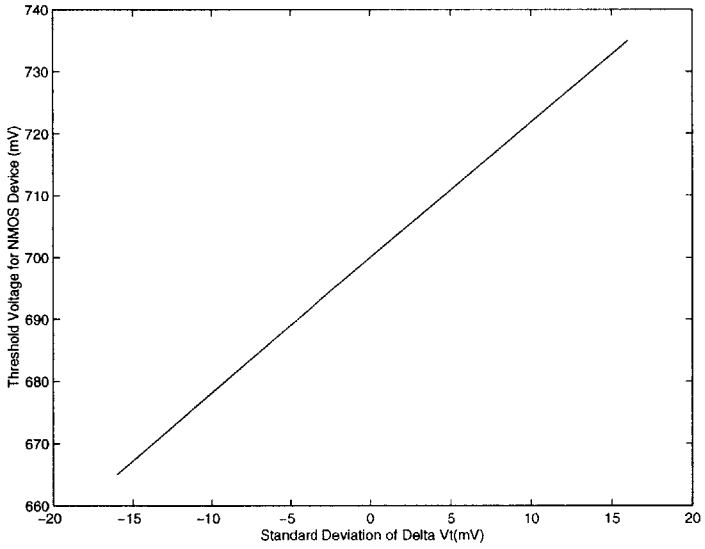

Figure 3-11: V_T for NMOS Device versus the Standard Deviation for a .35μm Process.

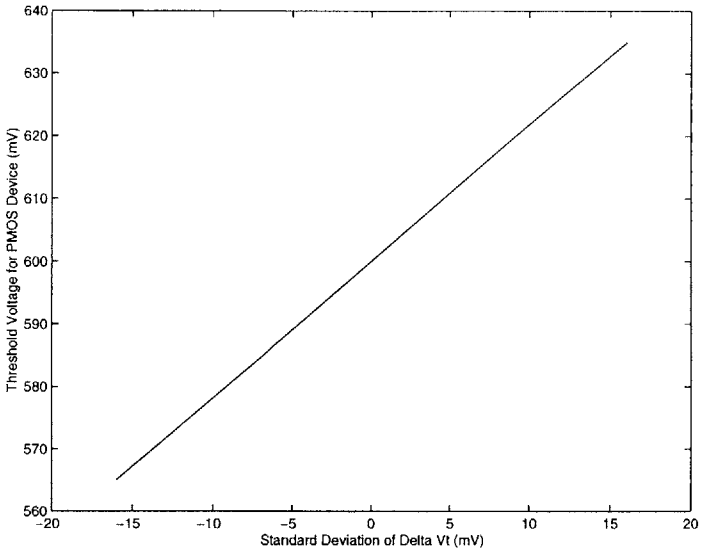

Figure 3-12: V_T for PMOS Device versus Standard Deviation for a .35μm Process.

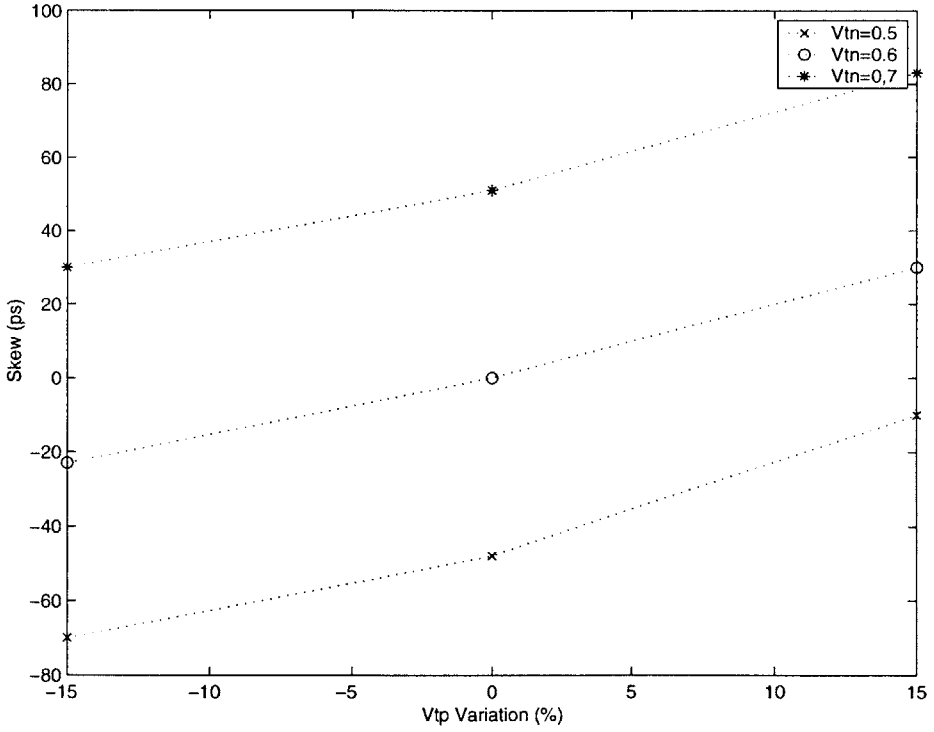

Figure 3-13: Effects of V_T Variation on Clock Skew for Optical Clock Receiver.

Channel Length Variation

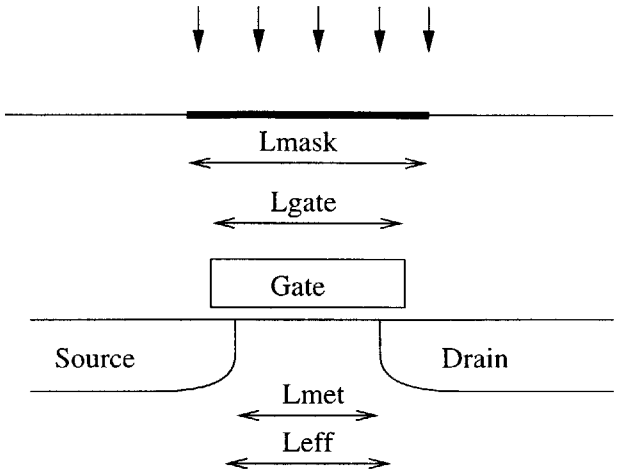

Figure 3-14: Cross Section Diagram of a MOS Device.

Figure 3-14 illustrates various definitions of channel length [25]. L_{mask} is the design length on the polysilicon etch mask, which is reproduced on the wafer as L_{gate} through lithography and etching processes. For the same mask, L_{gate} may vary from chip-to-chip, wafer-to-wafer and run-to-run. L_{met} is the distance between the metallurgical junctions of the source and drain diffusions at the silicon surface. L_{eff} is different from the above because it is defined through electrical characteristics of the MOSFET. Qualitatively, L_{eff} is a measure of how much gate-controlled current a MOSFET delivers in long channel devices. It is used for process monitoring and circuit modeling. L_{eff} can be related to L_{mask} by the following:

$$L_{eff} = L_{mask} - \Delta L$$

All process variation factors, for example, lithography, etch biases, lateral source drain implant straggle and diffusion, are lumped into ΔL. Current lithography and etch technology can typically achieve a variation of $\pm$5-10%. However, measurements of identical structures within the same die reveal variations on the order of 15-20% [23]. Sensitivity simulations for the receiver circuitry are shown in Figure 3-15. We see that skew varies linearly with poly length variation. A skew of 180ps was simulated for a poly length variation of 22.5%.

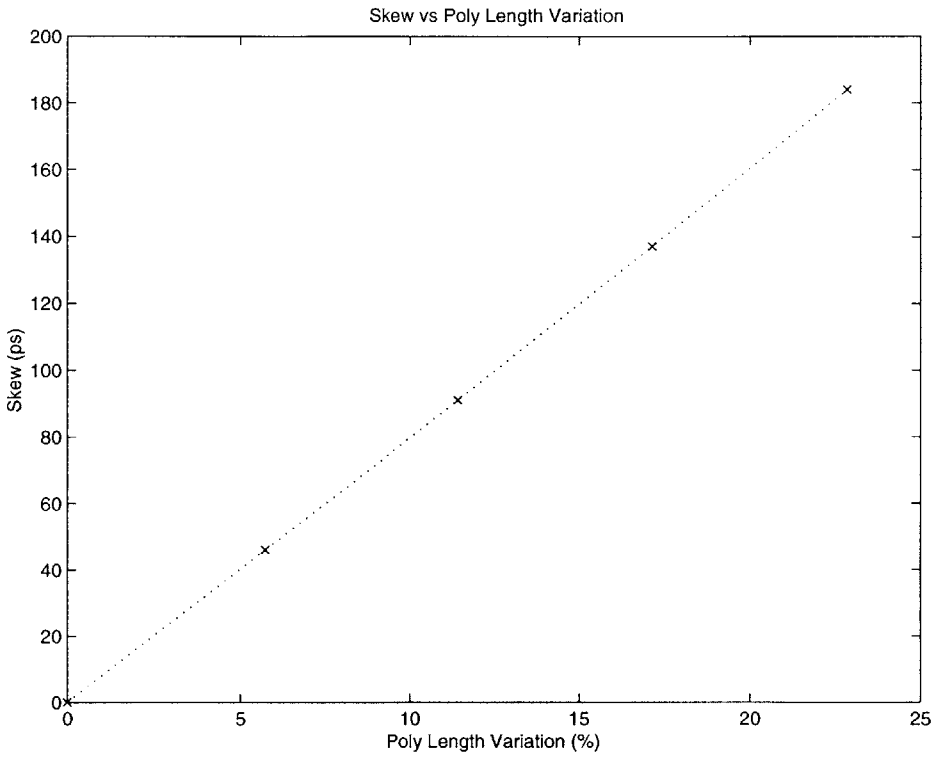

Figure 3-15: Effects of L_{poly} on Clock Skew for Optical Clock Receiver.

3.4.2 Power Supply Variation

Power supply in recent technology generations can vary up to $\pm 10\%$. Results from our simulations show that the receiver circuitry is susceptible to power supply variation. Sensitivity simulation results are shown in the Figure 3-16.

3.4.3 Operating Temperature Variation

Variations in operating temperature can cause significant changes in device characteristics, which will impact clock skew and delay in the receiver circuitry [20]. Simulations of temperature effects are performed with results shown in Figure 3-17.

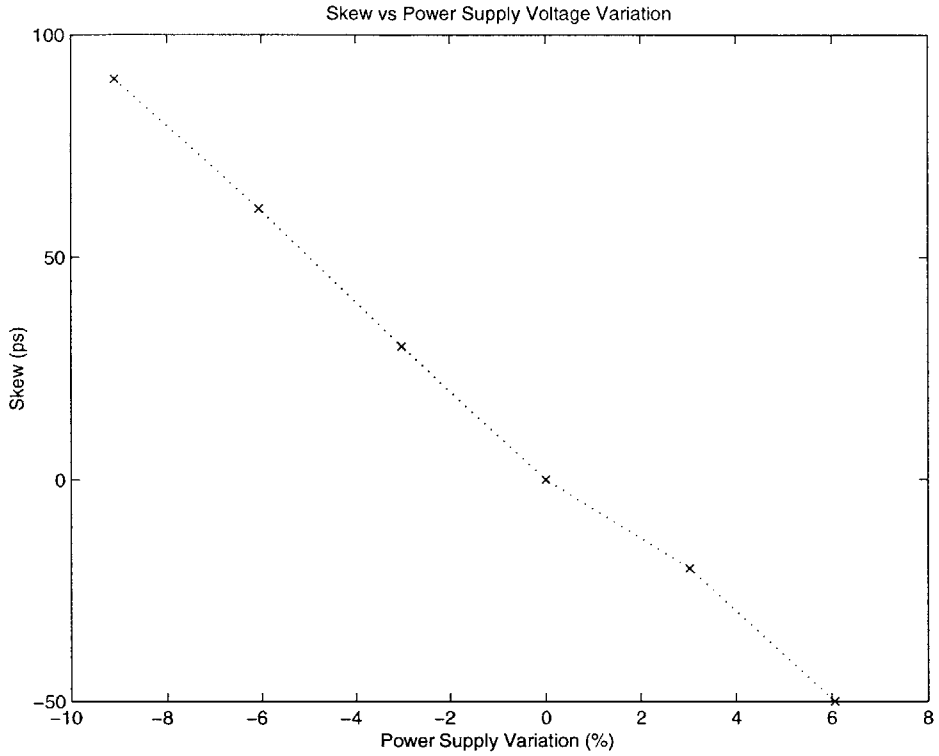

Figure 3-16: Effects of Power Supply Variation on Clock Skew for Optical Clock Receiver.

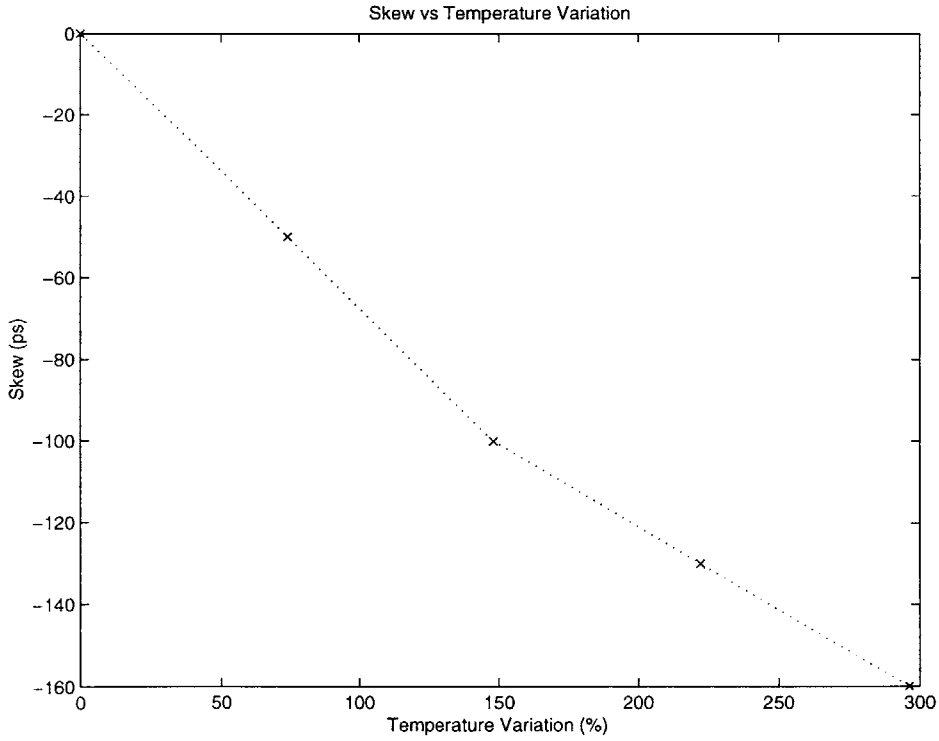

Figure 3-17: Effects of Temperature Variations on Skew for Optical Clock Receiver.

3.5 Summary of Process and Environmental Variation Effects

Upon looking at the results, the effects of poly length, threshold voltage, temperature and power supply variations can be modeled as a linear relationship. The sensitivity simulations are performed on each individual sources of variation; in order to understand their interaction, we combine all skew effects from individual contributions into an aggregate clock skew. This presents a unified picture, where some sources of variation have positive impact on skew while others have a negative impact on skew. The model equations for each source of variation are as follows:

$$\begin{aligned} Skew_{L_{poly}} &= 2295 * L_{poly} - 803.45 \\ Skew_{VTn,VTp} &= 276.7 * VTp + 486.7 * VTn - 480.9 \\ Skew_{Power} &= -278 * \text{Power} + 922 \\ Skew_{Temperature} &= -2 * \text{Temperature} + 46 \end{aligned}$$

In combining these equations, we obtain

$$Skew_{Total} = 2295 * L_{poly} + 276.7 * VTp + 486.7 * VTn - 278 * \text{Power} - 2 * \text{Temperature} - 316.35$$

Higher power supply and temperature will reduce the total skew while increasing poly length and threshold voltage will increase the total clock skew. In terms of sensitivity, we look at the change in skew for a 10% variation in the parameter (Table 3-3). Since these are linear equations, the skew impact can be scaled easily for other percentages.

Parameter	Skew for 10% variation
Temperature	10ps
Power Supply	100ps
Threshold Voltage	20ps
Poly Length	80ps

Table 3-3: Sensitivity of Variation Parameters.

Chapter 4

Optical and Cu Interconnect

Previous chapters covered the design of the baseline receiver and simulation results of variation effects based on this baseline receiver. In order to fully assess the feasibility of optical interconnects, these results need to be compared to the performance of conventional metal interconnects. In this chapter, we present a study of variation effects on copper interconnects pertaining to delay and clock skew. A comparison between optical and conventional interconnects then follows.

4.1 Variation Effects on Copper Interconnect[1]

In the copper damascene process, ILD is first deposited and patterned to define "trenches" where the metal lines will lie. Metal is then deposited to fill the patterned oxide trenches and polished to remove the excess metal outside the desired lines using chemical-mechanical polishing (CMP). Thus, the main source of variation resides in the metal wire geometry. During metal CMP, interconnect thickness is reduced due to effects of dishing and erosion, as shown in Figure 4-1. Dishing is defined as the

[1] **Work performed in collaboration with V. Mehrotra [16]**

recessed height of a copper line compared to the neighboring oxide, and erosion is defined as the difference between the original oxide height and the post-polish oxide height. This metal thickness variation in copper damascene CMP process can be modeled as a function of the metal pattern density, linewidth, and linespace [21].

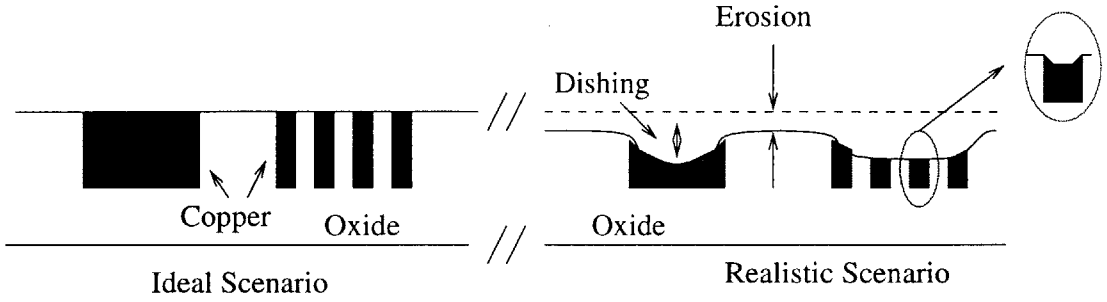

Figure 4-1: Effects of Copper Damascene CMP.

In assessing the impact of variation on clock skew and delay in copper interconnects, we employ the methodology shown in Figure 4-2. The layout and connectivity information are used to extract the capacitance and resistance values. Together with variation models and geometry information, the capacitance and resistance values form the input for the variation analysis tool. The output from the variation analysis tool is a perturbed structure from which a Spice netlist is obtained [16]. The author's efforts were concentrated on understanding the effects of variation on databus delay.

4.1.1 Interconnect Delay

In undergoing copper CMP, an array of interconnects will experience varying amounts of erosion based on its position within an array, resulting in the profile as shown in Figure 4-3. Each interconnect will then have different resistance, capacitance and resulting interconnect delay. In cases where these array of lines represent data buses, the impact from CMP variation effects is substantial because it results in different arrival times of data within the same array.

In order to better understand the effects, the delay of long interconnect lines is simulated. Interconnects are modeled using the distributed *RC* delay model in Figure

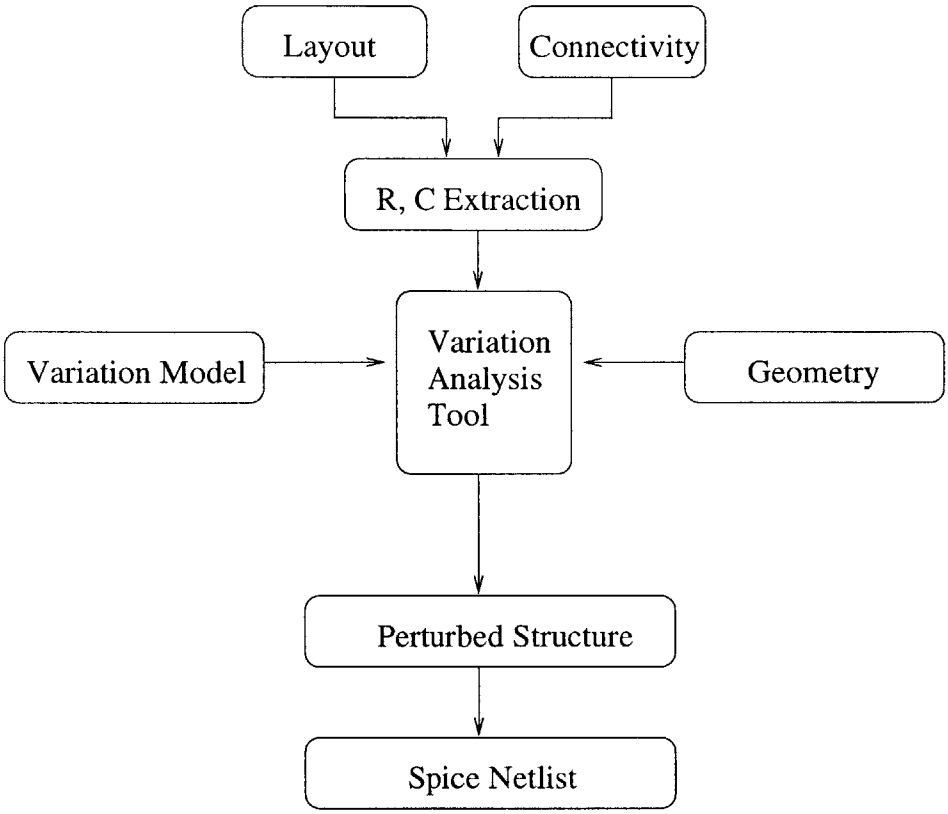

Figure 4-2: Methodology for Assessing the Impact of Spatial Variation.

4-4. Delay variation versus bit position of 5mm lines at various pitch in Cu interconnect with .80μm metal and ILD thickness is shown in Figure 4-5. The simulation is performed with the bits compared to the nominal case (where no erosion occurs) and with the assumption that the interconnects are surrounded by blanket oxide. Each bit in the array experiences different delay depending on its position.

Several key points can be summarized from the simulation. First, delay variation is a function of the inverse of pitch. This is due to the impact that Cu CMP has on lateral capacitance and resistance. Second, as the number of bits in the bus increases, the difference in erosion between the center and edge bits decrease, resulting in less delay variation. Over the range of parameters considered in our study, the maximum delay variation is 64ps.

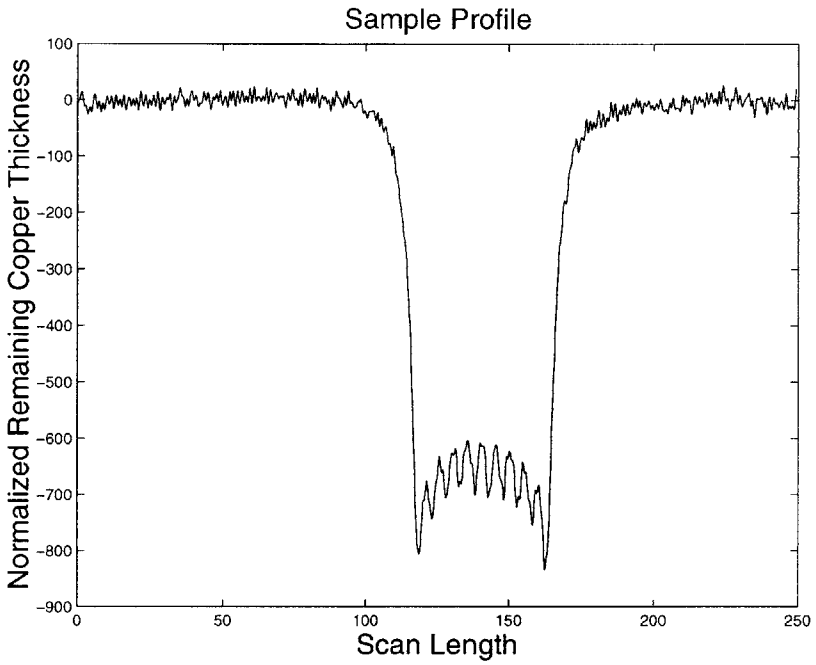

Figure 4-3: Profilometry Trace of Array of Interconnects after CMP.

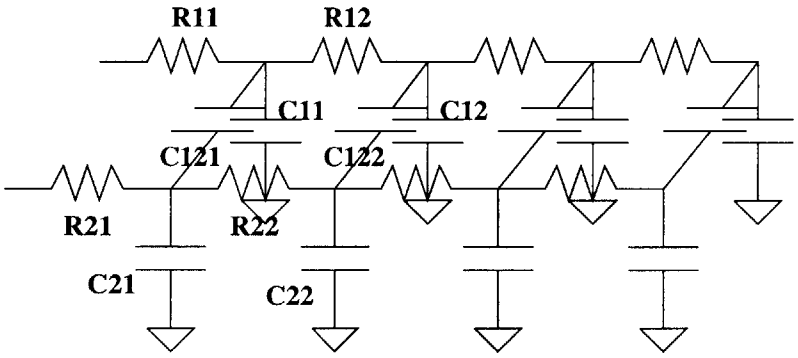

Figure 4-4: Interconnect Distributed *RC* Delay

4.1.2 Clock Skew

Clock skew was investigated by analyzing the effects of pattern dependent interconnect and device variation on a clock distribution circuit for a high speed microprocessor shown in Figure 4-6 [9]. The circuit, designed in a .22μm, 6 layer metal technology, uses copper interconnect with the top two metal layers designated for clock distribution. The circuit is driven by a series of cascaded drivers at the root and is loaded with latches at the output. This makes for a prime analysis candidate due to its highly symmetrical property, which allows for the isolation of process variation effects.

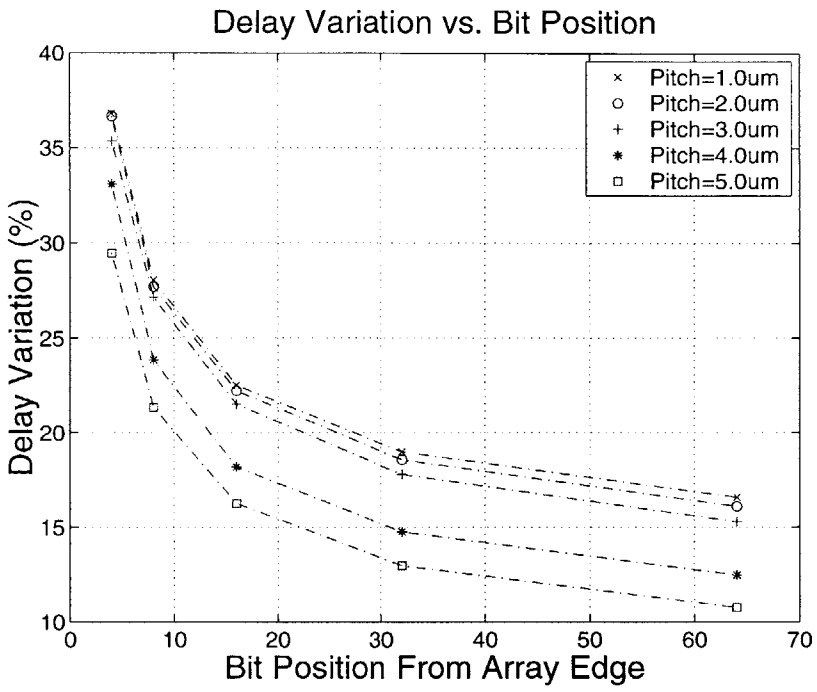

Figure 4-5: Effects of Cu CMP on Bus Delay

The effects of Cu CMP on metal thickness in the interconnect are modeled similarly as before. The effects of poly critical dimension variation are modeled under the assumption that a pattern dependent model captures the systematic variation. We further assume that the underlying poly density varies in large areas on the chip (as in dense SRAM, random logic and other blocks), resulting in the variation in poly length as shown in Figure 4-7.

Spice simulations are performed on the perturbed structures (from Cu CMP and poly CD variation) using the interconnect parameters in the Table 4-1. Table 4-2 summarizes the simulation results. Without taking into consideration the effects of device variation (poly CD), it is observed that most of the clock skew stems from the asymmetry of the H tree, interconnect variation adds on a mere 6ps to the existing clock skew. However, once device variation is taken into account, clock skew increases dramatically to 83ps.

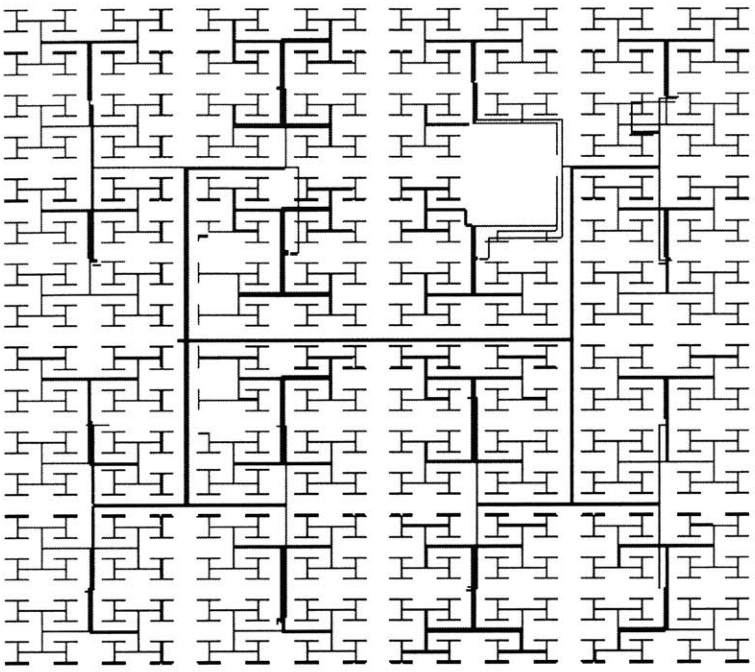

Figure 4-6: The Clock Distribution Circuit [9].

2%	**5%**
0%	**1%**

Figure 4-7: Percentage of Poly Length Variation

4.2 Comparison Between Optical and Copper Interconnect

The feasibility of optical interconnect for clocking and/or data distribution hinges on its performance with respect to various metrics of comparison. In this work, we approach the topic in light of the following:

Metal Level	Metal Thickness	ILD Thickness	Cu Resistivity
M5	1.0	0.8	35
M6	1.2	1.0	35

Table 4-1: Interconnect Parameters.

Variation Source	Maximum Clock Skew (ps)
None	34
Interconnect	40
Device	83

Table 4-2: Variation Impact on Conventional Clock Skew

- Power Requirement
- Clock Distribution
- Signal Propagation

4.2.1 Power Requirement

In implementing optical interconnects on chip, the receivers incur an area and power overhead. Thus, the optoelectronic conversion circuit designed has to be small in area and power consumptions for it to be feasible in dense optical interconnects. In order to further reduce power consumption on chip, one could transfer power consumption to the optical modules. This would mean higher optical power in the photon sources and potentially better performance as illustrated in the results presented in Tables 3-1 and 3-2.

In conventional clocking schemes, the circuit consists mostly of interconnects and buffers which require high-power clock drivers. By using optical interconnects, it might be possible to avoid building resynchronization circuits (for example, PLL and buffers). The Alpha 600MHz microprocessor uses a gridded clock hierarchy. The PLL clock signal is routed to the center of the die and is distributed by X-trees and H-trees to 16 distributed global clock drivers [1]. The global clock driver used consumes 10.2W, and the complete distribution network that is eventually driven by the global clock uses 5.8W. The optical receiver circuit designed here consumes power ranging from 11.5mW to 60mW. One could perform an optimization to obtain the number of receivers to incorporate on chip given the receiver power consumption and the

optical power consumption required for the optical distribution system. It appears, however, that substantial savings in power may be possible using optical global clock distribution.

4.2.2 Clock Distribution

Using optical interconnect for clocking distribution would be beneficial if evaluation is performed independent of the receiver circuitry. Optical signals have superior arrival time predictability and less dependence on temperature, qualities of an ideal candidate for clock distribution systems. Yet, this work reveals that the electrical circuitry has a huge impact on the overall performance.

Acceptable clock skew in the industry is usually 10% of the clock cycle. The 600MHz Alpha microprocessor has a skew target of 75ps. Simulation of the conventional clock distribution circuit used in this work [9] shows that most of the clock skew originates from the clock tree imbalance due to length variation. Cu CMP variation effects make minute contributions to the total clock skew because as the thickness of metal is reduced, there is a corresponding increase in resistance and a decrease in the lateral intra-layer coupling capacitance. Together, these result in cancellation effects. On the other hand, device (poly length) variations in the buffers have a much greater impact on clock skew. In the case of our simulations, poly length variations add around 50ps to the existing skew. Thus, copper interconnects are more affected by device variations than by Cu CMP variations.

The same trend is observed for optical interconnects. Variation in waveguides account for a mere 2ps skew. Device variations, on the other hand, have substantial impact on clock skew. For the designed baseline receiver, the variation effects are summarized in Table 4-3.

Variation Source	Percentage	Maximum Clock Skew (ps)
Waveguide	10	2
$Vt_{n,p}$	15	80
L_{poly}	15	100

Table 4-3: Variation Impact on Optical Clock Skew

These results illustrate the impact of receiver device variations on clock skew. Clearly, the baseline receiver is not sufficient to achieve the required performance. Possible improvements to the receiver to overcome some of these limitations are discussed in Chapter 6.

4.2.3 Signal Propagation

Conventional databuses suffer from cross talk due to capacitive coupling and inductance between the adjacent lines. In addition, Cu CMP variation effects result in different arrival time within the same databus array. By contrast, optical interconnect do not have such phenomenon. This is because they do not measure voltage but rather count photons. Thus, by switching to optical interconnects, one could eliminate cross talk effects in databus.

Electrical interconnects are limited by the total number of bits per second, B, of information that can flow through, approximately given by $B \approx B_o A/l^2$, with $B_o \approx 10^{16}$ for small on-chip lines and $10^{17} - 10^{18}$ for equalized lines. Since this limit is scale-invariant, exceeding it requires techniques such as repeatering, coding and multilevel modulation [18]. In using optical interconnects for routing data, the problem can be solved since they avoid the resistive loss physics that gives rise to this limit.

The above listed advantages can be realized only when we have a high performance receiver circuit. In datapaths, the overall speed of information flow (delay) is more important than that of skew; this results in different tradeoffs to be taken into consideration when designing or choosing the optimal receiver design.

Chapter 5

Implementation and Testing

A test chip was fabricated using the TMSC 0.35μm, 3 metal and 2 poly process to illustrate the concept of optical interconnect on chip. In addition to characterizing area and power requirements, the chip design also investigates the effects of variation on circuit performance. Since this is our first attempt at integrating the various components, a decision was made to omit the waveguides.

The test chip thus consists of the receiver and detector modules. The detector used is a p-i-n diode, as shown in Figure 5-1, largely chosen because it can be easily integrated on chip with current process. The diode operates in the reverse-biased region with $n+$ tied to Vdd and $p+$ tied to the input of the preamplifier. When electron-hole $(e-h)$ pairs are generated, electrons will be attracted to the $n+$ terminal and holes will be attracted to the $p+$ terminal, resulting in a current flow from $n+$ to $p+$. If there is a need to modify the current output, the $n+$ terminal can be connected to a bias voltage higher than Vdd. This results in a larger depletion region with more $e-h$ pairs collected, which increases the efficiency of the diode and thus increases the current.

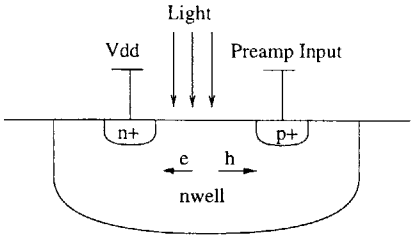

Figure 5-1: Silicon p-i-n Diode.

5.1 Physical Realization

The test chip consists of five modules, as depicted in Figure 5-2. Each module consists of a receiver circuit and a detector in its vicinity. Two identical modules, with the designed poly length of 0.35μm, are placed at the top left and bottom left corners of the chip to observe the spatial variation effects. Two other modules have intentionally introduced variation in their poly length, with 0.40μm (located at the top right corner) and 0.45μm (located at the bottom right corner) respectively. The receivers occupy an area of 150μm x 200μm each. All receiver modules have individual power supply pads for independent power supply.

The motivation behind the choice and layout of these modules is to observe the impact of variation. In this chip, we have isolated poly length variation and power supply variation, and with similar modules (the two receivers with 0.35μm poly length), we seek to demonstrate the effects of spatial variation and other manufacturing effects.

To facilitate testing, a separate receiver, the top middle block, and detector module, the right middle block, was also fabricated. The receiver module takes in direct current from the pad and the detector module has a direct analog pad for output current measurement.

The entire chip was covered with higher level metal to protect the devices from being exposed to laser pulses during testing, as this will introduce electron and hole pairs in the silicon. Due to the large capacitances at the output pads, the output clock pulses are divided down to a frequency of around 60MHz with a divide-by-16 divider.

The divider circuitries also have independent power supply pads in order to isolate the impact of power supply variation on the receiver modules.

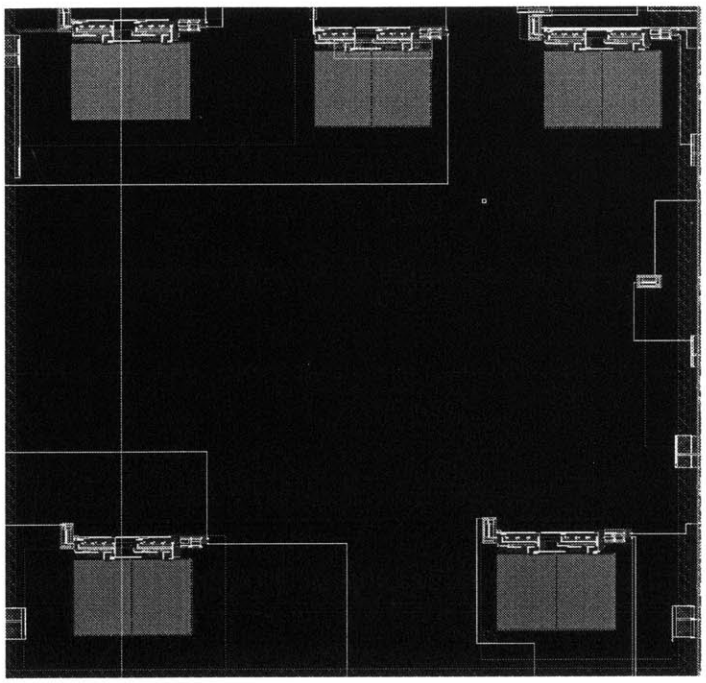

Figure 5-2: Die Picture.

5.2 Test Chip Results

Testing was performed incrementally. Initial effort was concentrated on ensuring the operationality of the detector. This phase of the testing was performed on a probe station. The unpackaged die was reverse biased and the output current was tapped from the analog pad. It was discovered that for the intended laser setup, the detector would merely produce an output current of 0.5μA, as opposed to the designed 1μA.

Several reasons account for this outcome:

1. The narrow opening of the i region in the detector

2. The combined thickness of poly and metal layers.

When designing the detector, the intrinsic region was intentionally kept as small as possible to achieve maximum speed, as shown in Figure 5-3. The side effects resulting from a small narrow intrinsic region was not taken into account of. With a small intrinsic region (smaller than half of the wavelength of the laser pulse), there will be two effects. Firstly, the total exposed area of the detector is very small and this will reduce the current generated. Secondly, there will be a diffraction effect at the opening of the detector, which is further compounded by the fact that the intrinsic region is deeply buried under various layers of material.

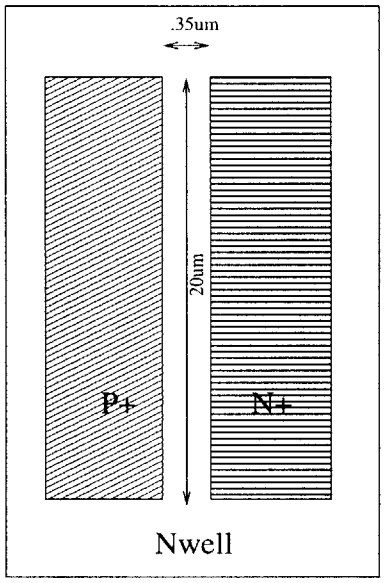

Figure 5-3: Top View of Detector.

A cross section of the device is shown in Figure 5-4. The thickness of various layers used in the process is shown in the following Table 5-1

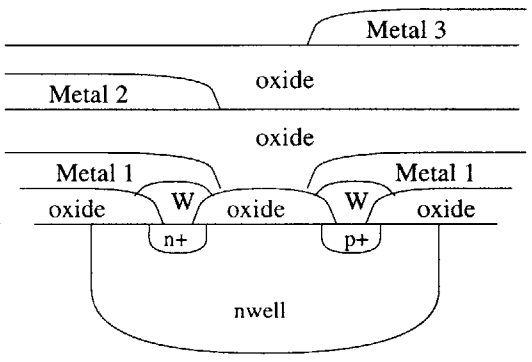

Figure 5-4: Cross Section of Detector.

Layer	Thickness (A)
Poly1	2750
Poly2	1800
Metal1	6700
Metal2	6400
Metal3	9250

Table 5-1: Thickness of Various Layers Used in the Process

5.2.1 Possible Solutions

The following are the possible solutions to the problem.

1. Utilize a stronger laser
2. Redesign the detector
3. Enlarge the detector slit on the existing chips
4. Test the modules with a direct current input

The most obvious solution of utilizing a stronger laser or redesigning the detector would require a significant turnaround time.

Solution 3 would affect the speed of the detector because the p+ and n+ area will be exposed to the laser. The electron-hole pair generation in the p and n side will cause a change in conductivity which then broadens the current pulse and slows it down.

The last solution is testing the chip in its current condition, in which case the only module that can be tested is the receiver with a direct current input from the pad.

The solution of choice is to test the existing chip with a direct current input to the receiver module through the pad, which can be extended to testing with a off-chip detector. This is the best compromise given our time and equipment availability.

5.2.2 Testing of Receiver Module

Preliminary testing of the chip (as shown in Figure 5-5) was performed using a function generator. The chip was soldered onto an adaptor for the SSOP 28 packaging and mounted onto a prototyping board. Capacitors are connected between power and ground to reduce power supply noise. The chip is driven with a stimulus generator. Testing was conducted starting at a frequency in the low MHz range. The output of the receiver, as shown in Figure 5-6, has a swing of 3.3V observable up to 300MHz, upon which it becomes very hard to trigger. The output waveform is also observed to be very noisy at higher frequencies, as illustrated in the scope picture shown in Figure 5-7. As the frequency increases, the frequency of the output voltage gradually fails to keep up. In order for the receiver circuitry to operate at 1GHz, the input capacitance has to be kept in the range of $100fF$. Testing the receiver through direct input current results in a much higher capacitance, and thus reduces the bandwidth of the amplifier.

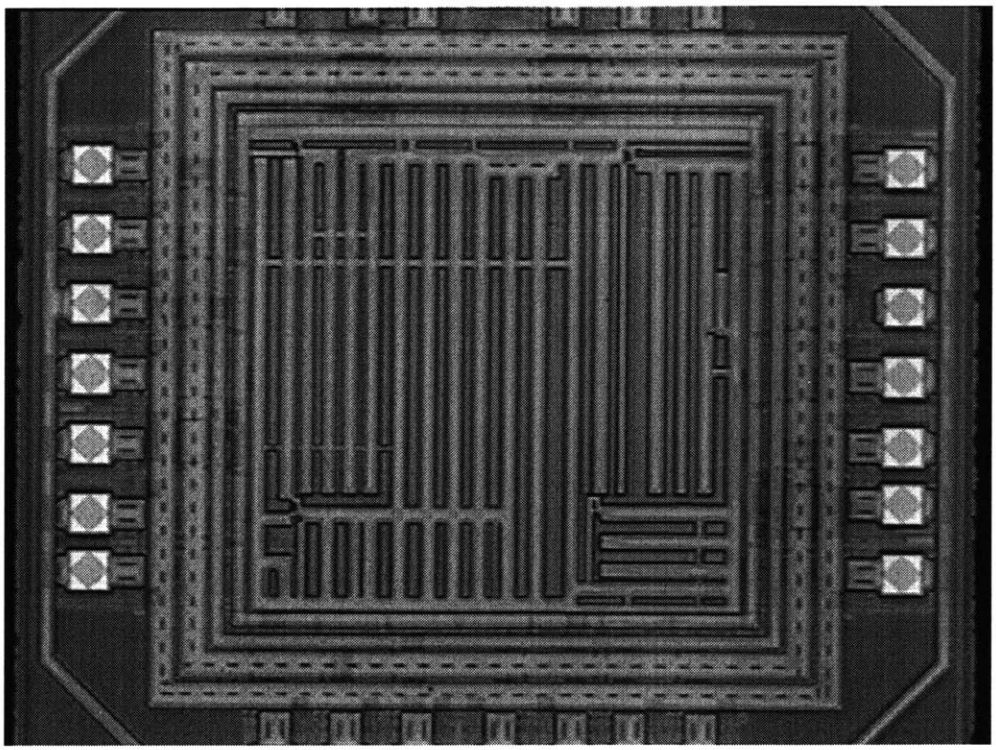

Figure 5-5: Test Chip.

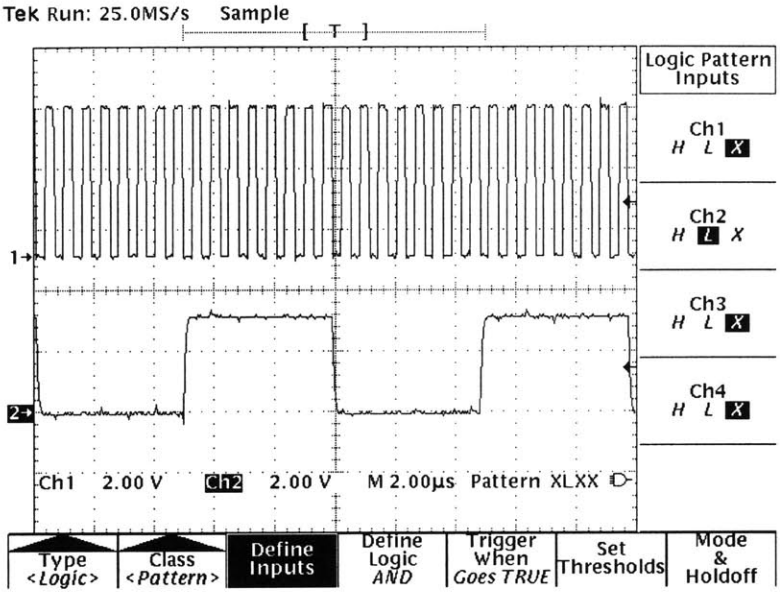

Figure 5-6: Test Chip Output Shown in the Lower Trace.

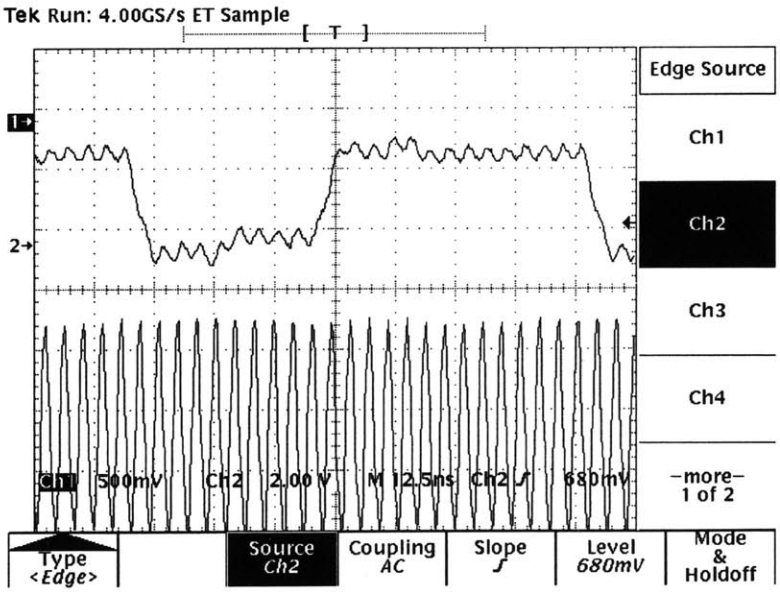

Figure 5-7: Test Chip Output Shown in the Upper Trace.

Chapter 6

Test Chip Revision

This chapter details some possible revisions to the optical receiver test chip in light of the results from this run. These suggestions improve on the apparent weaknesses of the baseline receiver circuitry and the detector.

6.1 Detector

One of the challenges in implementing a high speed monolithically integrated silicon based optical receiver is to develop a photodiode structure compatible with current fabrication processes which is capable of high speed operation with acceptable responsivity.

Planar photodiode structures for operation at 850ηm, fabricated on bulk silicon, typically attain high responsivities while sacrificing bandwidths. Schow et. al [7] have identified the weak penetration of the electric field into the silicon substrate as the cause; this is further aggravated by the long absorption length of 850ηm light in silicon. Due to the long absorption length, most of the carriers created are at depths where electric field strength yields a velocity much lower than the saturation velocity.

The low drift velocity results in these carriers being collected very slowly. Coupled with the long distance to the surface electrodes, this leads to the degradation in planar photodiode frequency response.

One option is to design a structure to eliminate the collection of the slower carriers at the expense of responsivity. Woodward et al. [28] has realized the n-well of the standard CMOS process can be used as a screening terminal in the same way as the buried collector terminal of a BiCMOS process. The screening terminal collects most of the slowly diffusing carriers and screens it from the amplifier, resulting in a high response speed. The n-well of a standard CMOS process is held at a fixed potential while the intrawell p-diffusions define the active contact of the detector. This terminal is connected to the input of a CMOS multistage receiver. A cross sectional view of the design is in Figure 6-1. The n-well region in which the detector resides is surrounded by a grounded p^+ guard ring. Inside the n-well an interdigitated network of p^+ source-drain material forms the active terminal of the detector. The n-well is tied to the detector bias and is intended to screen the active terminal from the slowly responding bulk-generated carriers. The designed detector has a low dark current, remaining below 1nA to 9V reverse bias and a capacitance of $100fF$ [28].

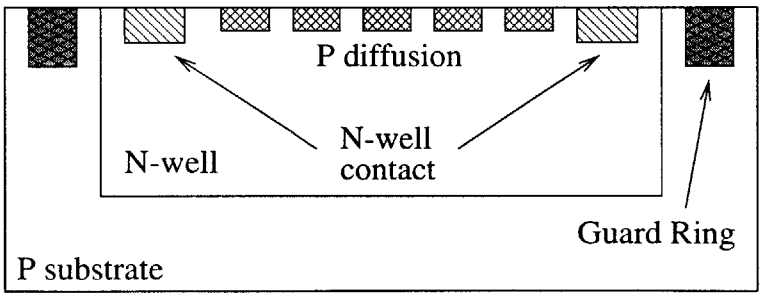

Figure 6-1: Cross Sectional View of Detector.

Other options will be to introduce process modifications at the expense of economy tradeoffs. An effective solution to the diffusive carrier transport problem can be obtained by using low-doped substrate materials as the starting point for the electronics. One could also use a twin-tub CMOS process. Devices can be created in the thick epitaxial layer, which is a ready-made low-doped region [29]. Figure 6-2 illustrates a

cross section of the p-i-n diode. The highly doped n^+ substrate would serve as the cathode while the epitaxial layer would serve as the intrinsic layer and the p^+ region would be used as the anode.

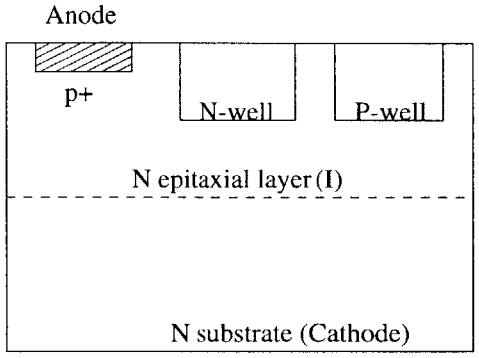

Figure 6-2: Cross Sectional View of Twin Tub Detector.

6.2 Receiver Module

6.2.1 Power Supply Sensitivity

Power-supply noise perturbs analog circuitry in various ways. The most common way is the induced ripple which affects circuits with high power supply sensitivity. The current flowing in the substrate also creates voltage gradients in the substrate, resulting in modulated threshold voltages of MOS devices. To alleviate the problem of power supply sensitivity, a linear regulator can be implemented on chip [10].

6.2.2 Receiver Circuit Topology

The baseline receiver circuitry used in this work has limited immunity against process variations and noise. In order to achieve better performance, one could use an automatic offset correcting circuit to compensate for the threshold voltage fluctuation, and substrate noise between the analog and digital parts can be addressed by implementing a design that is less sensitive to noise.

Substrate cross talk noise is easily transmitted because of the small substrate resistance and large junction capacitance of the device. Cross talk sensitivity, defined as cross talk gain over signal gain, is proportional to drain capacitance and inversely proportional to the transconductance, *gm*. Thus, increasing *gm* and decreasing drain capacitance will result in less cross talk noise. Cross talk noise particularly affects the preamplifier because the input signal is low. The configuration shown in Figure 6-3 used for the preamplifier has a large drain capacitance and low transconductance. A modified configuration shown in Figure 6-4 is superior because it will have less drain capacitance and higher transconductance [5]. This circuit is also less sensitive to threshold voltage variation because the source-follower transistor has been eliminated. This configuration can also be implemented as a differential ended circuit, as a symmetrical configuration would be highly immune to substrate noise and power supply modulation.

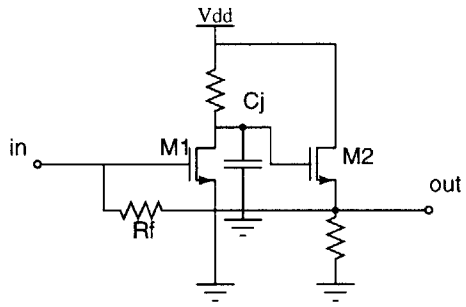

Figure 6-3: Conventional Preamplifier Configurations.

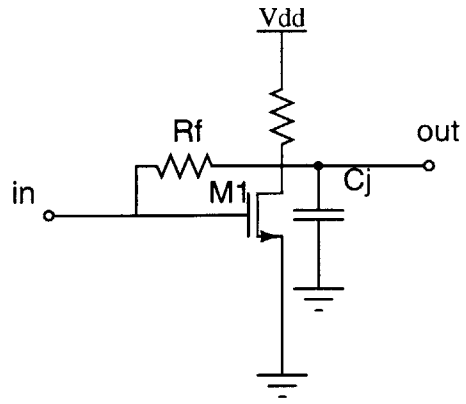

Figure 6-4: Modified Preamplifier Configurations.

In order to further limit the effects of threshold voltage fluctuation, one can implement adjustment circuitries (if used) less sensitive to threshold voltage variation. Circuitries can also compensate for the offset current from the photodetector. An example of an adjustment circuit is the variable-gain control amplifier shown in Figure 6-5. This circuit is less sensitive to threshold voltage fluctuation because the gain is controlled by only one transistor. To correct the offset current from the photodetector, one can implement a simple offset control circuit based on a current mirror configuration as shown in Figure 6-6.

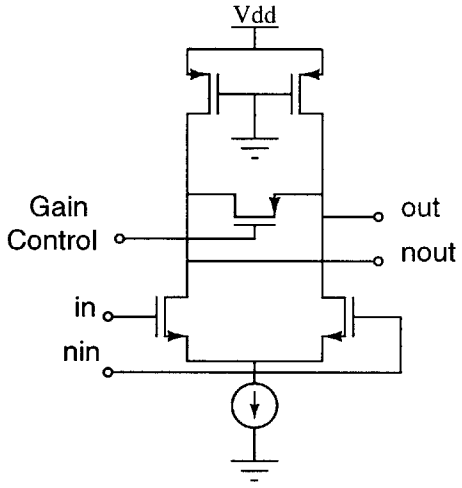

Figure 6-5: Automatic Gain Control Circuit.

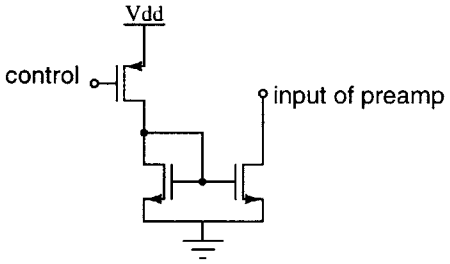

Figure 6-6: Offset Circuit.

Some other techniques used to reduce the effects of threshold voltage and poly length variations include the following:

- Keeping a constant channel length and width for matching purposes. In cases where one needs to have different sizing ratios, the width should be the only

variable. Also, larger device sizes will be better for matching purposes.

- Keeping matching devices close together on the chip.
- Using a common centroid, cross quad layout to help alleviate lateral variations in oxide thickness.
- Keeping the same current flow direction in the layout. The slanted source and drain implantation results in different dimensions in the source and drain; in order to get the same current, the flow direction must be the same.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

This work has revealed heavy performance dependency on optoelectronic circuits when attempting to integrate optics on chip. Evaluation of optical performance independent of receivers has been undertaken by many and the benefits are self evident in terms of frequency enhancement, accurate arrival time, and absence of induced cross talk. However, in taking into consideration the receiver circuitry, the challenges of integration become more complex.

7.1.1 Optoelectronic Circuitry

In order for optical interconnects to be implemented with superior performance, the corresponding optoelectronic circuitry requires low power dissipation, small area consumption and high resistance to variations. This work reveals that most of the clock skew and delay effects on the baseline receiver are caused by device variations and environmental variations. More research has to be conducted in the area of circuit

techniques to develop new designs more resilient to effects of variation. Chapter 6 mentions some possible methods to reduce effects of threshold variation, poly length variation and receiver cross talk effects. It is essential to evaluate optical interconnect as a system, and not as individual modules of optics, waveguides and circuits.

7.1.2 Detectors

Coupled with the above problem is the challenge of integrating photodetectors on chip. In order to avoid a complex receiver design with high sensitivity, detectors need to have a small capacitance and large responsitivity which will lead to better noise immunity and fewer gain stages.

A silicon-based detector is not the prime choice due to its long absorption length. This in turn results in low diode efficiency and long tails in the detector response time. The previous chapter details some possible solutions, but these solutions can only address the problem partially.

Other options include using quantum well modulators and VCSELs. Quantum well modulators require an external beam to be brought onto the modulator but have been successfully made in large arrays that have been solder bonded to the circuits. VCSELs, on the other hand, are less well understood, even though substantial research work has been conducted in recent years [6].

7.2 Future Work

In light of our results, future work can be implemented in areas such as the circuitry, the optoelectronic device, integration and variation effects .

7.2.1 Optoelectronic Circuitry

Various improvements can be made in the receiver circuitry, some mentioned in Chapter 6. It is invaluable to understand how far one can push the limits of current and future circuit technology in terms of power, area, noise immunity, crosstalk, and variation. One other alternative would be to investigate direct conversion schemes such that optical interconnects can run receiver-less.

7.2.2 Optoelectronic Devices

A redesign of the silicon detector is required. Also, it would be beneficial to look into using VSCELs and quantum well modulators as optoelectronic output devices.

7.2.3 Integration

There are two aspects of integration to be looked into, one being incorporating waveguides, silicon detector and receivers on chip, the other being incorporating VCSEL arrays on chip together with the receivers. However, testing procedures need to be thought through carefully before implementation.

7.2.4 Variation Analysis

The variation analysis performed in this work merely gives an overall picture to the effects that variation has on the overall performance of optical systems. Substantial work is required to model the variation effects in greater detail.

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