INTEGRATED SILICON PRESSURE SENSORS USING WAFER BONDING TECHNOLOGY

by

Lalitha Parameswaran

B.Eng., Carleton University (1990)
S.M., Massachusetts Institute of Technology (1993)

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 1997

Author .....
Department of Electrical Engineering and Computer Science
April 12, 1997

Certified by 4/17/97
Martin A. Schmidt
Associate Professor, Department of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Departmental Committee on Graduate Students

Integrated Silicon Pressure Sensors using Wafer Bonding Technology

by

Lalitha Parameswaran

Submitted to the Department of Electrical Engineering and Computer Science
on April 14, 1997, in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

ABSTRACT

Many electronic devices interact with the external world through sensors and actuators. The widespread use of such devices has fueled the interest in designing "smart" sensors with signal processing circuitry incorporated with the basic sensor or actuator. This thesis describes the development of a process for the fabrication of integrated microelectromechanical devices using single crystal silicon as the mechanical material, referred to as the MEMSCMOS process. It enables the formation of a variety of mechanical structures, including those using capacitive detection which often require on-chip amplification to minimize stray capacitance.

The integrated MEMSCMOS process is partitioned into three sections: front-end micromachining, integrated circuit formation, and back-end micromachining. Front-end micromachining consists of using silicon wafer bonding to make a sealed cavity microstructure that is the base element of the transducer. Back-end micromachining steps consist of release etches from the front and backside of the wafer to form surface and bulk-micromachining-like structures respectively, and the formation of a top capacitive electrode. To ensure that the sealed cavity plate can withstand the high temperature thermal cycles typically seen in IC fabrication, it is formed by wafer bonding in a controlled ambient to achieve a reduced gas pressure inside the cavity. A model of the sealed cavity was developed to determine geometries and bonding conditions necessary to avoid plastic deformation. Plates with unconstrained as well as constrained downward deflections were considered in the model, which was incorporated into a simulation program to predict the onset temperature of plastic deformation for any square or circular cavity. The model was experimentally verified by means of defect studies on sealed cavity plates undergoing various high temperature anneals.

The feasibility of the MEMSCMOS process was demonstrated with the fabrication of a testchip containing a variety of electrical and mechanical test structures, all of which were successfully operated confirming that there was minimal impact on device performance as a result of the merged process steps. The mechanical test structures incorporated both surface and bulk-micromachining-like devices, none of which showed any evidence of plastic deformation. The process was also transferred to a commercial production facility at Motorola. A capacitive pressure sensor was fabricated and tested in two modes of operation, conventional and touchmode. It was also combined and tested with a sensing and calibration circuit in two forms, hybrid and integrated. Discrete devices were combined with a separate sensing chip in a hybrid package, and an integrated sensor-circuit chip exercising the complete MEMSCMOS process was also fabricated.

Thesis Supervisor: Martin A. Schmidt
Title: Associate Professor, Department of Electrical Engineering and Computer Science

ॐ

Acknowledgements

The long and sometimes arduous course of graduate studies requires the involvement of many people to come to successful completion. I would first and foremost like to thank my advisor, Professor Martin Schmidt, for providing guidance, support and a fount of knowledge for me to rely on. It was truly a pleasure and privilege to work in his group. I would also like to acknowledge the other members of my committee, Professors Charles Sodini and Hae-Seung Lee for their suggestions and comments, as well as Professor Stephen Senturia who was kind enough to do a critical reading of my thesis on somewhat short notice.

I was fortunate to be associated with a wonderful group of people in the Schmidt Group both past and present, including Errol Arkilic, Arturo Ayon, Ted Bloomstein, Roberto Devoto, Samara Firebaugh, Howard Goldberg, Charles Hsu, Michael Huff, CC Lin, Vince McNeil, Aravind Padmanabhan, Mark Sheplak, Ravi Srinivasan, Joel Voldman and Jo-ey Wong. Because they were and are involved in a wide spectrum of projects, I benefitted greatly from their collective knowledge, as well as the breadth of discussion topics of both a technical and more casual bent. I'd like to thank Charles in particular for the joint work we did in process development and other collaborative work. I would also like to thank Jennifer Lloyd, who spent much effort in redesigning her circuit to operate in conjunction with my sensor, as well as for providing some of the final test data. I think they, along with all the other students in the Microsystems Technology Labs that I've come to know, are one of the nicest groups of people I've had the chance to work with and I wish them the very best in all of their endeavours.

I owe a great deal of gratitude to the staff of the MTL for all of their assistance and support in the cleanrooms, which was invaluable. Thanks also go to David Breslau in the Center for Space Research for his help in device packaging, and our administrative assistant Pat Varley for keeping the office running smoothly.

The majority of this work was supported by the Semiconductor Research Corporation under contracts 92-SC-309 to 96-SC-309. Through the SRC I had the opportunity to spend some time at Motorola Semiconductor Products Sector in Phoenix during summer internships. In addition to experiencing the joys of an Arizona summer ("but it's a *Dry* heat!"), I got to work with a great group of people and in particular would like to mention Dr.Andy Mirza and Wendy Chan in the Sensor Products Group, and Dr.David Bosch, Dr.Frank Secco d'Aragona and the staff of the Direct Wafer Bond Group for all of their help. A good portion of this work was done in their facilities, as well as a fair amount of "remote" processing when I was back at MIT.

Finally, I thank my parents and brother for all of their love, support and confidence in me. I couldn't have done it without them.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Microelectronic devices are ubiquitous in modern life, with some manner of electronic interface being found in virtually every environment, to control and enhance the performance of equipment of all varieties. Most if not all of these items interact in some way with the outside world, through sensors to convey input to the machine's controller and actuators which provide output to act on the external world, both of which can be categorized generally as transducers. The group of solid state transducers encompass such devices as piezoelectric quartz sensors, platinum RTDs, metal oxide gas and humidity sensors, and strain gauges, to name a few. The subset of semiconductor-based transducers has drawn much attention in recent years and has come to be known generally as MEMS (microelectromechanical systems). MEMS encompass sensors, actuators, and electronics that interface with the physical world by converting physical stimuli from the mechanical, thermal, chemical and optical domains to the electrical domain. There has been a tremendous amount of research and development in microelectronics technology, much of which is being assimilated and used to develop and increase the capabilities of MEMS. It is logical to utilize this technological base to fabricate sensors and actuators, thereby taking advantage of the sophisticated batch fabrication and production methods used in a modern integrated circuit (IC) foundry. Working from the vast knowledge base accumulated over decades of silicon process development supplemented by specialized lithography, deposition and etching techniques, a range of structures has been designed and fabricated. New innovations in process technology and modelling have been developed to meet the needs of a wide variety of transducer applications, ranging from simple pressure sensors and nozzles for printers, to displays, inertial sensors, and actuators for optical alignment, and complex flow systems for chemical and biomedical applications. The development of microscale mechanical

devices was predicted as far back as 1959 by Feynman [1] and MEMS devices had expanded to encompass varied applications by the time a review paper by Petersen was published in 1982 [2], summarizing the state of the art at the time. Since that paper, the next logical step of merging micromechanical devices with the circuit world has been tackled with varying degrees of success.

Since the bulk of solid state electronics is made from silicon, it is natural to consider this as raw material for transducers also. Silicon exhibits a number of transduction effects, such as piezoresistivity, magnetoresistivity, photoconductivity and thermoresistivity [3], all of which are exploited in various sensors. In addition, it is an excellent mechanical material, having high modulus, hardness and strength (3 times that of stainless steel), and with appropriate surface finishing, a high fatigue strength. Perhaps most importantly, it can be manipulated into a variety of shapes through the use of the same lithography and etching tools used to fabricate integrated circuits, as will be described in subsequent sections.

1.1 Integrated sensor technologies

This section reviews some of the current approaches being developed to achieve sensor-circuit on-chip integration. Since separate optimization of both sensor and circuit would be ideal, a decision must be made as to the order of fabrication of each of the two types of devices. Practically speaking, this leaves three choices: micromachining first, circuits first, and a partitioned approach. In addition, a choice is also made as to the micromachining toolset to be used, usually one of surface micromachining, bulk micromachining, wafer bonding, or dissolved wafer processes. The following sections give examples of each of these categories.

The most commercially sucessful approach so far has been the circuits-first approach, as embodied by currently available conventional bulk and surface micromachined devices. This consists of fabrication of the integrated circuit on the substrate and passivation of the circuit, followed by micromachining steps, usually some form of etch to remove material, and finally with dicing and packaging. The basic bulk micromachined device, as exemplified by a pressure sensor, consists of a silicon diaphragm formed by anisotropic wet etching, around which is placed signal conditioning circuitry (fig. 1-1a) [4]. This highly successful technique relies on its simplicity, limiting the micro-

machining to one final (wet) etch to define the membrane. This etch step can be a simple as a timed etch (poor thickness control) but more commonly employs some form of etchstop such as a buried p++ layer, buried oxide or electrochemical etch. The membrane material need not be limited to silicon but can be any other deposited film with good etch resistance as compared to silicon, such as silicon dioxide or nitride, or even a metal layer. One of the drawbacks to this method is that it produces a low device density, since the size of the opening on the back of the wafer is much larger than the sensor as a result of the anisotropic nature of the etch. With the progression to larger diameter (and thicker) wafers, this problem can only become worse. Thickness control of the membrane is also an issue, and has been resolved with the development of etchstop techniques such as those mentioned above.

An alternative bulk micromachining process that alleviates the density issue is that of performing the final silicon removal on the front of the wafer, after encapsulating the structure in layers of a suitable masking material (fig. 1-1b) [5, 6]. The silicon etch is done with a conventional anisotropic etchant such as ethylene-diamine pyrocatechol (EDP), potassium hydroxide (KOH) or tetramethyl ammonium hydroxide (TMAH). With appropriate passivation layers and/or the use of silicon-doped TMAH as the etchant (see sec. 3.3.1), this can be done as a maskless step. This method is particularly appealing for devices that require thermal isolation as evidenced by its use in infrared sensors and thermopiles; however it is not as suitable for mechanical sensors since they would consist of layers of different films, with associated stress issues. This process has been standardized so that the circuits and structural layers can be fabricated in a commercial foundry, and the final release etch is the only step that is done by the micromachinist.

Conventional surface micromachined integrated sensors are also circuit-first processes, where after circuit fabrication, a succession of structural and sacrificial layers (usually polysilicon and silicon dioxide) are deposited and patterned. The final step is a wet release (usually using hydrofluoric acid) to remove the sacrificial layers. Key concerns which have been addressed in making this technology viable are the elimination of stiction between the structural layer and the substrate during the wet release [7, 8], control of the mechanical properties of the thin film structural layer [9] with post-circuit annealing, and the use of high temperature (tungsten) metallization for the circuitry [10] to accomodate such anneals. Many of these issues have been resolved to the extent that the technology is currently being used in an integrated capacitive accelerometer [11] with

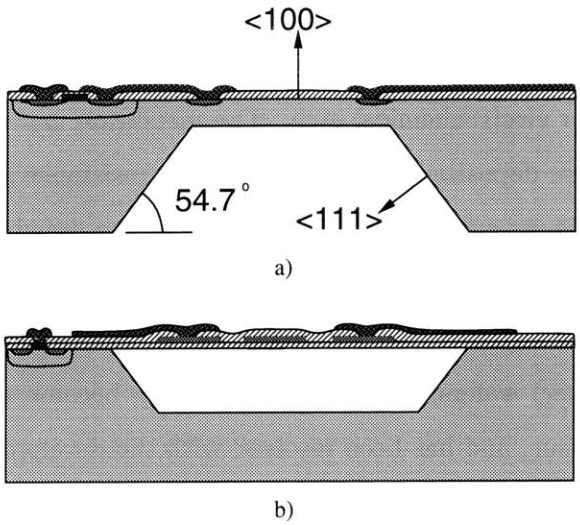


Figure 1-1: Bulk micromachined pressure sensor. a)Traditional backside etching b)Frontside bulk etching using TMAH.

extensive signal conditioning. It is also available as a foundry-based service [12], with a fairly well-established set of design rules within which the designer can construct any structure that can be defined by a mask. While this technique is fairly widely used, it is difficult to make high aspect ratio structures as they require thick film depositions. In addition, control of the structural properties of the thin film(s) is extremely important and somewhat difficult to control from run to run.

Silicon-on-insulator (SOI) substrates can also be used to make single crystal silicon surface micromachined devices, by treating the buried oxide layer as the sacrificial layer. This has been done to make an accelerometer [13] with a BESOI (bond-etchback SOI) wafer and a microphone [14] with a SIMOX (separation by implantation of oxygen) wafer. Pressure sensors have also been made by growing epitaxial silicon on top of the SIMOX silicon layer, after which the buried oxide is removed [15].

The micromachining-first approach has not been commonly used as it involves fabricating the mechanical element first, which must then withstand the integrated circuit process intact. Since many of these elements are suspended structures made of thin films with temperature sensitive properties, some means of protection must be afforded the devices if this method is to succeed. Therefore, an interleaved approach is preferred, where the micromechanical element is partially fabricated, stabilized in some manner to protect it during the circuit process, and then exposed at

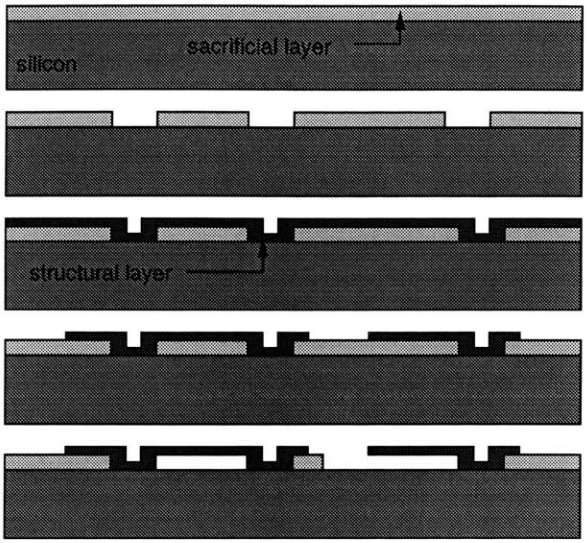


Figure 1-2: Surface micromachining.

the end of the process. Recently, Sandia Labs has developed such a process utilizing polysilicon as the structural element [16]. The polysilicon structures are formed in a trench initially etched in the starting substrate, after which they are completely embedded in a deposited oxide which fills the trench. The oxide is planarized with chemical-mechanical polishing (CMP) and sealed with a silicon nitride cap, and CMOS processing then proceeds. The polysilicon is released at the end with a conventional wet sacrificial oxide etch. This technique offers the advantages of process modularity but requires CMP, as well as having the same release and thin film control issues of conventional surface micromachining.

The dissolved wafer process is another example of a mixed approach in which the structural regions are defined with the formation of recessed areas and p++ diffusions. The wafer is then anodically bonded to a glass substrate and etched in an anisotropic etchant with a high selectivity to p++ silicon to dissolve the lightly doped remainder of the wafer, leaving the heavily doped regions bonded to the glass (fig 1-3). In order to be able to incorporate circuitry into such devices, an active-dissolved wafer process has been designed, using electrochemistry to protect selective lightly doped areas of the silicon substrate during the bulk removal step. These areas contain the circuits as well as some additional resistors to assist in the electrochemical etch. This process has been used to make accelerometers integrated with CMOS opamps [17].

Other techniques used in conjuction with those previously described to achieve integration include

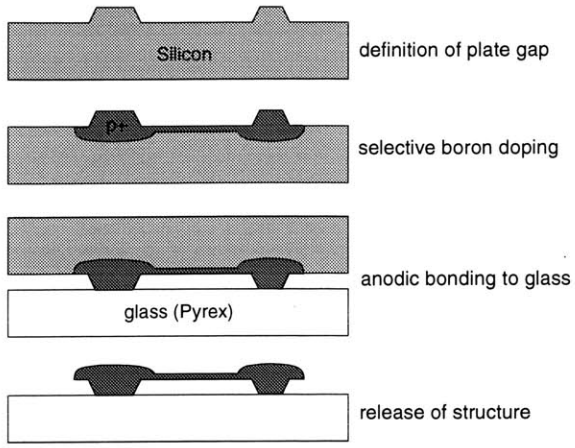


Figure 1-3: Dissolved wafer process.

LIGA [18], which can be considered to be a circuits-first technique where metal layers are plated onto wafers patterned with very thick photoresist layers for the construction of thick-film metal structures such as inductors, and epitaxial lateral overgrowth (ELO) [19], which involves the growth of single crystal silicon on top of dielectrics by using exposed silicon surfaces as seed areas. ELO has been used to make thick dielectrically isolated structures with very little stress-related warpage since the mechanical material is single crystal silicon. However as the growth is fairly slow, this method may not be suitable for the formation of large solid plates. Another post-circuits technique is the SCREAM process [20] developed at Cornell, which utilizes a series of reactive ion etches and plasma-enhanced CVD film depositions to define high aspect ratio suspended single crystal silicon structures such as beams and lateral capacitors.

In order to be able to combine the advantages of bulk micromachining (single-crystal structural material) and surface micromachining (small structures), silicon wafer bonding can be utilized. In this case a thin silicon layer is added to a base substrate with predefined cavities. Therefore no wet release to remove sacrificial material is required, and the suspended layer can be as thin as $<1\mu$m or as thick as a full wafer. In addition, annealing is not necessary for stress relief of the thin film, and since the substrate and film material are identical, there is no mismatch in thermal coefficients to consider.

The basic wafer bonding process consists of the hydration, contacting and annealing of two polished silicon surfaces, one or both of which may be covered with a layer of silicon dioxide. Hydration involves the creation of hydroxyl groups on the wafer surface, by means of an immersion in

H_2SO_4:H_2O_2, nitric acid, or with a conventional RCA clean [21]. When the hydrated surfaces are placed in contact, hydrogen bonds are initiated and are sufficient to hold the wafers together until they are subjected to a high temperature anneal. During this anneal a number of transitions occur as the temperature is raised. At temperatures of 200-700°C the hydroxyl groups are converted to water molecules which then dissociate, allowing the oxygen to bond to the silicon while the hydrogen diffuses through the wafer. At higher temperatures the oxygen diffuses into the lattice, and silicon atoms fill in any surface roughness through diffusion. The mechanisms of bonding, as well as studies of the bond interface, are explained in detail in [22, 23, 24]. After the anneal, the bond interface is virtually indistinguishable from the bulk of the silicon, and bond strength measurements have indicated that the strength approaches the fracture strength of single crystal silicon. Although high temperatures are generally required for maximum bond strength, it is possible to achieve acceptable bond strength at anneal temperatures as low as 200°C [25].

Silicon wafer bonding was developed in the 1960s [26], and re-emerged as a viable and useful technology in 1985 with its use in the fabrication of substrates for silicon-on-insulator substrates [27] and as a substitute for thick epitaxial layer growth for power devices [28]. It was quickly recognized as a valuable addition to the micromachining toolset and was used to make pressure sensors with high temperature stability [29]. In the past 10 years wafer bonding has been used to fabricate a range of transducers, including piezoresistive pressure sensors [29, 30], accelerometers[31], valves[32], and shear stress sensors[33]. The availability of new plasma etchers that enable the formation of deep high aspect ratio trenches has expanded the range of devices that can be fabricated. Other materials have also been bonded, including silicon nitride, deposited oxides, and compound semiconductors [34].

In addition to silicon wafer bonding, there are a number of other bonding techniques that are frequently utilized. These include anodic, adhesive, eutectic and thermocompression bonding, of which the latter will be described in chapter 3. Anodic bonding is used to attach sodium containing glasses to semiconducting substates and consists of contacting the surfaces to be bonded and applying a negative voltage to the glass with respect to the silicon, creating a high field at the interface. As with fusion bonding, heating of the substrates will complete the bonding mechanism, and the field aids in the process by providing an attractive force sufficient to pull the surfaces together, so that the surface smoothness is not as stringent as for the high temperature bond.

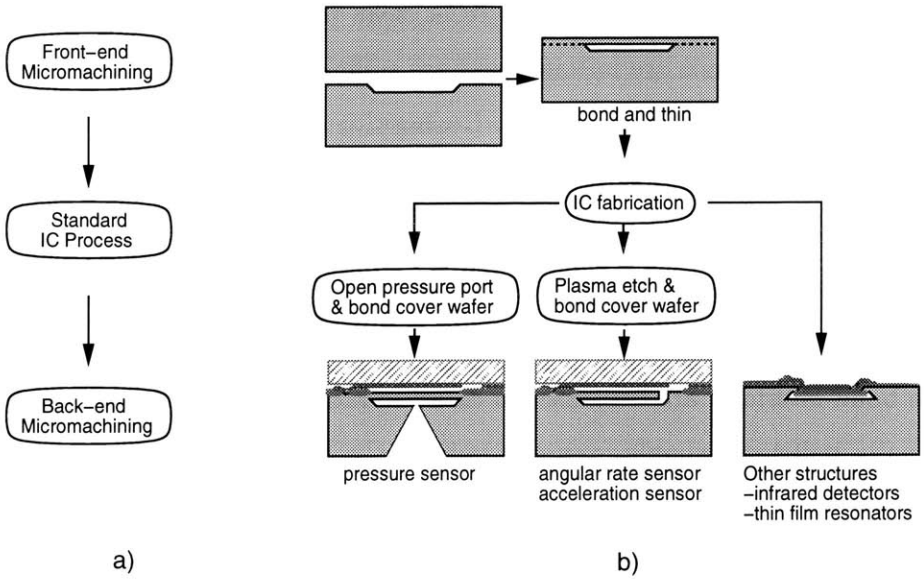


Figure 1-4: a) Partitioning of process b) Generalized sealed cavity approach

Packaging of the sensors usually utilizes anodic bonding for attachment of glass base layers to the sensor chip, and the glass of choice is generally Corning 7740 Pyrex as it has a coefficient of thermal expansion that is fairly close to that of silicon. Recently other glasses are also being designed with better thermal matching [35].

Adhesive bonding, as the name suggests, incorporates an intermediate glue layer such as epoxy or some form of low reflow temperature deposited glass. The eutectic bond uses the fusion of metal and semiconductor at the eutectic of the two materials to create a bond. Both of these are generally found as back-end or packaging functions. A comprehensive review of these and other bonding techniques is given in [36].

The integrated circuit process proposed in this thesis utilizes silicon wafer bonding and various etching methods to fabricate sensors, as illustrated in figure 1-4. The details of this MEMSCMOS process are given in chapter 3, and its central element is the sealed cavity with a suspended single crystal silicon plate which will be used to make the sensor/actuator element. The cavity has been designed to be robust enough to withstand conventional circuit fabrication, and the process is versatile enough to be used to make a wide variety of devices, ranging from pressure and acceleration sensors to thin film resonators [37] and infrared detectors [38].

1.2 Pressure sensors

The pressure sensor is by far the most commercially successful micromachined device and is available in two main categories - piezoresistive and capacitive, both of which rely on the deformation of a plate or membrane to produce an electrical signal change.

One of the first semiconductor pressure sensors was a piezoresistive diffused diaphragm sensor [39]. This sensor relies on a resistance change induced by a displacement causing strain, through the piezoresistive property of the semiconductor. This is a direct extension of the solid state strain gauges currently being widely used, where the strain-sensitive resistive element is a diffused resistor on a membrane or plate. The gauge factor is a measure of the efficiency of the piezoresistance effect and is a function of both the geometry and the strain dependence of the resistivity of the piezoresistor. The gauge factor depends on the dopant type and level, and is highly sensitive to temperature, so that some form of temperature compensation is almost always incorporated with the sensor. The temperature coefficient (TC) can be reduced by using doped polycrystalline or amorphous films instead of monocrystalline silicon, but with an accompanying reduction in gauge factor ([3]p.113). This reduction in TC can also be achieved in single crystal silicon by selecting an appropriate dopant level. In addition, the resistor placement is crucial as the maximum stress in a thin plate is highly localized to the edge of the plate whereas the resistor has a finite size limited by lithography so that stress averaging effects can reduce sensitivity significantly.

Capacitive pressure sensors rely on the modulation of a gap to provide the change in signal, and therefore the stress in the plate is not a primary concern. This immediately gives the advantage over the piezoresisive sensor of higher intrinsic sensitivity [40] (10-20 times the piezoresistance effect) and lower temperature sensitivity. The devices also have lower power consumption. However the response is highly nonlinear as compared to piezoresistance. Since the capacitance of the sensor is directly related to its size and micromachining is used to scale down device sizes, the critical constraint for micromachined capacitive sensors is the low signal level. A stray capacitance equal to or larger than the sensor capacitance can overwhelm the signal. This is one of the reasons that capacitive devices have not gained the commercial acceptance that piezoresistive sensors enjoy until the advent of technologies that enable the incorporation of on-chip amplification and noise suppression. In terms of processing challenges, although lateral alignment of features is not as

crucial as for piezoresistive devices (resistor placement to minimize stress averaging), maintenance of a precisely known vertical gap is of great importance.

Although the vast majority of devices fall into the piezoresistive and capacitive categories, there are other pressure sensing schemes also in use. Pressure measurements with micromachined devices have been taken using thermal effects as in the CMOS surface micromachined thermal sensor described in [41], where the heat transfer across an air gap between a heat source and sink is pressure dependent. Optical pressure sensors have been fabricated using antiresonant reflecting optical waveguides (ARROW) and cavity modulation by means of a diaphragm deflecting with pressure [42]. Resonant beams have also been utilized as pressure transducers [43], in which a beam optically excited into resonance exhibits a change in resonant frequency with pressure. For acoustic vibration sensing, piezoelectric materials such as ZnO, PZT and AlN have been deposited on membranes [44], and high temperature applications make use of diamond and SiC as the material of choice for the membrane.

As previously mentioned, the small size of micromachined capacitive sensors and the large parasitics surrounding them is incentive to develop methods of incorporating signal conditioning electronics on chip, and recently several of these sensors have been fabricated, using many of the techniques listed in section 1.1. One of these is an integrated capacitive sensing array using polysilicon movable plates and conventional surface micromachining techniques with a vacuum CVD oxide deposition to seal the gap after the wet release [45]. Another surface micromachined device incorporates a backside etch stopping on a buried p++ layer which is subsequently removed [46]. The movable bottom plate is the remaining silicon whereas the top plate is polysilicon and the gap is defined with a wet etch of the spacer oxide. The dissolved wafer process has also been used to make a capacitive sensor array for barometric pressures [47]. The devices operate in touch mode and are sized to switch in sequence as the pressure is varied.

The sensor developed in this work is illustrated in figure 1-5. It consists of a deformable single crystal silicon plate and a stationary metal plate on a (glass) capping wafer. Contact to the bottom plate is made by means of a diffusion on the surface whereas the top plate is accessed via a metal thermocompression bond. The rigid capping wafer and the cavity under the silicon plate supply overpressure protection, and the pressure is applied on the back of the chip, thereby providing a

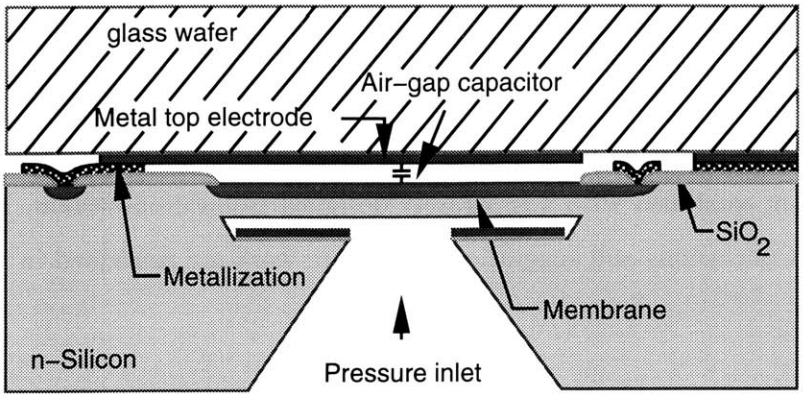


Figure 1-5: Capacitive pressure sensor.

degree of isolation from the medium. The pressure range is essentially "mask programmable" by plate diameter, provided that the plate dimensions are properly designed to survive high temperature process steps (see chapter 4). Both reference and sense capacitors can be simultaneously fabricated and the devices can be integrated with on-chip electronics, as well as with other suspended microstructures like accelerometers. In addition, if capacitive sensing is not desirable the process can be used in conjuntion with many of the other sensing schemes listed previously since almost all of them incorporate a plate or membrane as an integral element of the sensor.

1.3 Thesis outline

Chapter 1 has given an overview of current integrated sensor processes and introduced the integrated MEMSCMOS process utilizing silicon wafer bonding that is the focus of the thesis. The demonstration vehicle for the MEMSCMOS process is a capacitive pressure sensor, thus a brief discussion of the comparative merits of capacitive and piezoresistive pressure sensors has also been included. Chapter 2 gives design criteria for the capacitive pressure sensor. The complete process flow is delineated in detail in chapter 3, with descriptions of the pre and post micromachining steps required to fabricate sensors analogous to both bulk and surface micromachined devices. The plastic deformation issues that must be considered in order to obtain robust sealed cavity silicon plates are considered in chapter 4. Modelling and experimental studies of sealed cavities under high temperature steps typically seen in a CMOS process were used to develop and verify a set of design rules for cavity dimensions. Chapters 5 contains test results demonstrating the successful

implementation of the MEMSCMOS process. Both electrical and mechanical test devices were fabricated and tested with no apparent performance degradation from the added micromachining and circuit process steps. Chapter 6 contains capacitive pressure sensor test results for discrete devices and sensors combined with a separately designed calibration system, in both hybrid and integrated form. Conclusions and suggestions for future work are contained in the final chapter.

Chapter 2

Capacitive pressure sensor design

The vehicle for demonstration of the integrated sensor process is a capacitive pressure sensor; therefore this chapter contains design calculations for the sensor, in two modes of operation - normal and touchmode.

The basic element of a capacitive presssure sensor is a pair of conductive parallel plates separated by an air gap, with one plate stationary and the other plate deforming under an applied pressure, thus changing the gap. The physical structure under consideration for this work is illustrated in figure 1-5 and schematics defining the dimensions of the device are given in figure 2-1. It consists of a stationary metal top plate, a deformable single crystal silicon bottom plate clamped at its periphery, and an air gap. The surface of the silicon plate is heavily doped to serve as an electrode. The plate geometry is selected such that it will normally deform under small deflection conditions, where the center deflection w_o is less than 20% of the plate thickness h. Circular plates are used to minimize stress concentrations as well as simplify the analysis.

2.1 Static pressure response

The vertical deflection of a plate transversely loaded with a pressure q and with arbitrary boundary conditions is obtained from the solution of the general equation for the deflection of a plate in pure bending [48]:

$$\nabla^4 w = \nabla^2(\nabla^2 w) = \frac{q}{D} \tag{2.1}$$

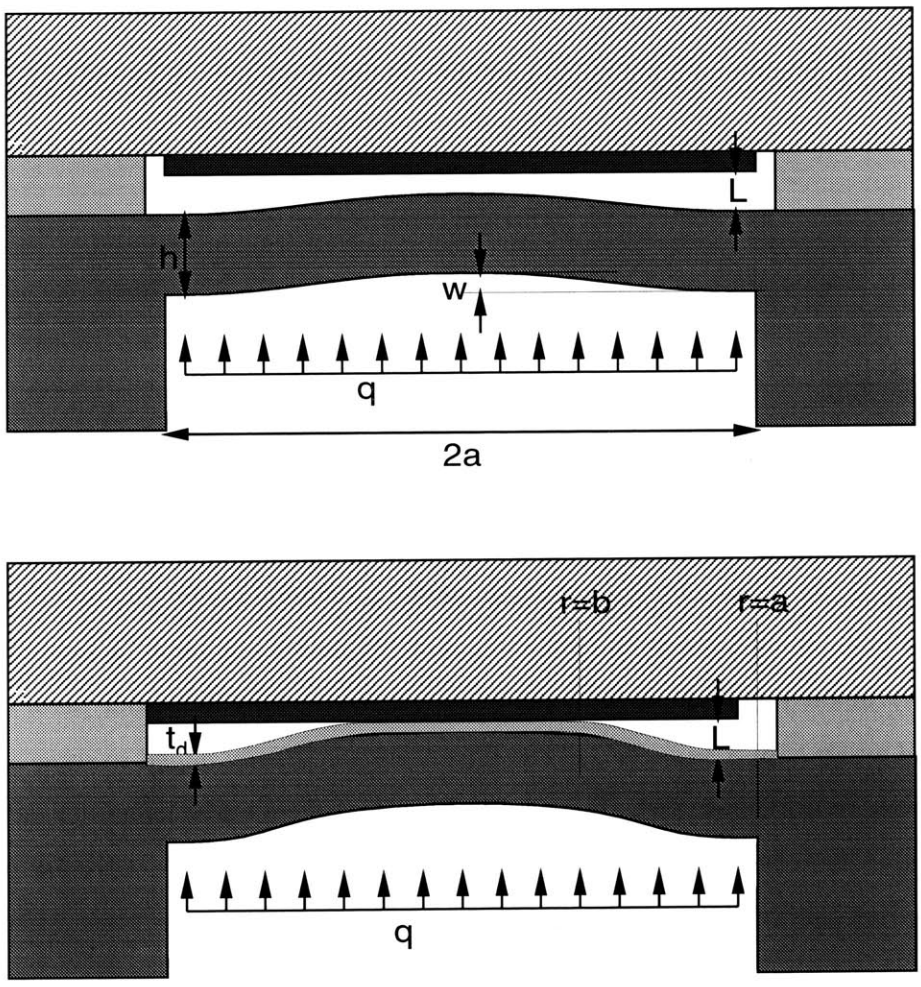


Figure 2-1: Schematic cross section of capacitive pressure sensor: a)definition of dimensions, b)dimensions for operation in touchmode.

where

$$\nabla^2 = \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right) = \left(\frac{\partial^2}{\partial r^2} + \frac{1}{r}\frac{\partial}{\partial r} + \frac{1}{r^2}\frac{\partial^2}{\partial \theta^2}\right) \tag{2.2}$$

The flexural rigidity of the plate is $D = \frac{Eh^3}{12(1-\nu^2)}$. This analysis is valid for plates in small deflection, where the deflection does not exceed a fraction of the thickness.

The capacitance of the device is obtained by integrating the gap with deflection over the area of the plate:

$$C = \int_A \frac{\epsilon_o dA}{L - w} \tag{2.3}$$

For a clamped circular plate with radius a and uniform pressure load q, the deflection is a function of the radial distance from the center of the plate:

$$\begin{aligned} w(r) &= w_o\left(1 - \frac{r^2}{a^2}\right)^2 \\ w_o &= \frac{qa^4}{64D} \end{aligned} \tag{2.4}$$

where w_o is the center deflection.

Substituting equation 2.4 into 2.3 gives:

$$\begin{aligned} C &= \int_0^{2\pi}\int_0^a \frac{\epsilon_o}{L - w(r)} r dr d\theta \\ &= 8\pi\epsilon_o\sqrt{\frac{D}{qL}}\tanh^{-1}\left(\frac{a^2}{8}\sqrt{\frac{q}{DL}}\right) \\ &= C_o\sqrt{\frac{L}{w_o}}\tanh^{-1}\sqrt{\frac{w_o}{L}} \end{aligned} \tag{2.5}$$

with a zero pressure capacitance of $C_o = \frac{\epsilon_o \pi a^2}{L}$.

The pressure sensitivity is

$$\begin{aligned} \frac{dC}{dq} &= \frac{4\pi\epsilon_o}{q}\left[\frac{8a^2D}{64DL - a^4q} - \sqrt{\frac{D}{qL}}\tanh^{-1}\left(\frac{a^2}{8}\sqrt{\frac{q}{DL}}\right)\right] \\ &= \frac{1}{2q}\left[\frac{C_o}{1 - w_o/L} - C\right] \end{aligned} \tag{2.6}$$

P_{fs}	40psi
a	240μm
h	10μm
L	2μm
w_{max}	1μm
C_o	0.80pF
C_{max}	1.0pF
$\frac{dC}{dq}_{max}$	7.5fF/psi

Table 2.1: Typical sensor dimensions and parameters, for $K_h = 0.1$ and $K_L = 0.5$.

Using as the criterion of small deflection $K_h = \frac{w_o}{h} \leq 0.2$ one design rule for the dimensions of the device is:

$$P_{fs}\left(\frac{a}{h}\right)^4 \leq \frac{64E}{12(1-\nu^2)}K_h \tag{2.7}$$

To avoid touching of the plates, another limit on the deflection is that $K_L = \frac{w_o}{L} \leq 1$. For a desired full scale pressure P_{fs}, an appropriate $\frac{a}{h}$ ratio is selected. For example dimensions for a typical sensor with $K_h = 0.1$ and $K_L = 0.5$ are given in table 2.1.

The capacitance is a nonlinear function of the pressure since it varies inversely with w (itself a nonlinear function of P), and the full-scale percent nonlinearity of the capacitance can be defined as:

$$\%N = 100 \times \frac{C - C_{linear}}{C_{fs} - C_o} \tag{2.8}$$

where

$$C_{linear} = C_o + \left[\frac{C_{fs} - C_o}{P_{fs}}\right] P \tag{2.9}$$

and P_{fs} and C_{fs} are the desired full scale pressure and capacitance respectively (see fig. 2-2). If this nonlinearity is calculated for sensors of two different plate radii and identical pressure ranges, it is apparent that the smaller device is much more linear but has a low sensitivity, while the opposite is true for the larger device. Figure 2-3 illustrates the difference in capacitance values, sensitivity and nonlinearity between a large (a=240μm) and small (a=130μm) device. This discrepancy can be exploited in a linearity calibration technique, as developed in [49], in which the highly linear small sensor is used in a continously running loop to correct for the nonlinearity of the larger sensor that is providing the actual signal.

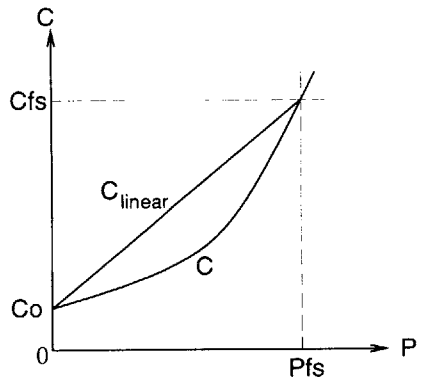


Figure 2-2: Definition of nonlinearity for capacitive pressure sensor.

The sensors fabricated in this work have typical dimensions of radius=100-350μm, plate thickness=10μm, and plate gap=1-2μm. This results in quite a wide range of full scale pressure, from 10 to 2700psi.

With a suitable dielectric present on the surface of one or both plates, the device can also be operated in a touch-mode, where the deformable plate is pressed against the stationary plate as in figure 2-1b. In this case, the deflection of the circular plate can be obtained from the general equation, but with modified boundary conditions to account for the flat central portion of the plate [48]:

$$w = C_1 + C_2 r^2 + C_3 \ln(r) + C_4 r^2 \ln(r) + \frac{qa^4}{64D} \tag{2.10}$$

where the constants C_i are determined from the boundary conditions:

$$\begin{aligned} w(a) &= 0 \\ w(b) &= L \\ \frac{\partial w}{\partial r}(a) &= 0 \\ \frac{\partial w}{\partial r}(b) &= 0 \\ M_r(b) &= -D\left[\frac{\partial^2 w}{\partial r^2} + \frac{\nu}{r}\frac{\partial w}{\partial r}\right] = 0 \end{aligned} \tag{2.11}$$

In order to account for stretching effects in the middle plane as the plate is pressed against the stationary electrode, a modified value for the flexural rigidity is used as derived in [50] and given

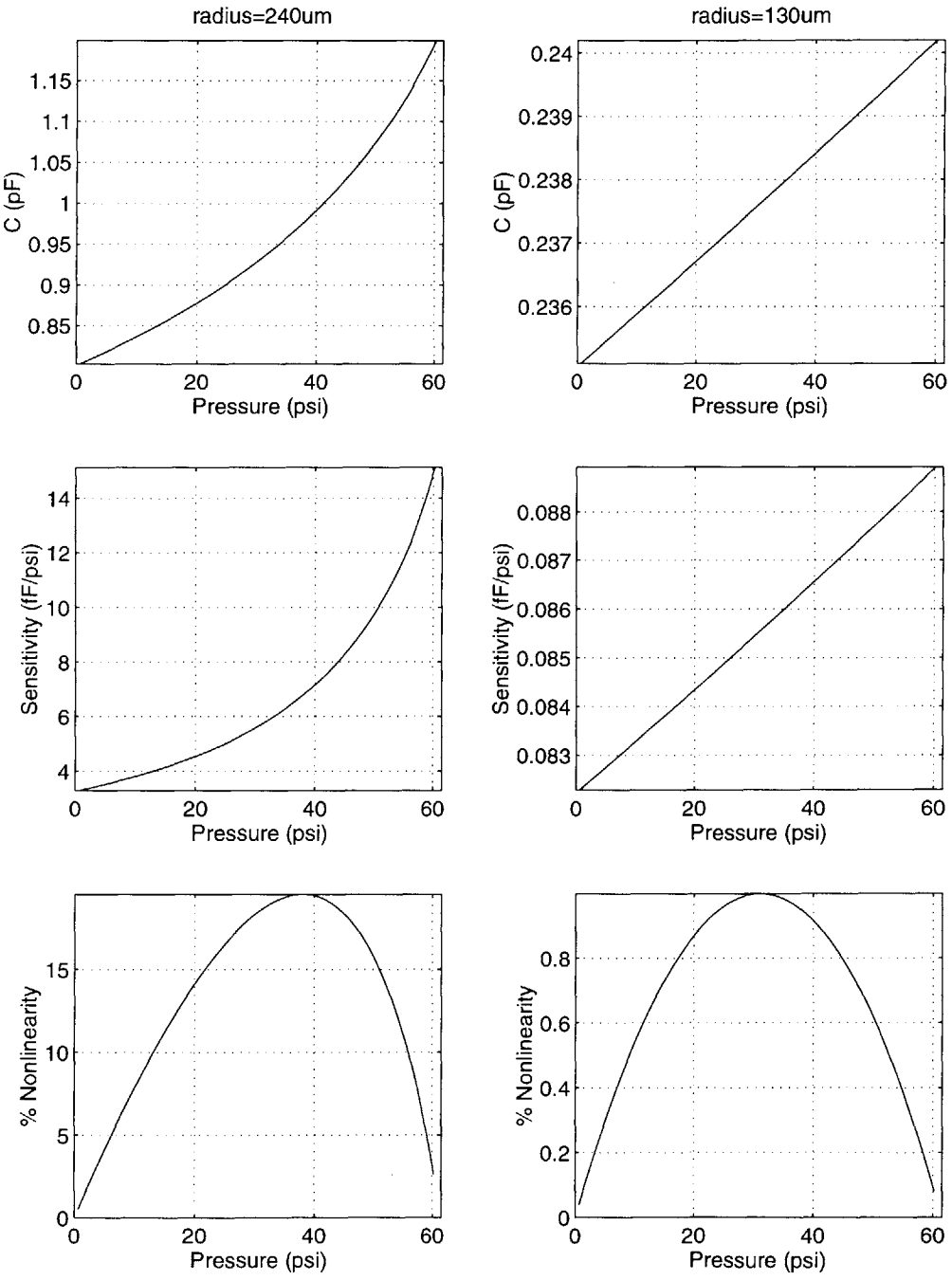


Figure 2-3: Comparison of performance of two different sensor sizes. Both devices have $h = 10\mu$m, $L = 2\mu$m. Full scale pressure is set to 60psi.

below (see appendix A for derivation):

$$\begin{aligned} D_{eff} &= \left[\left(\frac{1.0246\phi}{D}+\sqrt{\left(\frac{1.0246\phi}{D}\right)^2+\phi^3\psi}\right)^{\frac{1}{3}}+\left(\frac{1.0246\phi}{D}-\sqrt{\left(\frac{1.0246\phi}{D}\right)^2+\phi^3\psi}\right)^{\frac{1}{3}}\right]^{-1} \\ \phi &= \left(\frac{64h}{qa^4}\right)^2 \\ \psi &= 0.3187 \end{aligned} \tag{2.12}$$

The final capacitance of the structure in touchmode is then:

$$\begin{aligned} C &= 2\pi\int_0^a \frac{\epsilon_o}{\frac{t_d}{\kappa_d}+L-t_d-w(r)}rdr && w(0)\le L-t_d \\ &= \frac{\kappa_d\epsilon_o\pi b^2}{t_d}+2\pi\int_b^a \frac{\epsilon_o}{\frac{t_d}{\kappa_d}+L-t_d-w(r)}rdr && w(0)>L-t_d \end{aligned} \tag{2.13}$$

where t_d and κ_d are the thickness and relative permittivity of the dielectric respectively. Since D_{eff} is a function of the load q, equation 2.13 must be numerically integrated along with equations 2.10 to 2.12 to solve for the capacitance.

The capacitance in the touched-down regime shows an improvement in linearity as indicated by the calculated curves in figure 2-4. This has been used to advantage in the fabrication of capacitive pressure sensors with more linear response [51, 50], and is also demonstrated in the sensors fabricated for this thesis. There are other methods of increasing the linearity of such a sensor, including the incorporation of ribs or bosses into the plate [51] as well as tailoring of the shape of the stationary electrode [52].

2.2 Frequency response

From equation 2.1 we can get the propagation equation for the displacement of the plate with a time-dependent load, by taking the time derivative:

$$\nabla^4 w+\frac{12\rho(1-\nu^2)}{Eh^2}\partial_t^2 w=0 \tag{2.14}$$

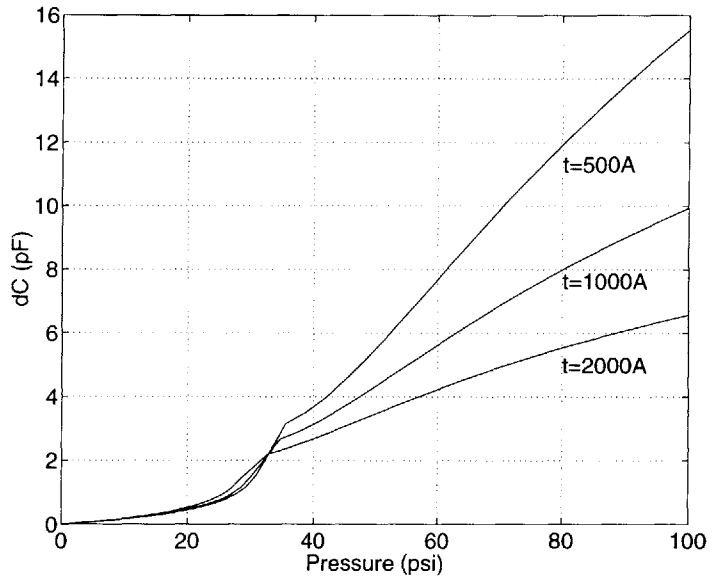


Figure 2-4: Calculated capacitance-pressure characteristic for sensor with a=300μm, h=10μm, L=2μm, t=dielectric (SiO_2) thickness

where ρ is the volume density of the plate. Solving for the time dependence of w, the fundamental vibration frequency of the plate is then [53]:

$$f_{01} = 0.467 \frac{h}{a^2} \sqrt{\frac{E}{\rho(1-\nu^2)}} \tag{2.15}$$

Figure 2-5 shows the variation of f_{01} with plate radius and thickness. For typical device dimensions used in this thesis, the resonant frequency of the plate is above 100kHz.

Structures with narrow gaps experience damping from compression of the gas in the gap, known as squeeze-film damping. This effect can be modeled by considering a simple electrical equivalent to the combined system of the plate and the vented air gap as shown in figure 2-6. The plate and cavity each have a component of mass, compliance and resistance, so the system can be drawn as an equivalent circuit composed of inductance (mass), capacitance (compliance) and resistance (mechanical resistance), driven by a voltage (pressure), with the components having the following values [53]:

$$\begin{aligned} m_e &= \frac{1}{5}\rho a^2 \\ C_{me} &= \frac{9}{16}\frac{a^2(1-\nu^2)}{\pi E h^3} \end{aligned}$$

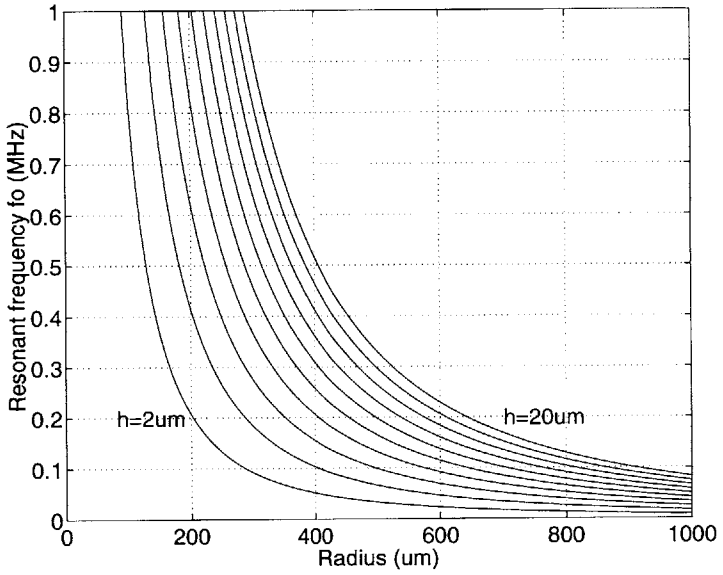


Figure 2-5: Resonant frequency of plate as a function of plate geometry. Each line represents a thickness increment of 2μm.

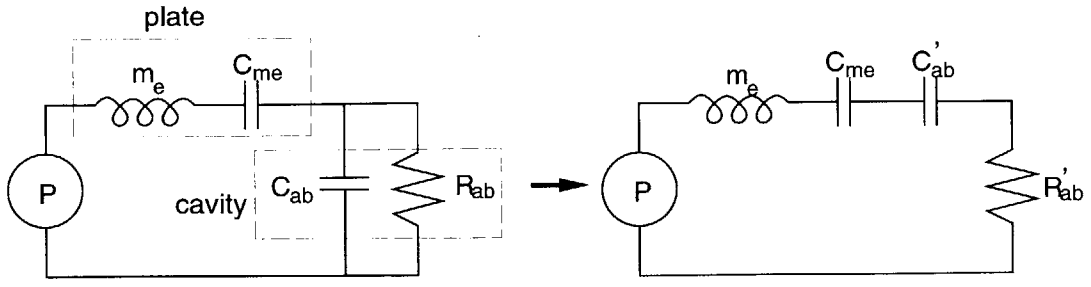


Figure 2-6: Electrical equivalent model of acoustics of plate and cavity.

$$\begin{aligned} R_{ab} &= b_a \\ C_{ab} &= \frac{1}{k_a} \end{aligned} \tag{2.16}$$

The compliance C_{ab} and resistance R_{ab} of the air in the cavity are pressure and frequency dependent and are related to the spring constant k_a and the damping coefficient b_a as follows [54]:

$$\begin{aligned} k_a &= \frac{64\sigma^2 PA}{\pi^8 d} \sum_{m,n_{odd}} \frac{1}{(mn)^2[(m^2+n^2)^2+\sigma^2/\pi^4]} \\ b_a &= \frac{64\sigma PA}{\pi^6 \omega d} \sum_{m,n_{odd}} \frac{m^2+n^2}{(mn)^2[(m^2+n^2)^2+\sigma^2/\pi^4]} \end{aligned} \tag{2.17}$$

where

$$\sigma = \frac{12\mu A\omega}{Pd^2} \tag{2.18}$$

is the squeeze film number at ambient pressure P, μ is the viscosity of air, and d is the plate gap.

The system response can be obtained by solving the general equation for a second order mechanical system:

$$m\ddot{y} + b\dot{y} + ky = F = P_{applied}A \tag{2.19}$$

where for this specific system, the equivalent mass m, damping coefficient b and spring constant k with components from both the plate and the air in the cavity are:

$$\begin{aligned} m &= m_e \\ b &= R'_{ab} \\ k &= \frac{1}{C_{me}} + \frac{1}{C'_{ab}} \end{aligned} \tag{2.20}$$

The frequency response of the equivalent circuit for a fairly small sensor with dimensions a=300μm, h=10μm, L=2μmis plotted in figure 2-7. The load is a sinusoidal time varying pressure with amplitude $P_{applied}=P|_{w=L}$ and assuming an ambient pressure of 1 atmosphere. Also plotted is the response of the plate by itself (no damping). There is little difference in the two responses for a frequency range of up to 10kHz. For low frequencies, k is essentially that of the plate as the air in the cavity is incompressible so that k_a=0. As the frequency increases, the spring constant of the air in the cavity becomes dominant, and the cavity damping declines. Therefore the mechanics of the

plate dominate the response for frequencies of interest (<10kHz). (Note that for higher ambient pressures or smaller gaps the damping term becomes more dominant so that the resonant frequency will be shifted upwards due to cavity stiffening.)

To get another idea of the effect of damping on the structure, the mechanical thermal noise due to dissipation from mechanical damping can be expressed as [55]:

$$p = \sqrt{4k_B T R/A^2} \tag{2.21}$$

where A is the area of the plate, and the acoustic resistance in the system R is composed of two parts, the loss associated with squeeze film damping of the air in the gap:

$$R_{ab} = \frac{3\mu A^2}{2\pi h^3} \tag{2.22}$$

and the radiation resistance, only significant at higher frequencies:

$$R_{rad} = \frac{\rho c \pi a^2 (ka)^2}{4} \tag{2.23}$$

where k is the acoustic wavenumber. (The cavity resistance R_{ab} is the limit of the frequency dependent expression for low squeeze number, at low frequency.) For the same typical device dimensions as used above, and operating the device at 1kHz, the noise pressure is $p = 12\mu Pa/\sqrt{Hz}$, and is almost entirely a contribution from the damping loss.

This chapter has briefly summarized design calculations to select appropriate dimensions for capacitive pressure sensors, test results of which are given in chapter 6. The next chapter will discuss the fabrication process.

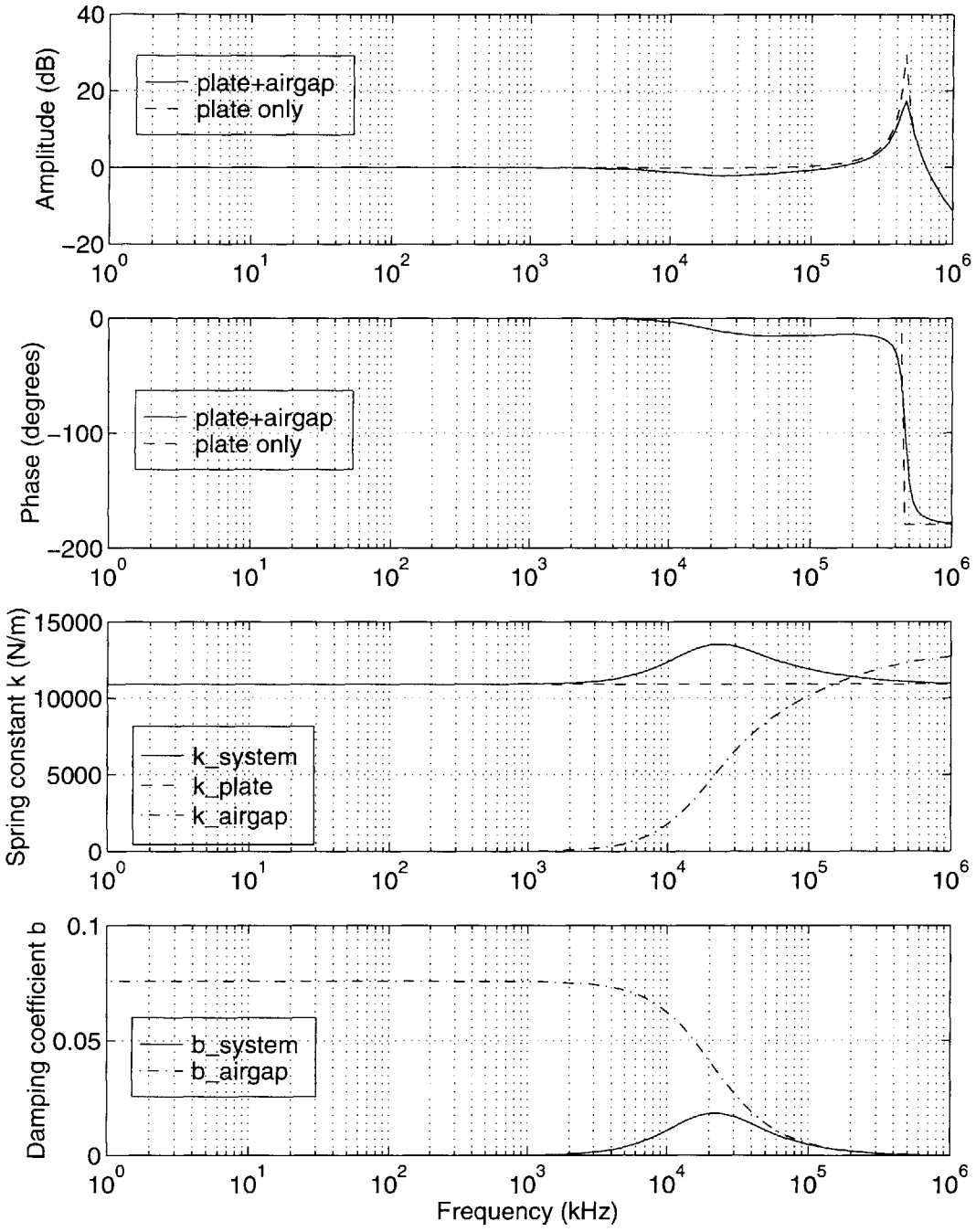


Figure 2-7: Calculated frequency response of plate & cavity. Dimensions are a=300μm, h=10μm, L=2μm, ambient pressure=1atm.

Chapter 3

MEMSCMOS Process Description

This chapter gives a detailed description of the integrated MEMSCMOS process, with a discussion of the micromachining steps required to construct both bulk and surface-micromachining-like devices that can be capacitively detected. The process uses a partitioned approach, as given in figure 1-4. The micromachining steps are decoupled from the integrated circuit fabrication steps, and these three sections are designed to be independent of one another; in particular, no modifications to the center block of the (foundry) integrated circuit process is necessary to accomodate the substrate, thus allowing independent optimization of process parameters that impact on circuit and sensor performance.

Figure 1-4b is a schematic illustration of the general process flow, in which the front-end micromachining block consists of the formation of the sealed cavity substrate. The circuit fabrication can be any existing (commercial) process, since the cavity is internal to the substrate such that no special fixturing for the wafers is required. The cavities are formed by contacting the wafers in a controlled ambient, resulting in membranes that are able to withstand the high temperatures seen in an IC process. The rationale for this bonding technique is detailed in chapter 4. This sealed cavity substrate can be sent out for placement of circuits in the field areas, after which the back-end micromachining steps, designed to be low temperature predominantly dry processes, are performed.

The complete process flow illustrated in figure 3-1 is described in detail in the following sections of this chapter, as developed to make a pressure sensor and accelerometer (representative of bulk and

surface micromachining-like sensors respectively), and CMOS circuitry. The sealed cavity has also been used in modified form to fabricate structures that require thermal and electrical isolation via a thin silicon nitride membrane, such as infrared detectors [38] and piezoelectric thin film resonators [37].

3.1 Front-end micromachining

The purpose of the front-end micromachining stage is to form the sealed cavity, and it is composed of three subsections:

- substrate preparation
- wafer bonding
- wafer thinning

Starting substrates for the front-end micromachining are two <100> single crystal silicon wafers, selected according to the post-bond wafer thinning method to be used:

1. Electrochemical thinning (fig. 3-2a)
   - active wafer: p-type substrate with n-type epitaxial/diffused layer
   - handle wafer: any dopant type, $\rho < 1\Omega$cm
2. Chemical thinning (fig. 3-2b,c)
   - active wafer: thick film SOI wafer, any dopant type
   - handle wafer: no restriction

The thickness of the n-type layer in case 1, or the top silicon in case 2, determines the final thickness of the sealed cavity silicon plate and thus the final sensor element. If electrochemistry is used, the handle wafer must have a fairly low resistivity to provide adequate electrical contact through the

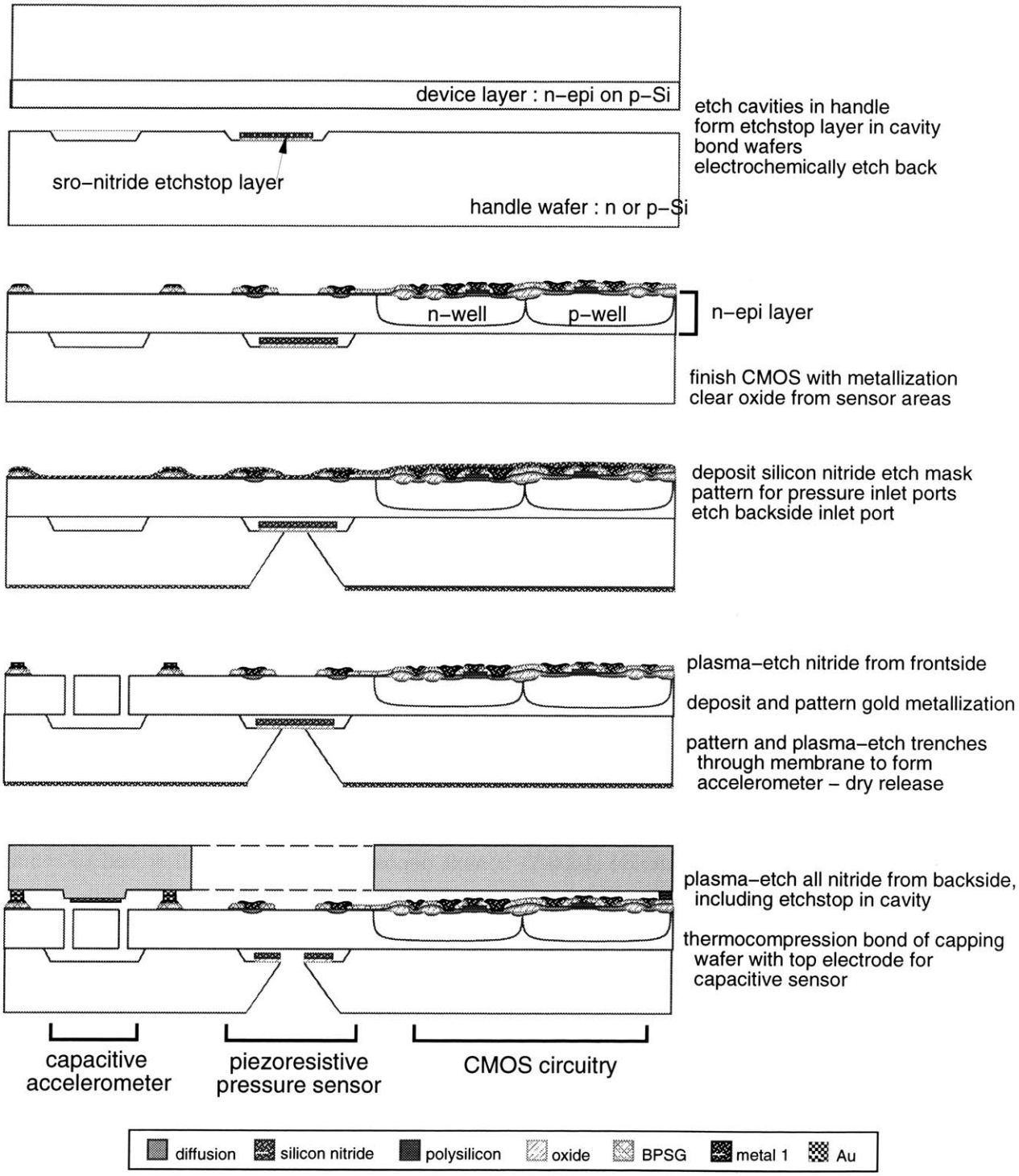


Figure 3-1: MEMSCMOS process flow.

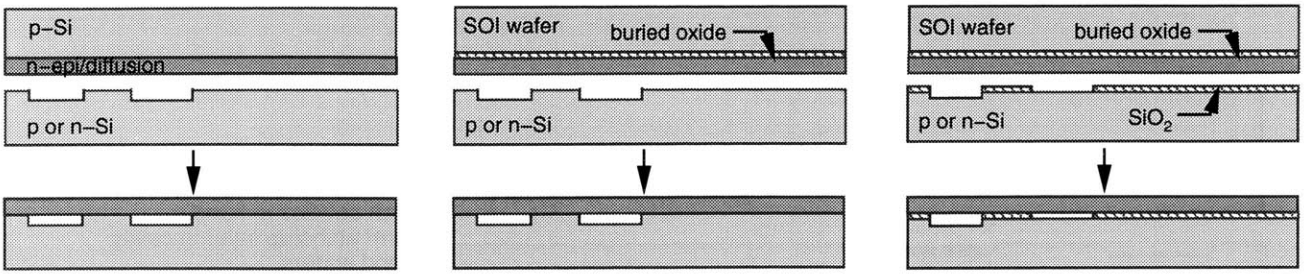


Figure 3-2: Active-handle wafer combinations and thinning methods. a)electrochemical etching, b)chemical etching, c)chemical etching with dielectrically isolated bonded layer

wafer during the etch. In both cases, the handle wafer should be polished on both sides to facilitate subsequent alignment to embedded cavities through the wafer.

Fabrication starts with the formation of cavities in the handle wafer (typically done with an SF_6-CCl_4 plasma etch). This may be followed by or replaced with an oxidation and patterned removal of the oxide for dielectrically isolated silicon plates (see fig. 3-2c). A stack of thermal oxide (430Å) and LPCVD low stress silicon nitride (1500Å) is next deposited, patterned and etched to remain only in cavities where access to the plate from the back of the wafer is required (eg. pressure sensors). (Note that some care must be taken to ensure that no nitride/oxide residues remain in the field areas surrounding the cavities, as they can result in failure to bond, and void formation.) The handle and device wafers are joined with a silicon wafer bond, consisting of an RCA clean, followed by contacting in an oxygen ambient with the bonding setup to be described in section 4.2, and annealing at >1000°C for a minimum of 1 hour. Subsequently, the bonded pair is thinned by grinding to remove approximately 400μm of silicon, polishing to remove an additional 30μm of surface grind damage, and one of the two etching methods described in section 3.1.1. The resulting substrates with uniform silicon plates over enclosed cavities are now ready for the placement of circuits.

3.1.1 Wafer thinning

The two thinning methods available are the chemical and the electrochemical etch, both of which involve the use of wet anisotropic silicon etchants. The chemical etch relies on the presence of an etchstop layer of either silicon dioxide or a heavily boron doped layer. The electrochemical etch utilizes the different bias dependent behaviour of n and p-type silicon in the etchant. In both cases, the etchant is a 20% by weight KOH solution at a temperature of 95°C (other hydroxide etchants such as tetramethyl-ammonium hydroxide (TMAH) can also be used). A surfactant [56] is added to the solution (in the amount of 4mL/L of etchant) to decrease bubble evolution and improve the smoothness of the final etched surface.

Chemical etchstop

As previously mentioned, the etchstop layer can be either a)a buried oxide or b)heavily boron doped. In method a) the buried oxide is part of an SOI active wafer, which in the case of a thick-film top silicon layer, is usually itself formed by bonding and thinning (by grind and polish). It is also possible to use a SIMOX wafer if the required bonded layer thickness is less that about 1μm. For method b), the etchstop is a layer with a high concentration ($> 10^{20}/cm^3$) of boron [57] in which case the active wafer contains two layers of epitaxial silicon - a lower p++ layer and an upper lightly doped epi which is the final bonded layer. However use of this type of wafer limits the maximum bonding anneal temperature to about 800°C in order to prevent spreading of the boron and reduction of the etchstop efficiency. In addition, heavily boron doped layers exhibit high tensile stresses induced by lattice strain, resulting in dislocations in any silicon grown on top of the layer. This strain can be compensated by codoping the silicon with germanium, typically to a concentration of $> 10^{21}/cm^3$ [58] to produce a dislocation-free layer. The germanium appears to have no effect on the efficacy of the etchstop.

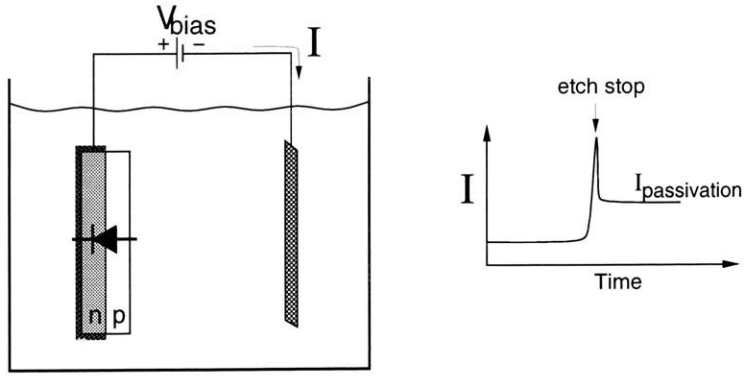


Figure 3-3: Electrochemical etch.

Electrochemical etchstop

Electrochemistry is a bias dependent technique in which a voltage applied to the silicon in the etching solution causes the formation of an anodic oxide that passivates the surface [59, 60, 61]. The difference in passivation potentials between p-Si and n-Si can be utilized to selectively etch p-Si over n-Si in a diode structure, by biasing the n-layer at a level anodic to its passivation potential. Figure 3-3 illustrates the principle - a positive voltage is applied to n-Si with respect to the solution and the p-Si potential is left floating, creating a reverse biased diode that allows the p-Si to be etched until the junction is reached. At this point current flow commences through the remaining n-Si and the resulting anodic oxide passivates the exposed surface, terminating the etch. The endpoint is indicated by a rise in the current through the wafer-etchant system, after which the current level drops to that required to maintain the anodic oxide ($I_{passivation}$). The dopant in the bonded layer must be n-type, although there is no requirement that the layer be heavily doped, so that it is still suitable for use as a circuit substrate. The electrochemical etch has been used with both n and p-type handle wafers [62].

Extensive work has been done by a number of groups to characterize the etch-rate and current-voltage characteristics of p and n-type silicon as well as pn junctions for various etchant concentrations and temperature conditions, the majority of the studies being done using KOH [63, 60, 61]. A consensus of these investigations was that there are two factors that can affect the success of the electrochemical etching technique. The first involves the formation of ohmic drops along the n-type etchstop layer. It was found that if the sample is contacted at only one point, as is often the case

when fabricating bond-and-etchback-SOI substrates, voltage drops along the n-layer due to resistive losses can result in the bias in portions of this layer falling below the passivation potential[60]. In these areas, the anodic oxide required to passivate the surface is not formed and the silicon is overetched, thus destroying the membrane to be formed. The problem can be avoided by using a setup that allows contact over a large area of the n-type etchstop layer. This can be accomplished easily with a structure that contains a direct silicon-silicon bond without an insulating layer, since all parts of the etchstop layer are then electrically accessible from the back of the wafer. With this type of structure, the ohmic losses along the etchstop layer are much reduced so that no portion of the layer falls below the passivation potential. If an SOI configuration must be used, then ohmic drops can be reduced by providing electrical contact through the insulating layer by means of conductive vias [64].

The second problem in using ECE concerns the occurrence of premature passivation of the etch in the p-type silicon, resulting in an etched-back layer that is thicker than the junction depth of the etchstop layer. This problem has been observed by a number of groups, and appears to be affected by a variety of factors including the etchant type and temperature, the applied bias voltage, and the quality of the diode formed by the etchstop layer. Experiments done to characterize the temperature dependence of the etchstop position have shown that the etch terminates within 0.1μm of the metallurgical junction when appropriate bias and temperature conditions are applied [65]. Table 3.1 summarizes the results of a temperature study in which the p-Si layer thickness remaining after etch termination at various temperatures was measured using spreading resistance profiling (etch sample is illustrated in figure 3-4). The trend can be explained as being caused by the relative temperature dependence of the peak passivation current and the junction leakage current. The passivation current is due to hole consumption and electron release at the silicon surface during dissolution of the silicon. If the magnitude of the peak current during passivation is a stronger function of temperature than the junction leakage current, then at a sufficiently high etchant temperature, this current will exceed the leakage current until the p-layer has been completely removed. This appears to indicate that higher etchant temperatures can be used to decrease the effect of high junction leakage currents [65, 66].

Table 3.1: Electrochemical etch temperature experiment

Etchant temp. (^{o}C)	x_p from SRP (μm)
95	0.1±0.05
90	0.5±0.05
80	1.2±0.10
70	1.7±0.10

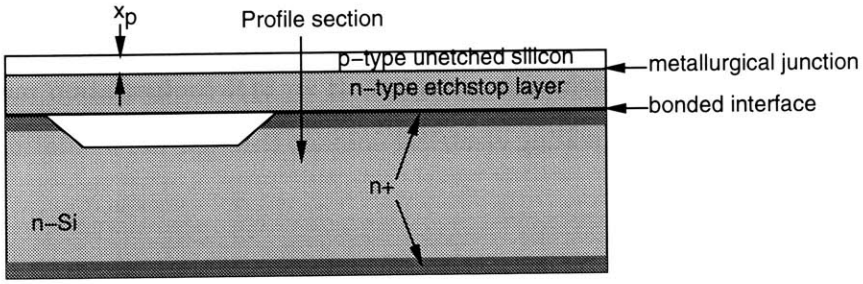


Figure 3-4: Schematic of sample used for spreading resistance profiles.

3.1.2 Post wafer-thinning process

Note that if electrochemistry is to be used for wafer thinning, the bonding anneal is followed by an additional doping step ($POCl_3$ liquid source for n-handle, boron implant for p-handle) to heavily dope the backside of the wafer pair for obtaining good electrical contact during the electrochemical etch. Alternatively if the chemical etch is to be used, the bonding anneal should be done in an oxidizing ambient or an additional oxidation performed, to grow a protective oxide for the handle wafer during the thinning step.

The use of an SOI active wafer results in a final surface roughness which is comparable to that of an unprocessed wafer, whereas electrochemical thinning leaves a roughness of <100Å. This may necessitate a final polish of the wafer surface to render it acceptably smooth for circuit fabrication.

3.2 Circuit fabrication

Any existing circuit process can be used at this stage. For devices described in this work, circuits are fabricated using a 1.75μm twin-well CMOS process [67] completed up to and including one level

of aluminum metallization. The substrates at this stage are represented in figure 3-1b).

The initial alignment in the circuit process requires that surface features be aligned to the buried cavities. This can be accomplished in one of two ways. The alignment marks can be "transferred" to the surface by means of a photolithography step using infrared illumination from the back of the wafer to align the transfer marks to the buried features, after which a shallow (<1000Å) silicon plasma etch serves to define the marks on the top surface of the wafer. However, for sufficiently thin silicon plates there is enough of an IR component in the illumination provided by a conventional stepper alignment microscope to be transmitted through the silicon plate, so that the cavity underneath is visible in the alignment screen. For a typical halogen light bulb emitting white light, the transmission depth of silicon is on the order of 1-10μm. Therefore it is possible to "see" cavities with plate thicknesses in this range, thereby eliminating the photolithography and etch steps as well as the need for through-wafer infrared alignment, and this method has been used to align to buried features with minimum dimensions of 3x100μm.

Because the wafers will be subjected to further handling after the CMOS process, a protective passivation layer of silicon nitride over the metal is highly recommended to protect the aluminum lines and bondpads from scratches.

3.3 Back-end micromachining

The post-CMOS back-end micromachining steps are shown in figures 3-1c) and d) and can be divided into three sections:

1. backside release
2. frontside release
3. top electrode formation

The presence of aluminum metallization on the wafers at this stage requires that all of these steps be performed at low (<350°C) temperatures.

Prior to the steps listed above, the passivation doped oxide is removed from micromechanical structure areas with a wet etch. The oxide can also be removed at the contact etch step in the CMOS process, however the silicon is then left exposed at the metal etch stage, as well as influencing the contact etch as a result of increasing the area over which the etch endpoints.

After the two release etches to be described, a sinter step is added to eliminate any excess charges introduced as a result of the plasma etching and ashing required for the releases.

3.3.1 Backside release

The backside release serves to form the backside pressure inlet holes for pressure sensors. This is done with an anisotropic etch in potassium hydroxide, using a layer of PECVD silicon nitride as an etch mask to protect the rest of the wafer. The photolithography to define the etch holes requires an infrared alignment to be able to align the openings in the etch mask to the sensor cavities near the front surface of the wafer. The etchant stops on the buried Si_3N_4+SiO_2 stack inside the cavities, after which the silicon nitride etch mask is removed from the front of the wafer with a blanket plasma etch in SF_6. (Note that the silicon plates are not passivated with an oxide so that they are exposed to the plasma at the end of the etch.) The nitride+oxide in the cavity is kept in place and is removed prior to wafer sawing, to keep the cavities dry during subsequent photolithography steps.

A suitable PECVD silicon nitride layer was obtained using a low frequency plasma system developed by Surface Technology Systems Ltd. (KOH etch rate of 300Å/hr at 95°C). However, in attempting to use this film as a cover for the metallized frontside of the wafers, poor step coverage over the metal combined with what appeared to be stress-related cracking of the nitride film at the metal edges resulted in peeling of the nitride over the metal, and subsequent overetching of the aluminum metallization. Therefore, to protect the front of the wafer a coating of Carnauba wax [68] was applied and used as an adhesive for KOH-resistant tape [69]. The combination of wax and tape was resistant to KOH at 60°C for the 20 hours required to complete the etch. The wax, available in flake form, was applied by melting onto the wafer, and removed by dissolving in heated photoresist stripper (n-methyl pyrrolidone). The melting point of the wax (82°C) limits the etchant

temperature to be less than 70°C to maintain a stable adhesion to the wafer.

As an alternative etchant, silicon-doped TMAH has been shown to have a high etch resistance to aluminum [70, 71] (dissolved silicon lowers the pH of the solution such that the aluminum oxide etch rate is much reduced). However, the depth of the vias (500μm), combined with TMAH's tendency to form hillocks resulted in etch times that were too long for the aluminum to withstand the etchant without an additional protective layer.

In order to avoid the use of a wet etchant for this step, a deep dry silicon etch would be a much more desirable alternative. New deep silicon etchers are now capable of etching narrow ($\approx$ 20μm) deep ($\approx$ 500μm) vias in silicon with only photoresist required as a mask, and with a suitable etchstop layer inside the cavity (SiO_2) can be used for this purpose.

3.3.2 Frontside release

Conventional frontside releases in surface micromachining experience stiction of released structures to the substrate as the wafers are dried [8], necessitating special procedures like CO_2 drying [7]. However, the frontside release used in this process does not have this problem as it does not utilize wet etchants. It consists of a two-step plasma etch (using SF_6 and CCl_4) through the silicon membrane that results in the formation of surface-micromachined-like suspended structures. Details of this technique developed by C.Hsu are given in [62], and are briefly outlined here and illustrated in figure 3-5.

The first stage is a partial etch of the silicon plate in an area away from the main mechanical element. This etch acts on a small opening, and is done to a depth of about half the final thickness of the plate. The second stage is the definition of the mechanical element. The purpose of the first partial etch is to provide a pressure release for the large plate during the final etch. As the second etch proceeds, the release hole is opened first, thereby equalizing the pressure on both sides of the suspended plate. If the release hole is omitted, the sudden equalization of pressure over large areas of the plate often causes it to rupture.

To complete processing of the silicon substrate, the remaining silicon nitride etch mask on the back

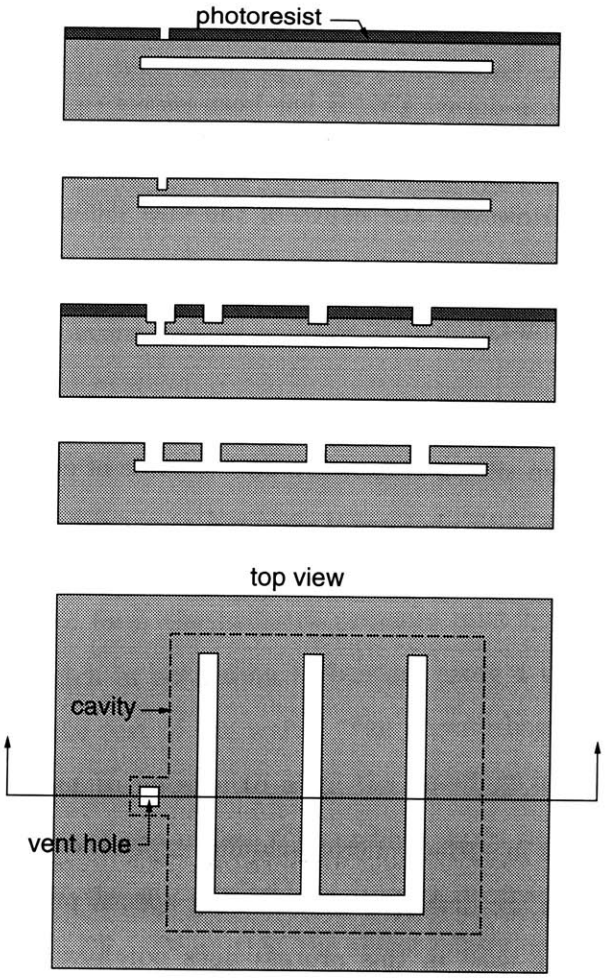


Figure 3-5: Frontside release procedure.

of the wafer is removed, again with a dry etch in SF_6. In the process the cavity etchstop nitride is also removed, thus releasing the pressure sensor membranes. The wafer is now ready for die separation and the addition of the top electrode.

3.3.3 Upper electrode formation

If capacitively detected devices are to be fabricated, a top electrode is added to the base substrate by means of a thermocompression bond between a layer of metal on the silicon substrate and a complementary layer on a (glass) wafer. In addition to providing an electrical contact to the top electrode through the metal-metal bond, the use of a rigid capping wafer provides an overpressure stop for the mechanical structures. Initially a Pyrex wafer is used for ease of alignment; however

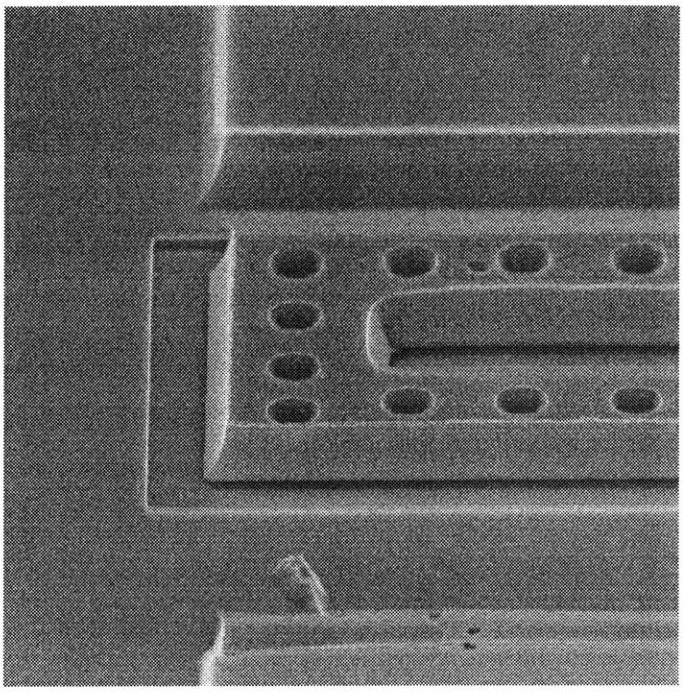


Figure 3-6: SEM of frontside released structure.

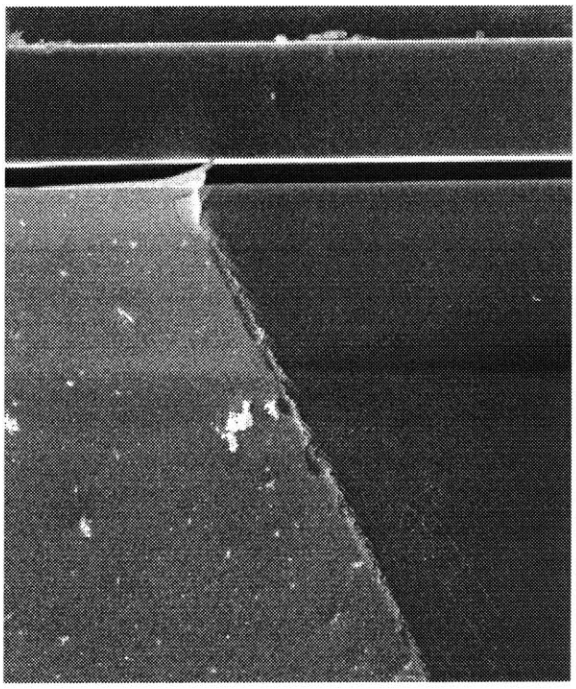


Figure 3-7: SEM of edge of backside pressure inlet port.

for better thermal matching a silicon wafer may be desirable.

The metal used for the thermocompression bonding technique is a layer of 5000Å of gold (over an adhesion layer of 100Å of chromium), deposited by electron-beam evaporation and patterned using liftoff. Gold is selected as the metallization for two reasons: first, it does not form a surface oxide in air, therefore scrubbing/ultrasonic action is not needed to break through the oxide, and second, it can be bonded at a relatively low temperature due to its softness. The silicon substrate gold is deposited and lifted off prior to the frontside release etch. (Note that at this stage the backside vent holes have not been fully opened and the cavity etchstop is still in place, so that the wafer can be handled without the need for special fixturing.) Since the bond quality is adversely affected by the presence of any organic material adsorbed on the gold surfaces, they are cleaned with an ultraviolet ozone exposure, after which the surfaces are aligned, contacted, and heated to 350°C on a hotplate while a pressure of about 20 psi is applied for a period of 2 minutes. Studies of the strength of the thermocompression bond [66] have indicated that the shear strength is comparable to that of conventional wire bonds, and that failure of the bond usually occurs in the bulk of the silicon or glass, not at the gold-gold interface.

Currently the thermocompression bonding is done on a chip level using a jig setup to hold and align the chips prior to bonding [72]. This sometimes results in problems with particulate generation during handling. However, the process can be transferred to wafer level with suitable equipment that is capable of applying enough uniform pressure over the whole wafer to initiate the bond. This necessitates the machining of holes in the capping wafer prior to bonding for access to bond pads on the silicon chip. To prevent water from entering between the two wafers during the sawing operation, the chip edges should be sealed with gold as indicated in figure 3-8. Internal areas that require vacuum sealing can also be formed with appropriate gold patterns. Electrical contact to internal vacuum sealed areas can be achieved by means of diffused or polysilicon bridges leading out to exposed bondpads (bridge resistance minimized since L<W). By covering the glass side of the wafer pair with tape during the sawing operation, the chip is protected from the saw slurry. The schematic in figure 3-8 gives a representative gold sealing pattern as required for a chip with an integrated capacitive pressure sensor and accelerometer.

Figure 3-1e) represents the final chip cross section, as fabricated for a capacitively detected ac-

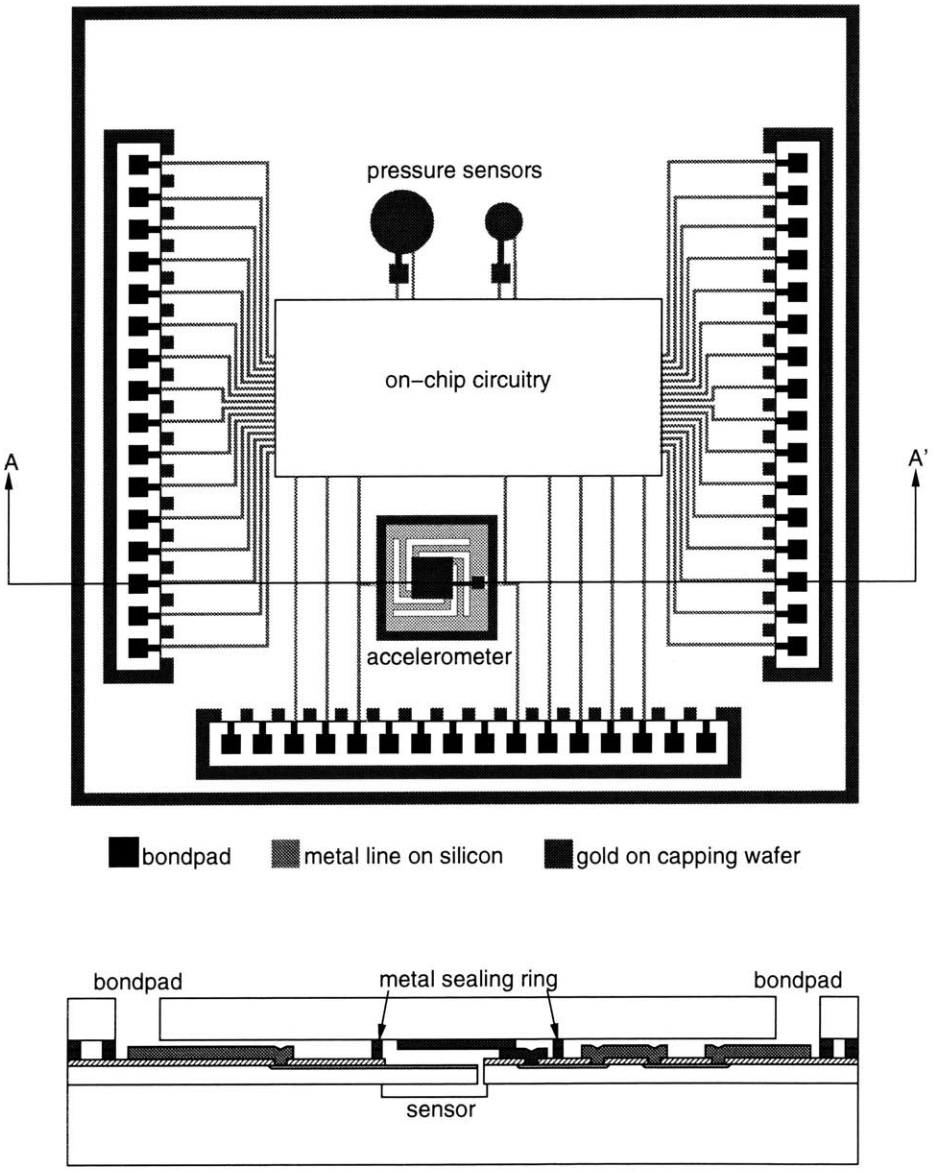


Figure 3-8: Proposed metallization pattern for wafer-level thermocompression bond.

celerometer, a piezoresistive pressure sensor, and CMOS devices with one layer of metal. A complete process flow is given in appendix I, including details of the MIT baseline CMOS process. The micromachining adds a maximum of 7 additional lithography steps and 21 additional film depositions and etches.

This chapter has given the details of the MEMSCMOS process in which the sealed cavity is formed using silicon wafer bonding in a controlled ambient. The next chapter will discuss the reasoning for using this method of bonding.

Chapter 4

Plastic deformation in sealed cavity plates

The success of the sealed cavity integrated sensor process hinges on the ability to make cavities that can withstand high temperatures without damage. As mentioned in chapter 3, during the wafer bonding step the wafers are contacted in a controlled ambient to achieve a reduced gas pressure inside the cavity. The reasoning behind this requirement is explained in this chapter. Models and experimental characterization of the high temperature behaviour of sealed cavity silicon plates are presented. The analytical models are combined with finite element simulations to produce a program that can be used as a tool for sealed cavity design.

4.1 Plastic deformation of silicon

Silicon is desirable as a mechanical material for microstructures because of its high strength and reliability, and well-characterized electrical properties. Its mechanical properties have been studied extensively, and its elastic-plastic behaviour is fairly well known. At temperatures below approximately 600°C silicon is a brittle material with a fracture strength of 0.7GPa. Above this temperature, it becomes ductile and exhibits a stress-strain curve characteristic of most semiconductors, schematically illustrated in figure 4-1. Note that there is a significant drop in the stress from the upper to the lower yield (or flow) point, both of which decrease in magnitude with increasing tem-

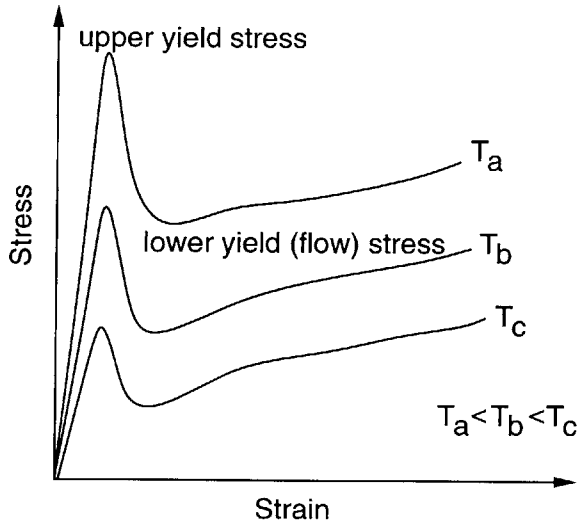


Figure 4-1: Qualitative stress vs. strain behaviour of silicon

perature. When the induced stress in the material exceeds the upper yield stress for a given strain rate, the silicon will plastically deform, after which the deformation is sustained if the stress in the material stays above the flow stress. The plastic deformation is manifested as a warpage of the silicon when cooled back to room temperature, as well as an increased concentration of dislocations. Experimentally determined yield and flow stress variations with temperature and strain rate for single crystal silicon are shown in figure 4-2 [73]. The transition temperature from brittle to ductile behaviour is determined by the strain rate, and is also influenced by other factors not indicated in the data, most notably the content of impurities such as oxygen, and initial dislocation density (float-zone vs. Czochralski growth). This data has been confirmed by additional experiments done to extend the temperature range to 1200°C [74].

In conventional integrated circuits the mechanical strength of the silicon is not a primary concern as it is not used as a structural material. However there is ample evidence that thermomechanical stresses during processing (in particular during wafer heating/cooling from furnace loading) can result in plastic deformation, producing dislocations that lead to nonuniform electrical properties, through their interaction with already present dopants and impurities in the substrate. These thermal stresses are most commonly manifested as overall wafer warpage [75], and localized deformation (slip) at film edges [76, 77]. In electrical performance, dislocations lead to enhanced leakage currents when present at junctions, enhanced diffusion of dopants and formation of pipes [78]. Modern starting substrates are dislocation-free, and they are introduced during processing

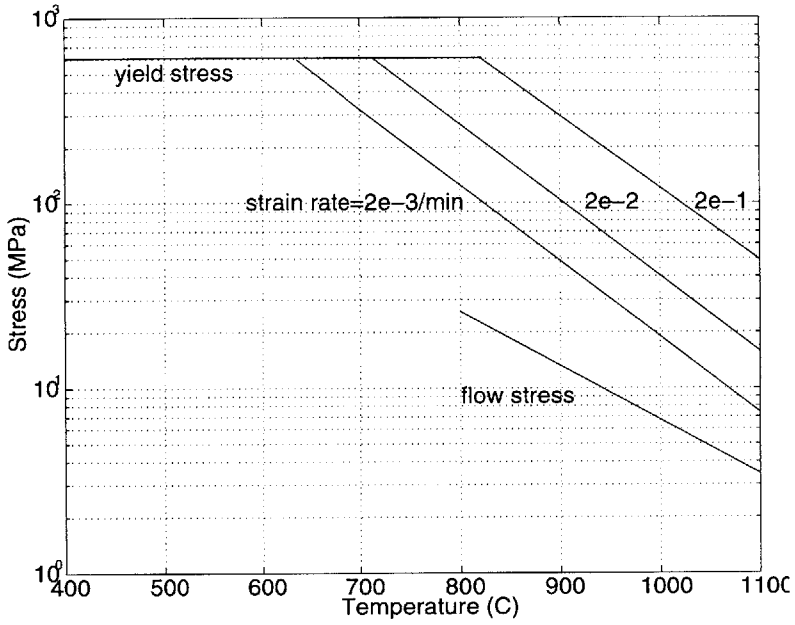


Figure 4-2: Temperature dependence of silicon yield and flow stress.

as a result of differing thermal expansion coefficients between thin films, deposition of films with intrinsic stress, and introduction of dopants, particularly when implanted.

In addition to the above mentioned sources of stress common to all semiconductor device processes, there are additional mechanical stresses generated in sealed cavities. Localized plastic deformation in sealed cavities can also arise from the expansion of trapped gas inside the cavity at high temperatures. Its onset is dependent on the device geometry as well as the pressure of the gas trapped inside the cavity. The expansion of this trapped gas creates a uniform pressure load on the plate as it is heated past the transition temperature of the silicon from the brittle to the plastic regime. The effect of heating a sealed cavity is illustrated very simply in figure 4-3, where the sealed cavity is formed by contacting the starting wafers in normal air conditions and annealing to complete the wafer bond. After thinning of the top wafer the silicon plate is initially deflected downwards into the cavity as a result of the wafer bonding process, in which the oxygen content of the trapped air inside the cavities is consumed through oxidation of the surrounding silicon sidewalls during the high temperature bonding anneal, thus leaving a reduced pressure of about 0.8 atmospheres inside the cavity at room temperature [79]. Upon subsequent heating of this structure, gas expansion causes the plate to deflect upwards. If the maximum temperature is kept below 600°C, the plate will either return to its original shape upon cooling, or rupture if the load exceeds the fracture

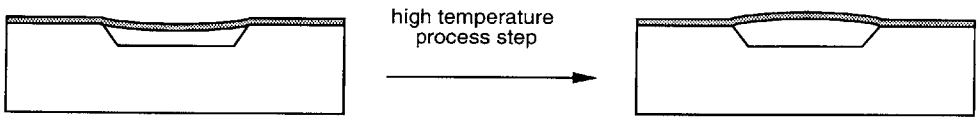


Figure 4-3: Plastic deformation of a sealed cavity plate

strength of 0.7GPa. However, if the maximum temperature is greater than 600°C and the stress in the plate exceeds the yield stress, plastic flow commences and the plate will not return to its original shape upon cooling but will maintain an upwardly deflected shape. Plastic deformation has been used to advantage to make domed structures such as pressure switches [80], but for the most part is to be avoided, as it results in a change in the shape, and therefore the mechanical behaviour, of the plate. Therefore this entails keeping stresses in these silicon plates below the upper yield stress at all stages of processing, either by limiting the temperature to 600°C or by modifying the cavity shape such that lower stresses are generated. Obviously the upper temperature limit of of 600°C is not feasible as it complicates the integration of such structures with conventional circuitry. Since the loading is a result of gas expansion, control of the gas pressure in the cavity provides a means of raising this temperature limit, as will be discussed in the next section.

4.2 Controlled ambient bonding

The phenomenon of plastic deformation in thin silicon plates over sealed cavities was described in detail by Huff [81], in which a model was developed to predict the onset temperature of plastic deformation of these plates under high temperature anneals. From this model, it is apparent that one method of avoiding this phenomenon is to reduce the gas expansion loading of the plate by reducing the trapped gas pressure inside the cavity. This is achieved by controlling the ambient in which the wafers are contacted, either by contacting in a vacuum or in an oxygen-rich environment. A setup designed to provide an oxygen contacting ambient is illustrated in figure 4-4 [65] (this apparatus is a simplified version of one developed at Duke University [82], (see appendix C for detailed drawings). The chamber holds the two wafers to be bonded, separated by Teflon shims, and is flooded with a controlled mixture of oxygen and nitrogen gases. The separators are removed and bonding is initiated with a point contact at the center of the wafers, after which they are

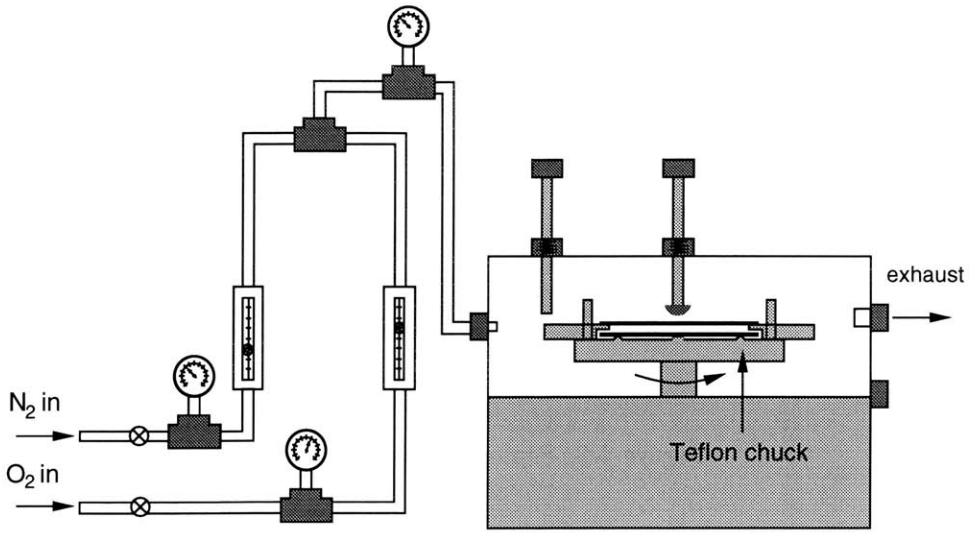


Figure 4-4: Setup for controlled ambient bonding

annealed in a conventional furnace tube. The gas pressure inside the cavity after the bonding anneal is determined by the proportion of the contacting gas mixture that was nitrogen. This apparatus has been used to construct cavities with a range of cavity residual gas pressures [66]. Upon subsequent annealing of these sealed cavities, it was shown that there is a definite transition temperature above which plastic deformation occurs in the silicon plate, dependent on the bonding ambient and the dimensions of the cavity and plate. The transition temperatures and gas pressures can be determined by means of a model of the cavity, to be described in the next section.

4.3 Model for plastic deformation

The maximum allowable temperature for a given set of device dimensions and cavity pressures can be calculated by modelling the structure as a clamped plate over an enclosed cavity with an ideal gas trapped inside the cavity, as shown in figure 4-5. For simplicity, only circular and square geometries will be considered.

The stress in a sealed cavity plate is dependent on the loading and deflection of the plate at a given temperature. Assuming the gas in the cavity behaves as an ideal gas, the following set of relationships apply:

$$q = P_{CAV} - P_{ATM} \tag{4.1}$$

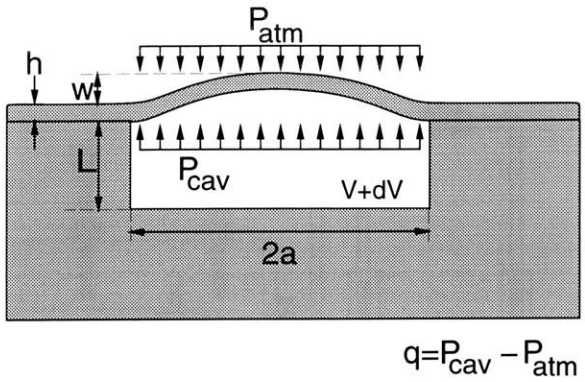


Figure 4-5: Sealed cavity dimensions

$$\frac{P_{CAV_0} V_{CAV_0}}{T_0} = \frac{P_{CAV} V_{CAV}}{T} \tag{4.2}$$

$$V_{CAV} = V_{CAV_0} + dV_{CAV} \tag{4.3}$$

$$dV_{CAV} = f(w) \tag{4.4}$$

$$w = f(q) \tag{4.5}$$

where the subscript 0 refers to conditions at room temperature.

Equations 4.1-4.5 can be solved to obtain a set of plate deflections as a function of temperature, for a given starting cavity pressure. For small deflections the plate edge will have the maximum stress whereas plates in large deflection undergo stretching in the middle plane so that the maximum stress is at the center of the plate. In order to determine whether or not plastic deformation will take place, the edge and center stresses are calculated and compared to the yield and flow stress properties of silicon. The criterion used for the onset of yielding is the von Mises criterion, derived by considering the maximum distortion strain energy [83]. Normally this criterion is used when dealing with failure in ductile materials such as metals, whereas single crystals yield by the mechanism of slip along certain planes, as a result of the regular arrangement of atoms in the material. Appendix D contains a discussion of the validity of the use of the von Mises condition for predicting yielding in single crystal silicon, based on its definition as a shear stress along one of the principal slip planes in silicon.

For circular plates, the center deflection of a uniformly loaded clamped circular plate is given by:

$$w = w_o \left(1 - \frac{r^2}{a^2}\right)^2 \tag{4.6}$$

$$\frac{w_o}{h} + 0.488\frac{w_o^3}{h^3} = \frac{qa^4}{64D} \tag{4.7}$$

where w_o is the deflection at the center of the plate. This is an approximate solution of equation 2.1 obtained by using the energy approximation method for plates in large deflection [48] (see appendix A for derivation). Combining this expression with equations 4.1-4.5 and solving gives the deflection and cavity pressure as a function of temperature.

The plots in figures 4-6 to 4-9 show calculated stresses in plates with dimensions suitable for use in pressure sensors. Figures 4-6 and 4-7 plot stress vs. temperature in circular plates for two sets of geometries: a relatively "small" cavity (a=300μm, L=2μm) and a "large" cavity (a=1000μm, L=20μm). The limiting temperature is the point at which the stress exceeds the yield stress curve (using yield data for the lowest available strain rate). The values plotted are von Mises stresses, which by definition are always positive; a change in the slope of the line signifies a change in sign from compression to tension or vice versa. Thus the change in slope of the stresses in figure 4-6 for P_{CAV}=0.8 atm at 130°C indicates that the plate deflection is in transition from being downward to upward, and the stress at the edge of the plate is changing from tension to compression whereas the opposite is occurring at the center of the plate. At P_{CAV}=0.2 atm, the plate remains deflected downward for the entire temperature range, so that the edge remains tensile and the center remains compressive.

For a small cavity with P_{CAV}=0.8 atm (wafers contacted in air) the upper temperature limit is 825°C whereas reducing P_{CAV} to 0.2 atm raises this limit to 1060°C, Similar calculations can be done for square plates using the appropriate equations for deflection and stress [84], and are plotted in figures 4-8 and 4-9. From figure 4-8, P_{CAV}=0.8 atm results in T<990°C whereas P_{CAV}=0.2 atm gives T<1250°C.

In general, it was found that P_{CAV}<0.2 atm at room temperature is sufficient to avoid plastic deformation of small plates for temperatures of up to 1000°C. However, it should be noted that

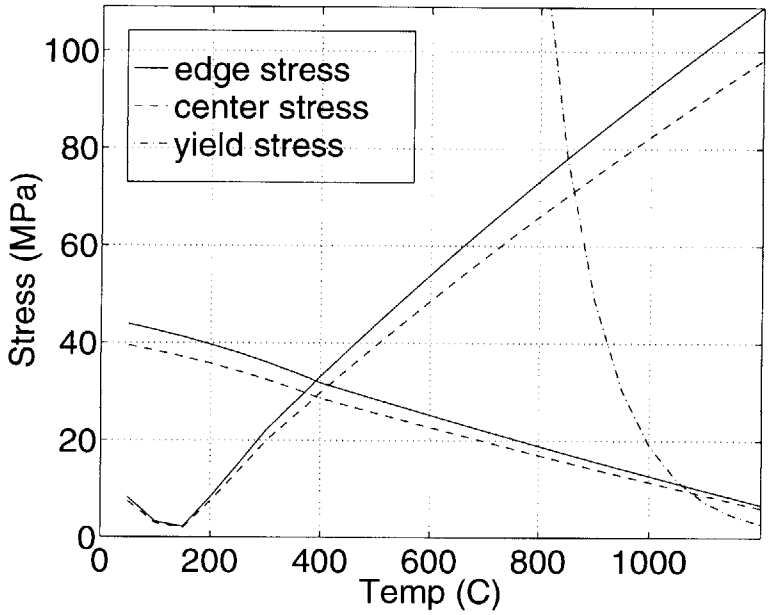


Figure 4-6: Stress vs. temperature for small circular plate, a=300μm, h=10μm, L=2μm

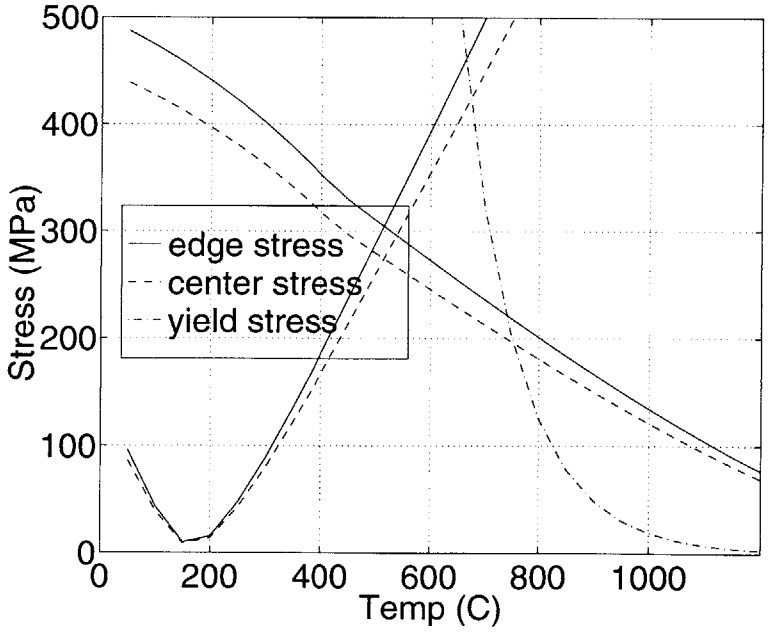


Figure 4-7: Stress vs. temperature for large circular plate, a=1000μm, h=10μm, L=20μm

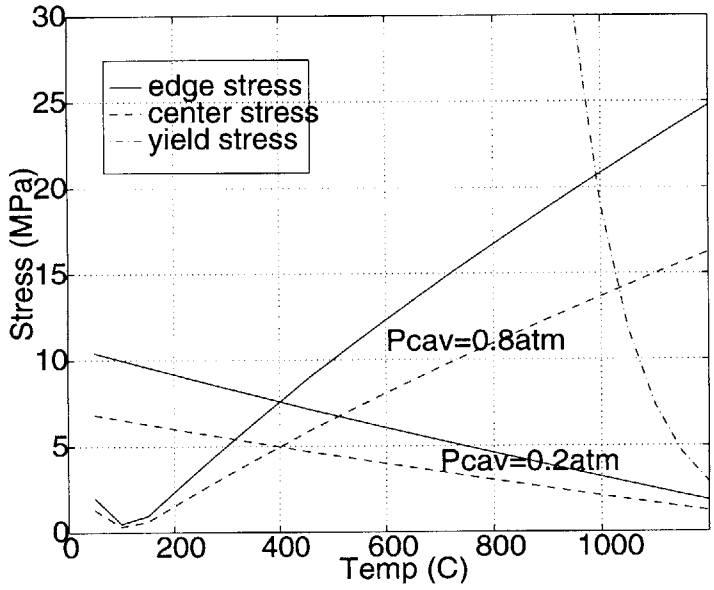


Figure 4-8: Stress vs. temperature for small square plate, side=600μm, h=10μm, L=2μm

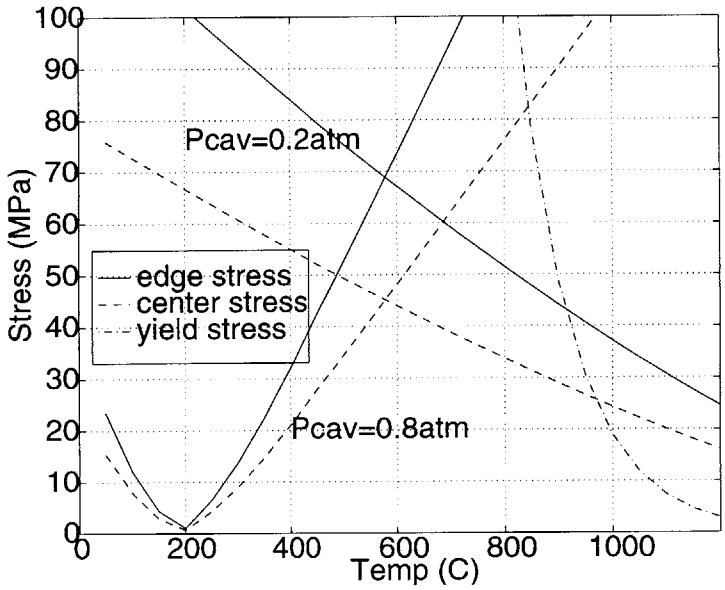


Figure 4-9: Stress vs. temperature for large square plate, side=2000μm, h=10μm, L=20μm

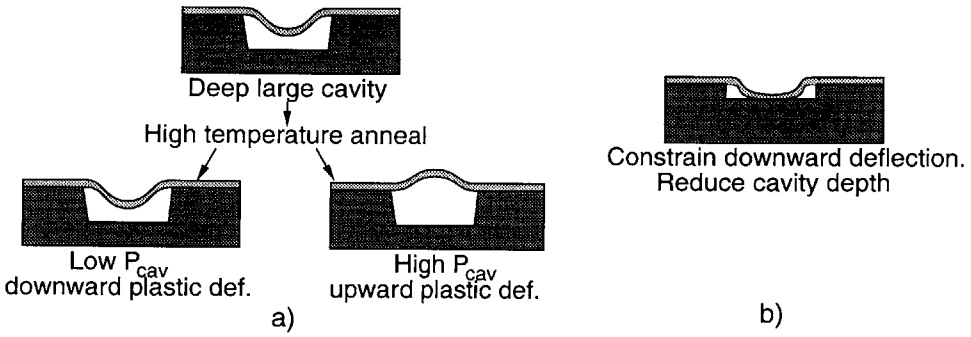


Figure 4-10: Controlled ambient bonding for varying cavity depths.

permanent deformation in the downward direction can occur in plates over deep large cavities at low residual pressures, as indicated in figures 4-7 and 4-9. For a circular plate with L=20μm, a cavity pressure of 0.8 atm gives a temperature limit of 650°C, but reducing P_{CAV} to 0.2 atm results in downward load large enough to exceed the yield stress at a temperature of 750°C. Excessive downward deflection should therefore be avoided by limiting the deflection with a smaller cavity depth, and the behaviour of such structures is discussed in section 4.3.1.

4.3.1 Constrained deflections

The previously described model is useful in obtaining limits for the geometries of plates that will have to withstand high temperature process steps. The calculations indicate that plates over deep cavities can plastically deform in the downward direction under low cavity pressures. This may be addressed by reducing the cavity depth, resulting in structures with the deflection shape shown in figure 4-10b, where the downward deflection of the plate is constrained against the bottom of the cavity. Such structures can experience high bending stresses at points of locally small radius of curvature. It is of interest to see if these stresses will result in the formation of dislocations, and thus plastic deformation at these points.

In order to model circular plates with this bending shape, finite element simulations (using abaqus [85]) are utilized instead of the analytical equations for touched-down plates as given in chapter 2. This is done in order to more accurately account for the boundary conditions on the plate, which are not fully clamped as assumed in the equations. The modification of the boundary to account for the physical structure results in the edge of the plate being rotationally compliant as compared

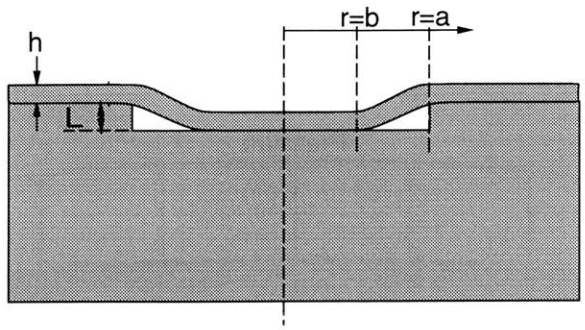
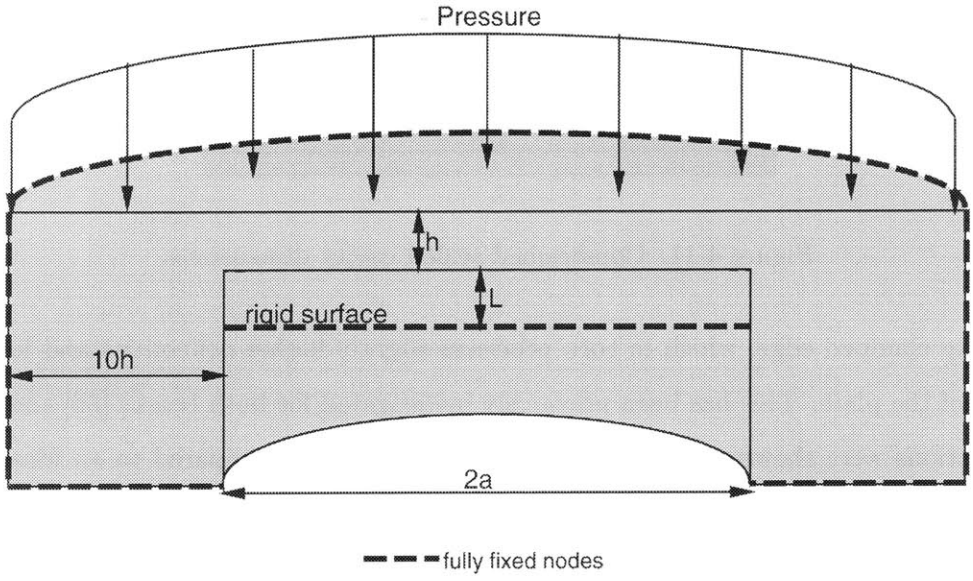


Figure 4-11: Constrained sealed cavity dimensions.

to a perfectly clamped edge, which in turn produces slightly higher deflections and lower stresses at the edge of the plate. This has been previously investigated for both beams [86] and plates [87], where deflections were shown to increase by as much as 30% as compared to an ideally clamped edge. The FEM model of the plate and support utilized to simulate plate stresses is shown in figure 4-12b. In this case, the support is included in the structure, and the clamped nodes have been moved away from the plate edge. The width of the rim is set to 10x the plate thickness. The boundary conditions are fully fixed along the outside edge and base of the support, and the load is applied over the top of the entire structure. Figure 4-12a shows the placement of the fixed nodes in the simulations. Both circular and square plates utilize a quarter-plate model, with 8-node solid elements, in two layers on the plate and one layer for the support rim. The base of the cavity is modeled as a rigid surface and reduced integration elements have been used. The relevant dimensions are defined in figure 4-11.

The stress distribution for a representative plate of radius a=1000μm and a vacuum in the cavity is shown in figure 4-13. There are high stress regions at the edge of the plate (r=a) and at a point near the touchdown radius (r=b).

In figure 4-14 the maximum von Mises stresses at the plate edge r=a and touchdown radius r=b are plotted for a range of radii and thicknesses, at an initial cavity pressure of vacuum. Each curve has two distinct regions - in the first region σ is proportional to $(a/h)^2$ and represents the plate before it has "bottomed-out" on the base of the cavity. Beyond this point the plate deflection is constrained against the cavity base. The dividing line between plates that will and will not experience plastic deformation is dependent on the yield stress at the desired maximum temperature limit, and points on the curves above this stress value will therefore experience defect formation. The plot shows



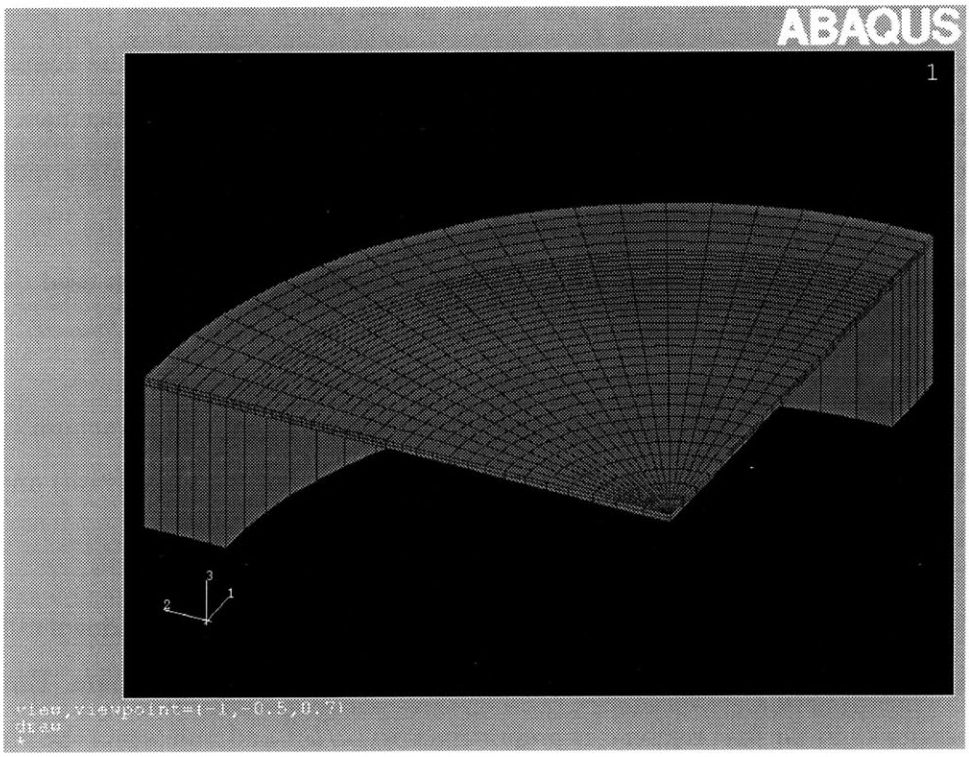


Figure 4-12: FEM model for simulations. a)location of clamped nodes, b)mesh for circular plate, quarter plate model.

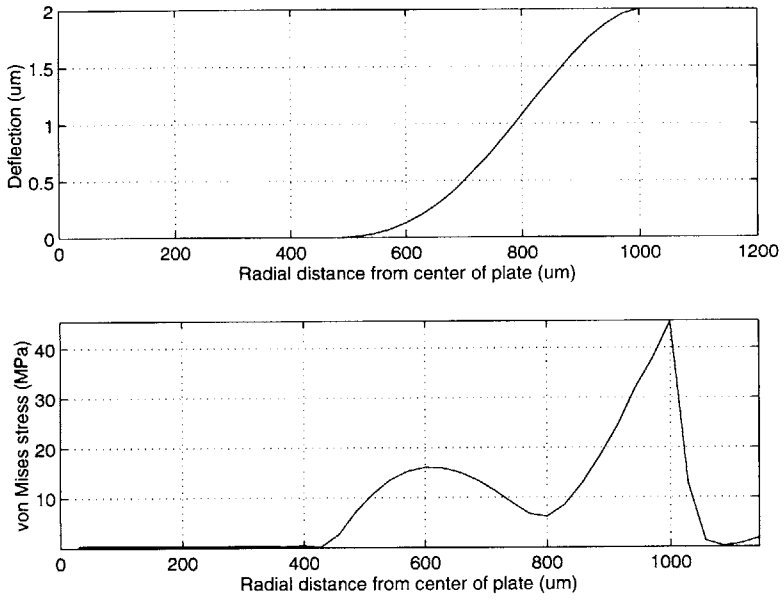


Figure 4-13: Deflection and stress in constrained circular plate, a=1000μm, h=11um L=2μm, P_{CAV}=vacuum.

that when cavity pressure is vacuum, stresses at both the edge as well as the touchdown radius will exceed the yield stress for an example of $T_{max} = 1000°C$ with $\sigma_{yield} = 18MPa$. However, when cavity pressure is increased to 0.2 atmospheres (fig: 4-16), gas expansion during heating is sufficient to reduce plate deflection without excessively deforming the plate upwards, so that stress levels are kept below the yield point. Similar results are obtained with square plates, as indicated in figures 4-18 and 4-20.

4.4 Experimental evidence of defects

As a confirmation of the model for the behaviour of plates with constrained deflections, a set of plates was fabricated and annealed at various temperatures and under different ambients. Table 4.1 gives a summary of the annealing conditions for each set of structures.

Defects are delineated by etching in Secco etchant (a mixture of HF and $K_2Cr_2O_7$)[88]. The common feature in all of the large plates is the presence of a ring of defects corresponding approximately to the touchdown radius of the plate. Figures 4-15 and 4-19 show plates with a nominal cavity pressure of vacuum that have been oxidized at 1000°C. When etched in Secco etchant the dislocations are

Wafer	Process cycle
1	field oxidation: wet SiO_2 1000°C
2	n-well: phosphorus implant + anneal
3	p-well: boron implant + anneal
4	LOCOS: dry SiO_2 950°C+ LPCVD Si_3N_4
5	field oxidation: wet SiO_2 1000°C

Table 4.1: Constrained plates - annealing conditions.

clearly indicated by a ring at the touchdown radius. These plates correspond to the plots in figures 4-14 and 4-18, where the stress at the given plate radius/length is close to or exceeds the yield stress. Conversely, by increasing the cavity gas pressure the defect formation is eliminated, as indicated in figures 4-17 and 4-21. Note that the pressure in the cavity was not a perfect vacuum but was estimated to be no greater than 100 mTorr. Thus the location of the defect ring corresponds to the touchdown radius at the elevated temperature, which is smaller than that at room temperature.

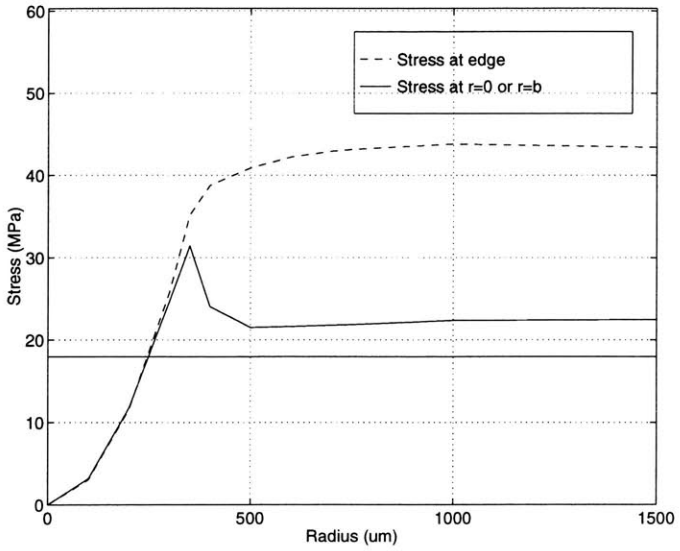


Figure 4-14: σ vs. radius for constrained circular plate: h=11μm L=2μm P_{CAV}=vacuum.

Figure 4-15: Plate from wafer 2 (P implant+anneal), a=1000μm, h=11μm, L=2μm, P_{CAV}=vacuum. Note defect ring at r_b, the touchdown radius. r_b at 1000°C is less than r_b at room temperature because P_{CAV} is non-zero.

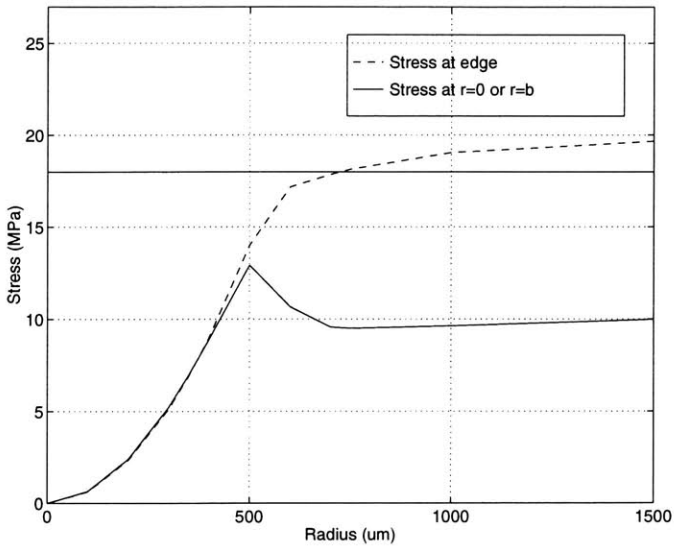


Figure 4-16: σ vs. radius for constrained circular plate: h=11μm L=2μm P_{CAV}=0.2 atm.

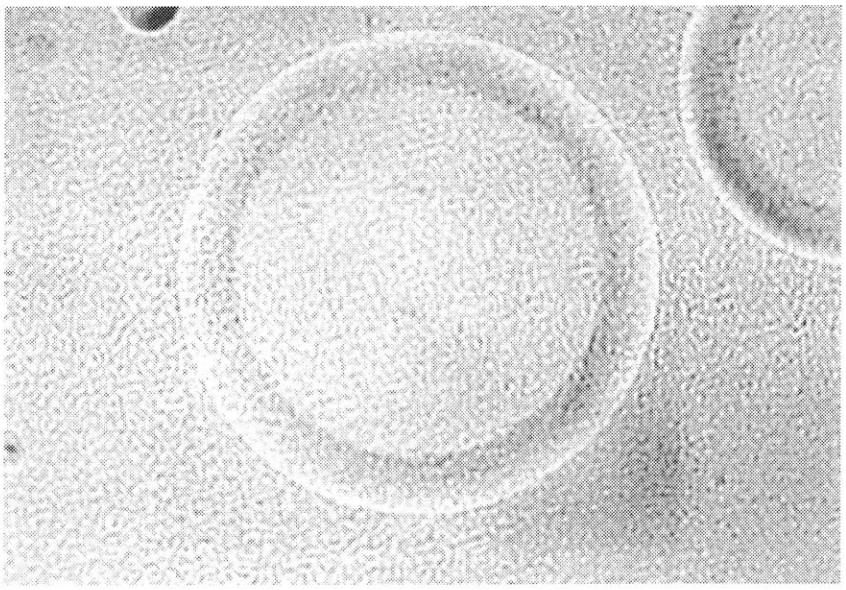


Figure 4-17: Plate from wafer 5 (field oxidation), a=1000μm, h=11μm, L=2μm, P_{CAV}=0.2 atm. Note absence of defects.

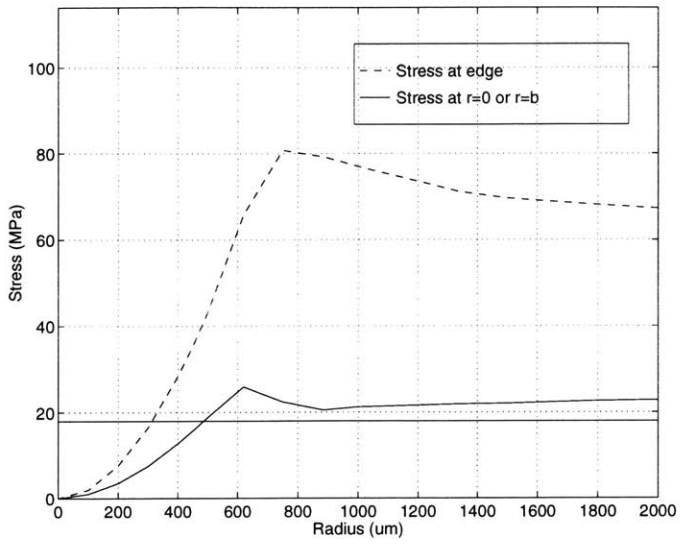


Figure 4-18: σ vs. radius for constrained square plate: h=11μm L=2μm P_{CAV}=vacuum.

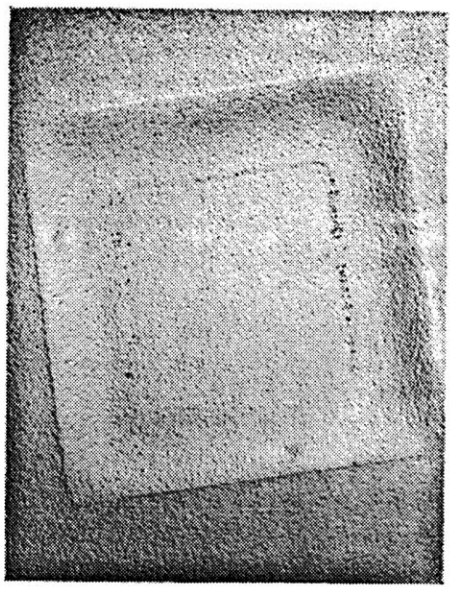


Figure 4-19: Plate from wafer 1 (field oxidation), side=1772μm, h=11μm, L=2μm, P_{CAV}=vacuum. Note ring of defects.

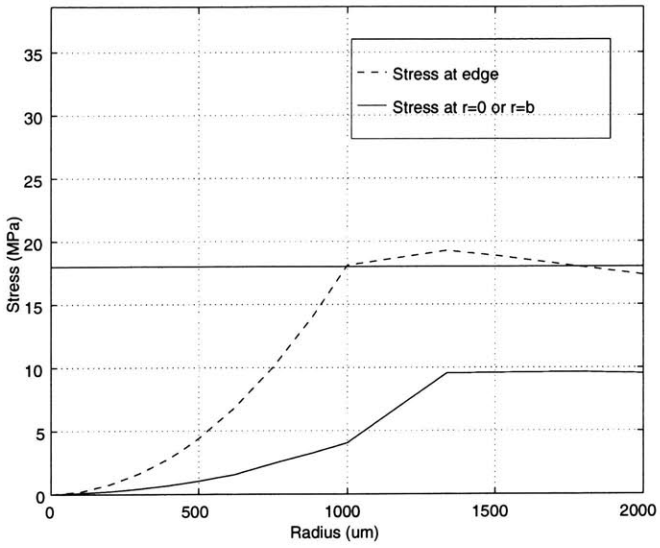


Figure 4-20: σ vs. radius for square plate: h=11μm, L=2μm, P_{CAV}=0.2 atm.

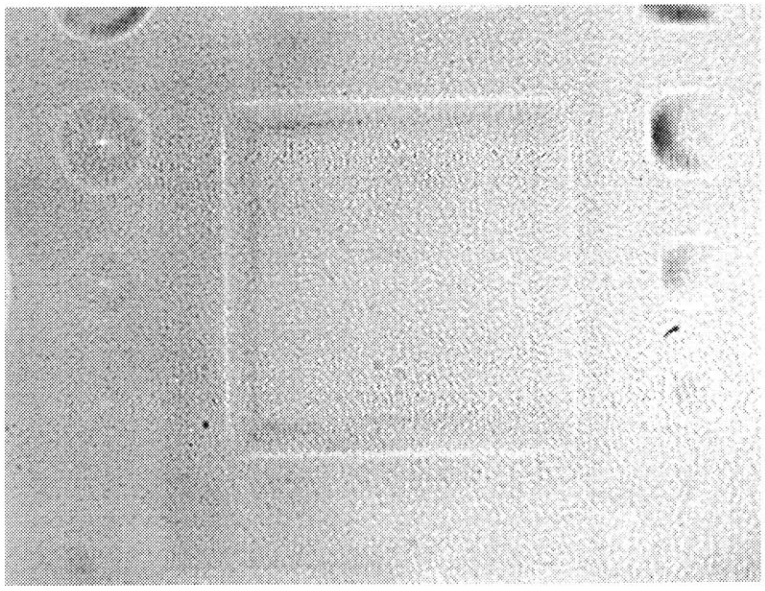


Figure 4-21: Plate from wafer 5 (field oxidation), side=1772μm, h=11μm, L=2μm, P_{CAV}=0.2 atm. No defects visible.

Figure 4-22 shows SEM images of the etch pits on the surface of the plate. Note that the pits take one of two shapes, oval indicating a dislocation oriented perpendicular to the surface and propagating through the plate, and teardrop shaped, indicating one inclined at 60° to the horizontal. The elongated pits are pointed in the <110> directions, as expected since this is the principal slip direction. The remaining photographs show other plates taken from the wafers listed in the table. There are varying levels of defect densities, with phosphorus doped samples (fig. 4-23 to 4-25) showing the highest density. 4-27). The boron doped plates (fig. 4-28) show a wide band of slip lines around the touchdown perimeter. and plates with a nitride-oxide layer present during the anneal (fig. 4-26) have a fairly well-delineated but narrow strip of defects.

Although the simulated stresses at the edge of the plate are high, the apparent complete lack of dislocation formation is notable and may be explained by the fact that the bonded interface under the edge of the plate plays some role in acting as a "sink" for the dislocations, whereas the defects at the touchdown radius have no such interface underneath them. Another point to note is that stresses at the edge of the plate are tensile whereas those in the center are compressive, and this difference in sign may play a role in the onset of yielding.

As a final added observation, figure 4-29 shows a plate (from wafer 4) that has been bonded to a central pedestal of silicon with a diameter of 20μm. Note the extremely high contentration of dislocations at this point, again indicative of high stresses caused by what is effectively a point load at the center of the plate. Also present are two rings, corresponding to the bending of the plate down to and back up from the base of the cavity. If such a structure is to be fabricated, some care must be taken to maintain a sufficient gas pressure inside the cavity during processing.

Dopants have a significant effect on dislocation mobility, as evidenced by the widely varying densities in the photos. In particular, donors (P, As, Sb) enhance mobility, whereas acceptors (B) do not have much of an effect. In addition, dislocations are immobilized by impurities such as oxygen, nitrogen and phosphorus. Phosphorus has a complicated effect on mobility, in that it increases the upper yield stress but decreases the lower yield (flow) stress. Implantation of phosphorus has been shown to result in high defect densities at localized high stress regions, as evidenced by emitter edge defects around film edges over phosphorus implants [75]. These facts can explain the high density shown by phosphorus-implanted samples, in which dislocations nucleated by the implantation glide

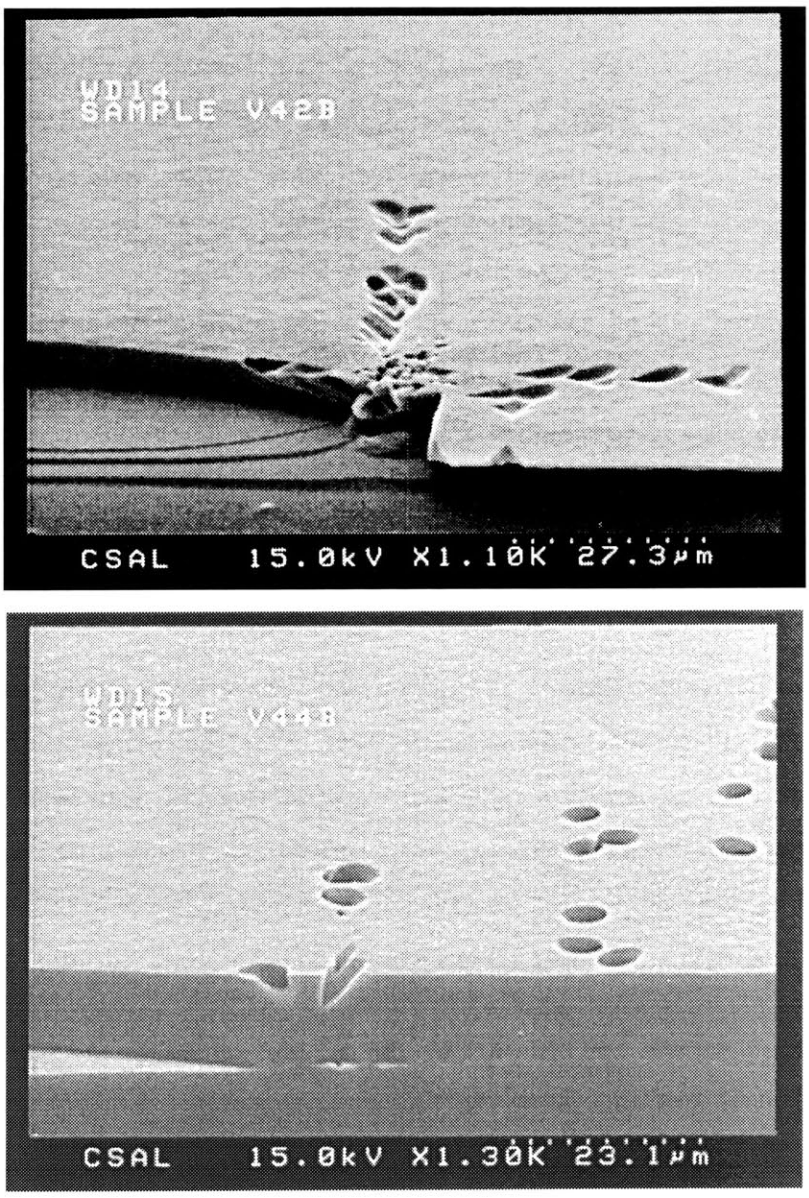


Figure 4-22: SEM of etch pits in plastically deformed plate.

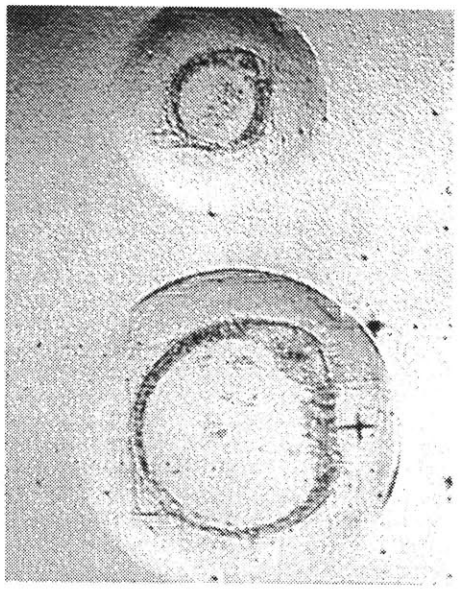


Figure 4-23: Plate from wafer 2 (P implant+anneal), a=750,500μm, h=11μm, L=2μm, P_{CAV}=vacuum. Note heavy dislocation density at touchdown perimeter.

Figure 4-24: Plate from wafer 2 (P implant+anneal), a=350, 300, 250μm, h=11μm, L=2μm, P_{CAV}=vacuum. No defects visible.

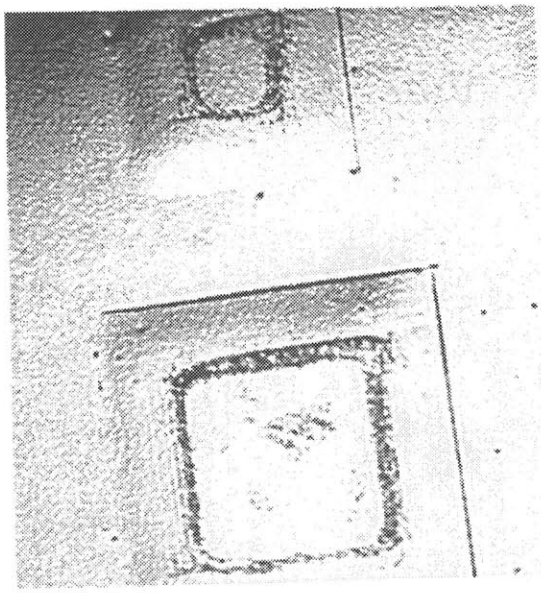


Figure 4-25: Plate from wafer 2 (P implant+anneal), side=1339, 886μm, h=11μm, L=2μm, P_{CAV}=vacuum. Heavy defect density at touchdown perimeter.

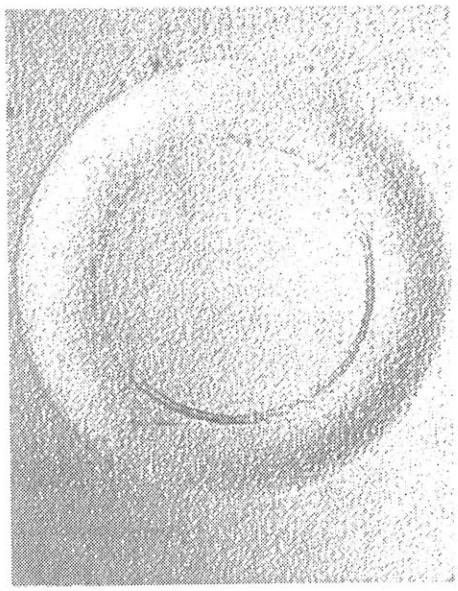


Figure 4-26: Plate from wafer 4 (LOCOS:oxide+nitride), a=1000μm, h=11μm, L=2μm, P_{CAV}=vacuum.

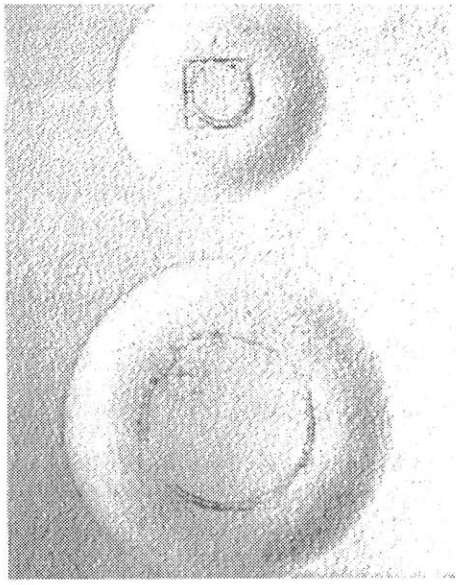


Figure 4-27: Plate from wafer 4 (LOCOS:oxide+nitride), a=750,500μm, h=11μm, L=2μm, P_{CAV}=vacuum.

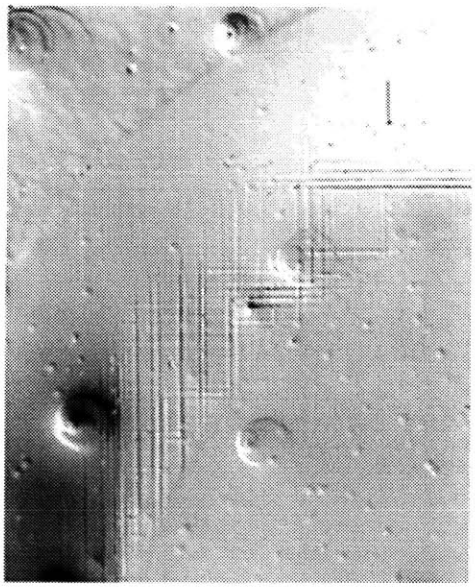


Figure 4-28: Plate from wafer 3 (B implant+anneal), a=1000μm, h=11μm, L=2μm, P_{CAV}=vacuum. Closeup, edge of plate.

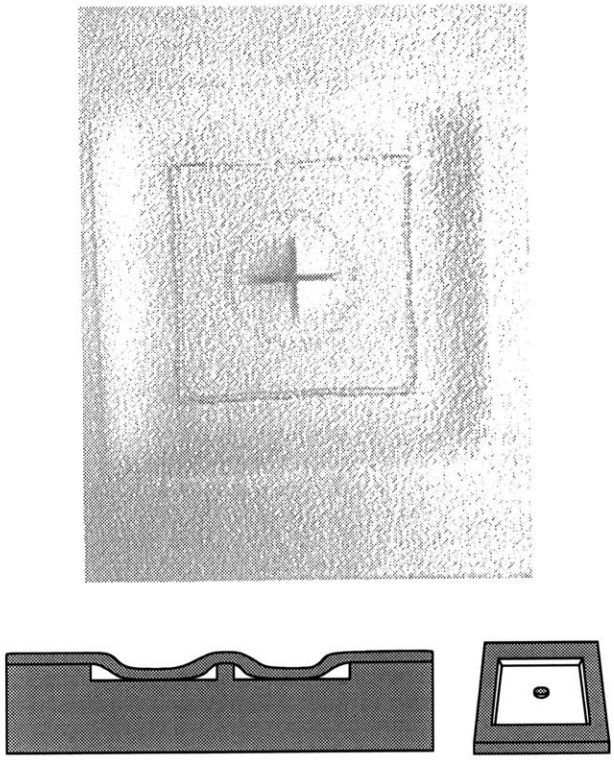


Figure 4-29: Plate from wafer 4 (LOCOS:oxide+nitride), square plate with central pedestal, side=1772μm, h=11μm, L=2μm, P_{CAV}=vacuum. b)Plate geometry.

under the influence of stress and come to rest at the highest stress points, in this case at the touchdown radius. It should be possible to reduce the density by utilizing a liquid source for the phosphorus, instead of implanting. Plates with nitride-oxide layers as used for a field isolation process also displayed well-defined and localized rings of dislocations as compared to those with only an oxide. The added interfacial strain between the nitride film, which has an intrinsic tensile stress, and the remainder of the plate may enhance the mobility of dislocations already nucleated by the shear stress from bending. This would provide an added driving force for them to migrate to the highest stress points on the deformed plate. The surface finish also plays a role in dislocation nucleation, and scratches are usually the source of defects. The samples in the experiments were prepared using electrochemistry, therefore the surface roughness was approximately 100Å; however the etching may actually help to smooth the surface of any scratches.

The preceding results have been incorporated into a simulation program that can be used to calculate maximum stresses as a function of temperature for circular and square plates of any geometry, as well as predict the onset temperature of plastic deformation. The FEM data are used to obtain a relationship for $\sigma = f(a, h, P_{CAV})$ in the touched-down regime by least squares fitting of the simulated stress. For the pre-touch down region the analytical solution is used with a prefactor to account for the modified boundary conditions. The program is included in its entirety in appendix E.

Although extensive plastic deformation does cause significant warpage and changes the plate geometry, the presence of the ring of dislocations in constrained plates may not have a significant impact on the mechanical behaviour of any structures fabricated from the plates. However, they will affect the performance of any electrically active junctions placed at those locations (piezoresistors for example), and may also affect the reliability especially for resonating beams that cross the defective area. Additionally, if there is significant defect formation, there will also be an associated warpage of the plate. Thus the ability to predict plastic deformation in arbitrarily sized structures is vital to obtaining reliable MEMS devices using the sealed cavity process. As a final practical point of note, it may not be possible to construct cavities of widely varying dimensions all on the same substrate, since each may require a specific cavity pressure to stay within the bounds prescribed by the model. This fact should be taken into account when designing arrays of cavities of various sizes, for applications such as pressure sensors for example.

The plastic deformation analysis was used to construct devices within the safe bounds calculated by the program, and the integrated MEMSCMOS process exercised in their fabrication. The following two chapters give characterization results of these devices.

Chapter 5

MEMSCMOS Process Verification

The MEMSCMOS process described in chapter 3 was demonstrated with the completion of 3 sets of wafers, hereafter referred to as MEMSCMOS1, 2 and 3. The first two lots were composed of a set of test structures to be described in section 5.1, and the third lot contained an integrated capacitive pressure sensor system. In addition, the capacitive pressure sensor was fabricated and tested in a discrete form, with these devices also being used in a hybrid version of the sensor-circuit system. Finally, the sealed cavity section of the process was utilized to fabricate a simple piezoresistive pressure sensor at Motorola's facilities. This chapter presents test results from lots MEMSCMOS1 and 2, for characterization and verification of process compatibility of the circuit and sensor processes. Test results from the pressure sensors are discussed in the next chapter.

5.1 Testchip description

The testchip used for process verification is shown in figure 5-1. The bonded layer for these test wafers was 11μm of arsenic doped epitaxial silicon, electrochemically thinned. The accompanying block diagram indicates the types of devices included, which can be divided into two categories, electrical and mechanical test structures. Electrical test structures primarily consisted of a set of discrete nMOS and pMOS transistors ranging in size from 20x1.5μm to 70x70μm. Mechanical test structures included a set of single crystal silicon beams (cantilever and double-end clamped), a set of piezoresistive pressure sensors, and an accelerometer proof mass with plate dimensions of 500x500μm.

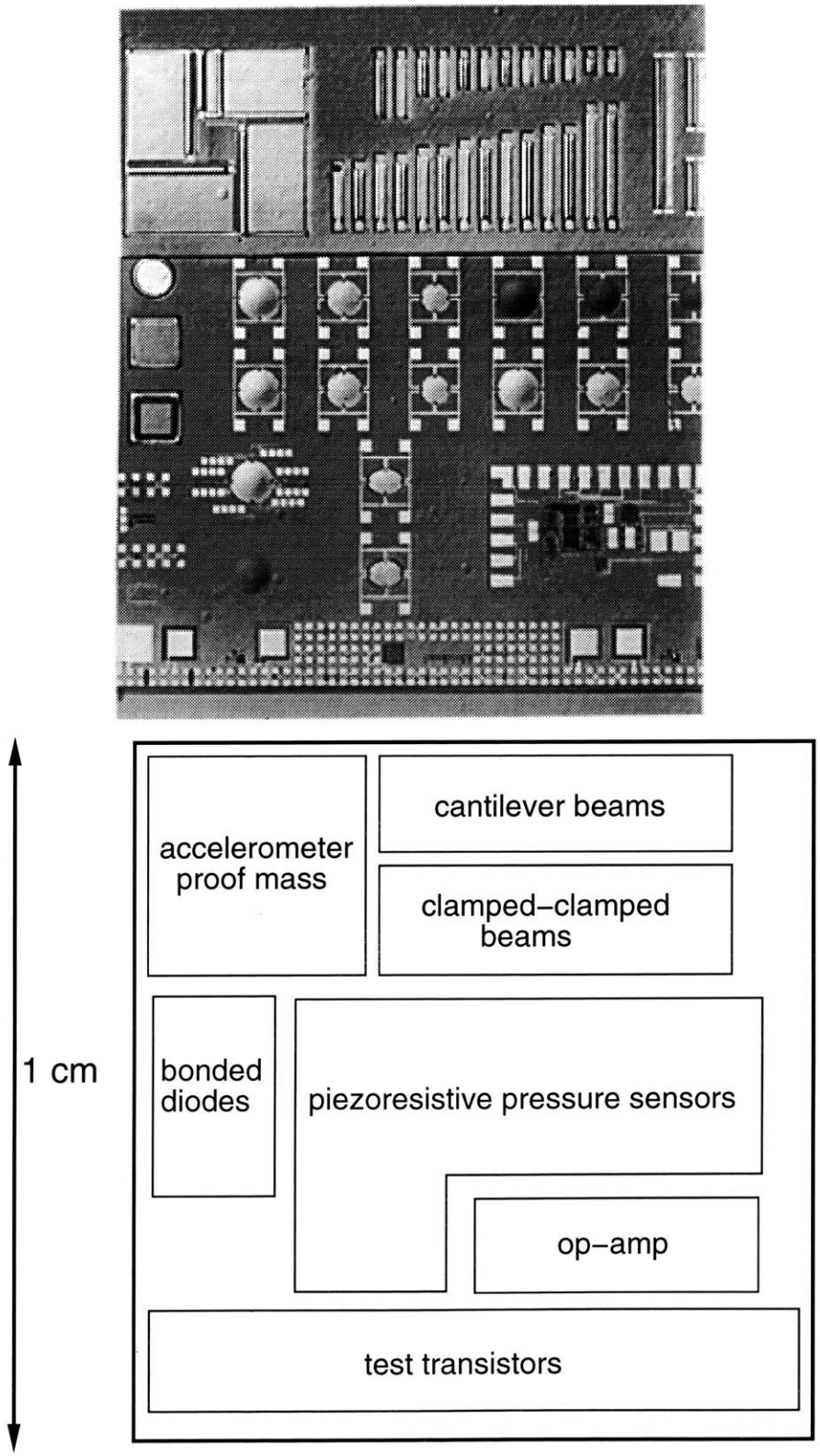


Figure 5-1: Layout and photograph of completed MEMSCMOS testchip.

Lot	Substrate	V_{T_n}	V_{T_p}
MEMSCMOS1	bonded wafer	0.68±0.054	-1.00±0.031
MEMSCMOS1	control wafer	0.71±0.044	-0.98±0.069
MEMSCMOS2	bonded wafer	0.654±0.022	-0.984±0.019
MEMSCMOS2	control wafer	0.633±0.038	-0.995±0.014

Table 5.1: Average threshold voltages for nMOS and pMOS devices

5.2 Electrical device characterization

In order to confirm the integrity of the electrical test structures after the post-IC micromachining steps, a non-bonded control substrate was processed simultaneously with the bonded substrates. This control wafer was a conventional p-epi on p++ substrate, and was not subjected to any of the micromachining steps.

Typical transistor characteristics were measured for both bonded and non-bonded substrates and representative curves are shown in figures 5-2 to 5-3. Discrepancies in $I_{d_{sat}}$ are due to a difference in gate oxide thickness (bonded wafer t_{ox}=219Å, control wafer t_{ox}=232Å). Table 5.1 compares threshold voltages, averaged across 85 devices on a wafer for both lots. Leakage currents were low (less than $25\mu A/cm^2$), as expected since the active device area is well above the bonded interface.

5.3 Mechanical tests

The silicon plates were robust, with an overall yield on the sealed cavity wafers after the CMOS process of greater than 98%, with breakage occurring only on one isolated die at the wafer edge. As discussed in chapter 4, the plates can be designed to avoid plastic deformation by controlling the residual pressure and geometry. There are a number of ways in which to check for the occurrence of plastic deformation - the defect etch, also previously discussed, is a destructive test; visual inspection in an interferometric microscope can indicate warpage in released plates as well as the presence of slip lines; the third method is the measurement of pull-in voltage for suspended dielectrically isolated structures [89]. Mechanical properties of the bonded silicon layer were investigated by

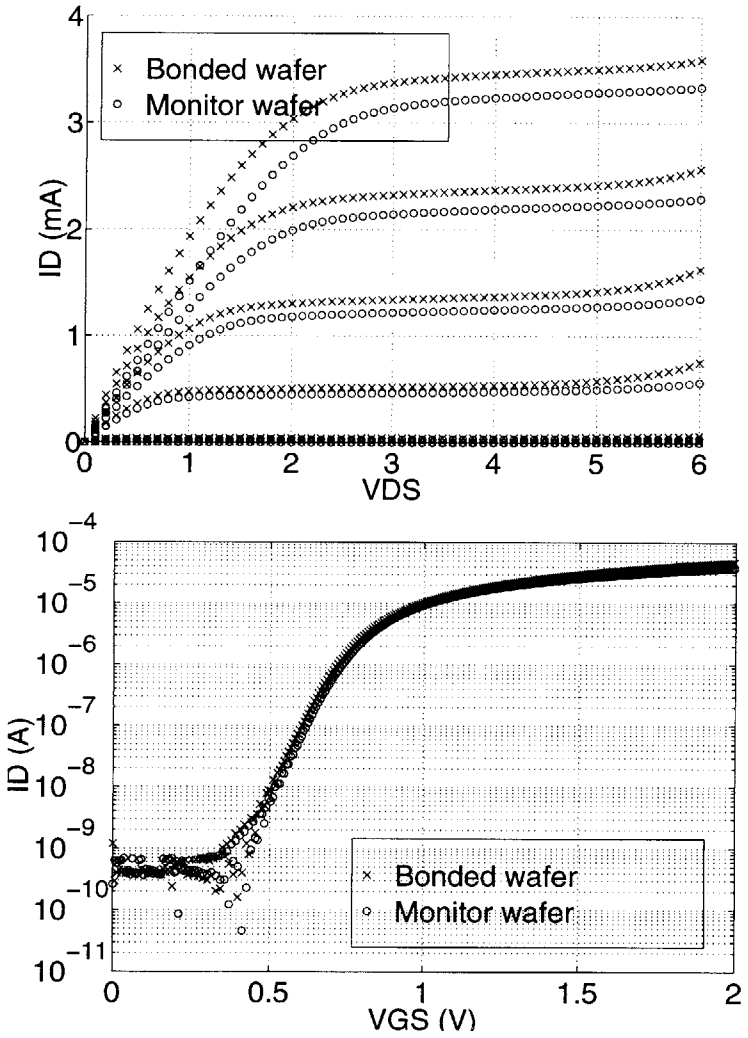


Figure 5-2: Representative nMOS transistor characteristics from lot MEMSCMOS1. W/L=20/2

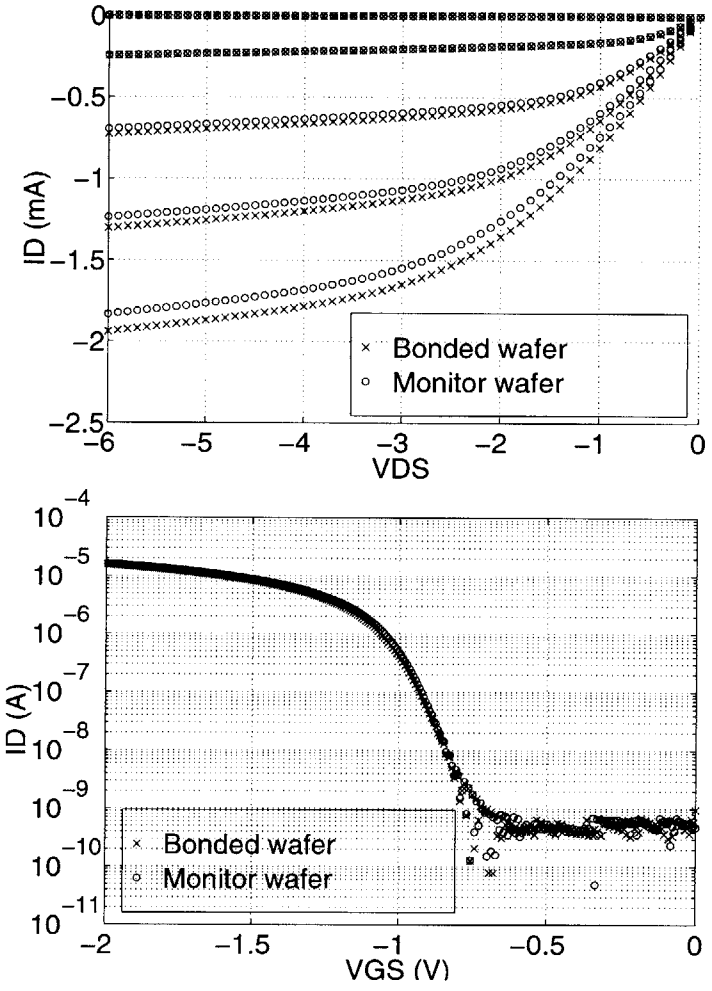


Figure 5-3: Representative pMOS transistor characteristics from lot MEMSCMOS1. W/L=20/2

means of this measurement on the set of cantilever beams. The pull-in test consists of applying a increasing voltage between the suspended beam and the substrate until the beam is pulled into the substrate, which is detected by the onset of current flow between the two electrodes. The pull-in voltage is a function of the beam geometry and material properties (Young's modulus and residual stress) of the beam. With a suitable substrate configuration (fig. 5-4a), comparison of the measured pull-in voltage can be used to determine the Young's modulus of the silicon, and in the case of the clamped-clamped beams, also gives a measure of the residual stress in the bonded layer. To obtain the dielectrically isolated beams required for this test, the sealed-cavity substrates were initially fabricated using an oxidized handle wafer with the cavity defined by selective removal of the oxide, and the active substrate was a bonded SOI wafer (see fig. 3-2c).

Figure 5-4a shows measured pull-in voltages for a range of cantilever beams, superimposed on a curve with calculated values for the same structures, and figure 5-4b is an analogous plot for clamped-clamped beams. The error bars indicate the standard deviation of measured voltages for a set of beams of the given size. The spread in the data stems from the non-optimal cross-section of the beam, caused by the plasma etch used to form them [90]. This changes the electric field and therefore the pull-in voltage. The calculated curves are obtained by solving the electromechanical equations for the beam with the assumptions of a modulus of 160 GPa and no residual stress, and the good matching between data and theory in figure 5-4b is an indication that the residual stress level in the bonded layer is low.

The fabrication of the accelerometer proof mass (dimensions of 500x500μm) [72] demonstrates the ability to make large plates without warpage, as shown by measurements of the flatness of the plate using a Wyko non-contact interferometric surface profilometer [91] (fig. 5-5). By observing the fringe pattern it can be inferred that there is no measureable curvature or warpage present in the plate, and consequently no stress gradient through the thickness of the plate. The Wyko plot indicates that the nonuniformity is less than the surface roughness of $\approx$100Å. Thus it has been confirmed that the silicon plate has undergone no permanent deformation from the CMOS thermal cycles, as expected from calculations for stress using the given dimensions (see sec. 4.3.1).

Also present on the testchip were a set of piezoresistive pressure sensors. Lot MEMSCMOS1 contained absolute sensors without the backside pressure inlet hole (fig. 5-6); thus the plates were

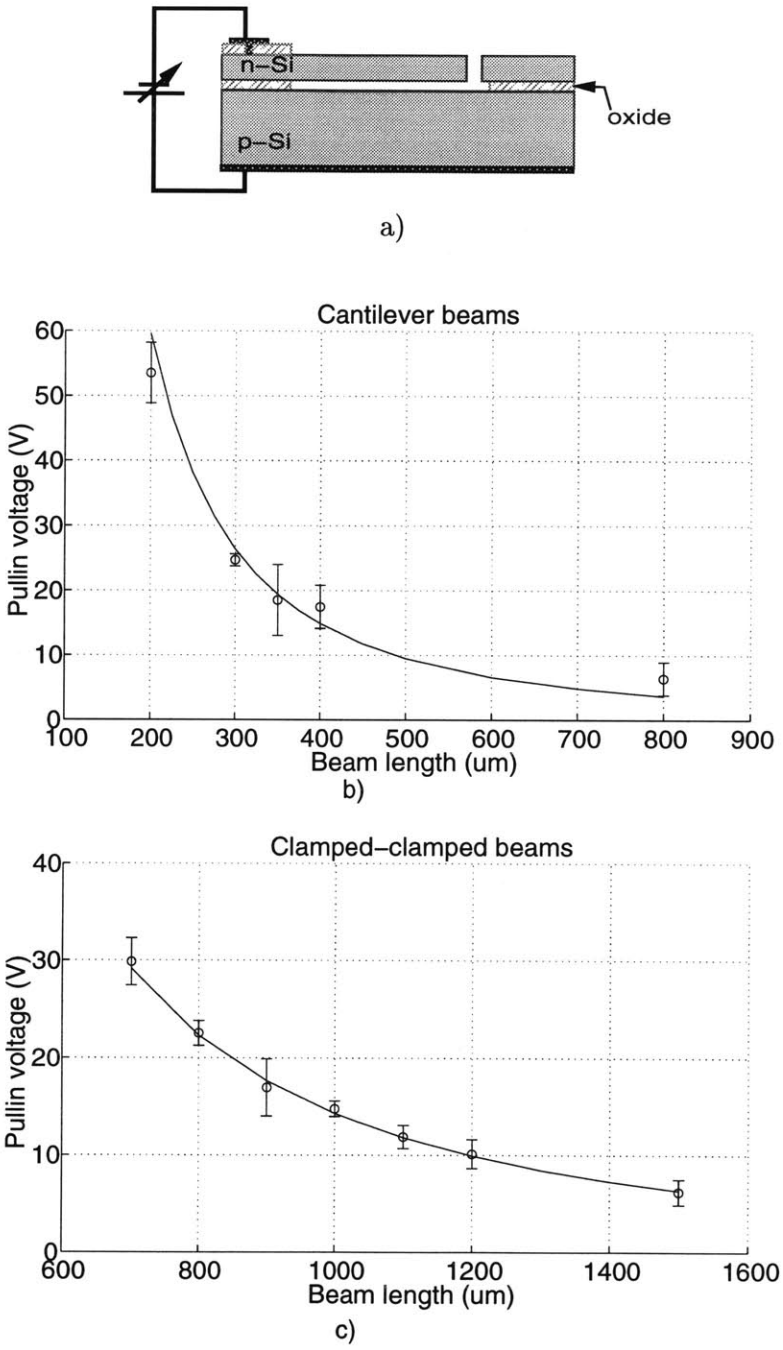


Figure 5-4: Pull-in test for beams. a)Test structure. Measured pull-in voltage for b)cantilever beams, c)clamped-clamped beams. Beam width=50μm thickness=10μm. Each data point is average of 13 devices. Solid line is theoretical value.

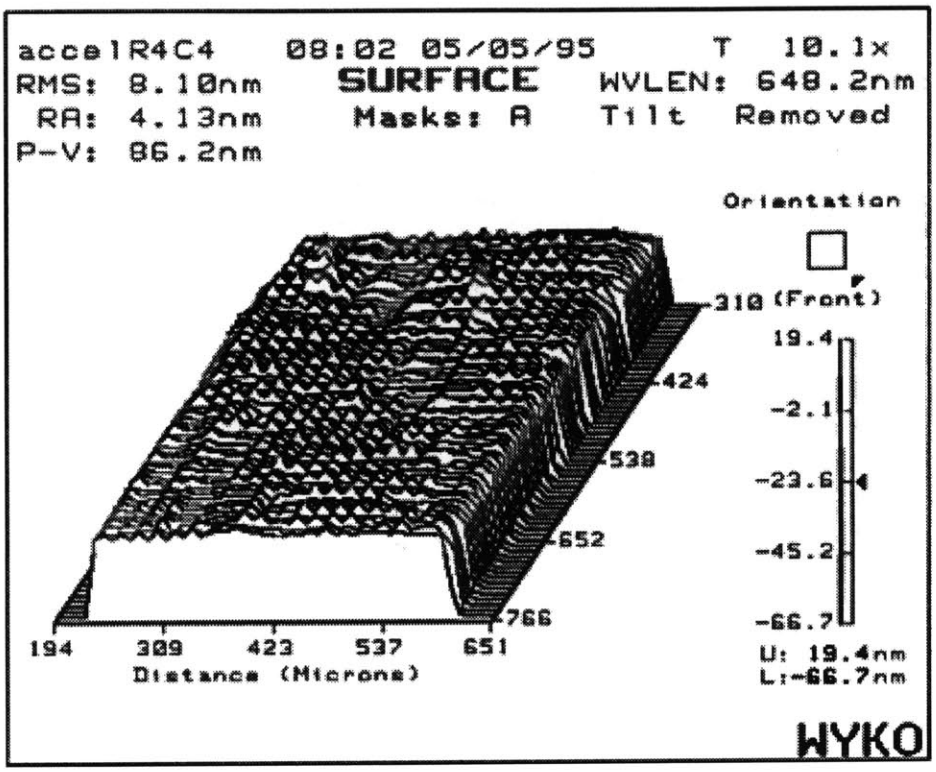


Figure 5-5: Surface map of accelerometer proof mass. Dimensions: side=500μm, thickness=10μm

nominally under a load of 1 atmosphere. Testing was done by placing the devices in a vacuum chamber and measuring the response as the chamber was pumped down to pressures below 1 atmosphere. The sensors had three radii: 200, 250 and 300μm and the bridge output voltage with a 5V DC source, is shown in figure 5-7a, for typical devices of each size. The calculated curves were obtained using closed form solutions for the deflection and stress, and gauge factors of $\pi_l = 16.5 \times 10^{-11}$/Pa and $\pi_t = -15.2 \times 10^{-11}$/Pa for heavily boron doped silicon [92] (σ taken at r=a-15μm, location of piezoresistor). The devices showed good agreement with the calculated response.

The second MEMSCMOS test lot incorporated the backside inlet port etch step, and the devices were mounted on plexiglass base with pressure applied via a compressed nitrogen source to obtain the results shown in figure 5-8. Again, there is good agreement between theory and experiment, as well as low nonlinearity (3%, 0.6% and 6% of fullscale for r=200, 250, 300μm respectively).

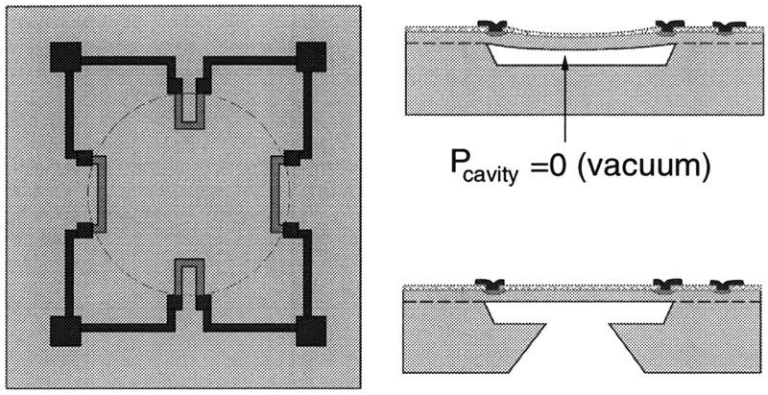


Figure 5-6: Piezoresistive pressure sensor.

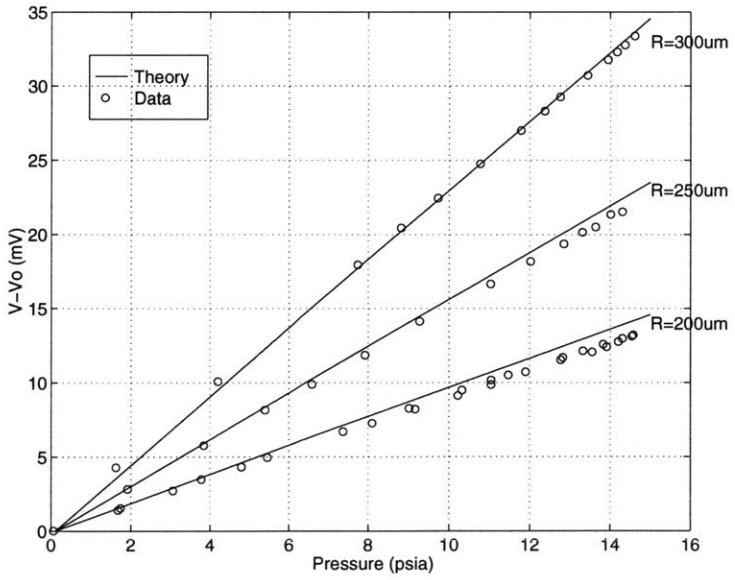


Figure 5-7: Piezoresistive absolute pressure sensors: pressure response.

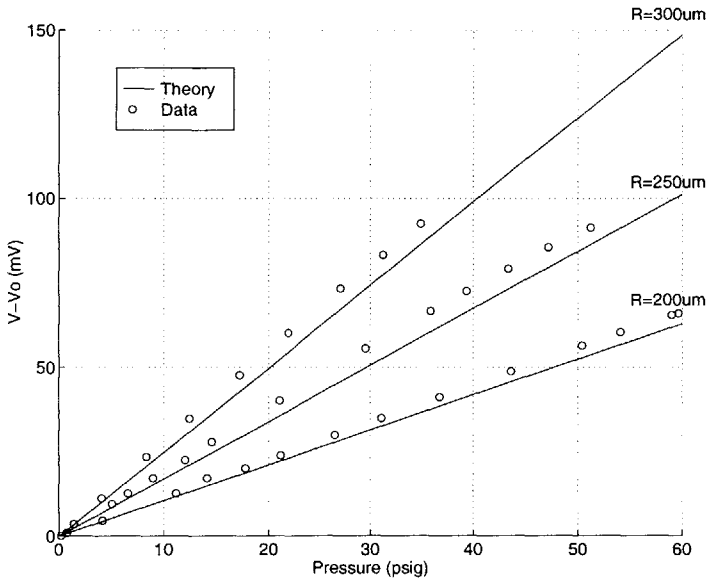


Figure 5-8: Piezoresistive differential pressure sensors: pressure respone.

5.4 Motorola sealed cavity piezoresistive pressure sensor

To demonstrate the ease with which the sealed cavity process can be used in a conventional circuit foundry, it was utilized to construct a simple piezoresistive pressure sensor in one of Motorola's bipolar transistor production lines located in Phoenix AZ. Front-end micromachining (sealed cavity formation) was done at MIT, after which the substrated were processed in a production bipolar line for placement of piezoresistors, passivation and metallization. Test results are given in chapter 6; however of note is the fact that the sealed cavity substrates posed no difficulties in processing in the IC line.

This chapter has summarized the results of characterization of test lots used to exercise the MEMSCMOS integrated sensor process. Results indicate that plastic deformation did not occur in suspended structures and that the post-IC micromachining did not affect transistor performance. The next chapter contains results from testing of capacitive pressure sensors, both in discrete device tests as well as in combination with a calibration system described in [49].

Chapter 6

Pressure sensor testing

This chapter contains test results from two types of devices. The first section contains a discussion of the piezoresistive pressure sensor fabricated in collaboration with Motorola, the purpose of which was to demonstrate the viability of processing sealed cavities in a commercial IC foundry. The remainder of the chapter is concerned with the capacitive pressure sensor, and test results are given for discrete devices as well as the performance of the sensor in conjunction with a calibration system, attached to the sensor in both hybrid and integrated form.

6.1 Motorola sealed cavity piezoresistive pressure sensor

The sealed cavity process was utilized to construct a simple piezoresistive pressure sensor in one of Motorola's bipolar transistor production facilities located in Phoenix AZ. The device is shown schematically in figure 5-6. Front-end micromachining (sealed cavity formation) was done at MIT, after which the substrates were sent to Motorola to be completed and tested.

Devices were square (side length=525μm) or circular (diameter=525μm) with plate thickness of 11μm, and a cavity depth of 2μm. The mask layouts are given in appendix F, along with the resistor process parameters. Three sets of tests were carried out using the automated test equipment at Motorola, these being pressure tests at moderate pressures, over temperature, and at high pressure (overpressure) conditions. The shift in slope in figure 6-1 is assumed to be entirely due to the temperature dependence of the gauge factor. The no-load offset at room temperature is

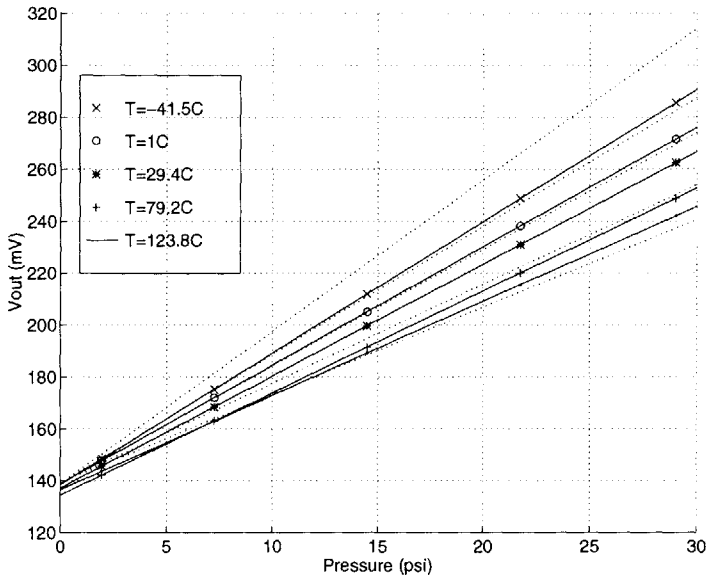


Figure 6-1: Motorola piezoresistive pressure sensor - pressure response of circular plate over temperature. Solid lines and symbols are data, dotted lines are calculated (see app.G).

approximately 143mV due to the initial downward deflection of the plate, and the room temperature offset decrease with temperature is caused by expansion of the small amount of residual gas in the cavity which reduces the deflection of the plate. Using gauge factors for the estimated dopant profiles of the lightly doped piezoresistors along with their actual placement from the edge of the plate, the pressure characteristic over temperature is calculated and indicated by the dotted lines in the figure. The discrepancy in sensitivity arises from an overestimation of the gauge factor. The devices were linear over both pressure and temperature, with some nonlinearity appearing at overpressure conditions, as indicated in figure 6-2. The touchdown pressure for the circular device is 93psi, and for the square is 79psi, and the nonlinearity begins approximately at these pressures.

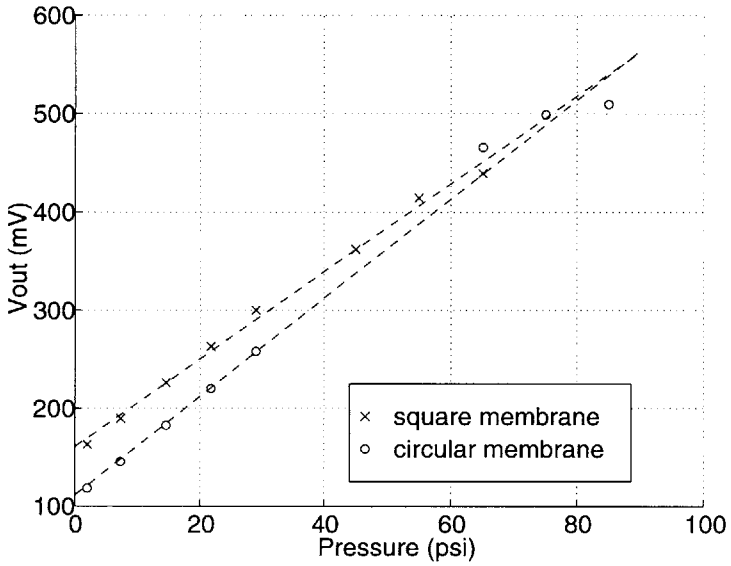


Figure 6-2: Motorola piezoresistive pressure sensor - overpressure response.

6.2 Capacitive pressure sensor

The capacitive pressure sensor is schematically illustrated in figure 1-5, and was fabricated in both discrete and integrated forms.

The basic device consists of a deformable silicon plate and a stationary metal plate on a glass capping wafer. The silicon plate is heavily doped with boron on the surface, and the metal top plate is a gold layer. Pressure is applied from the backside of the chip, pushing the plate upwards and decreasing the gap, thereby increasing the capacitance. Two types of devices were fabricated - those with and without a dielectric on the silicon plate. The MEMSCMOS process was used as previously described, with the CMOS portion replaced by two implants (boron to make the plate surface conductive and phosphorus in the field areas) and a drive-in anneal followed by an oxide deposition. The completed device is shown in a cross-sectional SEM in figure 6-3.

The parasitics surrounding the device are illustrated in figure 6-4. The bulk of the parasitic capacitance is the series combination of the oxide capacitance from the top and bottom plate leads. This oxide parasitic capacitance is nominally constant as the surface of the field areas is also heavily doped to prevent inversion. The field oxide is a 5000Åthick layer of LTO, so that the parasitic oxide capacitance is $0.07\text{fF}/\mu\text{m}^2$. Appendix G contains the layout of the tested sensors along with estimates for parasitic oxide capacitance, including the bondpad area. Calculated sensor capacitance values are compared to measured values to confirm that $C_{measured} = C_{sensor} + C_{oxide}$, where C_{oxide} is the series combination of C_{top} and C_{bottom}.

6.2.1 Discrete device testing

Capacitance-pressure characteristics were obtained via an HP4280 C-V meter in floating mode, and contact to the two plates of the device was obtained through probes to the bond pads (substrate left floating). The devices were mounted with epoxy on a plexiglass base with a pressure inlet tube and pressure was applied from a compressed nitrogen source. The inlet pressure was measured with a reference Honeywell 242PC60G piezoresistive gage pressure sensor with a range of 0-60psi. The maximum applied pressure was 60psi, a limitation imposed by the strength of the epoxy used to

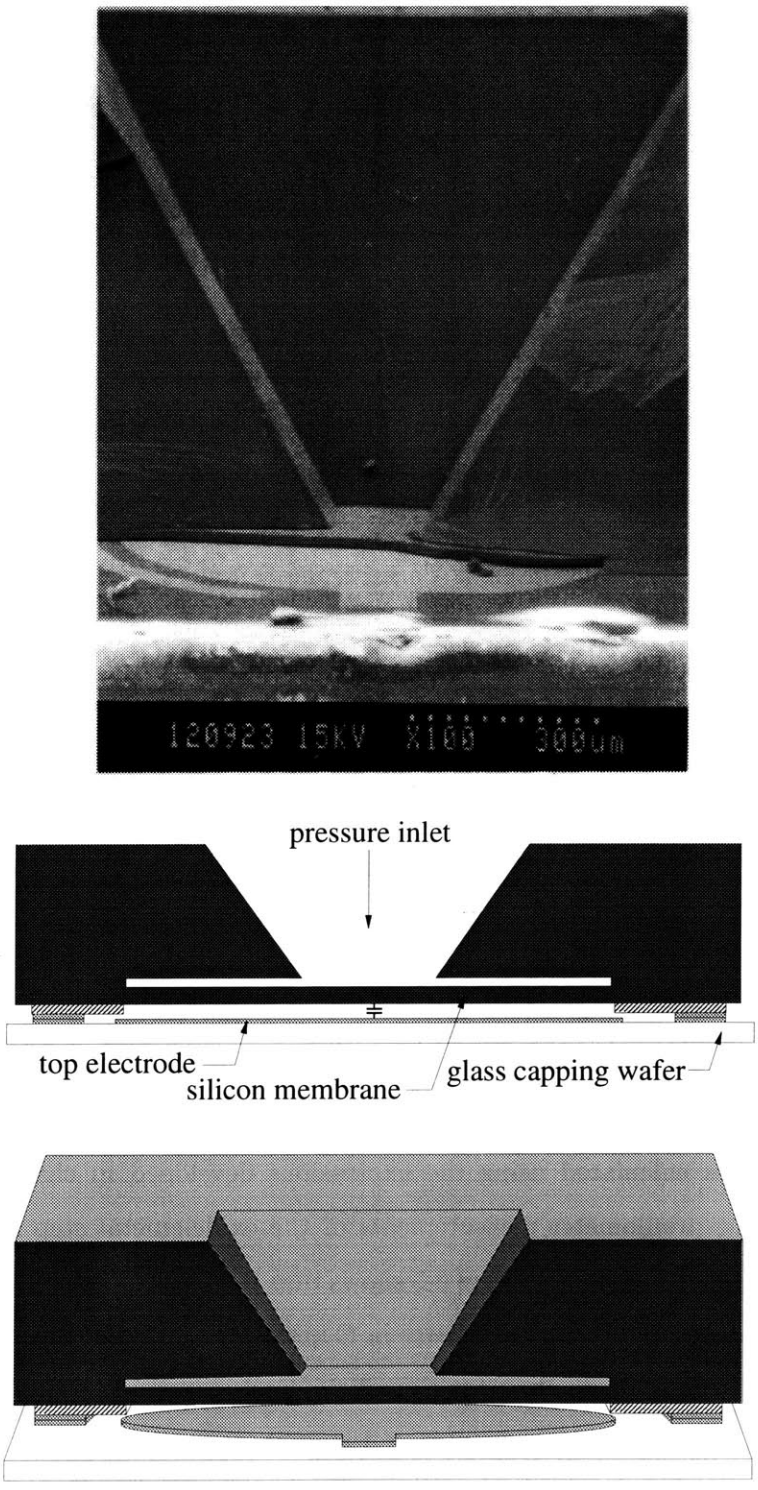


Figure 6-3: Capacitive pressure sensor.

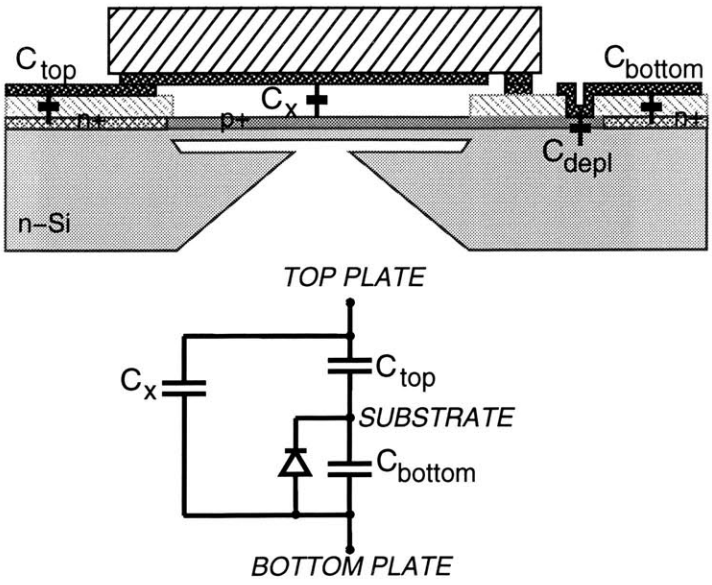


Figure 6-4: Parasitic capacitances.

hold the chip in place on its base (Torr Seal vacuum sealing epoxy).

Initially, connectivity to the top electrode through the thermocompression bond was checked with a resistance measurement using an additional metal pad leading to the top electrode thermocompression bond tab. Due to the length of the gold lines from the bond pads to the device, each device had a significant parasitic capacitance on the order of or greater than the nominal value.

Representative capacitance vs. pressure data from a variety of sensors are given in figures 6-5 to 6-8. $C_{nominal}$ refers to the airgap capacitance only, and C_0 is the measured value at zero applied pressure, including parasitics. The device # refers to table G.1. The measured data is in good agreement with curves calculated using the expressions developed in chapter 2. The gap was obtained from surface profilometer measurements of the oxide+metal step height, and the plate thickness was measured in the SEM. Figure 6-5 shows that the plates short together when they come into contact, as indicated by the rapid increase in C and G. Additional capacitance characteristics are given for other sensor sizes in the next two plots. Each curve represents 4 sweeps of pressure from zero to the maximum pressure, sampled at 1 second intervals.

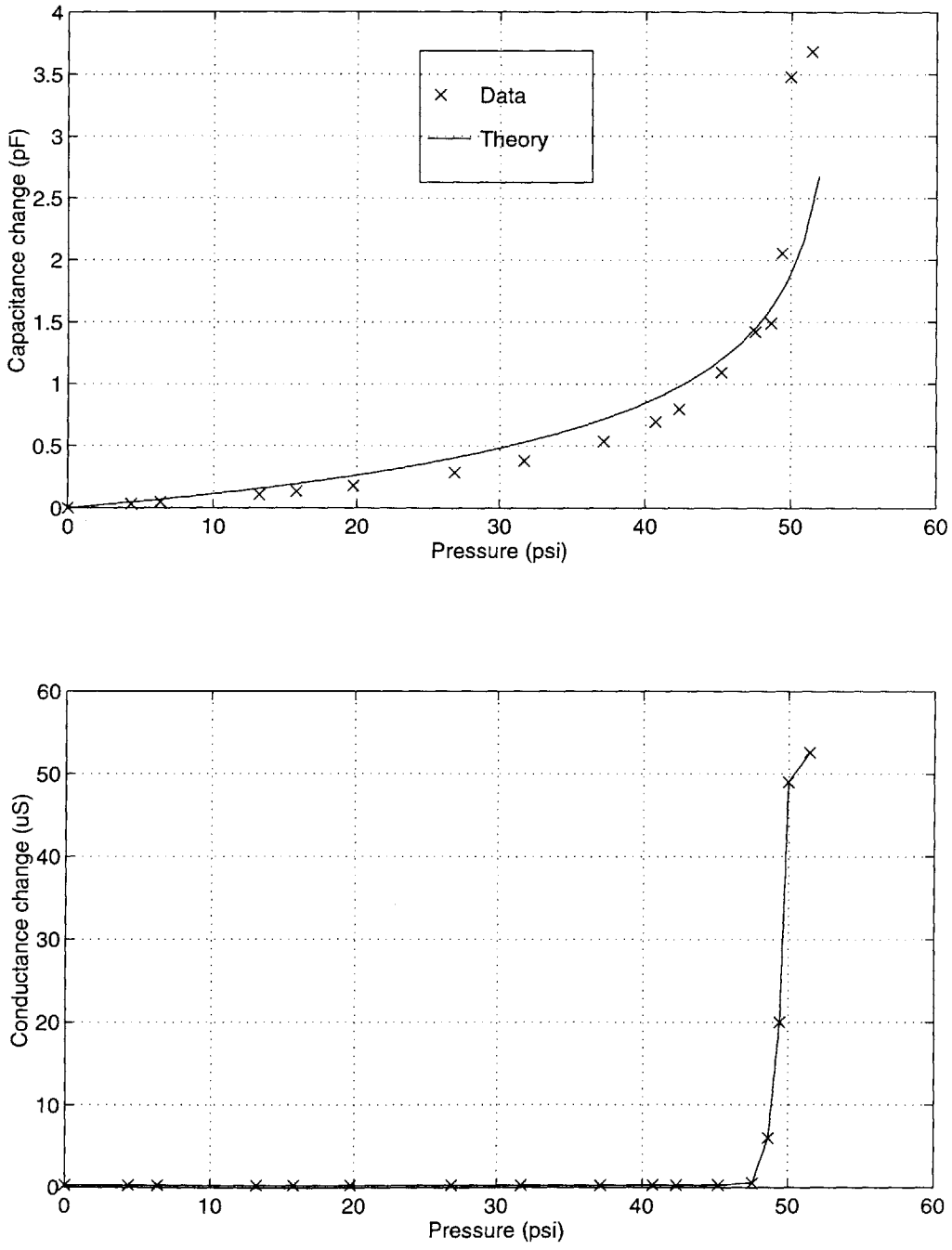


Figure 6-5: Capacitance-pressure data for device with dimensions a=240μm, h=11μm, L=1μm. a)capacitance vs. pressure, b)conduntance vs. pressure. Device #d11, C_0=4.7pF, $C_{nominal}$=1.6pF.

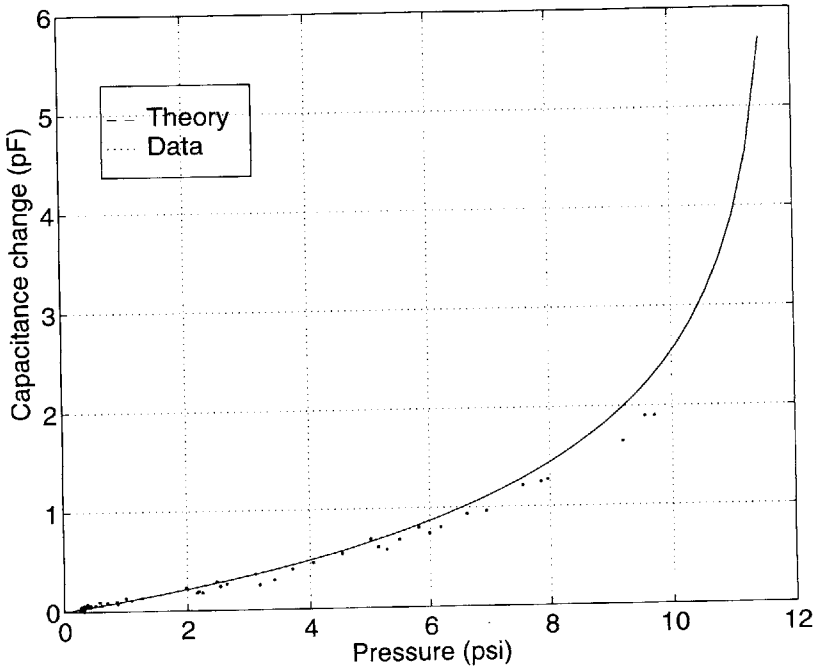


Figure 6-6: Capacitance-pressure data for device with dimensions a=350μm, h=11μm, L=1μm. Device #d1, C_0=5.6pF, $C_{nominal}$=3.4pF.

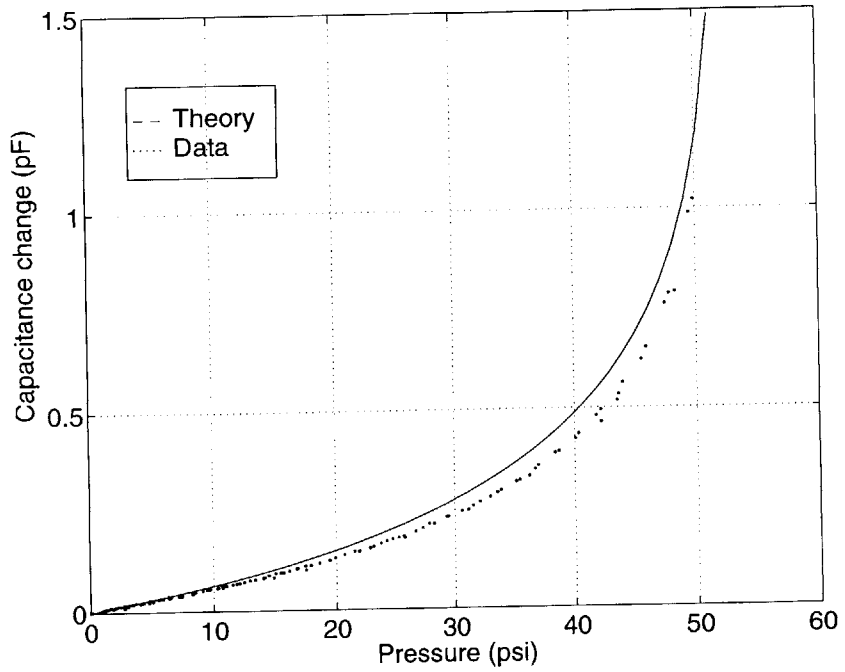


Figure 6-7: Capacitance-pressure data for device with dimensions a=240μm, h=9μm, L=1.8μm. Device #d11, C_0=3.78pF, $C_{nominal}$=0.89pF

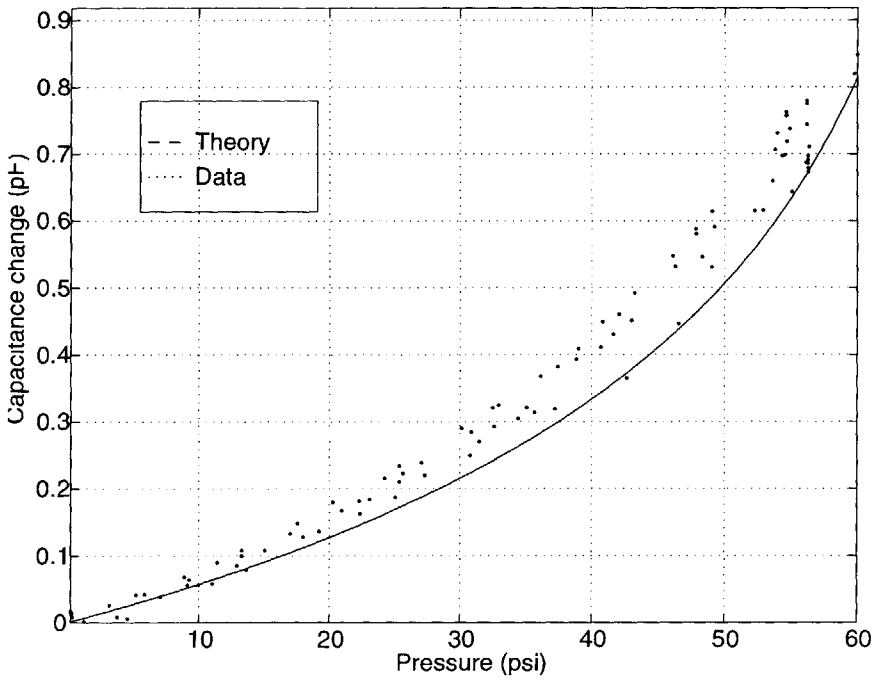


Figure 6-8: Capacitance-pressure data for device with dimensions a=200μm, h=9.5μm, L=1μm. Device #d15, C_0=8.54pF, $C_{nominal}$=1.1pF

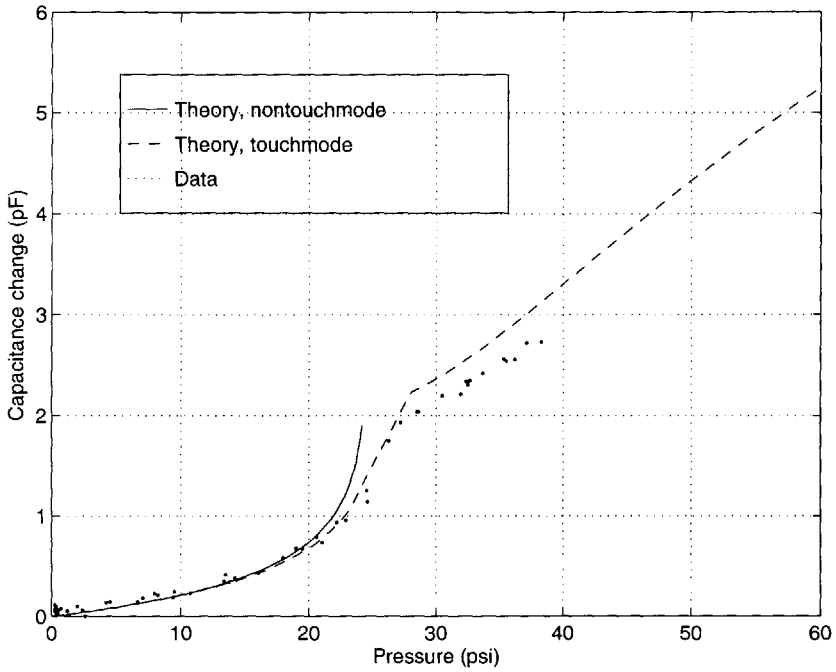


Figure 6-9: Sensor in touchmode: a=350μm, h=10μm, L=3μm, t_{ox}=0.2μm(fitted), Device #d1, C_0=2.8pF, $C_{nominal}$=1.2pF

Some sensors were fabricated with a layer of oxide on the silicon plate, thereby enabling them to be operated in touchmode. Figure 6-9 to 6-11 show the capacitance pressure characteristic of such sensors. It is apparent that the sensor behaves more linearly in the touched down regime. The theoretical curves were calculated using the approximate analysis given in chapter 2. The sensor was designed to have an oxide thickness of 1000Å. Due to the difficulty of measuring the thickness of the oxide on the plate, a measured value was not available, and a value of t_d=2000Å provided the best fit to the analytical solution.

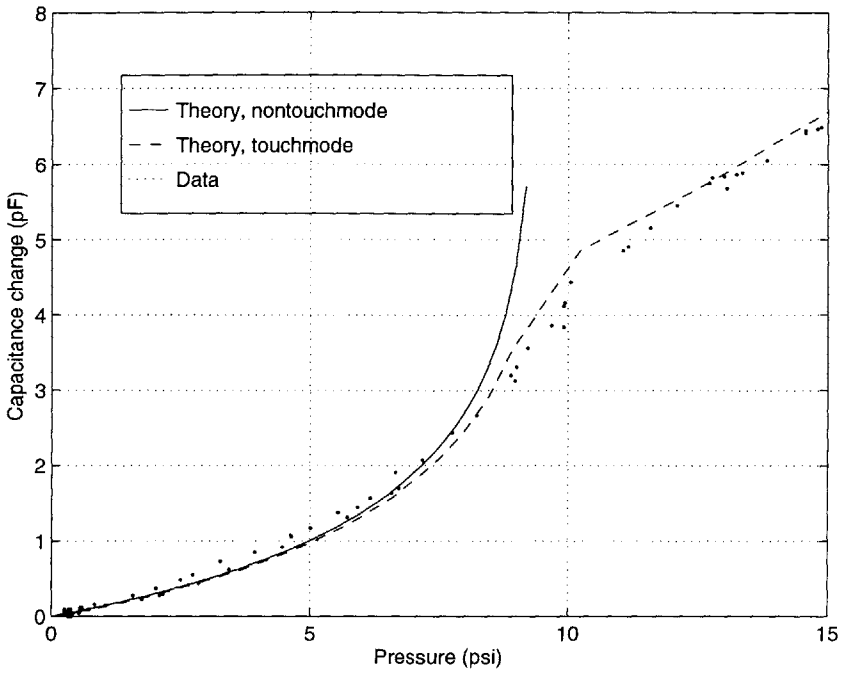


Figure 6-10: Sensor in touchmode: a=350μm, h=11μm, L=1μm, t_{ox}=0.2μm(fitted), Device #d13, C_0=5.6pF, $C_{nominal}$=3.4pF

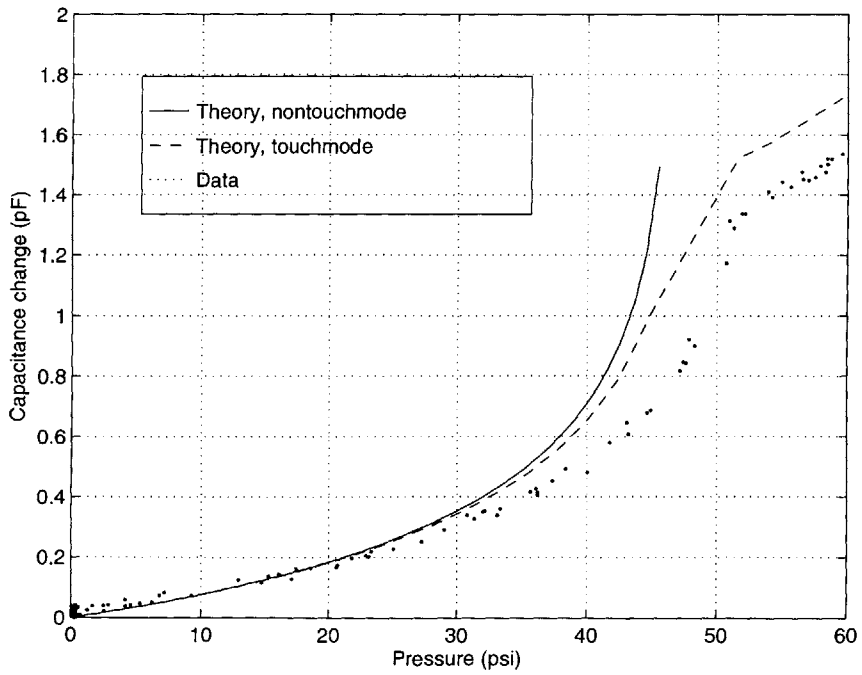


Figure 6-11: Sensor in touchmode: a=240μm, h=9μm, L=1.7μm, t_{ox}=0.2μm(fitted), Device #d11, C_0=4.4pF, $C_{nominal}$=0.89pF.

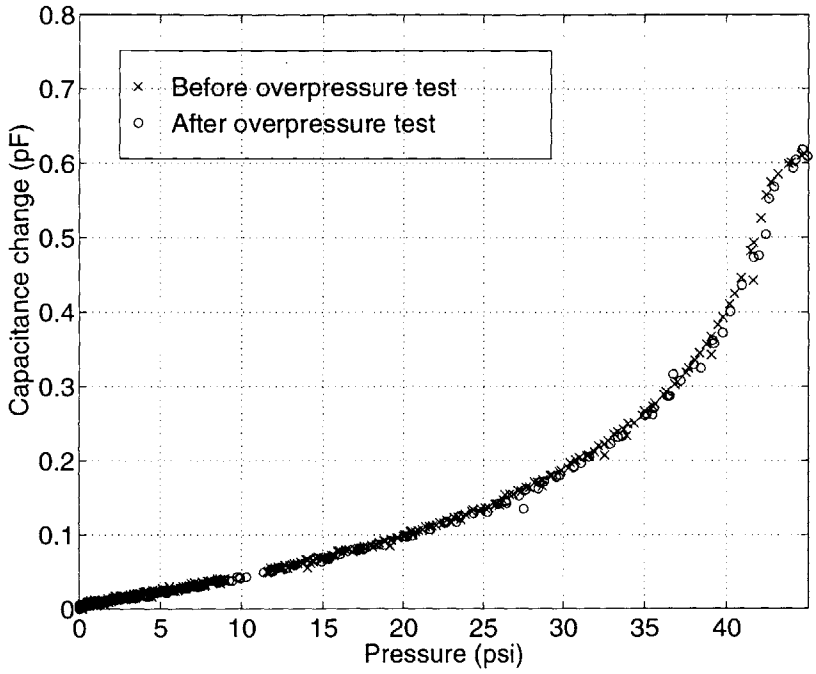


Figure 6-12: Capacitance before and after overpressure test. Overpressure conditions: 60psi maintained for 24 hours.

Overpressure test: Figure 6-12 shows the capacitance of a touchmode device with radius 240μm subjected to an overpressure of 60psi for a period of 24 hours. The plot gives measurements before and after the long term overpressure test, and indicates that there is no shift in the signal as a result of the overpressure.

Temperature sensitivity: Figure 6-13a) shows representative C-P curves at two temperatures. The base capacitance value changes substantially but the sensitivity remains approximately the same at both temperatures, as indicated in figure 6-13b). Since the sensitivity does not change much the variation is attributed to the parasitic MOS capacitance of the field oxide, as well as the contribution of the diode formed by the p+ plate and the n substrate.

To estimate the change due to temperature in a MOS capacitor with area A and unit capacitance C_t, the following can be used [93]:

$$\begin{aligned} T_{CC} &= \frac{1}{AC_t}\frac{d}{dT}(AC_t) \\ &= T_{CC}(th) + T_{CC}(sc) + T_{CC}(\epsilon_{ox}) \end{aligned}$$

$$= \left[\frac{1}{A}\frac{dA}{dT} - \frac{1}{t_{ox}}\frac{dt_{ox}}{dT}\right] + \left[\frac{C_{ox}}{C_s^2}\frac{dC_s}{dT}\right] + \left[\frac{1}{\epsilon_{ox}}\frac{d\epsilon_{ox}}{dT}\right] \quad (6.1)$$

Assuming $C_s >> C_{ox}$ (for heavily doped silicon surface), T_{CC} can be divided into three components as given above, which are due to thermal expansion in area and dielectric thickness, space charge capacitance, and dielectric constant respectively. Assuming a substrate thickness of a full wafer and neglecting changes in oxide thickness, $T_{CC}(th)$=5.6ppm/°C, and $T_{CC}(\epsilon_{ox})$=21ppm/°C from experiments [93]. Finally, the space charge contribution is dependent on the substrate doping and near flatband (V=0) is given by:

$$T_{CC}(sc) = \frac{C_{ox}k}{2q\sqrt{(\epsilon_{Si}N_d kT)}}\left[1 - T\left(\frac{1}{\epsilon_{Si}}\frac{d\epsilon_{Si}}{dT}\right)\right] \quad (6.2)$$

For a substrate surface concentration of $N_d \approx 4 \times 10^{18}/\text{cm}^3$, $T_{CC}(sc)$=225ppm/°C. This results in a total temperature coefficient of 252ppm/°C.

In addition to the field oxide parasitic, the p^+n junction of the bottom plate and the substrate forms a diode in parallel with C_{bottom}. This diode has an impedance associated with it, consisting of a parallel conductance G_D and diffusion capacitance C_D. To estimate the effect of the temperature dependence of G_D on the overall capacitance, the equivalent admittance of the system in figure 6-4b) is considered:

$$Y = j\omega C_x + G_{eq} + j\omega C_{eq} \quad (6.3)$$

where the equivalent capacitance C_{eq} is given by:

$$C_{eq} = \frac{G_D{}^2 C_T + \omega^2 C_T C_B{}^2 + \omega^2 C_T{}^2 C_B}{G_D{}^2 + \omega^2 (C_B + C_T)^2} \quad (6.4)$$

and C_T and C_B are the top and bottom oxide parasitics (neglect C_D since $C_D << C_B$) and G_D is exponentially dependent on temperature. The overall temperature sensitivity can then be caculated for the measurement signal used (30 mV sinusoid at 1 MHz). Taking the representative device characteristics in figure 6-13 with C_T=5.9pF, C_B=2.6pF, C_x=0.9pF and including the T_{CC} calculated above for the oxide parasitics, a change in G_D from $4\times10^{-9}/\Omega$ to $4\times10^{-6}/\Omega$ would result in a total sensitivity of 530ppm/°C. The measured shift for this device was 577ppm/°C. As a check on the plausibility of the shift in G_D, the extimated conductance for the diode present in this device is G_D=$8.4\times10^{-10}/\Omega$ at 25°C and G_D=$8.3\times10^{-7}/\Omega$ at 90°C.

Measurements on a set of 5 devices yielded an experimental T_{CC} of 428±246ppm/°C. Because of the small number of samples measured, there is a large uncertainty in the temperature sensitivity value, and further measurements are necessary to get a better estimate of this value. However, the neglible shift in $\triangle$C at elevated temperature implies that the device may have a low sensitivity to package stresses.

6.2.2 Sensor-circuit system

The capacitive pressure sensors were combined with a sensing and linearity calibration developed by J.Lloyd [49]. This system utilizes 8 sensors, of two sizes, in a two-loop calibration technique that exploits the linearity of the smaller sensor and the sensitivity of the larger device, to obtain polynomial functions of pressure that can be used to linearize the output of the large sensitive sensor. The pressure range of the system is determined by the dimensions of the large sensor, and the system uses 4 reference and 4 sensing capacitors. For this particular system, the physical dimensions of the sensors were:

- small sensor: radius=130μm, plate thickness=9μm, gap=1.8μm
- large sensor: radius=240μm, plate thickness=9μm, gap=1.8μm, range=54psi (touch pressure)

Hybrid sensor-circuit system

A hybrid version of the system was made by combining a chip with the individual sensors with a circuit chip (fabricated at MOSIS) in a 64-pin PGA package as illustrated in figure 6-14. Access to pressure inlet ports on the chip was obtained by means of holes in the base of the package cavity. The holes were drilled through the ceramic package using a hollow bit filled with diamond slurry [94, 95]. Polyethylene tubing of the same diameter as the holes was attached via epoxy to the package. To be able to center the circuit chip in the package, it was stacked on top of the sensor chip. The sensor chip can be much reduced in size by decreasing the spacing of the sensors.

The pressurization test setup is similar to that used for discrete device testing. The pressure source was compressed air, regulated by a Bellofram pressure transducer which provided an output of 3-120psi with a 0-10V DC input signal. Pressure was measured as before with a reference Honeywell

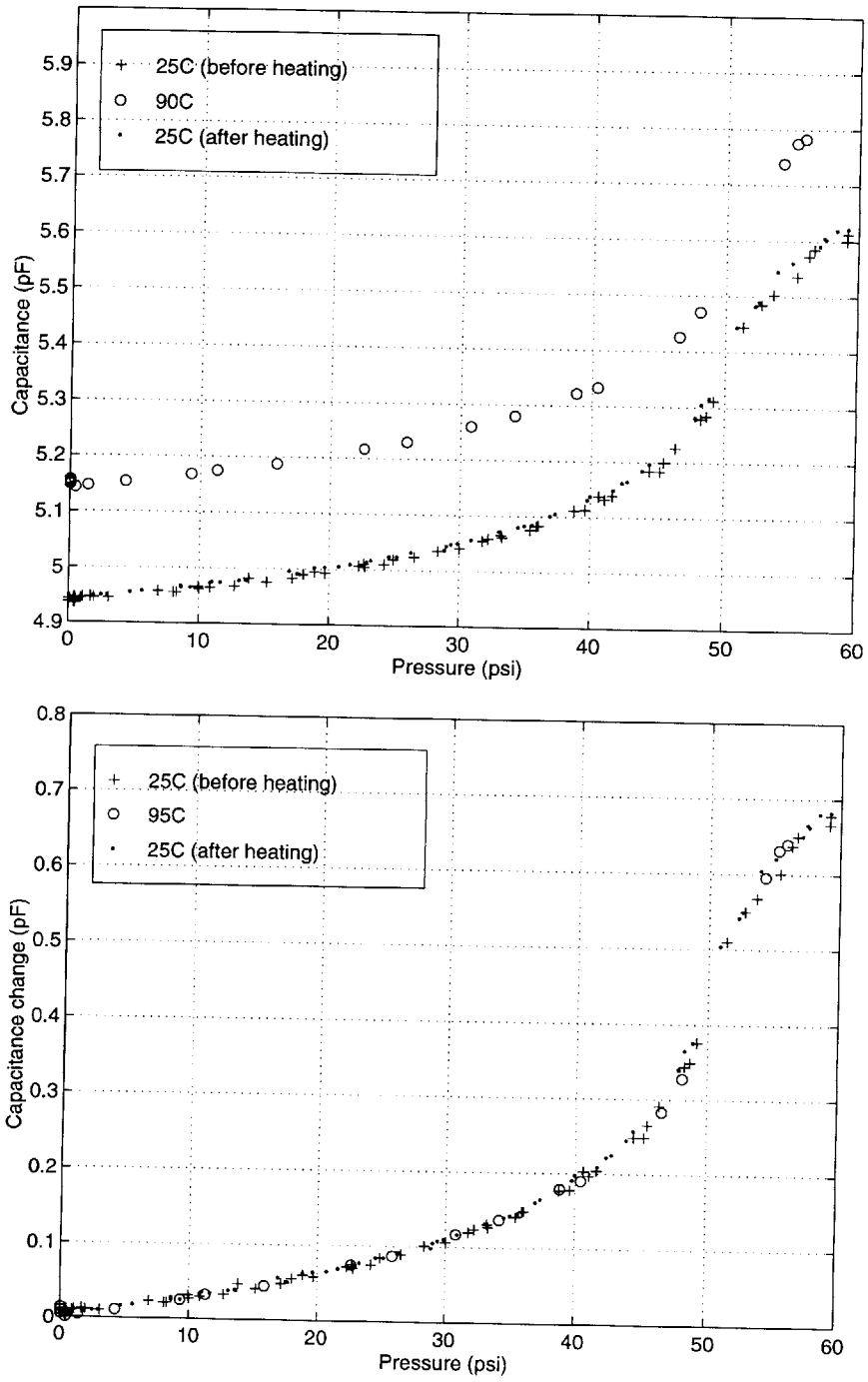


Figure 6-13: a)Capacitance response for device #h3 at 25°C, 90°C. b)Change in capacitance.

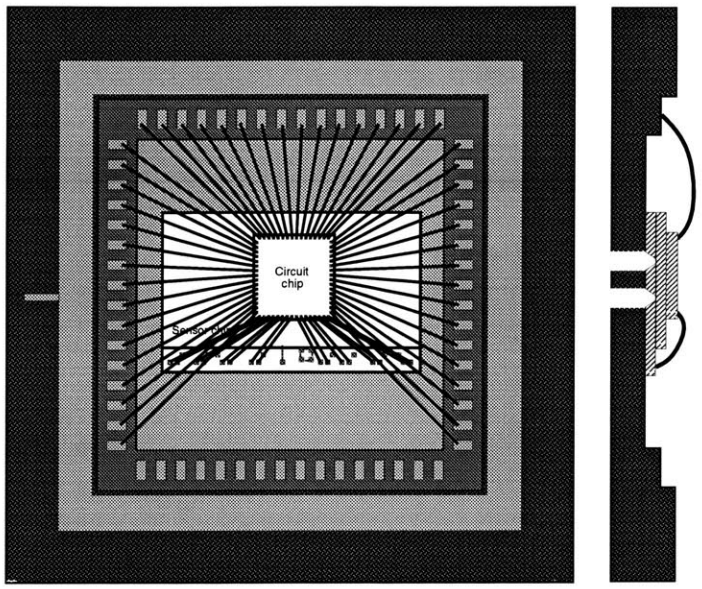


Figure 6-14: Packaging of hybrid sensor-circuit system

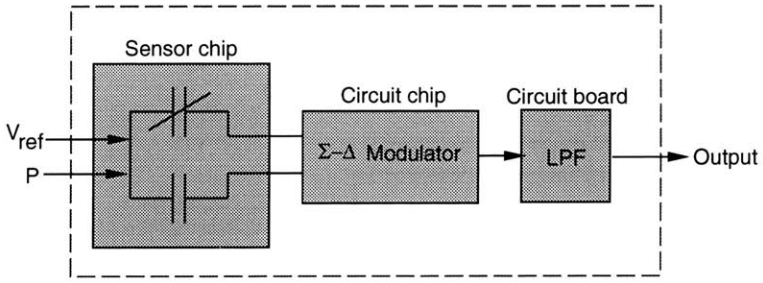


Figure 6-15: Block diagram of sensor-circuit system [49].

sensor. Figure 6-15 is a block diagram of one half of the sensing system containing one sense and reference capacitor, and figure 6-16 shows output from this system, for the large sensor with dimensions a=240μm, h=9μm, L=1.8μm. This represents the unscaled filtered value of the output from the Σ-Δ converter, which tracks changes in input pressure. The sensitivity increases with increasing pressure as expected when nearing the touchdown pressure of 54psi.

Integrated sensor-circuit system

The final set of test wafers contained the integrated sensor-circuit system, with the associated mask layout shown in figure 6-17.

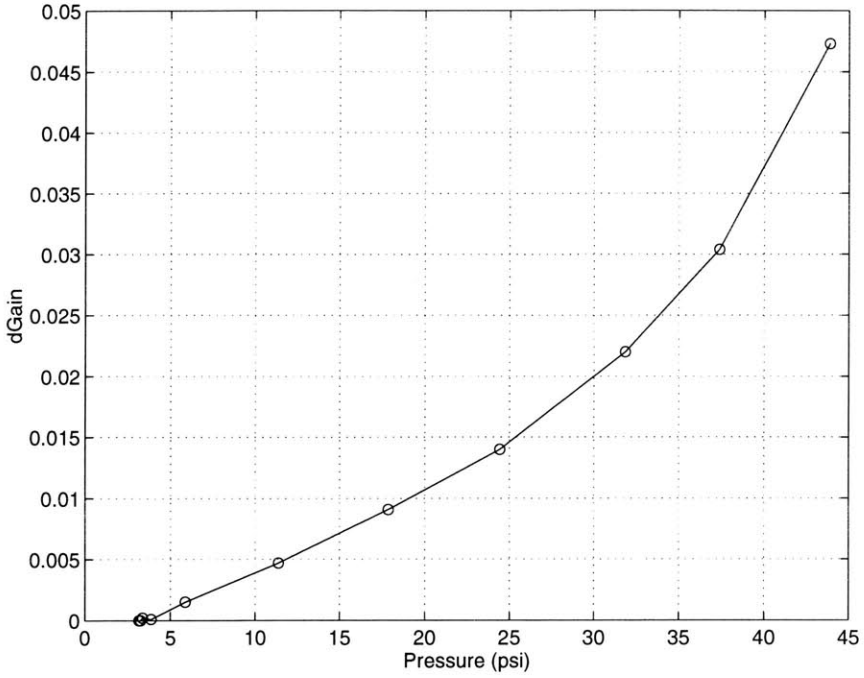


Figure 6-16: Output from hybrid sensor system.

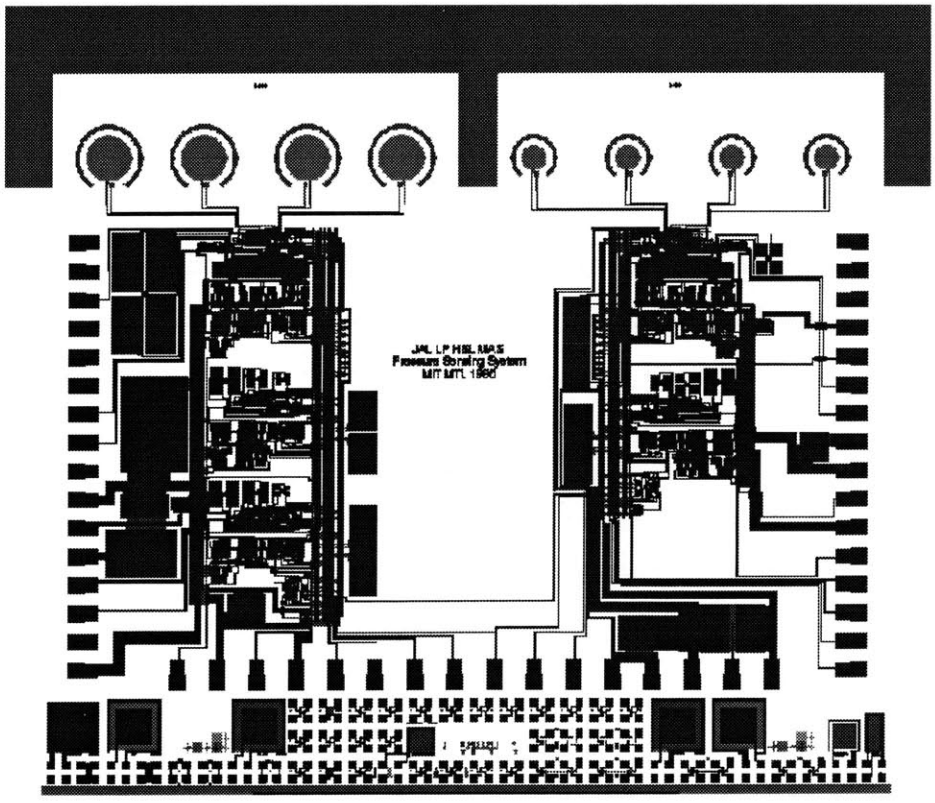


Figure 6-17: Layout of integrated sensor system.

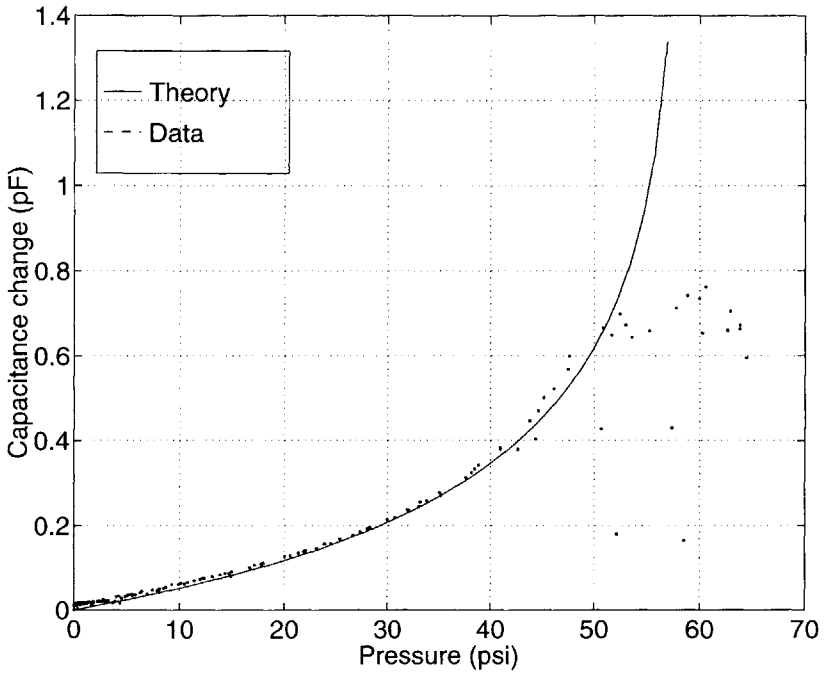


Figure 6-18: Capacitance-pressure data for large sensor on integrated chip, with dimensions a=240μm, h=9μm, L=2.0μm. $C_{nominal}$=0.80pF

Measurement of test transistors on this set of wafers indicated that the threshold voltages were anomalously high (V_{t_n}=1.2V, V_{t_p}=-1.3V), on both the test wafers with sensors and control wafers that did not undergo micromachining steps. Thus the full circuit was not functional, so the integrated system was not exercised. The problem appears to be caused by the omission of one of the threshold adjustment implants during the CMOS portion of the process. However since both the control and test wafers behaved identically, the lack of functionality was not due to the added micromachining steps. The sensors on the integrated chip were functional when tested independently as shown by a representative device characteristic in figure 6-18.

In this chapter results of pressure sensor testing have been presented. Process partitioning was demonstrated in the transfer of wafers to an external facility at Motorola to make piezoresistive pressure sensors. The capacitive pressure sensor was operated in both the conventional and touchdown modes, and displayed robustness to overpressure and temperature conditions.

Chapter 7

Conclusions

The goal of this thesis work was to develop and demonstrate a process that can be used to make integrated silicon sensors. The process was designed to take advantage of the beneficial properties of silicon as a good quality mechanical as well as electrical material, and also featured ease of integration into existing silicon foundries, thereby enabling separate optimization of all parts of the sensor-circuit system. The MEMSCMOS process incorporated silicon wafer bonding with a sealed cavity, buried etchstop layers for formation of backside pressure ports, and both front and backside release etches. A thermocompression bond was used to form a capacitive electrode.

7.1 Contributions of this work

The main element of the integrated MEMSCMOS process is a sealed cavity formed by silicon wafer bonding, and one of the key contributions of the thesis was the completion of a model for predicting plastic deformation in sealed cavities of various configurations, as seen in a typical sensor. This model enables the designer to determine appropriate bonding conditions and geometries to ensure that no dislocations are generated in the sealed cavity plate at any time during the circuit processing. The phenomenon of defect formation in plates with constrained downward deflection at high temperatures was examined, and analytical and finite element modelling results indicated that by creating a low but non-zero pressure inside the sealed cavity, it is possible to avoid defect formation in both constrained and unconstrained plates. These results were confirmed via controlled experiments with sealed cavities under various cavity pressures.

The complete MEMSCMOS process was demonstrated via three test lots. Characteristics of both mechanical and electrical elements on these lots were measured, and no degradation of electrical properties of transistors on micromachined substrates was observed. In addition, there was no apparent stress-induced damage to mechanical elements, as they were designed using the model developed for sealed cavities. This was confirmed by means of visual inspection for warpage, materials analysis using defect etching, and electrical tests via pull-in measurements. The fabrication of the test lots also demonstrated that it is possible with this technology to construct both surface and bulk micromachining type structures on the same substrate, with access on both sides of the chip. The substrates were also processed in an industrial process line at Motorola, demonstrating the ability to decouple micromachining and circuit fabrication steps.

The demonstration vehicle for the process was a capacitive pressure sensor, fabricated in two forms - a conventional device and a touchmode device. The sensors were tested both individually and as part of a sensing and calibration system [49]. The devices exhibited functionality and good matching to expected characteristics in both modes of operation, as well as displaying insensitivity to temperature. Additionally, the touchmode devices were shown to be robust at overpressure conditions. Finally, the sensor was operated in conjunction with a separately designed calibration circuit. A hybrid combination of the sensor and circuit was functional. The corresponding integrated version was fabricated using the MEMSCMOS process and sensors on this integrated chip were functional also.

7.2 Recommendations for future work

Future concerns in process development include two areas: the replacement of the wet etch for the backside port formation with a deep dry etch, thereby increasing device density further as well as simplifying the process, and the extension of the thermocompression bond to a wafer level and its possible use for packaging and hermetic sealing.

Further characterization of the pressure sensor in touchmode operation can be done, in conjunction with additional bond strength measurements of the thermocompression bond, to determine whether the metal bond interface shows any sign of failing at high overpressures.

The development of the model and process, along with the availability of equipment for controlled ambient and thermocompression bonding has brought the sealed cavity MEMSCMOS technology to a level that it can be transferred to industrial fabrication lines. With the addition of the above mentioned modifications to the process, it can be exercised in making a wide variety of integrated microelectronic transducers.

Appendix A

Derivation of D_{eff} in large deflection

The following analysis to obtain an expression for the effective flexural rigidity for a plate in large deflection was taken from Timoshenko [48] chapter 13.

For plates in large deflection where the deflection is large compared to the thickness but small compared to the radius, stretching of the middle plane must be considered in the analysis. Assume that the plate has a deflection shape similar to that of the small deflection regime:

$$w = w_o \left(1 - \frac{r^2}{a^2}\right)^2 \tag{A.1}$$

where w_o is the center deflection.

The strain energy in the plate from pure bending is

$$\begin{aligned} V_1 &= \frac{D}{2}\int_0^{2\pi}\int_0^a \left[\left(\frac{\partial^2 w}{\partial r^2}\right)^2 + \frac{1}{r^2}\left(\frac{\partial w}{\partial r}\right)^2 + \frac{2\nu}{r}\frac{\partial w}{\partial r}\frac{\partial^2 w}{\partial r^2}\right] r dr d\theta \\ &= \frac{32\pi}{3}\frac{w_o^2}{a^2}D \end{aligned} \tag{A.2}$$

The in-plane displacement is assumed to have the form:

$$u = r(a-r)(C_1 + C_2 r^2 + C_3 r^3 + ...) \tag{A.3}$$

so that $u(0) = u(a) = 0$. The strain energy from stretching is given by:

$$V_2 = 2\pi \int_0^a \left(\frac{N_r \epsilon_r}{2} + \frac{N_t \epsilon_t}{2} \right) r dr \tag{A.4}$$

where

$$\begin{aligned} \epsilon_r &= \frac{du}{dr} + \frac{1}{2}\left(\frac{dw}{dr}\right)^2 \\ \epsilon_t &= \frac{u}{r} \\ N_r &= \frac{Eh}{1-\nu^2}(\epsilon_r + \nu\epsilon_t) \\ N_t &= \frac{Eh}{1-\nu^2}(\epsilon_t + \nu\epsilon_r) \end{aligned} \tag{A.5}$$

(A.6)

If u is approximated by its first three terms an expression for the strain energy of stretching V_2 is obtained. To find the constants, the total energy of the plate at an equilibrium position is a minimum so that:

$$\begin{aligned} \frac{\partial V_1}{\partial C_1} &= 0 \\ \frac{\partial V_1}{\partial C_2} &= 0 \\ \frac{\partial V_1}{\partial C_3} &= 0 \end{aligned} \tag{A.7}$$

can be solved for C_1 and C_2. Thus the total strain energy $V_1 + V_2$ is:

$$V_1 + V_2 = \frac{32\pi D}{3}\frac{w_o^2}{a^2} + 8.043\frac{D w_o^4}{h^2 a^2} \tag{A.8}$$

assuming $\nu = 0.3$.

The deflection is calculated by using the principle of virtual displacements, in which the change in total strain energy is equal to the total work done in displacing the plate with an applied uniform load q:

$$\frac{d(V + V_1)}{dw_o} = 2\pi \int_0^a q\delta w r dr \tag{A.9}$$

This gives a cubic equation in w_o:

$$w_o + 0.480\frac{w_o^3}{h^2} = \frac{qa^4}{64D} \tag{A.10}$$

which when solved for w_o gives

$$w_o = \frac{qa^4}{64D_{eff}} \tag{A.11}$$

where

$$\begin{aligned} D_{eff} &= \left[\left(\frac{1.0246\phi}{D} + \sqrt{\left(\frac{1.0246\phi}{D}\right)^2 + \phi^3\psi}\right)^{\frac{1}{3}} + \left(\frac{1.0246\phi}{D} - \sqrt{\left(\frac{1.0246\phi}{D}\right)^2 + \phi^3\psi}\right)^{\frac{1}{3}}\right]^{-1} \\ \phi &= \left(\frac{64h}{qa^4}\right)^2 \\ \psi &= 0.3187 \end{aligned} \tag{A.12}$$

Appendix B

Process Descriptions

B.1 Integrated MEMSCMOS Process Traveller

The following is the description of the MEMSCMOS process required for use in the Microsystems Technology Laboratories at MIT. All photolithography was done on a GCA6800 wafer stepper, with the exception of the steps marked ** which were done using a Karl Suss model MA4 contact aligner.

MEMSCMOS PROCESS TRAVELLER

STARTING SUBSTRATES:

PROCESS A - Electrochemical etchstop
DEVICE WAFER
• epi-wafer - p-type, <100>, $\rho < 20\Omega$cm substrate with 10μm epitaxial layer, As-doped, $\rho > 20\Omega$cm
HANDLE WAFER
• n-type, <100>, P-doped, $\rho < 2\Omega$cm, double-side polished

PROCESS B - Chemical etchstop
DEVICE WAFER
• SOI wafer: Si layer is 10μm p-type, <100>, $\rho > 20\Omega$cm
buried oxide is 0.4μm SiO_2
substrate is p or n-type, <100>, $\rho < 20\Omega$cm
HANDLE WAFER
• p-type, <100>, B-doped, ρ=10-20Ωcm, double-side polished

PROCESS A or B
GLASS WAFER
• 7740 Pyrex glass wafer, thickness=500 μm

STEP	STEP DESCRIPTION
HANDLE WAFER	
1	Cavity pattern
2	Cavity plasma etch
3	Ash resist
4*	Grow stress relief oxide
5*	Deposit silicon nitride cavity etchstop
6	Coat front with resist
7*	Etch backside nitride
8	Ash resist
9	Pattern nitride cavity etchstop
10*	Etch nitride cavity etchstop
11	Piranha clean
12*	Etch stress relief oxide
DEVICE AND HANDLE WAFERS - PROCESS A - Electrochemical etch stop	
1*	Bond wafers (contact in oxygen)
2*	Bond anneal in non-oxidizing ambient
3*	Phosphorus dope surfaces
4*	Wet etch phosphorus glass
5	Grind and polish bonded pair
6*	Electrochemical wafer thinback
DEVICE AND HANDLE WAFERS - PROCESS B - Chemical etch stop	
1*	Bond wafers (contact in oxygen)
2*	Bond anneal in oxidizing ambient
3	Grind and polish bonded pair
4*	Chemical wafer thinback
DEVICE AND HANDLE WAFERS - PROCESS A or B	
1*	Post-KOH clean
2	**MIT Baseline CMOS process** [67]
3	Pattern MEMS structure areas
4*	Clear MEMS structure areas
5	Ash resist
6*	Deposit PECVD nitride etch mask
7**	Pattern backside vias - infrared alignment
8*	Plasma etch nitride mask for backside vias
9	Ash resist
10*	KOH etch backside vias
11*	Modified post-KOH clean
12*	Plasma etch frontside etch mask nitride
13	Pattern for gold metallization - image reversal resist required
14	Metal e-beam evaporation - 100Å Cr + 5000Å Au
15	Metal liftoff - NO ultrasonic agitation

16	Pattern release holes
17*	Etch release holes
18	Ash resist
19	Pattern structure release
20*	Etch structures
21*	Plasma etch backside and cavity nitride
22	Ash resist

****** SILICON WAFER COMPLETED ******

GLASS WAFER

1**	Pattern for metal - image reversal resist
2	Metal e-beam evaporation - 100Å Cr + 5000Å Au
3	Metal liftoff - ultrasonic agitation in acetone

****** GLASS WAFER COMPLETED ******

GLASS AND SILICON WAFERS

1	Saw wafers into chips
2*	Thermocompression bond chips
3	Attach to package and wirebond

****** DEVICES COMPLETED ******

B.2 Capacitive Pressure Sensor Process Traveller

The following is the process description used for fabrication of the discrete and hybrid capacitive pressure sensors. All photolithography was done on a Karl Suss model MA4 contact aligner.

STARTING SUBSTRATES:

DEVICE WAFER
- p-type, <100>, $\rho = 10 - 20\Omega$cm

HANDLE WAFER
- n-type, <100>, P-doped, $\rho < 2\Omega$cm, double-side polished

GLASS WAFER
- 7740 Pyrex glass wafer, thickness=500 μm

STEP	STEP DESCRIPTION
HANDLE WAFER	
1	Cavity pattern
2*	Cavity plasma etch
3	Ash resist
4*	Grow stress relief oxide
5*	Deposit silicon nitride etchstop
6	Coat front with resist
7*	Etch backside nitride
8	Ash resist
9	Pattern nitride etchstop
10*	Etch nitride stop
11	Piranha clean
12*	Etch stress relief oxide
DEVICE WAFER	
1*	Grow stress relief oxide
2	Implant phosphorus for plate - dose=5e15/cm^2, energy=160keV
3*	Drive in phosphorus for plate
4*	Etch stress relief oxide
DEVICE AND HANDLE WAFERS - Electrochemical etch stop	
1	Bond wafers (contact in oxygen)
2*	Bond anneal in non-oxidizing ambient
3*	Phosphorus dope surfaces
4*	Wet etch phosphorus glass
5	Grind and polish bonded pair
6*	Electrochemical wafer thinback
BONDED DEVICE AND HANDLE WAFERS	
1*	Post-KOH clean
2*	Grow stress relief oxide
3	Pattern p+ implant over sensors
4	Implant boron in plate - dose=1e15/cm^2, energy=40keV
5	Ash resist
6	Pattern n+ implant in field
7	Implant phosphorus in field - dose=5e14/cm^2, energy=50keV
8	Ash resist
9*	Activate implants
10*	Deposit LTO - 5000Å
11	Pattern LTO
12	Etch LTO - BOE wet etch
13	Deposit LPCVD nitride etch mask - 5000Å
14	Pattern backside vias
15*	Etch nitride mask for backside vias

16	Ash resist
17*	KOH etch backside vias
18*	Post-KOH clean
19*	Plasma etch frontside etch mask nitride
20	Pattern for gold metallization - image reversal resist required
21	Metal e-beam evaporation - 100Å Cr + 5000Å Au
22	Metal liftoff - NO ultrasonic agitation
23*	Plasma etch backside and cavity nitride

****** SILICON WAFER COMPLETED ******

GLASS WAFER

1	Pattern for metal - image reversal resist required
2	Metal e-beam evaporation - 100Å Cr + 5000Å Au
3	Metal liftoff - ultrasonic agitation in acetone

****** GLASS WAFER COMPLETED ******

GLASS AND SILICON WAFERS

1	Saw wafers into chips
2*	Thermocompression bond chips
3	Attach to package and wirebond

****** DEVICES COMPLETED ******

B.3 Process details

The following section gives details of process steps noted with as asterisk in the previous section, as they pertain to the Microsystems Technology Laboratories at MIT.

Wet etch recipes

Stress relief oxide etch:
- Etchant: BOE
- Time: 30 sec (to etch 430Å)

Phosphorus glass etch:
- Etchant: BOE
- Time: 60 sec (to etch 1200Å)

Clear MEMS structure areas:
- Etchant: BOE
- Time: 10 min (to etch 7000Å)

Chemical and Electrochemical wafer thinback:
- Etchant: KOH, 20% by weight
- Temperature: 95°C
- Etch rate: 2.5μm/min
- add surfactant [56] (4mL/L etchant) to reduce bubble evolution.

Plasma etch recipes

Silicon plasma etch - cavities:
- Recipe: 19
- Etcher: 1
- Chemistry: SF_6
- Power: 50 W
- Etch depth: 1μm
- Time: ≈3 min (characterize)

Silicon plasma etch - release holes, structure etch:
- Recipe: 19
- Etcher: 1
- Chemistry: SF_6 + CCl_4
- Power: 50 W
- Etch depth: release holes - 3μm, structure etch - 10μm
- Time: ≈10 min for release holes, ≈40 min for structure etch (characterize)

Silicon nitride plasma etch - frontside cavity etch-stop and backside nitride
- Recipe: 15
- Etcher: 1
- Chemistry: SF_6
- Power: 300 W
- Etch depth: 1500Å
- Time: endpoint on oxide (≈40 sec)

Silicon nitride plasma etch - front and backside via etch mask and cavity nitride:
- Etcher: RIE
- Chemistry: 11 sccm SF_6
- Power: 175 W
- Pressure: 100 mTorr
- Etch depth: 5000Å
- Time: ≈10 min (characterize)

Diffusion recipes

Stress relief oxidation:
- Recipe: 210
- Tube: A1 or A2 (ICL)
- Temperature: 950°C
- Time: 100 min dry O_2 + 30 min N_2
- Thickness: 430Å

Bonding anneal (non-oxidizing):
- Recipe: 225
- Tube: A3 (ICL)
- Temperature: 1100°C
- Time: 60 min in N_2

Bonding anneal (oxidizing):
- Recipe: 223
- Tube: A3 (ICL)
- Temperature: 1100°C
- Time: 20 min dry O_2 + 90 min steam + 20 min dry O_2
- Thickness: 8000Å

Phosphorus doping:
- liquid $POCl_3$ source, oxidizing ambient
- Recipe: 310
- Tube: A4 (ICL)
- Temperature: 950°C
- Thickness: 1200Å

Phosphorus plate implant drive-in:
- Recipe: 253
- Tube: B1 or B2 (ICL)
- Temperature: 1150°C
- Time: 15 hrs in N_2
- Junction depth: 10μm

Implant activation anneal:
- Recipe: 259
- Tube: B1 or B5 (ICL)
- Temperature: 1000°C
- Time: 30 min in N_2

Film depositions

Silicon nitride deposition - cavity etchstop:
- Tube: vertical deposition tube VTR (ICL)
- Film composition: 10:1 silicon-rich nitride
- Film thickness: 1500Å

LTO (low temperature oxide) deposition:
- Recipe: 430
- Tube: A7
- Film thickness: 5000Å

PECVD silicon nitride deposition [96]:
- Temperature: 350°C
- Film thickness: 5000Å

Other processes

Backside via etch:
Wax frontside protection: Heat wafer to 80°Con a hotplate. Spread Carnauba wax [68] flakes on the frontside of the wafer and allow to melt until the wafer is completely coated. Carefully apply etch-resistant tape [69] cut to the proper size on top of the wafer, making sure that no bubbles are present (note: the wafer can be attached to a glass plate using the wax, if the tape is not available). Remove the wafer from the hotplate and place on a cool surface to solidify the wax. Proceed with the etch. To maintain the integrity of the wax, the etchant temperature cannot exceed 65°C.

Post KOH clean:

- In RGL: DI water rinse for 10 min.
- In TRL:
  - Piranha clean 10 min.
  - Dump rinse 3 times in acid hood
  - BOE dip 10 sec.
  - Dump rinse 3 times in acid hood
  - Spin dry in photolithography room
  - Standard RCA clean in RCA station

Modified post KOH clean:

- In RGL: DI water rinse for 10 min.
- In TRL:
  - Piranha clean 10 min.
  - Dump rinse 3 times in acid hood
  - Spin dry in photolithography room

Thermocompression bonding of chips:

- Pre-bond clean: UV ozone exposure 10 min.
- Heat on hotplate @ 350°C
- Apply pressure of 20 lb/in^2 for 2 min.

B.4 Procedure for Wafer Bonding using Spin Bonder in TRL

1. Clean bonder chuck (not necessary for every use): Remove from chamber by unscrewing chuck from base. Prepare piranha (3:1 H_2SO_4:H_2O_2) in quartz tank, to an amount such that the level in the tank is about 1.5". This is necessary because the fitting on the back of the chuck is metal so the whole chuck cannot be immersed. Balance chuck on a wafer cassette handle face down and place in piranha for 5 minutes. Rinse well in DI water. With clean gloves, place on a clean fab wipe and blow dry, without touching the front surface. Wipe down inside of chamber with fab wipe and methanol. Screw chuck back onto base, again without touching the front of the chuck. Also wipe quartz wafer wand located beside the bonding table.

2. Turn on gases and set flow rates to desired levels. For the lowest pressure inside cavities, turn on oxygen valve fully and keep flow meter valves open fully. For 0.2 atm pressure in the cavity, set flowmeters to 1 scfh for N_2 and 4 scfh for O_2.

3. Clean wafers: Do RCA clean as per standard procedure. Use bonding carrier and handle, located in boxes on the shelf under the bonder table. Place wafers in cassette in pairs, with all wafer fronts facing the same way. Clean 2 pairs of large Teflon tweezers and one small pair (located in blue box also under bonding table) by immersing in organic clean bath for 5 minutes after wafers have been through this step, then rinse in dump rinser. Allow tweezers to dry on a clean fab wipe on bonding table.

4. Contact wafers: If bonding more than 5-6 pairs, split the lot while cleaning and leave the second half in the spin dryer while contacting the first half batch. To contact, place first wafer of pair face up on chuck and close chamber. Spin for 1 minute at 3000rpm. Turn off and open chamber, and place second wafer on Teflon shims face down. Close chamber and spin at 3000rpm for 5 minutes. Slow spin speed to 200rpm and press down Teflon rod to knock out shims. Turn off spinner and press center plunger to initiate contact, and hold down for 15-30 seconds to propagate bonding wave. Open chamber and remove wafers by picking up at the edge with tweezers.

5. Inspect: Take wafers to infrared inspection station. The switch to the whole setup is on the power bar under the station table. Check for voids due to trapped gases, making sure that the wafers do not touch the inspection station or your gloves. If there are gas pockets, try to squeeze them over to the edge of the wafer with the tweezers, and thus eliminate the void. Press from the middle to the edges of the wafer. If the bonding is very poor (due to particles) then set wafers aside so they can be split apart later, by immersing in water for a few minutes and then inserting tweezer edge between wafers.

6. Anneal: When all pairs have been contacted, load good pairs into tube in ICL for anneal. See bonding anneal process for details. If dopant spreading is not a problem, a higher anneal temperature (eg.1100°C) provides a better bond.

7. Turn off gases to bonding chamber. Clean up RCA station. Leave tweezers out on bonding table for use in IR inspection of wafers after anneal.

8. After anneal: Unload wafers and reset tube nitrogen flow to 20%. Check wafers at inspection station. Put tweezers, carrier and handle back in appropriate boxes under shelf. Make sure gases and inspection station are turned off.

Appendix C

Controlled ambient bonding apparatus

This appendix contains details of the controlled ambient bonding apparatus described in section 4.2, and illustrated here again.

The bonding chamber is a modified single wafer spinner manufactured by Laurell Technologies [97]. The chuck has been replaced with a specially designed Teflon version incorporating shims to hold the wafers apart. Chuck dimensions are given in figure C-2. The cover has two inlet ports, one of which holds the post to knock the shims out and allow the wafers to come into contact, and the other holding a central post to initiate bonding at the center of the wafers. The gases are controlled via flowmeters to set the ratio of N_2 to O_2, and mixed with a T-connector.

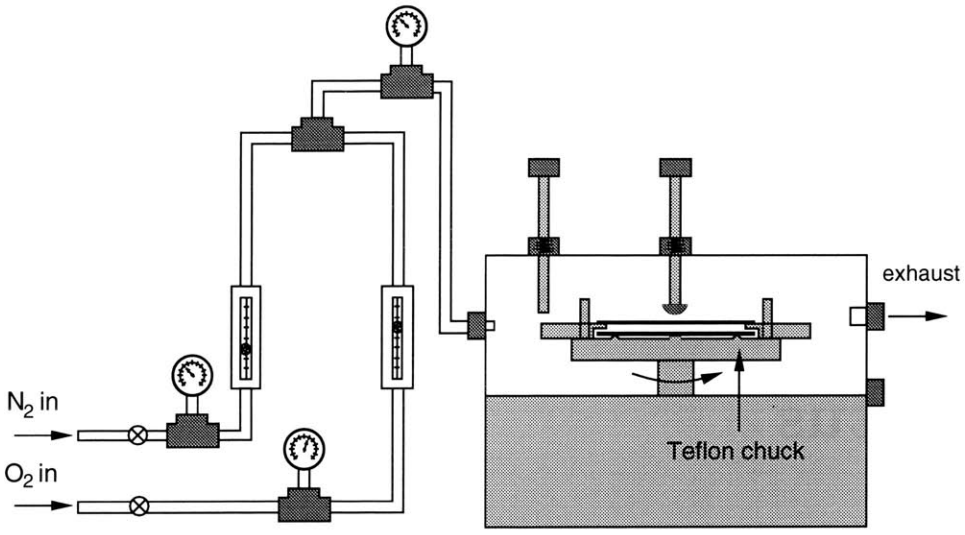


Figure C-1: Setup for controlled ambient bonding

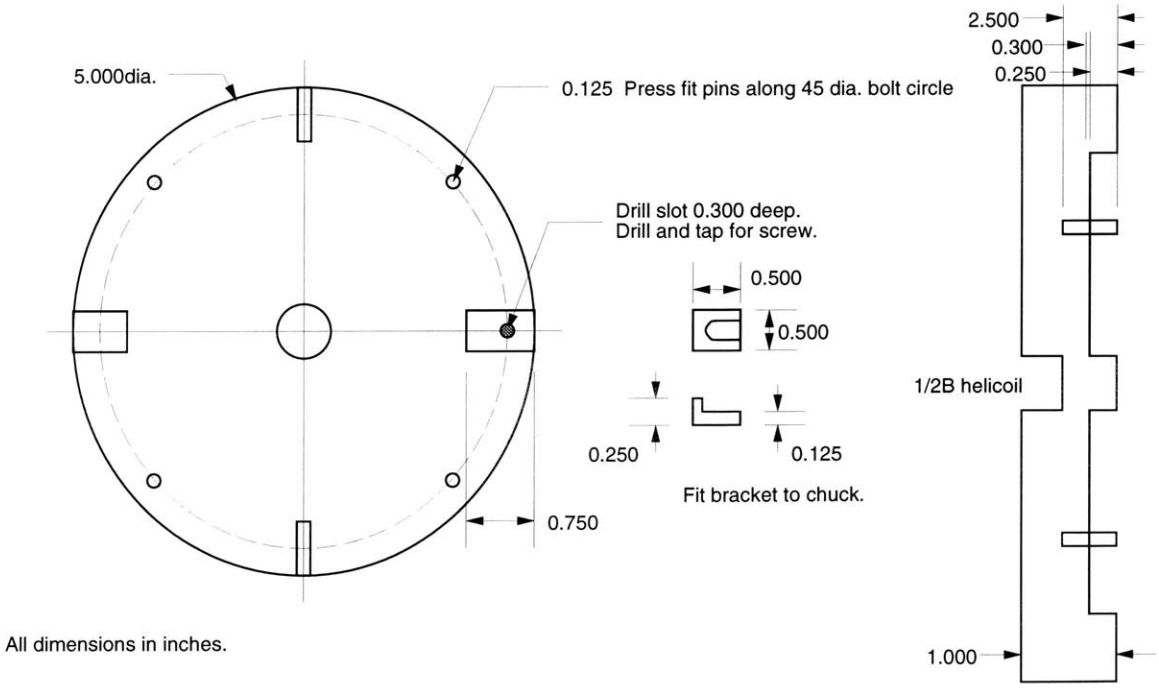


Figure C-2: Teflon wafer chuck specifications.

Appendix D

Yielding in silicon

The purpose of this appendix is to briefly describe the yield mechanism in silicon and the common criteria used to determine the onset of yielding.

Plastic deformation in single crystals takes place through slip (or glide) deformation, in which two sections of the crystal are displaced along a plane. This results in a shear deformation of the crystal. The slip occurs along specific planes and directions, and the driving force is the shear stress along the slip direction in the slip plane. For a purely tensile or compressive load, the shear stress resolved to the slip plane is given by:

$$\tau_r = \sigma \cos\lambda \cos\chi = \sigma\gamma \tag{D.1}$$

where γ is known as the Schmid factor and χ and λ are the angles from the load direction to the slip direction and normal to the slip plane respectively (see fig. D-1). In a perfect crystal, the ideal

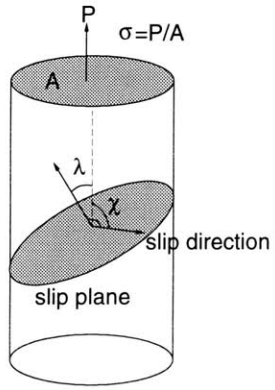


Figure D-1: Calculating resolved shear stress.

strength can be calculated from the knowledge of the structure of the crystal, and is usually in the range of 0.03-0.3G where G is the shear modulus. However in reality slip occurs at a much lower stress since it generally does not occur everywhere simultanously but only along a few planes where there are pre-existing defects. Thus the dislocations are generated heterogenously under a much lower stress, and are usually initiated at the surface and propagated into the bulk, or at internal point defect sites.

The aim of this appendix is to define both the mechanism of yielding in single crystal silicon, and some common yield conditions.

D.1 Calculating resolved shear stress in silicon

Single crystal silicon preferentially exhibits slip along the (110) set of directions, between [111] planes. Dislocations are initiated when the stress resolved to this system exceeds the critical resolved shear stress (CRSS). Therefore, the stress tensor must be resolved to this slip system. This is done by obtaining the direction cosines for the stress components acting on each element of the structure. The resolved shear stress is given by:

$$\tau_{nb} = l_{rn} l_{rb} \sigma_r + l_{\theta n} l_{\theta b} \sigma_\theta \tag{D.2}$$

where l_{rn}, l_{rb}, $l_{\theta n}$, and $l_{\theta b}$ are the direction cosines in the radial (r) and tangential (θ) directions along the slip direction (110) (b) and normal to the slip plane (n). Referring to the diagram in figure D-2, the direction cosines for the stress vector σ are:

$$l_r = [\cos(\theta + \frac{\pi}{4}), \sin(\theta + \frac{\pi}{4}), 0] \tag{D.3}$$

$$l_\theta = [-\cos(\frac{\pi}{4} - \theta), \sin(\frac{\pi}{4} - \theta), 0] \tag{D.4}$$

and those of the slip system are:

$$l_n = \frac{[1\bar{1}1]}{\sqrt{3}} \tag{D.5}$$

$$l_b = \frac{[110]}{\sqrt{2}} \tag{D.6}$$

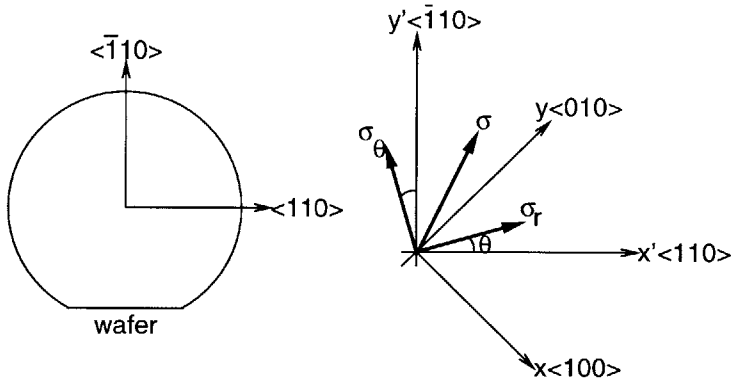


Figure D-2: Resolving plane stresses onto $< 110 > 111$ slip system.

Therefore, the resolved shear stress for this particular slip system becomes:

$$\tau_{nb} = \frac{\sin 2\theta}{\sqrt{6}}(\sigma_\theta - \sigma_r) \tag{D.7}$$

$$= \gamma \sin 2\theta(\sigma_\theta - \sigma_r) \tag{D.8}$$

The Schmid factor γ for this system is $\gamma = 0.41$. (The preceding analysis was taken from [75].)

D.2 Yield criteria

There are a number of criteria that are used to determine the onset of yielding in a material, the most commonly used being the maximum shear stress or Tresca condition, and the maximum distortion energy or von Mises condition. All of these criteria are usually defined in terms of the principal stresses on the element, and depend on the component of the total stress that is not hydrostatic, since hydrostatic stresses result only in an overall volume change.

The von Mises or maximum distortion yield condition requires that the shear stress on the octahedral plane exceeds the yield stress, and is obtained by resolving the total stress tensor onto the octahedral plane, which is that equally inclined to all of the three coordinate directions such that the direction cosines $\mu_x = \mu_y = \mu_z = \frac{1}{\sqrt{3}}$ (see fig. D-3). The von Mises yield condition is expressed as follows:

$$\tau_{OCT} = \frac{\sqrt{2}}{3}\sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_3^2 - \sigma_1\sigma_2 - \sigma_2\sigma_3 - \sigma_3\sigma_1} > \sqrt{\frac{2}{3}}\bar{k} \tag{D.9}$$

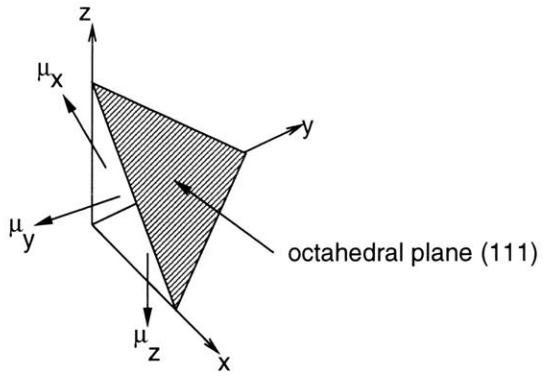


Figure D-3: Octahedral plane.

where $\bar{k}$ is the yield stress in pure shear. The von Mises condition is usually used for ductile materials, particularly metals.

Since the orientation of the principal stresses is not fixed with respect to the coordinate system of the body in question, but the octahedral planes do have a fixed orientation, this implies the assumption of isotropy of the yield stress $\bar{k}$. Also note that the resolved shear stress σ_s does not have a specific direction on the shear plane, thereby implying that for a uniaxial stress state, the yield stress is equal in tension and compression. The material should therefore have a high degree of symmetry for the preceding theories to be valid. (The preceding material was taken from [98].)

As previously described, in single crystals yielding occurs along specific planes and directions, so that in general, only stresses resolved to these systems will initiate slip. Note that the slip plane for silicon is the 111 plane, which is in fact identical to the octahedral plane. If the octahedral shear stress definition is compared to the resolved shear stress definition (with the assumption that $\sigma_3 = 0$ for plane stress), $\tau_{OCT} > \tau_{nb}$ so that the von Mises condition is more conservative than the "exact" resolved shear stress criterion. Therefore the use of the von Mises criterion for determining yield provides a fairly conservative representation of the actual yielding.

Appendix E

Plastic deformation program

The following is the program listing for program "allstress" which calculates maximum von Mises stresses in square and circular sealed cavity plates as a function of temperature.

```
/*************************************************************************

Program allstress.c

Calculate stress vs. temperature for circular and square plates
-uses Timoshenko (circle) or Hooke (square) approximation for deflection
 and FEM extracted solutions for stresses

Lalitha Parameswaran

*************************************************************************/

#define Tstep 25.      /* temperature increments      */
#define numsteps_c 200      /* circle - radial divisions      */
#define numsteps_s 30      /* square - side divisions      */
#define numtemp 46      /* number of temperature steps      */

#include <stdio.h>
#include <stdlib.h>
#include <ctype.h>
#include <math.h>
#include "constants.h"
#include "constants_hooke.h"
#include "mylib.h"

extern double a,h,L,D,Deff,Pres,Pext,Pcav;
```

```
double a,h,L,D,Deff,Pres,Pext,Pcav;

/********************** Output files ****************************/

/* file 'out_stress' contains output data as follows:
Temp, center defl., Pcav, Smises@edge, Smises@center, yield stress@T, flow stress@T */
FILE *outfile;

/********************** Internal functions **********************/

/* calculate large deflection with Timoshenko energy method sol'n */
double w_large(double q) {
      double k1,k2,w,temp1,temp2;
      k1=fabs(q)*a*a*a*a/(64*Deff); k2=0.488/(h*h);
      temp1=0.5*k1/k2 + sqrt(3.0)*sqrt((4.0+27.0*k1*k1*k2)/k2)/(18.0*k2);
      temp2=pow(temp1,0.3333333);
      w=temp2 - 1/(3*k2*temp2);
      if (q<0) w= -w;
      return (w*Kwfem);}

/************************** Main program ************************/

main(argc,argv)
      int argc;
      char *argv[];
{
      int i, j, k, m, iter, index;
      char *shape;
      double temp,err;
      double q,wo,V1,V2,PVT1,B,Q,q1,q2,Wo;
      double flow,yield,smises_edge,smises_cent;

      double *W = (double *)malloc(MAXSTEPS * sizeof(double));
      double *r = (double *)malloc(MAXSTEPS * sizeof(double));
      double *T = (double *)malloc(MAXSTEPS * sizeof(double));
      double *x = (double *)malloc(MAXSTEPS * sizeof(double));
      double *y = (double *)malloc(MAXSTEPS * sizeof(double));
      double **w = (double **)malloc(MAXSTEPS * sizeof(double));
      double **wu = (double **)malloc(MAXSTEPS * sizeof(double));
      double **wv = (double **)malloc(MAXSTEPS * sizeof(double));
      for(i = 0; i < MAXSTEPS; i++)   {
            w[i] = (double *)malloc(MAXSTEPS * sizeof(double));
            wu[i] = (double *)malloc(MAXSTEPS * sizeof(double));
            wv[i] = (double *)malloc(MAXSTEPS * sizeof(double));
      }
```

```
/*-------------------------------------------------------------------*/

      /* get inputs */

      if (argc!=7)      {
         printf("\nFormat: allstress shape radius thickness depth Presidual Pexternal \n");
         printf("\nUnits in microns and atmospheres.\n");
         printf("Select shape - c for circle, s for square.\n");
         printf("Output file is out_stress.\n\n");return(0);
      }

      shape=argv[1];
      if (*shape!='c' && *shape!='s')      {
            printf("Select shape - c for circle, s for square.\n\n");
            return(0);      }

      a=atof(argv[2])/1e6;            /* radius */
      if (*shape=='s') a=a*0.5;
      h=atof(argv[3])/1e6;            /* thickness */
      L=atof(argv[4])/1e6;            /* cavity depth */
      Pres=atof(argv[5])*Patm;      /* residual pressure */
      Pext=atof(argv[6])*Patm;      /* ambient pressure */

      outfile=fopen("out_stress","w");
      fprintf(outfile,"%d %e %e %e %e %e\n",numtemp,a,h,L,Pres,Pext);

/*-------------------------------------------------------------------*/

      D=Ey*h*h*h/(12*(1-v*v));      /* ideal flexural rigidity */

      /* calculate deflection wo at STP */

      q=Pres-Pext;
      Deff=Deff_func(q);
      if (*shape=='c')      {
            wo=w_large(q);
            B = findb(wo,q,0.0,numsteps_c);
            V1= V_circle(wo,B);
            if (wo<-L) printf("Plate touched down at radius = %6.2fum.\n",B*1e6);
            /* calculate deflection as function of radius: w(r) */
            for (j=0;j<=numsteps_c;j++) {
                  r[j]=j*a/numsteps_c;
                  W[j]=wo*(1-r[j]*r[j]/(a*a))*(1-r[j]*r[j]/(a*a));
            }

      }else      {
```

```
        Wo=w_hooke(x,y,w,wu,wv,q,numsteps_s);
        wo=Wo*h/K1;
        if (wo<-L)  printf("Plate touched down.\n");
        V1=V_hooke(x,y,w,q,numsteps_s);
}
printf("\nUnconstrained deflection at room temp = %6.2fum.\n\n",wo*1e6);

printf("Temp(C)  W(um)  Pcav(atm) Smises_e Smises_c Yield   R_touch \n\n");

/* loop for all temperatures */

Pcav=Pres;
for (i=0;i<=numtemp;i++)
{
        T[i]=i*Tstep+273.0+25.0;
        PVT1=T[i]*Pres*V1/Troom;

        if (Pres!=0.0)      {

                /* find cavity pressure Pcav for given temp T
                using ideal gas law and iterating on pressure */

                    iter=0;
                do {
                        iter++;
                        Pcav=Pcav*1.0002;
                        q=Pcav-Pext;
                        Deff=Deff_func(q);
                        if (*shape=='c')      {
                                wo=w_large(q);
                                temp=B;
                                B=findb(wo,q,temp,numsteps_c);
                                  V2= V_circle(wo,B);
                        } else      {
                                Wo=w_hooke(x,y,w,wu,wv,q,numsteps_s);
                                V2=V_hooke(x,y,w,q,numsteps_s);
                        }
                        err=(Pcav*V2/PVT1);
                } while (fabs(1-err)>1e-2 && iter<MAXITER);
        }

        if (*shape=='c')      {
                if (wo>-L)      {
                        /* plate not touched down - calculate w(r) and stress dist. */
                        q=Pcav-Pext;
                        for (j=0;j<=numsteps_c;j++)
```

```
                W[j]=wo*(1-r[j]*r[j]/(a*a))*(1-r[j]*r[j]/(a*a));
      } else
            /* touched down - find touch radius index in deflection W */
            index=w_general(W,B,numsteps_c);
} else      {
      wo=Wo*h/K1;
}

/* calculate stresses using fitted parameters from FEM */

if (wo>-L)      {
      /* not touched down */

      if (*shape=='c')      {
            smises_cent=fabs(0.44791*0.75*q*(a/h)*(a/h));
            smises_edge=fabs(0.45727*0.75*q*(a/h)*(a/h));
      } else {
            smises_cent=fabs(0.28391*0.3078*q*(a/h)*(a/h));
            smises_edge=fabs(0.66768*0.3078*q*(a/h)*(a/h));
      }

} else      {
      /* touched down */

      Q=q/101300.0;
      if (*shape=='c')      {
            q1= 0.0012959*Q*Q+0.0089383*Q+0.0076088 + 0.0204*(L*1e6-2);
            q2= -8.1042*Q*Q+30.143*Q+2.1735 + 0.1077*(L*1e6-2);
            smises_cent=fabs(1e6*(q1*(a/h)+q2)*sqrt(6e-6/h));
            q1= -0.031058*Q*Q+0.024553*Q-0.0073337 + 0.0018*(L*1e6-2);
            q2= -14.399*Q*Q+59.662*Q+13.404 + 13.765*(L*1e6-2);
            smises_edge=fabs(1e6*(q1*(a/h)+q2)*sqrt(6e-6/h));
      } else {
            q1= -0.0098017*Q*Q+0.017617*Q+0.01058 + 0.0118*(L*1e6-2);
            q2= -8.4512*Q*Q+30.143*Q+2.1735 - 0.4916*(L*1e6-2);
            smises_cent=fabs(1e6*(q1*(a/h)+q2)*sqrt(6e-6/h));
            q1= -0.011089*Q*Q-0.032255*Q-0.044541 - 0.0225*(L*1e6-2) ;
            q2= -24.391*Q*Q+99.563*Q+38.488 + 29.1634*(L*1e6-2);
            smises_edge=fabs(1e6*(q1*(a/h)+q2)*sqrt(6e-6/h));
            Wo=-L*K1/h; wo= -L;
            B=0.0;
      }
}

yield=yieldfunc(T[i]-273.0,1);
flow=flowfunc(T[i]-273.0);
```

```
            /* output data to screen and file */

            printf("%5.0fC %6.2fum %5.3fatm %8.3f %8.3f %7.2f %6.2fum",
             T[i]-273,wo*1e6,Pcav/Patm,smises_edge/1e6,smises_cent/1e6,yield/1e6,B*1e6);
            if (smises_edge>yield) printf("*e");
            if (smises_cent>yield) printf("*c");
            printf("\n");
            if (wo< -L) temp=-L; else temp=wo;

            fprintf(outfile,"%f %e %e %e %e %e\n",
                    T[i],temp,Pcav,smises_edge,smises_cent,yield,flow);

      }

      fclose(outfile);
}
/******************************** END **********************************/
```

The following is a listing of the subroutines used in the program "allstress".

```
/*************************************************************************
/*--------- procedures used in program allstress.c ---------*/

#include "constants.h"
#include "constants_hooke.h"
#include <math.h>
extern double a,h,L,D,Deff,Pres,Pext,Pcav;

/*-------------------------------------------------------------------------
Coefficients to calculate w(r)
the coefficients were obtained from the following solution of 5 equations
where w=c1+c2*log(r)+c3*r^2+c4*r^2*log(r)+k*r^4 and k=P/64D and
b is the radius of the touched-down region
and the boundary conditions are: w(a)=0, w(b)=-d, w'(a)=0, w'(b)=0, Mr(b)=0

[c1,c2,c3,c4,k]=solve({c1+c2*log(a)+c3*a^2+c4*a^2*log(a)+k*a^4=0,
                       c1+c2*log(b)+c3*b^2+c4*b^2*log(b)+k*b^4=-L,
                       c2/a+2*a*c3+c4*(a+2*a*log(a))+4*k*a^3=0,
                       c2/b+2*b*c3+c4*(b+2*b*log(b))+4*k*b^3=0,
                       -D*(-c2/b^2+2*c3+c4*(3+2*log(b))+12*k*b^2+
                          v*(c2/b^2+2*c3+c4*(1+2*log(b))+4*k*b^2)=0)},
                          {c1,c2,c3,c4,k})
-------------------------------------------------------------------------*/
double wcoeff(double b, double KW[6])      {
      double a2, a4, a6, b2, b4, b6;
      double denom;

      a2=a*a;       a4=a*a*a*a;       a6=a*a*a*a*a*a;
      b2=b*b;       b4=b*b*b*b;       b6=b*b*b*b*b*b;

      denom=16*b4*a2*log(a)*log(b)-8*b4*a2*log(a)*log(a)
            -8*b4*a2*log(b)*log(b)+b6+4*a4*log(a)*b2
            -6*a2*log(a)*b4-4*log(b)*a4*b2+6*log(b)*a2*b4-3*a6
            +2*a6*log(a)-2*log(b)*a6+7*a4*b2-5*a2*b4;
      KW[1]= -L*a2*(2*a4*log(a)-2*a4*log(b)-3*a4+3*a2*b2-8*b4*log(a)*log(a)
             +8*b4*log(a)*log(b)+4*b2*a2*log(a)-4*log(b)*b4)/denom;
      KW[2]= 4*b2*a2*L*(-2*b2*log(a)+2*b2*log(b)+a2-b2)/denom;
      KW[3]= -4*L*(a4*log(b)+a4-a2*b2-2*b2*a2*log(a)+log(b)*b4)/denom;
      KW[4]= 4*L*(a2-b2)*(a2-b2)/denom;
      KW[5]= -L*(2*a2*log(a)-2*log(b)*a2-a2+b2)/denom;
}
/*-------------------------------------------------------------------------
calculate w(r) using general equation from Timoshenko:
```

```
      w=A+Blog(r)+Cr^2+Dr^2log(r)+Er^4
-------------------------------------------------------------------------*/
int w_general(double *w, double b, int numsteps)      {
      double KW[6],r;
      int index,j;

      wcoeff(b,KW);
      for (j=0;j<=numsteps;j++)      {
            r=j*a/numsteps;
            if (r<=b)      {w[j]= -L; index=j;}
            else  w[j]=KW[1]+KW[2]*log(r)+KW[3]*r*r+KW[4]*r*r*log(r)+KW[5]*r*r*r*r;
      }
      w[numsteps]=0;
      return (index);
}
/*-------------------------------------------------------------------------
find Deffective - from W.Ko's paper
-------------------------------------------------------------------------*/
double Deff_func(double P)      {
      double phi1,phi2,term1,term2,temp1,temp2;

      phi1 = (64.0*h/(P*a*a*a*a))*(64.0*h/(P*a*a*a*a));
      phi2 = 0.3187*pow((1 + 0.703*(int_stress*a*a)/(Ey*h*h)),3);
      term1 = 1.0246*phi1/D; term2 = term1*term1 + pow(phi1,3.0)*phi2;
      temp1=term1+sqrt(term2); temp2=term1-sqrt(term2);
      temp1= pow(temp1,0.3333333);
      if (temp2>0.0) temp2=pow(temp2,0.3333333);
      else temp2= -pow(fabs(temp2),0.3333333);
      return (1/(temp1 + temp2));
}
/*-------------------------------------------------------------------------
find touchdown radius b using equation for k=P/64D
and coefficients from function wcoeff
-------------------------------------------------------------------------*/
double findb(double wo, double q, double b_old, int numsteps)      {
      double b,KW[6];

      if (wo< -L) {
            if (b_old==0.0)      b=a*sqrt(1-sqrt(fabs(L/wo))); else b=b_old+5e-6;
            do {
                  wcoeff(b,KW);
                  b=b-0.1e-6;
            } while (fabs((KW[5]*64*Deff-q)/q)>5e-3);
      }
      else      b=0.0;
      return (b);
```

```
}
/*-------------------------------------------------------------------------
calculate flow stress from Patel and Chaudhri paper, T in celcius
-------------------------------------------------------------------------*/
double flowfunc(double T)       {
        double temp;
        temp= -0.0029226*T;
        return 1e6*5361.6*pow(10.0,temp);
}
/*-------------------------------------------------------------------------
calculate yield stress from Patel and Chaudhri paper, T in celcius
-------------------------------------------------------------------------*/
double yieldfunc(double T,int stype)    {
        /* stress type: 1= strain rate is 5e-3 cm/min
                        2= strain rate is 5e-2 cm/min
                        3= strain rate is 5e-1 cm/min   */
        double temp;
        if (stype==1)   {
                if (T>622.0)    temp= -0.0041*T+4.3858;
                else            temp=log10(62.0);       }
        else    if (stype==2)   {
                if (T>717.0)    temp= -0.0041*T+4.7107;
                else            temp=log10(62.0);       }
        else if (stype==3)      {
                if (T>822.0)    temp= -0.0039*T+4.9900;
                else            temp=log10(62.0);       }
        return 9.81e6*pow(10.0,temp);
}
/*-------------------------------------------------------------------------
Calculate matrices for deflections in x,y,z using Hooke's series solutions
-------------------------------------------------------------------------*/
double w_hooke(double *x,double *y,double **w,double **wu,double **wv,double q,int numsteps)
      int i,j,k;
      double X,Y,W,U,V,w1,w3,s2,t2,Wo,Q,errs,temp1,temp2,Sq;

        /* solve for central deflection Wo using Q = a1*Wo + a3*Wo^3 */

      if (q>0) Sq=1.0;      else Sq= -1.0;
      Q=K1*a*a*a*a*fabs(q)/(Deff*h);            /* normalized load */
      temp1=0.5*Q/alpha3 +
        sqrt(3.0)*sqrt((4.0*alpha1*alpha1*alpha1+27.0*Q*Q*alpha3)/alpha3)/(18.0*alpha3);
      temp2=pow(temp1,0.3333333);
      Wo=temp2 - alpha1/(3*alpha3*temp2);
      Wo=Wo*Kwfem;

      /* calculate deflection matrices w,wu,wv */
```

```
        for (i=0;i<=numsteps;i++)       {
           x[i] = -a + 2*(i)*a/numsteps;
           X=x[i]/a;

           for (j=0;j<=numsteps+1;j++)     {
              y[j] = -a + 2*(j)*a/numsteps;
              Y=y[j]/a;

              w1=(1-X*X)*(1-X*X)*(1-Y*Y)*(1-Y*Y)*
                 (1+Ka*X*X+Kb*Y*Y+Kc*X*X*X*X+Kd*Y*Y*Y*Y+Ke*X*X*Y*Y);
              w3=(1-X*X)*(1-X*X)*(1-Y*Y)*(1-Y*Y)*
                 (Kt*X*X+Ku*Y*Y+Kv*X*X*X*X+Kw*Y*Y*Y*Y+Kz*X*X*Y*Y);
              s2=X*(1-X*X)*(1-Y*Y)*
                 (Kf+Kg*X*X+Kh*Y*Y+Kj*X*X*X*X+Kk*Y*Y*Y*Y+Kl*X*X*Y*Y);
              t2=Y*(1-X*X)*(1-Y*Y)*
                 (Km+Kn*X*X+Kp*Y*Y+Kq*X*X*X*X+Kr*Y*Y*Y*Y+Ks*X*X*Y*Y);
              W=w1*Wo+w3*Wo*Wo*Wo;
              U=s2*Wo*Wo;
              V=t2*Wo*Wo;
              w[i][j]=Sq*W*h/K1;
              wu[i][j]=U*h*h/(12*a);
              wv[i][j]=V*h*h/(12*a);
           }
      }
      return(Wo*Sq);
}
/*-------------------------------------------------------------------------
Calculate volume of cavity with (touched-down) deflected square membrane
-------------------------------------------------------------------------*/
double V_hooke(double *x,double *y,double **w,double q,int numsteps) {
      int i,j;
      double dx,dy,sum;

      sum=0.0;
      dx=fabs(x[2]-x[1]);
      dy=fabs(y[2]-y[1]);
      for (i=0;i<=numsteps;i++)
            for (j=0;j<=numsteps;j++)
                  if (w[i][j]> -L)      sum=sum+w[i][j]*dx*dy;
                  else                  sum=sum-L*dx*dy;
      return (4*a*a*L+sum);
}
/*-------------------------------------------------------------------------
Calculate volume of cavity with (touched-down) deflected circular membrane
-------------------------------------------------------------------------*/
```

```
double V_circle(double wo,double B) {
      if (wo> -L)       return (pi*a*a*L + pi*wo*a*a/3);
      else             return (pi*a*a*L - pi*L*(a-B)*(a-B)/3 - pi*B*B*L);
}
            for (i=1;i<=numsteps;i++)      {if (x[i]<temp)      temp=x[i];}
      return (temp);
}
```

Appendix F

Motorola pressure sensor details

The layout for the sensors are given in the following figures. The piezoresistors were nominally 3200Ω, with a sheet resistance of 320Ω/□, and the resistors were placed 25μm in from the edge of the plate. The minimum feature size was 8μm (for the piezoresistor width). The device fabrication is as follows:

- Starting wafers:
  - Handle wafer - n-Si (Phos doping) ρ=1Ωcm
  - Device wafer - 11μm n-epi (As doping), on p-substrate
- At MIT: sealed cavity preparation
  - Etch cavities.
  - Bond wafers.
  - Thin wafers with electrochemistry.
- At Motorola:
  - Pattern and implant p- piezoresistors.
  - Pattern and implant p+ resistor leadouts.
  - Pattern and implant n+ frontside contact areas.
  - Deposit dielectric layer (LTO).
  - Open contact holes.
  - Deposit and etch aluminum.

Measured resistor parameters are given in table F.1 and gauge factors used to calculate the curves in figure 6-1 are in table F.2 [92].

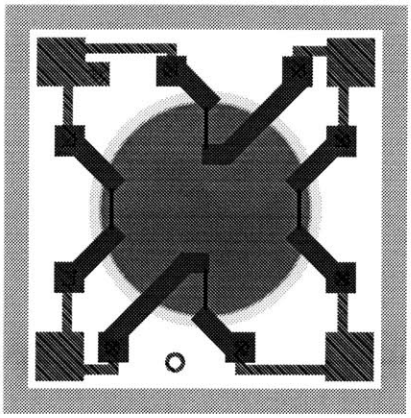


Figure F-1: Motorola piezoresistive pressure sensor - circular plate.

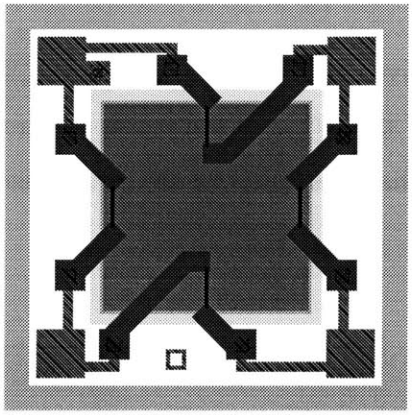


Figure F-2: Motorola piezoresistive pressure sensor - square plate.

Parameter	Value
Resistor	3120±118Ω
Sheet ρ	307.4±4.88Ω/□
Junction depth	3.03μm(from suprem)
Avg. resistivity	9.31Ωcm

Table F.1: Motorola sensor piezoresistor data.

Temperature (°C)	$\pi_l \times 10^{11}$/Pa	$\pi_t \times 10^{11}$/Pa
-40	93.3	-86.2
0	79.0	-72.9
25	71.8	-66.3
85	61.0	-56.4
125	53.9	-49.7

Table F.2: Motorola sensor - gauge factors.

Appendix G

Parasitic capacitances

The layout for the discrete and hybrid sensors are given in figures G-1 and G-2 respectively. The tables contain parasitic capacitances from leads and bondpads for each of the sensors.

Device #	Radius (μm)	C_{top}	C_{bottom}	$C_{parasitic}$
d1	350	3.7638	3.5221	1.8195
d2	240	3.0042	2.9282	1.4828
d3	200	4.3163	4.2127	2.1319
d11	240	5.7114	7.7901	3.2954
d12	350	2.7970	5.1105	1.8077
d13	350	17.1341	16.2570	8.3420
d14	240	14.4614	13.7501	7.0484
d15	200	11.7957	11.1534	5.7328
d23	240	6.0981	7.9282	3.4469
d24	350	3.2804	5.1934	2.0105

Table G.1: Parasitic capacitances associated with discrete pressure sensors, for 5000Å field oxide. Device # refers to mask figure G-1, devices are numbered d1-d24 in 4 rows.

Device #	Radius (μm)	C_{top}	C_{bottom}	$C_{parasitic}$
h1	130	5.5871	2.4137	1.6855
h2	240	2.5691	1.3881	0.9012
h3	240	5.3481	2.5725	1.7370
h4	130	3.3080	1.4088	0.9881
h5	130	4.9655	2.5518	1.6856
h6	240	2.6312	1.3432	0.8893
h7	240	5.8840	2.5967	1.8016
h8	130	3.5843	1.5711	1.0923

Table G.2: Parasitic capacitances associated with hybrid pressure sensors, for 5000Å field oxide. Device # refers to mask figure G-2, devices are numbered d1-d8 in 4 columns.

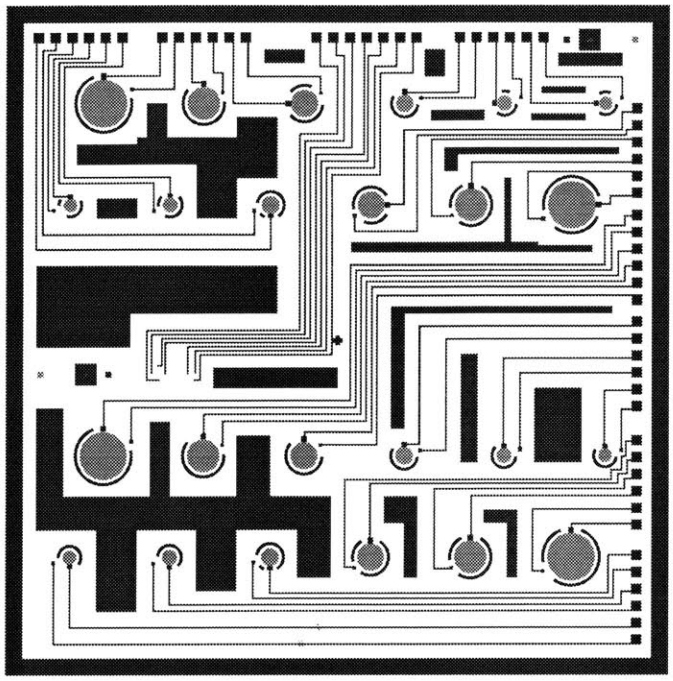


Figure G-1: Mask layout for discrete pressure sensors. Chip is 1cm square.

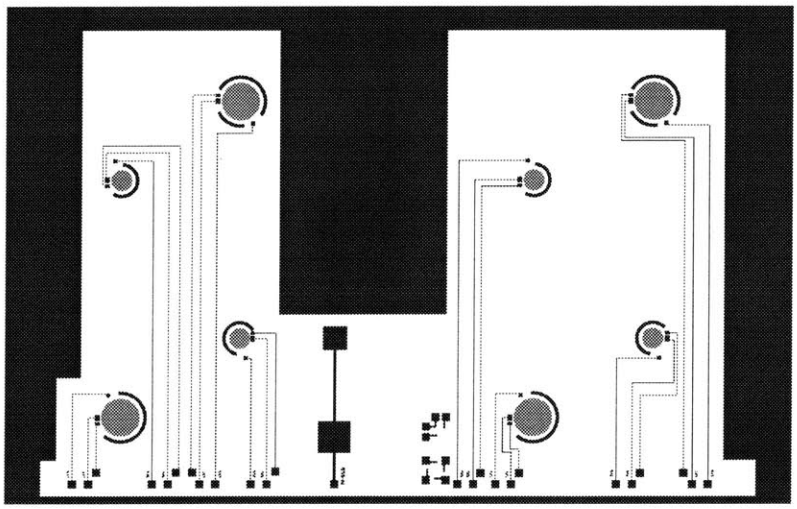


Figure G-2: Mask layout for hybrid pressure sensors. Chip is 1cm x 0.6cm.

References

[1] R. Feynman. There's plenty of room at the bottom. *IEEE Journal of Microelectromechanical Systems*, 1, No.1:60–66, 1992.

[2] K.E. Petersen. Silicon as a mechanical material. *Proceeding of the IEEE*, 70, No.5:420–457, 1982.

[3] S. Middelhoek and S. Audet. *Silicon sensors.* Delft University of Technology, 1994.

[4] Motorola Semiconductor Products Sector. *Motorola Sensor Device Data.*

[5] M. Parameswaran, A.M. Robinson, D.L. Blackburn, M. Gaitan, and J. Geist. Micromachined thermal radiation emitter from a commercial CMOS process. *IEEE Electron Device Letters*, 12, No.2:57, 1991.

[6] R. Leggenhager, H. Baltes, J. Peer, and M. Forster. Thermoelectric infrared sensors by CMOS technology. *IEEE Electron Device Letters*, 13, No.9:454, 1992.

[7] G.T. Mulhern, D.S. Sloan, and R.T. Howe. Supercritical carbon dioxide drying of microstructures. In *Transducers '93 - 7th Int. Conf. on Solid-State Sensors and Actuators*, pages 296–299. IEEE, 1993.

[8] C.H. Mastrangelo and C.H. Hsu. Mechanical stability and adhesion of microstructures under capillary forces. *IEEE Journal of Microelectromechanical Systems*, Vol.2, No.1:33–62, 1993.

[9] P. Krulevitch, R.T. Howe, G.C. Johnson, and J. Huang. Stress in undoped LPCVD polycrystalline silicon. In *Transducers '91 - 6th Int. Conf. on Solid-State Sensors and Actuators*, pages 949–952. IEEE, 1991.

[10] J.H. Smith, S. Montague, and J.J. Sniegowski. Material and processing issues for the monolithic integration of microelectronics with surface-micromachined polysilicon sensors and actuators. In *Proceedings SPIE, Vol.2639*, pages 64–73, 1995.

[11] W. Kuehnel and S. Sherman. Surface micromachined silicon accelerometer with on-chip detection circuitry. *Sensors and Actuators A*, A45:7–16, 1994.

[12] K.W. Markus, D.A. Koester, A. Cowen, R. Mahadevan, V.R. Dhuler, D. Roberson, and L. Smith. MEMS infrastructure: The multi-user MEMS processes (MUMPs). In *Proceedings SPIE, Vol.2639*, pages 54–63, 1995.

[13] K. Warren. Navigation grade silicon accelerometers with sacrificially etched SIMOX and BESOI structure. In *Tech.Digest, IEEE Solid State Sensor and Actuator Workshop*, pages 69–72. IEEE, 1994.

[14] P. Horwath, A. Erlebach, R. Köhler, and H. Kück. Miniature condenser microphone with a thin silicon membrane fabricated on SIMOX substrate. In *Transducers '95 - 8th Int. Conf. on Solid-State Sensors and Actuators*, pages 696–699, 1995.

[15] B. Diem, P. Rey, S. Renard, S. Bosson, H. Bono, F. Michel, M. Delaye, and G. Delapierre. SOI SIMOX: from bulk to surface micromachining, a new age for silicon sensors and actuators. *Sensors and Actuators A*, A46-47:8–16, 1995.

[16] J.H. Smith, S. Montague, J.J. Sniegowski, J.R. Murray, and P.J. McWhorter. Embedded micromechanical devices for the monolithic integration of MEMS with CMOS. In *Tech.Digest IEDM*, pages 609–612. IEEE, 1995.

[17] Y.B. Gianchandani, K.J. Ma, and K. Najafi. A CMOS dissolved wafer process for integrated p++ microelectromechanical systems. In *Transducers '95 - 8th Int. Conf. on Solid-State Sensors and Actuators*, pages 79–82, 1995.

[18] E.W. Becker, W. Ehrfeld, P. Hagmann, A. Maner, and D. Munchmeyer. Fabrication of microstructures with high aspect ratios and great structural heights by synchrotron radiation lithography, galvanoforming and plastic molding (LIGA process). *Microelectronic Engineering*, 4:35, 1986.

[19] J.J. Pak, G.W. Neudeck, A.E. Kabir, D.W. DeRoo, S.E. Staller, and J.H. Logsdon. A new method of forming a thin single-crystal silicon diaphragm using merged epitaxial lateral overgrowth for sensor applications. *IEEE Electron Device Letters*, 11, No.11:614, 1991.

[20] K.A. Shaw, L.Z. Zhang, and N.C. MacDonald. SCREAM I: A single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures. *Sensors and Actuators A*, A40:63–70, 1994.

[21] W. Kern and D. Puotinen. Cleaning solution based on hydrogen peroxide for use in semiconductor technology. *RCA Review*, page 187, 1970.

[22] W.P. Maszara, G. Goetz, A. Caviglia, and J.B. McKitterick. Bonding of silicon wafers for silicon-on-insulator. *Journal of Applied Physics*, 64, No.10:4943, 1988.

[23] R. Stengl, T. Tan, and U. Gösele. A model for the silicon wafer bonding process. *Japanese Journal of Applied Physics*, 28, No.10:1735, 1989.

[24] S. Bengtsson. Semiconductor wafer bonding: a review of interfacial properties and applications. *Journal of Electronic Materials*, 21, No.8:841, 1992.

[25] G. Kissinger and W. Kissinger. Void free silicon wafer bond strengthening in the 200-400c range. *Sensors and Actuators A*, A36:149–156, 1993.

[26] E.F. Cave. Method of making a composite insulator semiconductor wafer. *U.S. Patent No. 3,203,760*, 1966.

[27] J.B. Lasky. Wafer bonding for silicon-on-insulator technologies. *Applied Physics Letters*, 48, No.1:78, 1986.

[28] A. Nakagawa, K. Watanabe, Y. Yamaguchi, H. Ohashi, and K. Furukawa. 1800v bipolar-mode mosfets: A first application of silicon wafer direct bonding (SDB) technique to power device. In *Tech.Digest, IEDM*, pages 122–125. IEEE, 1986.

[29] K. Petersen, J. Brown, T. Vermullen, P. Barth, J. Mallon, and J. Bryzek. Ultra-stable, high-temperature pressure sensors using silicon fusion bonding. *Sensors and Actuators A*, A21-23:96–101, 1990.

[30] K. Petersen, P.W. Barth, J. Poydock, J. Brown, J. Mallon, and J. Bryzek. Silicon fusion bonding for pressure sensors. In *Tech.Digest, Solid-State Sensor and Actuator Workshop*, page 144. IEEE, 1988.

[31] F. Rudolf, A. Jornod, and P. Bencze. Silicon microaccelerometer. In *Transducers '87 - 4th Int. Conference on Solid-State Sensors and Actuators*, pages 395–398. IEEE, 1987.

[32] M.A. Huff, M.S. Mettner, T.A. Lober, and M.A. Schmidt. A pressure-balanced electrostatically-actuated microvalve. In *Tech.Digest, Solid-State Sensor and Actuator Workshop*, pages 123–127. IEEE, 1990.

[33] A. Padmanabhan, H.D. Goldberg, K. Breuer, and M.A. Schmidt. A wafer-bonded floating-element shear stress microsensor with optical position sensing by photodiodes. *IEEE Journal of Microelectromechanical Systems*, 5, No.4:307–314, 1996.

[34] H. Wada, T. Kamijoh, and Y. Ogawa. Direct bonding of inp to different materials for optical devices. In *Proceedings of Symposium on Semiconductor Wafer Bonding Science, Technology and Applications*, pages 579–591. Electrochemical Society, 1995.

[35] Hoya Glass.

[36] W. Ko, J. Suminto, and G. Yeh. Bonding techniques for microsensors. In *Micromachining and Micropackaging of Transducers*. Elsevier Science Publishers, 1985.

[37] J.J. Lutsky, R. Naik, C.G. Sodini, and R. Reif. Sealed cavity thin film resonator. In *Tech.Digest IEDM*, page 1. IEEE, 1996.

[38] R.J. Devoto. *Micromachined infrared detector using wafer bonding technology.* SM thesis, Massachusetts Institute of Technology, 1996.

[39] A.C.M Gieles. Subminiature silicon pressure transducer. In *Digest IEEE International Solid State Circuits Conference*, pages 108–109, 1969.

[40] S.K. Clark and K.D. Wise. Pressure sensitivity in anisotropically etched thin-diaphragm pressure sensors. *IEEE Transactions on Electron Devices*, ED-26, No.12:1887–1895, 1979.

[41] A. Haberli, O. Paul, P. Malcovati, M. Faccio, F. Maloberti, and H. Baltes. CMOS integration of a thermal pressure sensor system. In *IEEE International Symposium on Circuits and Systems*, pages 377–380. IEEE, 1996.

[42] A. Young. *Microfabricated pressure transducers based on anti-resonant reflecting optical waveguides.* PhD thesis, Massachusetts Institute of Technology, 1994.

[43] D. Burns, J.D. Zook, R. Horning, W. Herb, and H. Guckel. Sealed-cavity resonant microbeam pressure sensor. *Sensors and Actuators A*, A48:179–186, 1995.

[44] M. Motamedi. Acoustic sensor technology. In *IEEE International Microwave Symposium*, pages 521–524. IEEE, 1994.

[45] H. Dudaicevs, M. Kandler, Y. Manoli, W. Mokwa, and E. Speigel. Surface micromachined pressure sensors with integrated CMOS read-out electronics. *Sensors and Actuators A*, A43:157–163, 1994.

[46] C. Mastrangelo, X. Zhang, and W. Tang. Surface micromachined capacitive differential pressure sensor with lithographically defined silicon diaphragm. In *Transducers '95 - 8th Int. Conf. on Solid-State Sensors and Actuators*, pages 612–615, 1995.

[47] Y. Zhang and K. Wise. A high accuracy multi-element silicon barometric pressure sensor. In *Transducers '95 - 8th Int. Conf. on Solid-State Sensors and Actuators*, pages 608–611, 1995.

[48] S.P. Timoshenko. *Theory of Plates and Shells.* McGraw-Hill, 1940.

[49] J.A. Lloyd. PhD thesis, Massachusetts Institute of Technology, June 1997.

[50] X. Ding, L. Tong, W. He, J. Hsu, and W. Ko. Touch mode silicon capacitive pressure sensors. In *Proceedings ASME Winter annual meeting*, page 111, 1990.

[51] L. Rosengren, J. Söderkvist, and L. Smith. Micromachined sensor structures with linear capacitive response. *Sensors and Actuators A*, A31:200–205, 1992.

[52] H. Benzel, T. Kallfass, and E. Lueder. Highly linear capacitive pressure sensors with optimized electrode shapes. In *Tech.Digest IEDM*, pages 203–206. IEEE, 1993.

[53] Mario Rossi. *Acoustics and electroacoustics.* Artech House, 1988.

[54] M. Andrews, I. Harris, and G. Turner. A comparison of squeeze film theory with measurements on a microstructure. *Sensors and Actuators A*, A36:79–87, 1993.

[55] T. Gabrielson. Mechanical-thermal noise in micromachined acoustic and vibration sensors. *IEEE Transactions on Electron Devices*, ED-40, No.5:903–909, 1993.

[56] 3M Corporation. FC-129.

[57] H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgartel. Anisotropic etching of crystalline silicon in alkaline solutions. *Journal of the Electrochemical Society*, 137:3612, 1990.

[58] Y. Lee, N. Miyamoto, and I. Nishizawa. The lattice misfit and its compensation in the Si-epitaxial layer by doping with germanium and carbon. *Journal of the Electrochemical Society*, 122:530, 1975.

[59] H. Seidel. The mechanism of anisotropic electrochemical silicon etching in alkaline solutions. In *Tech.Digest, Solid-State Sensor and Actuator Workshop*, pages 86–91. IEEE, 1990.

[60] V.M. McNeil, S.S. Wang, and M.A. Schmidt. Issues regarding the application of the electrochemical etch-stop technique to fabricate structures using wafer bonding. In *Proceedings of Symposium on Semiconductor Wafer Bonding Science, Technology and Applications.* Electrochemical Society, 1991.

[61] V.M. McNeil, S.S. Wang, K-Y Ng, and M.A. Schmidt. An investigation of the electrochemical etching of (100) Si in CsOH and KOH. In *Tech.Digest, Solid State Sensor and Actuator Workshop*. IEEE, 1990.

[62] C.H. Hsu and M.A. Schmidt. Micromachined structures fabricated using a wafer-bonded sealed cavity process. In *Tech.Digest, Solid-State Sensor and Actuator Workshop*, pages 151–155, 1994.

[63] B. Kloeck, S. Collins, N. de Rooij, and R.L. Smith. Study of electrochemical etchstop for high precision thickness control of silicon membranes. *IEEE Transactions on Electron Devices*, ED-36, No.4:663–669, 1989.

[64] V.M. McNeil, M.J. Novack, and M.A. Schmidt. Design and fabrication of thin-film microaccelerometers using wafer bonding. In *Transducers '93 - 7th Int. Conf. on Solid-State Sensors and Actuators*, pages 822–825. IEEE, 1993.

[65] L. Parameswaran, V.M. McNeil, M.A. Huff, and M.A. Schmidt. Sealed cavity microstructure using wafer bonding technology. In *Transducers '93 - 7th Int. Conf. on Solid-State Sensors and Actuators*, pages 274–277. IEEE, 1993.

[66] L. Parameswaran. *Silicon pressure sensor using wafer bonding technology.* SM thesis, Massachusetts Institute of Technology, September 1993.

[67] P.K. Tedrow and C.G. Sodini. Twin well CMOS process, Version 1.3. Technical report, Massachusetts Institute of Technology, July 1993.

[68] Strahl & Pitsch Inc. Carnauba wax.

[69] 3M Corporation. Koh-resistant tape.

[70] U. Schnakenberg, W. Benecke, and P. Lange. TMAHW etchants for silicon micromachining. In *Transducers '91 - 6th Int. Conf. on Solid-State Sensors and Actuators*, pages 815–818, 1991.

[71] O. Tabata. pH-controlled TMAH etchants for silicon micromachining. *Sensors and Actuators A*, A53:335–339, 1996.

[72] C.H. Hsu. Personal communication.

[73] J.R. Patel and A.S. Choudhri. *Journal of Applied Physics*, 34:2788, 1963.

[74] I. Yonenaga. Upper yield stress of Si crystals at high temperatures. *Journal of the Electrochemical Society*, 148, No.8:L176–L178, 1996.

[75] S.M. Hu, S.P. Klepner, R.O. Schwenker, and D.K. Seto. Dislocation propagation and emitter edge defects in silicon wafers. *Journal of Applied Physics*, 47, No.9:4098, 1976.

[76] S.M. Hu. Stress related problems in silicon technology. *Journal of Applied Physics*, 47, No.9:4098, 1991.

[77] P.J. Halfpenny. Dislocation generation in silicon during CMOS device processing. *Journal of Materials Science: Materials in Electronics*, 3:107–112, 1992.

[78] P.M.Fahey et al. Stress-induced dislocations in silicon integrated circuits. *IBM Journal of Research and Development*, 36, No.2:158–182, 1992.

[79] M.A. Huff. *Silicon Micromachined Wafer-Bonded Valves.* PhD thesis, Massachusetts Institute of Technology, February 1993.

[80] M.A. Huff, A.D. Nikolich, and M.A. Schmidt. A threshold pressure switch utilizing plastic deformation. In *Transducers '91 - 6th Int. Conf. on Solid-State Sensors and Actuators*, pages 177–180. IEEE, 1991.

[81] M.A. Huff, A.D. Nikolich, and M.A. Schmidt. Design of sealed cavity microstructures formed by silicon wafer bonding. *IEEE Journal of Microelectromechanical Systems*, 2:74–81, 1993.

[82] R. Stengl, K-Y. Ahn, and U. Gösele. Bubble-free silicon wafer bonding in a non-cleanroom environment. *Japanese Journal of Applied Physics*, 27, No.12:L2364, 1988.

[83] S. Suresh. *Fatigue of materials.* Cambridge University Press, 1992.

[84] R. Hooke. Approximate analysis of the large deflection elastic behaviour of clamped, uniformly loaded, rectangular plates. *Journal Mechanical Engineering Science*, 11, No.3:256–268, 1969.

[85] Hibitt, Karlsson and Sorensen, Inc. *ABAQUS Version 4.8.*

[86] G. Gerlach, A. Schroth, and P. Pertsch. Influence of clamping conditions on microstructure compliance. *Sensors and Materials*, 8:79, 1996.

[87] X. Chauffleur, G. Blasquez, and P. Pons. Influence of bonding conditions on the response of capacitive pressure sensors. *Sensors and Actuators A*, A46-47:121–124, 1995.

[88] F. Secco d'Aragona. Dislocation etch for (100) planes in silicon. *Journal of the Electrochemical Society*, 119:948, 1972.

[89] P.M. Osterberg et al. *to be published in IEEE J. Microelectromechanical Systems*, June 1997.

[90] R.K. Gupta, C.H. Hsu, M.A. Schmidt, and S.D. Senturia. Monitoring plasma overetching of wafer-bonded microstructures. In *Transducers '95 - 8th Int. Conf. on Solid-State Sensors and Actuators*, pages 269–272, 1995.

[91] Wyko Corporation, Tucson, AZ. *TOPO-3D Surface Profilometer.*

[92] Y. Kanda. Piezoresistance effect of silicon. *Sensors and Actuators A*, A28:83–91, 1991.

[93] J. McCreary. Matching properties, and voltage and temperature dependence of MOS capacitors. *IEEE Journal of Solid State Circuits*, SC-16, No.6:608–616, 1985.

[94] D. Breslau. Personal communication.

[95] J.T. Kung. *Integrated capacitive sensors using charge-redistribution sense techniques.* PhD thesis, Massachusetts Institute of Technology, June 1992.

[96] Surface Technology Systems England. PECVD silicon nitride film.

[97] Ken Valeri. Laurell Technologies Corporation, 850 North Wales Road, Lansdale, PA.

[98] J.B. Martin. *Plasticity.* MIT Press, 1975. 3233-24