Threshold Voltage in Pentacene Field Effect Transistors with Parylene Dielectric

by

Annie I. Wang

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degrees of

Bachelor of Science in Electrical Engineering

and

Master of Engineering in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 2004

Author .....
Department of Electrical Engineering and Computer Science
May 20, 2004

Certified by.....
Akintunde Akinwande
Professor of Electrical Engineering
Thesis Supervisor

Certified by.
Ioannis Kymissis
Postdoctoral Associate
Thesis Supervisor

Accepted by.....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

Threshold Voltage in Pentacene Field Effect Transistors with Parylene Dielectric

by

Annie I. Wang

Submitted to the Department of Electrical Engineering and Computer Science
on May 20, 2004, in partial fulfillment of the
requirements for the degrees of
Bachelor of Science in Electrical Engineering
and
Master of Engineering in Electrical Engineering and Computer Science

Abstract

Organic field effect transistors (OFETs) offer a suitable building block for many flexible, large-area applications such as display backplanes, electronic textiles, and robotic skin. Besides the organic semiconductor itself, an important area in the development of OFETs is the gate dielectric material. In this thesis the organic polymer parylene is studied as a gate dielectric for pentacene OFETs. The three main areas of study were: (1) parylene's performance as a dielectric, (2) possible improvement of OFETs by surface treatments, and (3) the effects of interface traps on threshold voltage and parasitic bulk conductivity.

Parylene was found to provide a favorable, hydrophobic interface for pentacene growth, yielding transistors with mobilities $> 0.5 cm^2/Vs$ at -100V. While the two surface treatments explored did increase contact angle by 10-20°, neither the ammonium sulfide nor the polystyrene treatment significantly improved pentacene packing or mobility. Modification of the parylene surface using an oxygen plasma introduced traps at the semiconductor-dielectric interface, observable through a variety of characterization techniques. A model is developed to explain how the fixed and mobile charges these traps introduce influence the threshold voltage and parasitic conductivity in the device.

Thesis Supervisor: Akintunde Akinwande
Title: Professor of Electrical Engineering

Thesis Supervisor: Ioannis Kymissis
Title: Postdoctoral Associate

Acknowledgments

I am grateful to many people for their help in the preparation of this thesis. First, I would like thank my advisor, Prof. Tayo Akinwande, for discussions, encouragement, and for always pushing me to think about how? and why? in my research. Without his help, I'd soon be overwhelmed by details and completely miss the "big picture."

Also I would like to thank Prof. Vladimir Bulović and the members of the Laboratory of Organic Optics and Electronics (LOOE) for helpful discussions and insights. Much-appreciated advice and support came from the members of my research group: Liang-yu Chen, Jeremy Walker, and Dr. Yong-woo Choi. I owe thanks also to former group members Dr. Ching-yin Hong and Dr. Ioannis (John) Kymissis who brought me into the group as a UROP and got me started on real live research.

Most of all, I want to thank my advisor and mentor, Dr. John Kymissis. From the first day I joined the group as a UROP, John not only helped me set up my projects but was always available to share his considerable knowledge and insights. His unfailing encouragement and enthusiasm are worth more to me than I can express, and my thanks go to the best mentor one could possibly have.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation and applications

The proliferation of circuits applications requiring flexible, large area electronics is a driving factor in the development of new materials and processes. Suggested applications range from display backplanes and sensors to electronic textiles and robotic skin [1–5]. For practical large area electronics, there are several important considerations: (1) acceptable device performance and stability, (2) low cost, and (3) viable manufacturing processes. In particular, a low-temperature fabrication process is desirable in order to take advantage of cheap, lightweight, flexible polymer substrates such as polyimide. These substrates cannot withstand the high temperatures of traditional semiconductor processing.

While amorphous silicon has been well developed as a candidate material, organic semiconductors have the potential to overtake amorphous silicon for low cost, large area electronic circuits. The performance of organic semiconductors, typically benchmarked by mobility, has been significantly improved by considerable research into materials and processes over the past decade. A wide range of organic materials has been explored, from semiconducting polymers such as polythiophene and polyacetylene, to short conjugated oligmers such as tetracene and pentacene [1,2]. The flexible thin films can be consistently deposited onto room-temperature substrates over large areas, making organic semiconductor based-devices suitable building blocks for many

large area flexible applications.

Organic field effect transistors (OFETs) have already been demonstrated in applications such as electronic textiles, robotic skins, and radio frequency identifaction tags (RFIDs) [1, 2, 4–8]. Areas of OFET research in addition to organic semiconductors include the investigation of organic conductors, especially transparent materials that form ohmic contacts to organic semiconductors; the development of organic gate dielectrics, such as the polymer parylene studied in this thesis; and improved control over FET characteristics such as threshold voltage.

For organic FETs to become practical building blocks for circuits, the mass fabrication of transistors with consistent device characteristics must be realistically achievable. In particular, device parameters such as threshold voltage and mobility should be repeatable and controllable. The design of circuits using organic FETs would benefit from having a comprehensive model for the device, such as those developed for crystalline silicon. To address these issues, we need a better understanding of the physical mechanisms in the device, particularly at the interface between the semiconductor and gate dielectric. How does the semiconductor-insulator interface influence mobility and threshold voltage? The goal of this thesis work is to improve our understanding of the physical mechanisms occurring at the semiconductor-insulator interface. A full understanding of the operation of organic FETs is ultimately the key to their development as a building block in larger systems.

Chapter 2

Background

2.1 Organic FETs - device operation

The majority of organic semiconductors are p-type, since positively charged hole carriers dominate conduction in the semiconductor. One example is the conjugated oligmer pentacene, which consists of five fused benzene rings. The carbon atoms in the fused ring backbone are sp^2 hybridized. Each carbon is bonded to neighboring carbon and hydrogen atoms by a double bond and two single bonds. The carbon and hydrogen atoms share σ bonds (hybridized orbitals), while the carbon-carbon double bonds consist of a σ bond and a π bond (unhybridized p orbital). While the σ bonds are all in-plane, the π orbitals are out of plane. Because of conjugation in the molecule (i.e. alternating single and double bonds), the π orbitals overlap, forming a "racetrack" of delocalized electrons. This delocalization means that π electrons are less tightly bound to the molecule. Since the more electronegative carbon atoms pull electrons away from the hydrogen atoms, the carbon backbone is electron-rich and energetically more likely to lose electrons. The absence of an electron leaves a positively charged "hole" which can move around the molecule and, with additional complications, between molecules. These mobile charge carriers form the basis for conduction in the semiconductor.

2.1.1 The MIS capacitor

The simplest device structure to implement is a field-effect transistor, which is built on the metal-insulator-semiconductor (MIS) capacitor structure (Fig. 2-1). Conductivity in the semiconductor layer in MIS capacitor is modulated by the voltage applied to the gate metal with respect to the semiconductor bulk (V_{GB}).

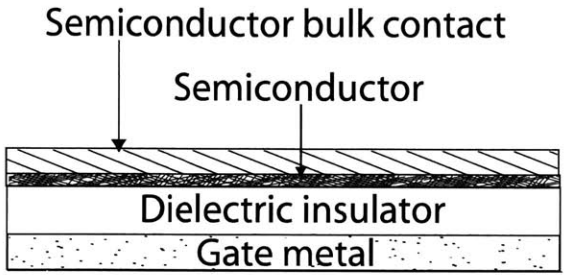


Figure 2-1: Schematic cross-section of MIS capacitor structure.

In a crystalline semiconductor, at equilibrium ($V_{GB} = 0V$) the insulator-semiconductor interface is depleted of hole carriers. As V_{GB} is decreased and becomes more negative, more holes are attracted to the surface. When the concentration of holes attracted to the surface becomes such that there is no charge induced in the semiconductor, the flatband condition is reached. The V_{GB} at which this condition occurs is called the flatband voltage V_{FB}.

Further decrease in V_{GB} beyond V_{FB} leads to the accumulation of holes at the interface and results in the formation of a 2D hole gas. The MIS structure can be modeled as a capacitor with the insulator as gate dielectric. Using the charge control model, the hole charge density is given by

$$Q_{ACC} = -C_{ins}\,(V_{GB} - V_{FB}) \tag{2.1}$$

Eqn. 2.1 forms the basis of our formulation of the OFET. An OFET is treated as a voltage-controlled resistor whose carrier density (i.e. conductivity) is controlled by the gate to bulk voltage V_{GB}.

As V_{GB} increases and becomes more positive, the positive gate voltage drives

holes away from the insulator-semiconductor interface and the semiconductor becomes more depleted. A wider depletion region results in a larger voltage drop across the semiconductor. At this point, the MIS structure is modeled as the series combination of the insulator capacitance and a depleted semiconductor layer capacitance. The semiconductor capacitance depends on the applied voltage V_{GB}.

Although electrons are generated for $V_{GB} > 0$, they remain local to the region in which they are generated because electrons have a short diffusion length in the semiconductor. Hence, in contrast to conventional semiconductors such as silicon, no inversion layer is formed and the width of the depletion layer will increase until the semiconductor thin film is fully depleted. At this point, the MIS structure is modeled as the series combination of the insulator capacitance and a depleted semiconductor layer capacitance. Since the semiconductor is fully depleted, the semiconductor capacitance is independent of the applied voltage V_{GB}.

2.1.2 An FET in the linear region

As described in the previous section, a 2D hole gas at the insulator-semiconductor interface is formed in the accumulation region. Thus, the accumulation region can be used as the basis for an organic FET. In contrast, conventional FETs rely on modulation of a 2D electron or hole gas in the inversion regime. It has been shown that organic FETs can be modeled by conventional semiconductor device equations, as derived below [9, 10].

In accumulation, the total channel hole charge Q_s is given by

$$Q = C * V = C_{ins} * [-V_G + \psi_s] \tag{2.2}$$

where C_{ins} is the insulator capacitance, V_G is the gate voltage, ψ_s is the surface potential. Defining the x-direction to be from the gate to bulk/substrate and the y-direction to be from the source to the drain, ψ_s is a function of y. Under the gradual channel approximation, the transverse field E_x is assumed to be much larger than the longitudinal field E_y. The surface potential $\psi_s(y)$ is then

$$\psi_s(y) = V(y) + V_T \tag{2.3}$$

where $V(y)$ is the bias between the point y and the grounded source and V_T is the threshold voltage. In a conventional semiconductor, V_T is the voltage required to reach inversion. Since OFETs operate in accumulation, the on voltage (V_{on}) corresponds to the flatband voltage (V_{FB}) plus the contribution of non-idealities such as interface traps that shift V_{on} positive or negative. For consistency with conventional notation, V_{on} is called the threshold voltage, V_T.

Conductivity of the semiconductor layer at a point y can be written as

$$\sigma(x) = qp(x)\mu(x) \tag{2.4}$$

where $\sigma(x)$ is the channel conductivity, q is the electron charge $1.6\text{x}10^{-19}$C, $\mu(x)$ is the hole mobility and $p(x)$ is the hole concentration. Assuming a constant mobility, the channel conductance g is then

$$g = \frac{W}{L}\int_0^{x_a} \sigma(x)dx = \frac{W}{L}\mu\left|Q_s\right| \tag{2.5}$$

where W and L are the channel width and length and x_a is the accumulation layer thickness. Since the channel resistance of a section dy is $dR = \frac{dy}{g*L} = \frac{dy}{W*\mu*|Q_s(y)|}$, the drain current I_D can be solved for as

$$-I_D = V/R = \frac{\int_0^{V_{DS}} dV}{\int_0^L dR} = \frac{\int_0^{V_{DS}} dV}{\int_0^L \frac{dy}{W*\mu*|Q_s(y)|}} \tag{2.6}$$

which becomes

$$-I_D = \frac{W}{L}\mu C_{ins}\left(V_{GS} - V_T - V_{DS}/2\right)V_{DS} \tag{2.7}$$

where V_{DS} is the drain voltage. In the linear region where V_{DS} is very small, the $V_{DS}/2$ term can be neglected and the equation becomes

$$-I_{D_{linear}} = \frac{W}{L}\mu C_{ins}\left(V_{GS} - V_T\right)V_{DS} \tag{2.8}$$

This is the same as the conventional equation for drain current in a transistor in the linear region. After taking partial derivatives with respect to V_{GS}, the field effect mobility can be solved for as

$$\mu_{linear} = \frac{L}{WC_{ins}VDS}\frac{d(-I_D)}{dV_G} \tag{2.9}$$

2.1.3 An FET in the saturation region

The saturation region is reached when $V_{DS} = V_{DS_{SAT}} = V_{GS}$ - V_T and the channel charge at the drain $Q_s(y = L)$ vanishes. At this point, the channel pinches off and drain current remains constant, to first order. Substituting $V_{DS_{SAT}}$ into Eqn. 2.8,

$$-I_{D_{SAT}} = \frac{W}{2L}\mu C_{ins}\left(V_{GS} - V_T\right)^2 \tag{2.10}$$

This is the same as the conventional equation for drain current in a transistor in the saturation region. Similarly to Eqn. 2.11, field effect mobility in the saturation can be solved for as

$$\mu_{sat} = \frac{L}{2WC_{ins}}\left(\frac{d\sqrt{(-I_D)}}{dV_G}\right)^2 \tag{2.11}$$

Because OFETs do not operate in inversion, there is no depletion region to isolate the channel from the bulk. Horowitz, et al. suggest that the optimal device structure is a thin-film structure, since a thinner semiconductor layer ($h < 100$nm) reduces parasitic bulk conductivity in the device [9]. Organic FETs are typically fabricated as polycrystalline organic thin film transistors (TFTs), although OFETs have been successfully fabricated on single crystal organic semiconductors. The scalability of these OFETs is limited by the small size of the organic single crystals, which were only a few millimeters in size [11–13]. In contrast, polycrystalline TFTs can cover large area flexible substrates.

2.2 Pentacene - an organic semiconductor

The organic semiconductor chosen for this thesis work was pentacene. Presently one of the best performing organic semiconductors, pentacene is a fused-ring aromatic hydrocarbon ($C_{22}H_{14}$), shown in Fig. 2-2. Reported mobilities are comparable to that of amorphous silicon ($\sim 1\ cm^2V^{-1}s^{-1}$) [14–17].

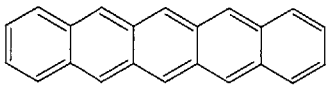


Figure 2-2: Structure of a pentacene molecule, $C_{22}H_{14}$.

Pentacene thin films are deposited by thermal evaporation in vacuum. The pentacene is heated in a crucible until it sublimes and lands on the substrate surface. The resultant thin film grows in Stransky-Krastanov growth mode, in which the initial layer-by-layer growth is followed by smaller islands forming on top [18].

It has been shown that the field effect mobility in FETs is improved by structural perfection in the pentacene layer; increased intermolecular packing and highly ordered structures produce better performance [15, 16, 19]. For closer packing, pentacene should be repulsed from the surface. This repulsion will cause the pentacene backbone to stand up on the substrate and pack into a crystalline structure [20]. Although subsequent layers become less ordered and form smaller grains, only the first few layers of pentacene are important in the operation of the transistor. These layers determine the field effect mobility, which may be much smaller than the mobility measured in single crystal pentacene. In fact, mobility is known to be sensitive to pentacene grain size, which is at least partly determined by the surface chemistry of the dielectric [18, 20, 21]. Thus, the properties of the interface between the gate dielectric and pentacene active layer are very important. The effects of changing this interface will be explored in this thesis.

2.3 Parylene - an organic gate dielectric

The gate dielectric chosen for study was an organic polymer, parylene (poly-p-xylylene). Although several varieties of parylene exist, including parylene-N, parylene-C and parylene-D, Yasuda et al. reported that the use of parylene C as a gate dielectric resulted in the best FET performance [22].

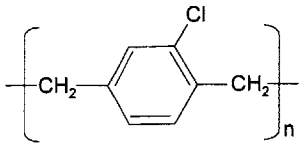


Figure 2-3: Structure of parylene-C.

Parylene-C is a conformal, vapor-deposited film with a dielectric constant of approximately 3.0. The chemical structure is shown in Fig. 2-3. The room-temperature vapor deposition of parylene results in a pinhole-free, relatively smooth and uniform film [23]. It has excellent electrical and mechanical properties for use as a gate dielectric. In fact, it has already been demonstrated in organic TFTs using the thiophene oligomer DH6T [24] as well as in transistors on single crystal rubrene [11] and pentacene [12].

Parylene is deposited by chemical vapor deposition (CVD) at pressures of ~0.1-1 Torr. The source material is supplied in dimer form. The solid dimer is first vaporized at 180°C and then cracked into monomer units at 690°C. The stable monomer then enters the deposition chamber to simultaneously adsorb and polymerize onto the room-temperature substrate. Film thickness is determined by the amount of dimer source material used.

The conformal, fully cross-linked polymer films can be easily etched by wet chemical processing or dry plasma etching. Because parylene is an organic polymer, its interfacial properties can be modified by the same chemistries used on other organics. This process compatibility makes parylene a good candidate material for organic FETs on flexible substrates. Parylene as a gate dielectric provides a suitable platform

for study in this thesis.

2.4 Direction/Focus of work

To gain a better understanding of how semiconductor-insulator interfacial characteristics affect OFET operation, we chose to study the pentacene field effect transistor with parylene as the gate dielectric. The surface properties of parylene affect pentacene film growth and influence device parameters such as mobility and threshold voltage. A vital question is: which properties are most significant to OFET operation, and how does the modification of those properties change the device behavior? In this thesis, three main areas are explored to address this issue:

- Parylene as a gate dielectric
- Surface treatment of parylene to improve performance
- Threshold voltage and traps

In Chapter 3, the suitability of parylene as a gate dielectric is studied. In addition to process compatibility, a gate dielectric should exhibit a high breakdown voltage, low leakage current, and an appropriate surface for semiconductor growth. As the film thickness is decreased, the capacitance and applied electric field increases. The field effect mobility should be enhanced as the effective field increases. These properties are confirmed for parylene.

In Chapter 4, possible improvement of FET performance by surface treatment of the parylene gate dielectric is explored. The two surface treatments investigated are an ammonium sulfide solution dip and a spin-coating of polystyrene. Senkevich, et. al. reported that treatment of parylene with ammonium sulfide successfully functionalized the surface, thereby increasing the hydrophobicity [25]. Polystyrene is itself a hydrophobic material. Both treatments are expected to increase the hydrophobicity of the parylene, thereby improving the pentacene crystalline layer growth. Better packing in the pentacene layer should translated into higher FET performance.

Finally, in Chapter 5, the effect of an oxygen plasma treatment of parylene prior to pentacene growth is studied. The process introduces traps at the parylene-pentacene interface, significantly changing the device performance. Traps induce both fixed and mobile charges that affect threshold voltage and bulk conductivity. This chapter discusses physical and electrical characterization results in order to gain a better understanding of the contribution of interface traps to transistor behavior.

Chapter 3

Parylene as a gate dielectric

Desirable qualities for a gate dielectric include a high breakdown voltage, low gate current leakage, and process compatibility. Thermally grown SiO_2 has been the dielectric of choice with a high breakdown voltage, low gate leakage, and a high quality interface. However, thermal oxide is not suitable for flexible polymer substrates, since the high temperature processing (800°-1200°C) required would destroy the polymer. The DuPont Kapton E polyimide films used as substrates, for instance, severely degrade above 400°C [26]. Parylene offers better process compatibility since the substrate remains at room temperature during chemical vapor deposition (CVD).

The goal of this chapter is to show that parylene performs well as a dielectric. Its performance can be compared against that of SiO_2 as a reference. From manufacturer specifications [23], the dielectric constant of parylene is expected to be $k = 3.10$. In comparison, the dielectric constant of SiO_2 is $k = 3.9$. The dielectric constant determines the capacitance; a higher dielectric constant results in a higher capacitance and higher electric field at the surface of the dielectric. A stronger field attracts more carriers to the surface. This effect directly affects mobility, which is a measure of how easily carriers drift in a material. As carrier concentration increases, localized trap states in the semiconductor are gradually filled, freeing additional carriers to move more easily through the semiconductor. Hence, mobility should increase with electric field until it saturates when all traps are filled [27].

In addition, the use of parylene as an encapsulation layer is tested. The diffusion

of gases over time into the pentacene semiconductor destroys transistor performance. Parylene encapsulation provides a barrier passivation layer to help protect the semiconductor and allows the design of multi-layered circuits. The addition of a parylene passivation layer is not expected to affect the FET device performance.

3.1 Fabrication Process

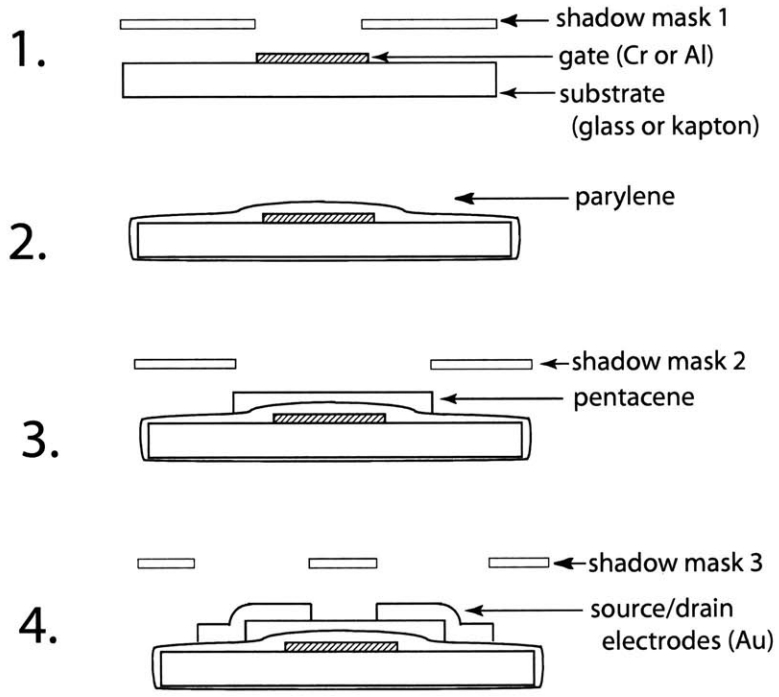


Figure 3-1: Fabrication process for top-contact organic thin film transistors.

Our hypotheses were tested by fabricating transistors and metal-insulator-metal (MIM) capacitors and conducting electrical measurements to determine capacitance, mobility, and I-V characteristics. The standard baseline process for fabricating pentacene FETs for this thesis is described below. This process follows the technique used by Kymissis, et al. [18]. In this work, the standard substrate was glass, although FETs were also successfully fabricated on flexible substrates such as polyimide (Kapton). Processing was done in the Exploratory Materials Laboratory (EML) and in

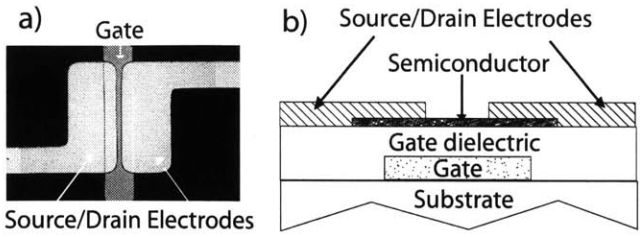


Figure 3-2: (a) Micrograph of top-contact pentacene FET. The device dimensions are 50μm x 1250μm. (b) Schematic cross-section of FET.

the Akinwande group lab at MTL.

The processing steps are shown in Fig. 3-1 and are described in detail below.

1. Metal gates are patterned through a shadow mask by electron beam deposition. The metal used is typically aluminum, although chrome may be used for better adhesion on substrates such as Kapton.

2. Parylene is deposited by CVD using a Speedline Technologies Parylene Deposition System. The substrate remains at room temperature in the deposition chamber, which is pumped down to 0.1 Torr.

3. Pentacene is thermally evaporated through a shadow mask onto the parylene gate dielectric. Typical background pressures were $10^{-6}-10^{-7}$ Torr in the homemade thermal evaporator. The pentacene was heated to 195°C−220°C; lower evaporation temperatures correspond to slower deposition rates.

4. Gold source/drain contacts are patterned through a shadow mask by electron beam deposition.

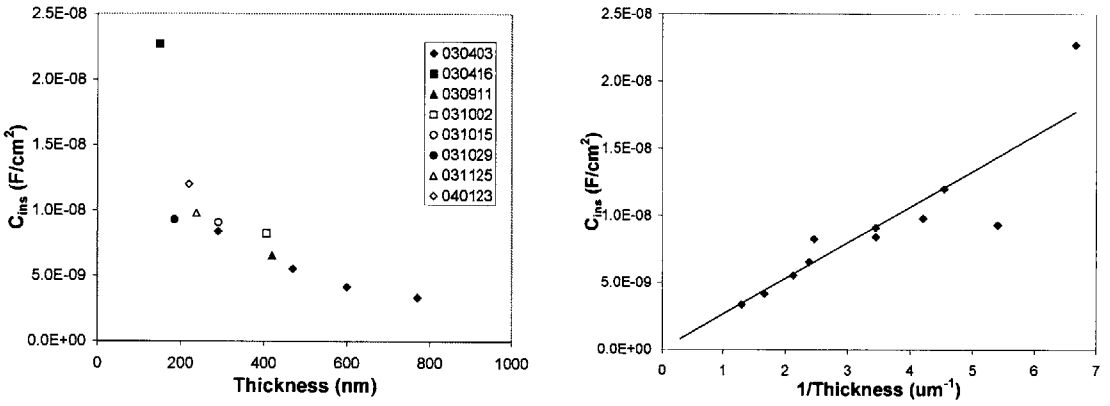
MIM and MIS capacitors are fabricated in parallel using different masks. A typical FET is shown in Fig. 3-2a and a schematic cross-section of the device in Fig. 3-2b.

3.2 Film thickness and capacitance

Initiallly, a set of transistors was fabricated with different parylene thicknesses (030403 data set). Over the course of this work, each new transistor set was also measured

and added to the plot in Fig. 3-3a. Although the pentacene deposition conditions varied across these samples, the deposited parylene films appear fairly uniform.

Film thickness was measured using a Dektak Surface Profiler and, for later samples, also by the crystal oscillator thickness monitor installed on the parylene machine. Capacitance was measured on an HP 4192A LF Impedance Analyzer at 10kHz.



(a) (b)

Figure 3-3: Capacitance vs. parylene film thickness. Capacitance was measured at 10kHz.

Fig. 3-3a plots the capacitance values of parylene samples vs. parylene film thickness. Capacitance per unit area is defined as

$$C_{ins} = \epsilon_{ins}/t_{ins} \tag{3.1}$$

where ϵ_{ins}=k_{ins} x ϵ_0 and t_{ins} = dielectric thickness. To find $k_{parylene}$, the same data was re-plotted in Fig. 3-3b with $1/t_{ins}$ on the x-axis to show a linear relationship. From the fitted line, the slope m = 2.661x10^{-13} yields

$$k_{parylene} = (\text{m} = 2.661\text{x}10^{-13}/(\epsilon_0 = 8.85\text{x}10^{-14}\ \text{F/cm}) = 3.0$$

with standard deviation = 0.5. This experimental value agrees with manufacturer-supplied specifications: k = 3.1 at 1kHz, k = 2.95 at 1MHz [23].

3.3 Field effect mobility

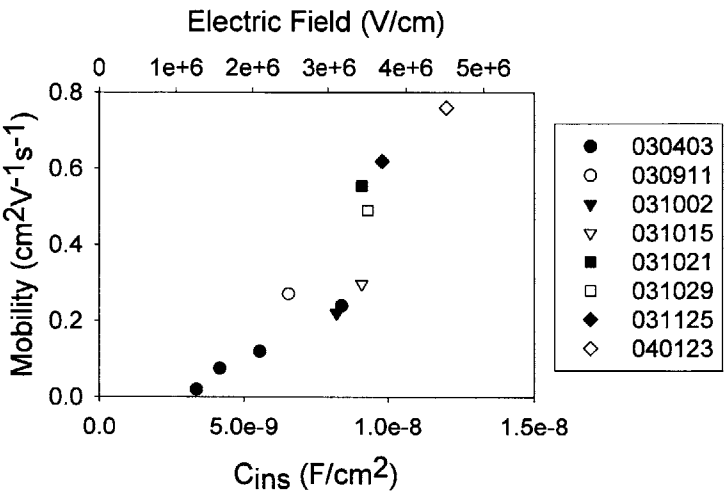


Figure 3-4: Mobility vs. capacitance, where capacitance is proportional to electric field. The saturation mobility was extracted at $V_{DS} = -100$V for all samples except for 040123, which was extracted at $V_{DS} = -70$V.

While mobility can be obtained in several different ways, the field-effect mobility was extracted from the transistor characteristics as suggested in [28], using the equations developed in Chapter 2. Although the pentacene deposition conditions (e.g. evaporation temperature, pre-purification) varied across these samples, the data in Fig. 3-4 shows the general trend.

Dimitrakopoulos, et al. showed that field effect mobility in pentacene is dependent on the concentration of channel carriers rather than gate field. At low carrier concentrations, most of the holes are trapped in localized states. These trap states are filled as carrier concentration increases, until all traps are full. Additional carriers can then move through the semiconductor with a mobility not reduced by trap-scattering. While the electric field depends only on the dielectric thickness, carrier concentration is determined by both the thickness and the dielectric constant [29,30]. In this case, the dielectric material was kept constant, so both carrier concentration and electric field varied as a function of thickness only.

Fig. 3-4 plots field effect mobilities against the dielectric capacitance. All mobilities were measured at $V_{DS} = -100V$, with the exception of the 040123 sample which was measured at V_{DS} =-70V. Since capacitance (C = ϵ/thickness) and electric field (E = voltage/distance) follow the same 1/(distance = thickness) relationship, this plot can be translated into mobility vs. applied electric field. Thus, mobility increases with decreasing dielectric thickness and increasing electric field in parylene. The thinner dielectrics result in a higher carrier concentration at the surface, so that more traps are filled and mobility is higher.

Among the plotted devices, the highest mobility, $\mu = 0.75 cm^2/Vs$, was obtained at $V_{DS} = -70V$ from the 040123 device. This parylene dielectric layer was 220nm thick. In comparison, Gundlach et al. reported a mobility of 2.1 cm^2/Vs on a 250nm thick octadecyltrichlorosilane-treated SiO_2 gate dielectric ($V_{DS} = -80V$) [17].

3.4 Gate leakage

Although breakdown voltage was not tested specifically, gate leakage can be considered a measure of the breakdown voltage of a dielectric. Gate leakage in the tested transistors was typically in the nA range. This is not as low as the pA leakage obtainable from thermally grown SiO_2 but is at several orders of magnitude lower than the drain current, which was generally in the tens to hundreds of μA range. This low gate leakage supports a high breakdown voltage for parylene. A high breakdown voltage means that the dielectric thickness can be decreased without decreasing the operating voltage. With a thinner dielectric, a higher electric field and higher device performance can be attained. Because a higher gate capacitance requires more current to charge/discharge, we might expect the switching time in logic circuits using OFETs to increase. However, Kymissis showed that the accompanying mobility improvement more than compensates for the delay since current in the semiconductor is increased. Switching time actually decreases, resulting in faster circuits [18].

3.5 Parylene as an encapsulant

To demonstrate that parylene can be used as an encapsulant without changing the FET behavior, a set of devices was fabricated, tested, encapsulated, and tested again. Figs. 3-5a and 3-5b show the I-V characteristics of a typical device before and after parylene encapsulation, respectively. The shape and magnitude of the I-V curves appear identical. Also, the extracted mobility and threshold voltage of this device are essentially the same (Table 3.1). From this data, it is clear that encapsulation does not affect the device performance.

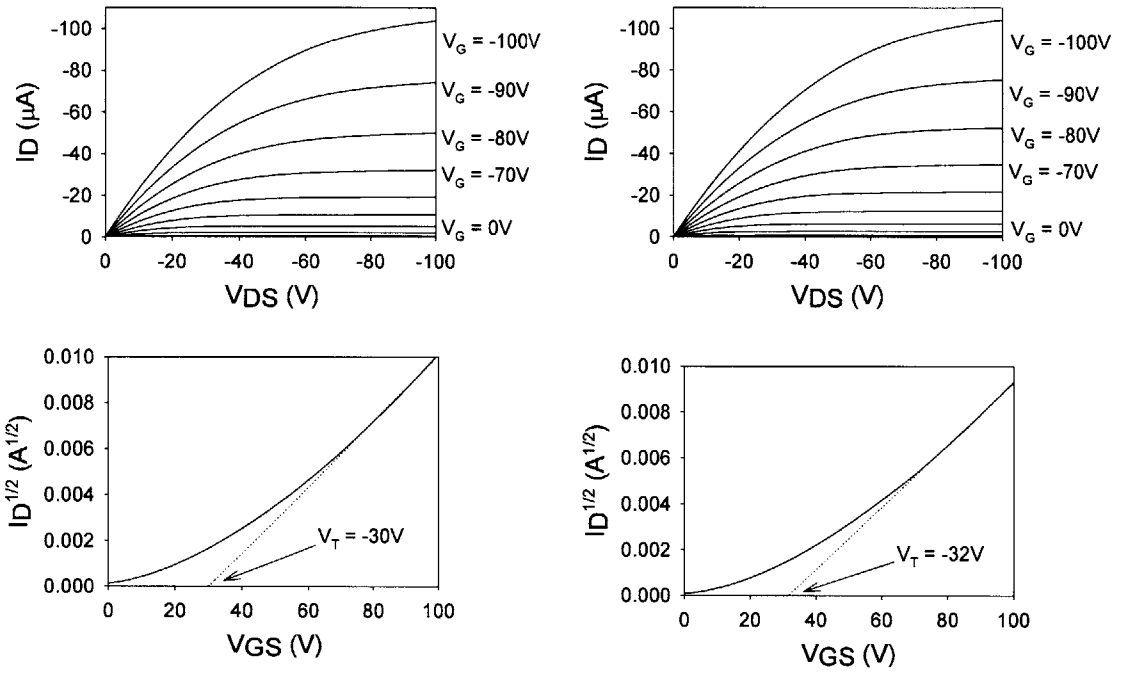


Figure 3-5: I-V characteristic for (a) an unencapsulated pentacene FET and (b) the same device following parylene encapsulation.

Although the effectiveness of parylene as a barrier to environmental contaminants such as water was not tested, it was verified that parylene encapsulation at least does not harm the device performance.

Transistor	Mobility (cm^2)	V_T (V)
Unencapsulated	0.25	-30V
Encapsulated	0.22	-32 V

Table 3.1: Comparison of device parameters for a typical transistor before and after parylene encapsulation.

3.6 Summary

The dielectric constant of parylene was verified to be k = 3.0±0.5. The field effect mobility in FETs using a parylene as a gate dielectric was shown to increase as a function of decreasing film thickness, although mobility saturation was not seen. Low gate leakage currents, typically in the nA range, were observed in FETs biased as high as 100V.

We demonstrated that parylene can be used as an encapsulation layer without affecting FET performance. Further studies can be conducted to quantitatively test the stability and reliability of parylene as a gate dielectric and encapsulant over time.

Chapter 4

Surface treatment of parylene gate dielectric to improve pentacene film growth

The goal of this study was to modify the parylene surface in order to improve pentacene growth. A more hydrophobic surface is expected to result in better packing of the pentacene molecules, as shown in Fig. 4-1. Yasuda, et al. reported "an obvious tendency for the hydrophobic dielectric layers to give a higher field-effect mobility for both crystalline organic semiconductors and amorphous polymer semiconductor" [22]. The first few layers in particular are most important in transistor operation, since in the accumulation region carriers are concentrated at the interface [31]. Larger grain sizes and hence, fewer grain boundaries, have been linked to improved mobility and higher performance [15, 20].

Two surface treatments were explored based on work in the literature: an ammonium sulfide treatment and a polystyrene treatment. Senkevich, et. al. reported that treatment of parylene with ammonium sulfide successfully functionalized the surface, thereby lowering the contact angle and increasing the hydrophobicity [25]. A 3M group reported improved FET performance after a styrene-based polymeric treatment on the gate dielectric [8]. We expected to show that these surface treatments increased the hydrophobicity of parylene and consequently improved pentacene

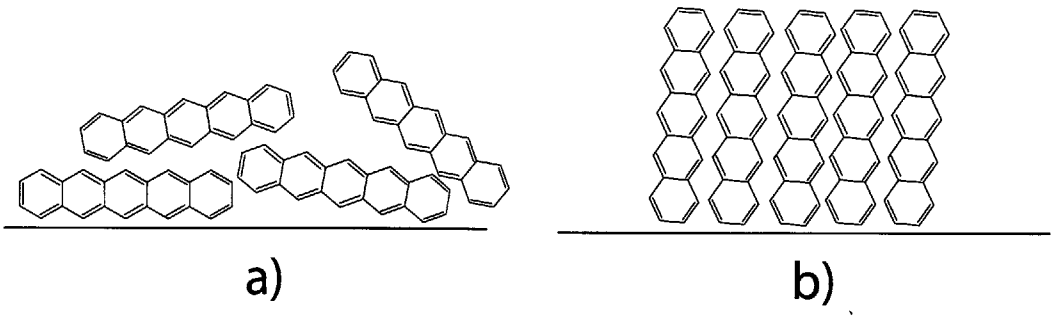


Figure 4-1: Schematic diagram of a pentacene film grown on (a) non-hydrophobic surface and (b) a hydrophobic surface. In the second, more desirable case, pentacene molecules are repelled from the surface and stand up, packing into a crystalline structure. (Adapted from [20].)

packing and FET performance.

4.1 Experiment

Three sets of devices were fabricated for each experiment: (a) untreated control devices, (b) devices treated with ammonium sulfide ($(NH_4)_2S$), and (c) devices treated with polystyrene. Except for treatment of the parylene dielectric prior to pentacene deposition, the fabrication process was exactly the same as described in the previous chapter.

The first set of devices (A) was fabricated using the standard baseline process with no surface treatment of the parylene prior to pentacene deposition. The second set of devices (B) was dipped in a 50% solution of ammonium sulfide for 5 minutes and then rinsed with DI water and blown dry. The last set of devices (C) was spin-coated with a 3.25% solution of polystyrene in anisol at 2000rpm for 40s and dried on a 60°C hotplate.

In the first experiment (030911 sample set), a 420nm parylene gate dielectric layer was deposited by CVD. A 10nm thick pentacene layer was thermally evaporated at a rate of 0.1Å/s. For the second, repeat experiment (031021 sample set), the parylene layer was reduced to 290nm but the other fabrications conditions remained the same.

Physical characterization of the parylene surfaces and pentacene morphology was performed using several techniques. Electrical data was obtained from characterization of the FET devices. The results of these two experiments (030911 and 031021 data sets) are analyzed in the following sections.

4.2 Surface characterization of treated parylene

The gate dielectric surfaces were characterized using contact angle goniometry, atomic force microscopy (AFM), and cross-polarization optical microscopy. Contact AFM measurements were performed on a Park Scientific Autoprobe CP. A Nikon Eclipse L200 optical microscope and polarization filters were used for cross-polarization measurements.

Parylene sample	Contact angle (°)	Avg roughness (nm)	
		030911 data	031021 data
untreated	75°	2.98±0.10	2.97±0.24
ammonium sulfide treated	85°	3.41±0.33	3.94±0.97
polystyrene treated	95°	3.22±0.29	2.152±0.10

Table 4.1: Surface characteristics of treated and untreated parylene.

From contact angle measurements, both the ammonium sulfide solution dip and spin-coated polystyrene resulted in a more hydrophobic parylene surface. Table 4.1 shows the increase in contact angle from 75° in the untreated parylene to 85° and 95° in the ammonium sulfide and polystyrene treated samples, respectively. While both treatments improved the hydrophobicity of the parylene surface, however, the surface roughness was increased after ammonium sulfide treatment. In the 031021B sample, AFM measurement showed spikes/irregularities on the treated parylene, possibly due to etching by the ammonium sulfide. It has been observed that increased surface roughness reduces pentacene grain size [14]. This roughness can explain the smaller pentacene grain sizes on the ammonium sulfide-treated surface.

Pentacene grain sizes were measured using both AFM and cross-polarization. The grain boundaries are clearly visible in the AFM image in Fig. 4-2. Since AFM

measures the topography of a surface, the grain sizes measured by AFM are smaller than the grains at the parylene interface. On the other hand, cross-polarization allows the measurement of grain size at the interface, which is the most important in device operation. Figs. 4-3a, 4-3b, and 4-3c show typical cross-polarization images of the pentacene layer in each sample.

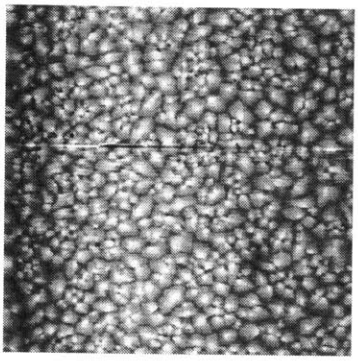


Figure 4-2: AFM image showing grain boundaries in pentacene layer in 031021C sample. This image covers a 5μm x 5μm scan area.

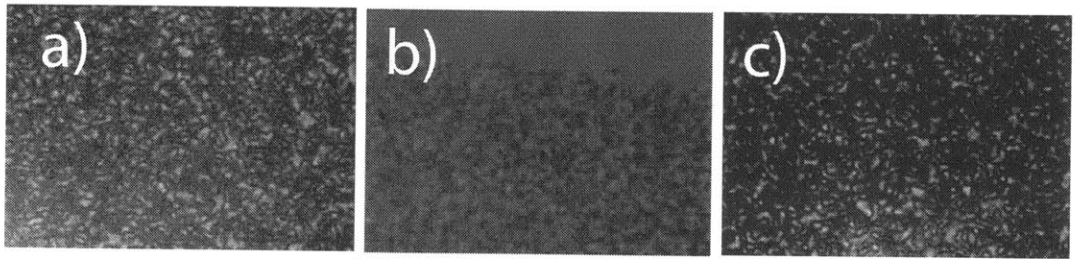


Figure 4-3: Cross-polarized images of pentacene on (a) untreated parylene (b) ammonium sulfide-treated parylene, and (c) polystyrene-treated parylene. Each image covers a 36.6μm x 25.6μm area. Image contrast was enhanced in Adobe Photoshop.

Pentacene grain sizes were determined from the AFM and cross-polarization images. Using the image processing software for the Autoprobe CP and the image processing toolbox in Matlab, grain size was calculated by dividing the number of grains passing through a line drawn on the image by the length of that line. Although this method does not give exact grain size, the relative sizes can be compared for the pentacene grains on untreated and treated surfaces.

Estimated grain sizes for each sample are summarized in Table 4.2. As expected from Stransky-Krastanov growth, the surface grains measured by AFM are smaller than the grains at the interface measured using cross-polarization. In both data sets, the ammonium sulfide treatment results in smaller pentacene grains while the untreated and polystyrene treated parylene samples show comparable pentacene grain sizes.

Parylene sample	Grain size [x-polar] (μm)	Grain size [AFM] (μm)
030911 samples		
untreated	–	0.187
ammonium sulfide treated	–	0.145
polystyrene treated	–	0.159
031021 samples		
untreated	0.847	0.267
ammonium sulfide treated	0.565	0.205
polystyrene treated	1.02	0.258

Table 4.2: Pentacene grain sizes on treated and untreated parylene for 030911 and 031021 data sets. Surface grains (measured by AFM) are smaller than the grains at the interface (measured using cross-polarization) but follow the same general trend.

As noted earlier, mobility has been shown to be linked to pentacene morphology. Electrical characterization of the fabricated FETs was performed expecting mobility to show the same trend determined from pentacene grain size measurements.

4.3 Electrical characterization of FETs

Since the field effect mobility is related to the applied electric field, which is inversely proportional to the dielectric thickness, the capacitance of each parylene sample was checked to make sure that the thicknesses were not drastically changed. Table 4.3 shows the capacitances of each parylene sample. The thinner dielectric in the 031021 samples appears as a higher overall capacitance than in the 030911 samples. Because the ammonium sulfide treatment etched the parylene slightly, decreasing dielectric thickness, the capacitance of the (B) samples is slightly higher. On the other hand, the spin-coating of polystyrene resulted in a thicker dielectric layer, noticeable as a

decrease in capacitance. The variation in thickness affects the electric field at the surface.

Parylene sample	Capacitance (F/cm^2)
030911 samples	
untreated	$6.6x10^{-9}$
ammonium sulfide treated	$7.0x10^{-9}$
polystyrene treated	$4.3x10^{-9}$
031021 samples	
untreated	$9.1x10^{-9}$
ammonium sulfide treated	$9.4x10^{-9}$
polystyrene treated	$5.6x10^{-9}$

Table 4.3: Comparison of parylene capacitances after surface treatment.

I-V characteristics were obtained for each device using an Agilent 4156C Precision Semiconductor Parameter Analyzer. Although transistor performance alone is only a rough indicator of the effect of surface treatment, the electrical characterization helps confirm the trend seen from physical characterization. Figs. 4-4, 4-5, and 4-6 show I-V characteristics for typical devices, treated and untreated.

Mobility was calculated for each type of sample in the saturation region as in Eqn. 2.11. Two values for each device were obtained; the first value was calculated with $V_{DS} = V_{GS}$ = -100V. Assuming that the dielectric constant was the same in all devices, the parylene thickness was determined from the capacitance and used to find electric field as a function of applied gate voltage. The second mobility value was then calculated for a constant electric field.

The I_{on}/I_{off} current ratio was calculated at $V_{DS} = -100V$ and V_T was determined from the I_D vs. V_{GS} curve. The values are summarized in Table 4.4.

Mobility is significantly poorer in the ammonium sulfide treated device. As noted earlier, the treated parylene surface was considerably rougher. Surface roughness contributes to mobility degradation since it increases carrier scattering at the semiconductor-insulator interface [32]. In addition, the smaller grain sizes mean that carriers must cross more grain boundaries, which causes mobility to drop.

While threshold voltage in the polystyrene treated FET is higher than in the other

Parylene sample	Mobility ($cm^2V^{-1}s^{-1}$)		I_{on}/I_{off}	V_T (V) (μm)
030911 devices				
	(a)	(b)		
untreated	0.27	0.18	$\sim 10^3$	-31
ammonium sulfide treated	0.20	0.12	$\sim 10^3$	-31
polystyrene treated	0.25	0.25	$\sim 10^5$	-48
031021 devices				
	(a)	(b)		
untreated	0.56	0.31	$\sim 10^3$	-35
ammonium sulfide treated	0.06	0.03	$\sim 10^4$	-37
polystyrene treated	0.37	0.37	$\sim 10^5$	-46

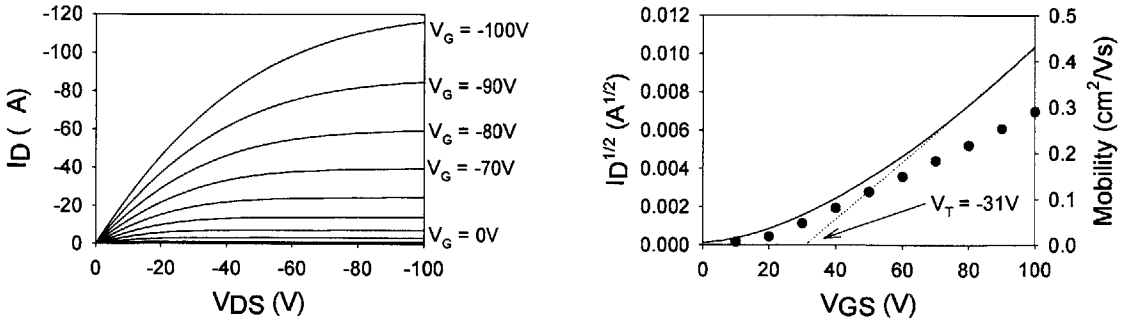
Table 4.4: Electrical characteristics of treated and untreated parylene. Mobility values were calculated (a) at $V_{DS} = V_{GS} = -100V$ and also (b) for normalized electric field E. ($E = 1.6x10^6 V/cm$ in 030911 devices and $E = 2.1x10^6 V/cm$ in 031021 devices.)

two FETs, this can be explained by the increased dielectric thickness. To reach the same electric field in the channel, a higher voltage must be applied. For an accurate comparison of the mobilities in each device, the gate voltage should be scaled with dielectric thickness in order to achieve the same electric field. Figs. 4-4b, 4-5b, and 4-6b show the mobility as a function of gate voltage. Table 4.4 also gives a comparison of the mobility in each device under the same electric field.

The thicker dielectric layer can also explain why the polystyrene treated FET shows the highest I_{on}/I_{off} ratio, since gate leakage current through the dielectric is reduced.

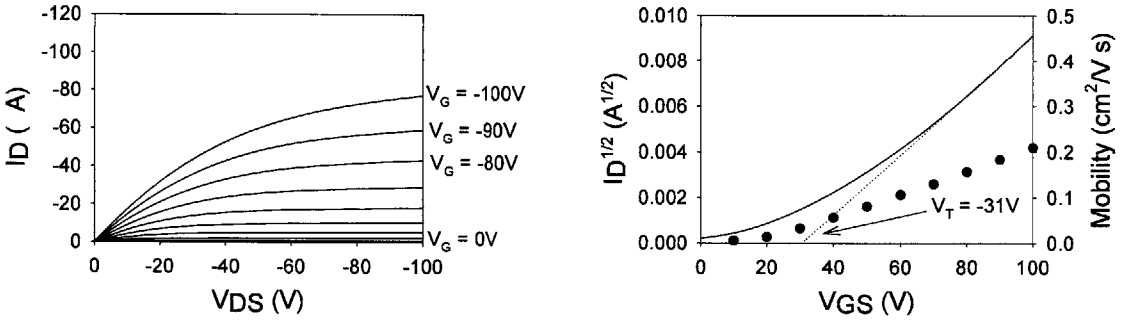
4.4 Summary

Although both ammonium sulfide treatment and polystyrene treatment increased the hydrophobicity of the parylene surface, parylene itself is already fairly hydrophobic. With the small change in contact angle, we did not see any significant improvements after applying either surface treatment. In fact, the ammonium sulfide treatment worsened the semiconductor-dielectric interface, so that both pentacene grain size and transistor performance were reduced. AFM measurements revealed increased



(a) (b)

Figure 4-4: (a) I-V characteristic for control transistor. (b) The circles plot mobility vs. gate voltage (right axis). The lines show the extraction of V_T from the saturation region, $V_{DS} = -100V$ (left axis).

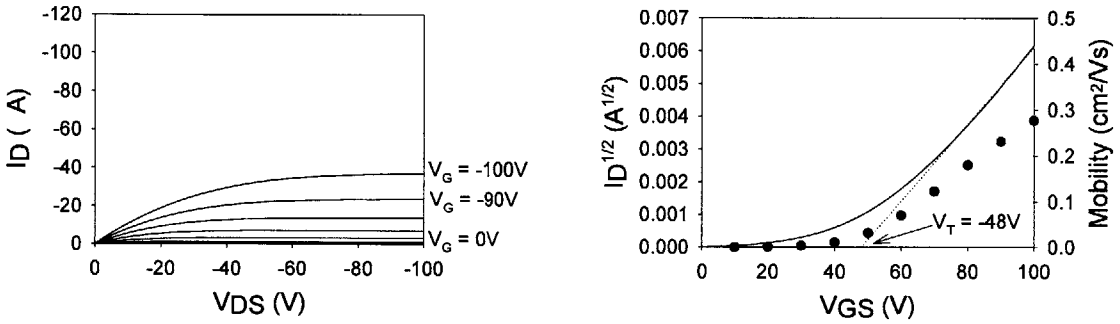


(a) (b)

Figure 4-5: (a) I-V characteristic for ammonium sulfide-treated transistor. (b) The circles plot mobility vs. gate voltage (right axis). The lines show the extraction of V_T from the saturation region, V_{DS} = -100V (left axis).

surface roughness after ammonium sulfide treatment; this roughness may explain the problem. While polystyrene treatment provides better results than the ammonium sulfide treatment, the best choice is untreated parylene. Without a considerable improvement in mobility and performance, the additional treatment requires a extra processing step that introduces more possibilities for contamination.

This section demonstrates the importance of the quality of the interface at the semiconductor-dielectric interface. The hydrophobicity of a material, measurable by contact angle, can be used to predict the quality of pentacene packing and obtainable mobility, although other factors such as surface roughness also contribute. Based on the results of this section, parylene offers a quality interface for pentacene growth. Though not employed here, other techniques that could be used to examine pentacene packing are scanning electron microscopy (SEM) and x-ray diffraction (XRD). For instance, XRD can be used to identify the crystalline phases, crystallite orientation and size. These techniques could provide additional insight to pentacene morphology.



(a) (b)

Figure 4-6: (a) I-V characteristic for polystyrene-treated transistor. (b) The circles plot mobility vs. gate voltage (right axis). The lines show the extraction of V_T from the saturation region, V_{DS} = -100V (left axis).

Chapter 5

Threshold voltage and traps

A key step in the development of OFETs is threshold voltage control, which ultimately determines circuit functionality and yield. In addition, understanding threshold voltage control enables a better understanding of transistor behavior.

A range of threshold voltages have been obtained for pentacene FETs. Positive V_Ts have been reported for FETs using solution-processed polymer dielectrics such as PVP [33] and sputtered materials such as SiO_2 [34]. These insulators tend to have incomplete cross-linking and are hence susceptible to dangling bonds and interface charges. Negative V_Ts have been reported for FETs using CVD polymer dielectrics such as parylene [24] and thermally-grown materials such as Si/SiO_2 [19, 35]. These insulators tend to have complete cross-linking and we can extrapolate that the interface will not have dangling bonds or interface charges. This suggests that the difference in threshold voltages is not necessarily intrinsic to the gate dielectric material but is related to process-dependent trap states at the semiconductor-dielectric interface.

A common approach for solution-processed dielectrics is to deposit a precursor and then perform a cross-linking step. Incomplete cross-linking results in unsatisfied bonds or reactive reagents being left over which can generate interface states. In contrast, parylene fully cross-links during deposition, obviating the need for a separate cross-linking step. Hence, we expect OFETs fabricated with a parylene gate dielectric to have low interface states, providing a suitable platform to study the effects of

process-induced traps.

In this study, pentacene OFETs with a parylene gate dielectric were fabricated and the parylene dielectric was treated with an O_2 plasma prior to pentacene deposition. We hypothesize that the O_2 treatment breaks bonds at the parylene surface, introducing parylene-pentacene interface trap states. These states dope the semiconductor, introducing mobile charges that increase parasitic bulk conductivity in the device. Trap states also introduce fixed charges that shift the threshold voltage. This chapter presents characterization results from treated and untreated devices and confirms that charges introduced by the traps influence threshold voltage and parasitic conductivity.

5.1 Process

Two sets of 42μm x 1250μm devices were fabricated together using the baseline process described in Chapter 3. Deposition of a 277nm blanket layer of parylene was followed by thermal evaporation of 10nm of pentacene at a rate of 0.1Å/s. Prior to pentacene deposition, the second set of devices underwent an additional process step. In this step, the parylene surface was treated with O_2 plasma in a Plasmod barrel plasma asher for 15 seconds. The plasma was formed at 200mTorr at 50W RF power. MIS (metal-insulator-semiconductor) capacitors were also fabricated in the same evaporation, CVD, and O_2-treatment runs. Electrical characterization of the transistors was performed using an Agilent 4156C Semiconductor Parameter Analyzer.

5.2 Threshold voltage and conductivity

Fig. 5-1a shows the I-V characteristic of a control transistor; Fig. 5-1b shows the same for an O_2 plasma treated transistor. As shown in the two plots, a dramatic change in the shape and magnitude of the drain current I_D occurs following O_2 plasma treatment of the dielectric. I_D is more than an order of magnitude larger and does not

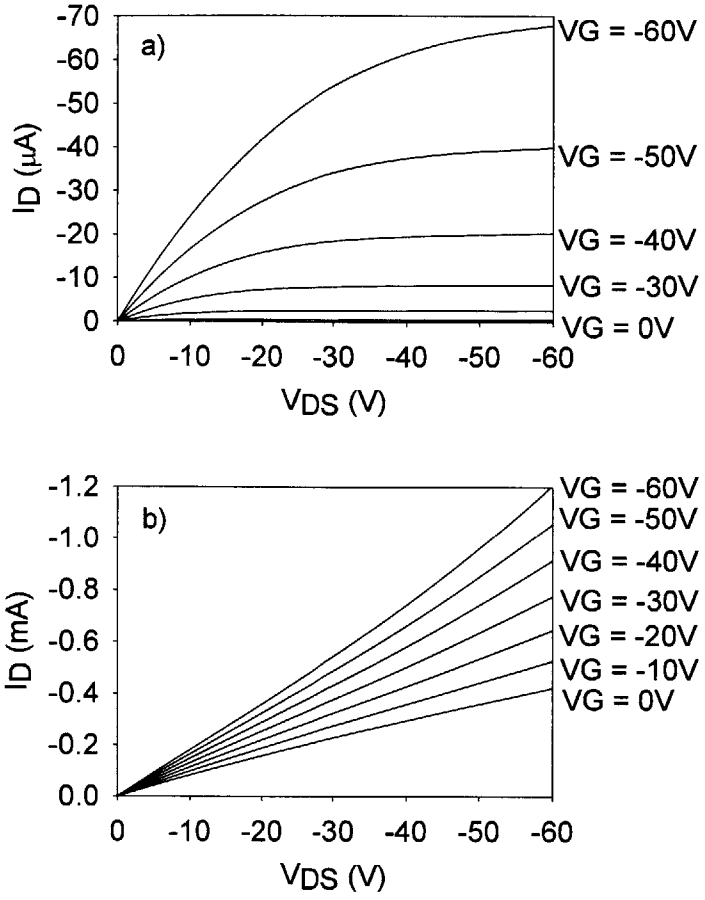


Figure 5-1: I-V characteristics for (a) control devices and (b) O_2-treated devices. The O_2-treated device shows much higher drain current and appears to have a significant parasitic bulk conductivity.

saturate in the O_2-treated device. This increase suggests (a) a change in pentacene morphology, (b) an enhanced field effect mobility, (c) a shift in threshold voltage, or (d) an increase in parasitic bulk conductance.

As noted in previous chapters, pentacene morphology has been linked to performance in OFETs and mobility has been shown to be sensitive to pentacene grain size [15]. In AFM and cross-polarization measurements of both the control and O_2-treated devices, pentacene grain sizes were approximately 150nm. The field effect mobility μ, extracted from the linear region at $V_{DS} = -10V$, changed from 0.26 $cm^2V^{-1}s^{-1}$ in the control device to 0.39 $cm^2V^{-1}s^{-1}$ in the O_2-treated device.

Neither a morphological change nor an enhanced mobility can account for the I_D increase. Both the threshold voltage and parasitic bulk conductance, however, change significantly. In the context of the following model, these two factors can explain the I_D increase in the linear region of OFET operation.

Although OFETs are typically modeled using conventional semiconductor device equations, more refined models have been developed to include the contributions of trap states as a gate voltage dependent mobility [36] or as localized band-gap states [37]. The following model attempts to explain the observed device characteristics in terms of trap-induced charges. As in [38], we assume a constant mobility and model traps as acceptors at the interface. For an OFET in the linear region, the contributions of traps are modeled as fixed and mobile charges. The model assumes a parallel conduction mechanism consisting of (a) a surface channel in which the carrier density in the surface accumulation layer is modulated by gate voltage and (b) a "bulk" layer away from the surface whose mobile carrier density is not modulated by the gate voltage. Fixed charges shift threshold voltage and mobile charges add parasitic conductivity:

$$-I_D = \frac{W}{L}\mu V_{DS}\left[C_{ins}\left(V_{GS} - (V_T - Q_{fixed}/C_{ins})\right)\right] + \frac{W}{L}\mu V_{DS} Q_{mobile} \tag{5.1}$$

where W = width of device, L = length, μ = field effect mobility, C_{ins} = dielectric insulator capacitance, V_{GS} = gate voltage, V_{DS} = drain voltage, V_T = threshold voltage, Q_{fixed} = fixed interface trap charge, and Q_{mobile} = parasitic mobile charge. This equation can then be rearranged to the form

$$-I_D = \frac{W}{L}\mu V_{DS}\left[\left(V_{GS} - V_T\right) C_{ins} + Q_{fixed} + Q_{mobile}\right] \tag{5.2}$$

and Q_{fixed} and Q_{mobile} can be determined from the I-V characteristics.

Figs. 5-2a and 5-2b show the extrapolated threshold values for the control and O_2 treated devices, respectively. As expected from the larger current modulation in the O_2-treated device I-V characteristics (Figs. 5-1a, 5-1b), threshold voltage V_T has

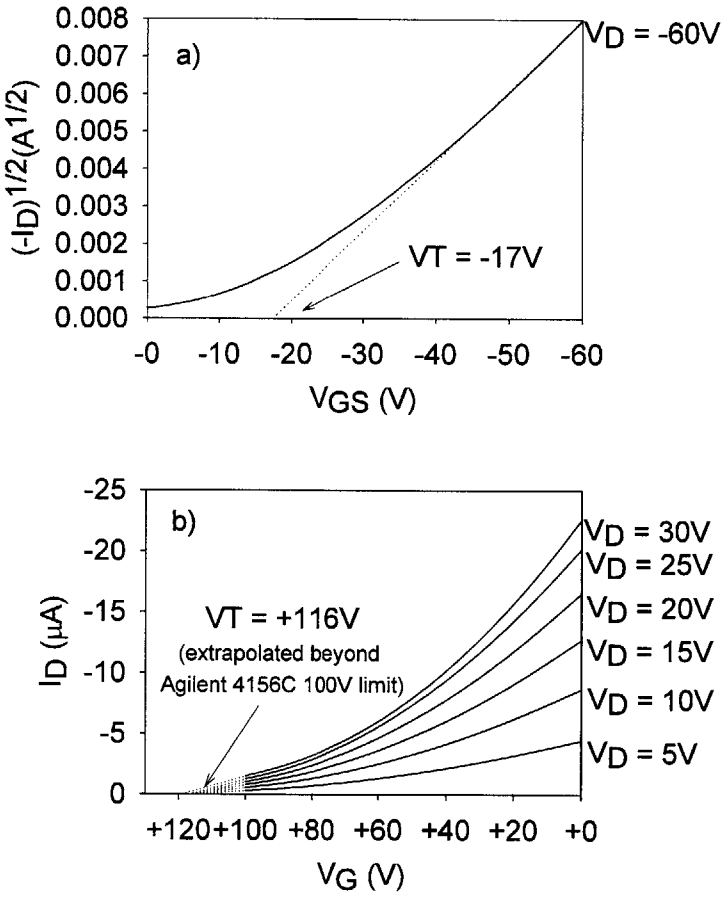


Figure 5-2: Extrapolated threshold voltage for (a) control devices and (b) O_2-treated devices. For the control device, V_T was extracted from saturation region measurements. Because the O_2-treated device does not saturate and I_D is high, V_T was extrapolated from V_{GS} close to V_T to minimize contact resistance effects. The threshold voltage has been shifted +133V by the O_2 treatment.

V_{GS}	Q_{mobile} (control)	Q_{mobile} (O_2-treated)
-30V	$5.8x10^{-8}$	$1.1x10^{-6}$
-40V	$9.2x10^{-8}$	$1.1x10^{-6}$
-50V	$1.1x10^{-7}$	$1.0x10^{-6}$
-60V	$1.1x10^{-7}$	$1.1x10^{-6}$

Table 5.1: Calculated values for Q_{mobile} at $0 \geq V_{DS} \geq -10V$.

shifted positive. V_T changes from $-17V$ in the control to $+116V$ in the O_2-treated device. Lee and Song noted a similar, much smaller, positive shift in V_T (-1.8±0.84V to 0.34±2.1V after 5 min. exposure time) following O_2 plasma treatment of pentacene FETs with an SiO_2 gate dielectric [35]. The threshold shift $\Delta V_T = +133V$ can be used to determine the relative difference in fixed charge between the control and O_2-treated devices. Using the measured value $C_{ins} = 1.5x10^{-8}F/cm^2$, $\Delta Q_{fixed} = \Delta V_T * C_{ins} = 2.0x10^{-6}C/cm^2$.

The presence of a mobile charge in the bulk produces a parasitic conductivity that is not modulated by the gate bias. The resulting increase in I_D can be modeled as $\Delta I_D = W/L * \mu V_{DS} * Q_{mobile}$, as given in the model above. Although only the relative difference in Q_{fixed} can be calculated, values for Q_{mobile} can be determined for both the control and O_2-treated devices. Since the measured values of V_T include the contribution of Q_{fixed}, Eqn. 5.2 can be written as

$$-I_D = \frac{W}{L}\mu V_{DS}\left[\left(V_{GS} - V_{T_{measured}}\right)C_{ins} + Q_{mobile}\right]$$

Differentiating this equation with respect to V_{DS} and solving for Q_{mobile}, we obtain

$$-Q_{mobile} = \left(V_{GS} - V_{T_{measured}}\right)C_{ins} + \frac{d(-I_D)/dV_{DS}}{W/L*\mu}$$

Table 5.1 gives the extracted values for Q_{mobile} in the linear region, where dI_D/dV_{DS} is calculated for $0 \geq V_{DS} \geq -10V$. The Q_{mobile} values for each device agree across several V_{GS} gate biases, indicating that the parasitic bulk conductivity is independent of gate voltage. Q_{mobile} in the O_2-treated device is an order of magnitude higher than in the control device and on the same order of magnitude as ΔQ_{fixed}.

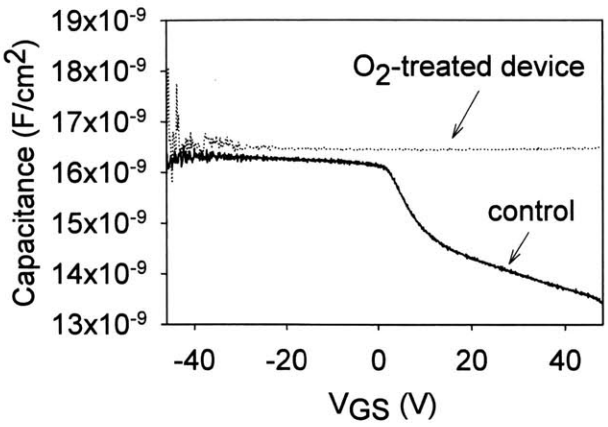


Figure 5-3: Quasistatic C-V curve for control and O_2-treated devices. The control device is in accumulation for negative gate voltages and enters depletion for positive V_{GS}. The O_2-treated device remains in accumulation throughout the measurement range and does not reach flatband.

5.3 Capacitance

The presence of traps introduced by O_2 plasma treatment is also observable in capacitance measurements. Quasistatic C-V measurements were performed using an Agilent 4156C Semiconductor Parameter Analyzer. An HP 4192A LF Impedance Analyzer was used to take C-V measurements from 1 kHz to 1MHz. Since O_2 plasma treatment etches parylene, the dielectric capacitance of the O_2-treated device is slightly higher than that of the control. Parylene thickness in the O_2-treated device was reduced from 277nm to 258nm, as measured using a Dektak Surface Profiler.

As shown in the quasistatic C-V curve (Fig. 5-3), the control device goes through accumulation, flatband, and depletion over the $-45\text{V} \leq V_{GS} \leq +45\text{V}$ measurement range. In contrast, the O_2-treated device stays in accumulation throughout. This shift in flatband voltage confirms the threshold voltage shift seen in the I-V characteristics and supports the existence of traps at the parylene surface.

Traps can be modeled as capacitances with an RC time constant related to the trapping and release of carriers [39, 40]. We modeled the parylene-pentacene interface as a combination of 3 capacitances: the pentacene depletion capacitance, traps on the dielectric, and the dielectric capacitance. In the conventional metal-oxide-

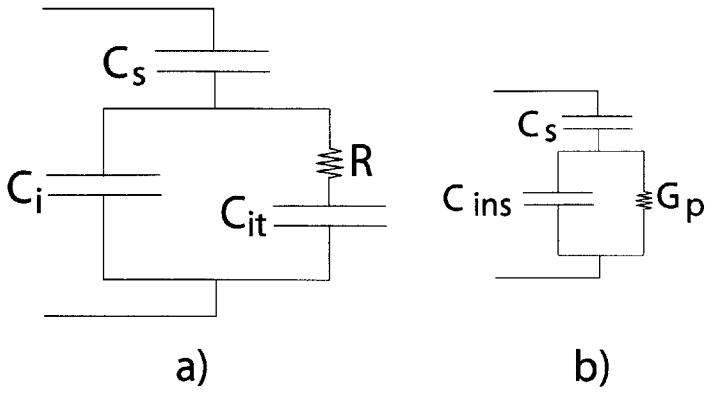


Figure 5-4: (a) Capacitance model. C_i is the parylene insulator capacitance; C_s is the semiconductor depletion capacitance; and C_{it} is the trap capacitance. Traps are modeled as a parastitic RC leg in parallel with the dielectric. (b) Equivalent capacitance model. Note that C_{ins} is the parallel combination of C_i and C_{it}.

semiconductor (MOS) capacitor model, interface traps are modeled in parallel with the semiconductor depletion capacitance, connected in series with the dielectric capacitance [39]. The total MOS capacitance then must be less than the dielectric capacitance alone, which was not the case in our measured data. In the proposed model, the interface traps are in parallel with the insulator capacitance (Fig. 5-4). The total capacitance is then

$$C_{total} = \left(\frac{1}{C_s} + \frac{1}{C_i + C_{it}}\right)^{-1} \tag{5.3}$$

where C_i = the parylene insulator capacitance, C_s = the semiconductor depletion capacitance, and C_{it} = the trap capacitance. In accumulation, the depletion capacitance C_s drops out and the model simplifies to the parallel combination of C_i and C_{it}, or C_{ins}.

The device was assumed to be in accumulation at a gate bias of -35V. From manufacturer data [23], we expected the parylene insulator capacitance to be constant over the frequency range measured. Measurements of plain metal-parylene-metal (MIM) capacitors support this assumption. From those measurements, C_i was found to be $9.4\text{x}10^{-9}\text{F/cm}^2$. Using this value, we calculated C_{it} for the control and O_2-treated devices for frequencies from 1kHz to 1MHz.

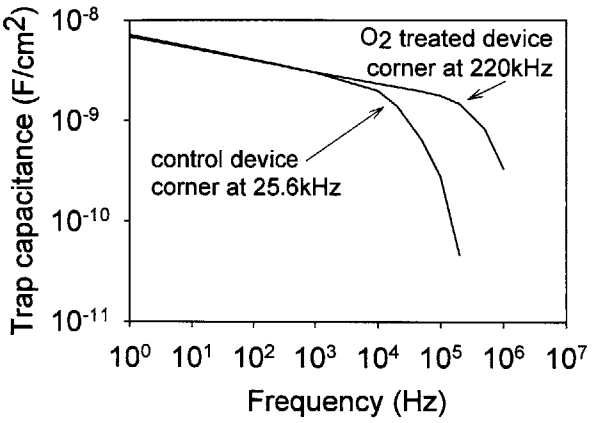


Figure 5-5: Extracted trap capacitances for control and O_2-treated devices as a function of frequency. The trap capacitance in the O_2-treated device is higher throughout the measured frequency range and falls off at a higher frequency than C_{it} in the control device. These observations suggests that the traps in the O_2-treated device are both faster and more numerous than in the control.

Extracted values for the trap capacitance C_{it} in the control and the O_2-treated devices are plotted in Fig. 5-5. The O_2-treated device's capacitance is always greater than that of the control. In addition, the dominant pole rolloff due to the trap-related RC time constant has moved out from 25.6kHz in the control device to 220kHz in the O_2-treated device. This data indicates that (1) more traps have been introduced by the O_2 treatment and (2) that the introduced traps are faster than the native traps seen in the control device.

As frequency increases, slower traps can no longer follow the AC voltage and at high frequency we expect reduced participation of traps [39]. Figs. 5-6a and 5-6b show decreasing capacitance with increasing frequency for both devices. As the test frequency increases from 1kHz to 1MHz, the O_2-treated device C-V measurements begin to look more like the control as the depletion capacitance reappears (Fig. 5-7).

5.4 Photosensitivity

The traps introduced by the O_2 treatment are also observable using photosensitivity measurements [41]. We characterized the O_2-treated and control devices in the dark

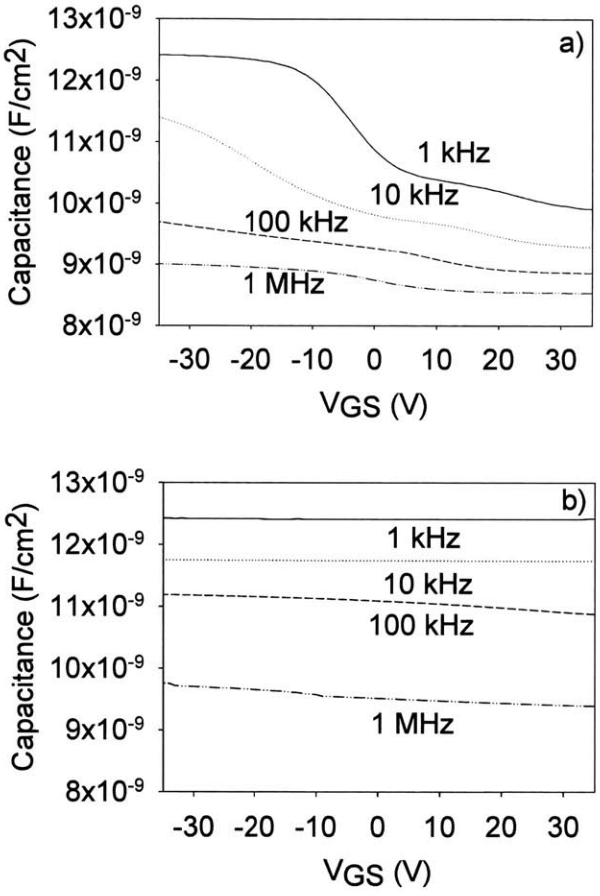


Figure 5-6: High-frequency C-V measurements of (a) control device and (b) O_2-treated device.

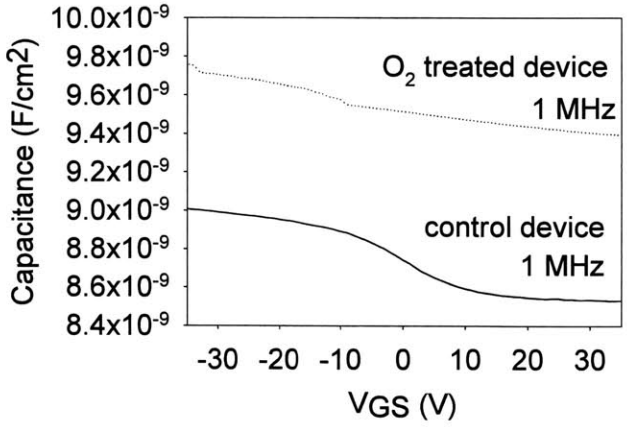


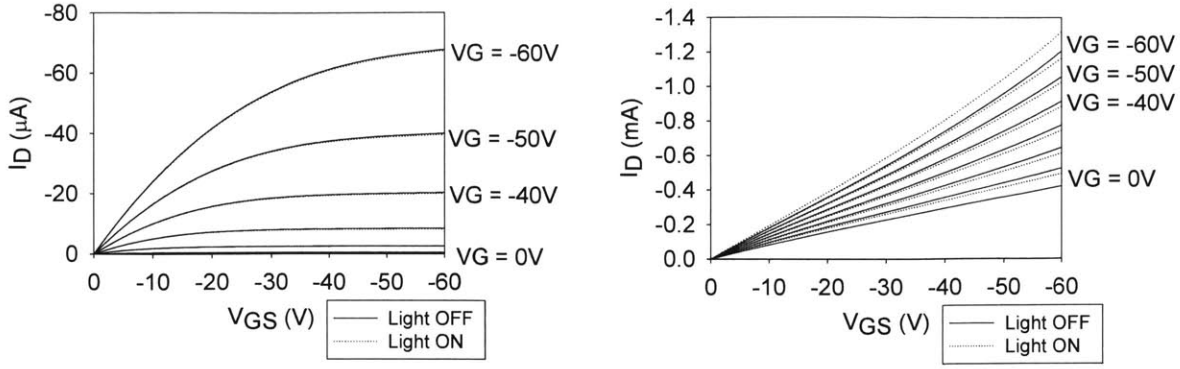
Figure 5-7: Comparison of 1MHz C-V measurements of control and O_2-treated devices. At higher test frequencies, the participation of traps is reduced and the C-V measurements of the O_2-treated device approach those of the control.

and under $3.4x10^3$ cd/m^2 luminance. At V_{DS}=V_{GS}=−60V, I_D changed by 0.5% in the control device, while in the O_2-treated device I_D increased by 8.3±1.0% (Fig. 5-8). This photosensitivity suggests that the traps introduced by the O_2 treatment can be probed optically.

5.5 Summary

Although AFM and cross-polarization measurements were performed to verify that the O_2 plasma treatment does not change the pentacene growth at the interface, another measurement technique that could be used is x-ray diffraction. Observation of the crystalline phases and crystallite sizes in the pentacene layer would confirm that the O_2 treatment does not affect pentacene growth.

We found that O_2 plasma treatment of the gate dielectric introduces trap states that can be observed through a variety of techniques. These traps induced both fixed charges that influence threshold voltage and mobile charges that increase parasitic bulk conductivity. A model was developed to explain the observed device characteristics in terms of these charges. Since this technique results in a negative threshold voltage shift, it can potentially be a way to tune threshold voltage at the process level



(a) (b)

Figure 5-8: I-V characteristics for (a) control device and (b) O_2-treated device in the dark and under illumination. The O_2-treated device exhibits enhanced photosensitivity.

for organic FETs.

Chapter 6

Conclusion

The gate dielectric material is an important research area in the development of OFETs. In this thesis, parylene was shown to be a good choice for a gate dielectric in pentacene FETs for (a) process compatibility, (b) low gate leakage, (c) a high quality interface for pentacene growth, and (d) easily modifiable surface characteristics. While two surface treatments were explored to increase the hydrophobicity of the parylene surface, neither the ammonium sulfide nor the polystyrene treatment resulted in significant improvements in pentacene packing and mobility. Parylene alone is already hydrophobic and provides a quality surface for pentacene growth since it is a fully cross-linked polymer.

By modifying the parylene surface using an oxygen plasma, traps were introduced at the semiconductor-dielectric interface. The contribution of traps to device behavior was studied and modeled in terms of the trap-induced fixed and mobile charges. Since the threshold voltage is modified by process-dependent traps at the interface, this method is a potential way to control threshold voltage at the process level. Further study is required to fully understand the contribution of traps and to find a way to remove or control the parasitic parallel conduction. These issues are essential to the development of organic FETs with controllable characteristics.

Bibliography

[1] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic thin film transistors for large area electronics," *Adv. Mat.*, vol. 14, no. 2, pp. 99–117, Jan. 2002.

[2] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM J. Res. & Dev.*, vol. 45, no. 1, Jan. 2001.

[3] E. Bonderover, S. Wagner, and Z. Suo, "Amorphous silicon thin film transistors on kapton fibers," in *Mater. Res. Soc, Electronics on Unconventional Substrates - Electrotextiles and Giant-Area Flexible Circuits Symposium Proceedings*, vol. 736, 2003, pp. 109–114.

[4] J. Lee and V. Subramanian, "Organic transistors on fiber: A first step towards electronic textiles," presented at the IEEE International Electron Devices Meeting (IEDM), Washington D.C., Dec. 2003.

[5] T. Someya and T. Sakurai, "Integration of organic field-effect transistors and rubbery pressure sensors for artificial skin applications," presented at the IEEE International Electron Devices Meeting (IEDM), Washington D.C., Dec. 2003.

[6] B. K. Crone, A. Dodabalapur, R. Sarpeshkar, R. W. Filas, Y.-Y. Lin, Z. Bao, J. H. O'Neill, W. Li, and H. E. Katz, "Design and fabrication of organic complementary circuits," *J. Appl. Phys.*, vol. 89, no. 9, pp. 5125–5132, May 2001.

[7] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, "Polymer gate dielectrics and conducting-polymer contacts for high-performance organic thin-film transistors," *Adv. Mat.*, vol. 14, no. 23, Dec. 2002.

[8] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, "Pentacene-based radio-frequency identification circuitry," *Appl. Phys. Lett*, vol. 82, no. 22, pp. 3964–3966, June 2003.

[9] G. Horowitz, X. Peng, D. Fichou, and F. Garnier, "The oligothiophene-based field-effect transistor: How it works and how to improve it," *J. Appl. Phy.*, vol. 67, pp. 528–532, Jan. 1990.

[10] S. M. Sze, *Semiconductor devices: physics and technology.* New York: John Wiley & Sons, 1985.

[11] V. Podzorov, V. M. Pudalov, and M. E. Gershenson, "Field effect transistors on rubrene single crystals with parylene gate insulator," *Appl. Phys. Lett.*, vol. 82, no. 11, pp. 1739–1741, Mar. 2003.

[12] V. Y. Butko, X. Chi, D. V. Lang, and A. P. Ramirez, "Field-effect transistor on pentacene single crystal," *Appl. Phys. Lett*, vol. 83, no. 23, pp. 4773–4775, Dec. 2003.

[13] V. Y. Butko, X. Chi, and A. P. Ramirez, "Free-standing tetracene single crystal field effect transistor," *Solid State Communications*, vol. 128, pp. 431–434, 2003.

[14] D. Knipp, R. A. Street, A. Volkel, and J. Ho, "Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport," *J. Appl. Phys.*, vol. 93, no. 1, pp. 347–355, Jan. 2003.

[15] C. D. Dimitrakopoulos, A. R. Brown, and A. Pomp, "Molecular beam deposited thin films of pentacene for organic field effect transistor applications," *J. Appl. Phys.*, vol. 80, no. 4, pp. 2501–2508, Aug. 1996.

[16] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, "Patterning pentacene organic thin film transistors," *J. Vac. Sci. Technology B*, vol. 20, no. 3, pp. 956–959, May/June 2002.

[17] D. J. Gundlach, C.-C. Kuo, S. F. Nelson, and T. N. Jackson, "Organic thin film transistors with field effect mobility >2 cm^2/v-s," in *57th Annual Device Research Conference Digest*, June 1999, pp. 164 – 165.

[18] I. Kymissis, "Morphology and performance in pentacene," Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, 1999.

[19] Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, "Stacked pentacene layer organic thin-film transistors with improved characteristics," *IEEE Elecron Device Lett.*, vol. 18, no. 12, pp. 606–608, Dec. 1997.

[20] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, "High-performance bottom electrode thin-film transistors," *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1060–1064, June 2001.

[21] D. Knipp, R. A. Street, and A. R. Volkel, "Morphology and electronic transport of polycrystalline pentacene thin-film transistors," *Appl. Phys. Lett.*, vol. 82, no. 22, pp. 3907–3909, June 2003.

[22] T. Yasuda, K. Fujita, H. Nakashima, and T. Tsutsui, "Organic field-effect transistors with gate dielectric films of poly-p-xylylene derivatives prepared by chemical vapor deposition," *Japan. J. Appl. Phys. Part 1*, vol. 42, no. 10, pp. 6614–6618, Oct. 2003.

[23] *Parylene Conformal Coating Specifications & Properties*, Specialty Coating Systems, Cookson Electronics. [Online]. Available: http://www.scscookson.com/parylene/properties.cfm

[24] C. D. Dimitrakopoulos, B. K. Furman, T. Graham, S. Hegde, and S. Purushothaman, "Field-effect transistors comprising molecular beam deposited α,ω-di-hexyl-hexathienylene and polymeric insulator," *Synth. Met.*, vol. 92, pp. 47–52, 1998.

[25] J. J. Senkevich, G.-R. Yang, and T.-M. Lu, "The facile surface modification of poly(p-xylylene) ultrathin films," *Colloids and Surfaces A: Physiochem. Eng. Aspects*, vol. 216, no. (1-3), pp. 167–163, Apr. 2003.

[26] *DuPont Kapton E High Modulus Polyimide Film*, DuPont High Performance Materials. [Online]. Available: http://www.dupont.com/kapton/products/H-78305.html

[27] P. Richman, *Characteristics and operation of MOS field-effect devices.* New York: McGraw-Hill, 1967.

[28] S. F. Nelson, Y.-Y. Lin, D. J. Gundlach, and T. N. Jackson, "Temperature-independent transport in high-mobility pentacene transistors," *Appl. Phys. Lett.*, vol. 72, no. 15, pp. 1854–1856, Apr. 1998.

[29] C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, "Low-voltage organic transistors on plastic comprising high-dielectric constant gate insulators," *Science*, vol. 283, pp. 822–824, Feb. 1999.

[30] C. D. Dimitrakopoulos, I. Kymissis, S. Purushothaman, D. A. Neumayer, P. R. Duncombe, and R. B. Laibowitz, "Low-voltage, high-mobility pentacene transistors with solution-processed high dielectric constant insulators," *Adv. Mat.*, vol. 11, no. 16, pp. 1372–1375, 1999.

[31] M. Kiguchi, M. Nakayama, K. Fujiwara, K. Ueno, T. Shimada, and K. Saiki, "Accumulation and depletion layer thicknesses in organic field effect transistors," *Japan. J. Appl. Phys. Pt. 2*, vol. 42, no. 12A, pp. L1408–L1410, Dec. 2003.

[32] D. K. Schroder, *Advanced MOS Devices*, ser. Modular series on solid state devices. Reading, MA: Addison-Wesley, 1987.

[33] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, W. Radlik, S. Ponomarenko, S. Kirchmeyer, and W. Weber, "High-mobility organic thin-film transistors based on α,α'-didecyloligothiophenes," *J. Appl. Phys.*, vol. 93, no. 5, pp. 2977–2981, Mar. 2003.

[34] H. Klauk, D. J. Gundlach, and T. N. Jackson, "Fast organic thin-film transistor circuits," *IEEE Electron Device Lett.*, vol. 20, no. 6, pp. 589–291, June 1999.

[35] M. W. Lee and C. K. Song, "Oxygen plasma effects on performance of pentacene thin film transistor," *Japan. J. Appl. Phys. Pt. 1*, vol. 42, no. 7A, pp. 4218–4221, 2003.

[36] P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson, "Modeling of organic thin film transistors of different designs," *J. Appl. Phys.*, vol. 88, pp. 6594–6597, Dec. 2000.

[37] A. R. Volkel, R. A. Street, and D. Knipp, "Carrier transport and density of state distributions in pentacene transistors," *Physical Review B*, vol. 66, p. 195336, 2002.

[38] R. A. Street, D. Knipp, and A. R. Volkel, "Hole transport in polycrystalline pentacene transistors," *Appl. Phys. Lett.*, vol. 80, pp. 1658–1660, Mar. 2002.

[39] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology.* New York: Wiley-Interscience, 1982.

[40] D. K. Schroder, *Semiconductor material and device characterization.* New York: Wiley-Interscience, 1998.

[41] G. Jarosz, R. Signerski, and J. Godlewski, "Photoenhanced currents in pentacene layers," *Adv. Mat. for Opt. and Electr.*, vol. 6, pp. 379–382, 1996.