Characterization and Modeling of Polysilicon MEMS Chemical-Mechanical Polishing

By

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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

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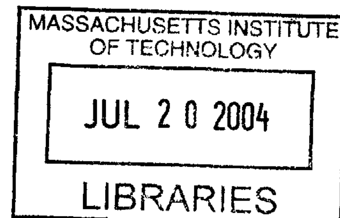

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ABSTRACT

Heavily used in the manufacture of integrated circuits, chemical-mechanical polishing (CMP) is becoming an enabling technology for microelectomechanical systems (MEMS). To reliably use CMP in the manufacturing process, designers must be able to accurately predict the CMP process and control final surface uniformity. This thesis extends integrated circuit CMP knowledge towards MEMS applications. Experiments were performed to characterize polysilicon MEMS CMP. A new test mask was created which contains test structures relevant to MEMS. Both single and dual material polish experiments were carried out and the resulting data fit against an adapted step height density model. Results show that integrated circuit CMP models are applicable to MEMS CMP, but the models need to be adjusted in order to contend with issues inherent to MEMS CMP. Further study may be necessary to accurately and completely characterize polysilicon MEMS CMP and make improvements to the models.

Thesis Supervisor: Duane S. Boning
Title: Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction and Motivation for Research

This chapter presents the motivation for studying chemical-mechanical polishing (CMP) for polysilicon microelectromechanical (MEMS) structures. Besides highlighting the uses of CMP in the fabrication of MEMS devices, it discusses how the process works and the key criteria used to characterize and evaluate CMP.

1.1 Motivation

Chemical-Mechanical Polishing (CMP) serves as the dominant method for wafer planarization in the integrated circuit industry. It is used in front end processing to remove the oxide overburden for shallow trench isolation. It also aids in the back end process to create metal interconnects, where CMP has been used for both oxide dielectric polishing, and damascene copper interconnect formation. Because of the key role CMP plays in the creation of integrated circuits, most past work has focused on examining the polish process for the ever-shrinking feature sizes prevalent in integrated circuits.

The MEMS industry, on the other hand, does not necessarily gain the same benefits from miniaturization. Mechanical structures might require features orders of magnitude larger than transistor gates. Without large structures to provide mass, MEMS based accelerometers and pressure sensors would not be sensitive enough to provide accurate readings. Integrated circuit CMP models focus on oxide, dielectrics, and copper

interconnects. MEMS CMP must cover a broader set of standard and non-standard materials, such as silicon carbide [1]. Our study examines the polishing of polysilicon, a structural material used widely in MEMS devices [2].

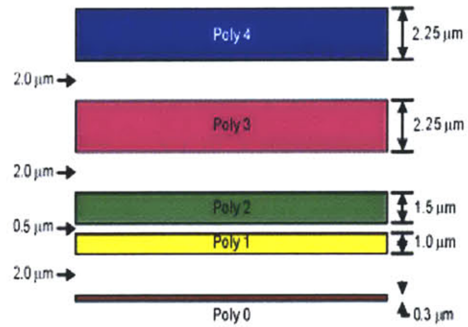


Figure 1-1: Four layers of oxide interspersed between 5 layers of polysilicon in the Sandia SUMMiT V process [3].

CMP plays an integral role in polysilicon surface micromachining. The Sandia SUMMiT V surface micromachining process [3] uses thick alternating layers (1-5µm) of polysilicon an oxide to build multilevel devices, as shown in Figure 1-1. However, each additional layer compounds topography from the lower layouts, causing lithography problems, layer-to-layer interference, and stringers. Nasby et al. [4] utilized CMP to flatten out the intermediate sacrificial layers and eliminate problems caused by topography build-up.

Besides planarizing intermediate layers like in Figure 1-2, Hetherington et al. [2] used CMP on structural device layers to ensure flat surfaces for optical devices and to reduce surface roughness, as seen in Figure 1-3. CMP plays an important role in polysilicon

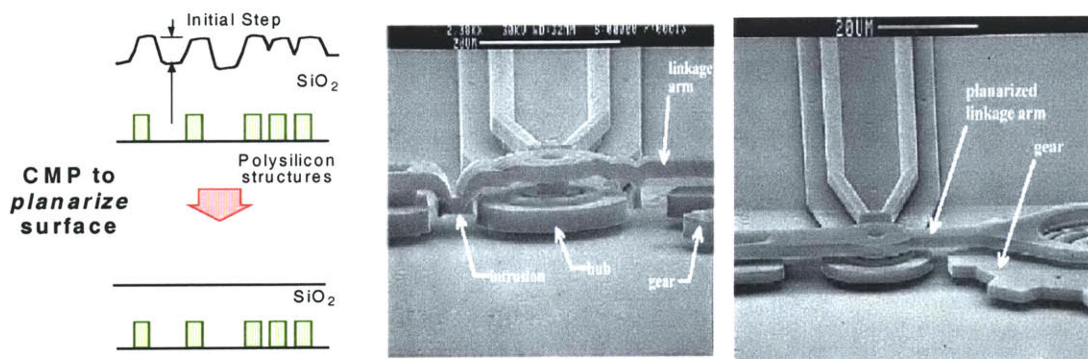


Figure 1-2: CMP eliminates topography in the intermediate layers of a MEMS gear system [4].

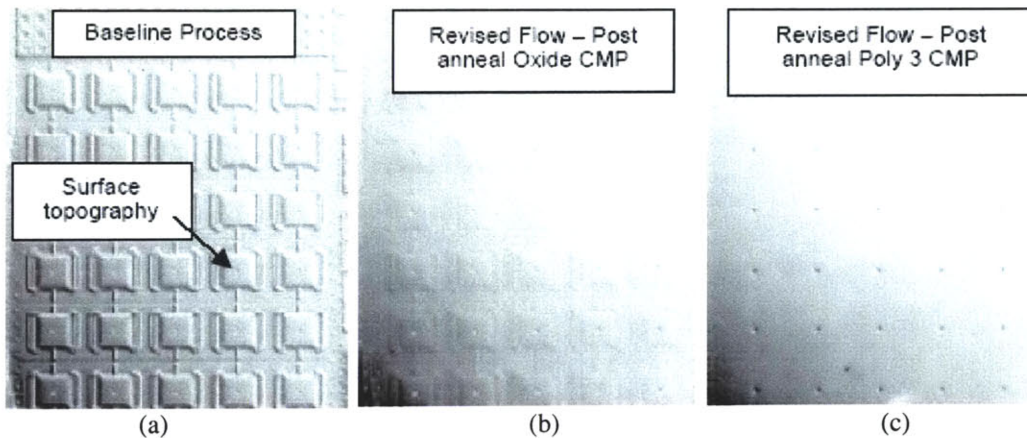


Figure 1-3: Polysilicon micromirror array topography after (a) the baseline process, (b) intermediate layer oxide CMP, (c) and polysilicon CMP [2].

surface micromachining to eliminate large step heights for thick films and to reduce surface roughness.

Besides planarizing surfaces, CMP is used to polish back material overburden to inlay material. Trenches are filled with polysilicon and planarized with CMP as shown in Figure 1-4. Fleming et al. [5] used this procedure to create high aspect ratio MEMS structures. CMP plays a crucial role in the fabrication of these polysilicon structures.

Another important difference between IC and MEMS CMP relates to wafer bonding,

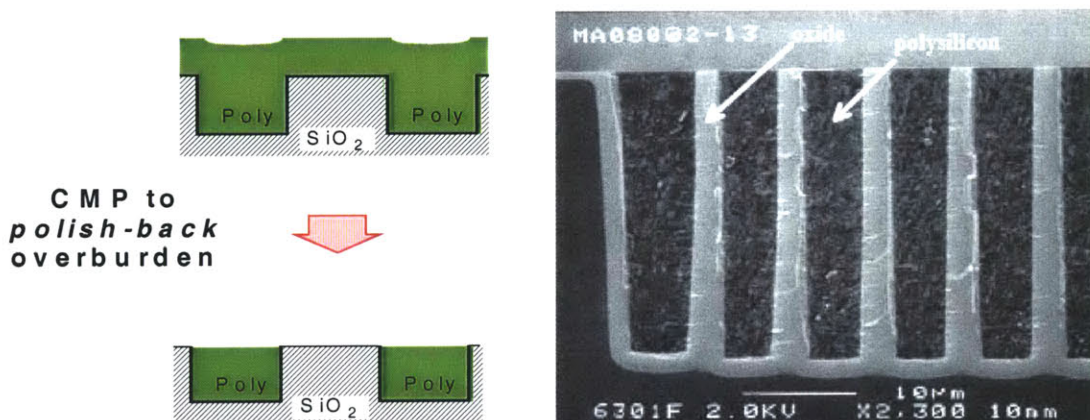


Figure 1-4: CMP to polish back overburden inlays polysilicon in a MEMS accelerometer proof mass [5].

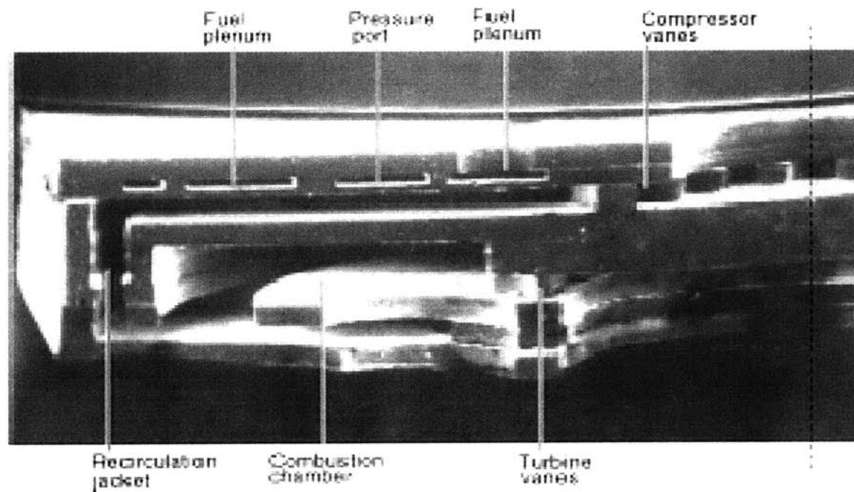


Figure 1-5: A cross section of the MIT Microengine. The device is created wafer bonding [6].

an enabling technology for many types of MEMS devices. Figure 1-5 illustrates the MIT Microengine, a device created through wafer bonding. Each wafer is individually patterned with a different layout to create the different parts of the engine. After the individual wafers are patterned and etched, the turbo engine is completed by bonding the stack of seven patterned wafers together [6]. Fabrication creates die and wafer level features, but will also increase surface roughness, impeding wafer bonding. CMP can be used for surface preparation to decrease the surface topography and roughness, and can enable previously non-bonding wafer pairs to bond [7].

At the same time, the polishing process will also affect the wafer's structural patterns. CMP may result in global non-uniformity caused by differences in pattern density or feature size across the die and wafer. Because this non-uniformity can affect device behavior, we need to characterize and model the CMP process. However, we cannot assume CMP will be the same for MEMS as it is for integrated circuits. The broader material set, thicker films, larger feature sizes, and other unique characteristics of MEMS might have wide implications upon our modeling and understanding of CMP.

1.2 Polysilicon Chemical Mechanical Planarization

As the name implies, CMP uses two synergistic methods to planarize wafer. At the macroscale, a large machine physically holds a wafer in place and mechanically wears away material from the wafer surface. At the atomic scale, chemical interactions lead to the breakdown of thin films, enhancing the ability of the macroscale machine to remove material.

1.1.1 CMP Machine and Pad

A CMP machine includes many different parts, as shown in Figure 1-6. The slurry feed introduces an abrasive chemical solution. This slurry can vary in particle size and composition. For polysilicon polishing, the Semisphere SS-25 slurry includes colloidal silica particles in an alkaline solution. The polishing head includes the carrier and holder, and is used to hold a wafer in place during polishing. Once in place, the wafer can be brought into contact with the polishing pad. The polishing head provides a down force to contact the wafer to the pad, and provides a back pressure to keep the wafer and pad in contact.

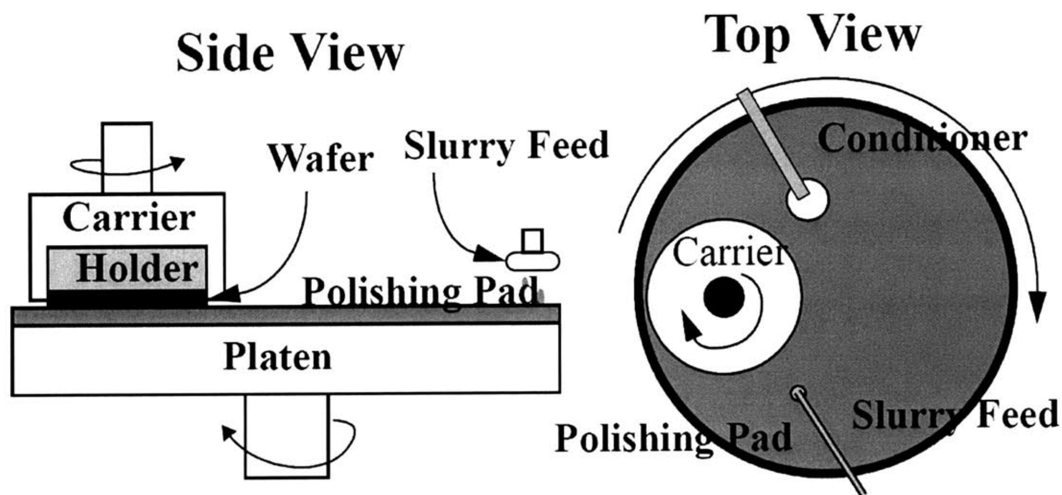


Figure 1-6: Diagram of a CMP tool.

Pads can be made from different materials, but must be able to hold and transport slurry. The pad used in the work reported here is a Rodel IC1000/Suba IV K-groove stacked polyurethane pad. Grooves in the pad measure 500 μm across and are placed 600 μm away from one another. The polishing pad sits upon the platen, which rotates independently of the carrier.

Material is removed from the wafer by a combination of mechanical and chemical methods. The rotation and pressure from the platen and carrier provides movement for the pad and abrasives to mechanically remove material. The slurry chemically modifies the surface of the wafer to ease material removal through mechanical methods.

1.1.2 Polysilicon CMP chemistry

Pietsch et al. [8] studied and proposed a removal mechanism of silicon using a silica slurry. For the proposed removal method seen in Figure 7, the slurry pH affects the way the silicon surface breaks apart.

Removal rate is the highest when pH of the system is at 11. The OH^- ions (site 1) strongly polarize surface Si-Si bonds (site 2), allowing attack on the silicon lattice. These polarized bonds easily react with either water or dissolved oxygen, breaking the silicon atoms apart (site 3a) or creating an internal oxygen bridge (site 3) between silicon atoms. A combination of mechanical action and back bond water attack (site 4) then splits the silicon atoms away from the bulk substrate, creating silica molecules in solution. The type of silica produced by the CMP depends on the amount of oxygen incorporated into the silicon surface. If the surface is attacked with only water, monomeric silica is produced (site 5). One internal oxygen bridge will causes the formation of dimeric silica (site 5a), two oxygen bridges the formation of trimeric silica (not shown), and so forth.

When the pH is below 11, CMP leads to silicon removal through a different mechanism. Here, the silicon surface terminating hydrogen atoms are replaced by OH^- through acid-base reactions. The surface terminating OH^- groups strongly polarize one of the silicon atoms, permitting a Si-Si bond to be broken by water. Once this occurs, CMP removes material in the same way as the case where the pH is 11, except no silicon-oxygen bridges are formed. The only products are monomeric silica for this case. The removal mechanism can be seen in Figure 1-7.

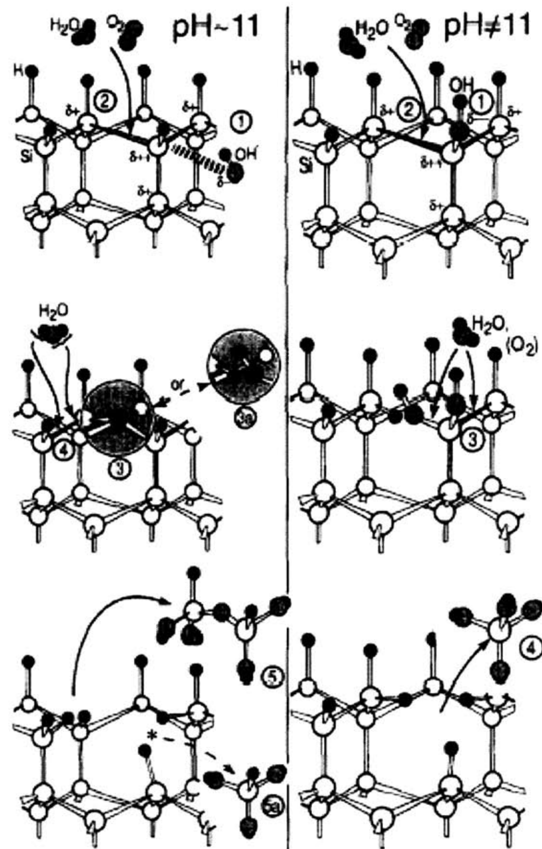


Figure 1-7: The removal mechanism for silicon when (a) the pH = 11, and (b) the pH ≠11 from [8].

1.3 Planarization uniformity metrics

In the ideal case, CMP would result in a perfectly flat surface film independent of the starting wafer topography. For the case where we planarize a surface, local regions are planarized very well by the CMP process. But variations in the underlying pattern density create global non-uniformities: different pattern density regions will eventually polish at the same rate, but a step height difference will remain and not be removed. The length scale where two different regions are locally planarized, but with different step height is called the planarization length. The planarization length can be examined in Figure 1-8.

CMP is also used to in damascene procedures to inlay one material within another. We want to CMP all the overburden polysilicon away, so that our material is perfectly inlaid within the oxide. Again, pattern density effects will alter the final film thicknesses after CMP, as can be seen in Figure 1-9. The same wafer will have areas where the polysilicon has been cleared, while other areas will not be cleared. For some of the cleared areas, the underlying oxide film will be polished, causing erosion. Other areas where the polysilicon is being inlaid will have dishing caused by over-polish. All of these issues affect the uniformity of CMP for damascene inlaid devices.

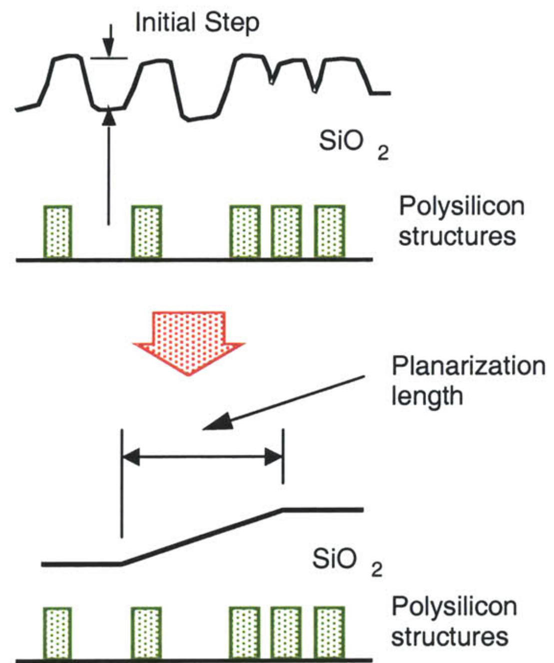


Figure 1-8: Planarization length

In the ideal case, regions are cleared of their overburden, and no dishing or erosion occurs. However, these non-uniformities are present in real world polishing. This work attempts to model the polishing process for polysilicon. We use the concepts of planarization length, dishing, and erosion to calibrate and examine whether our model accurately predicts the result of polysilicon CMP.

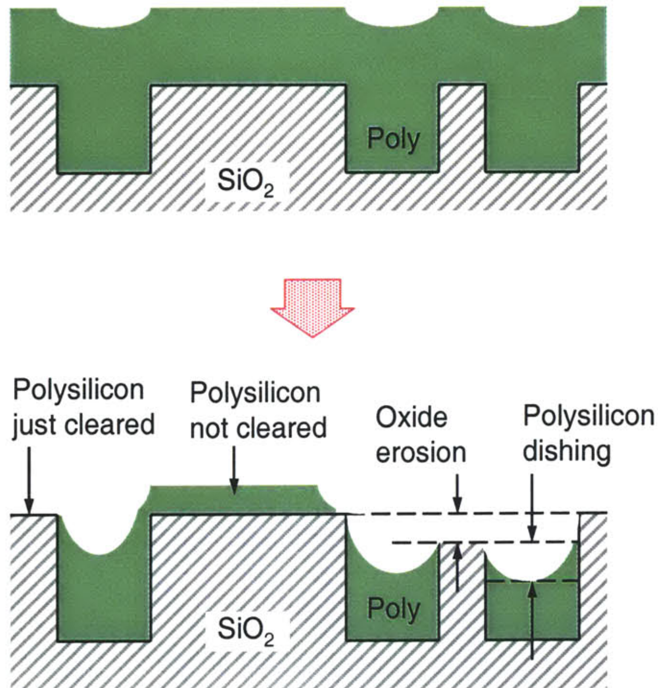


Figure 1-9: Overburden polishing showing non-uniformities.

1.4 Thesis Organization

The goal of this thesis is to characterize and model polysilicon polishing for MEMS applications. Specifically, we want to examine MEMS design characteristics and incorporate them into our model for CMP. Chapter 2 will review past models developed for CMP, and Chapter 3 will apply the models to a preliminary polysilicon MEMS CMP experiment. The results of the preliminary experiment lead to the creation of a new test mask. Chapter 4 documents the new MEMS test mask developed specifically to study, model and characterize MEMS CMP. Using the MEMS test mask, Chapter 5 describes a design of experiments and new results for MEMS CMP. Lastly, Chapter 6 presents our conclusions as well as future work.

Chapter 2

CMP Modeling Methodology

A model that accurately predicts post-CMP film thickness variation across an entire die or wafer is an invaluable tool for device designers. Designers working with multilevel planar processes can determine the uniformity of their post polish films. Optical device designers can examine whether their post-polish films meet optical tolerances. Dishing and erosion effects can be calculated for devices which use CMP to inlay one material within another. In this chapter, we examine the CMP models previously developed at the Massachusetts Institute of Technology. After reviewing these models, we adapt the updated density step height model to apply it to the polysilicon/nitride MEMS polishing experiments reported in this thesis.

2.1 Pattern Density Model

The pattern density model was initially developed to model oxide dielectric CMP for metal interconnect formation. Proposed by Stine et al. [9], the pattern density CMP model utilizes the wafer blanket removal rate K and effective pattern density $\rho(x, y)$ to analytically determine how features are polished. This formula comes from Preston's equation, and relates the polishing of features to pressure P, relative velocity v, and the empirical Preston coefficient k_p.

$$\frac{dz}{dt} = -\frac{K}{\rho(x,y)} = -k_p Pv \tag{1}$$

The polishing rate applies to areas of raised features, or "up" areas, as seen in Figure 2-1. We assume that the "down" areas are not polished until all up areas are cleared away and the step height between "up" and "down" areas is reduced to zero. After this reduction, the model assumes that the region is polished at the blanket removal rate.

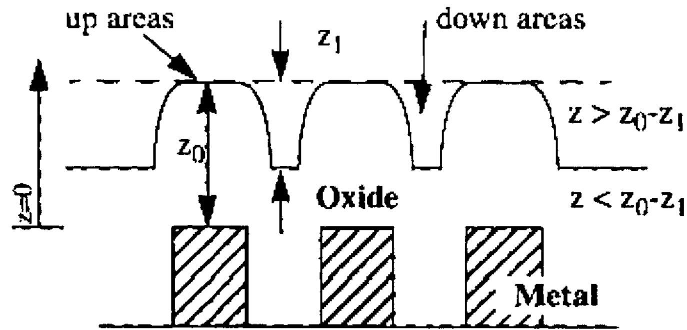


Figure 2-1: Terms used in the pattern density model [9].

The final film thickness at time *t* give by the model is:

$$z = \begin{cases} z_0 - \left(\dfrac{Kt}{\rho(x,y)}\right) & t < \rho(x,y)z_1 / K \\ z_0 - z_1 - Kt + \rho(x,y)z_1 & t > \rho(x,y)z_1 / K \end{cases} \tag{2}$$

Up area polishing depends on ρ, the effective density at location *(x, y)* on the die, and remains independent of time. We use the effective density of a position (*x*, *y*) to represent the idea that a real pad is not infinitely rigid. Rather, a pad can bend around the features on the wafer surface. Thus, the effective density represents a smoothing of the pattern density around one region. The effective density of position (*x*, *y*) is calculated by convolving a filter function around each position, averaging the local density around the

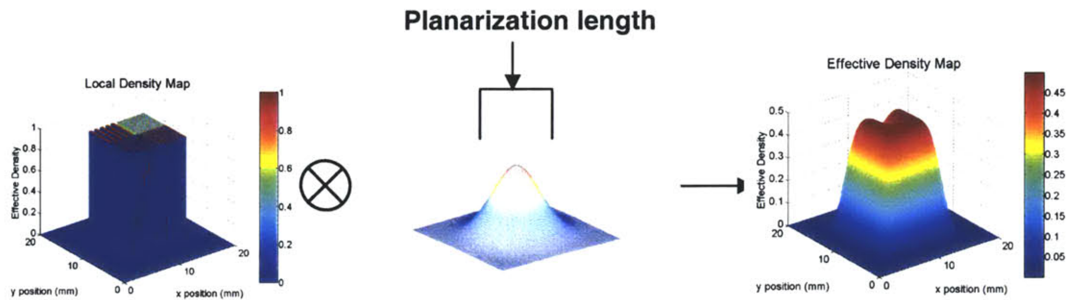


Figure 2-2: The local density is convolved with the Gaussian filter to get the effective density.

point (x, y), as shown in Figure 2-2. To define the size of the filter used, we go back to the idea of the *planarization length* defined earlier in Chapter 1. The planarization length represents the length scale over which two local regions are planarized, but a global step height still exists. It represents the limits of a pad and process's ability to planarize a surface. The planarization length incorporates assumptions about the behavior of the pad and process at a certain point (x,y) and explains how close features in the surrounding environment must be in order to affect the polishing at point (x,y).

The different density filters can take different shapes, such as squares, cylinders, Gaussian shapes, elliptical shapes, or cone shapes with the form of $1/(r+a)^b$. Ouma compared the effectiveness of several filter weighting functions, and found the elliptical shape to have the best performance [10]. The elliptical shape is thought to give the best performance because it is conceptually close to the physical bending of the CMP pad. Because the Gaussian also does an excellent job of approximating the model response and is computationally simple to use, the Gaussian is adopted in the work reported here. For the Gaussian filter, the planarization length is defined to be twice the standard deviation of the filter. Once the filter function shape and planarization length have been

selected, the effective density can be efficiently calculated by multiplying the fast Fourier transforms (FFTs) of the filter function and local density of the wafer.

2.2 Step Height Density Model

The Step Height Density Model was orignally developed by Smith et al. [11] to model oxide dielectric CMP for metal interconnects. It was later extended by Tugbawa et al. [12] to model dual material damascene CMP processes. In this section, we will explain how the model works in both cases.

2.2.1 Single Material Polish

Although the pattern density model encompasses long range bending of the polishing pad over the planarization length, it assumes that the "down areas" are not polished until the local step height is reduced to zero. The step height density model incorporates the idea of local pad bending, where the pad can compress and bend around local features, as originally described by Grillaert et al. [13]. Large step heights hold the pad up, resulting in no down area polishing. However, when the step height reaches or falls below the contact height h_c, both the up and down areas will be simultaneously polished. The removal rate depends directly on the step height and contact height, as seen in Figure 2. When above the contact height (Phase I), the die polishes as in the pattern density model, where only raised features polish. At or below the contact height, both up and down areas polish (Phase II). Because more material contacts the pad, the removal rate changes as the pad pressure is apportioned between up and down areas. When the step height dependence is finally removed by polishing, the whole die (both up and down areas) are polished at the blanket wafer removal rate.

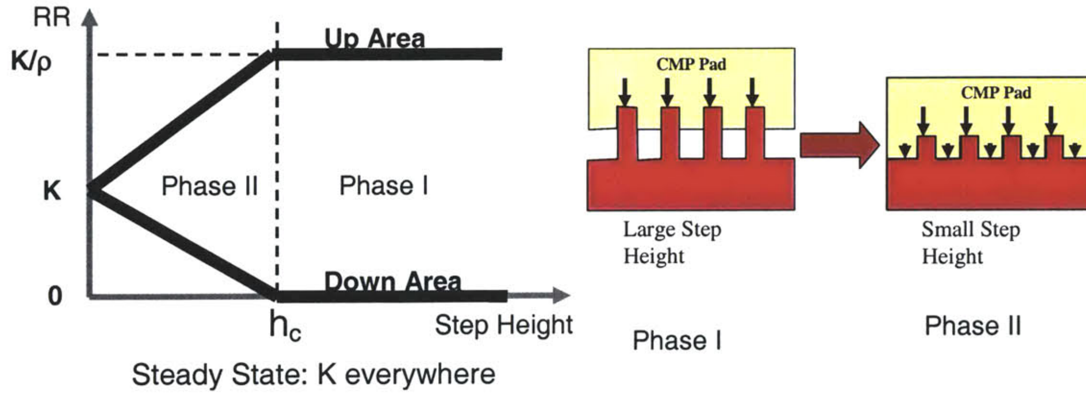


Figure 2-3: The removal rate dependence on step height proposed by Smith [11].

A derivation of the analytical formulas for the material removed in both Phase I and Phase II of the step height density model can be found in Lee [14 his thesis]. The amount of material removed in the "up" and "down" regions is given as follows:

$$AR_u = \begin{cases} tK/\rho & t \le t_c \\ t_c \dfrac{K}{\rho} + K(t-t_c) + (1-\rho)\dfrac{h_c}{\tau}\left(1-e^{-(t-t_c)/\tau}\right) & t > t_c \end{cases} \quad (3)$$

$$AR_d = \begin{cases} 0 & t \le t_c \\ K(t-t_c) - \rho\dfrac{h_c}{\tau}\left(1-e^{-(t-t_c)/\tau}\right) & t > t_c \end{cases} \quad (4)$$

The term K represents the blanket removal rate, t_c is the "contact time," and h_c is the "contact height," the time and step height when the pad first touches the down areas. The effective density is represented by ρ, and τ is the exponential time constant.

2.2.2 Dual Damascene Polish

The extension of the step height density model to dual damascene polishing was first demonstrated to model CMP for copper interconnects [12 ECS99], and then adapted to Shallow Trench Isolation CMP, where the two materials polished are oxide and nitride.

Shallow trench isolation inlays oxide into trenches between nitride coated active areas. The oxide overburden is polished back until the oxide remains only in recessed trenches. Polishing is spilt into Stage I and Stage II. When the pad only contacts the

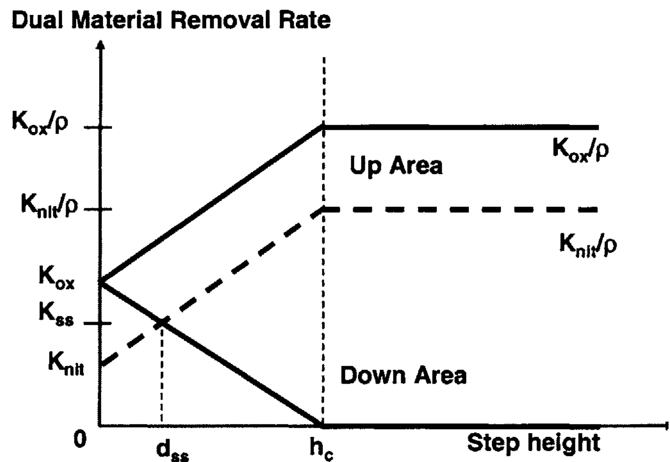


Figure 2-4: Dual material removal rate curve.

oxide overburden, the polish happens just like the single material case (Stage I). The idea of a contact height and the way material polishes during both Phase I and Phase II remain unchanged, as seen in Figure 2-4. However, the introduction of the extra material adds a level of complexity to the model. Both the oxide and nitride have different blanket removal rates. The ratio of the blanket removal rates, K_{ox}:K_{nit}, is defined as the selectivity, s. Polishing the two materials (Stage II) simultaneously will introduce a local step height, even when the starting surface is entirely flat. This step height is defined as dishing d_p, as explained in Chapter 1. As the dishing increases, the pad will begin to exert less pressure on the down areas in the trench. This leads to greater up area polish and lower down area polish. Eventually, the dishing will reach a value, d_{ss}, where the up and down area removal rates will be equal. This condition is known as steady-state dishing. Eventually, all the oxide is cleared off the "up" areas and all the nitride gets exposed. The time at whichoxide clearing occurs and nitride is first exposed is defined as the "touch down time" t_n, and the step height at this time is defined as h_n. However, oxide clearing occurs at different times on different parts of the wafer. The wafer is polished extra

amounts of time to ensure all of the oxide overburden has been removed. This over-polish leads to erosion of the nitride in some of the up areas, as defined in Chapter 1. The equations for the amount of material removed in the up and down regions, as well as the dishing and erosion during Stage II are given as follows:

$$AR_u = z_0 + K_{ss}(t - t_n) + \left(\frac{h_n - d_{ss}}{1 + \frac{s\rho}{1-\rho}} \right) \left(1 - e^{-(t-t_n)/\tau_{nit}}\right) \tag{5}$$

$$AR_d = z_0 - z_1 + h_n + K_{ss}(t - t_n) - \left(\frac{h_n - d_{ss}}{1 + \frac{1-\rho}{s\rho}} \right) \left(1 - e^{-(t-t_n)/\tau_{nit}}\right) \tag{6}$$

$$D(t) = (h_n - d_{ss})e^{-(t-t_n)/\tau_{nit}} + d_{ss} \tag{7}$$

$$E(t) = K_{ss}(t - t_n) + \left(\frac{(h_n - d_{ss})(1-\rho)}{1 + \rho(s-1)} \right) \left(1 - e^{-(t-t_n)/\tau_{nit}}\right) \tag{8}$$

The term τ_{nit} is the nitride time constant, and AR_u and AR_d are the amounts of material removed in the up and down regions respectively. The terms *D(t)* and *E(t)* give the equations for dishing and erosion as a function of time. A full derivation of the model is documented by Lee [14].

2.3 Updated Step Height Density Model

First described by Xie et al. [15,16], the updated step height density model reexamines the relation between the removal rate and the pad pressure and compares the results with the contact wear model. Proposed by Chekina [17] and Yoshida [18], the contact wear model uses pad displacement to map out local pressures on the wafer surface. By assuming a polishing rate linearly proportional to pressure, the local pressure

map defines local removal rates. As the film surface evolves through time, the pad displacement is changed, and thus local pressures and removal rates are modified.

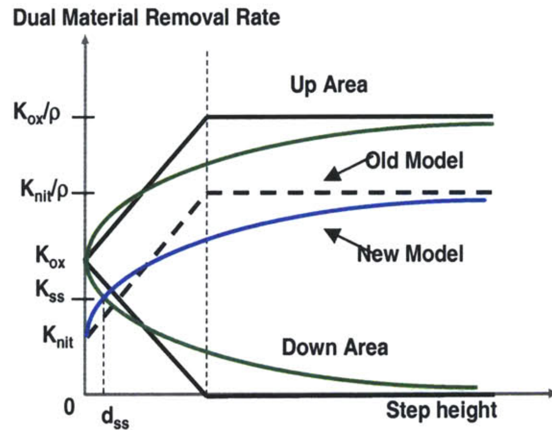


Figure 2-5: Removal rate diagram for the updated step height density model.

While the contact wear and step height density models followed the same trend, Xie discovered that the contact wear model suggests a removal rate curve like that shown in Figure 2-5. Rather than having a distinct contact height, the updated step height density model utilizes a continuous function to explain the dependence of removal rate upon step height. This model improvement also simplifies the calculation of material removed because the removal rate function is no longer discontinuous.

2.4 Adaptation of Model to Polysilicon MEMS Polishing

Our particular application of CMP models deals with the polishing of polysilicon. During single material polish, only polysilicon is being modeled, while dual material polish examines polysilicon and nitride film stacks. While examining this polishing process, we adapt the updated step height density model for the STI case.

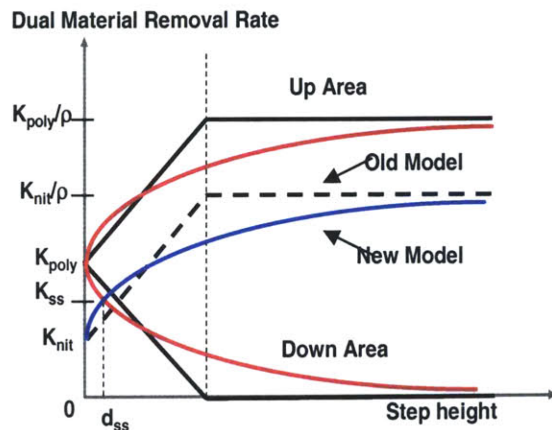


Figure 2-6: Removal rate diagram for the updated step height density model with a polysilicon/nitiride film stack.

The oxide is replaced by polysilicon. The removal rate curve for our polysilicon adaptation can be seen in Figure 2-6.

To analytically find an equation for the amount of material removed, we first examine the removal rate diagram. We fit the down area removal rate to a decaying exponential:

$$RR_d = K_{poly} e^{-\alpha\rho h} \tag{9}$$

The term K_{poly} is the polysilicon blanket removal rate, ρ represents the effective pattern density, h is the step height, and α represents a fitting term for exponential decay. With this equation in hand, we can solve for the amount of material removed in the down area:

$$AR_d = \frac{1}{\alpha}\log\left[1 + e^{-\alpha\rho h_0}(e^{\alpha K_{poly} t} - 1)\right] \tag{10}$$

Here, the term h_0 represents the initial step height and t represents the time of the polish. The formula for the amount of material removed in the up areas can be solved in the same way, resulting in:

$$AR_u = \frac{K_{poly}}{\rho} t - \frac{1-\rho}{\rho} AR_d \tag{11}$$

For dual damascene procedures, we determine the removal rate equations for the nitride. Again, we see the nitride curve has the same shape as the polysilicon curve. However, the intersection of the nitride removal rate curve and the polysilicon down area curve forms the point (d_{ss}, K_{ss}). To determine this point, we must use the removal rate equation for the nitride up areas:

$$RR_{up} = \frac{K_{nit}}{\rho} - \frac{(1-\rho)}{\rho} K_{nit} e^{-\alpha\rho h} \tag{12}$$

Using these two removal rate functions, we can find the total amount of material removed in the up and down areas when the polish reaches Stage II, as well as equations for dishing and erosion:

$$\beta = 1 + (s-1)\rho \tag{13}$$

$$AR_d = z_0 - z_1 + h_n + \frac{s\rho}{\alpha\beta}\log\left[1 - \beta e^{\alpha h_n} + \beta e^{\alpha\left(h_n + \frac{K_{nit}(t-t_n)}{\rho}\right)}\right] \tag{14}$$

$$AR_u = z_0 + \frac{K_{nit}}{\rho}(t-t_n) - \left(\frac{1-\rho}{s\rho}\right)\frac{s\rho}{\alpha\beta}\log\left[1 - \beta e^{\alpha h_n} + \beta e^{\alpha\left(h_n + \frac{K_{nit}(t-t_n)}{\rho}\right)}\right] \tag{15}$$

$$D(t) = z_1 + AR_d - AR_u \tag{16}$$

$$E(t) = AR_u - z_0 \tag{17}$$

All the terms in the above equations stand for the same things as they did previously in the chapter. The term, β, is used to simplify the equations.

2.5 Chapter Summary

In this chapter, we have examined the different models developed at MIT to model the CMP process. We will use the models to characterize our MEMS CMP experiments, and explain how the models reflect the results we see. Also, we will discuss whether other effects play a role in MEMS CMP and would require modifications to the current models.

Chapter 3

Preliminary MEMS CMP Experiment

This chapter presents the results of a preliminary polysilicon MEMS CMP experiment [19]. A MEMS test mask was used to examine the polishing of a single patterned polysilicon layer. MIT-developed CMP models were used to characterize the polishing process. Results of the preliminary experiment as well as implications for future MEMS CMP are discussed.

3.1 CMP Characterization Test Mask

The test mask, shown in Figure 3-1, is designed with MEMS feature scales in mind. The die is replicated across the entire wafer, creating a periodic surface layout. Each die

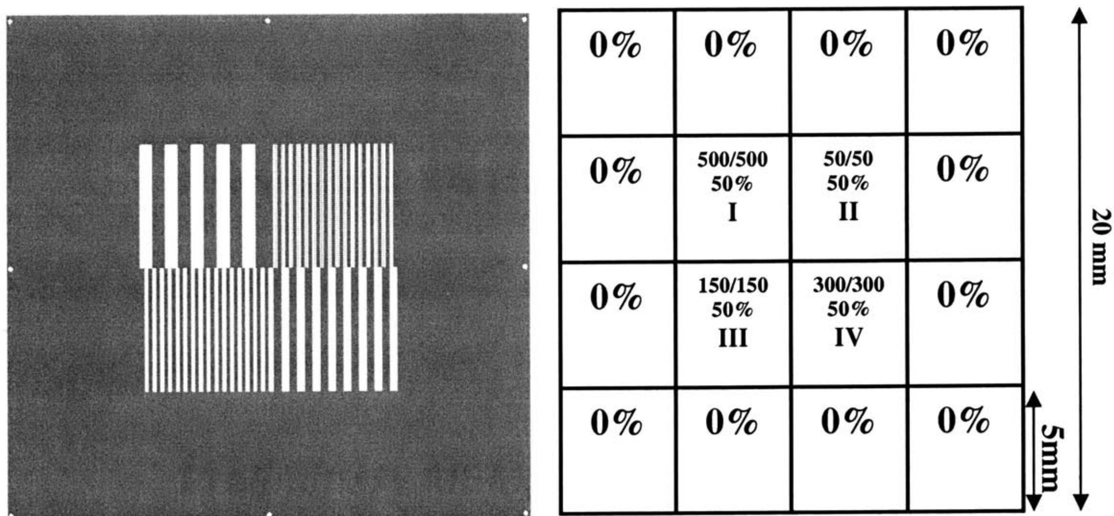


Figure 3-1: The test die (left) and layout (right). Layout blocks indicate line width/space in microns, as well as layout pattern density (in %).

contains four arrays of lines with a layout pattern density of 50%. Thus, the line width and line spacing is equal in these regions. The line width and space for the regions are 500, 50, 150, and 300 μm respectively in Arrays I, II, III, and IV. These arrays are extruded upward from the wafer surface. Surrounding the four line arrays are empty field regions with density of 0%. These "down" areas make up a large percentage of the die area; thus, the test mask features may interact with the polishing pad in new ways.

3.2 Process Flow and Measurement Strategy

The experiment calls for test wafers to be created with a desired wafer topography and surface films. This section will explain how the wafers were prepared and polished for the experiment. It will also outline the measurement strategy used on both pre- and post-polished wafers.

Process Flow and Experiment Parameters

The first step to creating the 6 inch p-type test wafers involves photolithography with the test mask. For our experiment, we used image reversal resist to protect the opposite areas of the die. Dark areas in the mask picture in Figure 3-1 are exposed, while the white areas are protected from exposure. After lithography, we used an Applied Materials P5000 plasma etcher and SF_6 chemistry to etch half a micron down from the wafer surface. After the etching was completed, we grew a thin thermal oxide layer measuring 50 nm. This oxide is used to separate the structural polysilicon from the bulk silicon substrate. The interface gives a good barrier for film thickness measurements. After the oxide growth, we deposited 1.0 μm of

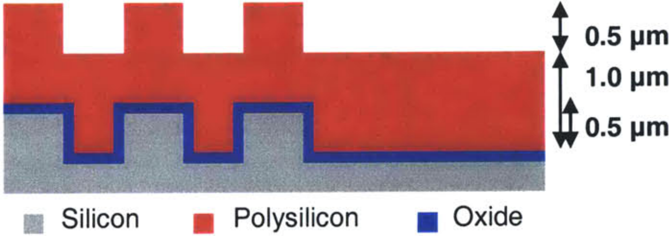


Figure 3-2: Schematic wafer cross-section details the film.

polysilicon at 625°C. We are interested in examining how the polysilicon layer polishes. A schematic cross section of the wafer can be viewed in Figure 3-2.

We polished 5 wafers at 10, 20, 30, 40, and 50 seconds, respectively. Polishing was carried out with a Strasbaugh 6EC Chemical Mechanical Polisher. We set the down force to 68.95 kPa (10 psi) and the back pressure to 55.16 kPa (8 psi). The table speed is set to 28 rpm, and head speed to 20 rpm. The Semisphere SS-25 silica slurry is introduced at a rate of 200 mL/min. A Tencor UV1280 tool is used for optical film thickness measurements.

Measurement Strategy

Measurement points are taken along a central scan through the middle of each array (y = 7.5 mm and 12.5 mm). The points are chosen to replicate a 1-dimensional system and help us evaluate how the different line width and space arrays affect the polishing in a 50% density region. Measurement locations are indicated on Figure 3-3. All up measurement sites are in the central scan regions of Arrays I through IV. The down area

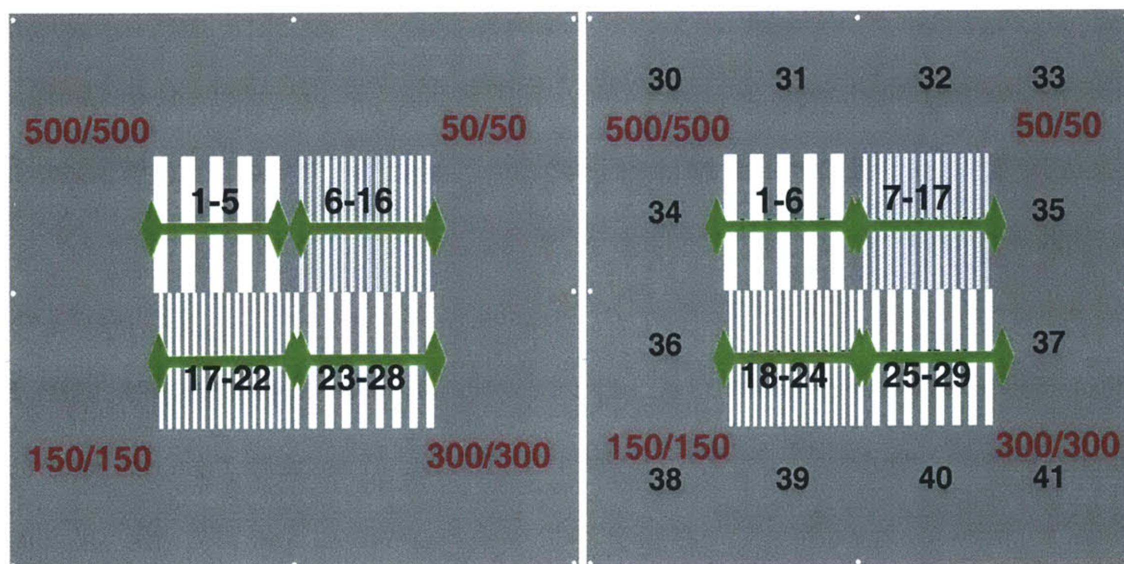


Figure 3-3: Measurement sites: up locations (left) and down locations (right).

measurement sites 1-29 also straddle the central scans in Arrays I through IV. However, down sites 30-41 are spread out among the down field regions surrounding the central array of extruded lines. We believe the field points to be outside the planarization length of the array features, and give a good indication of blanket removal for our CMP process. Measurements were taken on the die closest to the center of the wafer in order to minimize edge effects.

3.3 Results and Implications

Using the data collected from our measurements, the updated step height density model estimates how the topography of the die will change through each time step. We find that the model loses accuracy when trying to fit the larger features.

Model Fit

The updated step height density model extracts a blanket removal rate of 2826.3 Å/min, and a planarization length of 3.20 mm. The root mean square error between the model fit and measured data is 254.8 Å. The measurement and model predictions for remaining film thickness are shown in Figure 3-4. The data and model fit points are

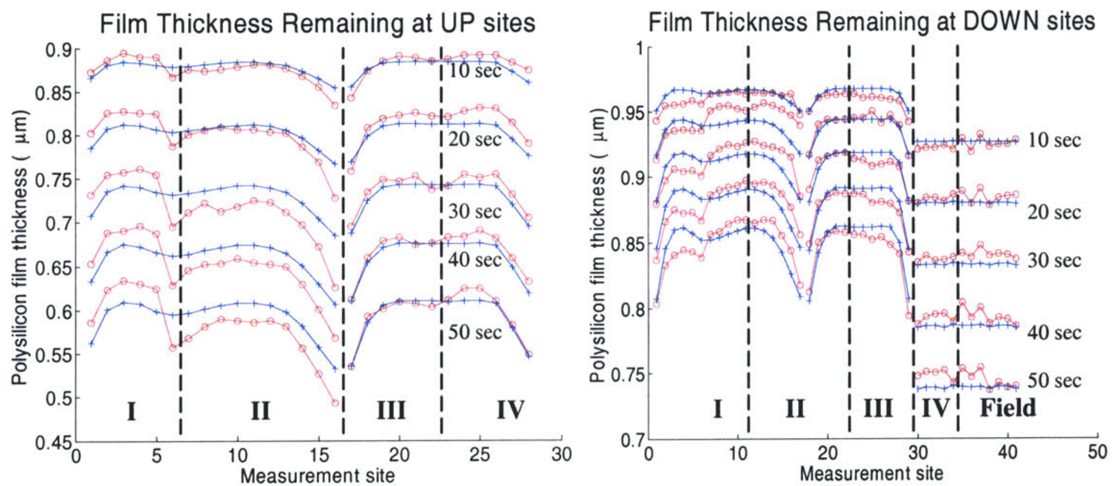


Figure 3-4: Predicted (+) and measured (o) thicknesses of film remaining.

broken up according to the array or field region the measurement originates from. Data from all time slices are aggregated together in order to view the evolution of the film thickness during the polish process.

From the measurements shown in Figure 3-4, we see that the model fits the data quite well. It is able to capture the trends of how polishing affects the remaining polysilicon film within each array. The model captures the extra material removed at the edges of the array, where the extruded features interact with the large down area field regions.

While the model captures the overall trends very well, it has difficulty correctly modeling the some of the large features in Array I. While both Array I and Array II have the same local density (50%), the amount of material removed from the up area of Array I is less than the amount removed from the up area of Array II. Conversely, we find more material being removed from the down regions of Array I than from the down regions of Array II. The model ends up finding a tradeoff between Array I and II measurement, ending with a predicted remaining film midway between the measured results of the two regions. This slight discrepancy between the model prediction and measurement data in Array I points out a place where the model might be able to be updated and fine tuned.

Die Topography Estimation

Using the extracted model parameters, we simulate the remaining film thickness for all points on the die. Using the initial conditions of film thickness and step height, we examine what the overall die topography will look like at each time step. In Figure 3-5, we show the predicted topography of the die after each polishing time step. As expected by the updated step height density model, the corners of the raised blocks polish more rapidly than the center. A slight depression near the upper middle part of the die is also

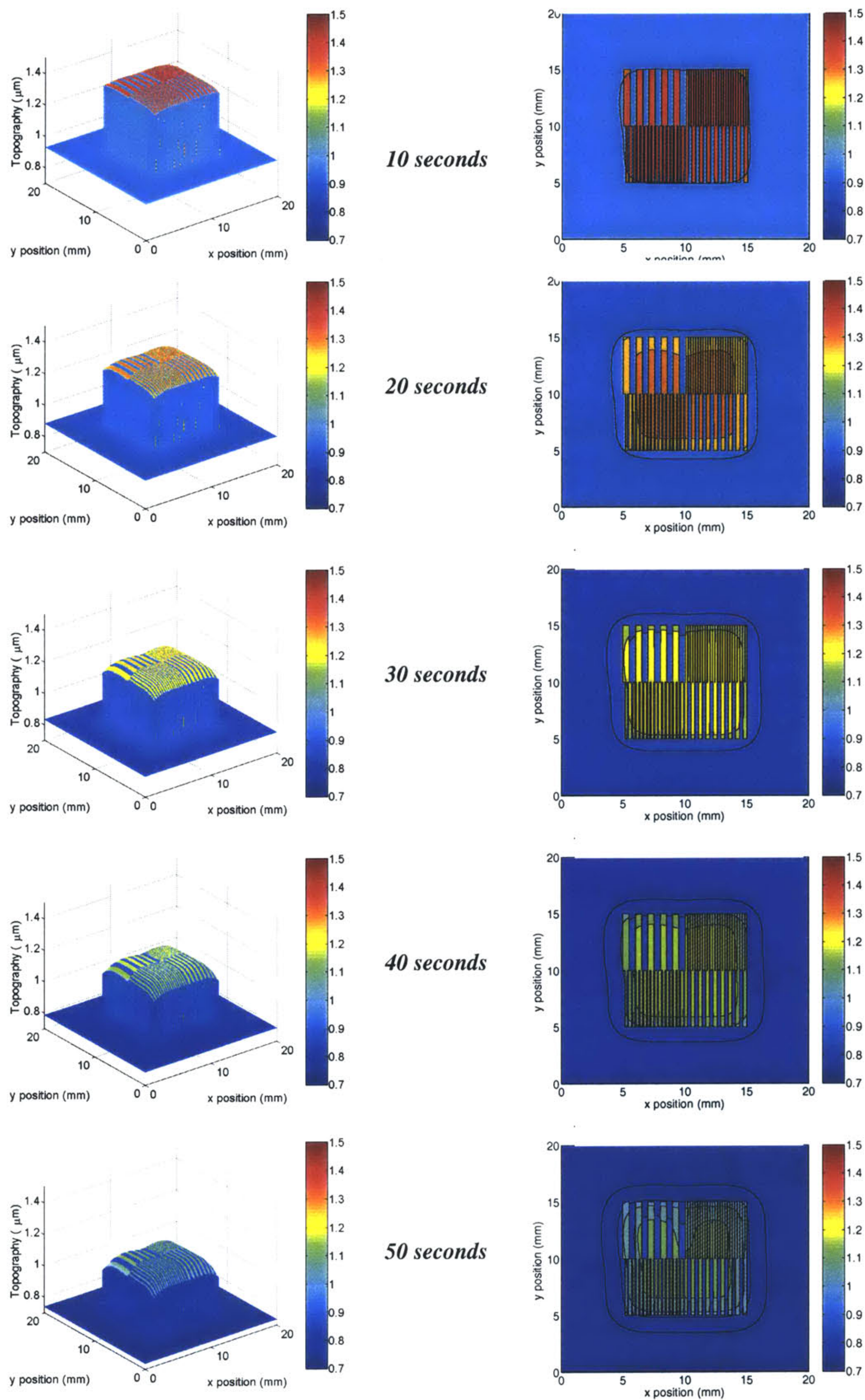


Figure 3-5: Die topography at 10 second intervals. 3D mesh plots at left, and contour plots at right.

captured by the model.

The contour plots show how polishing evolves in both the up and down areas. Even though Arrays II and III do not appear clearly in the contours, the contour plots still highlight the extreme corner rounding for the four arrays of extruded structures.

3.4 Experiment Implications

In general, the model fits the data well. It captures the general trends and follows the actual measurements for film thicknesses within each array. However, as mentioned previously in Chapter 3.3.1, the model has some limitations when predicting film thicknesses for the large features in Array I. We believe this discrepancy occurs due to pad bending across the size of the features in question. Because the step height is still quite large, the pad can bend down and polish more of the down area of Array I. More pressure is distributed down into the trenches of the down area. Conversely, the up areas

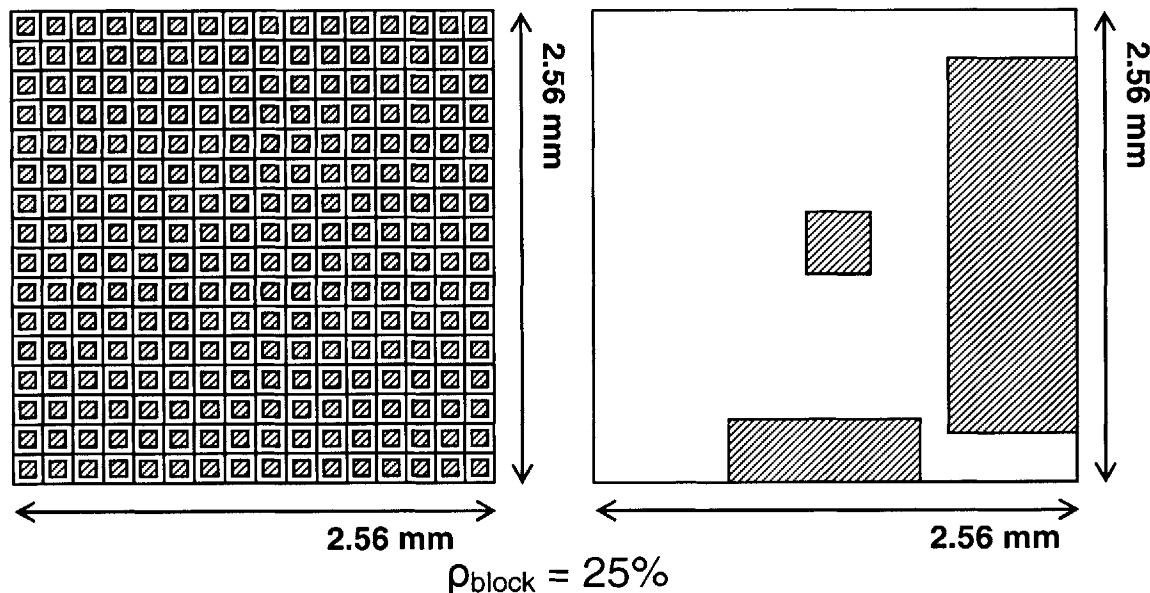


Figure 3-6: The two blocks near the centers of these regions see the same net surrounding pattern density, but a much different configuration of the patterns. The configuration on the right allows the pad to bend and contact the down areas, while the configuration on the left will more effectively hold the pad up out of contact with the down areas.

of Array I are polished less than expected.

When the die features approach the same order of magnitude as the planarization length (0.5 mm in Array I compared to 3.20 mm planarization length), the pattern density effect and the step height removal rate function become intertwined. The pattern density effect no longer averages together the densities of a large number of surrounding features. Instead, it is incorporating a small number of large features. Large feature areas might have appreciable down area polish because the features are spaced so far apart that the pad can bend down, even when the pattern density is the same as small feature areas, as demonstrated in Figure 3-6. The configurations of the features around the central points of the two blocks are very different. The different configuration of density (grouping into large features) on the scale of the planarization length causes different polishing. This suggests future model enhancements that take into account the large size of the features or the open spaces.

Xie [16] demonstrated how line space creates a second order effect in the application of the updated step height density model to shallow trench isolation. Line space was found to be inversely proportional to the exponential decay for the removal rate equation. The large features typical of MEMS CMP create the opportunity for designs with large, open line spaces. Line space dependence provides a natural location to examine the current model, and suggest future model enhancements for polysilicon MEMS CMP.

3.5 Chapter Summary

We have presented the findings of a preliminary polysilicon MEMS CMP experiment. The updated step height density model does a good job tracking the trends of MEMS CMP, but the study raised some model shortcomings. With the knowledge and

experience from this preliminary experiment, we have identified several layout features to incorporate and study in future experiments.

Chapter 4

New MEMS Mask for CMP Characterization

While the preliminary experiment discussed in Chapter 3 serves a good starting point, the mask used does not adequately provide a wide range of test structures needed to characterize MEMS CMP. A new mask specifically designed to characterize MEMS CMP is presented here, along with an explanation of the different test dies and test structures.

4.1 MEMS Mask Overview

The biggest difference between the new MEMS mask and other integrated circuit CMP test masks is the feature sizes of the test structures. Our MEMS mask contains large features on all test dies. Because it is designed for a 6 inch process, the contact mask measures 7 inches across on each side. While all test dies are transferred to the wafer, a number of fill or "dummy" structures surrounding the test dies will only be partially transferred: some dummy dies have only half their patterns transferred, while the other half will be outside the boundary of the wafer. While CMP engineers usually use stepper masks for integrated circuit testing, the new MEMS mask is a contact mask containing the whole wafer map. Unlike the shrinking exhibited by stepper mask systems, a contact mask has no optical shrinking of the mask's features. A scaled down version of the mask is seen in Figure 4-1. The large mask size makes discerning the difference between some

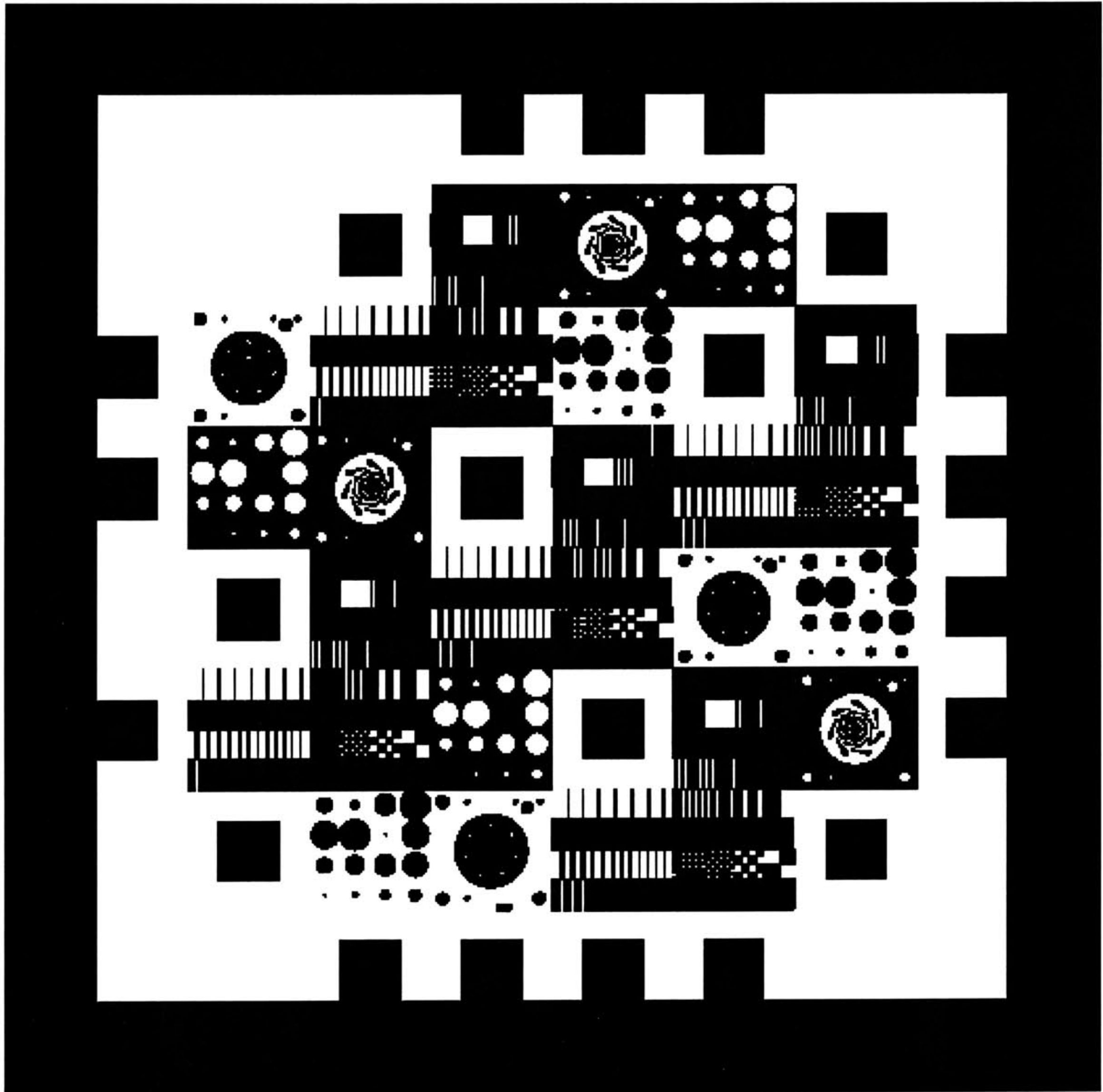


Figure 4-1: MEMS mask for CMP characterization.

of the dies hard. A large number of die look like a black block surrounded equally on all sides by a white moat. At great magnification, however, we will see that these two dies are actually quite different. Figure 4-2 gives the placement of the test dies on the wafer, while Table 1 explains the abbreviations used in Figure 4-2. Each die is represented in the format of *X* or *#X*, where *X* are letters, and *#X* is a number followed by letters. All #s are between 1 and 32. The numbers tells the position of the test die on the wafer. Each letter stands for the type of test die, as mentioned in Table 1. Therefore, if the designation *#X* =

			Y	Y	Y		
		1F	2D	3EP	4H	Y	
Y	5EN	6L	7Q	8P	9F	10D	Y
Y	11H	12EP	13F	14D	15L	16Q	Y
	17F	18D	19L	20Q	21EN	22P	Y
Y	23L	24Q	25H	26F	27D	28EP	Y
	Y	29P	30ENn	31L	32Q	Y	
		Y	Y	Y	Y		

Figure 4-2: Placement of the test dies on the MEMS mask.

14D means we are referring to the Density die in wafer position 14. Spaces in Figure 4-2 with neither letters nor numbers are empty and void of features.

Some of the test die are used mainly for calibration and verification purposes, while the rest of the die are actual MEMS structures. The Density, Lines, Filter, and Square dies are designed like previous CMP test structures. They all contain lines or squares, conforming to design rules from integrated circuits. All structures are distilled into minimum square features; thus, these test die contain only right angle features.

The other test dies, Holes, Pillars, Engine Negative, and Engine Positive more accurately reflect real MEMS devices. The holes and pillars replicate structures used to increase catalytic surface area for chemical and power MEMS devices. The Engine Negative and Engine Positive dies are borrowed from the MIT Microengine projects mentioned in Chapter 1, and in particular positive and negative versions of the turbo-pump layer. The additional die, Engine Negative name, ENn, is in only one position on the die. This device is different from Engine Negative, because it contains the mask design copyright information.

Table 1. Mapping of die letter to die name.

LETTER	DIE NAME
D	Density
L	Line
Q	Square
F	Filter
H	Hole
P	Pillar
EN	Engine Negative
EP	Engine Positive
ENn	Engine Negative with Name
Y	Dummy

These device dies are much different than typical CMP test dies because they include curves. The Hole and Pillar die contain circles of various diameters. The engine dies have not just circles, but irregularly shaped compressor blades. These dies were included in the MEMS mask to see how CMP works on real devices, not just on regular arrays of right angle shapes. These device help differentiate the MEMS test mask from conventional integrated circuit test masks. All dies, both regular test and device, measure 20 mm by 20 mm and will be described in depth in the following sections of this chapter.

4.2 D: Density Test Die

The Density test die contains features that vary the pattern density across the die. All structures are vertical lines with a length of 5 mm. The test die itself is broken into 16

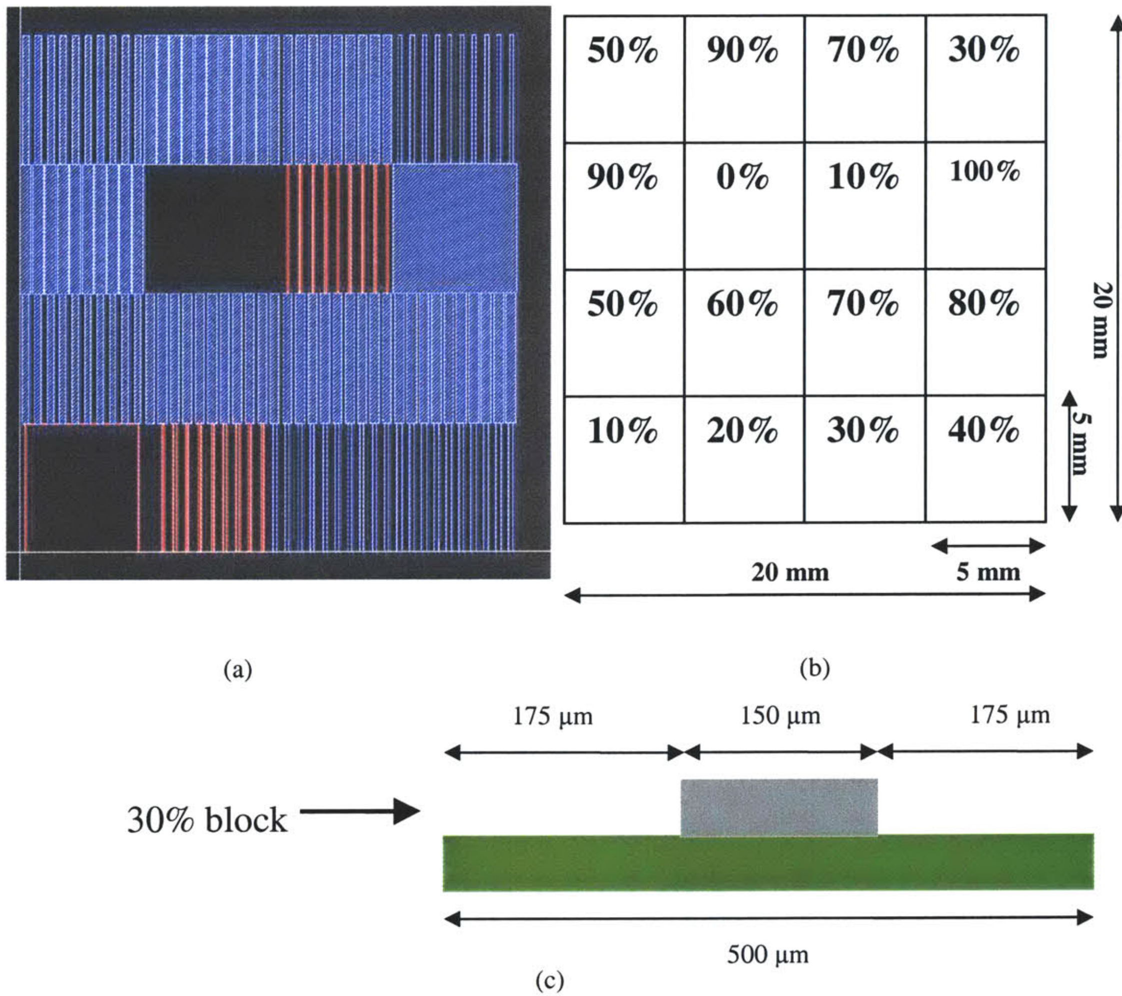


Figure 4-3: Description of the Density die. A picture of the die layout (a) and the die schematic (b). For a given block density of 30%, the structure and dimensions of a group within the block is shown (c).

blocks measuring 5 mm by 5 mm, and each block is again broken into groups of 500 μm by 5 mm. Each group has one line centered to the middle of the group, and the group is repeated 10 times to fill a block. The line inside a grouping can measure 0, 50, 100, 150, 200, 250, 300, 350, 400, 450, or 500 μm, corresponding to a bock density of 0%, 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, or 100%. A block with 100% pattern density has no down areas, only up areas. Measurements in this block only have meaning as up area, and no meaning for down area. Just the opposite of the 100% block, up area measurements in the 0% pattern density region have no meaning because there are no up

area features. A picture of the Density die as well as a schematic can be viewed in Figure 4-3.

4.3 L: Lines Test Die

The Lines test die examines polish dependencies upon line width and line space. This die is split into four rows, where each row is 5 mm in length. The top row has a fixed line space of 2500 μm. In between each space is a line of width (from left to right) 50 μm, 100 μm, 150 μm, 200 μm, 250 μm, 300 μm, and 350 μm. Due to restrictions on the size of the entire structure, the last line space on the right border of the die is only 1400 μm in size. The second row from the top is the exact negative of the top row. Here, the line width is fixed to 2500 μm while the line space varies.

The bottom two rows are set up just like the top two rows. In the third row from the top, the line space is fixed to 1250 μm. Line widths are (from left to right) 625 μm, 500 μm, 450 μm, 400 μm, 350 μm, 300 μm, 250 μm, 200 μm, 150 μm, 125 μm, 100 μm, and 50 μm. The last line space in this row is 1500 μm in size. The bottom row mirrors the row directly above it; for this row, the line widths are fixed to 625 μm, and all the line spaces vary according to the row above it. The layout of the die can be viewed in Figure 4-4.

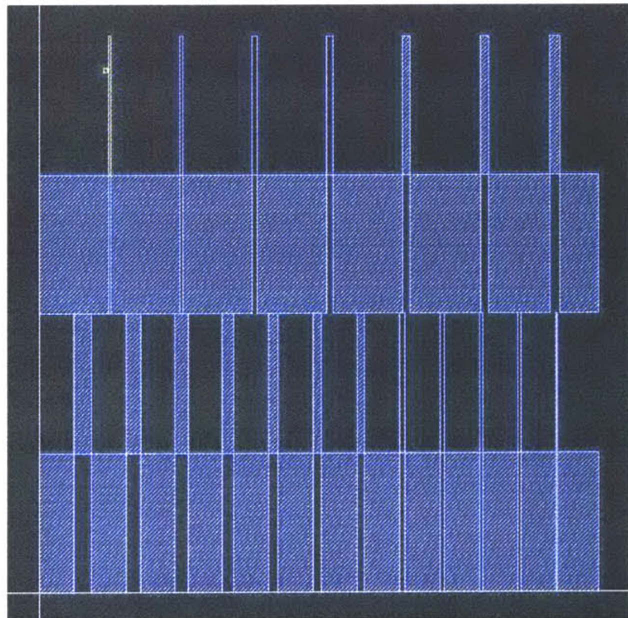


Figure 4-4: Picture of the Lines test die.

The Lines die examines polishing of a single isolated structure. This die was inspired by MEMS side-by-side flow channels formed by polysilicon damascene CMP [20]. The end product in that work consists of a hollow nitride cantilever, with two channels in the cantilever separated by a thin wall of nitride. The isolated line widths of the top and third from top rows replicate the thin middle wall.

4.4 F: Filter Test Die

The Filter test die examines the planarization length of a polishing process. The die consists of a 10 mm by 10 mm raised region centered in the 20 mm by 20 mm die. During polishing, the step of the raised area will be smoothed away. Profilometry of the die can provide a direct measurement of the planarization length. These measurements examine the changes to the planarization length over the course of an experiment. A picture of the Filter test die can be viewed in Figure 4-5.

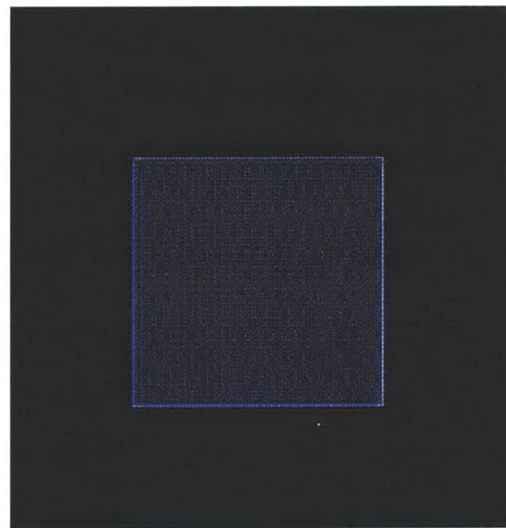


Figure 4-5: Picture of the Filter test die.

4.5 Q: Square Test Die

Like the Density test die, the Square test die (Q) has 16 different blocks. However, the grouping in each of the blocks is different. All blocks have a pattern density of 50%; the difference between blocks lies in the way the density is distributed. The top two rows of the die contain 5 mm long lines with varying widths. The bottom two rows contain squares in a checkerboard pattern, where the width of the square varies. The feature sizes

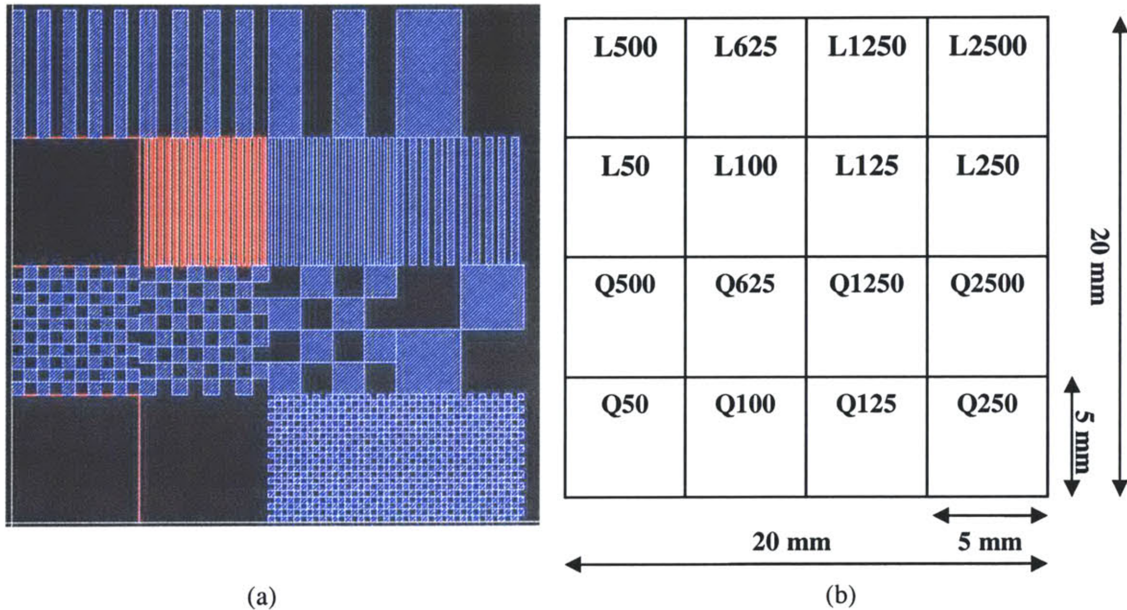


Figure 4-6: Picture (a) and schematic (b) of the Square test die. On the schematic, *L#* represents a block of consisting of lines with line width #. The *Q#* blocks represent blocks made of squares with square width #.

of interest, line width and square width are the same for both groupings. The critical sizes are 50 μm, 100 μm, 125 μm, 250 μm, 500 μm, 625 μm, 1250 μm, and 2500 μm. A picture and graphical schematic of this die can be seen in Figure 4-6.

4.6 H: Holes Test Die

The Holes test die simulates inlaid material in the form of vertical columns. The basis behind examining vertical columns comes from chemical reactor MEMS. Engineers design pillars into reaction chambers to provide extra surface area for catalysts.

This test die is split into 16 different blocks, where each block contains one hole of varying diameter. The hole diameters measure 500 μm, 100 μm, 1500 μm, 2000 μm, 2500 μm, 3000 μm, 3500 μm, 4000 μm, 4500 μm, and 5000 μm. A picture and schematic of this die can be seen in Figure 4-7.

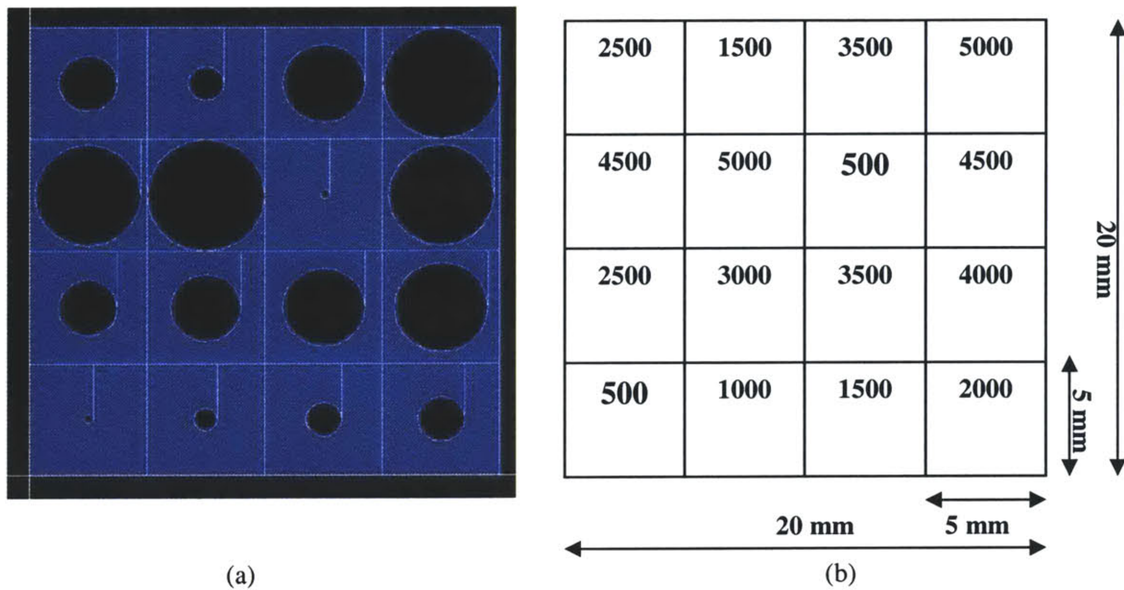


Figure 4-7: Picture (a) and schematic (b) of the Holes test die.

4.7 P: Pillars Test Die

The Pillars test die is the negative image of the Holes test die. All blocks of this die have the same diameters as the Holes die; the only difference for the Pillars die is that the round cylinders are extruded out of the wafer surface before polishing. A picture of the die can be seen in Figure 4-8.

4.8 EP and EN: MicroEngine Test Die

The Engine Positive, Engine Negative, and Engine Negative name test die are borrowed directly from the MIT Microengine program mentioned in Chapter 1. The goal of that project is to design and build a micro-fabricated turbo-engine. One of the seven layers in the device, the

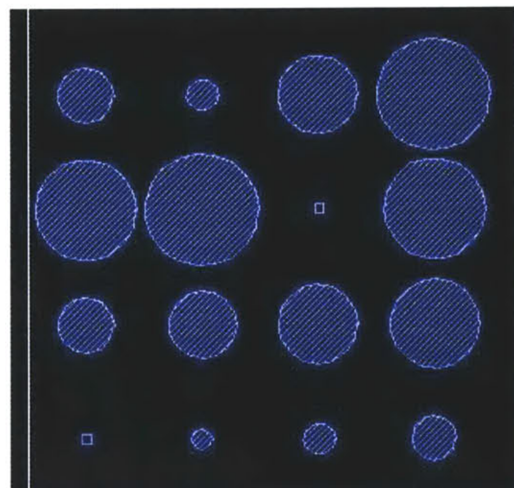


Figure 4-8: Picture of the Pillars test die. This die shares the same schematic as the Holes die.

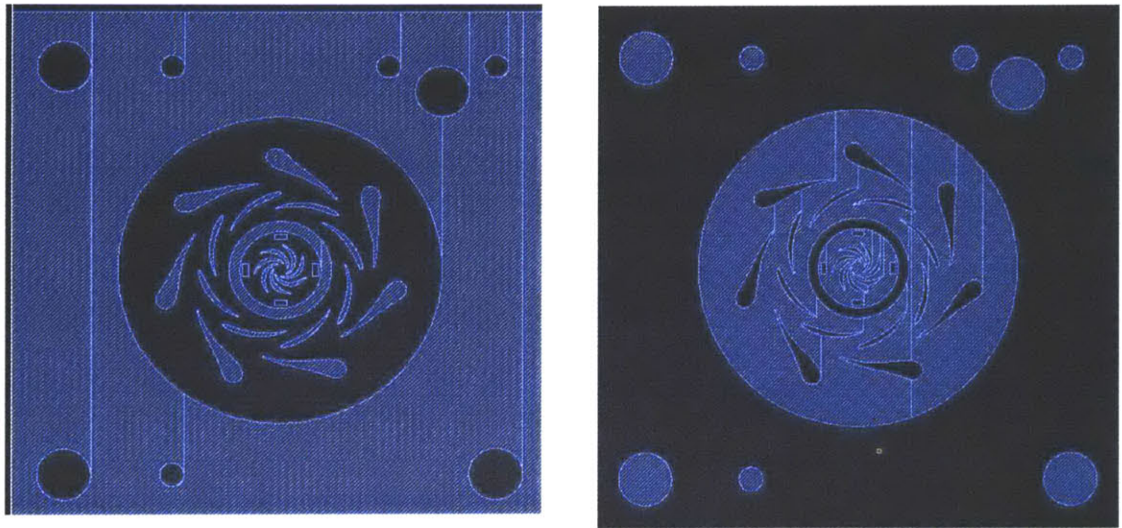


Figure 4-9: The Engine Positive (left) and Engine Negative (right) test dies.

turbopump, is used for the test die. This die is placed on the mask to examine how CMP can affect real MEMS devices. For the positive design, the turbopump blades become extruded, while the areas around the blades are the inlaid material. For the negative test die, material is inlayed into the pump blades, while the regions surround the blades themselves extrude upward before polishing. The Engine Negative name (ENn) test die differs from the Engine Negative die only in the placement of the mask author's name and the MIT copyright on the bottom edge of the test die.

An important feature of the Microengine test die lies within the interesting curved shapes. Unlike regular squares and rectangles, this die contains mostly curved and circular shapes. These acute angles and nonstandard shapes provide an opportunity to examine and study how the polishing process works on new and differently shaped features. Pictures of the different engine test die can be seen in Figure 4-9.

4.9 Y: Dummy Test Die

The Dummy Test die is placed around the edges on the wafer map to ameliorate wafer edge effects and control the way the slurry flows past the edge of the wafer and to

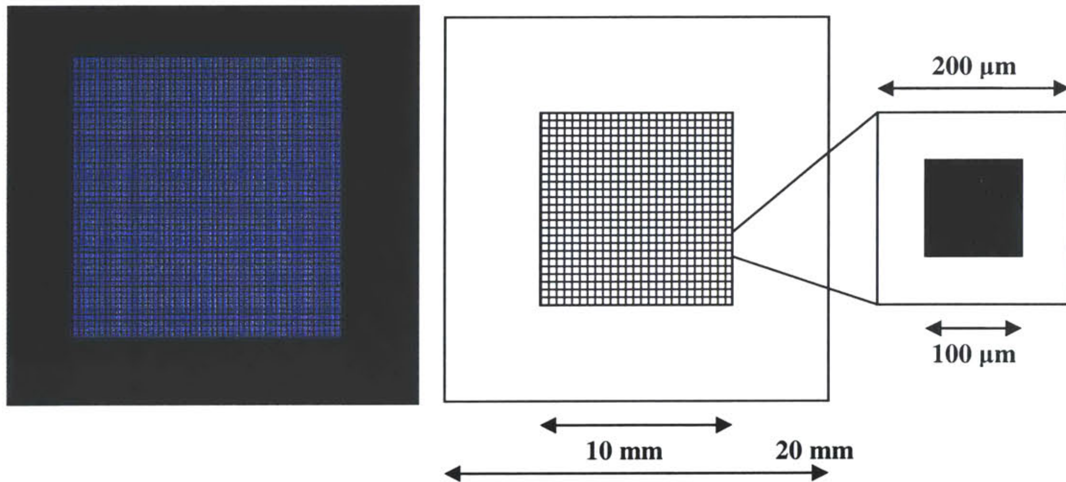


Figure 4-10: Picture (left) of the Dummy die, and its schematic (right). The schematic includes an expanded view of one of the 25% pattern density subunits that make up the central block of the Dummy die.

the actual test structures. Dummy dies around test dies 1F and 17F have been purposely omitted in order to allow experimenters to examine edge effects and how dummy test die affect the polish on different parts of the wafer.

The Dummy test die has all of its features enclosed within a 10 mm by 10 mm area in the center of the die. The pattern density of this middle block is 25%. The middle block itself is made up of 2500 subunits of size 200 µm by 200 µm; each of these subunits also has a pattern density of 25%. Each subunit has a solid 100 µm by 100 µm feature centered in its middle. A picture of the Dummy die and a schematic of its subunits are in Figure 4-10.

4.10 Chapter Summary

In this chapter, we have presented and described a new MEMS CMP characterization test mask. The mask contains a number of different test die, all of which are also described in this chapter. In the next chapter, we will discuss an experiment and results from using the new MEMS test mask.

Chapter 5

New MEMS Mask Experiment and Results

This chapter presents the experiments and results obtained for polysilicon MEMS CMP using the newly created MEMS test mask. The aim of this experiment is to examine polysilicon MEMS CMP in a damascene procedure, where the polysilicon becomes inlaid within another material. Unlike the preliminary experiment from Chapter 3, our new tests will involve dual material polishing of polysilicon and silicon rich silicon nitride. After running our experiment, we apply the MIT-developed CMP models to characterize and understand the process. The results of the experiments demonstrate the applicability of integrated circuit CMP models to characterize CMP for MEMS. We show that the CMP models can be used to help predict die topography, then qualitatively look at how polishing alters the surface of the wafers.

5.1 Process Flow and Measurement Strategy

This section describes the process flow used to create out test wafers. It also outlines the metrology tools and measurement strategies used to gather data about polysilicon MEMS polishing.

5.1.1 Process Flow and Experiment Parameters

Like the preliminary experiment discussed in Chapter 3, our process flow again begins with lithography. In this experiment, however, our 6 inch wafers are protected by

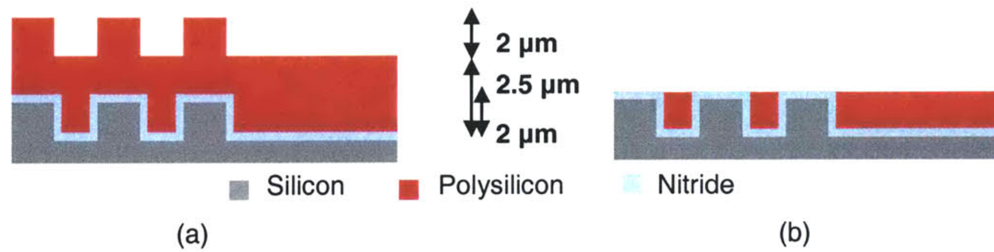


Figure 5-1: Schematic wafer cross-section, (a) pre-polish and (b) post-polish, for the damascene CMP experiment using the new MEMS test mask.

standard positive resist. Therefore, the shaded regions of the mask in Chapter 4 are protected, while the blank areas are exposed. After lithography, an Applied Materials P5000 plasma etcher and SF_6 chemistry plasma etch 2 μm down into the wafer substrate. After etching, a thin 50 nm pad oxide layer is grown before 500 nm of silicon rich silicon nitride is deposited on the wafer. After nitride deposition, we deposit 2.5 μm of polysilicon at 625°C.

We expect both the polysilicon and nitride layers to be polished, because the experiment will test a damascene process similar to shallow trench isolation. The polysilicon has been deposited over the nitride layer, and we will polish back all the overburden polysilicon until we have inlaid polysilicon between nitride. A schematic cross-section before polish and after polish can be seen in Figure 5-1.

For this damascene experiment, we polished 10 wafers at 50, 100, 150, 200, 250, 300, 350, 400, 450, and 500 seconds. The long polish times are necessary to polish the thick films. Also, the longer polish time ensures the clearing of all the polysilicon overburden above the nitride regions. We utilized the same CMP equipment and process parameters as were used in the preliminary experiment in Chapter 3. The Strasbough 6EC Chemical Mechanical Polisher utilized SS-25 silica slurry introduced at 200 mL/min. The down force was set to 68.95 kPa (10 psi) and the back pressure to 55.16 kPa (8 psi), while the

table speed and head speed are set to 28 rpm and 20 rpm, respectively. We used a Tencor UV1280 to make film thickness measurements.

5.1.2 Measurement Strategy and Metrology Issues

The new MEMS test mask provides many interesting different structures for measurement sites and data collection. However, for the experiment reported here, we limited our measurements to the Density test die 14D, because we want to quickly assess our CMP model for the polysilicon MEMS CMP process. Experience with CMP for integrated circuits also guides our measurement strategy. Our previous work has focused on examining chip scale pattern dependencies in CMP, where we have found that in order for a good CMP model to be formed, we must test a wide range of structures with different effective pattern densities. The 14D Density test die provides blocks with a wide range of pattern densities.

We use a Tencor UV1280 film thickness measurement system for metrology and data collection. However, the preliminary and new experiments differ in the way the UV1280 machine can be used. In the preliminary experiment, the different die blocks all had the same pattern density, so they had many similar polishing characteristics. For the new experiment, we polish a test die with a large variation in pattern density. The pattern density variation creates large film thickness non-uniformities. One die might have a few hundred angstroms of polysilicon remaining in up areas, while the down area trenches measure several microns in thickness. The film non-uniformities can cause measurement errors for the UV1280.

The UV1280 system measures film thickness by analyzing light reflected from the wafer sample. A beam of light is shined on the wafer surface at a predefined angle, and

the index of refraction of the surface film determines the amount of reflected light, as well as the reflection's optical properties. The system measures the properties of the reflected light to determine the thickness of the film being measured.

However, many of these reflections have similar properties, making it difficult for a system to accurately distinguish between the reflected spectrums of two different films. To ameliorate this problem, the UV1280 asks the user for a nominal seed value of film thickness. With the seed in hand, the system can filter through the list of similar reflected spectra and report the film thickness closest to the seed value. For polysilicon films, however, the seeds must be placed close together. We empirically determined that our film thickness seeds need to be approximately 300 nm apart in order for the system to reliably report film thickness. The experimental polysilicon film varies between 0 and 2.5 microns, so we need eight different seed values in order to obtain accurate measurements. While we can program a single recipe to make all the required measurements for the test die, we need eight copies of the recipe, each with a different seed, in order to accurately

Figure 5-2: Measurement sites for up (left) and down (right) areas.

measure the film. Running multiple measurement recipes and arduously recombining data into a coherent picture of the overall film thickness variation persuaded the experimenters to utilize a strategy that minimizes the number of measurements.

Our measurement strategy spans a variety of different pattern densities, while minimizing time spent working on metrology issues. We take 15 measurements points for both the up and down areas. Down area measurement points are in the center of each block within the Density test die. An example would be down site 1. It is located at $(x,y) = (2.5,2.5)$. Up area measurements occur in the middle of one of the lines at the center of each block; for example, up measurement site 1 is at $(x,y) = (2.25,2.5)$. The measurement locations can be seen in Figure 5-2. While there are only 15 measurement sites per die, there are 16 blocks within each die, because of the 100% and 0% pattern density regions. The 0% pattern density region does not have an up area measurement, because there are no features that are considered "up." Likewise, there are no down areas in a 100% pattern density region, so no down area measurement can be made in this block either.

5.2 *Experiment Results*

With metrology complete, we fit the data into the updated step height density model. We go beyond the simple Stage I polishing of the preliminary experiment, and inlay polysilicon into the down trenches. Using the parameters extracted from model fitting, we can predict the topography of the die as time goes forward. We also examine the clearing time needed to polish away all of the overburden, and explore dishing and erosion effects of the polishing.

5.2.1 Model Fit and Parameter Extraction

The updated step height density model extracts a blanket removal rate of 3216.2 Å/min, and an exponential decay constant, τ, measuring 2.9553e-4 $Å^{-1}$ for the Stage I polysilicon only polish. The planarization length for polysilicon only Stage I is 2.68 mm. The root mean square error for this stage is 1133.5 Å. The Stage I extracted model parameters aid our calculations for material removed during a Stage II dual material polish. For the dual material case, we find the nitride selectivity to be 5.202, and the nitride exponential decay term, τ_{nit} is 5.4076e-19 $Å^{-1}$. The overall root mean square error for both Stage I and Stage II is 2356 Å. The model fit and measured data can be examined in Figure 5-3.

Although the error is high, the model follows the general trend of how much material is removed. The model also covers the transition from a single to dual material polish. When the amount removed in the up areas reaches above 2.5 μm, the removal rate greatly slows down as the polishing process tries to remove the tougher nitride layer. On the whole, the model seems to be predicting more up and down area polishing than can be

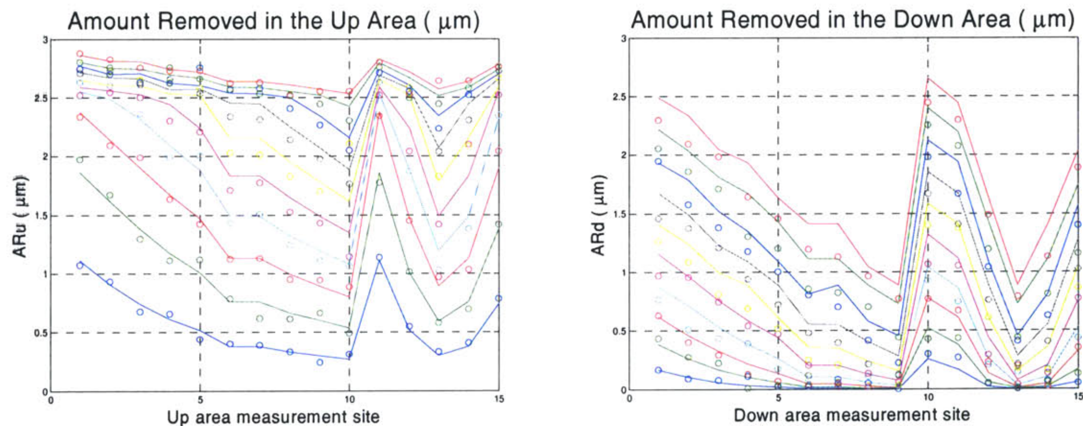


Figure 5-3: The measured (o) and expected (line) amounts of material removed in the up (left) and down (right) areas of the die.

supported by the actual measurements. However, the model accurately predicts the trends between the measured amounts removed at each time step. The primary difference between the model prediction and the measured data seems to a constant positive bias in the material removal graphs.

5.2.2 Die Topography Simulation

The updated step height density model seems able to model the general trends of MEMS CMP, but needs to be fine tuned to incorporate MEMS specific characteristics. However, the extracted parameters can still give a good rough estimate about how the topography of the die evolves during an extended polish time.

The overall Density test die can be simulated to show how the overall topography changes through time. Stage I shows purely polysilicon polishing before any nitride touchdown. Stage II polishing simulates dual material polish. Figure 5-4 shows the die topography for Stage I, while Figures 5-5 and 5-6 show the die topography for Stage II.

For Stage I polish, the density pattern dependence is very apparent. Even though the entire die starts out with the same film thickness, the polish will affect different regions differently. Regions with high pattern density will polish much slower than low pattern density regions. At 150 seconds, the 10% and 20% pattern density regions are on the threshold of touching down on the nitride. Yet the 90% and 100% pattern density regions still have approximately 1 μm of polysilicon overburden.Stage II polishing shows how the nitride, with a slower removal rate, affects the polishing of the whole die. After touch-down, the dual material polish begins. This slows the removal rate of the low pattern density regions, removing some topography built up in Stage I. Because the nitride and polysilicon have different removal rates, there will always be some

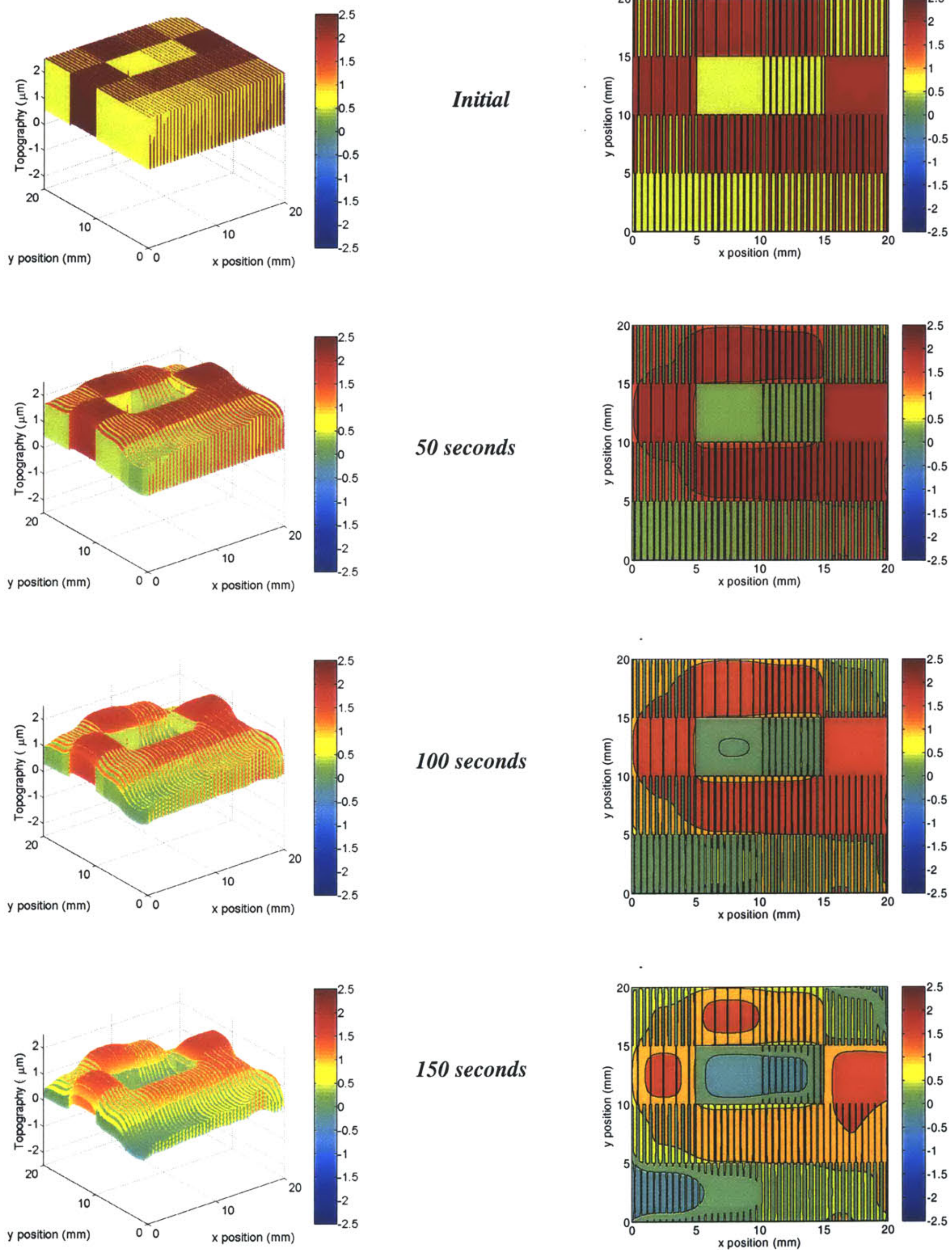


Figure 5-4: Die topography for Stage I polish. 3D meshes on the left, and contour plots on the right. This stage encompasses polish times of 50, 100, and 150 seconds.

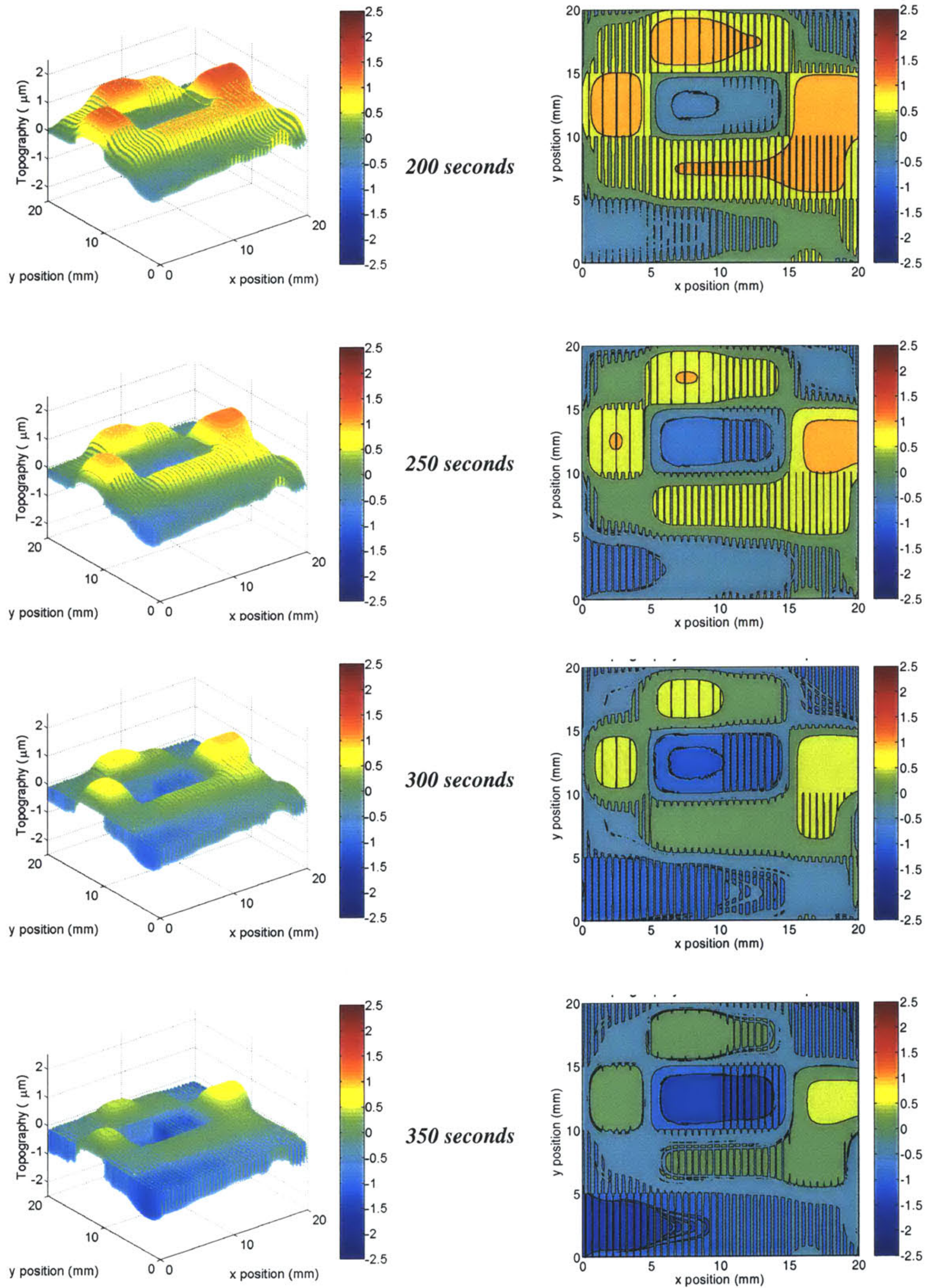


Figure 5-5: Stage II die topography for 200, 250, 300, and 350 seconds. 3D mesh plots on the left, and contour plots on the right.

Topography for 400 second polish

400 seconds

Topography for 400 second polish

Topography for 450 second polish

450 seconds

Topography for 450 second polish

Topography for 500 second polish

500 seconds

Topography for 500 second polish

Figure 5-6: Stage II die topography for 400, 450, and 500. 3D mesh plots on the left, and contour plots on the right.

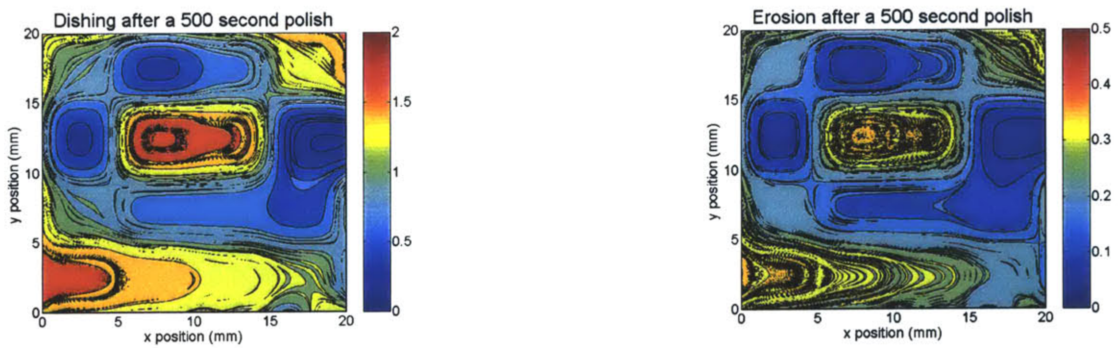


Figure 5-7: Simulated dishing (left) and erosion (right) after the 500 second polish.

topography that cannot be removed. Stage II polishing continues until all the overburden polysilicon has been removed from the die. We simulated the total clearing of all the polysilicon after a 500 second polish. Now that all the overburden has been removed, we can examine the dishing and erosion that affect the end thicknesses of nitride and the trench polysilicon in Figure 5-7. We discover that the maximum dishing is 1.8667 μm, while the maximum erosion is 0.4228 μm. Luckily, the maximum dishing and erosion sum to only 2.1871 μm. This sum is less than the 2.5 μm of polysilicon deposited in the down regions. While we have cleared the die surface of all the overburden, the extreme dishing and erosion can leave very little material actually inlaid within a trench.

5.2.3 Wafer Level Dishing and Erosion

While our model calibration and simulation examines only one die, our test wafers are filled with other test die. In addition to the 10 wafers mentioned in the new experiment, we polished two additional wafers for 550 and 600 seconds respectively. Photographs of the wafers were taken to get a visual perspective on the clearing, dishing, and erosion highlighted by the die level simulation.

Figure 5-8 shows a wafer photograph after a 50 second polish, showing features after a short Stage I polish. Close-ups of the Engine Negative 21EN and Engine Positive 28EP are also shown. In the picture, areas covered with a whitish film are down areas, where the polysilicon will be inlaid within the structure. The up areas, though appear jet black. This color scheme might have to do with surface roughness. Polished up areas have reduced surface roughness. The down areas are not polished as much, so their surface roughness may still be large enough to greatly scatter incoming light.

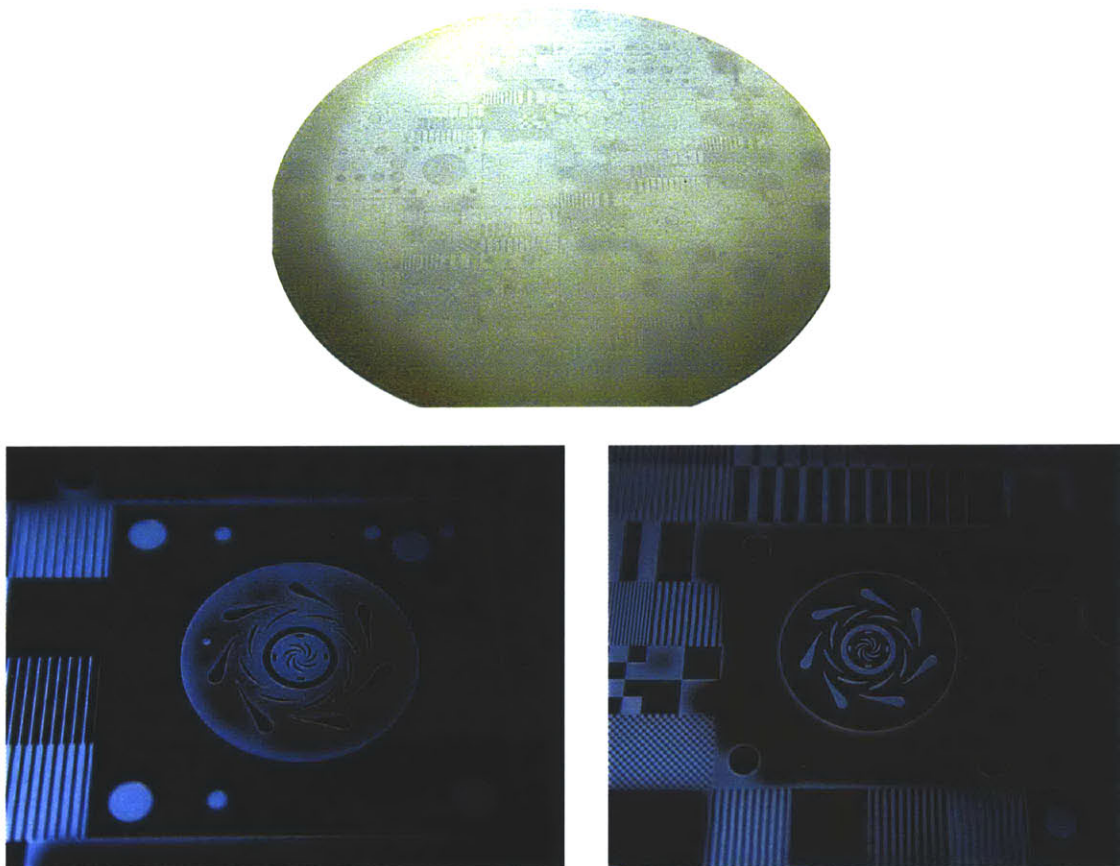


Figure 5-8: A wafer after a 50 second polish (top), a close-up of the 28EP die (left), and a close-up of the 21EN die (right).

Figure 5-9 shows the wafer after a 150 second polish. According to our simulation from the previous section, this is the last wafer before nitride touchdown. While the features are somewhat obscured in the picture, the different die are still distinguishable. The color variations across the wafer are caused by the non-uniform polysilicon overburden film. Pattern density effects cause non-uniform polishing during Stage I, and the results can be seen with the naked eye. The close-up picture of 28EP shows the same fringes on the die surface. The fringes on the blades of the compressor are particularly apparent, which are caused by the overburden polysilicon on top of the blades. The

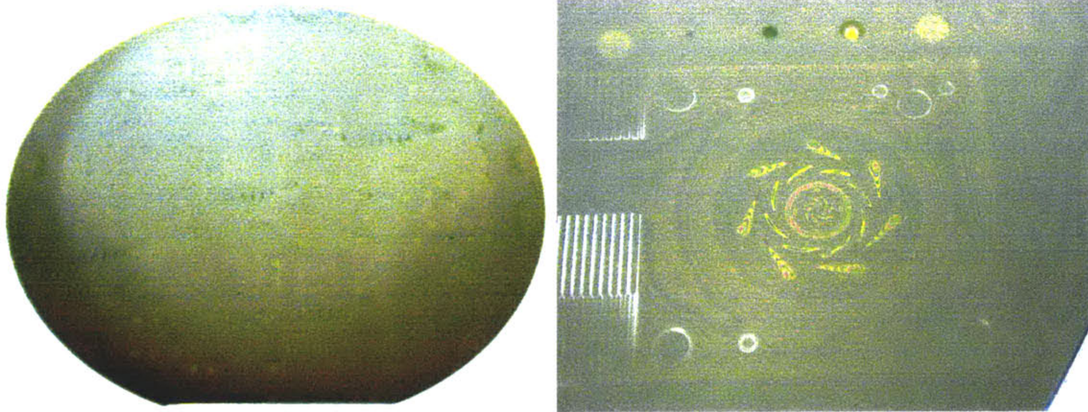


Figure 5-10: A 150 second polished wafer (left), and a close up of 28EP (right). The overburden polysilicon on top of the compressor blades create the color fringes.

compressor blades form islands in a vast, circular down region. This isolation makes the protruding overburden polysilicon particularly noticeable.

The 200 second polished wafer provides an excellent example of non-uniform overburden clearing. Seen in Figure 5-10, the wafer map provides a clear picture of the polysilicon overburden in the regions of high up area pattern density. The close-up picture of 28EP demonstrates how polysilicon clearing can occur at different times across

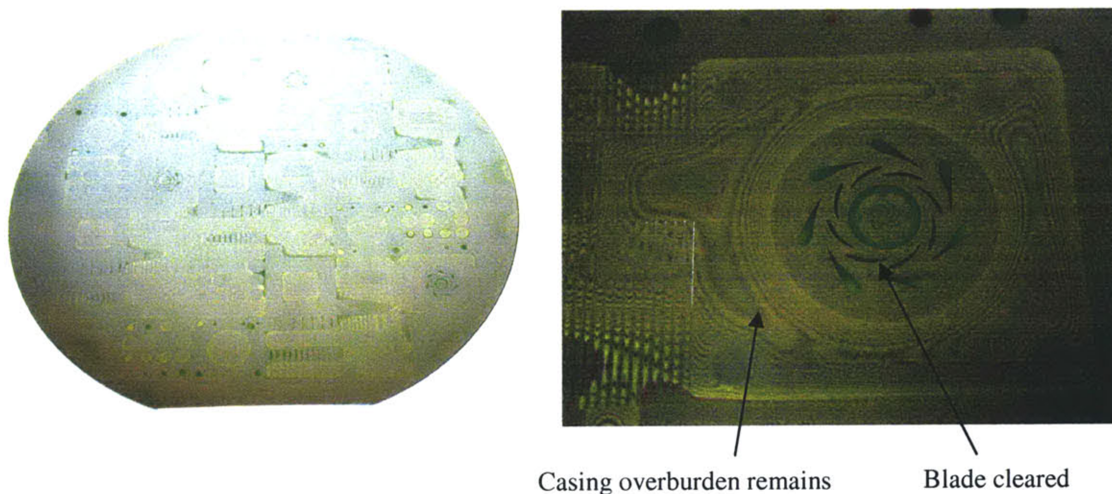


Figure 5-9: 200 second polished wafer (right) and 28EP close-up (left). The overburden on 28EP blade has been cleared, while the overburden on the casing is still visible.

a die. The overburden on top of the compressor blades, a low pattern density region, has been completely removed, and the underlying nitride can be seen. In the same die, the overburden in the high pattern density casing regions around the compressor chamber still exhibit bright fringe fields, signaling the presence of polysilicon.

After 250 seconds of polishing, less overburden remains visible on the wafer level picture in Figure 5-11. All elements of non-uniformities in dual material damascene polish can be seen in the pictures of 28EP and 21EN in Figure 5-12. Nitride erodes from 28EP's blades, while the casing overburden persists. Dishing in the casing region of 21EN occurs while the compressor region fails to clear.

After polishing for 300 seconds, even less overburden is apparent from a wafer level picture. Entire up regions have cleared polysilicon, and their nitride can be seen as the green features in Figure 5-11. However, the non-uniformity in clearing times has lead to some nitride areas to be over-polished. Even on the wafer level picture, eroded nitride regions show up purple in color. While 28EP still has a lot of overburden left in the casing region, Figure 5-12 shows that the die 21EN has mostly cleared the compressor chamber of polysilicon. Only one highly visible sliver of overburden remains. In

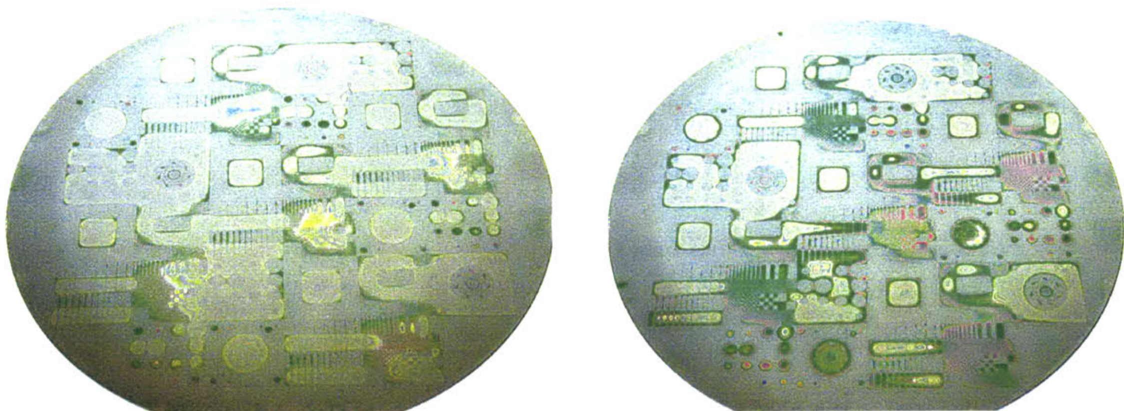


Figure 5-11: Wafers after a 250 second (left) and 300 second (right) polish. The area of colorful fringes representing overburden has been dramatically reduced.

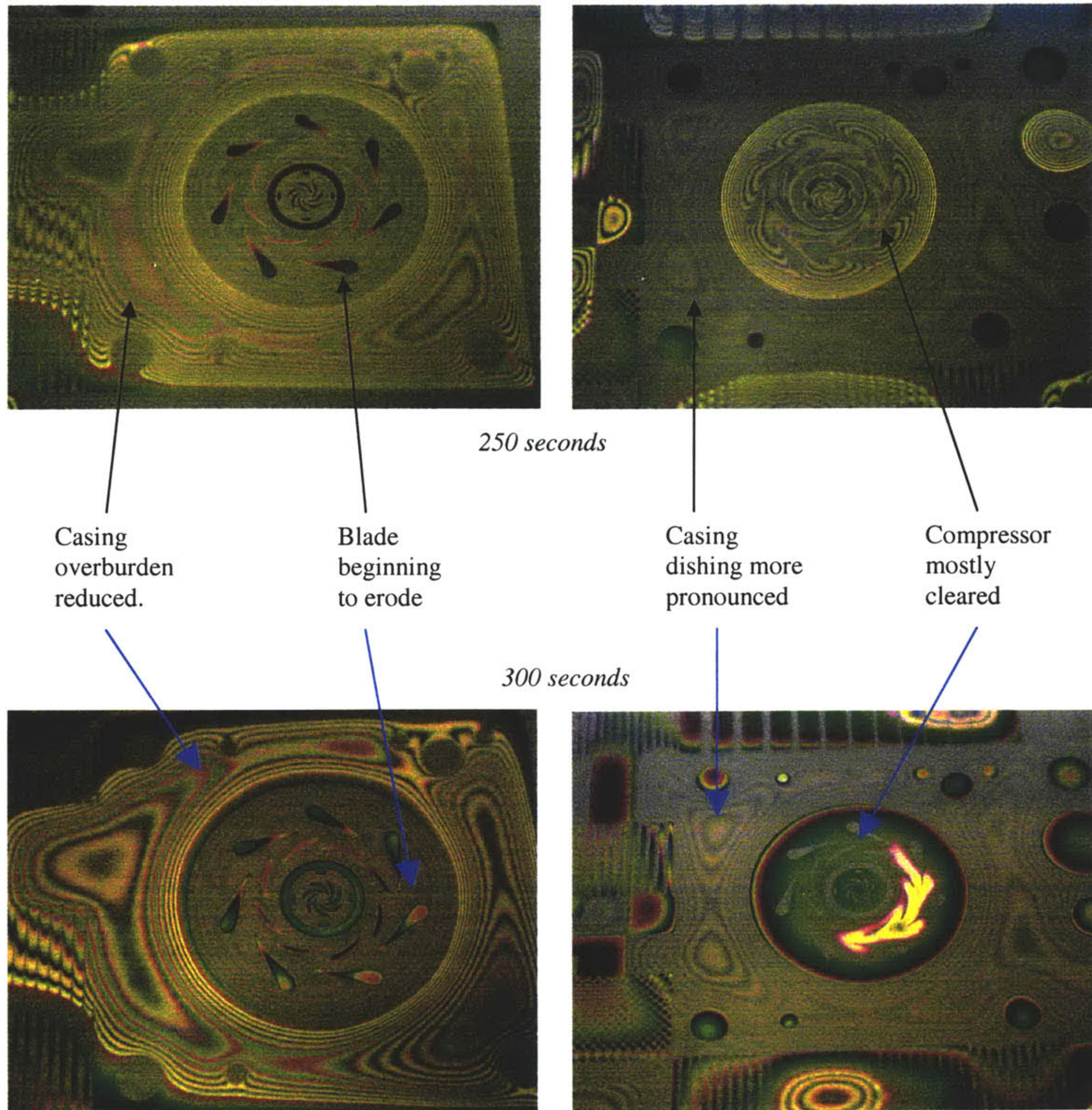


Figure 5-12: The dies 21EN and 28EP can be compared for 250 and 300 second polishes. The large blue arrows point out the topography changes created from the longer polish. The black arrows show the corresponding structures from the shorter polish time.

addition, the dishing in the casing region of 21EN is becoming more pronounced. Compared to the previous wafer, more fringe fields, indicating a wider range of non-uniform film thickness, can be seen.

As the polish times increase, more overburden can be seen disappearing from the wafer level pictures. No overburden polysilicon can be seen on the wafer surface for a 450 second polish, even though our earlier die simulation states a polish time of 500

seconds for complete clearing. But as the polish time increase, more and more nitride erosion occurs in the up areas of the wafer. Erosion is also not the only non-uniformity to consider. The wafer picture for a 500 second polish shows so much dishing in certain areas, that all inlaid polysilicon has been removed, and the nitride lining the bottoms of the down area trenches has been exposed.

Another problem, though not immediately visible in Figure 5-13, is extreme nitride erosion completely removing all nitride from some regions on the wafer surface. The extreme dishing and erosion of our test wafers can help us understand the kind of film thickness budget designers should consider when constructing process flows. Our experiment has shown that a 2 μm step height is too large, or a 2.5 μm overburden film is too thin to result in successfully inlaid polysilicon designs, given the wafer and die non-uniformities in this specific process.

Wafer level trends seen in Figure 5-13 can be verified by looking at the close up pictures of 21EN at different polish times in Figure 5-14. The compressor chamber will eventually have all or its overburden removed. But while this occurs, dishing can occur in the casing or even in the blades. Eventually, very long polishes will remove all the nitride from the compressor chamber, while the excessive dishing will remove all of the inlaid polysilicon from the casing area.

By examining the wafer pictures and close up pictures of the microengine dies, we have been able to link the die topography simulation to real polishing effects. We have seen how the non-uniformities affect the different die, and witnessed the results that excessive polishing will have on our devices. By examining this experiment, we can observe the interplay between the initial step height, the polysilicon, and the nitride film

thicknesses and devise ways to ensure that no layer with inlaid material is completely removed before all of its overburden has been cleared off a wafer surface.

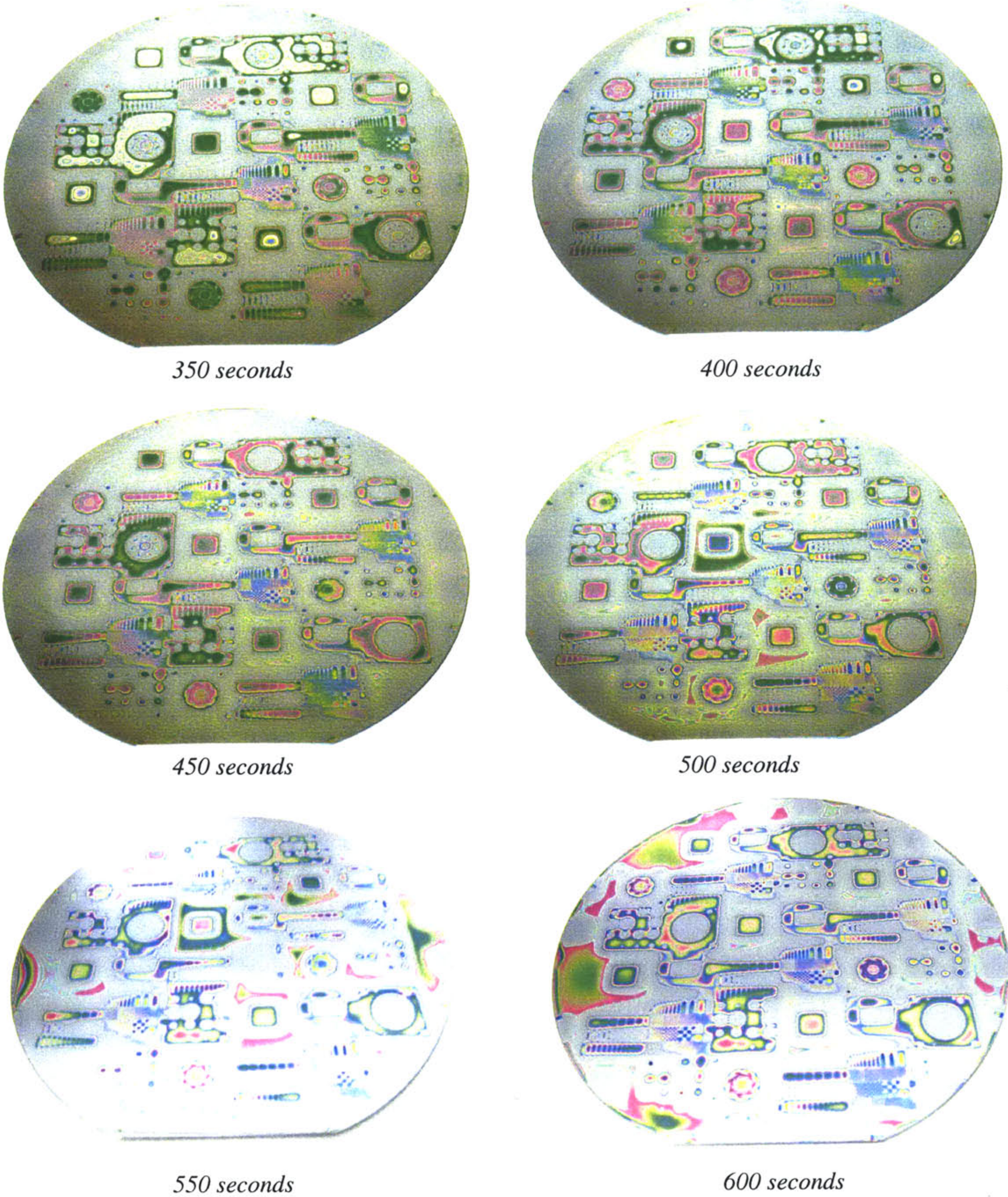
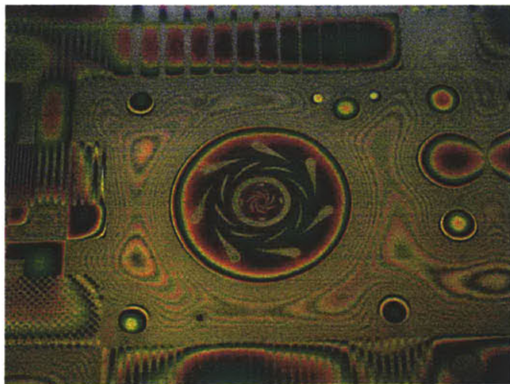
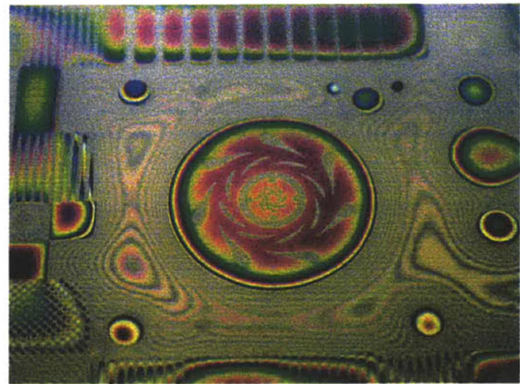


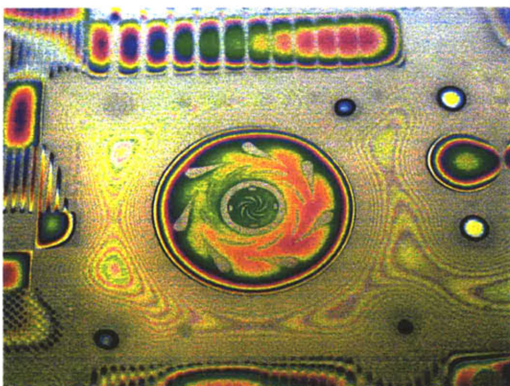
Figure 5-13: As polish time increase, the overburden recedes. Yet longer polishes create nitride erosion and down area dishing. Eventually, very long polishes can erode away all the nitride and remove all down area inlaid polysilicon through extreme dishing.



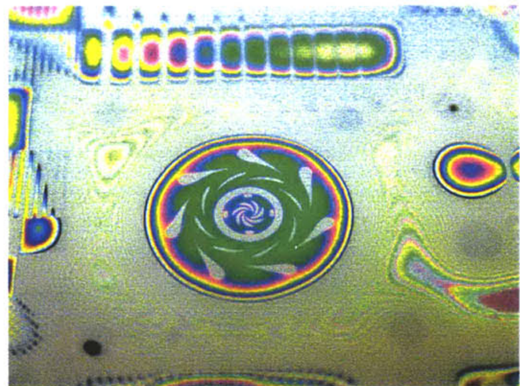
350 seconds



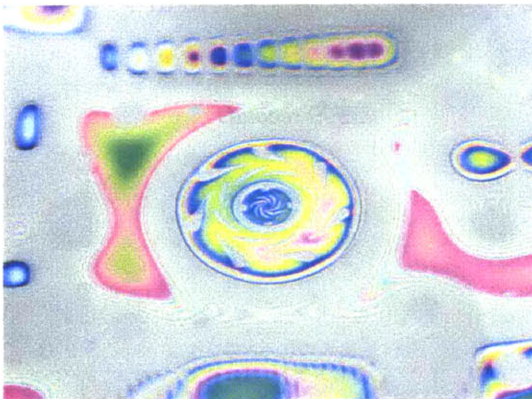
400 seconds



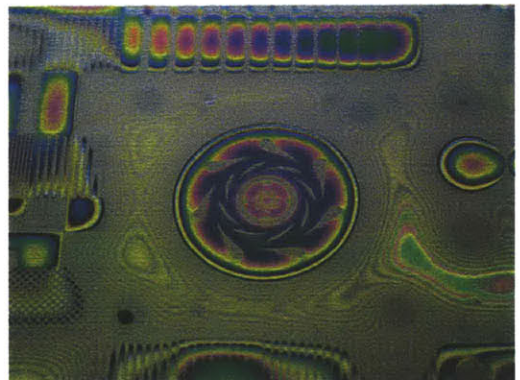
450 seconds



500 seconds



550 seconds



600 seconds

Figure 5-14: All the Engine Negative dies end up clearing their polysilicon overburden. But in the process, their underlying nitride is eroded and their inlaid polysilicon can be completely dished away.

5.3 Chapter Summary

This chapter has described a new CMP experiment examining damascene polishing for MEMS. We discussed the design of the experiment, as well as metrology for data collection. With the data collected, we demonstrated that a CMP model developed for integrated circuits can be applied to dual damascene MEMS CMP. Using the model, we simulated the evolution of a test die through different time steps. We qualitatively compared that simulation to pictures we collected to show how the entire test wafer evolves during chemical-mechanical polishing.

Chapter 6

Conclusions and Future Work

This work has examined chemical mechanical polishing for polysilicon MEMS applications. Experiments were carried out to characterize polysilicon MEMS CMP for both single and dual material polishing processes. Preliminary experiments led to the development of a new test mask specifically designed for MEMS applications. We examined whether CMP models from integrated circuits could be applied to MEMS CMP, then utilized the updated step height density model to simulate the evolution of a test die during CMP. The results of the simulation were then qualitatively compared to post-polish output of wafers patterned with the new MEMS CMP characterization mask.

6.1 Thesis Conclusions

Our study began with an introduction into chemical-mechanical polishing (CMP), microelectromechanical systems (MEMS), and how CMP can be used as an enabling technology for MEMS. In Chapter 2, we provided an in depth examination of past CMP models used for traditional integrated circuit processes. The shallow trench isolation (STI) process provided the basis for a model that examines polysilicon MEMS CMP. Using this adapted model, we completed a preliminary experiment in Chapter 3 that examined single material polysilicon MEMS CMP. This experiment helped us identify

unique and important characteristics that separate polysilicon MEMS CMP for other conventional CMP processes.

Using the insight gathered from the preliminary experiment, we created a new CMP characterization test mask specifically designed to explore unique characteristics of MEMS CMP. An explanation of the test structures and layout of the mask are provided in Chapter 4. Using the new MEMS mask, we performed a new experiment that confirmed the applicability of our adapted model to MEMS CMP. The experiment went beyond the scope of past work and studied dual material polish for polysilicon and silicon-rich silicon nitride. Chapter 5 describes the results of our new experiment, as well as compared the model simulation to the surface evolution of the new MEMS test wafers caused by CMP.

6.2 Future Work

The experiments presented in this thesis serve as a beginning to many possible studies of polysilicon MEMS CMP. One key area of further inquiry deals with the model used. Model adjustments should be made in order to incorporate and accommodate features important to MEMS CMP. An important effect to consider is the role of big, millimeter scale features, and how these features affect polishing. In particular, studies should pursue model updates based on polish dependences on large open areas or line spaces.

In order to make adjustments to the polysilicon MEMS CMP model, future experiments should more fully utilize the new MEMS CMP test mask. The mask contains other test structures in addition to the density test die utilized in our experiments. Some of the interesting structures to consider are the host of structures that vary line width or line space while keeping the other factor constant. Another test structure maintains a constant

pattern density, but varies the density configuration. This test die can help determine how much pattern density configuration can affect CMP. In addition to the two examples use here, there are many other possible uses for the MEMS test mask, and many interesting structures that are left to be examined and used.

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