Nanocrystalline Ge Flash Memories: Electrical Characterization and Trap Engineering

E.W.H. Kan[1], B.H. Koh[2], W.K. Choi[1,2], W.K. Chim[1,2], D.A. Antoniadis[1,3] and E.A. Fitzgerald[1,3]

[1]Singapore-MIT Alliance, 4 Engineering Drive 3, Singapore 117576
[2]Department of Electrical & Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117576
[3]Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA 02139-66307

***Abstract*—A single transistor memory structure with threshold voltage shift, V_{th}, exceeding ~1.5 V corresponding to interface charge trapping in nanocrystalline germanium (nc-Ge), operating at 0.96 MV/cm, is presented. The trapping effect is eliminated when nc-Ge is synthesized in forming gas thus excluding the possibility of quantum confinement and Coulomb blockade effects. Through discharging kinetics, the model of deep level trap charge storage is confirmed. The trap energy level is dependent on the matrix which confines the nc-Ge.**

***Index Terms*—Flash memory, nanocrystalline germanium, charge trapping, quantum dot.**

I. Introduction

CONVENTIONAL floating gate non-volatile memories (NVMs) present critical issues for device scalability beyond the sub-90 nm node, such as gate length and tunnel oxide thickness reduction [1]. Silicon (Si) and germanium (Ge) nanocrystal quantum dot flash memories are fully CMOS compatible technology based on discrete isolated charge storage nodules which have the potential of pushing further the scalability of conventional NVMs [2]. Quantum dot memories offer lower operating voltages as compared to conventional floating-gate (FG) Flash memories due to thinner tunnel dielectrics which allow higher tunneling probabilities. The isolated charge nodules suppress charge loss through lateral paths, thereby achieving a superior charge retention time [3].

In achieving non volatility in conventional FG memories, thicker control and tunnel oxides (~8 nm) are required to guarantee a ten-year retention time. The thicker control and tunnel oxides require large voltages for charge injection into the floating gate and also result in smaller capacitive coupling to the floating gate. In other words, the need for longer retention time can be achieved at the expense of higher operating voltage and longer operating time. Hence, there is a trade off between power and speed considerations and the charge retention time.

Earlier works on quantum dot Flash memories have been concentrated on using nanocrystalline silicon (nc-Si) to replace the continuous floating gate layer [3]. Over the years, numerous groups have proposed using nanocrystalline germanium (nc-Ge) and metal dots, such as Au, Ag, W, Pt and Sn [4]-[6] . The advantage of using metal nanodots is the creation of an asymmetrical barrier between the substrate and the storage nodules by engineering the metal work function, thus inducing a smaller barrier for writing and a larger barrier for retention [4]. Nevertheless, introducing metal nanodots compromises the compatibility to current silicon technology.

Nanocrystalline-Ge, though posing several fabrication challenges, is a perfect candidate to replace the floating gate. The smaller band gap, as compared to the Si substrate, results in a higher confinement barrier for retention and a smaller barrier for program and erase modes, similar to metal nanodots but without having any compatibility issues [7]. The fabrication of nc-Ge is more difficult than nc-Si due to the former's lower evaporation temperature and difference in surface energy with respect to the oxide. Nanocrystalline-Ge formation has been reported using methods like Ge ion implantation in SiO_2 [8], RF or DC sputter deposition [9] and oxidation of SiGe alloys with subsequent high temperature annealing to synthesize the nc-Ge [10].

Despite the considerable amount of efforts devoted to the study of nanocrystal Flash memories, the charge storage mechanism remains obscure. Interfacial defects of the nanocrystals seem to play a role in charge storage in recent studies [11]-[12], although storage in the nanocrystal conduction band by quantum confinement has been reported earlier [13]-[14]. Also, a more controllable fabrication method has yet to address the non-uniformity of dot dimensions and dot densities across devices. Such non-uniformities induce fluctuations in the electrical

Eric W.H. Kan is a research scholar with Singapore-MIT Alliance, 4 Engineering Drive 3, Singapore 117576 (e-mail:erickan@nus.edu.sg).

B.H. Koh is with Department of Electrical & Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117576 (e-mail:engp1660@nus.edu.sg).

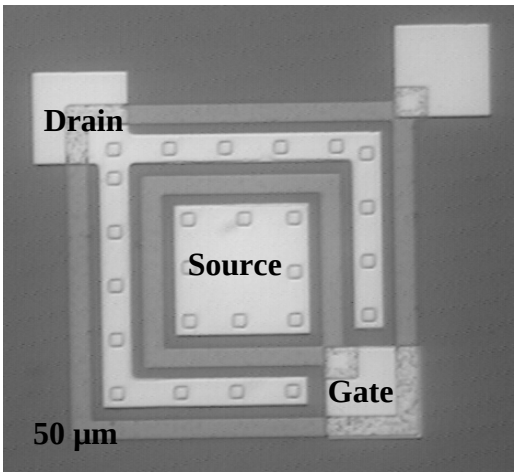

Fig. 1. Plan view of the memory transistor taken using an optical microscope. Gate length is 10 µm.

characteristics of the device.

In this paper, we fabricated nc-Ge embedded in SiO_2 by wet oxidation of $Si_{0.54}Ge_{0.46}$ films. The electrical characteristics of the memory devices are presented. Further emphasis is also given to determine the charge location and methods to improve retention time.

II. Device Fabrication

The nc-Ge Flash memories were fabricated on p-type (100) Si wafers using ring transistor structures of various gate lengths [Fig. 1]. The dielectric stack consisted of a 5 nm-thick (nc-Ge+SiO_2) layer sandwiched between a 5 nm-thick tunnel oxide and a control oxide of 40 nm thickness. Fig. 2 shows a schematic diagram of the cross sectional transistor structure accompanied by a high resolution TEM (HRTEM) image of the structure.

The tunnel oxide was first grown on the Si wafers via rapid thermal oxidation at 1000 ^oC for 35 s. A layer of $Si_{0.54}Ge_{0.46}$ film was then deposited by the rf sputtering technique at room temperature in argon (Ar) gas at a pressure of 3.3 mTorr. A typical deposition rate of 4 Å/s was obtained with a rf power of 100 W. The tunnel oxide plus $Si_{0.54}Ge_{0.46}$ film was annealed at 800°C for 6 h in pure nitrogen (N_2) ambient to form a tunnel oxide-polycrystalline $Si_{0.54}Ge_{0.46}$ structure. The thickness and Ge content of the $Si_{0.54}Ge_{0.46}$ film were determined using a step profiler and the Rutherford backscattering technique, respectively. The wet oxidation of $Si_{0.54}Ge_{0.46}$ film was then performed at 600°C for 4 min using a conventional three-zone furnace. The structure was then capped with a rf sputtered SiO_2 gate oxide layer deposited at room temperature to achieve a trilayer (tunnel oxide/oxidized polycrystalline $Si_{0.54}Ge_{0.46}$/rf sputtered SiO_2) structure. Finally, the trilayer structure was rapid thermal annealed (RTA) in either pure N_2 or forming gas (90%N_2+10%H_2) ambient using a double step (1000°C for 300 s followed by 700°C for 60 s) annealing process. The double-step annealing process was to enable the formation of spherical nc-Ge with good crystallinity, shape and size distribution in the silicon oxide matrix [15]. Fig. 3 shows the planar TEM image of the synthesized nc-Ge. The mean diameter (δ) of the nc-Ge was estimated to be 5.67±1.31 nm with an area density of ~9×10^{11} cm^{-2}.

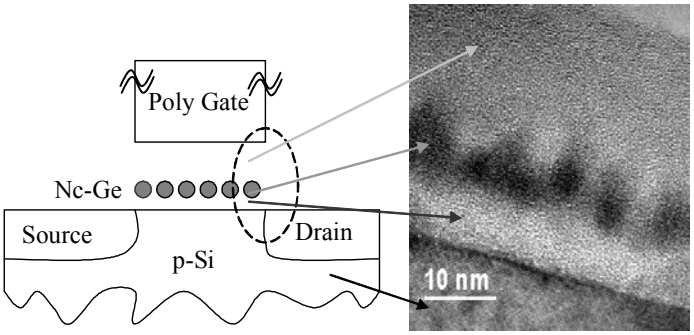

Fig. 2. Schematic cross-sectional structure of fabricated device and HRTEM image of the SiO_2/nc-Ge/SiO_2 structure.

A poly-Si gate electrode was deposited at 600 ^oC using LPCVD. The nc-Ge that remained after the gate etch step outside the channel region were removed by a subsequent 10% HF etch. After the source/drain and gate *n*+ implantation, a rapid thermal anneal was performed at 950 ^oC for 30 s in N_2. Al metal was deposited before a forming gas sintering process at 450 ^oC for 5 min.

As for capacitor structures, where capacitance versus time (C-t) measurements were performed, nc-Ge were synthesized in a conventional furnace at 800 ^oC for 30 min in pure N_2 ambient. This was to ensure that the replaced Al_2O_3 tunnel barrier would not succumb to crystallization that may lead to excessive current leakage.

III. Result and Discussion

A. Memory Operation and Charge Trapping

Fig. 4(a) shows the drain current (I_{DS}) versus gate voltage (V_{GS}) with write and erase voltages at 10 V and 1 V, respectively for various hold durations (t_{hold}). The measured threshold voltage shift (ΔV_{th}) between fresh and

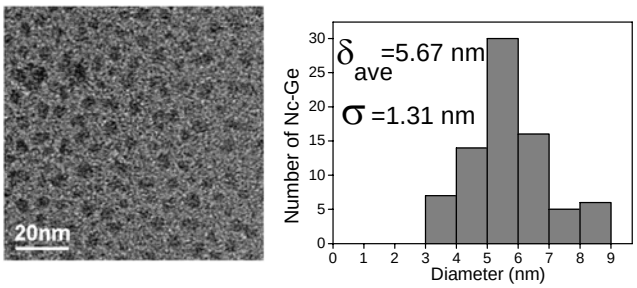

Fig. 3. Planar TEM image of self assembled nc-Ge embedded in SiO_2. The histogram plot shows the size distribution of the nc-Ge.

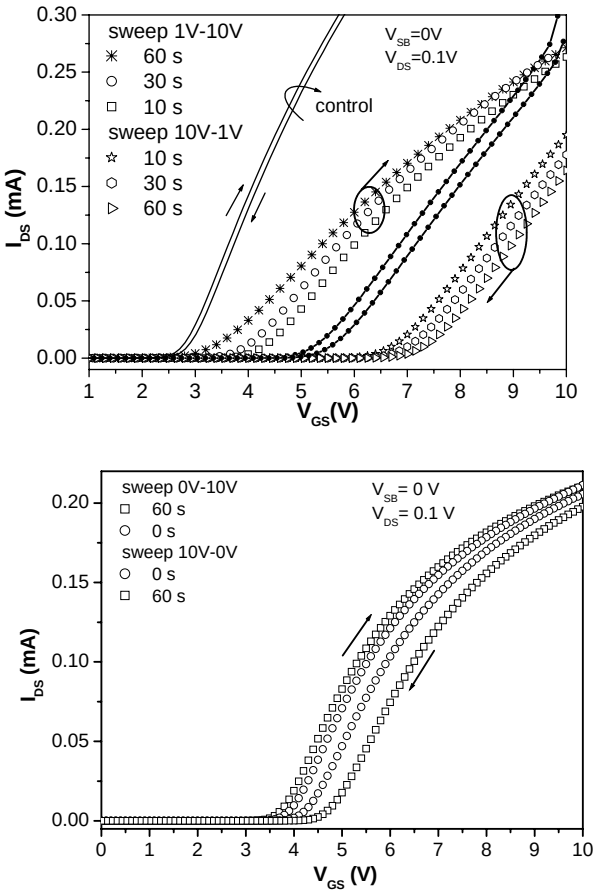

Fig. 4 (a). Hysteresis characteristics of the n-channel nc-Ge memory fabricated in pure N_2. No hysteresis was observed in control devices. (b) Hysteresis characteristics of similar nc-Ge memory fabricated in forming gas.

programmed device were about 1.5 V (write) and 1V (erase) for t_{hold} of 10 s. No hysteresis was observed in control devices which did not have nc-Ge. This indicates that nc-Ge plays a significant role in storing the charges and not the interface traps that may exist between the Si substrate and SiO_2 tunnel dielectric, or bulk traps in the host matrix of the nanocrystals. The significant positive shift in the overall V_{th} for devices containing nc-Ge as compared to the control samples indicates the presence of negative fixed charges with the introduction of Ge [16]. The hysteresis was significantly reduced when the nc-Ge was synthesized in forming gas (10% H_2 + 90% N_2), as shown in Fig. 4(b). TEM images indicate the presence of similar nc-Ge in the forming gas annealed/fabricated structures [17]. This suggests that the charges are stored in traps that can be passivated by hydrogen rather than within the conduction band of the nc-Ge.

B. Programming Characteristic and Data Retention

Fig. 5 shows the measured drain current transient during programming, presented in linear and logarithmic time scales. Bias voltages of V_{GS} = 9 V and V_{DS}= 0.1 V were used. A characteristic with short and long time constant regions was observed in these measurements; i.e., after an initial rapid change, the electronic state of the structure

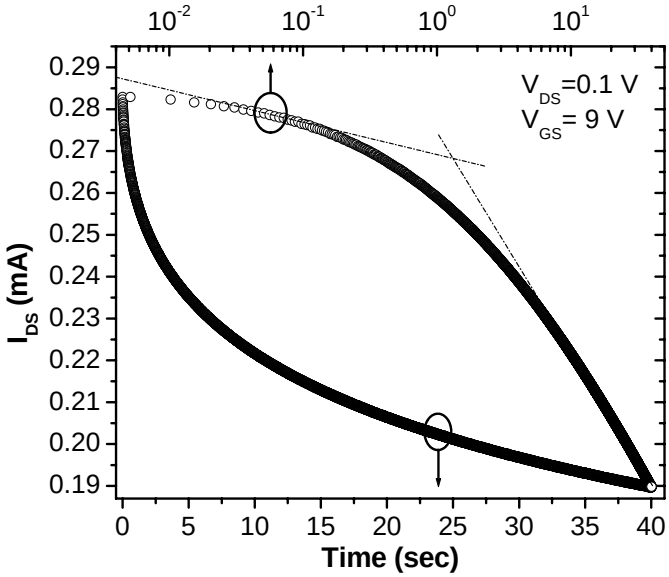

Fig. 5. Measured linear drain current transient during programming.. The drain current was decreased due to electron programming. Two time constants were observed.

changes slowly. The existence of two time constants described a two-step process consisting of carrier tunneling and nanocrystal interface trapping. Nevertheless, the preferred injection is through an efficient transmission into the nanocrystal which has a large capture cross-section and forms a path to possible localization at the interface defect [18]. Also, the density of traps and defects at the interfaces of the nanocrystals with the host matrix are enhanced due to the large surface- to-volume ratios and high surface roughness and composition disorders [7].

Fig. 6 shows the retention characteristics of the memory transistor device for the excess electron (write) state and excess hole (erase) state. After electrons were injected (programmed) from the inversion layer onto the dots with gate voltage 15 V for 20 s, retention characteristics were

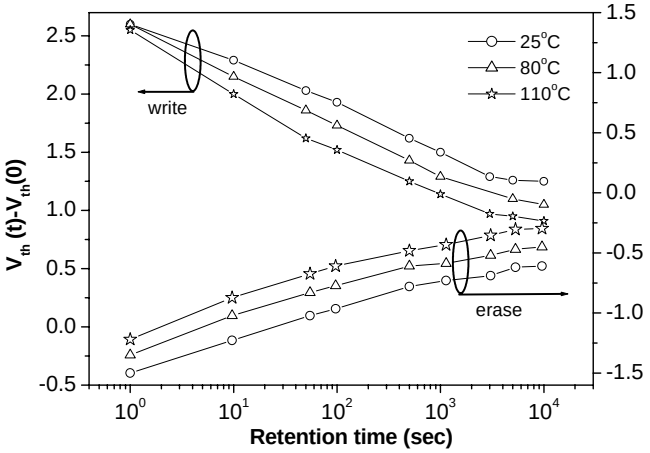

Fig. 6. Retention characteristics of excess electron and hole programmed states of the memory transistor at various temperatures.

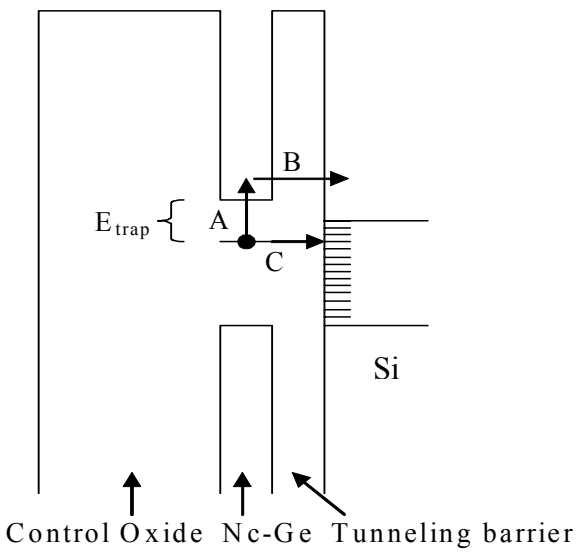

Fig. 7. Schematic diagram of deep level charge storage and discharging mechanism.

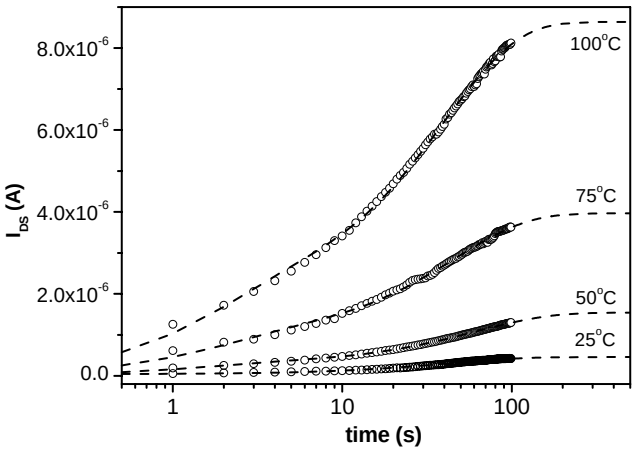

Fig. 8. Drain current (I_{DS}) transient at the read voltage of 5 V after writing at 15 V for 20 s. Symbols represent measured data and the lines are fitted data.

measured. The electron loss rate was observed to be at 0.31 V/decade at 25 °C, 0.35 V/decade at 80 °C and 0.45 V/decade at 110 °C. The retention characteristics of holes were also measured after erasing with a gate voltage of -15 V. The magnitudes of the hole loss rate were 0.27 V/decade (25 °C), 0.31 V/decade (80 °C) and 0.34 V/decade (110 °C). The smaller loss rate for holes results from a higher tunneling barrier for holes.

C. Nanocrystal Interfacial Trap Engineering

We have earlier discounted the possibility of charge storage within the conduction band of the nc-Ge. In this following subsection, we will experimentally confirm that the charge is indeed caused by the interfacial traps at the interface between the nc-Ge and the surrounding matrix.

The interface of bulk Ge and SiO_2 has been reported to have surface defect densities on the order of 10^{12} cm^{-2} [16]. Though the defect density is low on a nanocrystal (one defect per nc-Ge of 5 nm in diameter), the highly strained surface of each nanocrystal induces large surface stress which increases its defect density.

Fig. 7 illustrates the discharging model based on deep level charge storage caused by trap levels at the interface of the nc-Ge. Using the temperature dependence of the discharging time constant, two different discharging mechanisms are resolved in the experimental measurements. The first discharging mechanism is portrayed by paths A and B. This charge decaying mechanism involves thermal excitation of trapped electrons from the occupancy state to the conduction band of the nc-Ge followed by band-to-band tunneling into the Si substrate. The second decaying mechanism depicted by path C, which has lower temperature dependence, is trap-to-trap tunneling of electrons from the occupancy state to the Si-SiO_2 interface states. We have made assumptions that the tunnel barrier does not have any trap assisted leakage sites and that there is no tunneling of holes from the Si valence band into the nc-Ge under the influence of the internal electric field.

The discharging time constant is obtained by measuring the drain current (I_{DS}) transient. Fig. 8 shows I_{DS} transients with read voltage, V_R of 5 V after writing at 15 V for 20 s. It exhibits an S-shaped monotonically increasing curve due to the discharging of stored electrons in the nc-Ge. The increase in I_{DS} for higher temperatures could be well explained by the larger carrier mobility and the higher intrinsic carrier concentration of the substrate. The increased intrinsic carrier concentration reduces the Fermi level (ϕ_F) of the substrate. This causes the voltage drop at the substrate ($\sim 2\phi_F$) during inversion to reduce which would then enhance the vertical electric field across the gate stack oxide.

Each I_{DS} transient curve was fitted with a first-order double exponential decaying equation after Ref. [11],

$$I_{DS\,(transient)} = n_1(1-\exp(-\lambda_1 t)) + n_2(1-\exp(-\lambda_2 t)) \quad (1)$$

where $n_1+n_2=n$, total nc-Ge charging sites and λ_1 and λ_2 represent two different discharging mechanism. The discharging time constant (τ_D) was determined to be the time corresponding to 90 % of the I_{DS} at steady state. The inverse of τ_D is directly proportional to the thermal equilibrium emission constant (e_n).

Using the approach by Shockley, Read and Hall, the rate of emission (R_e) of electrons from traps in the nc-Ge is proportional to the number of occupied electron traps with the proportionality constant being the emission constant (e_n) [19],[20]:

$$R_e = e_n N_t f_t \quad (2)$$

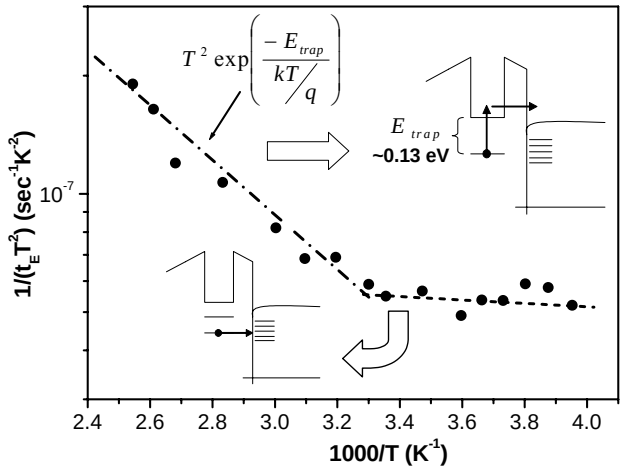

Fig. 9. Inversed discharging time constants divided by squared temperature (T) versus inversed T.

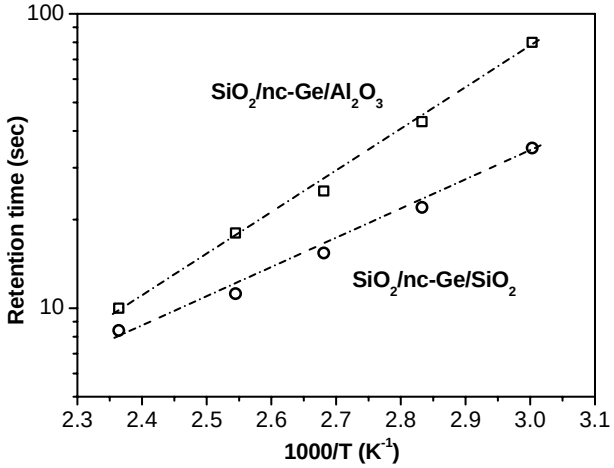

Fig. 11. Temperature dependence of retention time for nc-Ge capacitors with SiO_2 and Al_2O_3 tunnel barrier.

where N_t is the total number of electron traps (cm^{-3}) and f_t is trap occupation probability which is given by the Fermi-Dirac distribution function.

The thermal equilibrium emission constant (e_n) can be simplified [21], yielding:

$$e_n(E_{trap}) = AT^2 \exp\left[-E_{trap}q/kT\right] \quad (3)$$

where E_{trap} is the trap energy level measured from the conduction band of the nc-Ge, A is a non-temperature-dependent constant, *k* is Boltzmann's constant and T is absolute temperature.

Fig. 9 shows the $1/(\tau_D T^2)$ versus 1/T whereby the E_{trap} (0.13 eV) is indicated by the gradient of the slope at high temperatures. At lower temperatures, the temperature dependence is smaller than 0.13 eV and this region indicates the dominance of direct tunneling of electrons from deep level traps to the interface states at the Si/SiO_2 interface.

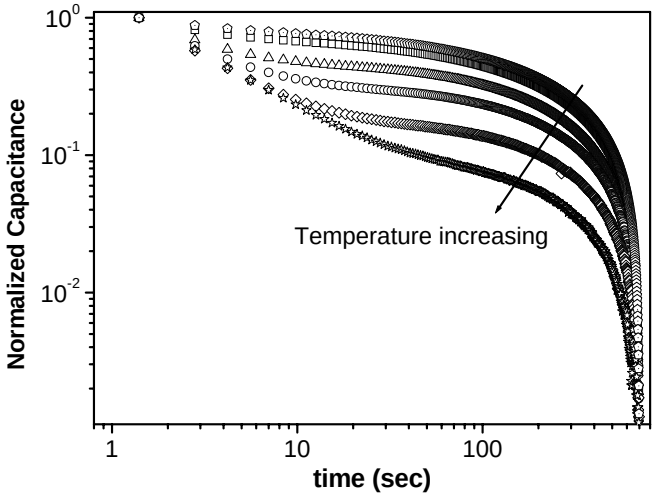

Fig. 10. C-*t* discharging curves for structure with nc-Ge and SiO_2 tunnel barrier at various temperatures.

Controlling the deep trap level where charge storage occurs is crucial to increase the retention duration of the memory device. The calculated range of discharging time constant for nc-Si varies on the order of 10^9 when the trap level shifts from the conduction band edge to midgap [11]. Engineering the trap energy level is achievable by manipulating the material of the host matrix.

To verify the above, we have fabricated basic capacitor structures with nc-Ge embedded within the dielectric of different tunnel barriers. C-*t* measurements of two capacitors with tunnel barriers of 5 nm SiO_2 and 5 nm Al_2O_3, respectively, were obtained. Fig. 10 shows the typical C-*t* plot of the capacitor structure with SiO_2 as the tunnel barrier. The retention time for the device at various temperatures is defined by the time taken for the capacitance to decrease to a normalized capacitance value of 0.5.

The Arrhenius plot of retention time shown in Fig. 11 shows the temperature dependence of the retention time with different tunnel barrier. Nc-Ge with Al_2O_3 shows higher temperature dependence than that of SiO_2. The difference in activation energy of the two cases implies differences in the discharging mechanism, thus suggesting that the nc-Ge/Al_2O_3 interface generate deeper trap levels than the nc-Ge/SiO_2 interface.

IV. Conclusion

Nanocrystal Flash memory is a perfect candidate to replace conventional floating gate technology with numerous advantages such as lower operating power, longer retention time and faster write/erase operation. Nanocrystalline-Ge, is particularly favorable due to its smaller band gap which results in a higher confinement barrier for retention and smaller barrier for program and erase mode operation. By modifying the host matrix which the nanocrystals are in contact, the trap level at the

interface of nc-Ge can be engineered to achieve a desirable depth for optimum memory performance.

ACKNOWLEDGMENT

The authors would like to thank the Singapore-MIT Alliance and the National University of Singapore for supporting this work.

REFERENCES

[1] Int. Tech. Roadmap for Semicond. (SIA, San Jose, CA), http://public.itrs.net/Files/2003ITRS/Home2003.htm, 2003.

[2] J.DeBlauwe, *IEEE Trans. Nanotech*, vol. 1, p. 72, 2003.

[3] H.I. Hanafi, S. Tiwari, and I. Khan, "Fast and long retention time nanocrystal memory," *IEEE Trans. Electron Devices*, vol. 43, pp.1553-1558. Sept. 1996.

[4] Z. Liu, C. Lee, V. Narayanan, G. Pei and E. C. Kan, "Metal Nanocrystal Memories – Part I: Device Design and Fabrication," *IEEE Trans. Electron Devices*, vol. 49, pp.1606-1613. Sept. 2002.

[5] Z. Liu, C. Lee, V. Narayanan, G. Pei and E. C. Kan, "Metal Nanocrystal Memories – Part II: Electrical Characteristics," *IEEE Trans. Electron Devices*, vol. 49, pp.1614-1622. Sept. 2002.

[6] A. Nakajima, T. Futatsugi, N. Horiguchi, H. Nakao and N. Yokoyama, "Single Electron charging of Sn Nanocrystals in Thin SiO_2 Film Formed by Low Ion Implantation," *Int. Electron Device Meet.* (1997) p.159.

[7] Y. Shi, K. Saito, H. Ishikuro and T. Hiramato, "Effects of traps on the charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystal," *J. Appl. Phys.*, vol. 84, pp. 2358-2360, 1998.

[8] Y.-C. King, T.-J. King, and C. Hu, "Charge-trap memory device fabrication by oxidation of $Si_{1-x}Ge_x$," *IEEE Trans. Electron Devices*, vol. 48, pp. 696-699, Apr. 2001.

[9] Y. Maeda, N. Tsukamoto, Y. Yazawa, Y. Kanemitsu, and Y. Matsumoto, *Appl. Phys. Lett*. vol. 59, p. 3168, 1991.

[10] M. Zacharias and R. Weigand, "A comparative study of Ge nanocrystals in $Si_xGe_yO_z$ alloys and SiO_x/GeO_y multilayers," *J. Appl. Phys.*, vol. 81, p. 2384, 1997.

[11] S.J. Baik, S. Choi, U.-I. Chung, and J.T. Moon, "Engineering on tunnel barrier and dot surface in Si nanocrystal memories," *Solid-State Electronics*, vol. 48, pp. 1475-1481, 2004.

[12] S.J. Baik, K.S. Lim, *Appl. Phys. Lett*. vol. 81, p. 5186, 2002.

[13] M. She and T.J. King, "Impact of Crystal Size and Tunnel Dielectric on Semiconductor Nanocrystal Memory Performance," *IEEE Trans. Electron Devices*, vol. 50, pp. 1934-1940, Sept. 2003.

[14] S. Tiwari, F. Rana, K. Chan. H. Hanafi, W. Chan, and D. Buchanan, "Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage," *Int. Electron Device Meet.* p.521, 1995.

[15] E.W.H. Kan, C.C. Leoy, W.K. Choi, W.K. Chim, D.A. Antoniadis and E.A. Fitzgerald, "Effect of annealing profile on defect annihilation, crystallinity, and size distribution of germanium nanodots in silicon dioxide matrix," *Appl. Phys Lett.*, vol. 83, pp. 2058-2060, Sept 2003.

[16] D. Nayak, K. Kamjoo, J.C.S. Woo, J.S. Park, and K.L. Wang, "Rapid thermal oxidation of GeSi strained layers," *Appl. Phys Lett.*, vol. 56, pp.66-68, Jan 1990.

[17] E.W.H. Kan, W.K. Choi, W.K. Chim, E.A. Fitzgerald and D.A. Antoniadis, "Origin of charge trapping in germanium nanocrystal embedded SiO_2 system: Role of interfacial traps?," *J. Appl. Phys.*, vol. 95, pp. 3148-3152, Mar 2004.

[18] J. A. Wahl, H. Silva, A. Gokimak, A. Kumar, J.J. Welser, and S. Tiwari, "Write, erase and storage times in nanocrystal memories and the role of interface states," *IEDM Tech. Dig*., 1999, p. 375.

[19] W. Shockley, and W.T. Read, *Phys. Rev*., vol. 87, p. 835, 1952.

[20] R.N. Hall, *Phys. Rev.*, vol. 87, p. 387, 1952.

[21] P.J. McWhorter, S.L. Miller, and T.A. Dellin, "Modelling the memory retention characteristics of silicon-nitride-oxide-silicon nonvolatile transistors in a varying thermal environment," *J. Appl. Phys.*, vol. 68, pp. 1902-1909, Aug. 1990.