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Effects of Platinum on NiPtSiGe/n-SiGe and NiPtSi/n-Si Schottky contacts

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***Abstract*—The I-V characteristics of 10nm Ni(Pt=0, 5, 10 at.%) germanosilicides/n-$Si_{0/7}Ge_{0.3}$ and silicides/n-Si contact annealed at 400 and 500°C were studied. For Schottky contact on n-Si, with the addition of Pt in the Ni(Pt) alloy, the Schottky barrier height (SBH) increases greatly. With the inclusion of a 10% Pt, SBH increases ~0.13 eV. However, for the Schottky contacts on SiGe, with the addition of 10% Pt, the increase of SBH is only ~0.04eV. This is explained by pinning of the Fermi level. The forward I-V characteristics of 10nm Ni(Pt=0, 5, 10 at.%)SiGe/SiGe contacts annealed at 400°C were investigated in the temperature range from 93 to 300K. At higher temperature (>253K) and larger bias at low temperature (<253K), the I-V curves can be well explained by a thermionic emission model. At lower temperature, excess currents at lower forward bias region occur, which can be explained by recombination/generation or patches due to inhomogenity of SBH with pinch-off model or a combination of the above mechanisms.**

***Index Terms*—Schottky barrier height (SBH), Thermionic emission model, Pinch-off model.**

I. INTRODUCTION

One of the problems limiting the performance of Silicon MOSFET is the speed that carriers can move from source to drain. Si/SiGe heterostructures on Si wafers are currently explored as channel materials for high performance MOSFETs. Self-aligned silicide has been formed at the source and drain regions in MOSFETs for several technological nodes [1-3]. Ni-silicide has been identified as the next potential candidate for advanced CMOS Si technology because of less silicon consumption etc. [4]. However NiSi has weak thermal stability and is easy to agglomerate as low as 600°C [5]. With the addition of Ge in the Si substrate, the degradation of film morphology happens at even lower annealing temperature. In addition, Ge out-diffusion occurs at low temperature (~500°C) [6,7]. It has been reported that the addition of Pt can improve thermal stability and surface morphology of NiSi on Si substrate [8]. Our previous work has shown that the addition of Pt can suppress agglomeration and Ge out-diffusion [9]. Solid phase reaction of NiPt/Si and NiPt/SiGe is one of the key issues for silicide (germanosilicide) technology. Especially, the NiPtSiGe, in which four elements are involved, is a very complex system. As a result, a detailed study is necessary for the interfacial reaction between NiPt alloy film and SiGe substrate. Besides using traditional material characterization techniques such as XRD, RBS, XTEM, characterization of Schottky diode is a good measure to detect the interface imperfections or defects, which are not easy to be found on large area blanket samples.

In addition, application of Schottky junction to source/drain (S/D) has been put forward recently and PtSi Schottky S/D MOSFET with lower barrier height has been reported [10,11]. Schottky source/drain MOSFET is attractive because there is no dopant implantation so that the high temperature dopant activation is eliminated.

In this article, we consider the Pt effect on the change of SBH. I-V characterizations are carried out and respective Schottky barrier heights are calculated by the thermionic emission model for Ni(Pt=0, 5, 10 at.%) annealed n-$Si_{0.7}Ge_{0.3}$ and n-Si at 400 and 500^0C, respectively. In addition, the I-V characteristics of NiPtSiGe/ $Si_{0.7}Ge_{0.3}$ contact annealed at 400^0C are investigated in a temperature ranging from 93 to 300K.

II. EXPERIMENTS

In our study, the SiGe(100) growth was carried out by a ultrahigh vacuum chemical vacuum deposition (UHVCVD) technology using SiH_4 and GeH_4 as the source gases. The starting wafer was a 4" Si wafer, and a compositionally graded layer with a gradually increasing Ge composition was grown subsequently at 900ºC and 25mTorr on the Si wafer until it reached the desired Ge composition. The SiGe layers were in-situ doped with phosphorous to about 10^{17} cm^{-3}. In order to get n-$Si_{0.7}Ge_{0.3}$ buffer wafers, ten graded layers of 2000Å at 3% Ge steps were deposited. Hence, the graded region was 2µm thick, followed by a 1.5µm thick relaxed n-$Si_{0.7}Ge_{0.3}$. The details of the growth conditions and the characterization of the

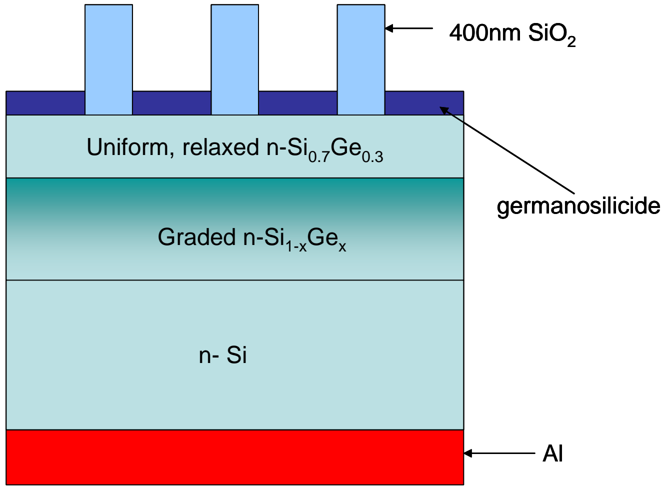


Fig. 1. Schematics of final NiSiGe/SiGe Schottky diode structure. Similar NiSi/Si Schottky diodes were fabricated

relaxed SiGe films can be found elsewhere [12-14]. n-Si(100) wafers with a resistivity of 4~8Ω/sq wafers were also included for the study.

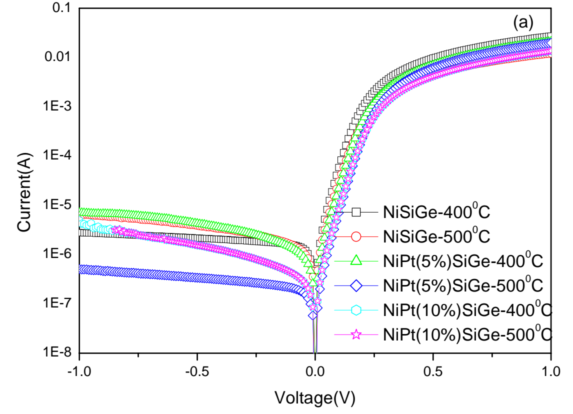
The relaxed n-$Si_{0.7}Ge_{0.3}$(100) samples were cleaned by piranha, while the n-Si(100) wafer was cleaned by the standard RCA solution, followed by HF dip. Then a 400nm thick oxide was deposited on the samples, followed by patterned lithography to create circular areas of $6.6\times10^{-3}cm^2$. After dipping in diluted BHF to remove the oxide on the exposed substrate area, both patterned SiGe and Si were immediately loaded into a sputtering machine with a base pressure of 5×10^{-7} Torr, and about 100 Å thick Ni(Pt) films were deposited onto the wafers at a deposition rate of 2 Å/s at deposition pressure of about 3×10^{-3} Torr. These samples were rapid thermal annealed at 400 and 500ºC for 60s in a N_2 ambient, respectively. Unreacted metals were etched by piranha. About 3000Å Al was deposited on the backside of those wafers by thermal evaporation to create an ohmic contact. I-V measurements were carried out by a computer controlled system, consisting of a HP 4155A semiconductor parameter analyzer, K-20 programmable temperature controller, and cryostat.

III. RESULTS AND DISCUSSION

Figure 1 shows schematically a final NiSiGe/SiGe Schottky diode cross-sectional structure. Similar NiSi/Si Schottky diodes were also fabricated. It has been reported that the full NiSi and NiSiGe can be formed at 400 and 500°C [9].

Figures 2(a) and 2(b) show the semi-logarithmic I-V curves of Ni(Pt=0, 5, 10 at. %)SiGe/SiGe and NiSi/Si annealed at 400 and 500^{0}C, respectively. For the Ni(Pt=0, 5, 10 at. %)Si/Si Schottky diodes, the reverse leakage current decreases ~1 order with the addition of Pt in the Ni(Pt) alloy. In addition, the ideality factor is lower than 1.08, which shows better interface morphology.

In addition, there is no apparent annealing temperature effect on the electrical performance of the diodes. However for the



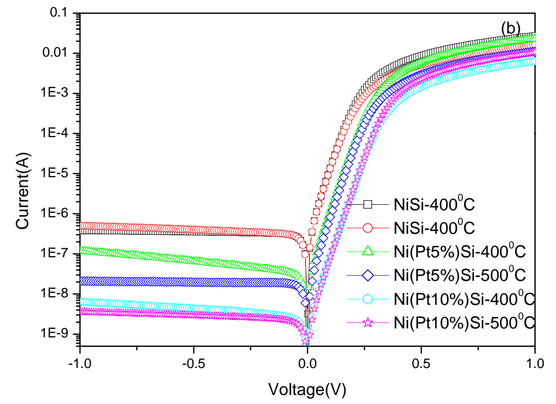


Fig. 2. I-V curves of (a) NiPtSiGe/SiGe and (b)NiPtSi/Si Schottky diode annealed at 400 and 500ºC, respectively.

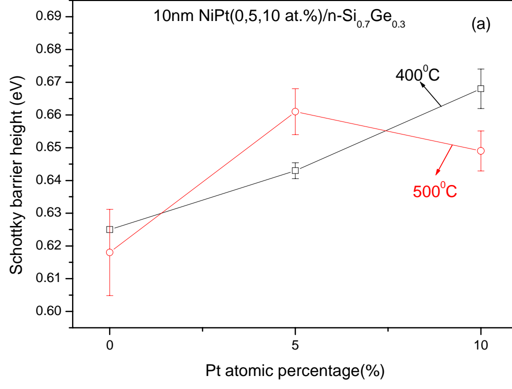
Ni(Pt)SiGe/SiGe Schottky diodes, higher leakage current is obtained compared to the corresponding Ni(Pt)Si/Si Schottky diode. The increased leakage current is possibly attributed to a change of the bandgap of the substrate. With the increase of the Pt atomic percentage, leakage current also decreases but it is not as dominant as in the NiPtSi/Si diode. The ideality factor of Ni(Pt)SiGe/SiGe is slightly larger than that of the pure NiPtSi/Si diode, which shows the relatively rough interface morphology due to the addition of Ge.

The experimental I-V data are analyzed using the thermionic emission model with the series resistance ignored [15].

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{1}$$

$$I_0 = AA^*T^2 \exp\left[\frac{-q\phi_{ms}}{kT}\right] \tag{2}$$

Where I_0 is the saturation current corresponding to zero bias, A denotes the effective device area, A^* is the effective Richardson constant, q is the elementary charge, k is the boltzman constant,



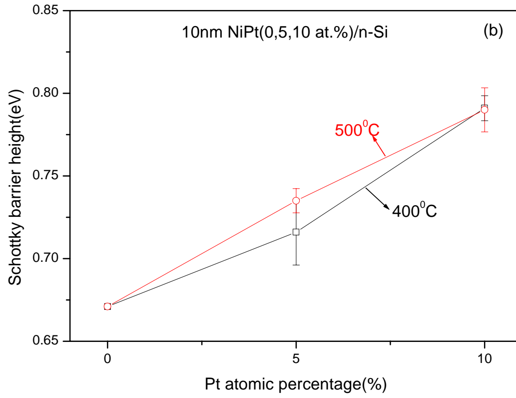


Fig. 3. SBH of (a) NiPtSiGe/SiGe and (b) NiPtSi/Si Schottky diode annealed at 400 and 500°C, respectively.

ϕ_{ms} is the zero-bias barrier height, T the temperature and n is ideality factor. In order to determine the barrier height, A, A^*, T, and I_0 should be known. It is generally assumed that A^* linearly depends on the Ge content [16]. For pure n-Si and n-Ge, A^* is 112 and 50 A/cm^2K^2, respectively [17]. As a result, A^* of n-$Si_{0.7}Ge_{0.3}$ is about 93.4 A/cm^2K^2. Using equation (1), I_0 can be extracted after plotting log (I) versus V. This is only valid for v>>kT/q. So equation (1) is sometimes expressed as follows [15].

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{-qV}{kT}\right)\right] \qquad (3)$$

Plotting log(I/(1-exp(-qV/kT)) against V can gives a linear curve till v=0. The current axis intercept of the straight line portion of the plot for V>>IR_s (R_s denotes the series resistance) gives the saturation current I_0. The barrier height can then be calculated using equation (4),

$$\phi_{ms} = \frac{kT}{q} LN\left(\frac{AA^*T^2}{I_0}\right) \qquad (4)$$

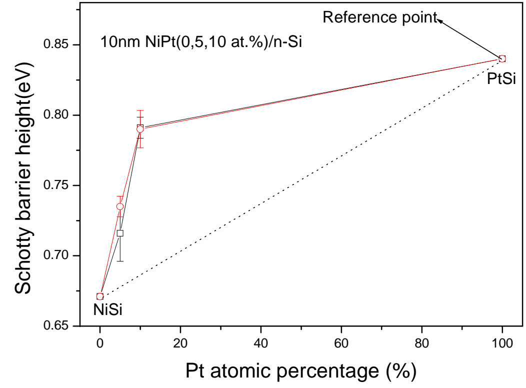


Fig. 4. SBH of NiPtSi/Si Schottky diode annealed at 400 and 500°C, respectively. PtSi is reference point.

At the same time, the ideality factor can be calculated from the slope of the straight line.

Figures 3(a) and 3(b) show the change of the Schottky barrier height values with annealing temperature and Pt atomic percentage. It is clear that SBH increases with the addition of Pt atomic percentage in the alloy films and there is no apparent effect of the annealing temperature on the Schottky barrier height. As reported, the barrier heights of Ni silicide and Pt silicide on n-type Si are about 0.67 and 0.84eV [17], respectively. It would be expected that Ni(Pt) alloy silicide will give a barrier height value between the pure Ni and the pure Pt silicide. For the SiGe substrate, the assumption is also anticipated. But for the NiPtSi/Si diodes, SBH increases rapidly with the addition of Pt in the NiPt alloy. Figure 4 gives the change of Schottky barrier height with an increasing Pt atomic percentage. Here we use PtSi as a reference point with a SBH equal to 0.84eV. With the addition of 10% Pt, the SBH is about 0.8 eV, a 0.13eV higher than the original 0.67 eV. The change in the SBH due to the addition of Pt is more prominent for the Si substrate. It is possible that the addition of 15~20 at.% Pt can increase the barrier height to 0.84eV or even higher than that of the pure PtSi. However, for NiPtSiGe/SiGe, the SBH change is only about 0.04eV even for a 10% inclusion of Pt. The small barrier height difference by the addition of Pt suggested that the Fermi level could have been pinned by interface states, which is used to explain a similar barrier height phenomenon in pure Pd and Pt on SiGe, respectively [18].

The I-V-T characteristics of the NiPtSiGe/SiGe diodes were also studied in detail. Figures 5(a)-(c) show the forward I-V curves of the Ni(Pt=0, 5, 10 at.%)SiGe/SiGe diodes annealed at 400°C for a measuring temperature range of 300 to 93K. The thermionic emission model is again used to analyze the forward I-V curves, but a series resistance Rs was included as a larger range of the forward bias was studied. The equation is expressed as [17]:

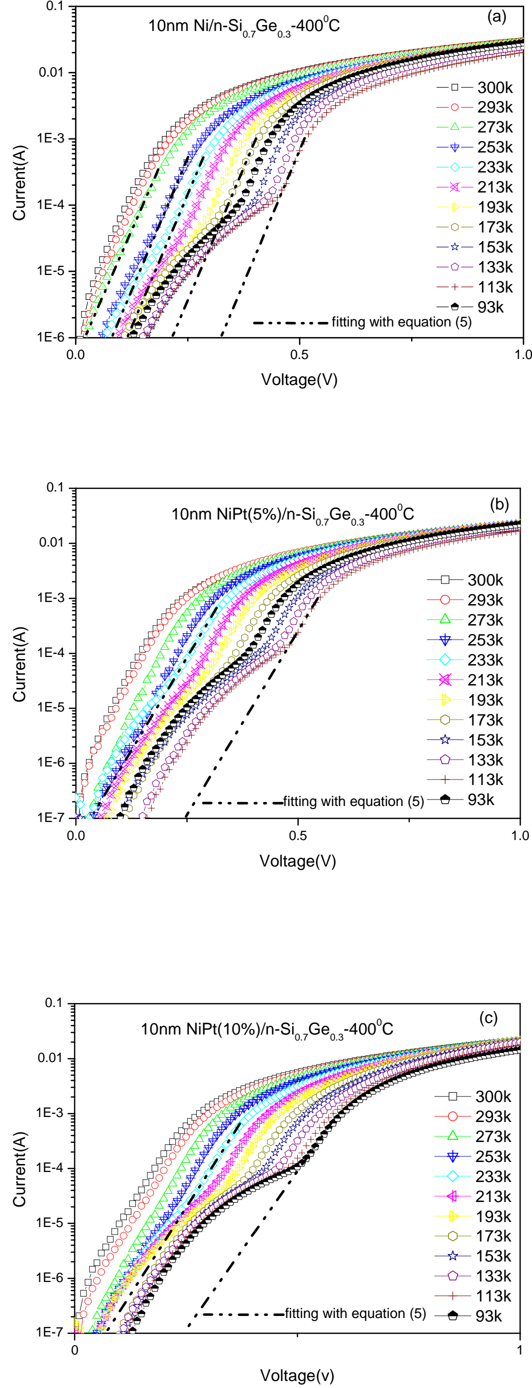


Fig. 5. The forward I-V characteristics of (a) NiSiGe/SiGe and (b) Ni(Pt5at.%)SiGe/SiGe and (c) Ni(Pt10at.%)SiGe /SiGe Schottky contacts annealed at 400°C.

$$I = I_0\left\{\exp\left[\frac{q(V - IR_s)}{nkT}\right] - 1\right\} \quad \text{for V>>3kT/q} \tag{5}$$

For the Ni(Pt=0, 5, 10 at.%)SiGe/SiGe diodes, as shown in Figs. 5(a)-(c), the experimental data matched well with the thermionic emission model for the higher temperature of >253k or for the larger bias region at lower temperatures of <253k. However, for lower temperatures, there are excess currents at smaller forward bias and the bias range of excess current increases with decreasing of the measured temperature.

The possible reasons of excess current observed are summarized as follows. Firstly, it could be related to tunneling current. As what we have known, quantum mechanical tunneling through the barrier may have a significant effect on the I-V characteristics measured at a low temperature and with high doping densities. As the measured temperature decreases, the reduction in the current component due to the tunneling mechanism is not as fast as the thermionic emission current, leading to an excess current. For the tunneling phenomenon, the critical energy is [17]:

$$E_{00} = 18.5 \times 10^{-15}\left(\frac{N_d}{\varepsilon_r m_n^* / m_0}\right)^{1/2} \tag{6}$$

Where N_d, ε_r, m_n, m_0 are the doping density, the relative permittivity of substrate, the effective mass of electron, the mass of free electron, respectively. E_{00} is ~1×10^{-3} eV. When E_{00} is roughly equal to KT, tunneling current is dominant. However, for measured temperature equal to 113 or 93K, KT is about 9.8 or 8 $\times 10^{-3}$ eV, which are larger than E_{00}. In addition, for pure NiPtSi on lightly doped Si diodes, the excess current is also observed. So it is expected that tunneling current is not significant in our experiments.

Secondly, the edge effect could be another possible mechanism. But since there is no apparent size and perimeter effect found on the current [19], so edge induced excess current is not the mechanism responsible for what we observed.

Thirdly, generation/recombination current in the space charge region (SCR) possibly contributes to the excess current because a higher ideality factor is observed in the I-V curves.

Finally, the excess I-V current under lower forward bias at lower temperature <253k is often explained by the barrier height inhomogenity [20-22]. According to the pinch-off model[20], the forward currents mainly include both current over the contact region with a uniform SBH(I_{TE}) and current through some small patches with lower SBH($I_{patch}(\gamma_i)$). The current through the small patches is dominant only at small bias and low measurement temperature. The total current can be expressed as:

$$I_{total} = I_{TE} + \sum_i c_i I_{patch}(\gamma_i) \tag{7}$$

Where c_i denotes the number of patches with a parameter of γ_i. γ_i indicates the extent of the barrier height inhomogenity, which is related to the size of the patches. For the pure NiSiGe/SiGe contact, shown in Fig. 5(a), a relatively apparent excess current occurs at 253K, however, the same extent of the excess current

occurs at 233k for the contact using the NiPt(5, 10 at.%) alloy, as shown in Fig. 5(b) & (c). Hence, the extent of the SBH inhomogenity change is roughly same.

IV. CONCLUSION

The electrical characteristics of Ni(Pt=0, 5, 10 at.%) germanosilicide/n-SiGe and silicide/n-Si are investigated in detail. The Schottky barrier heights of Ni(Pt)SiGe/SiGe and NiPtSi/Si are calculated using a traditional thermionic emission model. With the addition of Pt, the barrier height increases dominantly for Ni-silicide contact on Si, however, the change of SBH is smaller for Ni-germanosilicide contact on SiGe substrate. The forward I-V curves of the NiPtSiGe/SiGe contacts from measured between the room temperature and 93k are explained by a combination of a thermionic emission model and recombination/generation current or inhomogenity of SBH due to patches. Based on a pinch-off model, it is found that the starting temperature of the SBH induced inhomogenity is slightly reduced with the addition of Pt.

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