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SYNTHESIS OF GERMANIUM NANOCRYSTALS AND ITS POSSIBLE APPLICATION IN MEMORY DEVICES

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ABSTRACT

A novel method of synthesizing and controlling the size of germanium nanocrystals was developed. A tri-layer structure comprising of a thin (~5nm) SiO_2 layer grown using rapid thermal oxidation (RTO), followed by a layer of Ge+SiO_2 of varying thickness (6 - 20 nm) deposited using the radio frequency (r.f.) co-sputtering technique and a SiO_2 cap layer (50nm) deposited using r.f. sputtering, was investigated. It was verified using TEM that germanium nanocrystals of sizes ranging from 6 – 20 nm were successfully fabricated after thermal annealing of the tri-layer structure under suitable conditions. The nanocrystals were found to be well confined by the RTO SiO_2 and the cap SiO_2 under specific annealing conditions. The electrical properties of the tri-layer structure have been characterized using MOS capacitor test devices. A significant hysteresis can be observed from the C-V measurements and this suggests the charge storage capability of the nanocrystals. The proposed technique has the potential for fabricating memory devices with controllable nanocrystals sizes.

1. INTRODUCTION

Flash EEPROM (Electrically Erasable and Programmable Read Only Memory) are presently one of the most popular forms of non-volatile memories. Conventionally, nonvolatility in the form of 10-year data-retention time can be achieved by making the tunnel oxide thickness of these devices to be greater than 7nm. However, by incorporating a thick tunnel oxide, it greatly compromises the write and erase speeds of these devices [1]. In order to overcome the limitation imposed by the tunneling oxide thickness, some memory devices used the hot-electron injection mechanism to improve the write speed. However, the erase speed is still limited by the low tunneling current through the tunnel oxide [2].

It has recently been demonstrated that memory cells containing nanocrystals embedded within the gate dielectric improves on the performance limitation of a conventional floating gate device [3]. The advantages (e.g., low programming voltages and improved retention time) of replacing a conventional floating gate with nanocrystals created a great interest in this area. The syntheses of nanocrystals within the gate dielectric have been demonstrated in the form of silicon, germanium or tin nanocrystals formed through the ion implantation technique [3,4,5]. However, there exist limitations in the ion implantation technique. These include the minimal requirement for the control (cap) oxide thickness and also the possibility of degrading the tunnel oxide quality through the implantation process. Another method of synthesis of germanium (Ge) nanocrystals has been demonstrated through a sequence of thermal oxidation of $Si_{1-x}Ge_x$ at various temperatures [6].

In this paper, a tri-layer structure, which mimics the conventional floating gate oxide, is synthesized through RTO and co-sputtering techniques. Germanium nanocrystals of controllable sizes were successfully synthesized through annealing and the manipulation of the thicknesses of the various layers in the tri-layer structure. The charge storage capability of the germanium nanocrystals was also investigated.

2. EXPERIMENT

The samples consist of a novel tri-layer insulating configuration in a typical metal-insulator-semiconductor structure (MIS). The tri-layer insulating structure consists of a 5nm thick tunnel oxide grown on (100) p-type silicon (Si) substrate. This oxide was grown using rapid thermal oxidation (RTO) and was carried out using an AST SHS 10 rapid thermal processor. RTO was performed at 1000^oC for 30s in an O_2 ambient to obtain the desired oxide thickness. A middle layer of varying thickness, containing silicon dioxide (SiO_2) and Ge, was then cosputtered using an Anelva radio frequency (r.f.) sputtering system (SPH-210H) in argon ambient. The target for this process was prepared by attaching six pieces of Ge (10 x 10 x 0.3mm^3 each) on a 4-inch SiO_2 target and cosputtered at 3 x 10^{-3} Torr with the r.f. sputtering power set at 100W. Finally, a capping SiO_2 layer of 50nm was sputtered using pure SiO_2 (99.999% pure) target, employing the same sputtering conditions as previously stated. The samples then underwent rapid

thermal annealing at 1000°C for 300s in an inert argon ambient. Aluminum of 600nm thickness was evaporated on top of the insulating structure to form the MIS structure. Circular capacitor structures of 180μm diameter were then defined using photolithography.

Capacitance-voltage (C-V) measurement was carried out using a HP4284A LCR meter and high resolution transmission electron microscope (HRTEM) analysis was used to obtain cross-sectional images of the samples.

3. RESULTS AND DISCUSSION

Table 1 shows the different types of tri-layer structures that were used in the study and for comparison in the discussion.

Table1: *Structures of different tri-layer devices*

Device	Layer 1	Layer 2	Layer 3
A	5nm RTO	20nm SiO_2+Ge	50nm SiO_2
B	5nm RTO	20nm SiO_2	50nm SiO_2
C	5nm RTO	20nm SiO_2+Ge	No capping
D	5nm RTO	6nm SiO_2+Ge	50nm SiO_2

In order to determine the electrical characteristics of the different devices, capacitance versus voltage (C-V) characteristics for these devices before and after RTA were determined. Figure 1 shows the after-annealing C-V characteristics of devices A, B and C (refer to Table 1 for the tri-layer structure).

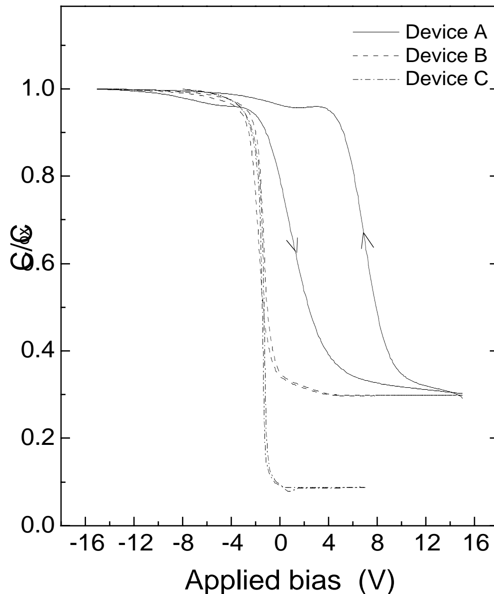

Figure 1: *C-V characteristics of devices A, B and C.*

From the C-V curve of device A, it can be seen that device A exhibits a counter-clockwise hysteresis with width of approximately 6V. This result shows a great difference as compared to the C-V characteristics (not shown) of unannealed device A, which exhibits negligible hystersis. From Figure 1, it can also be seen that device B, which contains a middle layer of 20nm thick pure sputtered SiO_2, shows a much smaller counter-clockwise hysteresis of 0.73V. An unannealed device B has also being fabricated and similar C-V measurement showed a hysteresis of 1.09 V. This implies that the RTA process has improved the sputtered oxide quality and has reduced the trapped charge density of device B from 3.62 X 10^{11} cm^{-2} (as-prepared) to 1.98 X 10^{11} (after RTA) cm^{-2}. This also suggests that the large hysteresis exhibited by device A is due to charge storage in the Ge nanocrystals located at the middle layer in device A. The presence of Ge nanocrystals in the middle layer is shown in the HRTEM results on device A in Figure 2.

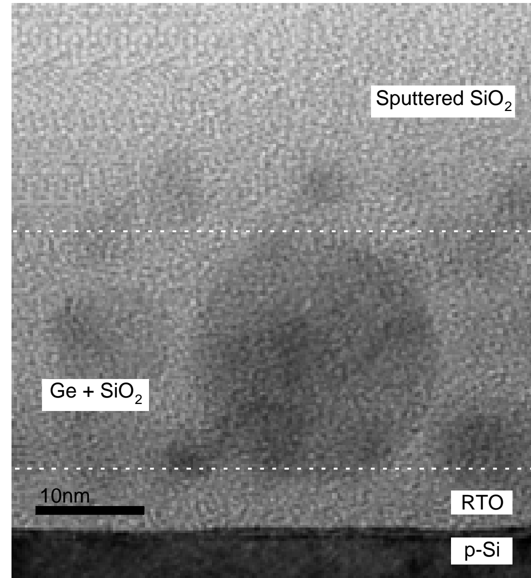

Figure 2: *Transmission electron micrograph of the trilayer structure that was rapid thermal annealed at 1000°C for 300s. The trilayer structure consists of 5nm of rapid thermal oxide, 20nm of co-sputtered Ge+SiO_2 layer and a 50nm of pure sputtered SiO_2 (device A).*

As can be seen from the micrograph in Figure 2, nanocrystals of sizes ranging from 6nm to 20nm were formed. It can clearly be noted that the largest nanocrystals are well confined by the RTO and capping oxide layer. In addition, Ge nanocrystals of diameter 6nm can be seen to form at the RTO SiO_2-sputtered Ge+SiO_2 and the sputtered Ge+SiO_2–pure sputtered oxide interfaces. Heinig *et al.* [7] suggested that as the concentration of Ge dissolved in SiO_2 is lower than the solubility at the Si-SiO_2 interface and higher in the bulk of the oxide, the concentration gradient can lead to a diffusion flux, resulting in an accumulation of Ge at the interface. Another possible reason for accumulation of Ge at these interfaces may be thermodynamically driven.

Formation of nanocrystals at these interfaces reduces the interfacial energy between the interfaces and hence is more favorable thermodynamically as compared to formation of nanocrystals in the middle of the sputtered layer.

It can also be seen from Figure 1 that C-V measurement for device C exhibits no significant hysteresis. A possible explanation for this is that during the reduction process of GeO_2 and GeO_x at high temperature to Ge, a dominant reactive process that might happen is the partial reduction of GeO_2 and GeO_x into GeO, which is volatile. As such, if there is an absence of the capping oxide layer, Ge may escape from the surface of the wafer. This implies that there will be fewer Ge within the middle layer to be able to cluster together to form elemental germanium nanocrystals. This may explain why sample C exhibits a poorer charge storage capability as there may be less charge trapping centers to store the injected charges. This is supported by the cross sectional TEM sample for device C shown in Figure 3.

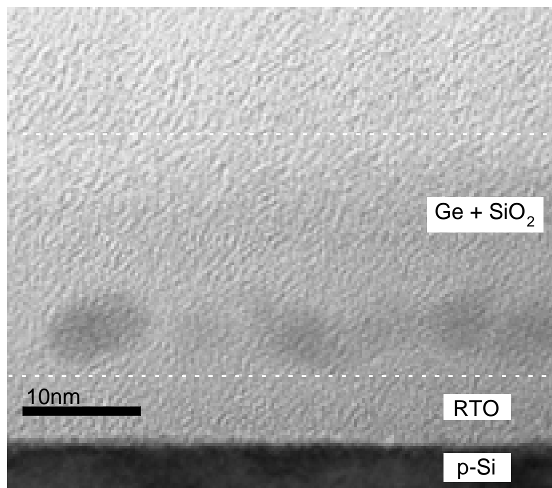

Figure 3: *Transmission electron micrograph of the two-layered structure that was rapid thermal annealed at 1000°C for 300s. The two-layered structure consists of 5nm of rapid thermal oxide and 20nm of co-sputtered Ge+SiO₂ layer (device C).*

From the TEM micrograph for device C shown in Figure 3, it can be noted that there is a reduction in the number of nanocrystals and an absence of Ge nanocrystals at the top of the middle layer, which suggests a substantial escape of Ge through GeO in the annealing process.

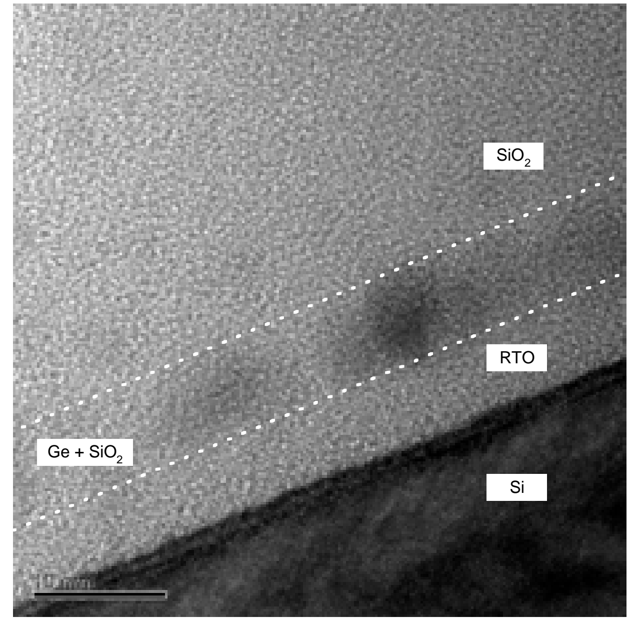

Figure 4: *Transmission electron micrograph of the trilayer structure that was rapid thermal annealed at 1000°C for 300s. The trilayer structure consists of 5nm of rapid thermal oxide, 6nm of co-sputtered Ge+SiO_2 layer and a 50nm of pure sputtered SiO_2 (device D).*

Figure 4 shows a TEM micrograph of device D. From the TEM micrographs for device A and device D, it can be seen that for both samples, the maximum size of the nanocrystals formed are well confined by the RTO oxide, as well as the capping oxide layer, for the given annealing conditions. This gives an indication that different sizes of nanocrystals can be formed in a similar fashion under certain annealing conditions. In fact, it can be seen from the TEM micrograph for device D that the sizes of germanium nanocrystals are relatively more uniform with most of the nanocrystals having a size of 6nm as compared to device A which has varying sizes of nanocrystals. This result encourages the use of a thinner middle layer since it enables the formation of more uniformly sized nanocrystals.

Incidentally, smaller size nanocrystals should exhibit better retention as storage nodes. The charge retention condition requires that the Coulomb energy of the system should be much higher than the thermal energy. The Coulomb energy increases with decreasing radius of the storage node and is given as $q^2/2C_{tt}$. C_{tt} is the capacitance of the nanocrystal or storage node and is inversely proportional to the linear dimension or radius of the nanocrystal [8]. This would be further investigated using capacitance versus time measurements in future experiments.

4. CONCLUSION

Different sizes of Ge nanocrystals were successfully fabricated using the tri-layer structure that has been proposed. It is verified using HRTEM that there is a good correlation between the middle layer thickness and the maximum size of the nanocrystals formed during the annealing process. It has also been shown that the charge storage capability of the tri-layer is due to the presence of Ge nanocrystals within the system.

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