SiGe-On-Insulator (SGOI) Technology and MOSFET Fabrication

Zhiyuan Cheng, E. A. Fitzgerald, and D. A. Antoniadis

Abstract – In this work, we have developed two different fabrication processes for relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) substrates: (1) SGOI fabrication by etch-back approach, and (2) by "smart-cut" approach utilizing hydrogen implantation. Etch-back approach produces SGOI substrate with less defects in SiGe film, but the SiGe film uniformity is inferior. "Smart-cut" approach has better control on the SiGe film thickness and uniformity, and is applicable to wider Ge content range of the SiGe film. We have also fabricated strained-Si *n*-MOSFET's on SGOI substrates, in which epitaxial regrowth was used to produce the surface strained Si layer on relaxed SGOI substrate, followed by large-area *n*-MOSFET's fabrication on this structure. The measured electron mobility shows significant enhancement (1.7 times) over both the universal mobility and that of co-processed bulk-Si MOSFET's. This SGOI process has a low thermal budget and thus is compatible with a wide range of Ge contents in $Si_{1-x}Ge_x$ layer.

Keywords – strained-Si, SiGe, SiGe-on-Insulator, SGOI, SOI, MOSFET, mobility, bonding, etch-back, etch-stop, smart-cut, hydrogen implantation.

I. Introduction

Relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) is a very promising technology, as it combines the benefits of two advanced technologies: the conventional SOI technology and the SiGe technology. SiGe-based devices have shown advantageous dc and rf performance using the enhanced electronic properties associated with strain engineering and heterojunction energy barriers. For example, it has been shown that enhanced carrier transport makes strained Si on relaxed SiGe a promising candidate for improving the performance of CMOS technology [1]. It is also of interest to develop SiGe-based devices in an SOI configuration, obtaining advantages associated with an insulating substrate, such as reduced parasitic capacitances, improved isolation, and reduced short-channel-effect. In addition, relaxed SGOI is very promising for low power RF application in 10 to 30 GHz region, as the insulating substrate results in less signal crosstalk and less power loss while still enhances the tradeoff of speed-power product. Relaxed SGOI is also a versatile substrate that can be used to integrate various device structures, such as strained-Si and strained-SiGe FETs, and III-V optoelectronics. Several research groups have reported work on a relaxed $Si_{1-x}Ge_x$-on-insulator structure [2-8]. Much of this work has concentrated on relaxed $Si_{1-x}Ge_x$-on-insulator substrates fabricated using the separation by implantation of oxygen (SIMOX) technology [2-4]. In that process, a high dose oxygen implant is used to bury high concentrations of oxygen in a $Si_{1-x}Ge_x$ layer, which is then converted into a buried oxide (BOX) layer upon annealing at high temperature (for example, at 1350 ^oC). The quality of the resulting $Si_{1-x}Ge_x$ film and the buried oxide layer is a concern in such processes. In addition, Ge segregation during high temperature annealing also limits the maximum Ge composition to a low value [2-4]. Another method reported [5-8] is to deposit an initially strained $Si_{1-x}Ge_x$ layer on an ultra-thin SOI substrate and then transfer the strain to the underlying thin Si layer at high temperature. In this case the SOI substrate was used as a "compliant substrate".

In this work, we have investigated SGOI substrate fabrication via two different approaches: etch-back [9] and "smart-cut" [10]. We also demonstrate strained-Si *n*-MOSFET's on relaxed SGOI (25% Ge) with electron mobility enhancement of approximately 1.7 times compared to unstrained Si control devices [9].

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II. SGOI Substrate by Etch-back

SGOI substrates were fabricated via two differenct approaches, etch-back and smart-cut. The substrate fabrication process is shown schematically in Fig. 1 and Fig. 2 respectively. In the etch-back approach, starting with a 4-inch Si

(100) donor wafer, high quality relaxed SiGe was grown at 900 ºC by UHVCVD using a graded $Si_{1-x}Ge_x$ buffer technique [11]. The Ge content *x* was graded from zero to 25% with a grading rate of 10% Ge/μm. A 2.5 μm-thick undoped, relaxed $Si_{0.75}Ge_{0.25}$ cap layer was deposited, as shown in Fig. 1(a). The slow grading rate and high growth temperature result in a completely relaxed cap layer with threading dislocation densities of ~10^5 cm^{-2} [12].

The as-grown relaxed $Si_{1-x}Ge_x$ layer has a surface roughness of around 11 to 15 nm, due to the underlying strain fields generated by misfit dislocations at the graded layer interfaces. Thus chemical-mechanical polishing (CMP) was used to smooth the surface. After a cleaning step to render the surface highly hydrophilic, the doner wafer was fliped over bonded to an oxidized Si handle wafer at room temperature, and then annealed at at 850 ºC for 1.5 hrs, as schematically shown in Fig. 1 (a). The bonded pair was then ground to remove the donor wafer substrate, as shown in Fig. 1(b). The wafer was then subjected to a TMAH solution to etch away the SiGe graded layer until SiGe with 20% Ge was exposed. A key factor in this wet etch process is the use of 20% SiGe as a natural etch stop. It has been shown that $Si_{1-x}Ge_x$ with Ge content greater than 20% is an excellent etch stop for various etchants (KOH, TMAH, and EPD), with selectivity better than the conventional p^{++} etch stop [13]. The structure was further thinned by CMP to expose the relaxed $Si_{0.75}Ge_{0.25}$ layer, and a relaxed SGOI substrate results.

Fig. 3(a) shows the infrared image of a typical SGOI substrate with 25% Ge content. The fringes in the infrared image reflect the non-uniformity of the SiGe film. The non-uniformity results mainly from the two CMP steps in the process.

III.SGOI SUBSTRATE BY "SMART-CUT"

The "smart-cut approach" is shown schamatically in Fig. 2. Before bonding, hydrogen ions (50~200 keV, 5E16~1E17 H^+/cm^2) was implanted into the relaxed SiGe cap layer of the donor wafer. The implanted hydrogen creates micro-bubbles in a certain depth determined by the implantation energy, Fig. 2(a). After bonded to an oxidized Si handle wafer, it was annealed at 400~600ºC. During the anneal, the bonded pair split at the buried hydrogen-rich layer, leading to the desired layer transfer of relaxed SiGe. A final 850ºC anneal improved the bond strength. Fig. 3(b) shows a 4-inch SGOI substrate prepared by "smart-cut" approach.

To investigate the surface of the as-transferred SGOI substrate, transmission electron microscopy (TEM) and atomic force microscopy (AFM) were used. The TEM cross-section view in Fig. 4(a) shows that a ~640 nm thick $Si_{0.75}Ge_{0.25}$ layer was transferred onto the top of a 550 nm thick buried oxide (BOX) in a typical SGOI substrate. Surface damage is also shown clearly at the splitting surface. Fig. 4(b) shows a surface roughness of 11.3 nm in an area of 5x5 μm^2 by AFM for the as-transferred SGOI, which is similar to the surface roughness reported for as-transferred silicon film by "smart-cut" processes [15-16]. The TEM and AFM results suggest that a top layer of about 100 nm should be removed by a final touch CMP step.

The advantage of "smart-cut" approach, compared to etch-back approach, is that the thickness and uniformity of the transferred SiGe film can be controlled well. Nevertheless, the "smart-cut" approach tends to give higher defect density on the SiGe film, typically in the range of 20/cm^2. We have observed one new faceted defects on SiGe film by "smart-cut" approach, which show characteristics of having ractangle crystal graphic shape and large size in the several hundred μm range. These defects were not observed in both the co-processed Si-on-insulator films using same "smart-cut" process and the co-processed SiGe-on-insulator films using etch-back process. This suggests that these new defects may originate from the epi defects present in SiGe growth and the formation of these new defects is related to the "smart-cut" process. Detail investigation is under progress. Growing an oxide layer on the SiGe donor wafer before implantation and bonding, could be one possible solution to reduce those defects.

IV. MOSFET'S FABRICATION ON SGOI

Large-area ring structure strained-Si *n*-MOSFET's were fabricated on the SGOI substrate prepared by etch-back approach. First, 100 nm p-type (doping 10^{16} cm^{-3}) relaxed $Si_{1-x}Ge_x$ was grown on the SGOI substrate at 850 °C, followed by 8.5 nm-thick undoped strained-Si layer grown at 650°C, as shown in Fig. 1(c). Large-area, ring structure *n*-MOSFET's were then fabricated utilizing a short-flow one-mask MOSFET process developed in this lab [14]. The gate stack consists of 300 nm LTO deposited via LPCVD at

400°C, and 50 nm of poly-Si deposited at 560°C. This large thickness of LTO gate dielectric facilitates the one-mask process, as described below. Capacitors fabricated with LTO in this lab have demonstrated interface state densities on par with thermal oxides (~5_10^{10} cm^{-2} eV^{-1}) [14]. The measured fixed oxide charge density is about $2.4x10^{11}$ cm^{-2}. The gate stack was then patterned and etched into ring MOSFET structures in the only lithography step. A key step is the use of buffered oxide etchant (BOE) to undercut the gate polysilicon, forming a large "T-gate" geometry. Arsenic ion implants (35 keV, total dose $1x10^{15}$ cm^{-2}) were performed to dope both the source/drain and gate regions at 4 perpendicular directions with a 7º tilt to extend the S/D region under the T-gate structure. The dopant was activated via RTA at 1000°C for 1 s. Because the strained-Si layer was in equilibrium, no relaxation via misfit dislocation introduction occurred. Blanket Ti/Al metallization was then performed via e-beam deposition at perpendicular incidence. Due to the extreme geometry of the "T-gate" FET structure and large gate LTO thickness, breaks occur in the metal which isolate the source, gate, and drain regions without further lithography. Two control structures were also co-processed: conventional bulk Si MOSFET's and strained-Si MOSFET's on relaxed bulk SiGe substrates which are identical to the donor wafer shown in Fig. 1(a).

The TEM photograph in Fig. 5 shows the structure of the finished strained-Si, surface channel *n*-MOSFET's on the relaxed SGOI substrate.

V. Device Characterization and Electron Mobility Enhancement

Some pieces of the finished wafer were used to conduct Triple-axis X-ray Diffraction Scans and EPD (etch pit density) experiments. The results show that both transferred and regrown SiGe films on SGOI were completely relaxed and the dislocation density was less than $8x10^5$ /cm^2, in the range of the bulk SiGe buffer. The EPD experiment showed no visible misfit dislocation between the top Si film and the relaxed SiGe layer, suggesting that the top Si film was strained.

The large square ring structure *n*-MOSFET's (L = 200 μm, ring perimeter = 4 x 250 μm) were used to evaluate the electron mobility as a function of vertical field. The effective electron mobility μ_{eff} was extracted from the linear regime device current, $\mu_{eff} = (L_{eff}/W_{eff})\ I_{DS} / [C_{ox}(V_{GS}-V_T)V_{DS}]$, where V_{DS} = 0.1 V. Taking into consideration the transistor's ring geometry, (W_{eff}/L_{eff}) was replaced by the appropriate geometry factor G = 0.138, obtained by numerical solution of the Laplace equation using MEDICI [14]. The oxide capacitance $C_{ox} = \varepsilon_{ox} / t_{ox}$ was obtained from C-V measurements on the same device, and the oxide thickness t_{ox} = 326 nm was also extracted. The effective vertical field E_{eff} is given by $E_{eff} = (Q_b + Q_{inv}/2) / \varepsilon_S$. Because of the uncertainties in the strained-Si/$Si_{0.75}Ge_{0.25}$ doping, the bulk depletion charge Q_b was not computed from the usual $N_A x_{d,max}$ approximation. Instead, Q_b was extracted from $E_{ox}\varepsilon_{ox} = Q_{inv} + Q_b$, where E_{ox} is the electric field in the gate oxide. As a result, the effective field can be approximated by $E_{eff} = [E_{ox}\varepsilon_{ox} - Q_{inv}/2] / \varepsilon_s$. The inversion charge Q_{inv} was taken as $C_{ox}(V_{GS}-V_T)$. E_{ox} was assumed to be equal to V_{GS}/t_{ox}, which holds under the conditions of strong inversion and $V_{GS} >> V_{DS}$, when the potential difference between the strongly-inverted Si surface and the S/D regions is negligibly small compared with the large potential drop across the thick gate oxide.

The measured μ_{eff} as a function of E_{eff} is shown in Fig. 6. The mobilities of two controls are also shown in the figure for comparison. Since all three devices have the same geometry and were processed simultaneously, possible errors due to factors such as the extraction of the ring geometry factor, and approximations in E_{eff} evaluation do not impact the relative comparison of the electron mobility characteristics. In addition, the measured mobility for the CZ Si control device is close to the universal mobility curve [17]. The measured electron mobility enhancement for strained Si MOSFETs fabricated on SGOI, compared to the mobility of co-processed bulk Si MOSFET's is significant (~1.7 times). In addition, the electron mobilities are comparable for devices fabricated on SGOI and bulk relaxed SiGe layers, demonstrating that the superior mobility performance introduced by the strained-Si channel is retained in this SGOI structure. This enhancement factor of 1.7 is consistent with

previously reported experimental and theoretical values for strained-Si *n*-MOSFETs on bulk relaxed SiGe films [18].

V. CONCLUSION

In summary, we have demonstrated fabrication of 4-inch diameter relaxed SiGe-on-insulator (SGOI) substrates, using a combination of UHVCVD $Si_{1-x}Ge_x$ heteroepitaxial growth and layer transfer by hydrogen-induced delamination or etch-back utilizing 20% SiGe layer in the grade buffer as a natural etch stop. We also have demonstrated long-channel strained-Si MOSFET's fabricated in SGOI with a high Ge content of 25%. The measured electron mobility for strained-Si *n*-MOSFET's fabricated on SGOI is significantly higher than both the universal mobility and that of co-processed bulk Si MOSFET's. In contrast to the SIMOX process, where the high annealing temperature limits the Ge content to a low level, this new SGOI process has a low thermal budget and thus is compatible with a wide range of Ge contents in $Si_{1-x}Ge_x$ layer.

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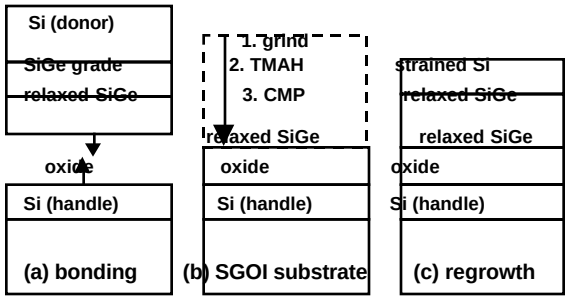


Fig. 1. SGOI fabrication processes via etch-back approach and relaxed-SiGe/strained-Si regrowth.

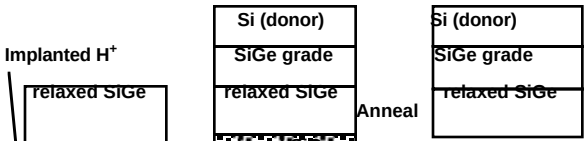
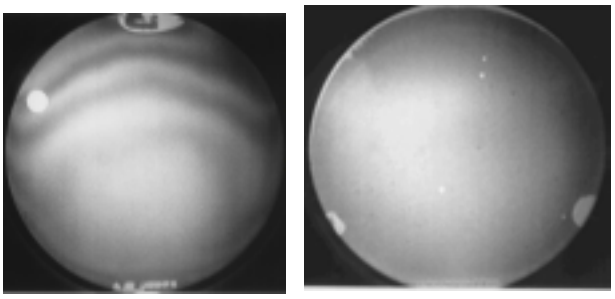
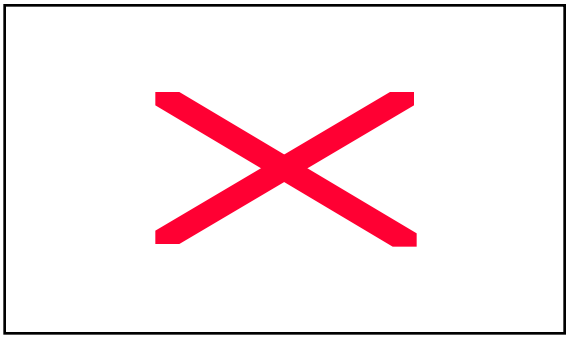


Fig. 2. SGOI fabrication processes via "smart-cut" approach.



(a) by etch-back (b) by "smart-cut"

Fig. 3. 4-inch SGOI substrates fabricated via (a) etch-back appoach, and (b) "smart-cut" approach



(a) TEM (b) AFM image

Fig. 4. As-transferred relaxed $Si_{0.75}Ge_{0.25}$-on-insulator substrate by "smart-cut" approach: (a) TEM cross-section view, and (b) AFM image, showing a surface roughness of 11.3 nm in an area of 5x5 μm^2.

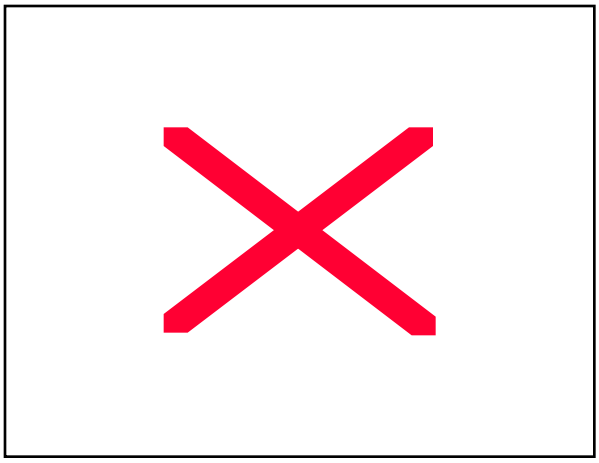


Fig. 5. TEM photograph of the finished strained-Si surface channel MOSFET's fabricated on relaxed $Si_{0.75}Ge_{0.25}$-on-insulator (SGOI) substrate.

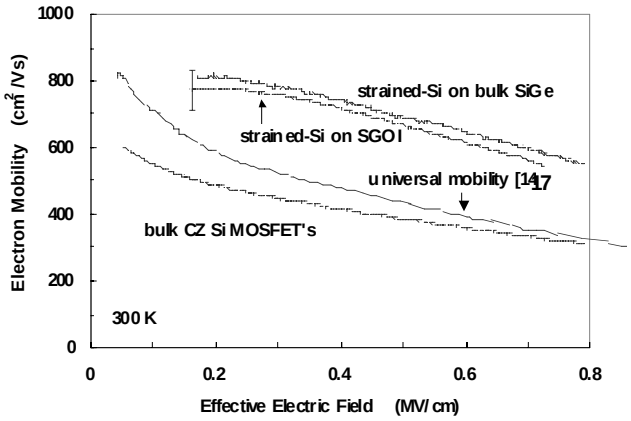


Fig. 6. Measured effective electron mobility vs. effective electric field. The error bar represents the variation among devices. The universal mobility from [17] is also shown for comparison.

Picture

Zhiyuan Cheng obtained B. Eng in Electronic Engineering in 1990 from Tsinghua University and Ph.D. in Electrical Engineering in 1999 from National University of Singapore. He is now a post-doc in MIT, working on SiGe technology.

Picture

Eugene A. Fitzgerald

Picture

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