View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by DSpace@MIT

INVESTIGATION OF THE FUNDAMENTAL RELIABILITY UNIT FOR CU DUAL-DAMASCENE METALLIZATION

C. L. Gan[1,*], C. V. Thompson[1,2], K. L. Pey[1,3], W. K. Choi[1,3], F. Wei[2], S. P. Hau-Riege[4], R. Augur[5], H. L. Tay[6], B. Yu[6] and M. K. Radhakrishnan[6]

1 Advanced Materials for Micro- and Nano- Systems Programme, Singapore-MIT Alliance, 4 Engineering Drive 3, Singapore 117576.
2 Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139.
3 Department of Electrical & Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117576.
4 Intel Corp., now with Lawrence Livermore National Laboratory, USA.
5 International Sematech, Inc., Austin, Texas 78741, USA.
6 Institute of Microelectronics, 11 Science Park Road, Singapore 117685.

[*]Phone: (65) 874-2144, E-mail: smap9050@nus.edu.sg

ABSTRACT

An investigation has been carried out to determine the fundamental reliability unit of copper dual-damascene metallization. Electromigration experiments have been carried out on straight via-to-via interconnects in the lower metal (M1) and the upper metal (M2), and in a simple interconnect tree structure consisting of straight via-to-via line with an extra via in the middle of the line (a "dotted-I"). Multiple failure mechanisms have been observed during electromigration testing of via-to-via Cu interconnects. The failure times of the M2 test structures are significantly longer than that of identical M1 structures. It is proposed that this asymmetry is the result of a difference in the location of void formation and growth, which is believed to be related to the ease of electromigration-induced void nucleation and growth at the Cu/Si_3N_4 interface. However, voids were also detected in the vias instead of in the Cu lines for some cases of early failure of the test lines. These early failures are suspected to be related to the integrity and reliability of the Cu via.

Different magnitudes and directions of electrical current were applied independently in two segments of the interconnect tree structure. As with Al-based interconnects, the reliability of a segment in this tree strongly depends on the stress conditions of the connected segment. Beyond this, there are important differences in the results obtained under similar test conditions for Al-based and Cu-based interconnect trees. These differences are thought to be associated with variations in the architectural schemes of the two metallizations. The absence of a conducting electromigration-resistant overlayer in Cu technology allows smaller voids to cause failure in Cu compared to Al. Moreover, the Si_3N_4 overlayer that serves as an interlevel diffusion barrier provides sites for easy nucleation of voids and also provides a high diffusivity path for electromigration. The results reported here suggest that while segments are not the fundamental reliability unit for circuit-level reliability assessments for Al *or* Cu, vias, rather than trees, might be the appropriate fundamental units for the assessment of Cu reliability.

I. INTRODUCTION

Several kilometers of metal interconnects are used to construct each single Si-based high-performance integrated circuit [1]. In each circuit, millions of metal segments exist and these elements are a great reliability concern due to electromigration-induced failures. Current design rules and practices usually attempt to be overly conservative to ensure that a circuit is immune to electromigration-induced failures. In order to optimize the performance for each generation of technology while maintaining a high overall reliability, a new design methodology is needed to more accurately account for the effects of circuit layout on the risk of generating electromigration-induced failure.

Presently, most modeling and experimental analyses on circuit level interconnects focus on straight stud-to-stud test structures. However in reality, multiple segments of straight-lines are connected at junctions in laid-out integrated circuits. An "interconnect tree" has been defined as a unit of continuously connected high-conductivity metal lying within one layer of metallization [2-3]. Existing circuit-level reliability assessment methods are based on breaking up trees into individual segments and assessing the reliability of each segment separately, using the results from straight via-to-via test lines. This method is generally inaccurate as materials within the tree can diffuse freely between the segments, and the stress evolution in the different segments is coupled. Hau-Riege *et al.* have demonstrated that an interconnect tree is the appropriate fundamental reliability unit for circuit-level assessments of the reliability of Al-based metallization [3].

One key difference between electromigration in Al and Cu interconnects is that grain boundaries provide the highest-

diffusivity paths for electromigration in polycrystalline Al lines, while in Cu metallization, the Cu/liner or Cu/Si_3N_4 interfaces provide an even higher diffusivity path than the grain boundaries [4-8]. It also seems likely that the Cu/Si_3N_4 interface provides a site for void nucleation at relatively low tensile stresses. These differences are important because they are the determining factors for the locations and modes of electromigration-induced failure.

In this paper, we compare the failure characteristics of straight via-to-via test structures in first (M1) and second (M2) layers of metallization, which differ only in the direction of electron flow at their cathode-ends. Furthermore, we report on the electromigration studies on dual-damascene Cu-based dotted-I interconnect tree structures, stressed under different current configurations, as previously done earlier for Al [3].

II. EXPERIMENTS

Test samples were fabricated using a Cu dual-damascene process, both in the Institute of Microelectronics, Singapore (IME) and International Sematech Inc., USA. At IME, a 13500Å-thick dielectric stack of SiO_2 / Si_3N_4 / SiO_2 was first deposited onto a Si wafer using plasma-enhanced chemical vapor deposition (PECVD) at 400°C. A trench was etched down to a Si_3N_4 etch stop for the first level of metallization (M1). Next, a 250Å-thick Ta diffusion barrier and 2000Å-thick Cu seed layer were sputter-deposited into the trench before electrodeposition of Cu. After chemical-mechanical polishing (CMP), a 14000Å-thick inter-layer dielectric (ILD) stack consisting of Si_3N_4 / SiO_2 / Si_3N_4 / SiO_2 was deposited before patterning the second level of metallization (M2). M2 was formed using a dual-damascene process and the respective thickness of the M1 and M2 Cu lines was approximately 3400Å and 2400Å after CMP. After patterning the second level of metallization, a Si_3N_4 / SiO_2 dielectric stack was deposited as passivation. The bond pads were opened and a layer of Al was deposited and patterned over the bond pads to improve the quality of wire bonds. The dice were packaged in ceramic packages and Au wires were used to connect the bond pads to package lead frames. At IME, the samples were stressed in an Xpeqt electromigration test system at a temperature of 350°C. Package level testing was also carried out at Sandia National Labs and Intel Corp.

Three test structures were designed and fabricated as shown in Figure 1. In the M1 structures, the tested Cu line was in the first layer of metallization and was narrower than the two lines in the second layer of metallization that connect to the M1 line at the vias at either end. The M2 structure is identical except that the narrow line terminating at dual-damascene vias is in the second layer of metallization. A variation of the test structure shown in Figure 1 has four vias in a 2 x 2 array at the end of the test lines. In this case, the ends of the test lines were widened to accommodate the additional vias. M1 and M2 test structures with different line widths, lengths, and number of vias were tested at current densities between 2.3 and 3.6 MA/cm^2.

The third test structure is the dotted-I interconnect tree, which was in the second level of metallization and was electrically connected to the bond pads through much wider M1 connectors. This design allows currents of different magnitudes and directions to be applied independently in the two segments.

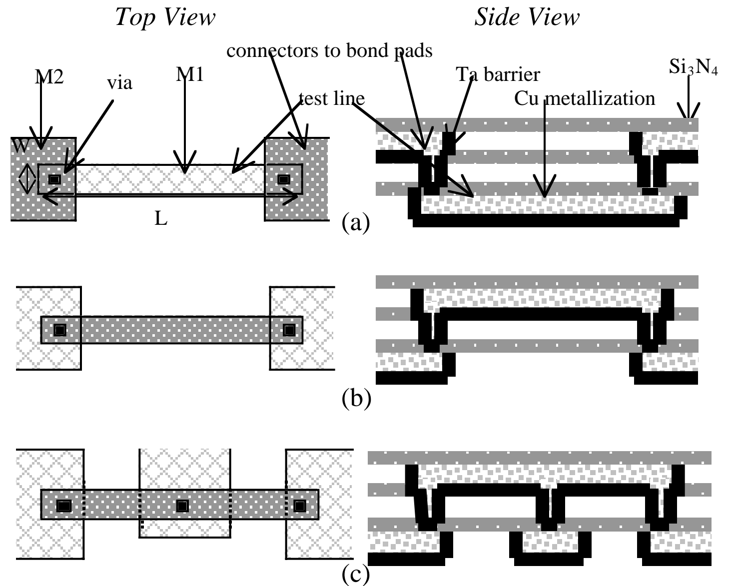


Fig. 1: Schematic diagrams of top and side views of a (a) M1 test structure, (b) M2 test structure, (c) dotted-I test structure.

III. EXPERIMENTAL RESULTS

A lognormal plot of the failure times for 800μm-long, 0.28μm-wide single via and 1.0μm-wide 4-via, M1 and M2 structures is shown in Figure 2. The median-times-to-failure (t_{50}'s) from tests on paired populations of M1 and M2 structures are tabulated in Table I. Figure 2 and Table I both show large variations in the measured lifetimes, suggesting the operation of multiple failure mechanisms. However, for a variety of line widths, lengths, and number of vias, the measured t_{50}'s of the M2 structures are consistently larger than those of the M1 structures.

Physical analysis of some of the failed structures was carried out using focused-ion-beam (FIB) microscopy, which allows both ion beam sputtering for sectioning of vias and

Table I: Test results for populations of M1 and M2 test structures with various physical characteristics. The structure label indicates the metallization level of the test line (e.g., level 2 for M2_1) and the number of vias at the end of the test line (e.g. 4 for M2_4). t_{50} is the measured median time to failure, including unfailed lines, and σ is the standard deviation of the natural log of the failure times, excluding unfailed lines.

Structure	Length (μm)	Width (μm)	j (MA/cm^2)	t_{50} (mins.)	σ	% unfailed lines (test time in mins.)

M1_1	800	0.28	2.5	1720	1.07	6.7 (28731)
M2_1	800	0.28	2.5	6420	1.53	6.3 (28731)
M1_1	800	1.0	2.3	204	0.53	0 (10163)
M2_1	800	1.0	3.6	480	1.16	0 (10163)
M1_4	800	0.28	2.3	5604	0.42	0 (19018)
M2_4	800	0.28	3.6	16002	2.21	50 (19018)
M1_4	800	1.0	2.5	3200	0.72	0 (11473)
M2_4	800	1.0	2.5	7516	0.17	0 (11473)
M1_1	100	0.28	2.5	1230	0.85	6.3 (11541)
M2_1	100	0.28	2.5	7370	1.54	27.3 (26065)
M1_1	50	0.28	2.3	1248	1.48	12.5 (9937)
M2_1	50	0.28	3.6	4122	1.58	31.3 (9937)

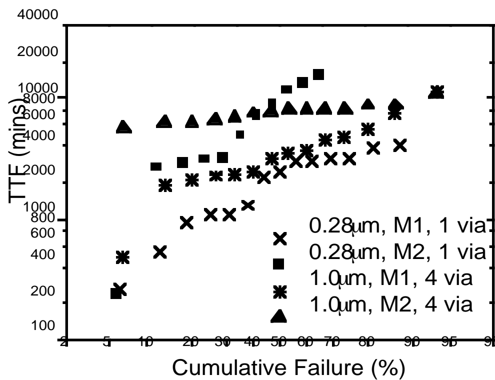


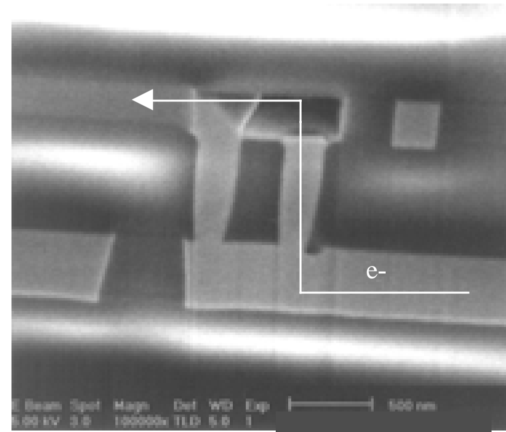
Fig. 2: Times-to-failure for 800μm-long, 0.28μm-wide single-via and 1.0μm-wide 4-via, M1 and M2 test structures stressed at 350°C and 2.5 MA/cm^2. The data show that M2 structures are more reliable and are more likely not to fail after very long test times.

imaging using ion-induced secondary electrons, as well as transmission-electron-microscopy (TEM) for investigation of the integrity of the Ta liner after testing. Figure 3(a) shows an FIB image of the cathode end of a M2 structure that terminated with 4 vias. The length and width of the structure is 800μm and 0.28μm, respectively. The sample was stressed at 350°C and 3.6 MA/cm^2 until it failed as an open circuit. The void formed at the top surface of the M2 line and grew in length (along the line) as well as thickness. Figure 3(b) shows the anode end of a different 4-via M2 structure. This test line was 800μm long and 0.28μm wide and was also stressed at 350°C and 3.6 MA/cm^2. However, in this case failure took a much longer time and it can be seen that voids formed in the much wider metal 1 connector at the anode end of the M2 test line, where the tensile stress was very large *in the M1 connector*. As can be seen from these figures, the voids tend to form at the Cu/Si_3N_4 interface even in the wider connector lines held at much lower current densities.

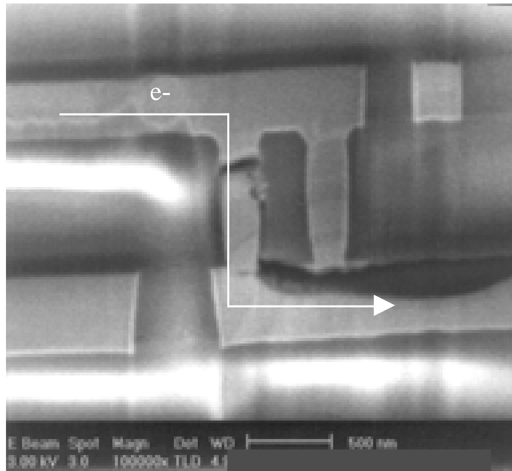
The lognormal distributions shown in Figure 2 indicate multiple failure mechanisms. During physical characterization, some voids were detected in the via instead of in the line. Figure 4 shows competing failure mechanisms as observed in a 800μm-long, 1.0μm-wide 4-via-terminated M2 structure. Voids are seen both at the bottom of a via and in the M2 Cu line. A TEM image of one of the vias showed that void nucleation started from the side of the via at the bottom, where the Ta liner was virtually absent (Figure 5).

Five different current configurations were tested on a 0.28μm-wide and 500μm-long dotted-I structure as shown in Figure 6(a). Figure 6(b) shows the lognormal distribution of the times-to-failure (TTF) of the dotted-I structures tested at 350°C, with a constant current density of j_{e1} = 2.5 MA/cm^2 in the left limb, and a current density with varying direction and magnitude, j_{e2}, in the right limb. Failure was defined as the minimum time for a 30% increase in the resistance in either one of the segments in the test structure. The lognormal plots indicate that the lifetime of the test structure depends on the current configuration in the right segment, with t_{50} increasing from case (v) to case (i). Similar values of t_{50} were obtained for case (v) in the Sematech samples.

Failure analysis was also carried out on selected stressed dotted-I structures to study the failure mechanisms. Figures 7(a) and (b) are FIB images of the failure sites on a representative subset of the samples that was stressed with



(a)



(b)

Fig. 3: (a) FIB image of voids formed at the surface at the cathode end of a 800μm-long, 0.28μm-wide 4-via M2 line in a M2 test structure. (b) Cross sectional view of voids at the surface of a wide M1 connector to a 800μm-long, 0.28-μm wide 4-via M2 line in a M2 test structure. Voiding occurred at the cathode of the M1 connector and the anode of the M2 test line. Samples were stressed at T = 350°C and j = 3.6 MA/cm^2. The arrows indicate the direction of electron flow.

configurations (ii) and (v) respectively, as indicated in Figure 6(a). Figure 7(a) shows that the electrons flow from M1 into the left segment of M2 only. However, a void had formed in the via and extended into the *right* limb, where no current was flowing during stress. In Figure 7(b), the void that had formed in the middle via, extended into both the left and right segments above the via. In this case, the electrons were flowing from M1 through the middle via into both M2 limbs. However, in both cases, the voids have resulted in an open failure of the test structure.

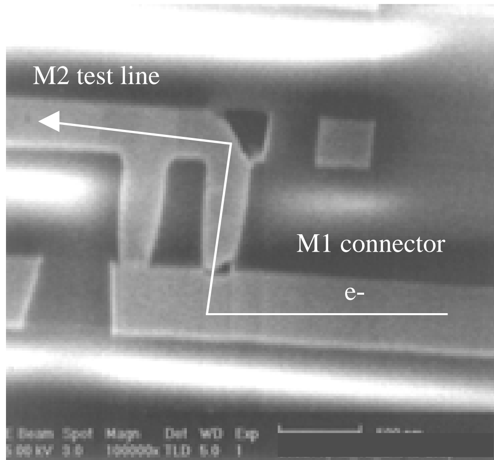


Figure 4: FIB image of voids in both the M2 line and bottom of a via at the cathode end of a 800μm-long, 1.0μm-wide 4-via M2 test structure. The sample was stressed at T = 350°C and j = 3.6 MA/cm^2.

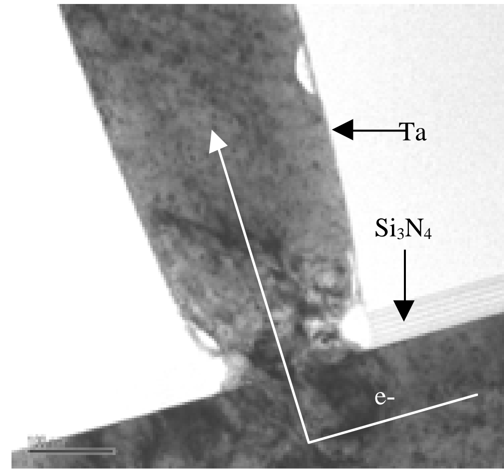
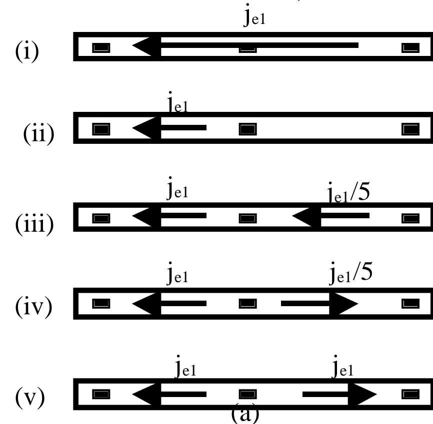


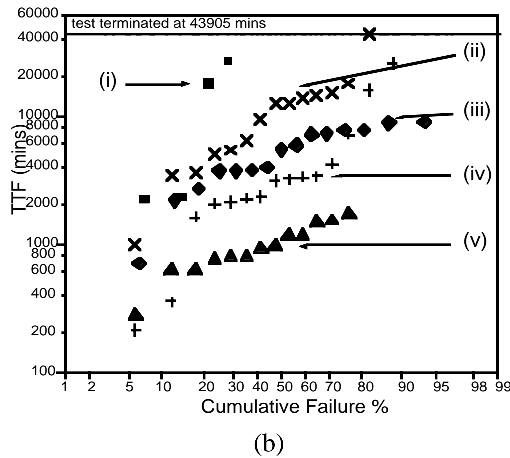
Figure 5: TEM image of voids nucleated at the sides of the bottom of a via, at the Cu/Si_3N_4 interface.

IV. DISCUSSION

A. M1 and M2 Structures

From the physical characterization and electrical results, we postulate that the observed asymmetry in the reliability of the M1 and M2 structures is related to the ease of nucleation and growth of electromigration-induced voids at the Cu/Si_3N_4 interface [9]. A similar asymmetry in the reliability of vias stressed with opposite current directions has also been observed in Al-based interconnects, and has been attributed to differences in locations for void nucleation [10]. During Cu electromigration, a tensile stress develops at the cathode ends of the lines, where the Ta liner forms a blocking boundary to the diffusing Cu [11-12]. If the critical tensile stress for void nucleation is reached, a void forms. In the M2



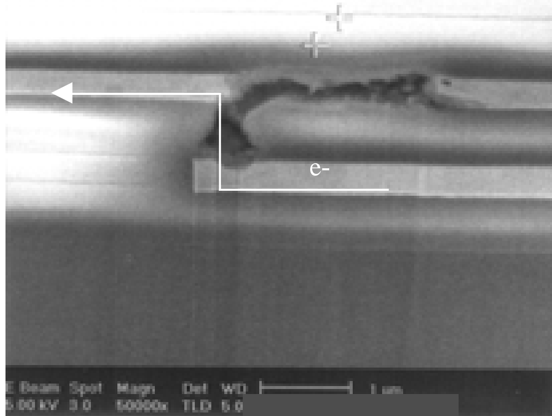


(b)

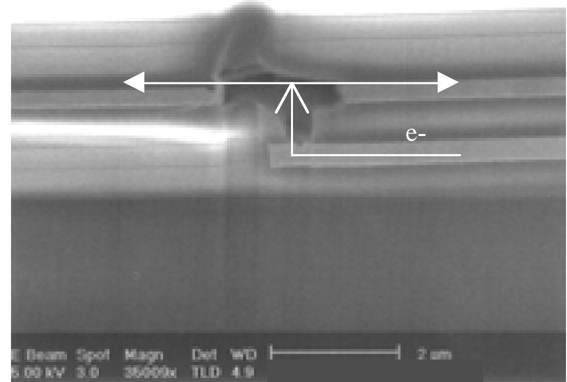
Fig. 6: (a) Schematics of dotted-I test structures with five different current configurations used in the experiments. Tests were carried out at T = 350°C and j_{e1} = 2.5 MA/cm^2. The arrows show the direction of electron flow. (b) Times-to-failure for 500μm-long, 0.28μm-wide dotted-I structures with different electron current configurations as shown in (a).

structures, the maximum tensile stress is reached at the base of the vias, where the Cu is bound on all sides by Ta. On the other hand, in the M1 structures the maximum tensile stress develops at the Cu/Si_3N_4 interface near the cathode vias of the metal 1 lines. It has been suggested that the Cu/Si_3N_4 interface provides a faster diffusion path than the Cu/Ta interface [5-7, 13-14]. It also seems likely that the Cu is less adherent to the Si_3N_4 so that there is a lower barrier to void formation at this interface. Thus, for the M2 structures, a void may preferentially nucleate and grow at the Cu/Si_3N_4 interface at the cathode end of the M2 line instead of in the via itself where the tensile stress is expected to be highest.

After a void has nucleated at the Cu/Si_3N_4 interface of the M2 structure, it will initially grow in the direction of the electron flow, resulting in a partially spanning void. As a



(a)



(b)

Fig.7: FIB images of voids in the middle via of a representative failed dotted-I for (a) test condition (ii) and (b) test condition (v). Samples were stressed at T = 350℃ and j = 2.5 MA/cm^2 in each M2 segment.

result, the resistance of the test structure will increase only slightly while there is still a high-conductivity Cu path for current. An open-circuit failure will result only when the void grows to span the whole thickness of the metal line. This forces all the current to flow through the thin Ta liner layer, inducing significant Joule heating in the liner and leading finally to an open circuit failure.

For the M1 structure, voids will preferentially nucleate at the Cu/Si_3N_4 surface near the cathode end of the M1 line. As such voids grow, even a partially spanning void can block current through the via since the Si_3N_4 does not provide a conducting path to shunt current as seen in Figure 3(b). Thus, a much smaller void volume is required for failure of the M1 structures than the M2 structures, resulting in longer lifetimes for the M2 structures, and even in the observation of damage in the wider metal 1 connectors for M2 test structures.

Ogawa *et al.* [15] have also reported the observation of voids in vias of lines that had failed early. They attributed this phenomenon to processing defects. From our TEM analysis of the lines that failed very early, poor sidewall coverage in the high aspect-ratio via (~10%) during Ta sputter deposition may cause insufficient sidewall coverage in some of the vias, possibly resulting in Cu being in direct contact with the Si_3N_4 layer. Moreover, as the tensile stress at the bottom of the via at the cathode end of a M2 line is maximum, the sidewall liner of a "weak" via may rupture under electromigration stress. With the Cu/ Si_3N_4 as the preferential void nucleation interface, a void may form rapidly. This mechanism may occur simultaneously with the normal void formation at the Cu/Si_3N_4 interface at the surface of the M2 line as observed in Figure 4. Since a much smaller volume of Cu is needed to block the current in a via than in the line, the time-to-failure will also be much shorter of voiding that occurs in the via due to insufficient sidewall coverage of the via by the Ta. This may be the reason that voids are observed in the vias of lines that failed early.

B. Dotted-I Structures

The lognormal plot in Figure 6(b) shows that the direction and magnitude of the electron current in the right segment of the dotted-I structure affect the overall reliability of the whole interconnect tree. The t_{50} increases from test configuration (v) to (i), which is different from what was observed in Al metallization [3]. We will discuss each of the five different cases below.

For configuration (v), electrons moved from the middle via to the two outer vias, with the same electron current density in both segments and twice the electron current density in the middle via. With the Ta liners at the bottom of the vias acting as sites for atomic flux divergence, a tensile hydrostatic stress builds up rapidly in the central via until void nucleation occurs. As observed in Figure 7(b), a void had formed in the middle via and in the line just above the middle via where the tensile stress was largest, resulting in simultaneous failure of both the right and left segments.

In case (iv), the current density in the right limb was decreased to 0.5 MA/cm^2 while it was still kept at 2.5 MA/cm^2 in the left limb. Because the copper flux into the right segment was decreased, the time for void nucleation in the middle via also decreased, resulting in an increase in the t_{50} of the structure compared to the previous case.

For configuration (iii), the t_{50} of the dotted-I structure is higher than that in case (iv). In both cases, the right limb of the structure acted as an “active” reservoir of Cu atoms. However in case (iv), the right segment was an active sink for metal atoms, draining more Cu atoms from the central via. On the other hand in case (iii), the right segment was an active source of Cu atoms for the central via, which slowed the rate of increase of the tensile stress in the central via, thus increasing the lifetime of the left limb. In this experiment, it was observed that the lifetime of the right limb (j_{e2} = 0.5 MA/cm^2) was lower than that of the left limb (j_{e1} = 2.5 MA/cm^2). This implies that the electron flow from the right via towards the central via slowed the rate of increase of the tensile stress in the central via to such an extent that the critical stress for void nucleation was reached in the right via first, causing failure of the right segment before the left segment.

In case (ii), the right limb had no current during test and was therefore a “passive” reservoir that acted as a source of Cu atoms for the middle via. This slowed the build-up of tensile stress, increasing the lifetime of the structure compared to cases (v) and (iv). However, the t_{50} for this configuration was lower than that of the left segment in case (iii). In case (iii), we saw that the right segment was acting as an active source for Cu atoms, and therefore suppressed the build-up of tensile stress in the central via even more effectively than in case (ii). As observed from the failure analysis shown in Figure 7(b), a void had formed in the via and extended into the right limb. As a tensile stress develops under the central via, Cu from the “unstressed “ right segment diffuses towards the central via because of the resulting stress gradient. The void therefore grows into the right segment.

For configuration (i), more than half of the samples did not fail after more than 700 hours of stressing. This is different from the results reported for Al-metallization [3]. In the Al dotted-I structure, the lines were terminated in W-vias, which acted as perfectly blocking boundaries to Al atom flow. In our Cu dotted-I structures, an approximately 30Å Ta liner at the bottom of the via is the blocking boundary to the flow of Cu atom. However, the higher stresses that evolved in longer lines could rupture this thin layer of diffusion barrier [16]. If this occurs, the vias no longer act as sites for flux divergence and the lifetime increases substantially [13].

V. CONCLUSIONS

Our results on straight via-to-via lines demonstrate that the direction of current flow through a dual-damascene via must be accounted for in the assessment of the reliability of an integrated circuit fabricated with Cu metallization. Multiple failure modes were also observed from the failure analyses. Voiding readily occurred at the Cu/Si_3N_4 interface at the top of the Cu lines, but also sometimes occurred inside the vias, perhaps also at the Cu/Si_3N_4 interfaces where the sputtered Ta liner was not continuous. In some cases, we postulate that liner rupture can prevent the flux divergences that lead to voiding, resulting in very long lifetimes as Cu flows from large reservoirs to large sinks. The lifetime of a straight via-to-via segment therefore depends on the reliability of the barrier and on the direction of current flow in the Cu metallization scheme.

Our experiments on Cu-based dotted-I interconnect trees showed that the reliability of a given segment tested under the same conditions can be very different, depending on the magnitude and direction of the electron current in the neighboring segments. These differences observed in Cu indicate that segments in a Cu-based interconnect tree are not the fundamental reliability units that must be assessed in circuit-level reliability analysis, as was demonstrated earlier for Al [3]. However, the variations of segment lifetimes with variations in stress conditions in neighboring segments are different in Al and Cu. It is likely that this difference is due to the different architectural schemes of the two metallizations. In Cu technology, unlike Al technology, liner rupture can lead to interactions among trees. Thus, this work suggests that while segments are not the fundamental reliability units for Cu, trees may not be either. The reliability of all segments, trees, and vias are all coupled if vias are not blocking boundaries for electromigration. Because interconnect reliability is related to via reliability in Cu-based interconnect structures, vias may be the most fundamental unit to consider in circuit-level reliability analyses for Cu. However, a computationally manageable and not overly conservative approach for such an analysis is yet to be developed.

ACKNOWLEDGMENTS

This research is supported by the Singapore-MIT Alliance (SMA) and Semiconductor Research Corporation.

C.L. Gan holds an SMA research scholarship. The authors would like to thank S.-M. Chen (currently at Shanghai Huahong) for laying out the test chip, W.K. Ong (IME) for assisting in testing, K. Vaidyanathan and S.C. Chong (IME) for assisting in packaging, S. Koh (IME) for FIB microscopy, and C.-H. Tung and A.Y. Du (IME) for TEM analysis. The authors would also like to thank Lap Chan (Chartered Semiconductor Manufacturing), W.K. Chim, C.M. Ho and W. Lim (NUS) for their technical assistance.

REFERENCES

[1] Semiconductor Industry Association Technology Roadmap, 2001.

[2] S. P. Hau-Riege, and C. V. Thompson, "Electromigration saturation in a simple interconnect tree," *J. Appl. Phys.*, vol. 88, no. 5, p. 2382, 2000.

[3] S. P. Hau-Riege, and C. V. Thompson, "Experimental characterization and modeling of the reliability of interconnect trees," *J. Appl. Phys.*, vol. 89, no. 1, p. 601, 2001.

[4] J. R. Lloyd and J. J. Clement, "Electromigration in copper conductors," *Thin Solid Films*, vol. 262, p. 135, 1995.

[5] C.-K. Hu, R. Rosenberg and K. Y. Lee, "Electromigration path in Cu thin-film lines," *Appl. Phys. Lett.*, vol. 74, no. 20, p. 2945, 1999.

[6] L. Arnaud, G. Tartavel, T. Berger, D. Mariolle, Y. Gobil and I. Touet, "Microstructure and electromigration in copper damascene lines," *Microelectron. Reliab.*, vol. 40, p. 77, 2000.

[7] N. D. McCusker, H. S. Gamble and B. M. Armstrong, "Surface electromigration in copper interconnects," *Microelectron. Reliab.*, vol. 40, p. 69, 2000.

[8] J. Proost, T. Hirato, T. Furuhara, K. Maex and J.-P. Celis, "Microstructure and electromigration-induced drift in electroplated damascene Cu," *J. Appl. Phys.*, vol. 87, no. 6, p. 2792, 2000.

[9] C. L. Gan, C. V. Thompson, K. L. Pey, W. K. Choi, H. L. Tay, B. Yu and M. K. Radhakrishnan, "Effect of current direction on the lifetime of different levels of Cu dual-damascene metallization," to be published in *Appl. Phys. Lett.* Dec. 2001.

[10] L. Kisselgof and J. R. Lloyd, "Electromigration induced failure as a function of via interface," Mater. Res. Soc. Symp. Proc. 473, p. 401, 1997.

[11] P.-C. Wang, G. S. Cargill III, I. C. Noyan, and C.-K. Hu, "Electromigration-induced stress in aluminum conductor lines measured by X-ray microdiffraction," *Appl. Phys. Lett.,* vol. 72, p. 1296, 1998.

[12] R. G. Filippi, G. A. Biery and R. A. Wachnik, "The electromigration short-length effect in Ti-AlCu-Ti metallization with tungsten studs," *J. Appl. Phys.*, vol. 78, no. 6, p. 3756, 1995.

[13] C.-K. Hu, L. Gignac, S. G. Malhotra and R. Rosenberg, "Mechanisms for very long electromigration lifetime in dual-damascene Cu interconnections," *Appl. Phys. Lett.*, vol. 78, no. 7, p. 904, 2001.

[14] E. T. Ogawa, A. J. Bierwag, K.-D. Lee, H. Matsuhashi, P. R. Justison, A. N. Ramamurthi, P. S. Ho, V. A. Blaschke, D. Griffiths, A. Nelsen, M. Breen and R. H. Havemann, "Direct observation of a critical length effect in dual-damascene Cu/oxide interconnects," *Appl. Phys. Lett.*, vol. 78, no. 18, p. 2652, 2001.

[15] E. T. Ogawa, K.-D. Lee, H. Matsuhashi, K.-S. Ko, P. R. Justison, A. N. Ramamurthi, A. J. Bierwag and P. S. Ho, "Statistics of electromigration early failures in Cu/oxide dual-damascene interconnects," *Proc. 39th Int. Reliability Physics Symp.*, p. 341, 2000.

[16] F. Wei, C. L. Gan, C. V. Thompson, S. P. Hau-Riege, J. J. Clement, H. L. Tay, B. Yu, M. K. Radhakrishnan, K. L. Pey and W. K. Choi, "Length effects on the reliability of dual-damascene Cu interconnects," SMA 2nd Annual Symposium, 2002.