

# Modeling Dielectric Erosion in Multi-Step Copper Chemical-Mechanical Polishing

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**Abstract**—A formidable challenge in the present multi-step Cu CMP process, employed in the ultra-large-scale integration (ULSI) technology, is the control of wafer surface non-uniformity, which primarily is due to dielectric erosion and Cu dishing. In contrast with the earlier experimental and semi-theoretical investigations, a systematic way of characterizing and modeling dielectric erosion in both single- and multi-step Cu CMP processes is presented in this paper. Wafer- and die-level erosion are defined, and the plausible causes of erosion at each level are identified in terms of several geometric and physical parameters. Experimental and analytical means of determining the model parameters are also outlined. The local pressure distribution is estimated at each polishing stage based on the evolving pattern geometry and pad deformation. The single-step model is adapted for the multi-step polishing process, with multiple sets of slurry selectivities, applied pressure, and relative velocity in each step. Finally, the effect of slurry-switching point on erosion was investigated for minimizing dielectric erosion in the multi-step Cu CMP. Based on the developed multi-step erosion model, the physical significance of each model parameter on dielectric erosion is determined, and the optimal polishing practices for minimizing erosion in both multi-step and single-step polishing are suggested.

**Index Terms**—Chemical-Mechanical Polishing, Dielectric Erosion, Semiconductor Manufacturing.

## I. INTRODUCTION

THE relentless advances in ultra-large-scale integration (ULSI) technology necessitate the design and fabrication of sub-micron features of higher resolution, denser packing and multi-layer interconnects. The present success in satisfying the stringent specifications is largely due to the excellent local and global planarization

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capabilities of the Cu CMP process. The greatest challenge in Cu CMP, however, is the control of wafer surface non-uniformity primarily due to dielectric erosion and Cu dishing as shown in Fig. 1.

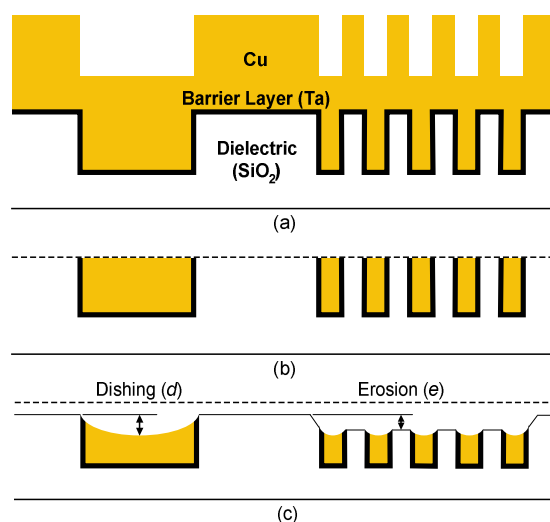


Fig. 1. Schematics of a single-layer Cu interconnect: (a) before polishing (b) ideal case after polishing and (c) real case after polishing.

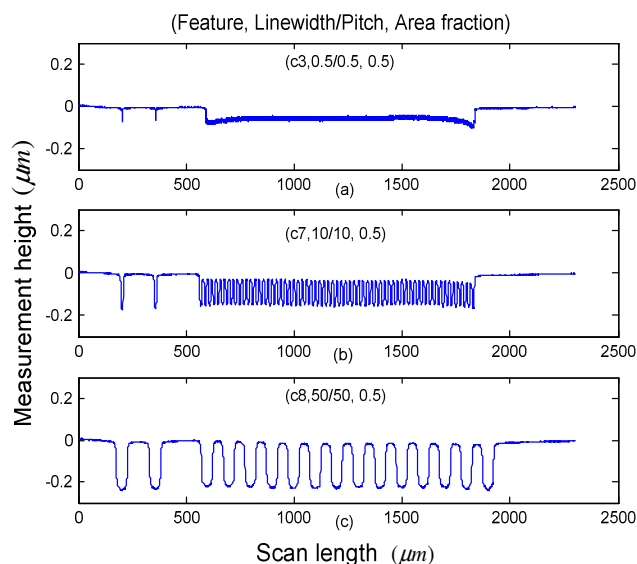


Fig. 2. Dielectric erosion and Cu dishing after single-step Cu CMP for (a) sub-micron, (b) intermediate and (c) global wiring level.

Generally, dielectric erosion is more prevalent than Cu dishing in the dense sub-micron, copper-line region, whereas dishing is more significant than erosion at the global-wiring level, as shown in Fig. 2 [1]. The continual decrease in the width of Cu lines makes it evermore important to characterize and minimize dielectric erosion in Cu CMP.

Past efforts to characterize the relations between dielectric erosion and process parameters have been primarily confined to extensive experimental investigations [2]-[10]. Several semi-theoretical models are available; but such models essentially address single-step polishing and the model parameters are somewhat ad hoc [2]-[5], [11], [12]. The prevailing two- and three-step polishing practices require, however, a clear understanding of the causes of material loss for mitigating both dielectric erosion and Cu dishing.

In this paper, accordingly, a systematic way of characterizing and appropriate modeling of dielectric erosion in single- and multi-step Cu CMP processes are presented. Wafer- and die-level erosion are clearly defined, and the possible causes of erosion at each level are identified in terms of several geometric and physical parameters. Experimental and analytical means of determining the model parameters are also outlined. The local pressure distribution is characterized at each polishing stage based on the evolving pattern geometry and pad deformation. Additionally, the single-step model is adapted for the multi-step polishing process, with multiple sets of slurry selectivities, applied pressure, and relative velocity for each step. Finally, the effect of slurry-switching point is investigated for minimizing dielectric erosion in the multi-step Cu CMP.

## II. THE EROSION MODEL

### A. Basic Modeling Parameters

Material removal rate in CMP is expressed by the celebrated Preston equation [13]:

$$\left| \frac{dh}{dt} \right| = k_p \cdot p \cdot v_R \quad (1)$$

where  $h$  is the thickness of the layer removed,  $t$  the polishing time,  $p$  the nominal pressure,  $v_R$  the relative velocity, and  $k_p$  a constant known as the Preston constant. While the Preston equation represents material removal rate at any point on the wafer, it is often used for estimating the average material removal rate at global level in blanket wafer polishing. In the latter case, the pressure and relative velocity are assumed to be uniform over the entire wafer and that the Preston constant is independent of pressure and velocity [12]. A new dimensionless term  $\chi$  may be introduced as the product of the Preston constant and the

average pressure, which represents the normalized material removal rate.

$$\chi \equiv k_p \cdot p_{av} \quad (2)$$

The normalized material removal rates of blanket Cu, barrier layer and oxide dielectric are thus represented by  $\chi_{Cu}$ ,  $\chi_b$  and  $\chi_{ox}$ . Additionally, the slurry selectivity may be defined as the ratio of the removal rates of two different materials. Thus

$$S_{Cu/ox} \equiv \frac{\chi_{Cu}}{\chi_{ox}} = \frac{k_{pCu}}{k_{pox}}, \quad S_{b/ox} \equiv \frac{\chi_b}{\chi_{ox}} = \frac{k_{pb}}{k_{pox}} \quad (3)$$

Fig. 3 is a schematic of a Cu damascene structure, in which the pattern geometry is represented by two parameters: area fraction, or density, and linewidth of the Cu interconnects in the underlying dielectric trench pattern.  $A_f$  is defined as the mask pattern area ratio of the Cu interconnect line.

$$A_f \equiv \frac{A_{Cu}}{A_{total}} = \frac{w}{\lambda} \quad (0 \leq A_f \leq 1) \quad (4)$$

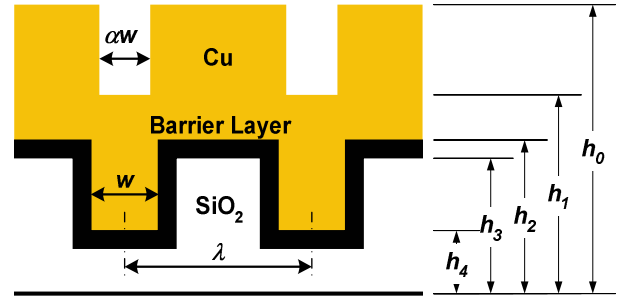


Fig. 3. Definition of pattern geometry in Cu damascene structure, based on the Cu interconnect linewidth,  $w$ , pitch,  $\lambda$ , and Cu deposition factor,  $\alpha$ .

Although the underlying geometry of the damascene structure is defined by  $A_f$  and  $w$ , another factor must be introduced to characterize the topography the Cu-deposited, patterned wafer surface. Due to individual characteristics of the Cu deposition processes, such as physical vapor deposition (PVD) and electroplating, the surface Cu pattern is generally different from the underlying trench pattern, as shown in Fig. 3. It is observed that the surface linewidth is in fact smaller than the underlying Cu interconnect linewidth. The ratio of these two is mainly dependent on the interconnect linewidth. In any case, the Cu deposition factor  $\alpha$  may be defined as:

$$\alpha \equiv \frac{w_{up}}{w_{original}} \quad (0 \leq \alpha \leq 1) \quad (5)$$

When  $\alpha = 0$ , for example, the top surface is flat

regardless of the underlying pattern geometry. When  $\alpha = 1$ , the surface topography is a replica of the underlying trench pattern.

A major problem in Cu CMP, as well as in others, is that the material removal rate is not uniform across the wafer for various reasons: for example, due to non-uniform pressure and velocity distributions, and even the Preston constant. Thus to model the wafer-level non-uniformity in erosion, a new parameter  $\beta$  is introduced, which represents the material removal ratio between two (usually reference) points having the same pattern geometry but in different dies as shown in Fig. 4. Thus  $\beta$  may assume any positive value greater than zero but less than or equal to unity, i.e.,  $0 < \beta \leq 1$ .

$$\beta \equiv \frac{\left| \frac{dh}{dt} \right|_{die1}}{\left| \frac{dh}{dt} \right|_{die2}} = \frac{\chi_{die1}}{\chi_{die2}} \quad (0 < \beta \leq 1) \quad (6)$$

By definition, then, if  $\beta = 1$  the wafer is polished uniformly, but as  $\beta$  decreases the wafer-level non-uniformity increases.

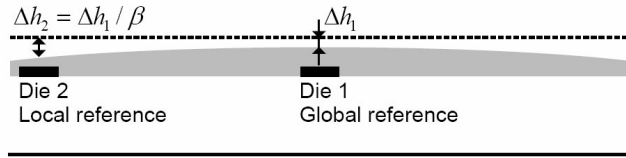


Fig. 4. Definition of wafer-level non-uniformity factor  $\beta$ : Material removal rate ratio of local reference point at each die with respect to the global reference point.

Another factor that needs to be introduced into the erosion model is the local pressure distribution parameter,  $\gamma$ , defined as the ratio of the pressure on a Cu interconnect line to the average pressure on the wafer as shown in Fig. 5. Thus

$$\gamma \equiv \frac{p_{Cu}}{p_{av}} \quad (0 \leq \gamma \leq 1) \quad (7)$$

where,  $p_{av} = F / A_{wafer}$  and  $F$  is the total normal force on the wafer.

At the start of polishing, the pad contacts the peaks of the Cu-deposited wafer and the value of  $\gamma$  is zero, because the space above the Cu line now is a valley and the pad cannot deform to fill in. As the pattern is polished off, i.e., the wafer is planarized, the whole wafer surface supports the normal load, the pressure is uniform, and the  $\gamma$  value is unity. Later, as the pad contacts the diffusion barrier layer,  $\gamma$  starts to decrease from one to zero since the surface is no longer planar. The non-planarity is due to different rates of removal of the barrier layer, dielectric, and the Cu interconnect. The parameter  $\gamma$  now assumes some intermediate values as

determined by dishing, a rigorous analysis of which is beyond the scope of this paper.

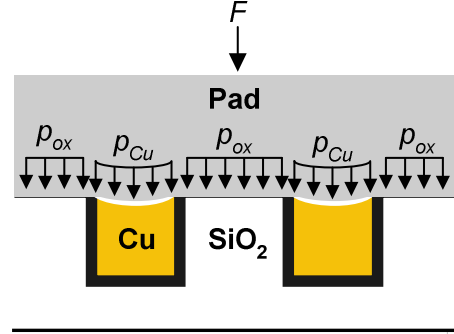


Fig. 5. Definition of local pressure distribution factor  $\gamma$ : As the pad contacts the barrier and dielectric layers,  $\gamma$  starts decreasing from one to zero.

### B. Dielectric Erosion Model for Single-Step Cu CMP

The material removal rate at each height in Fig. 3 is based essentially on the local pressure distribution. Initially, the pad contacts the top of the wafer surface, which is filled with Cu of certain deposit geometry. The local pressure, and hence the material removal rate, at this stage can be calculated by the pattern geometry and average pressure. After the pattern is polished, the material removal rate is the same as that of a blanket Cu wafer. When the barrier and oxide layers are polished,  $\gamma$  affects the local pressure distribution as discussed already. The material removal rates in these regimes are given by:

$$\begin{aligned} h_1 < h \leq h_0 & \quad \left| \frac{dh}{dt} \right| = \frac{1}{\beta} \chi_{Cu} v_R \left( \frac{1}{1 - \alpha A_f} \right) \\ h_2 < h \leq h_1 & \quad \left| \frac{dh}{dt} \right| = \frac{1}{\beta} \chi_{Cu} v_R \\ h_3 < h \leq h_2 & \quad \left| \frac{dh}{dt} \right| = \frac{1}{\beta} \chi_b v_R \left( \frac{1 - \gamma A_f}{1 - A_f} \right) \\ h_4 < h \leq h_3 & \quad \left| \frac{dh}{dt} \right| = \frac{1}{\beta} \chi_{ox} v_R \left( \frac{1 - \gamma A_f}{1 - A_f} \right) \end{aligned} \quad (8)$$

The amount of dielectric erosion at the end of each stage and at the end of the process can be readily calculated by the above equations. Fig. 6 shows a schematic of a time-based erosion model for single-step polishing.

Based on (8), the end-point  $t_{ep}$  for the global reference point, a local reference point, and for a particular feature in any die can be expressed as:

$$\begin{aligned} t_{ep_{global}} &= \frac{h_0 - h_2}{\chi_{Cu} v_R} + \frac{h_2 - h_3}{\chi_b v_R} + \frac{\Delta h_o}{\chi_{ox} v_R} \\ t_{ep_{local}} &= \frac{h_0 - h_2}{\frac{1}{\beta} \chi_{Cu} v_R} + \frac{h_2 - h_3}{\frac{1}{\beta} \chi_b v_R} + \frac{e_1}{\frac{1}{\beta} \chi_{ox} v_R} \end{aligned} \quad (9)$$

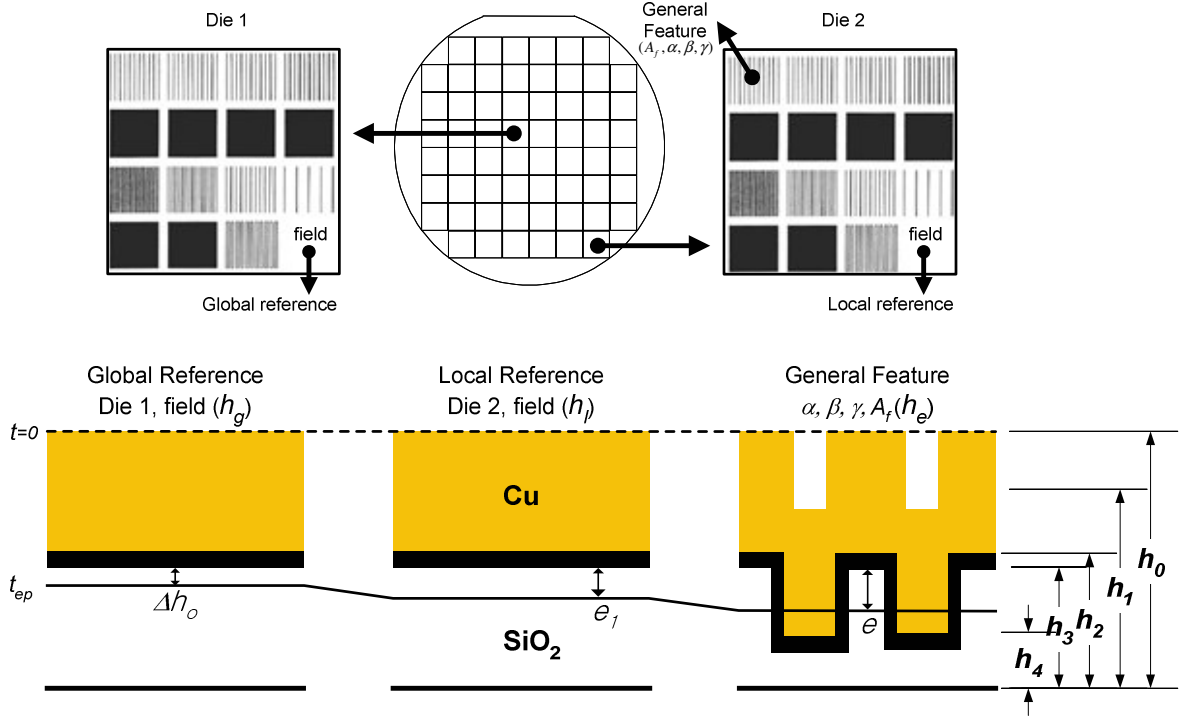


Fig. 6. Schematics of time-based erosion,  $e$ , calculation for general feature in a single-step polishing process when a global reference point is overpolished as the amount of  $\Delta h_o$ .

$$t_{ep_{general}} = \frac{h_0 - h_1}{\frac{1}{\beta} \chi_{Cu} v_R \left( \frac{1}{1 - \alpha A_f} \right)} + \frac{h_1 - h_2}{\frac{1}{\beta} \chi_{Cu} v_R} + \frac{h_2 - h_3}{\frac{1}{\beta} \chi_b v_R \left( \frac{1 - \gamma A_f}{1 - A_f} \right)} + \frac{e}{\frac{1}{\beta} \chi_{ox} v_R \left( \frac{1 - \gamma A_f}{1 - A_f} \right)}$$

where  $\Delta h_o$  is the amount of overpolishing,  $e_1$  is wafer-level erosion, and  $e$  is the total dielectric erosion of any feature.

In this paper, the dielectric erosion is expressed in a dimensionless form  $e^*$ , the ratio between dielectric erosion and the designed Cu interconnect thickness, or the trench depth.

To consider the wafer-level erosion specifically, a local reference point for each die needs to be selected so that the pattern effect can be disregarded. The field, or flat, region in each die with no feature is the logical, local reference point. Thus, wafer-level erosion  $e_1^*$  for the local reference points in each die can be rewritten as:

$$e_1^* = \left( \frac{1}{\beta} - 1 \right) \left[ \frac{1}{S_{Cu/ox}} \left( \frac{h_0 - h_2}{h_3 - h_4} \right) + \frac{1}{S_{b/ox}} \left( \frac{h_2 - h_3}{h_3 - h_4} \right) \right] + \frac{1}{\beta} \left( \frac{\Delta h_o}{h_3 - h_4} \right) \quad (10)$$

Equation (10) shows that three parameters significantly

contribute to wafer-level erosion: the wafer-level non-uniformity factor  $\beta$ , the set of selectivities among Cu, barrier and the dielectric, and the amount of overpolishing,  $\Delta h_o$ , of the global reference point, which usually is the field region of a center die.

By comparing the time  $t_{ep}$  between the local reference and any feature, the total erosion of that feature,  $e^*$ , is expressed as:

$$e^* = \left( \frac{1}{1 - A_f} \right) \left[ \frac{1}{S_{Cu/ox}} (1 - \gamma A_f) \alpha \left( \frac{h_0 - h_1}{h_3 - h_4} \right) + \frac{1}{S_{b/ox}} (1 - \gamma) \left( \frac{h_2 - h_3}{h_3 - h_4} \right) \right] + \left( \frac{1 - \gamma A_f}{1 - A_f} \right) e_1^* \quad (11)$$

Equation (11) shows that several parameters affect the amount of the dielectric erosion in Cu CMP: the area fraction of a feature  $A_f$ , the local pressure distribution factor  $\gamma$ , the interconnect deposition factor  $\alpha$  and the selectivities among the Cu, barrier layer and dielectric. Also, the wafer-level erosion greatly affects die-level erosion if  $\beta$  is not unity.

### C. Dielectric Erosion Model for Multi-Step Cu CMP

Fig. 7 is a schematic of the prevailing end-point, and slurry-switching time, detection technique by the *in situ*, wafer-level, average reflectance measurements in both single- and multi-step polishing processes [14]. When the barrier layer on the fastest die is being exposed ( $t = t_c$ ), the

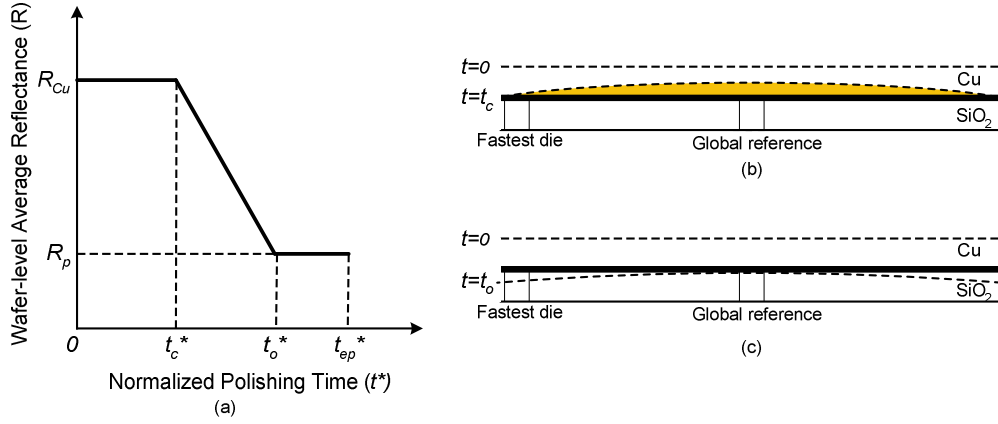


Fig. 7. Slurry-switching point detection by using (a) wafer-level average reflectance ( $R$ ) in Cu CMP: (b)  $R$  starts decreasing when the barrier layer at the fastest die is exposed to the polishing surface, and (c)  $R$  reaches steady state value,  $R_p$ , when all the excess Cu at the global reference point is removed.

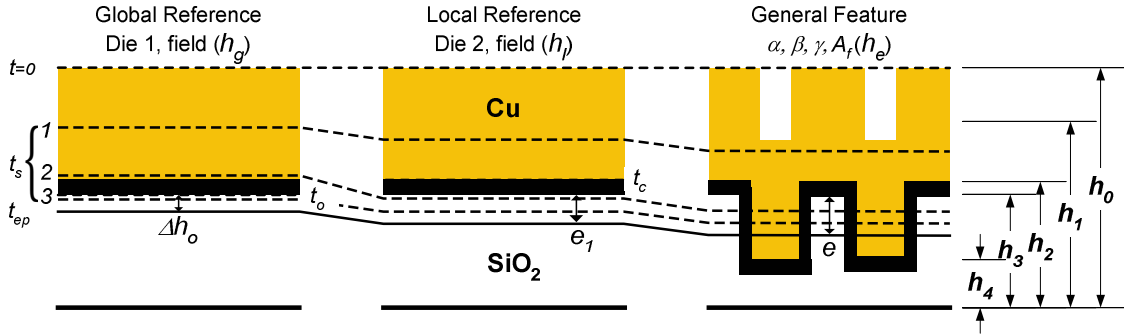


Fig. 8. Schematics of time-based erosion,  $e$ , calculation for general feature in a multi-step polishing process when a global reference point is overpolished as the amount of  $\Delta h_o$  with the slurry-switching time,  $t_s^*$ .

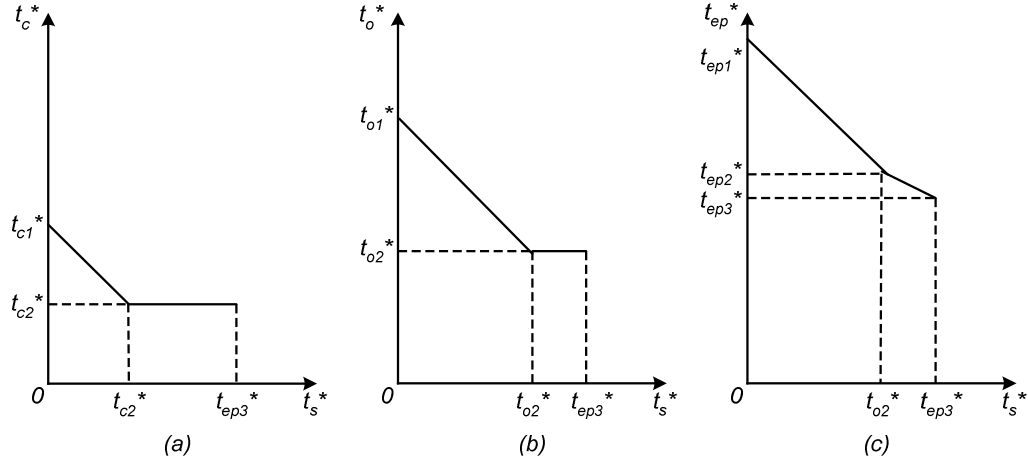


Fig. 9. Effect of slurry-switching time,  $t_s^*$  on (a) the time when excess Cu at the fastest die is removed,  $t_c^*$ , (b) the time when all the excess Cu at the global reference point is cleared,  $t_o^*$  and (c) process end-point,  $t_{ep}^*$ .

average reflectance ( $R$ ) starts decreasing until excess Cu at the global reference is completely removed ( $t = t_o$ ). Polishing is terminated after a certain thickness of the dielectric at global reference is removed to assure that all excess Cu on the wafer is cleared ( $t = t_{ep}$ ). To calculate slurry-switching time dependency on the dielectric erosion, a

dimensionless time is introduced as:

$$t^* \equiv \frac{t}{\left( \frac{h_0 - h_2}{\chi_{Cu1} v_R} \right)} \quad (12)$$

Fig. 8 shows the schematics of time-based erosion for multi-step polishing. Due to the different material removal rates, or selectivities, among the multi-step slurries,  $t_c^*$ ,  $t_o^*$  and  $t_{ep}^*$  directly depend on the slurry-switching time,  $t_s^*$ . Each time can be calculated by considering each case of  $t_s^*$ , and can be plotted as a function of  $t_s^*$  as shown in Fig. 9. The end-point  $t_{ep}^*$ , for example, decreases as  $t_s^*$  increases because the period of application of the high material removal rate, first-step slurry increases.

In order to calculate dielectric erosion in multi-step polishing process, the slurry-switching time  $t_s^*$  must be categorized depending on the condition of polishing surface. In two-step polishing process, for instance,  $t_s^*$  can be divided into three cases as shown in Fig. 8.

1)  $0 \leq t_s^* < t_c^*$ : Dielectric erosion in this case is affected only by second-step slurry, which may be considered as single-step polishing with the second-step slurry. Therefore,  $e^*$  can be calculated by (11) with  $S_{Cu/ox2}$  and  $S_{b/ox2}$ .

2)  $t_c^* \leq t_s^* < t_o^*$ : Dielectric erosion in this case is affected by both first- and second-step slurries and is represented as a function of the slurry-switching time  $t_s^*$ .

$$e^* = \left( \frac{1 - \gamma A_f}{1 - A_f} \right) \left\{ \left[ \frac{1}{S_{Cu/ox2}} \frac{1 - t_s^*}{\beta} + \frac{1}{S_{Cu/ox1}} \frac{t_s^*}{\beta} \right] \left( \frac{h_0 - h_2}{h_3 - h_4} \right) - \frac{1}{S_{Cu/ox1}} \left[ (1 - \alpha A_f) \left( \frac{h_0 - h_1}{h_3 - h_4} \right) + \left( \frac{h_1 - h_2}{h_3 - h_4} \right) \right] \right\} + \left( \frac{1}{1 - A_f} \right) \left[ \frac{1}{S_{b/ox2}} \frac{1}{\beta} (1 - \gamma A_f) - \frac{1}{S_{b/ox1}} (1 - A_f) \right] \cdot \left( \frac{h_2 - h_3}{h_3 - h_4} \right) + \left( \frac{1 - \gamma A_f}{1 - A_f} \right) \frac{1}{\beta} \left( \frac{\Delta h_o}{h_3 - h_4} \right) \quad (13)$$

3)  $t_s^* \geq t_o^*$ : Dielectric erosion in this case is affected only by first-step slurry, which can be considered as the single-step polishing with the first-step slurry. Therefore,  $e^*$  can be calculated by (11) with  $S_{Cu/ox1}$  and  $S_{b/ox1}$ .

### III. EXPERIMENTAL

A Cu damascene structure was designed to study the effects of the various parameters on wafer- and die-level erosion. To verify the present model, one set of single-step polishing experiments, Experiment 1, was performed. Additionally, another set of data, Experiment 2, from published literatures was considered [4], [5]. Each experimental set had different material properties and process parameters as shown in Table I and Table II.

TABLE I  
MATERIAL PROPERTIES.

Properties	Exp. 1	Exp. 2
Mask	MIT-ME	SKW6-2
Cu deposition	PVD	Electroplating
Cu thickness (nm)	1500	1500
Barrier Layer thickness (nm)	20 (Ta)	25 (TaN)
SiO <sub>2</sub> trench (nm)	1000	800
Pad	IC1400	IC1000
Slurry	ICue5001	ICue5001

TABLE II  
EXPERIMENTAL CONDITIONS.

Parameters	Exp. 1	Exp. 2
Diameter of Wafer (mm)	100	200
Normal Load (N)	391	171
Normal Pressure (kPa)	48	21
Rot. Speed (rad/s)	7.8	9.4
Linear Velocity (m/s)	0.70	0.85
Duration (sec)	60-360	60-180
Slurry Flow (ml/sec)	2.5	1.5

Fig. 10 shows the pattern layouts on the mask for experimental sets 1 and 2. Experiments were conducted on a rotary CMP machine with the experimental conditions listed in Table II. Blanket wafers were also polished to determine the selectivities, followed by patterned-wafer polishing.

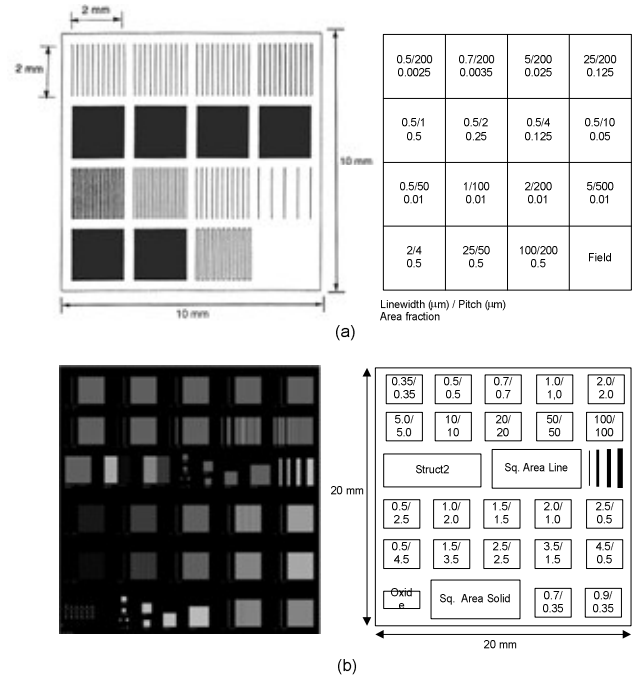


Fig. 10. Schematics of the mask layout and pattern geometry layout for (a) experimental set 1 with MIT-ME mask and (b) experimental set 2 with SKW6-2 mask [4], [5].

## IV. RESULTS

### A. Determination of Model Parameters

The developed single- and multi-step dielectric erosion models show that the most significant parameters in dielectric erosion are the selectivities of each-step slurry. The selectivities of each slurry were determined by blanket wafer polishing experiments.

The interconnect deposition factor  $\alpha$  was obtained by measuring the deposited top surface of a patterned wafer by Scanning Electron Microscopy (SEM). Fig. 11 shows the SEM measurements of two patterns with the same area fraction (0.5) but different linewidths ( $0.5 \mu\text{m}$  and  $2 \mu\text{m}$ ). The results show that the value of  $\alpha$  is closely related to the Cu interconnect linewidth  $w$ .

The wafer-level non-uniformity factor  $\beta$  was obtained from blanket wafer material removal rates at two selected points on the same wafer at different times. Fig. 12 shows the Cu blanket wafers after 2, 3 and 4 min of polishing. Photographs of the wafers show that the edge is polished faster than the center area as polishing time increases. The maximum of the material removal rate ratio is about 0.85.

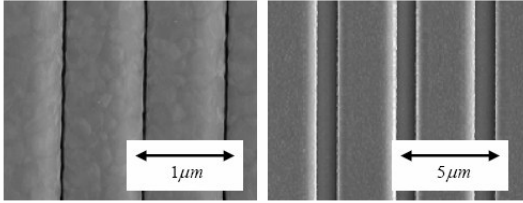


Fig. 11. SEM micrographs for the effect of interconnect deposition factor,  $\alpha$ , (a)  $A_f=0.5$ ,  $w=0.5 \mu\text{m}$ ,  $\alpha=0.1$  and (b)  $A_f=0.5$ ,  $w=2 \mu\text{m}$ ,  $\alpha=0.5$ .

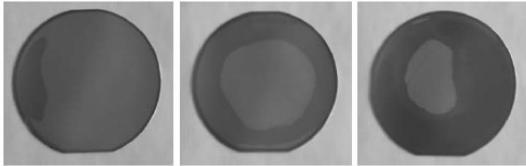


Fig. 12. Observation of the effect of wafer-level non-uniformity factor,  $\beta$  in Cu blanket wafer polishing at (a)  $t=2\text{min}$ , (b)  $t=3\text{min}$  and (c)  $t=4\text{min}$ .

### B. Experimental Validation for Single-Step Cu CMP

After determining all the modeling parameters, they have been used for calculating dielectric erosion based on the present model. Fig. 13(a) and Fig. 13(b) compare the developed model and experimental data for each experimental set.

Again, the dimensionless dielectric erosion  $e^*$ , the ratio between dielectric erosion and the designed Cu interconnect thickness, or the trench depth, is used for all measurement and calculation.

As shown in Fig. 13(a) and Fig. 13(b), the proposed dielectric erosion model match the single-step polishing experimental data both in low area-fraction and high area-fraction region.

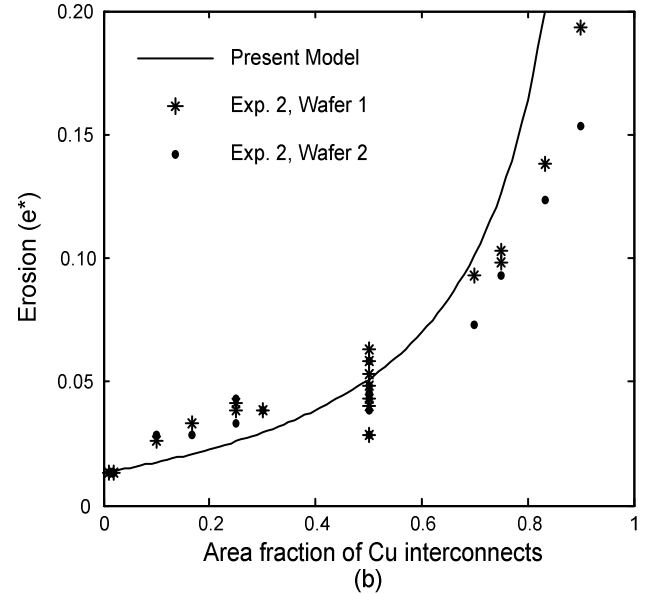
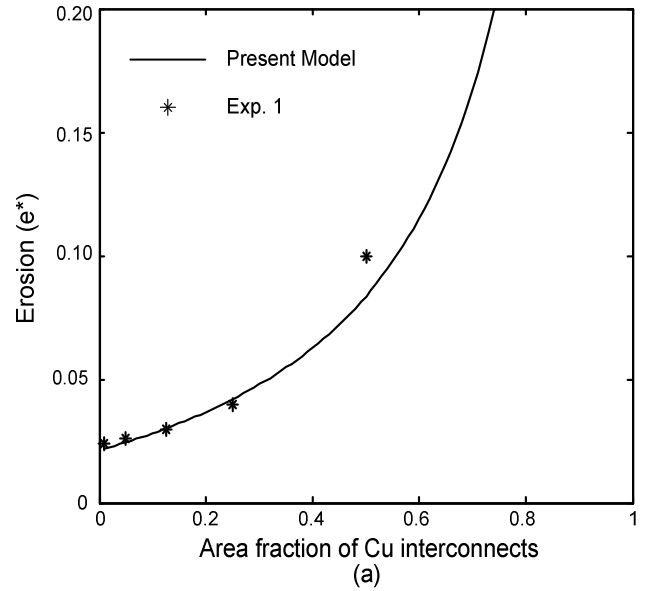


Fig. 13. Experimental results for a single-step Cu CMP and proposed dielectric erosion model validation: (a) experimental set 1 with MIT-ME mask and (b) experimental set 2 with SKW6-2 mask [4], [5].

### C. Parameter Sensitivity

Based on the present single- and multi-step dielectric erosion models, the physical significance of each model parameter on dielectric erosion can be readily ascertained. For example, Fig. 14 shows the effect of model parameters on dielectric erosion for single-step Cu CMP based on (11). For the two-step polishing process, the effects of the selectivities of the first- and second-step slurry are shown in Fig. 15(a) and Fig. 15(b) based on (13). Furthermore, the effect of slurry-switching time,  $t_s^*$  on the dielectric erosion is presented in Fig. 15(c). Based on these figures, it is possible to suggest optimal polishing practices for minimizing dielectric erosion in both single- and multi-step polishing because the model is based on experimentally obtained parameters.

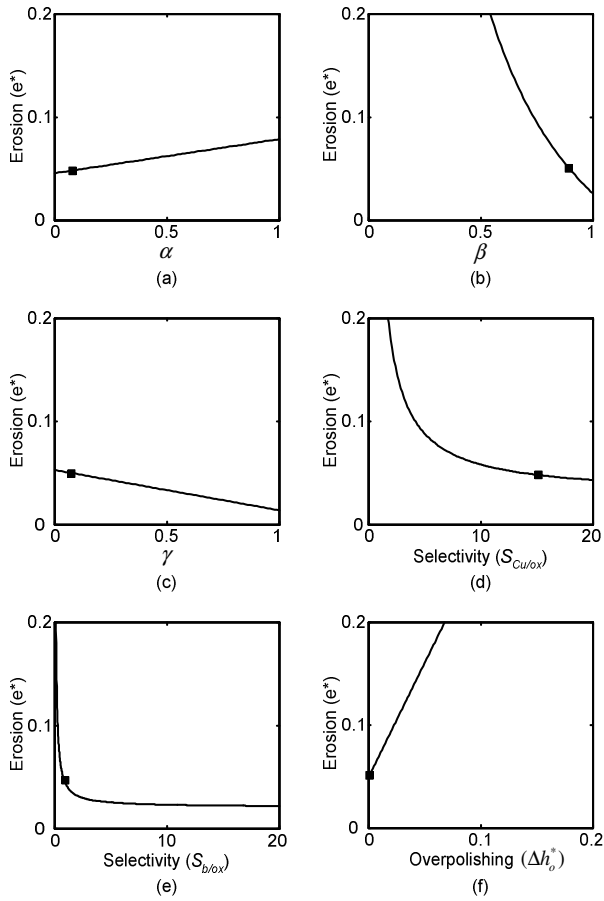


Fig.14. Effect of model parameters on the dielectric erosion for single-step Cu CMP. Parameters include (a) Selectivity  $S_{Cu/ox}$ , (b) Selectivity  $S_{b/ox}$ , (c) Cu deposition factor  $\alpha$ , (d) wafer-level non-uniformity factor  $\beta$ , (e) local pressure distribution factor  $\gamma$  and (f) overpolishing,  $\Delta h_o$ : Each model parameters except variable is set as  $S_{Cu/ox}=14.4$ ,  $S_{b/ox}=0.8$ ,  $A_f=0.5$ ,  $\alpha=0.1$ ,  $\beta=0.9$ ,  $\gamma=0.1$ , and  $\Delta h_o=0$ .

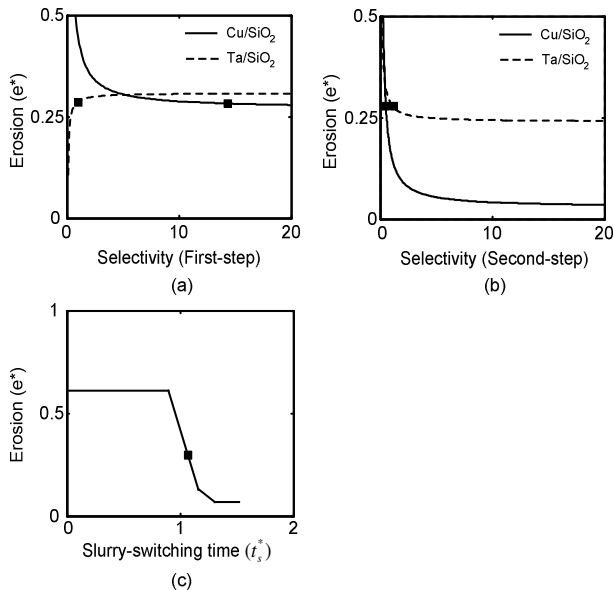


Fig.15. Effect of model parameters on the dielectric erosion for multi-step Cu CMP. Parameters include selectivities of (a) first-, (b) second-step slurry and (c) slurry-switching time,  $t_s^*$ : Each model parameters except variable is set as  $S_{Cu/ox1}=14.4$ ,  $S_{b/ox1}=0.8$ ,  $S_{Cu/ox2}=0.5$ ,  $S_{b/ox2}=1.0$ ,  $A_f=0.5$ ,  $\alpha=0.1$ ,  $\beta=0.85$ ,  $\gamma=0.1$ ,  $\Delta h_o=0$  and  $t_s^*=1.05$ .

## V. CONCLUSIONS

In this paper, a systematic way of characterizing and modeling dielectric erosion in single- and multi-step Cu CMP processes is presented. Wafer- and die-level erosion are clearly defined, and the plausible causes of erosion at each level are identified in terms of the geometric and physical parameters. Such parameters include: Cu interconnect deposition factor ( $\alpha$ ), wafer-level non-uniformity factor ( $\beta$ ), local pressure distribution factor ( $\gamma$ ), selectivities among Cu, barrier material and dielectric ( $S_{Cu/ox}, S_{b/ox}$ ), and the slurry-switching time ( $t_s^*$ ). Experimental and analytical means of determining the model parameters are outlined. The local pressure distribution is characterized at each polishing stage based on the evolving pattern geometry and pad deformation, although further analysis of pad deformation is required. The chemical and chemo-mechanical effects are included as slurry selectivities and are obtained by experiments on 100 mm blanket wafers and the published literature. The developed dielectric erosion model is expressed in a dimensionless form ( $e^*$ ), which is the ratio between dielectric erosion and the designed Cu interconnect thickness, and is validated by data from single-step Cu CMP experiments on patterned wafers. Additionally, the single-step model is adapted for the multi-step polishing process, with multiple sets of slurry selectivities, applied pressure, and relative velocity in each step. Finally, the effect of slurry-switching point ( $t_s^*$ ) on erosion was investigated for minimizing dielectric erosion in the multi-step Cu CMP.

Based on the present multi-step erosion model, the physical significance of each model parameter on dielectric erosion can be clearly delineated – for example, the roles of the first- and second-step slurry selectivities, and the slurry-switching point. Furthermore, it is possible to suggest optimal polishing practices for minimizing dielectric erosion in both multi-step and single-step polishing because the model is based essentially on experimentally obtained parameters. A comprehensive model, which is being developed, however should address Cu dishing.

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## REFERENCES

- [1] *Interconnect*, International Technology Roadmap for Semiconductors, 2001.
- [2] J.-Y. Lai, N. Saka and J.H. Chun, "Evolution of Copper-Oxide Damascene Structures in Chemical-Mechanical Polishing - Contact Mechanics Modeling", *J. Electrochem. Soc.*, vol. 149, pp. G31-G40, 2002.
- [3] J.-Y. Lai, N. Saka and J.H. Chun, "Evolution of Copper-Oxide Damascene Structures in Chemical-Mechanical Polishing – Copper Dishing and Oxide Erosion", *J. Electrochem. Soc.*, vol. 149, pp. G41-G50, 2002.



- [4] T. Park, T. Tugbawa and D. Boning, "Pattern Dependent Modeling of Electroplated Copper Profiles", *International Interconnect Technology Conference*, pp. 274-276, 2001.
- [5] T. Tugbawa, T. Park, and D. Boning, "Integrated Chip-Scale Simulation of Pattern Dependencies in Copper Electroplating and Copper Chemical Mechanical Polishing Processes", *International Interconnect Technology Conference*, 2002.
- [6] D.-Z. Chen and B.-S. Lee, "Parameter Analysis of Chemical Mechanical Polishing: An Investigation Based on the Pattern Planarization Model", *J. Electrochem. Soc.*, vol. 146, pp. 3420-3424, 1999.
- [7] D.-Z. Chen and B.-S. Lee, "Pattern Planarization Model of Chemical Mechanical Polishing", *J. Electrochem. Soc.*, vol. 146, pp. 744-748, 1999.
- [8] D. Ouma, B. Stine, R. Divecha, D. Boning, J. Chung, G. Shinn, I. Ali and J. Clark, "Wafer-Scale Modeling of Pattern Effect in Oxide Chemical Mechanical Polishing", *Proc. SPIE Microelectronics Mfg. Conf.*, 1997.
- [9] Z. Stavreva, D. Zeidler, M. Pltner, G. Grasshoff and K. Drescher, "Chemical Mechanical Polishing of Copper for Interconnect Formation", *Microelectron Eng.*, vol. 33, pp. 249-257, 1997.
- [10] J.M. Steigerwald, R. Zirpoli, S.P. Murarka, D. Price and R.J. Gutmann, "Pattern Geometry Effects in the Chemical-Mechanical Polishing of Inlaid Copper Structures", *J. Electrochem. Soc.*, vol. 141, pp. 2842-2848, 1994.
- [11] L. Yang, "Modeling CMP for copper dual damascene interconnects", *Solid State Technology*, vol. 6, p111, 2000.
- [12] K. Noh, N. Saka and J.H. Chun, "A Mechanical Model for Erosion in Copper Chemical-Mechanical Polishing", *Chemical-Mechanical Planarization for ULSI Multilevel Interconnect Conference (CMP-MIC)*, pp. 445-452, 2003.
- [13] F.W. Preston, "The Theory and Design of Plate Glass Polishing Machines", *J. Soc Glass Technology*, vol. 11, pp. 214-256, 1927.
- [14] B.W. Adams, B. Swedek, R. Bajaj, F. Redeker, M. Birang and G. Amico, "Full-Wafer Endpoint Detection Improves Process Control in Copper CMP", *Semiconductor Fabtech*, vol.12, 2001.

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