DEPENDENCE OF NANOCRYSTAL FORMATION AND CHARGE STORAGE/RETENTION PERFORMANCE OF A TRI-LAYER MEMORY STRUCTURE ON GERMANIUM CONCENTRATION AND TUNNEL OXIDE THICKNESS

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Abstract— **The effect of germanium (Ge) concentration and the rapid thermal oxide (RTO) layer thickness on the nanocrystal formation and charge storage/retention capability of a trilayer metal-insulator-semiconductor device was studied. We found that the RTO and the capping oxide layers were not totally effective in confining the Ge nanocrystals in the middle layer when a pure Ge middle layer was used for the formation of nanocrystals. From the transmission electron microscopy and secondary ion mass spectroscopy results, a significant diffusion of Ge atoms through the RTO and into the silicon (Si) substrate was observed when the RTO layer thickness was reduced to 2.5 nm. This resulted in no (or very few) nanocrystals formed in the system. For devices with a Ge+SiO$_2$ co-sputtered middle layer (i.e., lower Ge concentration), a higher charge storage capability was obtained than with devices with a thinner RTO layer, and the charge retention time was found to be less than in devices with a thicker RTO layer.**

*Index Terms—***Ge nanocrystal, Floating gate, Metal-insulator-semiconductor**

I.   INTRODUCTION

The charge storage property of semiconductor nanocrystals embedded in a silicon oxide matrix is currently under intense investigation due to its potential application in future non-volatile memories.[1-3] As charge loss through lateral paths in nanocrystal based memory devices is suppressed by the oxide isolation between nanocrystals, these devices exhibited superior charge retention characteristics compared with conventional floating-gate memory devices.[1] We have previously reported memory effect in germanium (Ge) nanocrystals, which were embedded in the silicon oxide (SiO$_2$) matrix of a metal-insulator-semiconductor (MIS) device.[4,5] The MIS device consisted of a trilayer insulator structure: a rapid thermal oxide (RTO) layer (2.5 to 5 nm thick)

grown on a p-type silicon substrate, a co-sputtered Ge + SiO$_2$ middle layer (3 to 20 nm thick) and a 50 nm thick sputtered silicon oxide capping layer. The Ge nanocrystals in the middle layer were synthesized by rapid thermal annealing (RTA) of the as-prepared samples at 1000ºC for 300 s in argon. From the high-resolution transmission electron microscopy (HRTEM) images, we found that the maximum size of the Ge nanocrystals formed in the vertical (z-) direction was confined by the RTO and the capping oxide layers. We also observed previously that for devices with fixed RTO and capping oxide layer thicknesses, the capacitance versus voltage (C-V) results show better charge storage capability (i.e., larger hysterisis in C-V curve) for devices with a thinner middle layer. This was attributed to the higher density of nanocrystals found in such devices.[5] In this article, we examine the effect of Ge concentration and the RTO layer thickness on the formation of nanocrystals and the charge storage characteristics of the MIS devices.

II.   EXPERIMENT

The trilayer insulator structure of the MIS devices used in this work have generally similar dimensions as reported in our earlier work. A RTO layer, with thickness of 2.5 to 5 nm, was first grown on a (100) p-type silicon (Si) substrate. We varied the Ge concentration by using a pure sputtered Ge middle layer (4 nm thick) or a co-sputtered Ge + SiO$_2$ (6 nm thick) middle layer. This was followed by a sputtered capping silicon oxide layer of thickness ranging from 46 to 64 nm. Details of the fabrication processes can be found in our earlier work.[4] The structure was then processed by RTA at 1000°C for 300s in argon before forming the gate electrode (Al) of the MIS structure. The high frequency (100 kHz) C-V measurements were carried out using a HP 4284 impedance analyzer and the capacitance-time (C-t) measurements were carried out using a Keithley 590 C-V analyser. A   high-resolution   transmission   electron

microscope was used to obtain the cross-sectional and planar TEM images of the devices.

III.   RESULTS AND DISCUSSIONS

From Fig. 1(a), it can be seen that a number of nanocrystals are in contact with the Si substrate for the structure sputtered with a pure Ge middle layer and a 5 nm-thick RTO layer (device P5). There are also nanocrystals that have penetrated into the RTO layer but are not in contact with the Si substrate. Note that the planar TEM image of Fig. 1(b) shows even smaller (and more numerous) nanocrystals that were very difficult to be identified from the cross sectional TEM image of Fig. 1(a). The density of the nanocrystals was estimated to be about 9.3×10^{11} cm^{-2} from several planar TEM images (similar to Fig. 1(b)) of device P5. The densities of the nanocrystals in our earlier work[5] of the co-sputtered Ge + SiO$_2$ systems (with the RTO and capping oxide layer thickness fixed at 5 and 50 nm, respectively) were estimated to be about 5.7×10^{11} cm^{-2} and 1.6×10^{12} cm^{-2} for devices with a middle layer thickness of 6 nm and 3 nm, respectively. Therefore, we are not able to obtain a higher density of nanocrystals with a pure Ge middle layer structure. It should be noted that with a 100% Ge concentration in the middle layer and a thin RTO layer, significant diffusion of Ge through the RTO layer is possible, and Ge atoms can also coalesce to form larger nanocrystals in contact with the Si substrate (see Fig. 1(a)). As a significant number of Ge atoms were used up either in the formation of the large nanocrystals and some would have been diffused away through the RTO layer, this could have resulted in a lower density of nanocrystals formed. It is interesting to note from Fig. 1(b) that the smaller nanocrystals are generally separated from each other by a few nanometers and not in contact with the Si substrate. This is important as charge loss, either through tunneling between adjacent nanocrystals or into the Si substrate, can be minimized by such a separation. The charge retention property of these devices will be examined later when we discuss the C-t results.

Figure 1(c) shows the TEM image of a device with a pure Ge middle layer and 2.5-nm thick RTO layer that has been RTA at 1000°C for 300 s (device P2-5). The original pure Ge layer has disappeared after RTA and we could not locate any nanocrystals in the device. The RTO-Si substrate interface also appears to be rather uneven. We have reported earlier that for devices with a co-sputtered Ge+SiO$_2$ middle layer, the RTO layer and the capping oxide layer has been effective in confining the nanocrystals in the middle layer.[5] In device P2-5, due to the steep Ge concentration gradient between the middle layer and the Si substrate and the thin RTO barrier for diffusion, it is likely that most of the Ge may have diffused into the Si substrate during RTA at 1000°C.[6] As a consequence, no (or very few)
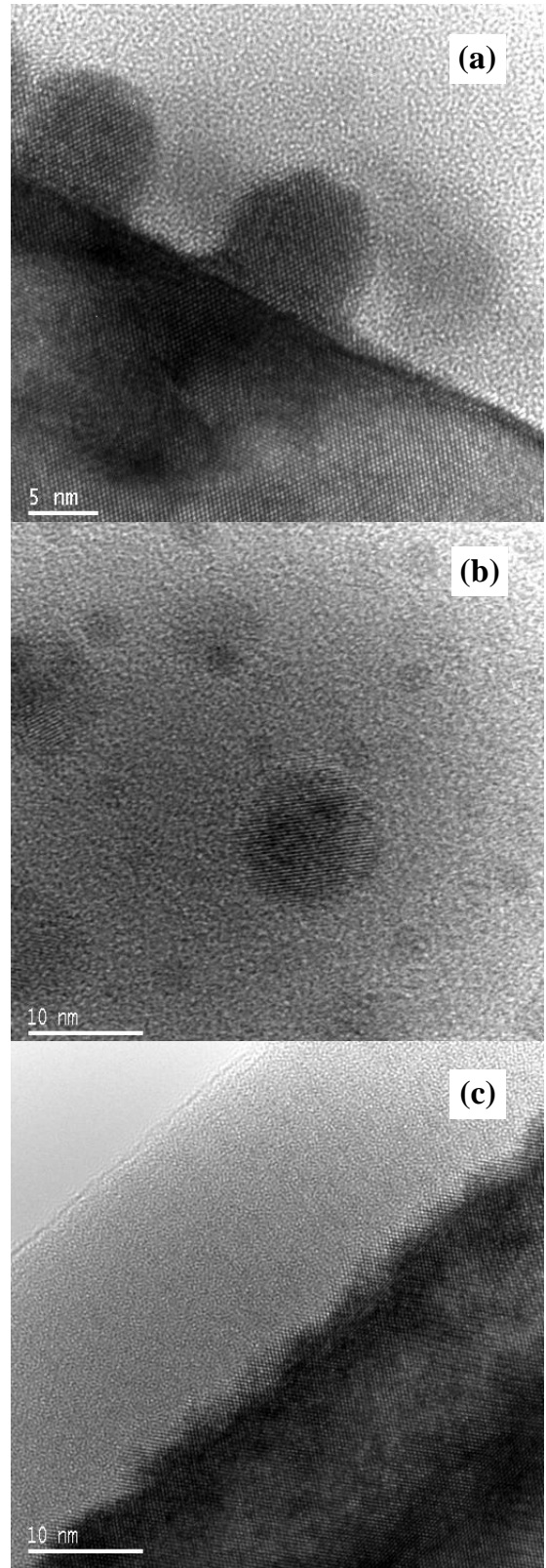

Fig. 1:(a) Cross-sectional and (b) planar HRTEM images of device P5, and (c) cross-sectional HRTEM image of device P2-5. The devices have a 4-nm thick pure sputtered Ge middle layer and a 46 nm and 65 nm capping oxide layer for devices P2-5 and P5, respectively. The RTO thickness of devices P5 and P2-5 are 5 nm and 2.5 nm, respectively. Note that both devices P5 and P2-5 have been subjected to RTA at 1000°C for 300 s.

nanocrystals were formed in the MIS structure. The uneven RTO-Si interface may be due to the pronounced diffusion of Ge from the middle layer to the Si substrate.

Figure 2 shows the secondary ion mass spectroscopy (SIMS) results (obtained using a 2 keV Cs^+ source) of as-prepared and annealed devices P5 and P2-5. The SIMS results of device P2-5 show that Ge from the middle layer diffuses to the capping layer and the RTO-Si substrate region. Compared to the Ge profile of the as-prepared device, there appears to be a pronounced diffusion of Ge to the RTO-Si substrate region. This is in agreement with our discussion earlier. If we compare the Ge profiles of the annealed devices P5 and P2-5, it is obvious that the thicker RTO layer has reduced the diffusion of Ge to the RTO-Si region. As a consequence, a more pronounced out-diffusion of Ge with higher Ge concentration into the capping layer is observed in device P5 compared to device P2-5. This may account for the formation and location of nanocrystals observed in device P5 and the general absence of nanocrystals in device P2-5, as shown in Figs. 1(b) and 1(c).

The charge storage density was estimated to be 2.3 x 10^{12} cm^{-2}. However, only 50% of the tested devices with the device P2-5 structure exhibited a C-V characteristic as shown in Fig. 3 (a); the other 50% exhibited no proper C-V curves. For those P2-5 devices that exhibited proper C-V characteristics, a significantly smaller hysteresis of ~2.4 V was observed.

One would expect that the hysteresis of device P2-5 to be larger than that of device P5 as a larger number of charge carriers are able to tunnel across the thinner RTO layer and be stored in the nanocrystals. However, as no (or very few) nanocrystals were formed in device P2-5 (see Fig. 1(c)), it is reasonable to expect a much smaller hysteresis in such devices. Figure 3(a) also shows the quasi-neutral C-V curve, obtained by restricting the gate bias to a very narrow range to minimize the charging up of nanocrystals, for device P5. The C-V curve of device P2-5 shifts towards a more positive gate voltage as compared to the quasi-neutral C-V curve of device P5. This may be due to Ge penetration through the RTO layer and into the Si substrate.
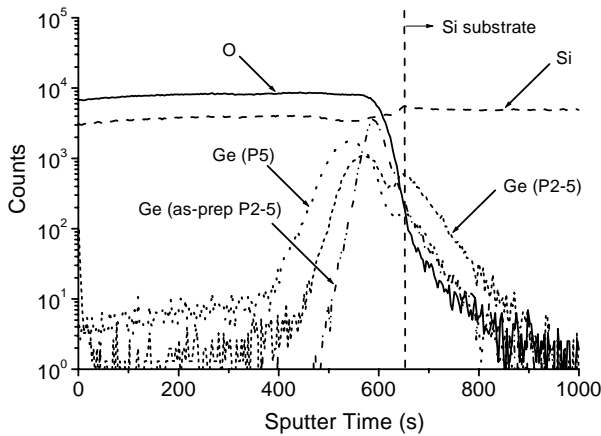

Fig. 2: Secondary ion mass spectroscopy results of as-prepared (as-prep P2-5) and annealed (P2-5 and P5) devices. Due to the difference in the capping oxide and RTO thickness of devices P5 and P2-5, we have adjusted the SIMS results by shifting the SIMS profiles horizontally by using the Si profile as the reference (i.e., matching the Si profiles of devices P5 and P2-5 at the RTO-silicon interface as indicated by the vertical dashed line).

Figure 3(a) shows the forward and reverse sweep C-V characteristics of devices P5 and P2-5 measured with the bias held at +15V and -15V for 240s before commencing each C-V sweep. This is to ensure that the charging and discharging processes in the devices have reached a steady state (i.e., the flat-band voltage shift has saturated). We found that 80% of the tested devices with the device P5 structure exhibited a counter-clockwise C-V hysteresis, with an average hysteresis width of ~12 V.
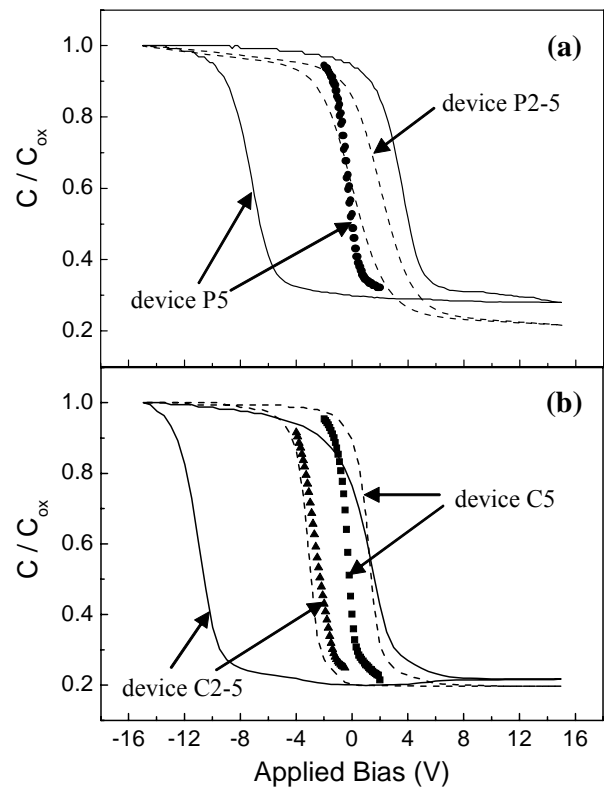

Fig. 3: High frequency C-V characteristics of (a) devices P5 and P2-5 and (b) devices C5 and C2-5. Note the quasi-neutral C-V curves for the respective devices (symbols ●, ▲ and ■) were obtained by restricting the gate bias to a very narrow range to minimize charging up of the Ge nanocrystals.

Figure 3(b) shows the C-V characteristics of devices with a 6-nm thick co-sputtered middle layer and RTO layer thicknesses of 2.5 nm (device C2-5) and 5nm (device C5). Both C-V curves show counter-clockwise hysteresis and the charge stored for devices C2-5 and C5 was estimated to be 3.7×10^{12} cm^{-2} and 1.3×10^{12} cm^{-2}, respectively. In agreement with results of our earlier work,[7] the amount of charge stored in devices with a co-sputtered middle layer increases as the RTO layer thickness is reduced. This is reasonable as a larger number of charge carriers from the Si substrate are therefore able to tunnel across the thinner RTO layer, resulting in an increase in the charge stored in device C2-5 as compared to device C5. Note that the flat-band voltage of the uncharged device C5 is close to zero (obtained from the quasi-neutral curve in Fig. 2(b)) but is negative for the uncharged device C2-5. The reasons for this have been explained in our earlier work.[7]

Note that in Fig. 3(b), there exists a gentler slope of the C-V curve for device C2-5 as compared to device C5. We have pointed out previously that it is difficult to separate the influence of the charging/discharging processes and the interface traps on the slope of the C-V curves of memory devices. We have carried out a series of C-V measurements on device C2-5 at different sweep rates ranging from 0.1 to 10 V/s and found that a higher sweep rate resulted in a steeper C-V curve as the nanocrystals have lesser time to charge and discharge. This suggests that the gentler C-V slope in device C2-5 is likely a result of the smaller RTO thickness affecting the ease of the charging and discharging processes occurring concurrently during the C-V sweep. This also means that even though device C2-5 has a better charge storage capability (i.e., larger hysteresis), it is likely to have a poorer charge retention capability than device C5. The charge retention capability was investigated using the C-t measurements. Returning to Fig. 3(a), one can also observe a gentler slope in the C-V curve of device P5 as compared to its quasi-neutral curve, which is not surprising as the quasi-neutral curve represents the uncharged condition of the device. Device P2-5 also exhibits a gentler C-V slope as compared to device P5. Since device P2-5 exhibits negligible charge storage, it is likely that this gentler C-V slope is attributed to a poorer Si-RTO interface, possibly a result of the Ge penetration causing an uneven interface as shown previously in Fig. 1(c).

In the charge retention capability study, the devices were first fully charged up at 12 V for 60 s as manifested by the saturated capacitance value in the C-t curve. After which the bias voltage was switched abruptly to the discharging voltage, the latter ranging from –15 V to 1 V. The inset of Fig. 4 shows typical discharging C-t curves for devices C5 and C2-5 at discharging biases of –2V and –12V, respectively. These values of discharging biases resulted in maximum charge

retention for the devices shown in Fig. 4. Similar to the C-t results presented by Kim *et al.*,[8] the normalized capacitance in the C-t plot in Fig. 4 was calculated based on the formula $\dfrac{C(t) - C_{sat}}{C_{max} - C_{sat}}$, where C_{sat} is the saturation capacitance taken at the end of the C-t discharging experiment while C_{max} is the initial capacitance at the start of the discharging experiment. The retention time was defined as the time for the normalized capacitance to reach 50% of C_{max}.
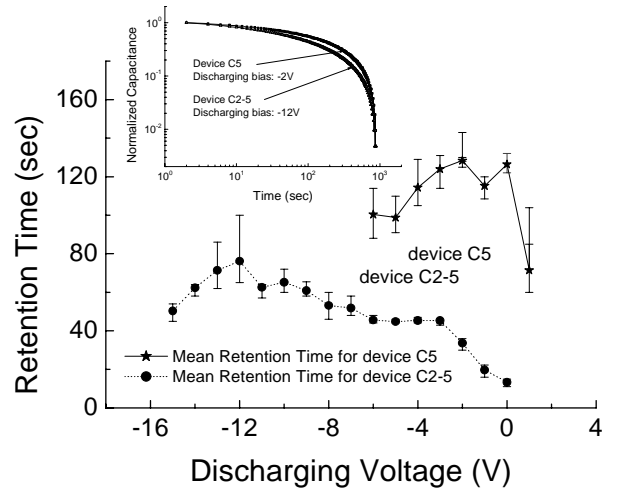

Fig. 4: Retention characteristics of devices C5 and C2-5 for various discharging bias. Both devices have a 6-nm thick Ge + SiO$_2$ co-sputtered middle layer and a 50-nm thick capping oxide. The RTO thickness of devices C5 and C2-5 are 5 nm and 2.5 nm, respectively. The inset shows the C-t results of devices C5 and C2-5 under a discharging bias voltage of –2 V and –10 V, respectively.

In Fig. 4, five tested devices for each device structure (i.e., device C2-5 and C5) were used to obtain the maximum, minimum and mean retention times at different discharging biases. It is observed that device C2-5 has a poorer peak mean retention time of 80 s as compared to 130 s for device C5. This agrees with our earlier deduction when we examined the slopes of the C-V curves of Fig. 3(b) that device C2-5 is expected to exhibit a poorer retention capability as compared to device C5.

IV. CONCLUSION

In conclusion, the RTO and the capping oxide layers are not effective in confining the Ge nanocrystals in the middle layer of the trilayer insulator structure of an MIS memory device when the Ge concentration is high. A significant diffusion of Ge atoms into the Si substrate occurred when the RTO layer thickness was reduced to

2.5 nm and resulted in no (or very few) nanocrystals formed in the system. For devices with a co-sputtered middle layer, even though a higher charge storage capability was obtained from devices with a thinner RTO layer, the charge retention capability is poorer as compared to devices with a thicker RTO layer.

ACKNOWLEDGEMENT

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