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RELIABILITY OF MULTI-TERMINAL COPPER DUAL-DAMASCENE INTERCONNECT TREES

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ABSTRACT

Electromigration tests on different Cu dual-damascene interconnect tree structures consisting of various numbers of straight via-to-via lines connected at the common middle terminal have been carried out. Like Al-based interconnects, the reliability of a segment in a Cu-based interconnect tree strongly depends on the stress conditions of connected segments. The analytic model based on a nodal analysis developed for Al trees gives a conservative estimate of the lifetime of Cu-based interconnect trees. However, there are important differences in the results obtained under similar test conditions for Al-based and Cu-based interconnect trees. These differences are attributed to the variations in the architectural schemes of the two metallization systems. The absence of a conducting electromigration-resistant overlayer in Cu technology and the low critical stress for void nucleation at the Cu/inter-level diffusion barrier (i.e. Si_3N_4) interface leads to different failure modes between Cu and Al interconnects. As a result, the most highly stressed segment in a Cu-based interconnect tree is not always the least reliable. Moreover, the possibility of liner rupture at stressed dual-damascene vias leads to significant differences in tree reliabilities in Cu compared to Al. While an interconnect tree can be treated as a fundamental unit whose reliability is independent of that of other units in Al-based interconnect architectures, interconnect trees can not be treated as fundamental units for circuit-level reliability analyses for Cu-based interconnects.

I. INTRODUCTION

Several kilometers of metallic interconnecting wires (interconnects) are required in a single high-performance integrated circuit (IC) [1]. Cu-based metallization for interconnection is replacing Al-based metallization due to copper's lower electrical resistivity, which leads to significantly reduced RC delay in complex ICs. In each IC, millions of metal segment exist and the reliability of each of these elements governs the reliability of the circuit as a whole. Electromigration (EM), electronic-current-induced atomic diffusion of metal atoms, and electromigration-induced failure has been an important reliability issue in Al metallization and continues to be so for Cu-based interconnects [2].

Presently, most experiments and circuit-level interconnect reliability analyses focus on straight via-to-via (or contact-to-contact) test structures. However, in real circuits, multiple via-to-via segments are connected at junctions and many such junctions are connected within the same layer of metallization. An "interconnect tree" is a unit of continuously connected high-conductivity metal lying within one layer of metallization [3-4]. Most circuit-level reliability assessment methods are based on individual segments that combine to form interconnect trees, using the results from straight via-to-via test lines to analyze the reliability of segments. This method is generally inaccurate as materials within the tree can diffuse freely between the segments, and the stress evolution in the different segments of a tree is coupled. It has been argued that an interconnect tree is the appropriate fundamental reliability unit for circuit-level assessments of the reliability of Al-based metallization [4]. The fundamental reliability units should have reliabilities that can be treated independently, and it has been shown through modeling and experiments that trees have this characteristic in Al technology.

One key difference between electromigration in Al and Cu interconnects is that in polycrystalline Al lines, grain boundaries provide the highest diffusivity paths for electromigration while in Cu metallization, the Cu/liner or Cu/inter-level diffusion barrier (usually Cu/Si_3N_4) interfaces provide even higher diffusivity paths than the grain boundaries [2, 5-7]. The Cu/inter-level diffusion barrier

interface is also thought to provide a site for void nucleation at relatively low tensile stresses [8, 9]. Moreover, in dual-damascene Cu metallization, interconnects terminate at diffusion barriers such as a thin Ta liner instead of W-filled vias as in Al metallization. It has been reported that the Ta liner at the base of the vias may rupture under high stress [10, 11] and thus may not act as a perfectly blocking boundary. These differences are important because they are the determining factors for the locations and modes of electromigration-induced failure in Cu-based metallization.

In this paper, we discuss results from experiments on electromigration in straight via-to-via dual-damascene Cu-based lines with an extra via in the middle of the line (dotted-I), stressed under different current configurations [12]. The experimental trends are compared to the results reported for Al-based structures [4]. The reliability of the dotted-I test structures was further studied by varying the distribution of a fixed current density through the middle terminal into the two connected segments. The lifetime of 3-terminal (dotted-I), 4-terminal (T) and 5-terminal (cross) interconnect trees with the same current density through the common middle via was also determined. Lastly, the analytical model previously developed for Al-based interconnect trees [4] is tested for Cu-based interconnect trees.

II. EXPERIMENTS

Test samples were fabricated using a Cu dual-damascene process. First, a 13500Å-thick dielectric stack of $SiO_2/Si_3N_4/SiO_2$ was deposited onto a Si wafer using plasma-enhanced chemical vapor deposition (PECVD) at 400°C. A trench was etched down to the Si_3N_4 etch stop for the first level of metallization (M1). Next, a 250Å-thick Ta diffusion barrier and a 2000Å-thick Cu seed layer were sputter deposited into the trench before electroplating a 1μm-thick Cu film. After the film was annealed at 300°C and chemical-mechanical polished (CMP), a 14000Å-thick inter-metal dielectric (IMD) stack consisting of $Si_3N_4/SiO_2/Si_3N_4/$ SiO_2 was deposited. The second level of metallization (M2) was formed using a via-first etch dual-damascene process and the thickness of the M2 Cu line was approximately 2400Å after CMP. After patterning the second level of metallization, a Si_3N_4/SiO_2 dielectric stack was deposited as passivation layer. The bond pads were opened and a bilayer of Al/Ta was deposited and patterned over the bond pads to improve the quality of wire bonds. The dice were packaged in ceramic packages and Au wires were used to connect the bond pads to package lead frames.

Electromigration experiments were carried out on 0.28μm-wide dotted-I, T and cross interconnect trees as shown in Figure 1. The length of each segment from via-to-via was 250μm. The test structures were in the second level of metallization and were electrically connected to the bond pads through much wider M1 connector lines at the vias. This design allows currents of different magnitudes and

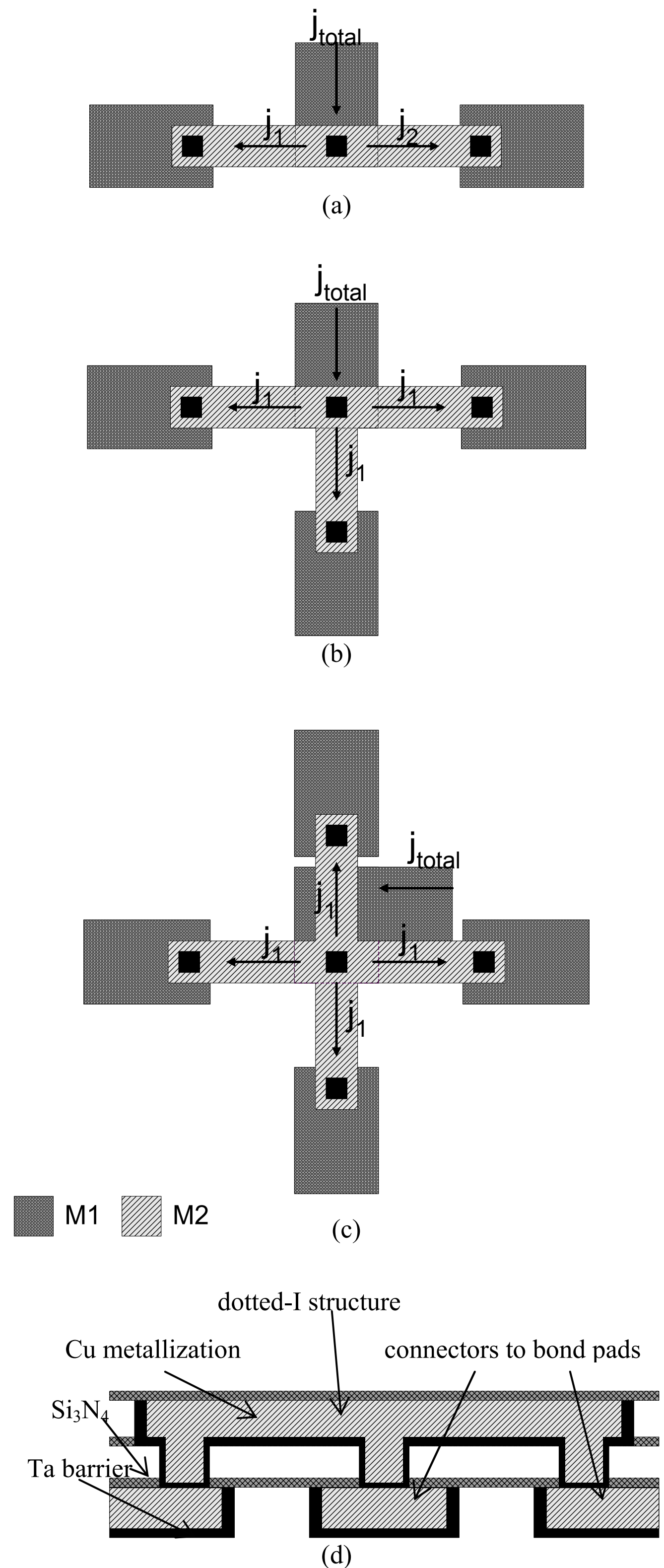


Figure 1: Schematic diagram of a (a) dotted-I (b) T and (c) cross interconnect tree. The arrows show the directions of electron flow. (d) Side view of a dotted-I test structure.

directions to be applied independently in the individual segments of the interconnect trees. The samples were stressed in a *Xpeqt* electromigration test system at a temperature of 350°C.

III. ANALYTICAL MODEL

While simulation of electromigration in complex interconnect trees is possible [3], less computationally-intensive analytic models are needed for circuit-level reliability analyses. A conservative model for the analysis of interconnected trees has been previously proposed by Hau-Riege and Thompson [4] and verified for Al-based dotted-I structures. In the analysis, the stress evolution at a node in an Al-based interconnect tree has been conservatively estimated as

$$\sigma(t) = \sqrt{\frac{4t}{\pi}}\frac{\rho q^*}{\Omega}\sqrt{\frac{B\Omega}{kT}}\frac{\sum_i D_i j_i}{\sum_i \sqrt{D_i}} + \sigma_0 , \qquad (1)$$

where $q^* = Z^*e$ is the effective charge, e is the elementary charge, and Z^* is the effective charge number. In Equation (1), ρ is the electrical resistivity of the migrating metal layer, Ω is the atomic volume, B is the effective elastic modulus of the material surrounding the migrating material [13, 14], kT is the thermal energy, σ_o is the initial hydrostatic stress in the tree, and D_i and j_i are the atomic diffusivity and current density in segment i, respectively.

Assuming constant and time-independent diffusivity along the segment, we can estimate the time, t_{nucl}, when the tensile stress exceeds the critical stress for void nucleation, σ_{nucl}, at the node. From Equation (1),

$$t_{nucl} = \left(\frac{\sigma_{nucl}\Omega}{\rho e Z^*}\sqrt{\frac{\pi}{4}}\sqrt{\frac{kT}{B\Omega}}\frac{\sum_i \sqrt{D_i}}{\sum_i D_i j_i}\right)^2 . \qquad (2)$$

Once a void nucleates, it starts growing and leads to a resistance increase in one of the limbs. Assuming that the void spans the whole width and thickness of the interconnect, the void length as a function of time, t, is given by

$$L_v = \frac{Z^* e\rho}{kT} t \sum_i D_i j_i . \qquad (3)$$

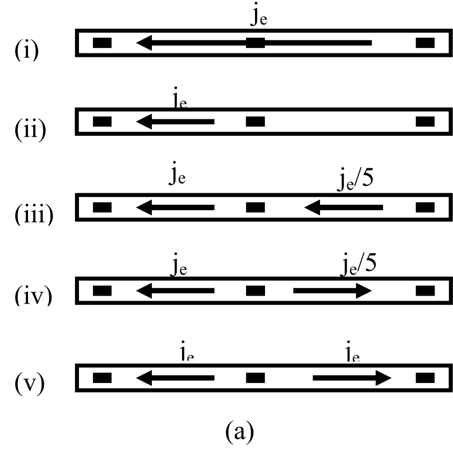
The corresponding resistance increase, ΔR, of the segment is then given by

$$\frac{\Delta R}{R_o} = \frac{L_v}{L}\left(\frac{\rho_l A_{Cu}}{\rho_{Cu} A_l} - 1\right) , \qquad (4)$$

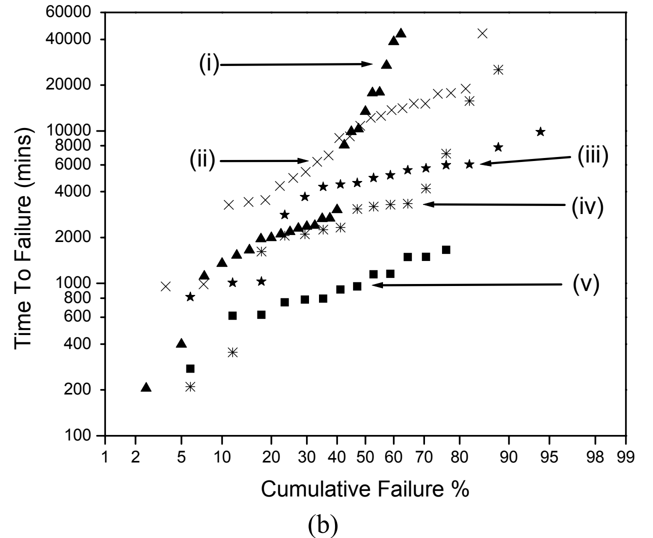
where R_o is the initial resistance of the line, L is the initial length of the conductor, ρ is the electrical resistivity, A is the cross-sectional area of the specific layer and the subscripts l and Cu refer to the diffusion barrier liner and Cu metal conductor, respectively. The time at which one of the segments exceeds an acceptable resistance increase, t_{grow}, is thus given by

$$t_{grow} = \frac{LkT}{Z^* e\rho}\frac{1}{\sum_i D_i j_i}\frac{\Delta R}{R_o}\left(\frac{\rho_{Cu} A_l}{\rho_l A_{Cu} - \rho_{Cu} A_l}\right) . \qquad (5)$$

The time-to-failure of a node due to voiding, t_{void}, is taken to be the maximum of t_{nucl} and t_{grow}. Similarly, the TTF of the node due to extrusions, $t_{extrusion}$, can be derived by considering the critical compressive stress for dielectric failure. The time-to-failure for the node, t_{fail}, is then conservatively estimated to be the minimum between t_{void} and $t_{extrusion}$. All the nodes of an interconnect tree are evaluated individually and the smallest t_{fail} is taken to be the lifetime of the interconnect tree.



(a)



(b)

Figure 2: (a) Schematic diagrams of dotted-I test structures with the five different current configurations used in the experiments. Tests were carried out at T = 350°C and j_e = 2.5 MA/cm^2. The arrows show the direction of electron flow. (b) Times-to-failure for 500μm-long, 0.28μm-wide dotted-I structures with the different electron current configurations shown in (a).

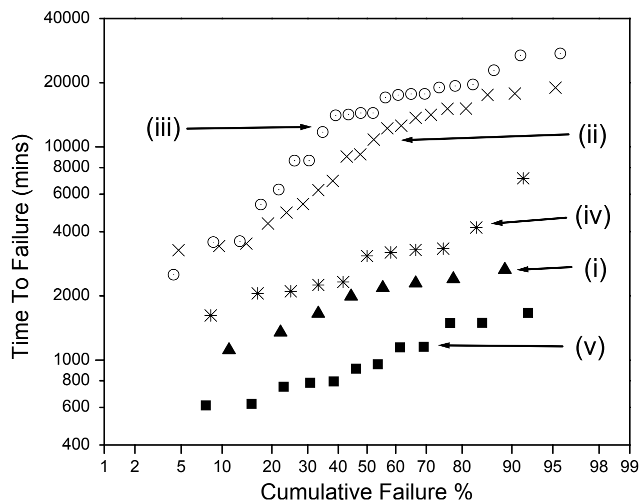


Figure 3: Times-to-failure of the left segments of dotted-I structures for cases (ii) to (v) and the lower lifetime distribution in case (i). This trend is similar to the one observed in Al dotted-I interconnect trees [4].

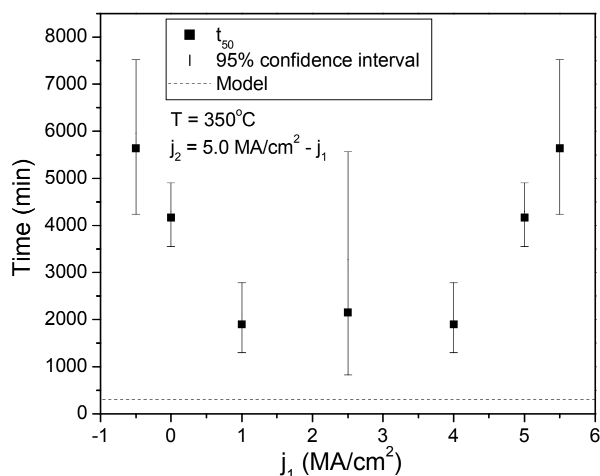


Figure 4: Distribution of failure times of the dotted-I interconnect tree (i.e. Figure 1(a)) with a constant current density of 5.0 MA/cm^2 through the middle via.

IV. EXPERIMENTAL RESULTS

Figure 2(a) shows five different current configurations that were used in tests of the dotted-I structures. A constant current density of j_1 = 2.5 MA/cm^2 was applied in the left segment, while a current density with varying direction and magnitude, j_2, was used to stress the right limb (segment). The distribution of the times-to-failure, TTFs, of the dotted-I structures is plotted on a lognormal scale in Figure 2(b). Failure was defined as the minimum time needed for a 30% increase in the resistance in either one of the segments in the test structure. The lognormal plots indicate that the lifetime of the left-hand segment of the test structure depends on the

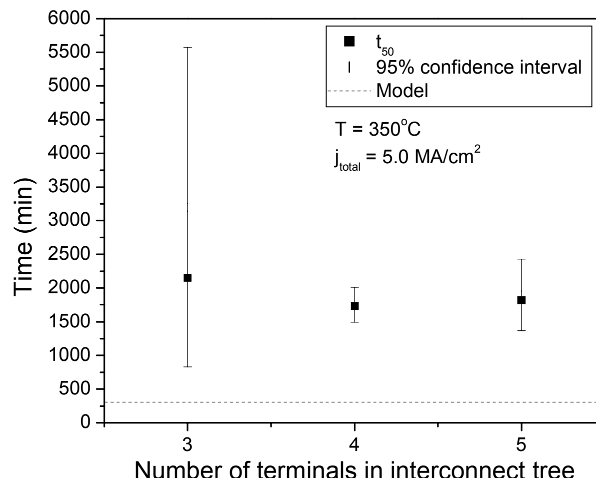


Figure 5: Distribution of failure times of dotted-I (3-terminal), T (4-terminal) and cross (5-terminal) interconnect trees with a constant current density of 5.0 MA/cm^2 through the middle via.

current configuration in the right-hand segment, with t_{50} increasing from case (v) to case (i). Figure 3 shows the TTFs of the *left* segment for cases (ii) to (v) and the lower lifetime distribution of case (i) in Figure 2. The trend seen in Figure 3 is similar to the one observed in Al dotted-I interconnect trees [4].

Figure 4 shows the distribution of failure times for the dotted-I interconnect tree shown in Figure 1(a), with different distributions of a 5.0 MA/cm^2 current density into the two adjoining segments through the middle terminal. Our experimental results show an increase in reliability when the current distribution was not equal in the two connected segments, which is contrary to the results predicted by the analytical model based on the Al results [4]. Figure 5 shows the distribution of failure times of different types of Cu interconnect trees with the same current density through the middle via. Our experimental results qualitatively agree with the expectations derived from the analytical model, in that the reliability of these Cu interconnect trees is independent of the number of segments connected at the middle via.

Focused-ion-beam (FIB) and transmission-electron-microscopy (TEM) analyses were carried out on selected stressed samples to study the failure mechanisms. It was verified that the formation of voids that fully spanned the M2 line in the vicinity of the vias have resulted in the open-circuit failures observed in their resistance measurements [12, 15].

V. DISCUSSION

The lognormal plot in Figure 2(b) shows that the direction and magnitude of the electron current in the right segment of the dotted-I structure affects the overall

reliability of the whole interconnect tree. The t_{50} increases from test configuration (v) to (i), which is different from what was observed previously for Al metallization [4].

For configuration (v), electrons move from the middle via to the two outer vias, with the same electron current density in both segments and twice the electron current density in the middle via. With the Ta liners at the bottom of the vias acting as sites for atomic flux divergence, a tensile hydrostatic stress rapidly builds up in the middle via until void nucleation occurs. FIB analysis has shown that voids formed in the middle of the line where the tensile stress is the largest, resulting in simultaneous failure of both the right and left segments.

In case (iv), the current density in the right limb was decreased to 0.5 MA/cm^2 while it was kept at 2.5 MA/cm^2 in the left limb. With decreased current density flowing away from the middle node (via) into the right segment, the total electromigration driving force through the middle via was reduced, causing a corresponding decrease in the total copper atomic flux away from the middle node. Thus both t_{nucl} and t_{grow} are larger than those in case (v). As a result, the observed t_{50} for this test condition is higher than in case (v).

Configuration (iii) is similar to case (iv) except that the 0.5 MA/cm^2 current density in the right segment was in the reverse direction. It was observed that the t_{50} of the dotted-I structure in case (iii) is higher than that in case (iv). In case (iv), the right segment is an active sink for metal atoms, draining more Cu atoms from the middle via. However, in case (iii) the right segment is an active source of Cu atoms for the middle via, so that the net flux of atoms moving away from the middle via is reduced and the rate of increase of the tensile stress in the middle via is correspondingly reduced so that the lifetime of the left limb, and therefore the entire tree, is increased. For this testing configuration, the lifetime of the right limb (j_2 = 0.5 MA/cm^2) was lower than that of the left limb (j_1 = 2.5 MA/cm^2). This implies that the Cu atoms flowing from the right via towards the middle via, had sufficiently slowed down the rate of void growth at the middle via such that fatal voids were more likely to form at the right-hand via.

In case (ii), the right limb had no current during tests and was therefore a passive reservoir that acted as a source of Cu atoms for the middle via. This slowed the build-up of tensile stress, increasing the lifetime of the structure compared to cases (iv) and (v). However, the t_{50} for this configuration was lower than that of the *left* segment in the previous case (iii), which is the same phenomenon as observed for Al dotted-I structures [4]. In case (iii), the right segment was acting as an active source of Cu atoms for the middle terminal, and the right limb was *drained* of Cu atoms at a sufficient rate that the right limb failed *faster* than the left limb. The lower overall lifetime of the interconnect tree for testing configuration (iii) is due to the failure of the right limb instead of the left limb. This result is different from what was found for Al, and could be due to the lower barrier to void nucleation in Cu than for the case of Al, as has also been indicated by other studies [8, 9]

For configuration (i), we observed a bimodal distribution of failure times, as shown in Figure 2(b). The lower lifetime distribution in this case has a t_{50} that is actually lower than that of case (iv). This trend is the same as reported for Al dotted-I structures [4]. On the other hand, the higher lifetime distribution has the largest t_{50} compared to all other cases, with about 46% of the samples not failing after more than 800 hours of stressing. This failure characteristic is also different from that of Al-metallization. In the Al dotted-I structures, the lines terminated at W-filled vias that acted as perfectly blocking boundaries to Al atom flow. In our Cu dotted-I structures, the Ta liner at the bottom of the via could be as thin as 30Å, which acted as the blocking boundary to the flow of Cu atoms. However, the high stresses that evolve at longer lines can cause rupture of this thin diffusion-barrier layer [11]. If this occurs, the vias no longer act as sites for flux divergence and the lifetime of the test structure increases substantially [10].

The TTFs of the *left* segments for cases (ii) to (v) and the lower lifetime distribution of case (i), where voids were observed near the middle via and right via respectively, are plotted in Figure 3. The trend seen in this case is similar to the one observed for Al dotted-I interconnect trees [4], as the failure locations are the same for the two cases. However, the actual TTF trends for the Cu dotted-I interconnect trees, as shown in Figure 2(b), is significantly different. These discrepancies are mainly due to the possibility that liners at vias may not provide fully blocking boundaries and the low barrier to void nucleation at the Cu/Si_3N_4 interface. As a result, failures do not necessarily always occur in the most highly stressed segment of an interconnect tree.

As shown in Figure 4, the analytical model developed for the analysis of nodes in Al interconnect trees [4] predicts that the lifetime of the dotted-I structure is independent of the current distribution through the middle terminal. However, our experimental results for Cu dotted-I clearly show an increase in the reliability when the current distribution of 5.0 MA/cm^2 was not equal in the two connected segments. This is especially so for the cases when the right segment is acting as a reservoir (j_2 = 0 MA/cm^2) or an active source of Cu atoms (j_2 = -0.5 MA/cm^2). It is believed that the low barrier for void nucleation at the Cu/Si_3N_4 interface [8, 9] in Cu dotted-I structures results in a different failure mechanism as compared to that of Al dotted-I structures. For the case of j_2 = -0.5 MA/cm^2, in the Cu dotted-I structures, most of the failures were detected in the right segment whereas in Al trees, failures occurred in the left segment for a similar test condition. It was observed that the time-to-failure did not change significantly even when the electron current draining from the middle via into the left segment was increased from 2.5 MA/cm^2 to 5.5 MA/cm^2, with the right segment acting as a source with a constant current density of 0.5 MA/cm^2. However, it is interesting to note that for the case of j_1 = 2.5 MA/cm^2, all

failures occurred in the right segment while for j_1 = 5.5 MA/cm^2, about 33% of failures actually occurred in the left segment.

The distribution of failure times of 3-, 4- and 5-terminal Cu interconnect trees with the same current density through the middle via is shown in Figure 5. According to the analytic model, the time-to-failure of an interconnect is determined by the larger value between the time to void nucleation and the time for void growth. As the critical stress for void nucleation at the Cu/Si_3N_4 interface is low, the void nucleation time is correspondingly short compared to the void growth time. As a result, the reliability of these Cu interconnect trees depends strongly on the total current density through the common middle terminal as predicted in Equation (5), and is thus independent of the number of segments connected at the middle via. Our experimental results qualitatively agree with expectations based on Al results, although the analytical model gives a very conservative estimate of the lifetimes of the test structures.

VI. CONCLUSIONS

Our experimental results for Cu-based dotted-I interconnect trees are in some ways similar to those reported for Al [4]. The reliability of a given segment depends on the magnitude and direction of the electron current in a neighboring segment, and the analytic model based on a nodal reliability analysis developed for Al interconnect trees also gives a conservative reliability estimate for Cu trees.

There are also important differences in the trends of times-to-failure of Cu and Al dotted-I structures. One of these differences is that the most highly stressed segment in an interconnect tree may not be the least reliable, possibly due to the low critical stress for void nucleation at the Cu/Si_3N_4 interface. Another significant distinction is that the liners at the base of vias in dual-damascene Cu technology do not provide fully-blocking boundaries like the W-filled vias in Al metallization. This means that the reliability of trees can be affected by the reliability of neighboring trees that are in *different levels of metallization*. As a result, the interconnect tree, which has been shown previously to be the fundamental reliability unit for Al metallization schemes, is not a fundamental unit for Cu technology.

It has been suggested that individual vias should be the focus of reliability analyses [15]. However the reliability of vias depends on the stress conditions of all adjacent segments, and the reliability of these segments depend, in turn, on the stress conditions of their neighbors. Via or node-based reliability analyses must either be based on worst-case analytic models, or on as much information as possible about the stress conditions of segment neighborhoods.

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