

MOSFET Channel Engineering using Strained Si, SiGe, and Ge Channels

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Abstract—Biaxial tensile strained Si grown on SiGe virtual substrates will be incorporated into future generations of CMOS technology due to the lack of performance increase with scaling. Compressively strained Ge-rich alloys with high hole mobilities can also be grown on relaxed SiGe. We review progress in strained Si and dual channel heterostructures, and also introduce high hole mobility digital alloy heterostructures. By optimizing growth conditions and understanding the physics of hole and electron transport in these devices, we have fabricated nearly symmetric mobility p- and n-MOSFETs on a common $\text{Si}_{0.5}\text{Ge}_{0.5}$ virtual substrate.

Index Terms—SiGe, strained silicon, germanium, MOSFETs, hole mobility

I. INTRODUCTION

Epitaxial relaxed SiGe buffer layers [1] create a larger lattice constant on a Si substrate, allowing subsequent SiGe layers to be strained in tension or compression. Early work in application of strain via relaxed SiGe concentrated on investigating elevated carrier mobility in pure tensile Si layers deposited on relaxed $\text{Si}_{1-x}\text{Ge}_x$. [2][3]. Relatively short channel MOSFETs containing strained Si have shown that higher mobility and drain current measured in long channel devices are retained at shorter channel lengths. [4][5] A quantitative method to correlate the effect of mobility enhancement in long and short channels shows that approximately 50% of the long channel drain current enhancement is obtained in shorter channels. [6] Thus, large MOSFET devices can be used to rapidly probe heterostructures for channel enhancement, as well as limits to processing. [7][8] In this summary, we report on advanced SiGe heterostructures to understand the potential of strained Si/SiGe heterostructures in MOSFETs.

II. SINGLE STRAINED SI CHANNELS ON RELAXED $\text{Si}_{1-x}\text{Ge}_x$

In strained Si surface channel n-MOSFETs, mobility enhancements increase linearly with strain up to about 20%

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Ge, saturating at roughly 80% enhancement. [7] For strained Si on virtual substrates with greater than 20% Ge content, the subband splitting in the conduction band is large enough to completely suppress intervalley scattering (figure 1a). Holes also have increased mobility in strained Si due to subband splitting (figure 1b); however, greater strain levels in the strained Si are required to achieve the same hole mobility enhancement as achieved for electrons. Unlike electrons, the in-plane and out-of-plane mobility of holes in strained Si also increases, resulting in a more complicated picture of hole transport. Fig. 2 shows the carrier mobility enhancement factors for electrons and holes as a function of Ge concentration in the relaxed $\text{Si}_{1-x}\text{Ge}_x$. The data are extracted from one-mask-step large gate length MOSFETs (figure 3) that have vertical electric fields in the channel comparable to MOSFETs with shorter gate lengths. The data for $x < 0.5$ are from references [7][8].

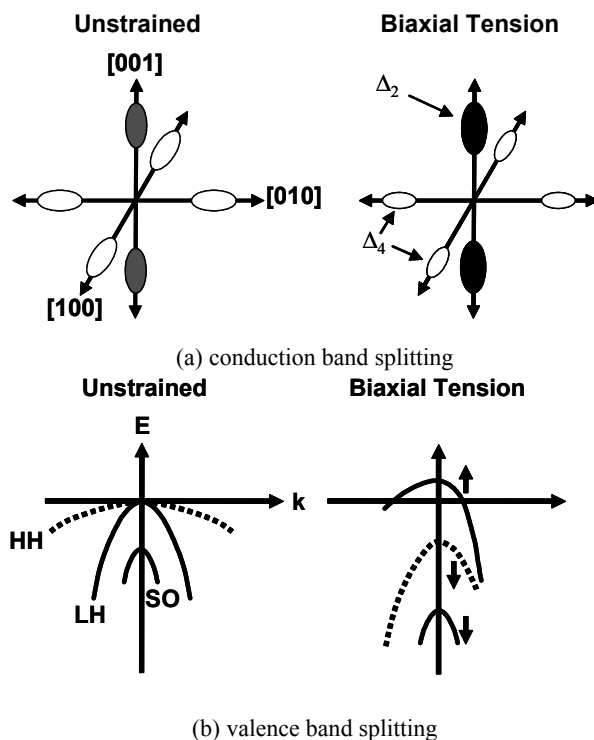


Fig. 1 Qualitative picture of strain induced splitting of conduction band (a) and valence band (b) in strained Si

We report that mobility enhancement (enhancement factor 2.7) in strained Si PMOS devices can continue to increase with $x > 0.5$, despite the theoretical suppression of intervalley scattering at $x = 0.4$. The unexpected jump in hole

mobility enhancement for surface strained Si on $\text{Si}_{0.3}\text{Ge}_{0.7}$ is explained in more detail in section IV. Planar strained Si layers (partially relaxed through the introduction of dislocations) have been achieved on all buffer layer compositions, including pure Ge by very low temperature chemical vapor deposition ($T \leq 400^\circ\text{C}$).

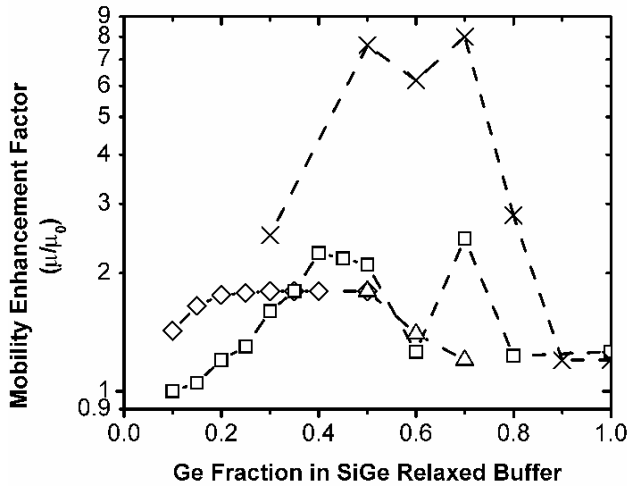


Fig. 2 Summary of mobility enhancements extracted from one-mask-level, large MOSFETs with a vertical effective field of approximately 0.6 MV/cm: single channel NMOS (diamonds), single channel PMOS (squares), dual channel NMOS (triangles), dual channel PMOS (crosses).

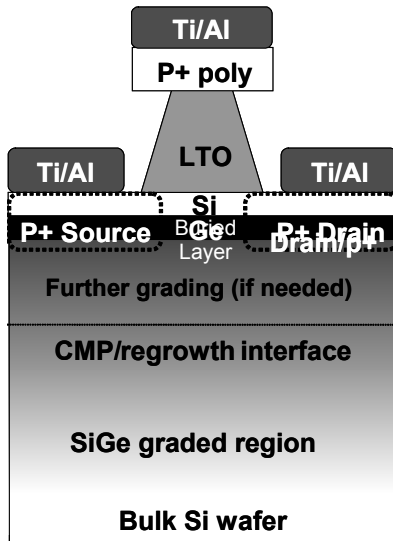


Fig. 3 Schematic of the short-flow MOSFET for quickly probing advanced SiGe heterostructures

III. DUAL CHANNEL HETEROSTRUCTURES ON $\text{Si}_{1-x}\text{Ge}_x$

Although hole mobility enhancements of 2.7 are even larger than the maximum electron mobility enhancement, we have shown that incorporating a compressively strained $\text{Si}_{1-y}\text{Ge}_y$ layer below the tensile-strained surface Si layer increases the hole mobility to an even greater extent [9]. Electron mobility is unaffected in these dual channel heterostructures

due to the type II band alignment of strained Si with SiGe (figure 4).

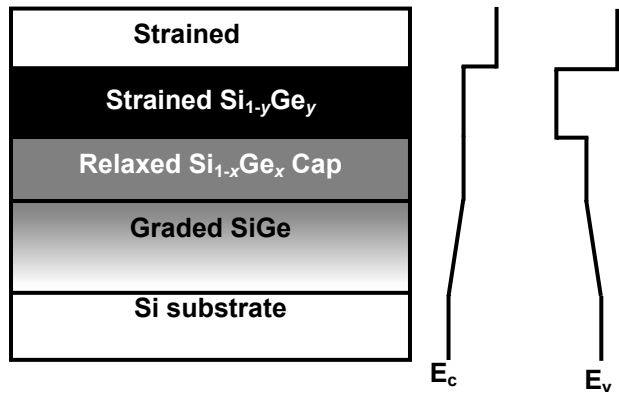


Fig. 4 Band alignments in dual channel heterostructures

In order to avoid strain induced undulations in the buried compressive layer, the channel must be grown at $350\text{-}400^\circ\text{C}$. Direct comparison of severely undulated layers grown at 550°C with planar layers grown at 400°C shows that morphology is a key factor in determining hole mobility. Our UHV-CVD system allows high quality growth with little impurity incorporation despite growth rates as low as 10^{-3}A/s . All dual channel heterostructures in our research are capped with a layer of pure strained Si in order to maintain compatibility with SiO_2 gate technology.

Dual channel heterostructures with $y=0.6$ to 1.0 have shown hole mobility enhancement factors in p -MOSFETs from 2.5 to 8 times. The highest hole mobilities were measured in structures consisting of pure Si and pure Ge strained layers, and the 8 times mobility enhancement was maintained at fields as high as 0.65 MV/cm [10]. Previous work with integration of strained Ge onto $\text{Si}_{1-x}\text{Ge}_x$ utilized virtual substrates with $x=0.7$. The high mismatch between Si and $\text{Si}_{0.3}\text{Ge}_{0.7}$ caused a high density of threading dislocations to nucleate in the Si cap (figure 5). While hole mobility appears to be unaffected by the presence of defects, the electron mobility enhancement is slightly degraded to ~ 1.5 . Thus a lower virtual substrate composition may be needed to integrate the highest mobility electron devices with the highest mobility hole devices, and this particular challenge is addressed in section V.

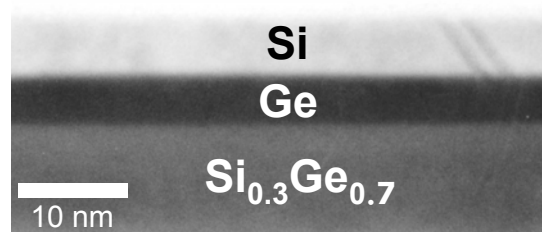


Fig. 5 Cross-section TEM of strained Ge dual channel heterostructure. Note the defects in the Si cap layer.

We have also used dual channels to demonstrate that alloy scattering does not preclude high hole mobility in

compressively strained $\text{Si}_{1-y}\text{Ge}_y$ alloy channels, despite the $y \cdot (1 - y)$ dependence of alloy scattering. Figure 6 shows the effective mobility of pMOSFETs fabricated with a variety of buried alloy channels. In all devices, the compressive strain in the buried layer was held at 1.3%.

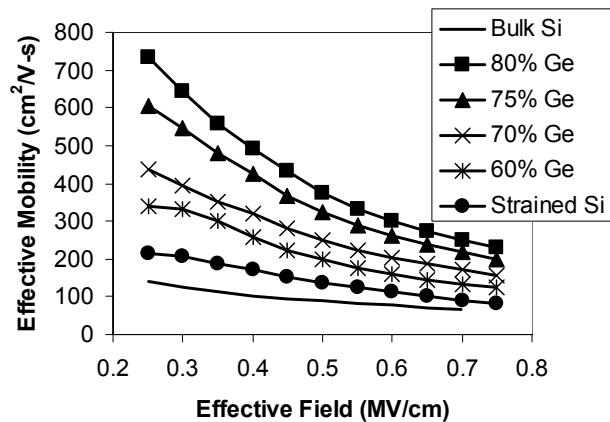


Fig. 6 Effective Mobility of dual channel pMOSFETs fabricated with various buried channel alloy compositions and constant strain.

Because the vertical field changes the position of the hole wave function with respect to the buried and surface layers, the layer thicknesses strongly affect mobility enhancements. Figure 7 is a plot of hole mobility enhancement over bulk Si versus vertical field for a series of strained Si/ $\text{Si}_{0.4}\text{Ge}_{0.6}$ structures grown on relaxed 30% Ge virtual substrates. In this plot, thin layers are 40 Å while thick layers are 85 Å. These plots clearly illustrate the advantage of having a thin strained Si surface layer. The sample with an 85 Å $\text{Si}_{0.4}\text{Ge}_{0.6}$ channel and a 40 Å strained Si cap displays the highest mobility enhancement over the entire range of vertical fields investigated. In this case, the strained Si layer is too thin to allow significant hole population, forcing holes to occupy the high mobility buried channel. The strained Si surface layer should have even less influence for higher Ge content channels, where the large band offset between the buried compressive $\text{Si}_{1-y}\text{Ge}_y$ and surface Si effectively confines holes within the buried layer. Thus, the extent to which dual channel heterostructures are buried or surface channel devices can be modulated by varying channel thicknesses.

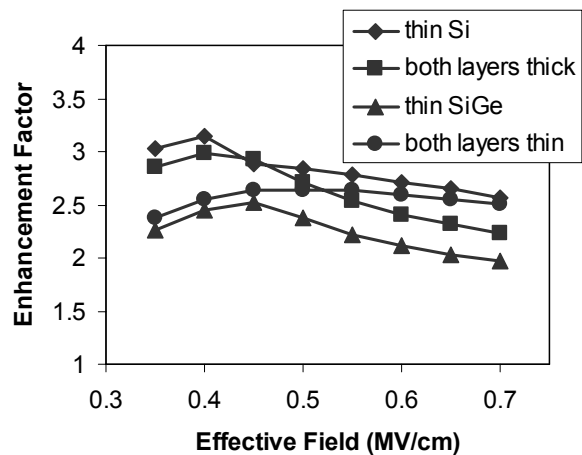


Fig. 7 Mobility enhancement factor for dual channel heterostructures (strained Si surface/ $\text{Si}_{0.4}\text{Ge}_{0.6}$ buried) and the effect of varying layer thicknesses. “Thin” layers are 40 Å and “thick” layers are 85 Å.

Clearly, a tremendous amount of flexibility can be introduced to the engineering of strained layer MOSFETs through the use of dual channel heterostructures. Fig. 2 summarizes the best carrier mobility enhancements in large research MOSFETs achieved to date for different heterostructures on relaxed $\text{Si}_{1-x}\text{Ge}_x$ on Si.

IV. THIN STRAINED SI ON RELAXED $\text{Si}_{1-x}\text{Ge}_x$ AND DIGITAL ALLOY CHANNELS

Combining the single channel and dual channel data, we speculate that the heterostructures in many of the PMOS devices have a thickness less than the vertical extent of the hole wavefunction and therefore the properties of the hole are determined by a combination of the hole wavefunction in the gate dielectric, the strained Si, the compressed $\text{Si}_{1-y}\text{Ge}_y$ (if present), and the relaxed $\text{Si}_{1-x}\text{Ge}_x$ alloy. Layer thickness and vertical electric field are variables in determining the character of the hole wavefunction in the channel. The hybridization of the hole wavefunction explains the unexpected jump in hole mobility for surface strained Si grown on $\text{Si}_{0.3}\text{Ge}_{0.7}$. At high E_{eff} , the hole mobility in thin (~40 Å) strained Si on relaxed $\text{Si}_{0.3}\text{Ge}_{0.7}$ actually approaches the mobility of a dual channel device with a buried, compressed $\text{Si}_{0.3}\text{Ge}_{0.7}$ layer (figure 8).

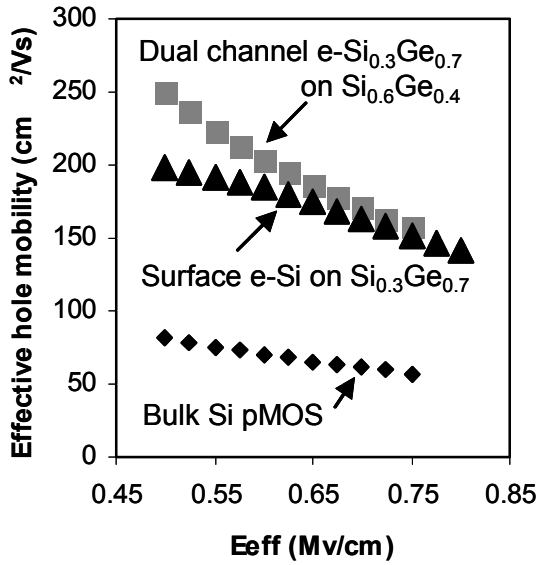


Fig. 8 Hole mobility of strained Si on $\text{Si}_{0.3}\text{Ge}_{0.7}$ compared to mobility of dual channel heterostructure

For a sufficiently thin Si cap, the hole can hybridize the valence band splitting of the strained Si with the low effective mass of the relaxed $\text{Si}_{0.3}\text{Ge}_{0.7}$, effectively reproducing the valence band of a compressed layer without ever growing one. This effect is qualitatively outlined in figure 9. At low field, the hole transport is primarily dominated by the relaxed $\text{Si}_{0.3}\text{Ge}_{0.7}$. Since the SiGe is relaxed, its valence band is degenerate and intervalley scattering operates as a mobility limiting mechanism.

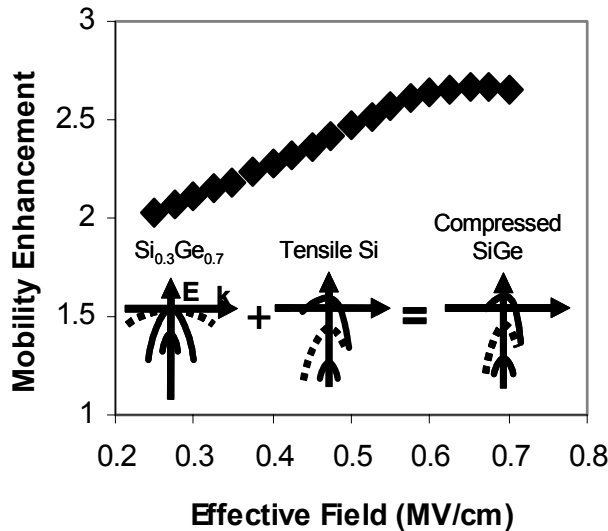


Fig. 9 Qualitative picture of hybridization of valence band structure for thin ($\sim 40\text{\AA}$) strained Si grown on relaxed $\text{Si}_{0.3}\text{Ge}_{0.7}$ alongside measured hole mobility enhancements

As the gate overdrive is increased, the centroid of the wave function is pulled closer and closer to the surface, and the hole

begins to sample the valence band splitting in the e-Si cap. Since the Si cap is so thin for this structure, the hole can never be completely confined at the surface.

To further elucidate this observation, we have built a digital alloy channel (greater than 100\AA in total channel thickness) composed of extremely thin layers of tensile Si and $\text{Si}_{0.3}\text{Ge}_{0.7}$ on a relaxed $\text{Si}_{0.3}\text{Ge}_{0.7}$ substrate (Fig.10).

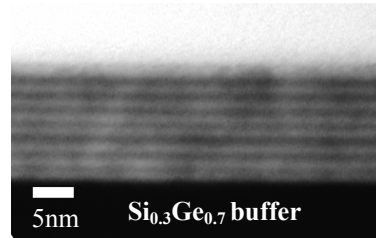


Fig. 10 Cross-section TEM of digital alloy channel. Bright layers are e-Si, dark layers are $\text{Si}_{0.3}\text{Ge}_{0.7}$

In this way, we have hybridized the top surface Si in our previously discussed single channel structure with the buried relaxed $\text{Si}_{0.3}\text{Ge}_{0.7}$. The p -MOSFETs fabricated from this material show that the mobility enhancement factor (2.1) is independent of vertical field, as expected since the wavefunction is averaging over all of the digital alloy layers at all electric field values (figure 11). Cross sectional TEM of the digital alloy after MOSFET processing revealed that our low thermal budget process did not cause significant interdiffusion and that the interfaces between the thin “digits” were still sharp. We also note that compositionally, the digital alloy is equivalent to a tensile $x=0.35$ random alloy on relaxed $\text{Si}_{0.3}\text{Ge}_{0.7}$, which has been shown to have a degraded mobility compared to bulk Si.[8]. Even though the layers comprising the digital alloy are on the order of several atomic layers thick, the hole does not suffer from alloy scattering and is able to combine the unique benefits intrinsic to each component of the alloy.

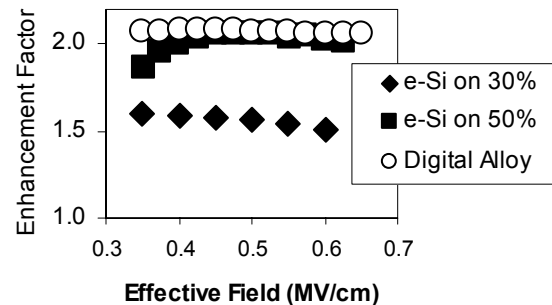


Fig. 11 Mobility enhancement of digital alloy PMOSFET plotted alongside conventional strained Si devices

V. SYMMETRIC MOBILITY N- AND P-MOSFETs ON A SINGLE SUBSTRATE – THE ULTIMATE DUAL CHANNEL

Our work with digital alloy structures demonstrates the spreading of the hole wave function over nanometer-scale layers and how each layer contributes to the effective

mobility. The observation of hybrid wave functions also has important implications in the design of optimal compressive Ge heterostructures due to the strain-induced lowering of the out-of-plane effective mass of holes in Ge. We grew strained Ge/strained Si dual channel heterostructures on $\text{Si}_{0.3}\text{Ge}_{0.7}$ and $\text{Si}_{0.5}\text{Ge}_{0.5}$ virtual substrates (1.3% and 2% compressive strain, respectively). The strained Ge and strained Si layers were 60Å thick on both buffer compositions. If spreading of the hole wave function is ignored, theory would indicate that the structure grown on the 50% buffer would have higher mobility, both because of the lowered in-plane effective mass of holes and the larger ΔE_v between the strained Ge and relaxed SiGe. However, as seen in figure 12, the p-MOSFET with *lower* strain exhibits consistently higher mobility across the entire range of E_{eff} .

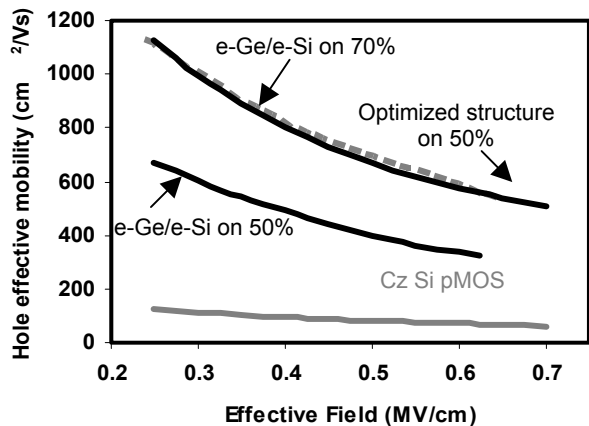


Fig. 12 Comparison of the 60Å Ge / 60Å Si structure grown on $\text{Si}_{0.5}\text{Ge}_{0.5}$, $\text{Si}_{0.3}\text{Ge}_{0.7}$ and the optimized structure

In Ge, compressive strain lowers the out-of-plane effective mass even more than the in-plane effective mass. Therefore, layers above and below the strained Ge can make a strong contribution to hole transport, and we are lead back to the concept of a hybrid wave function. In the structure grown on $\text{Si}_{0.5}\text{Ge}_{0.5}$, the higher compressive strain and higher out-of-plane mobility causes the hole wave function to penetrate further into the strained Si cap and the lower mobility relaxed buffer below. While the same hybridization takes place in the structure grown on $\text{Si}_{0.3}\text{Ge}_{0.7}$, the extent of the wave function is less and the hole mobility in the relaxed buffer is higher. To address the large wave function, we again deposited strained Ge onto $\text{Si}_{0.5}\text{Ge}_{0.5}$, but doubled the layer thickness to 120Å. By decreasing the weighting factor of the relaxed buffer on hole transport, the 8 times hole mobility enhancement was recovered (figure 12, “optimized” structure). n-MOSFET devices fabricated on the same wafers verify that the electron enhancement in strained Si is unaffected by the presence of the buried Ge layer, provided the cap is at least 50Å thick. Figure 13 shows that nearly symmetric mobility n- and p-MOSFETs can be fabricated on a single substrate. The high defect density in the Si cap is avoided due to the symmetric mismatch of the strained Ge and strained Si layers on $\text{Si}_{0.5}\text{Ge}_{0.5}$. Note that at low field, the hole mobility in the optimized dual channel heterostructure actually

exceeds the electron mobility and that the mobility of the n- and p-MOSFET never deviate from each other by more than 25%.

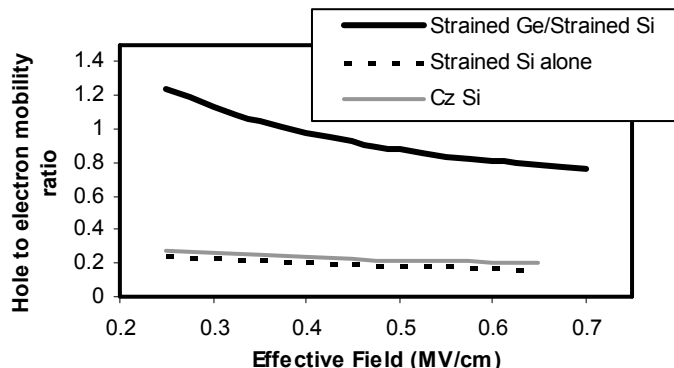


Fig. 13 Comparison of pMOS to nMOS mobility ratios in various CMOS implementations

VI. CONCLUSIONS

Short flow, one-mask-step large MOSFETs have been used to explore the potential of heterostructure CMOS channels. Electron mobility enhancements as high as 1.8 and hole enhancements of over 8 have been achieved. The ability of the hole to hybridize different band structures in nanometer scale layers explains unexpected improvements in hole mobility (thin strained Si on $\text{Si}_{0.3}\text{Ge}_{0.7}$) as well as unexpected degradations in hole mobility (60Å strained Ge on $\text{Si}_{0.5}\text{Ge}_{0.5}$). Strained Si p-MOSFETs display moderate enhancements in hole mobility over bulk Si, and are relatively simple to incorporate into CMOS processes. Dual channel heterostructures display large hole mobility enhancements (and identical mobility to strained Si surface channel n-MOSFETs), and hole mobility increases with buried channel Ge content. However, as Ge content increases, these layers become more difficult to grow and incorporate into CMOS processes. Essentially, this is analogous to traditional CMOS scaling, where each technology node (gate length) brought increased performance but required extensive research and development. Now, with Ge content as the new scaling parameter, each step in Ge composition will greatly increase performance but will also require thorough optimization of growth and process parameters. SiGe-based heterostructure MOSFETs not only offer the potential for greatly increased MOSFET performance, they also emerge as the new scaling platform as traditional device scaling comes to an end. Device modeling studies indicate that subthreshold characteristics are degraded in both n-MOSFETs and p-MOSFETs based on dual channel heterostructures, so an acceptable trade-off between drive current enhancements and subthreshold characteristics needs to be determined. In general, the key question remaining to be answered in these devices is: will the tremendous increases in hole mobility translate into increased

overall circuit performance? While the high mobilities in these heterostructures demonstrated are an important first step, individual device performance needs to be placed into the context of overall circuit design issues (such as cost versus performance). Finally, in a fashion similar to surface channel strained Si MOSFETs, process optimization studies should be undertaken in state-of-the-art MOSFETs based on these heterostructures in order to determine the unique processing requirements for this class of devices.

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