SiGe-On-Insulator (SGOI): Two Structures for CMOS Application

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Abstract **– Two SiGe-on-insulator (SGOI) structures for CMOS application are presented: surface-channel strained-Si on SGOI (SSOI) and dual-channel SGOI structures. Comparisons between two structures are made from both device performance and CMOS process point of view. We have demonstrated both structures on SGOI, and have fabricated n-MOSFET's and p-MOSFET's on those two structures respectively. Device characteristics are presented. The devices show enhancement on both electron and hole mobilities.**

Keywords **– strained-Si, SiGe, SiGe-on-Insulator, SGOI, strained-Si on SGOI, SSOI, SOI, dual-channel, surface channel, MOSFET, mobility, bonding, etch-back.**

I. Introduction

Relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) is a very promising technology, as it combines the benefits of two advanced technologies: the conventional SOI technology and the SiGe technology. SiGe-based devices have shown advantageous dc and rf performance using the enhanced electronic properties associated with strain engineering and heterojunction energy barriers. SOI configuration brings in more advantages associated with an insulating substrate. Relaxed SGOI is also a versatile substrate that can be used to integrate various device structures, such as strained-Si devices on SGOI, pure Ge devices on SGOI, and III-V optoelectronics on SGOI, utilizing SGOI's capability of matching the lattice constant of SiGe with other materials.

One promising application of SGOI technolgy is to improve the performance of CMOS technology. We have demonstrated ealier [1-2] that by using tensile strained-Si layer grown on relaxed SGOI substrate (SSOI structure), significant electron mobility enhancement was obtained on surface channel strained-Si n-MOSFET's. Such a surface-channel SSOI structure has been considered as a promising structure for high mobility CMOS [3-6], with enhancement of both electron and hole mobilities. Nevertheless, although SSOI provides significant enhancement on hole mobility, the hole mobility is still about 4-5 times lower than electron mobility in the SSOI CMOS.

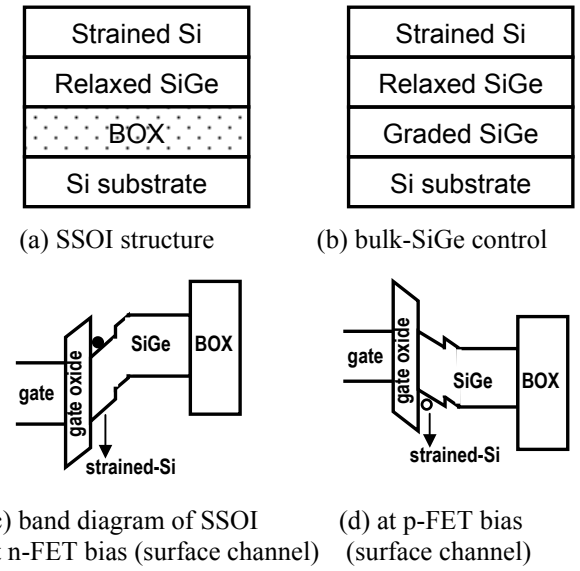
To further boost hole mobility, compressively strained $Si_{1-y}Ge_y$ grown on relaxed $Si_{1-x}Ge_x$ structure (y>x) can be used for p-MOSFET's [7]. A dual-channel structure combining a tensile strained Si layer for n-MOSFET's and a compressively strained $Si_{1-y}Ge_y$ layer for p-MOSFET's was proposed for a possible structure for CMOS. Our research group in MIT has demonstrated ealier such a dual-channel structure on bulk relaxed SiGe substrate, and has demonstrated significant hole mobility enhancement (up to 5.15 times at field of 0.3 MV/cm for 80% strained-SiGe on 50% relaxed-SiGe) on p-MOSFET's [8]. It is of great interest to demonstrate such a dual-channel structure on SGOI substrate.

In this paper, we demonstrate both those two structures on SGOI, and study n-MOSFET and p-MOSFET devices for CMOS application. In the first structure, the SSOI structure, a tensile strained Si is grown on a relaxed SGOI substrate where the relaxed SiGe layer has Ge fraction of 22%, as shown schemetically in Fig. 1(a). In the second structure, the dual-channel SGOI structure, a compressively strained $Si_{0.4}Ge_{0.6}$ layer and then a tensile strained Si layer are grown on relaxed SGOI substrate where the relaxed SiGe layer has Ge fraction of 30%, as shown in Fig. 2(a). n-MOSFET's and p-MOSFET's were fabricated on those two structures respectively for device characteritic study.

II. Comparison of SSOI and Dual-channel SGOI Structures for CMOS

A. Surface-channel SSOI Structure for CMOS

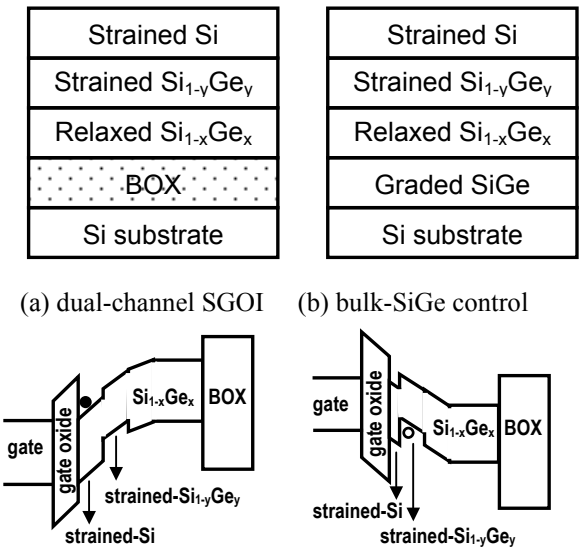
The surface-channel CMOS devices built on SSOI stucture provides enhancement on both electron and hole mobilities. The corresponding band diagrams of SSOI under n-FET and p-FET bias condition are illustrated in Fig. 1(c) and (d) respectively. Electrons and holes are both populated at the surface strained-Si layer for n-MOSFET's and p-MOSFET's respectively. As surface channel devices, SSOI CMOS has advantage on subthreshold slope.



(a) SSOI structure (b) bulk-SiGe control

(c) band diagram of SSOI at n-FET bias (surface channel) (d) at p-FET bias (surface channel)

Fig. 1. Schematic layer sequence and band diagram for SSOI: (a) SSOI sturture: strained-Si on SGOI, (b) bulk-SiGe control: strained-Si/relaxed-SiGe on bulk Si substrate, (c) band diagram of SSOI under n-FET bias condition, and (d) band diagram of SSOI under p-FET bias condition, where holes are populated on the surface strained-Si layer (surface channel).



(a) dual-channel SGOI (b) bulk-SiGe control

(c) band diagram at n-FET bias (surface channel) (d) at p-FET bias (buried channel)

Fig. 2. Schematic layer sequence and band diagram for dual-chanel SGOI: (a) dual-channel SGOI structure: strained-Si and strained-$Si_{1-y}Ge_y$ on SGOI, (b) bulk-SiGe control: strained-Si/strained-$Si_{1-y}Ge_y$ /relaxed-$Si_{1-x}Ge_x$ (y>x) on Si substrate, (c) band diagram of dual-channel SGOI under n-FET bias condition where an electron channel forms on the surface strained-Si layer (surface channel), and (d) band diagram of dual-channel SGOI under p-FET bias condition where the hole channel forms on the buried strained-$Si_{1-y}Ge_y$ layer (buried channel).

It has been shown theoretically and experimentally that the electron and hole mobilities increase with the Ge fraction in the relaxed SiGe layer, but their dependence is different [9]. 15% Ge gives about 70% enhancement for electron mobility, and the enhancement appoarches saturation beyond 15% Ge. Similar enhancement on hole mobility requires much higher Ge content and hole mobility starts to saturate at 35% of Ge fraction based on theoretical predictions.

B. Dual-channel SGOI Structure for CMOS

Unlike surface channel SSOI CMOS, dual-channel SGOI structure ultilizes different layers for electron channel and hole channel. As shown in Fig. 2(a), the surface strained-Si layer is used for n-MOSFET's (surface channel), and the underneath strained-$Si_{1-y}Ge_y$ layer for p-MOSFET's (buried channel). The corresponding band diagrams under n-FET and p-FET bias condition are illustrated in Fig. 2(c) and (d) respectively. This structure features high hole mobility enhancement. Starting with a relaxed $Si_{0.7}Ge_{0.3}$ buffer, for example, a strained-Si layer provides n-MOSFET's over 80% mobility enhancement, while a strained-$Si_{0.4}Ge_{0.6}$ (60% Ge fraction) layer gives p-MOSFE's about 200% hole mobility enhancement as demonstrated by experiment in bulk SiGe substrate [8].

The n-MOSFET's require a thick enough strained-Si layer for its eletron surface channel. The p-MOSFET's, on the other hand, require the surface strained-Si layer to be very thin, otherwise parasitic hole channel will form in this strained-Si layer at high gate bias. That means in the CMOS process, the surface strained Si layer, starting thick for n-MOSFET's, should be etched to a thinner thickness, selectively on the p-MOSFET regions only, so that the holes will mainly populate on the buried strained $Si_{1-y}Ge_y$ layer. This represents a process challenge.

C. Comparison between surface-channel SSOI and dual-channel SGOI structure for CMOS

Table. I shows the comparison between the two SGOI structures for CMOS application: the surface-channel SSOI structure and dual-channel SGOI structure. The comparison also holds for their two counterpart structures on bulk-SiGe substrates: i.e. the surface-channel strained-Si/relaxed-SiGe on Si substrate and the dual-channel strained-Si/strained-$Si_{1-y}Ge_y$/relaxed-$Si_{1-x}Ge_x$ on Si substrate.

TABLE. I

COMPARISON BETWEEN SURFACE-CHANNEL SSOI AND DUAL-CHANNEL SGOI STUCTURE FOR CMOS

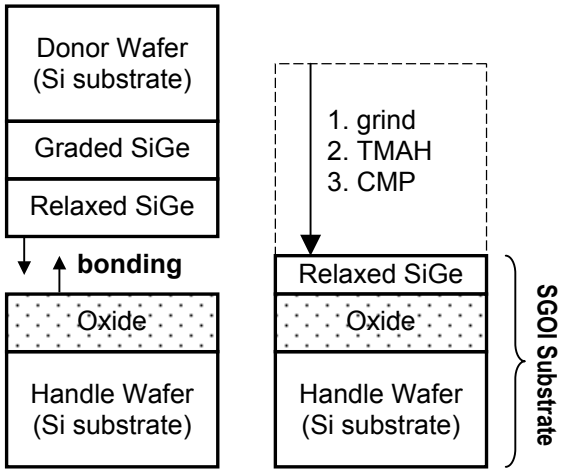
	Two SGOI structures for CMOS Application	
	Surface-channel SSOI structure: strained-Si on SGOI	Dual-channel SGOI structure: strained-Si/strained-$Si_{1-y}Ge_y$ on SGOI
Note: the comparisons also hold for the following counterpart structures on bulk-SiGe:		
bulk-SiGe counterpart	strained-Si/relaxed-SiGe on Si	strained-Si/strained-$Si_{1-y}Ge_y$/$Si_{1-x}Ge_x$ on Si
Electron mobility	High	High
Hole mobility	Moderate	High
Channel: surface or buried	Surface channel for both n- and p-FET's	Surface channel for n-FET's Buried channel for p-FET's
Strained-Si thickness	Same for n-FET's and p-FET's	Thicker for n-FET's, thinner for p-FET's
Parasitic channel for p-FET's	Parasitic channel may form in the relaxed SiGe layer at low bias	Parasitic channel may form in the surface strained-Si layer at high bias: The strained-Si layer need to be very thin to avoid parasitic channel
Process complexity	Simpler	More steps: thinning Si layer in p-FET region
Optimization for n-FET & p-FET	Can't optimize separately	Can optimize separately: strained-Si for n-FET, & strained-$Si_{1-y}Ge_y$ for p-FET

From device performance point of view, the surface-channel SSOI gives good subthreshold characteristics. The dual-channel SGOI structure, on the other hand, could provide much higher hole mobility than SSOI structure. It also has advantage to optimize strained-Si layer and strained-$Si_{1-y}Ge_y$ layer for n-FET and p-FET separately. But the present of the strained-$Si_{1-y}Ge_y$ layer may affect the performance of n-FET devices. From process point of view, selective etching the surface strained-Si layer on the p-MOSFET regions only and stopping at a thin Si thickness is a process challenge, and the process for dual-channel CMOS thus becomes more complicate than SSOI. Moreover, higher Ge fraction epi layer may subject to higher defect density during epi growth.

Since many aspects are involved as described above, extensive experiments and analysis need to be done to determine which is a better or more practical structure for SGOI CMOS. As a guide, when optimizing either structure for CMOS application, one needs to consider not only electron/hole mobility, but also the complete and overall device characteristics, and the process and epi growth aspects as well.

III. SGOI SUBSTRATE BY ETCH-BACK

Relaxed SGOI substrates used in this study were fabricated by an etch-back approach that we reported ealier [1-2]. The substrate fabrication process is illustrated schematically in Fig. 3. Starting with a 4-inch Si (100) donor wafer, high quality relaxed SiGe was grown at 900 ºC by ultrahigh vacuum chemical vapor deposition (UHV-CVD) using a graded $Si_{1-x}Ge_x$ buffer technique [10]. The Ge fraction *x* was graded from zero to 22% or 30% with a grading rate of 10% Ge/μm. A relaxed SiGe cap layer was deposited, as shown in Fig. 3(a). The slow grading rate and high growth temperature result in a completely relaxed cap layer with threading dislocation densities of ~10^5 cm^{-2} [11].



(a) epi and bonding (b) etch-back and CMP

Fig. 3. SGOI substrate fabrication processes via wafer-bonding and etch-back approach. (a) SiGe epi layer is grown on Si donor wafer and then bonded to oxidized Si handle wafer, (b) the bonded pair is ground and etched from donor wafer side and the CMP step results in a relaxed SGOI structure

The as-grown relaxed $Si_{1-x}Ge_x$ layer has a surface roughness of around 11 to 15 nm, due to the underlying strain fields generated by misfit dislocations at the graded layer interfaces. Thus chemical-mechanical polishing (CMP) was used to smooth the surface. After a cleaning step to render the surface highly hydrophilic, the donor wafer was fliped over and bonded to an oxidized Si handle wafer at room temperature, and then annealed at at 850 ºC for 1.5 hrs, as schematically shown in Fig. 3 (a). The bonded pair was then ground to remove the donor wafer substrate, as shown in Fig. 3(b). The wafer was then subjected to a TMAH solution to etch away the SiGe graded layer until reaching SiGe layer with Ge fraction greater than 20%, which acts as an etch-stop for TMAH [1-2]. The structure was further thinned by CMP to expose the relaxed SiGe cap layer, and a relaxed SGOI substrate results.

The relaxed SGOI substrates are then used to grow SSOI or dual-channel SGOI structures as described in the next section. As the device performance depends on Ge content, choosing the right Ge fraction is a matter of process and device optimization. In this work, we arbitrarily choose 22% of Ge on SGOI for SSOI structure, and 30% for dual-channel SGOI sturcture.

IV. SSOI Structure and Electrical Properties of n-MOSFET's

A. SSOI structure and n-MOSFET's Fabrication

To grow the SSOI structure, the SGOI substrates (with 22% Ge) were put back to UHV-CVD reactor for device layer growth. A relaxed SiGe layer with the same Ge mole fraction was grown first on the SGOI substrate, before the growth of a 18 nm-thick undoped strained-Si device layer at 650°C, resulting in a SSOI structure as shown in Fig. 1(a).

Full-mask partially-depleted n-MOSFET's with conventional FET structure were fabricated on those SSOI structures. A bulk-SiGe control structure, i.e. n-MOSFET's on strained-Si on relaxed bulk $Si_{0.78}Ge_{0.22}$ (strained-Si/relaxed-SiGe) was also co-processed, whose layer structure is shown in Fig. 1(b). All the devices fabricated in this work had a SiGe body contact. The gate oxide was grown by thermally oxidizing part of the strained Si layer at 800°C. The gate oxide thickness is around 5 nm. The final strained Si layer thickness on MOSFET's is expected to be 12 nm after process. The channel is doped by Boron ion implants (BF_2 : 17 keV, dose $4x10^{15}$ cm^{-2}) to a doping level of about 3E17/cm^3. Phosphorus ion implants (P: 15 keV, dose $4x10^{15}$ cm^{-2}) were performed to dope both the source/drain and poly gate regions, and the dopant was activated via furnace anneal at 850°C for 30min. The MOSFET's have channel length ranges from 0.5 μm to 400 μm.

Partially-depleted p-MOSFET's on the same SSOI and bulk-SiGe control structures, and fully-depleted n-MOSFET's and p-MOSFET's are also under process and will be reported later.

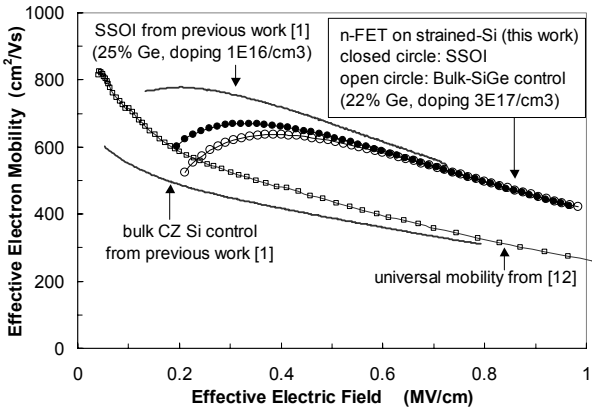


Fig. 4. Measured effective electron mobility vs. effective electric field from n-MOSFET's on SSOI structure and bulk-SiGe control structure. The mobilities are extracted from drain current with the inversion charge extracted from the gate-to-channel capacitance Cgc in Fig 5. The mobilities from our previous work [1] are also shown in the figure for comparision. The universal mobility is from [12].

B. Eletrical Properties of n-MOSFET's on SSOI

Fig. 4 shows the effective electron mobilities versus effective field from n-MOSFET's on SSOI structure and the bulk-SiGe control structure (strained-Si/relaxed-SiGe) respectively, ploted with the universal mobility from [12]. The mobilities are extracted from drain current measurements with low drain voltage and with the inversion charge extracted from the gate-to-channel capacitance Cgc from the same device, which is shown in Fig. 5. The gate-to-body capacitance (relaxed-SiGe body in the partially-depleted n-MOSFET's) is also shown in the figure. The electron mobilities from our previous work [1] are also shown in the figure for comparison, where on a similar SSOI substrate (Ge fraction of 25%, low channel doping of 10^{16} cm^{-3}) large-area ring-structure strained-Si *n*-MOSFET's with a thick deposited gate oxide (300nm) were fabricated utilizing a short-flow one-mask process, which is designed for mobility extraction mainly.

The plots show the SSOI sturcture in this work has the same electron mobility enhancement as the bulk-SiGe control structure (strained-Si/relaxed-SiGe), demonstrating that the superior mobility performance introduced by the strained-Si channel is retained in this

SSOI structure. The mobilities are close to that from our earlier work [1], and have significant enhancement over the universal mobility. The mobility enhancement factor remains roughly constant over the entire electric field range up to 1 MV/cm. The mobility at very low field region drops, as a result of high channel doping $3x10^{17}cm^{-3}$.

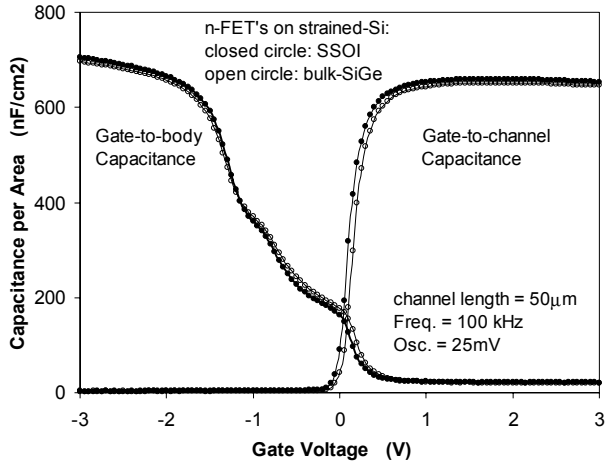


Fig. 5. Split-CV characteritics for the SSOI device on Fig. 4. The gate-to-channel capacitance Cgc is measured between gate and source/drain terminals with body contact (the relaxed SiGe body contact) terminal grounded. The gate-to-body capacitance Cgb is measured between gate and body-contact terminals with source/drain terminals grounded. The Si substrate is floated during the measurements.

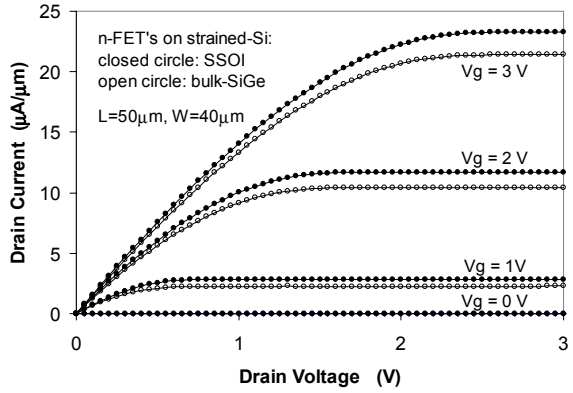


Fig. 6 Drain current output characteristics: drain current versus drain voltage for SSOI (closed circle), and bulk-SiGe control (open circle). Channel length: 50 μm, channel width: 40 μm. The SiGe body contact terminal is grounded during measurement.

Typically drain current output characteristics of the n-MOSFET's on SSOI and on bulk-SiGe control structure are shown in Fig. 6. The subthreshold characteristics are shown in Fig. 7. The subthreshold swing are 84 mV/dec and 86 mV/dec for SSOI and bulk-SiGe control respectively. The corresponding transconductance charateristics divided by channel width (G_m/W) are shown in Fig. 8.

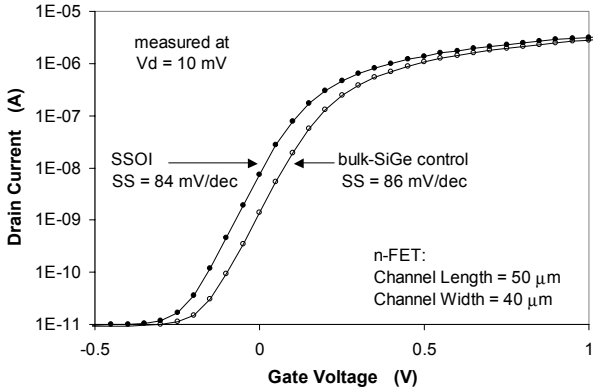


Fig. 7 Subthreshold characteristics: drain current versus gate voltage at low drain voltage for SSOI (open circle), and bulk-SiGe control (closed circle). Channel length: 50 μm, channel width: 40 μm. The SiGe body contact terminal is grounded during measurement.

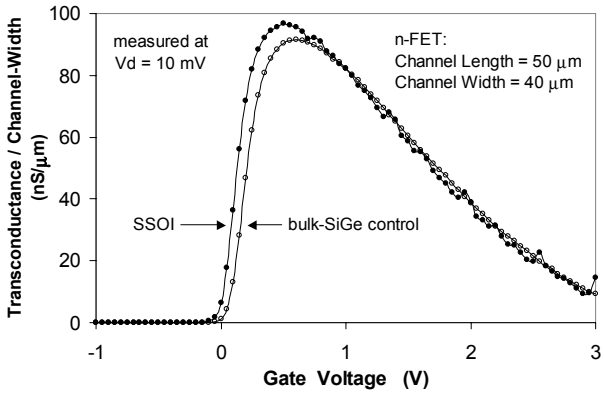


Fig. 8 Transconductance characteristics divided by channel width. SSOI: open circle; bulk-SiGe control: closed circle. Channel length: 50 μm, channel width: 40 μm. The SiGe body contact terminal is grounded during measurement.

V. Dual-channel SGOI Structure and Electrical Properties of p-MOSFET's

A. Dual-channel SGOI structure and p-MOSFET's Fabrication

The SGOI substrates (with 30% Ge) were used for dual-channel SGOI structure growth. A relaxed SiGe layer with the same Ge mole fraction was grown first on

the SGOI substrate, before the growth of a 10nm thick compressively strained $Si_{0.4}Ge_{0.6}$ layer, then a 18nm thick tensile strained Si layer grown, resulting in a dual-channel SGOI structure as shown in Fig. 2(a). The structure was doped to about $10^{17}cm^{-3}$ during the growth.

As the buried-channel p-MOSFET's are the focus of study, we only fabricated p-MOSFET's on this dual-channel SGOI structure in this work. The surface-channnle n-MOSFET's are expected to have similar performance as those on SSOI structure. The coressponding dual-channel bulk-SiGe control structure, i.e. the dual-channel structure on bulk $Si_{0.7}Ge_{0.3}$ substates, were also processed in the same run, whose layer structure is shown in Fig. 2(b). A bulk CZ Si control was also co-processed.

The MOSFET fabrication processes are mostly identical to those for SSOI devcies described above. The gate oxide thickness is about 5 nm. Boron ion implants (BF_2: 15 keV, dose $3x10^{15}$ cm^{-2}) were performed to dope both the source/drain and poly gate regions, and the dopant was activated via furnace at 850C for 30min.

B. Eletrical Properties of p-MOSFET's on Dual-channel SGOI Structure

Fig. 9 shows the subthreshold characteristic of p-MOSFET's on dual-channel SGOI and that on dual-channel bulk-SiGe control structure, together with that on bulk CZ Si control. As a result of buried channel device, the subthreshold swing, 85 mV/dec and 88 mV/dec for dual-channel SGOI and bulk-SiGe control respectively, are larger than the bulk CZ Si control (65 mV/dec). Typical split CV characteristics for dual-channel SGOI is shown in Fig. 10.

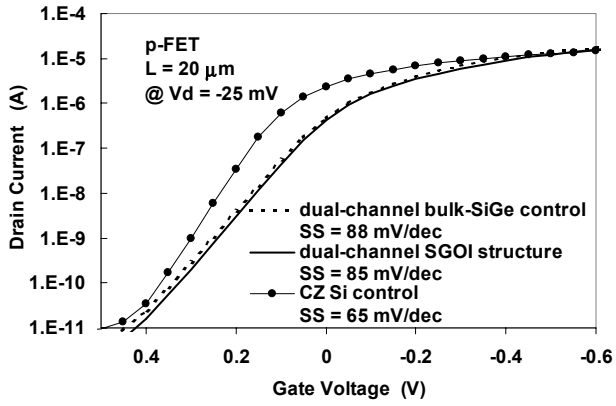


Fig. 9. Subthreshold characteristics of dual-channel SGOI: drain current versus gate voltage at low drain voltage for p-MOSFET's on dual-channel SGOI, dual-channel bulk-SiGe control, and CZ Si control. Channel length: 20 μm. The SiGe body contact terminal is grounded during measurement.

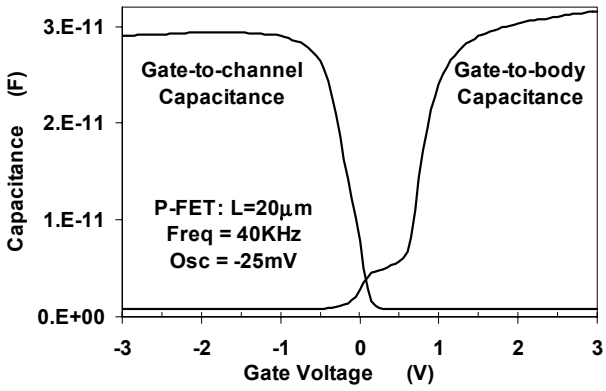


Fig. 10. Split-CV characteristics of dual-channel SGOI: The gate-to-channel capacitance Cgc is measured between gate and source/drain terminals with body contact (the relaxed SiGe body contact) terminal grounded. The gate-to-body capacitance Cgb is measured between gate and body-contact terminals with source/drain terminals grounded. The Si substrate is floated during the measurements.

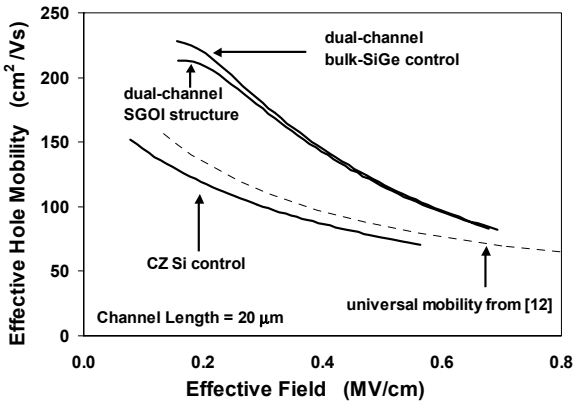


Fig. 11. Measured effective hole mobility vs. effective field from p-MOSFET's on dual-channel SGOI, dual-channel bulk-SiGe control, and CZ Si control. The mobilities are extracted from drain current with the inversion charge extracted from the gate-to-channel capacitance Cgc in Fig. 11. The universal mobility is from [12].

Fig. 11 shows the effective hole mobilities versus effective field from p-MOSFET's on the dual-channel SGOI structure and on the bulk-SiGe control structure. The mobility from bulk CZ Si control, and the universal mobility from [12], are also shown in the figure for comparison. The mobilities are extracted from measurement using the same method as in the last section.

The plots show the performance of p-MOSFET's on dual-channel SGOI structure are very similar to that on

the dual-channel bulk-SiGe control. The hole mobility enhancement over the bulk Si control is about 90% at effective field of 0.2 MV/cm, and about 60% at 0.5 MV/cm. The enhancement reduces with the electric field increases, as also observed in the experiment on bulk SiGe [8]. Although there is enhancement on hole mobility, this enhancement factor is smaller than what is expected based on the experiment on bulk SiGe substrate [8]. This is most probably due to the poor control of MOSFET fabrication process and thermal budget. The anneal step of 850°C for 30min is believed too high and may cause the strained-$Si_{1-y}Ge_y$ layer lost its strain, leading to small enhancement on hole mobility. We believe better process control will produce higher hole mobility.

VI. Summary

In summary, we have compared two SGOI structures for CMOS application: the SSOI is simpler for CMOS process and has the subthreshold advantage associated with surface channel device; the dual-channel SGOI structure has potential to give much higher hole mobility, but the process is more complicate. We have fabricated n-MOSFET's and p-MOSFET's on those two SGOI substrates respectively. Device characteristics are presented. The devices show enhancement on both electron and hole mobilities.

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