Fabrication of Highly Ordered Nanoparticle Arrays Using Thin Porous Alumina Masks

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Abstract **—** Highly ordered nanoparticle arrays have been successfully fabricated by our group recently using ultra-thin porous alumina membranes as masks in the evaporation process. The sizes of the nanoparticles can be adjusted from 5-10 nm to 200 nm while the spacing between adjacent particles can also be adjusted from several nanometers to about twice the size of a nanoparticle. The configuration of the nanoparticles can be adjusted by changing the height of the alumina masks and the evaporation direction. Due to the high pore regularity and good controllability of the particle size and spacing, this method is useful for the ordered growth of nanocrystals. Different kinds of nanoparticle arrays have been prepared on silicon wafer including semiconductors (e.g., germanium) and metals (e.g., nickel). The germanium nanoparticle arrays have potential applications in memory devices while the nickel catalyst nanoparticle arrays can be used for the growth of ordered carbon nanotubes.

Index Terms **—** Porous alumina, Nanoparticle arrays, Nanofabrication, Germanium, Nickel, Carbon nanotubes.

I. Introduction

NANO-structured materials have been widely investigated in the last two decades. There are three kinds of nanomaterials according to their configurations: nanoparticles (zero-dimensional nanomaterials), nanowires (one-dimensional nanomaterials) and nanofilms (two-dimensional nanomaterials) [1]. In the application of nanomaterials, there is a technological need to fabricate nanostructures with high regularity so that good controllability of their properties can be achieved. Different types of nanomaterials normally require different methods to obtain regular structures. The template method is a commonly used approach to achieve ordered one-dimensional nanostructures [2]. Electron beam lithography (EBL) and self-organization growth are also two most widely used methods for fabricating ordered nanoparticle arrays. However, both EBL and self-organization methods have their own drawbacks. The throughput of EBL is low and typically only small areas can be patterned. The capital investment for a high resolution EBL instrument is also very high. As for the self-organization growth method, only a few types of materials can be fabricated into ordered nanoparticle arrays, and most of these are organic materials. This motivates us to investigate methods to fabricate highly ordered nanoparticles over large areas using relatively inexpensive equipment. Preferably, the proposed method should be widely applicable for fabricating nanoparticles using different types of material.

Highly ordered porous alumina membranes, as a widely used template for fabricating nanowires and nanotubes of different materials [2-10], seems to be an attractive approach for fabricating ordered nanoparticle arrays. There are four main advantages in using the alumina membrane mask [2]: nanometer sized pore arrays, high aspect ratio, high regularity of the pore arrays and controllable pore size on a larger scale. All these features are useful in the fabrication of nanoparticle arrays except high aspect ratio. In this work, we have used ultra-thin alumina membranes as masks in the fabrication of germanium (Ge) and nickel (Ni) nanoparticle arrays.

Up to now, our work has mostly focused on three fronts: (a) the fabrication of ultra-thin alumina masks on substrates, mostly on silicon (Si) wafers; (b) the fabrication of Ge nanoparticles and their possible application in memory devices [11]; and (c) the fabrication of Ni, Co, or Fe nanoparticle arrays and their possible application in the fabrication of highly ordered carbon nanotube (CNT) arrays [12].

II. Experiments, Results and Discussion

A. Ultra-thin Alumina Mask on Si Wafer

Ultra-thin alumina masks were fabricated using two methods: The first method is to fabricate an ultra-thin alumina membrane by performing a two-step anodization process on aluminum foils [13]. The alumina membrane is then mounted onto the surface of a Si wafer. The second method involves performing the anodization directly on an aluminum layer thermally evaporated onto the Si wafer. Because the regularity of the second method is typically not very good, we usually use the first method. However, the second method has its own advantages, such as a better adhesion/contact between the alumina mask and substrate which makes it worthy of further investigation.

The detailed fabrication process has been reported previously [12]. Briefly, we use PMMA as a transfer material

so that the ultra-thin alumina mask can be mounted onto the Si wafer surface. After mounting, the PMMA layer is removed in acetone, resulting in an ultra-thin alumina mask on the Si substrate.

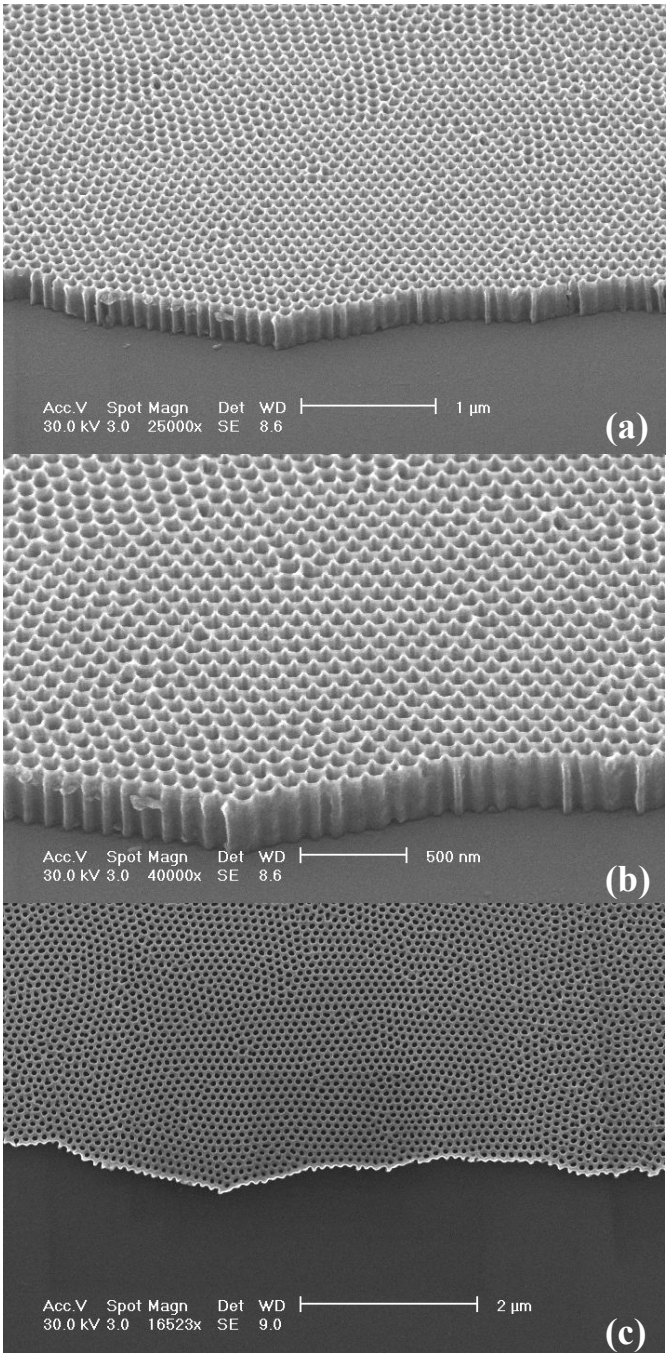


Fig. 1. FESEM images of an ultra-thin alumina mask on Si wafer. (a) and (b) are 3-D views while (c) is the top view. The alumina mask was fabricated in oxalic acid solution under a 40 V bias. The thickness of the mask is about 300 nm while the pore diameter is about 80 nm.

Figure 1 shows an ultra-thin alumina mask on a Si wafer. The cell size is about 100 nm and the diameter of the widened pores is about 80 nm. Figures 1(a) and 1(b) are three-dimensional (3-D) views obtained using a field-emission scanning electron microscope (FESEM) while (c) is the top view. The regularity of the pore arrays is very high. However, the most important feature is that the mask is very thin, about 300 nm in thickness. Thus, the aspect ratio is very small, nearly 1:3. This low aspect ratio will facilitate the evaporated material getting into the pores and reaching the surface of the substrate.

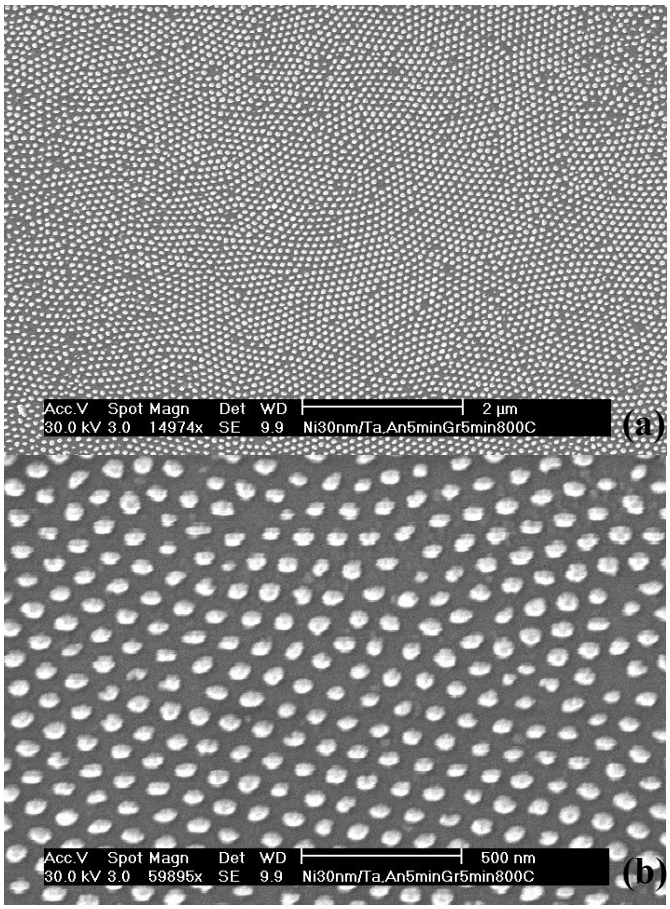
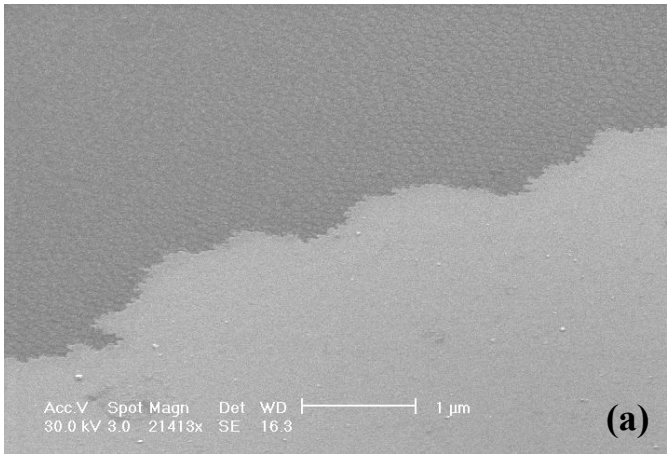
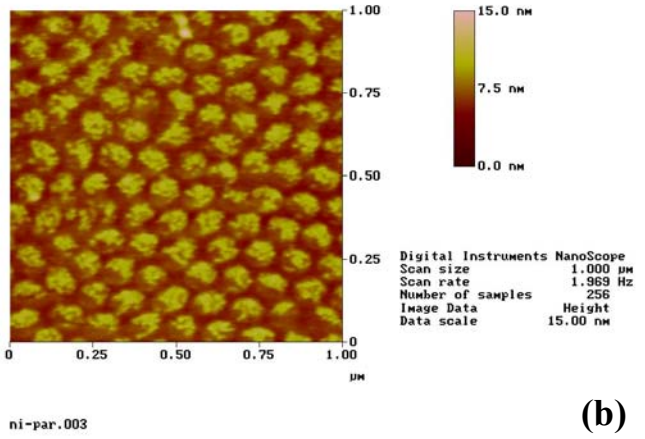


Fig. 2. FESEM images of Ge nanoparticle arrays on Si wafer. (a) and (b) are 3-D views while (c) is the top view. The alumina mask was fabricated in oxalic acid solution under a 40 V bias. The thickness of the mask is about 400 nm while the pore diameter is about 60 nm.

B. Highly Ordered Ge Nanoparticle Arrays

The continual down-scaling of device dimensions requires more stringent and better controlled fabrication processes. One way to conveniently achieve nanometer range structures without sophisticated nanolithography techniques is through the synthesis of nanocrystals. Tiwari *et al.* [14] demonstrated the use of silicon nanocrystals to replace the floating gate of a conventional memory device. The reduced density of states and the Coulomb blockade effect, brought about by the utilization of nanocrystals, enable low-voltage programming at a faster programming speed (write and erase pulse durations of hundreds of nanoseconds) and improved retention times in the nanocrystal memory devices. This has generated great interest in the electronic applications of quantum dots [15-18]. However, to successfully fabricate memory devices using nanocrystals, the growth of nanoparticles with constant size and uniform distribution is of utmost important.





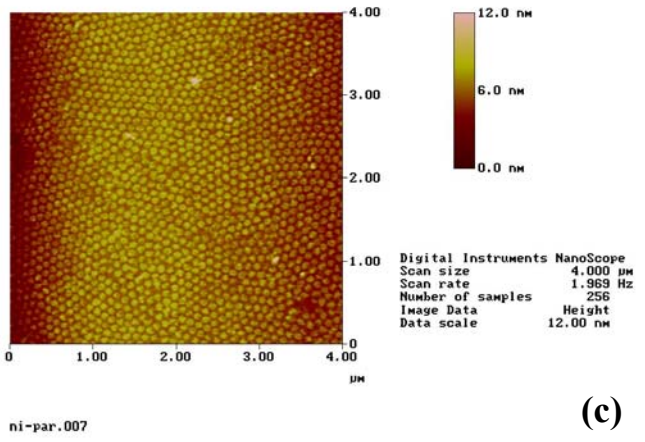


Fig. 3. FESEM image (a) and AFM images [(b) and (c)] of Ni nanoparticle arrays (with thickness of about 10 nm) on Si wafer. (a) is a 3-D view, (b) and (c) are top views. The alumina mask was fabricated in oxalic acid solution under a 40 V bias. The thickness of the mask is about 200 nm while the pore diameter is about 80 nm.

Over the last few years, we have carried out research on the formation of germanium (Ge) nanocrystals embedded in silicon oxide synthesized by sputtering and rapid thermal annealing [11,19]. We are currently investigating the possibility of using such nanocrystal devices for flash memory application. To achieve controllable device characteristics, we are looking at ways to manipulate the arrangement or spatial order of the Ge nanocrystals. We have achieved moderate success in the vertical ordering of the nanocrystals by controlling the thickness of the sputtered Ge layer in a trilayer structure of rapid thermal oxide/Ge mid layer/sputtered capping oxide [11]. Recently, we have successfully achieved lateral spatial ordering of the Ge nanoparticles by using the above ultra-thin mask during Ge sputtering. We hope that this kind of ordered Ge nanoparticle arrays may result in memory devices with controllable electrical characteristics.

Figure 2 shows the FESEM images of the Ge nanoparticle arrays fabricated using the masks in Fig. 1. The particle size and the spacing between adjacent particles are about 50 nm, giving a cell size of about 100 nm. The particle size is smaller than the pore diameter of the ultra-thin mask, indicating that the evaporating direction is not totally perpendicular to the substrate surface.

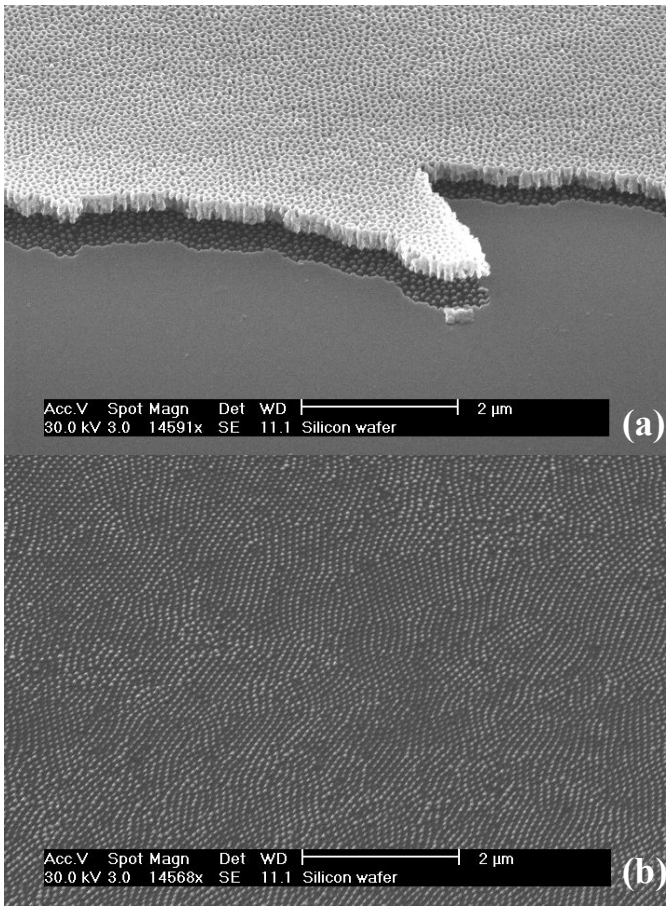


Fig. 4. FESEM images of Ni nanoparticle arrays (with thickness of about 30 nm) on Si wafer. (a) is the sample before removing the alumina mask while (b) is the sample after removal of the mask. The alumina mask was fabricated in oxalic acid solution under a 40 V bias. The thickness of the mask is about 400 nm while the pore diameter is about 60 nm.

C. *Highly Ordered Ni Particle Arrays and CNT arrays*

We have also used the ultra-thin mask for the growth of carbon nanotube (CNT) arrays. The recent interest in CNT alignment not only originates from the idea that the aligned carbon nanotubes can be a desirable material for the fabrication of field emission devices, but also from the fact that aligned tubes are very helpful in studying the properties of the nanotubes [20]. Much research work has been done in this field [21-26]. Normally, there are two approaches in fabricating aligned carbon nanotubes. The first is to fabricate aligned nanotubes by chemical vapour deposition (CVD) on different substrates [21-24]. These substrates include mesoporous silica [21], glass [22], porous silicon on silicon wafers [23,24] and other materials. The other approach is to grow nanotubes in some kind of membrane to obtain highly ordered arrays [25,26]. However, both approaches have their drawbacks: the regularity of the alignment is usually not good for the highly graphitized nanotubes prepared by the first approach [21,22]. For the second method, although the regularity is very good, the graphitization is usually not good probably due to the interaction between the pore walls of the membranes and the tubes [20,23,24]. Based on the above, the better way to fabricate highly ordered CNT arrays is to combine the advantages of the two approaches. An ultra-thin alumina mask and a highly ordered nanoparticle array of a catalyst material will serve such a purpose well.

Recently, by using the following method, we have successfully fabricated CNT arrays with good regularity [12]. First, a highly ordered catalyst array is fabricated on the surface of a silicon substrate by using an ultra-thin alumina mask to obtain good regularity. The mask is subsequently removed and the growth of nanotubes on the catalyst array is carried out to obtain good graphitization. The method may pave the way for fabricating highly ordered CNT arrays with high graphitization and excellent field emission properties.

Different kinds of Ni nanoparticle arrays with different particle heights were prepared to compare the CNT growth (Figs. 3 to 5). Figure 3, 4, and 5 are FESEM images of the Ni particles with thickness of about 10 nm, 30 nm, and 50 nm. The following two points can be noted from the figures:

1) Not only the pore diameters of the mask affect the size of the nanoparticles and the spacing of adjacent particles, but also the height of the masks greatly affects them. The 10 nm thick sample in Fig. 1 is fabricated using a thinner mask than those for the 30 nm and 50 nm thick samples in Figs. 4 and 5. It is seen that the size of the 10 nm thick particles is slightly larger than that of the 30 nm and 50 nm thick particles although their height is lower.

2) The configuration of the nanoparticles can be adjusted by changing the aspect ratio of the ultra-thin masks. When the aspect ratio of the mask is high (larger than 1:6), the nanoparticles are usually pyramidal in shape [Fig. 5 (d)]. In the case that the mask is very thin (with aspect ratio smaller than 1:3), the particles are almost flat disks. Sometimes when

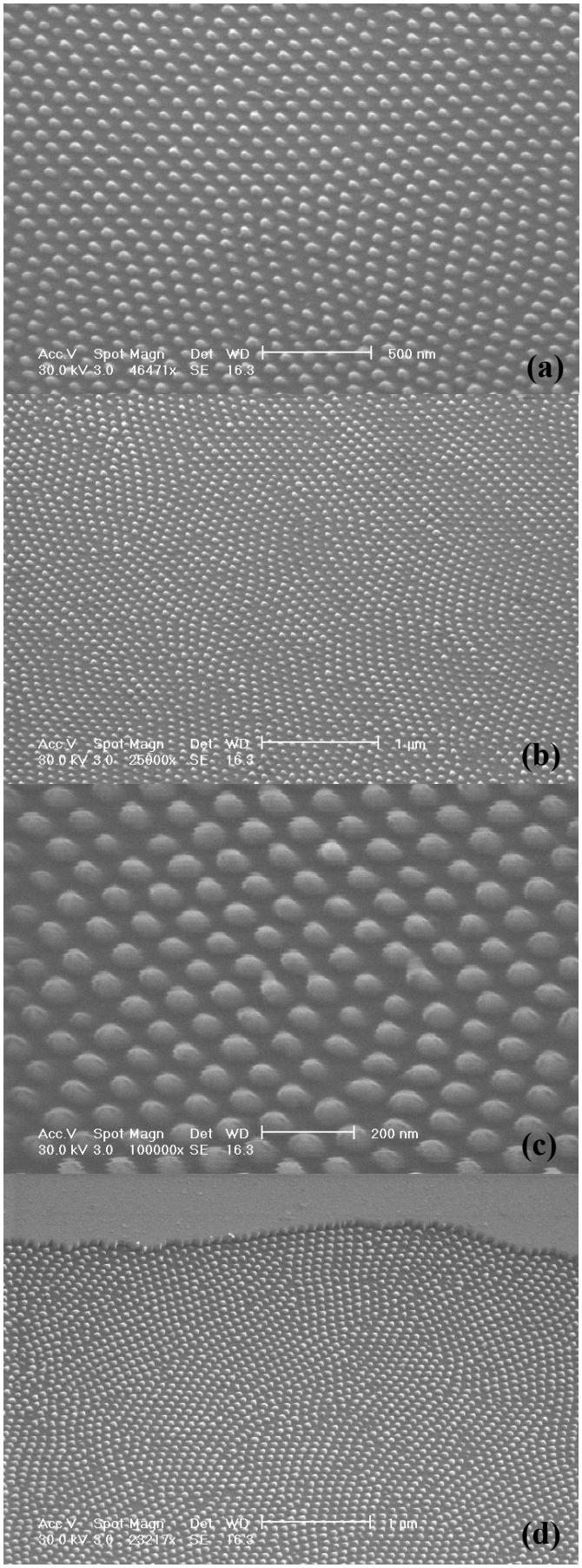


Fig. 5. FESEM images of Ni nanoparticle arrays (with thickness of about 50 nm) on Si wafer. The alumina mask was fabricated in oxalic acid solution under a 40 V bias. The thickness of the mask is about 600 nm while the pore diameter is about 60 nm.

the evaporation direction is tilted, we can obtain tilted nanoparticles on the Si wafer [Figs. 5(a) and 5(b)].

We have also fabricated regular CNT arrays using the above ordered Ni nanoparticle arrays as catalysts for CNT growth [12]. Figure 6 shows the SEM images of the regular CNT arrays on a Si wafer. The CNT arrays have a much better regularity than those fabricated on a bare silicon wafer without alumina mask or on other substrates [2]. From the top views [Figs. 6(b) and 6(c)], the tubes beneath the catalyst particles cannot be seen. This suggests that the nanotubes are perpendicular to the silicon surface and are very straight. Also, the catalyst particles (equal to the diameter of the nanotubes) are rather uniform.

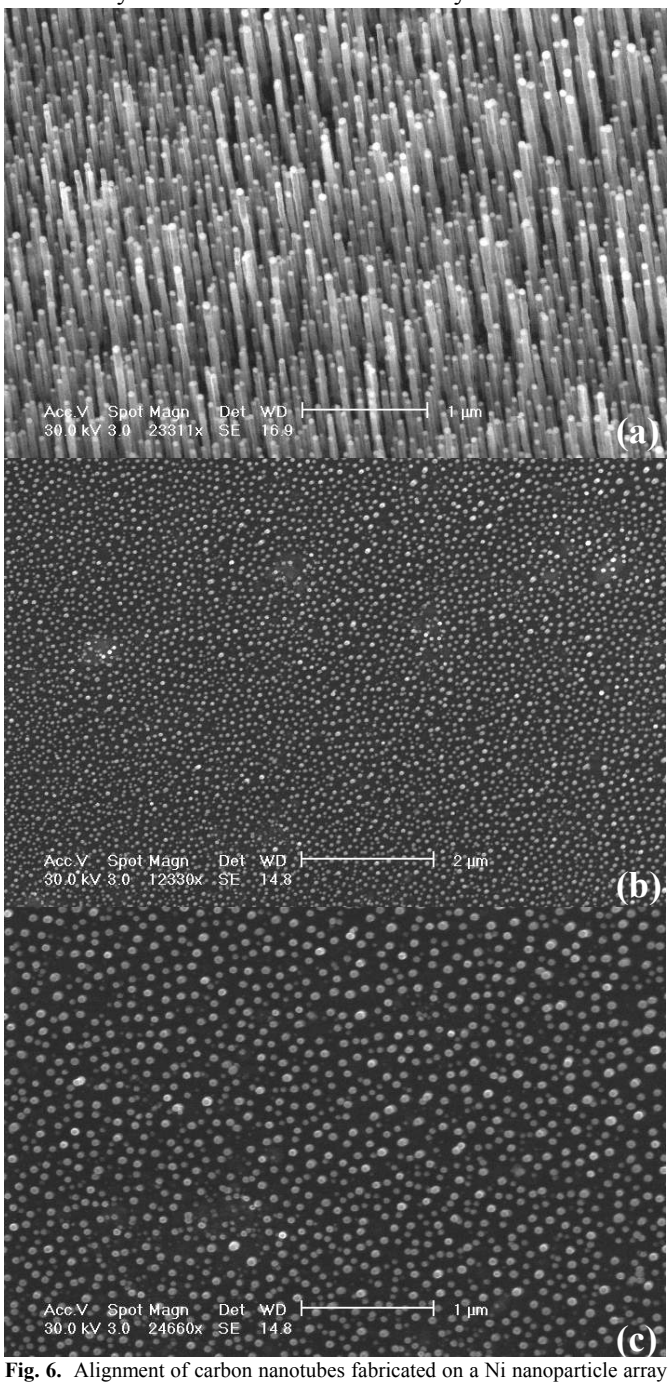


Fig. 6. Alignment of carbon nanotubes fabricated on a Ni nanoparticle array on top of a Si wafer. (a) is a 3-D view while (b) and (c) are the top views. The outside diameters of the nanotubes range from 40 to 60 nm, with 45 nm being the most typical.

D. Other Highly Ordered Nanoparticle Arrays (in progress)

We are in the process of preparing other types of nanoparticle arrays, including ZnO, CdS, In_2O_3, and SnO_2. CdS was evaporated directly into the mask pores to form the nanoparticle arrays. For the other three materials, we first evaporated metal nanoparticle arrays including Zn, In, and Sn. The metal arrays were subsequently oxidized in a tube furnace, resulting in oxidized nanoparticle arrays. The above four materials have been reported to give good photoluminescence (PL) properties [27]. Also, because of their high regularity, it is possible to fabricate optical devices with controllable characteristics by such a method.

III. CONCLUSION

We have successfully fabricated highly ordered nanoparticle arrays of germanium, nickel and other materials. The highly ordered germanium nanoparticle arrays have potential applications in memory devices while the nickel catalyst nanoparticle arrays can be used for the growth of ordered carbon nanotubes.

REFERENCES

[1] H. Gleiter, ***Prog. Mater. Sci.***, **33**, 223 (1989).

[2] J. C. Hulteen, and C. R. Martin, ***Nanoparticles and Nanostructured Films***, Chapter 10, Ed. by J.H. Fendler, Wiley-Vch, 235 (1998) (and references therein).

[3] H. Masuda and K. Fukuda, ***Science***, **268**, 1466 (1995).

[4] T.M. Whitney, J.S. Jiang, P.C. Searson, and C.L. Chien, ***Science***, **261**, 1316 (1993).

[5] Y. Lei, Zhang L. D., Meng G. W., Li G. H., Zhang X. Y., Liang C. H., Chen W. and Wang S. X., ***Appl. Phys. Lett.***, **78**, 1125 (2001).

[6] Y. Lei, L.D. Zhang, and J.C. Fan, ***Chem. Phys. Lett.***, **338**, 231 (2001).

[7] Y. Lei and L.D. Zhang, ***J. Mater. Res.***, **16**, 1138 (2001).

[8] G.L. Che, B.B. Lakshmi, E.R. Fisher, and C.R. Martin, ***Nature***, **393**, 346 (1998).

[9] R. Parthasarathy and C.R. Martin, ***Nature***, **369**, 298 (1994).

[10] M. Nishizawa, V. P. Menon, and C. R. Martin, ***Science***, **268**, 700 (1995).

[11] L.W. Teo., W.K. Choi, W.K. Chim., V. Ho, M.S. Tay, C.M. Moey, C.L. Heng, Y. Lei., D.A. Antoniadis and E.A. Fitzgerald, *Appl. Phys. Lett*. **81,** 3639 (2002).

[12] Y. Lei, J.T.L. Thong, K.S. Yeong, L.W. Teo, W.K. Chim and W.K. Choi., *Proceedings of* ***The International Conference on Carbon in 2002***, Sept 15-20, Beijing, P. R. China.

[13] H. Masuda and M. Satoh*, Jpn. J. Appl. Phys*. **35**, L126 (1996).

[14] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E.F. Crabbé and K. Chan, *Appl. Phys. Lett.* **68**, 1377 (1996).

[15] I. Kim, S. Han, H. Kim, J. Lee, B. Choi, S. Hwang, D. Ahn and H. Shin, *Tech. Dig. Int. Electron Devices Meet*., 111 (1998).

[16] A. Dutta, Y. Hayafune and S. Oda, *Jpn. J. Appl. Phys*. **39**, 855 (2000).

[17] Y.C. King, T.J. King and C. Hu, *Tech. Dig. Int. Electron Devices Meet*., 111 (1998).

[18] S.T. Futatsugi, A. Nakajima and H. Nakao, *Fujitsu J. Sci. & Tech*. **34** 142 (1998).

[19] W.K. Choi, W. K. Chim, C.L. Heng, L.W. Teo, Vincent Ho, V. Ng, D.A. Antoniadis and E.A. Fitzgerald, *Appl. Phys. Lett*. **80**, 2014 (2002).

[20] Harris PJF. Carbon nanotubes & related structures, Cambridge: Cambridge University Press, 1999.
[21] W.Z. Li, S. S. Xie, L. X. Qian, B. H. Chang, B. S. Zou, W. Y. Zhou, R. A. Zhao and G. Wang, *Science* **274,** 1701 (1996).
[22] Z.F. Ren, Z. P. Huang, J. W. Xu, J. H. Wang, P. Bush, M. P. Siegal and P. N. Provencio, *Science* **282,** 1105 (1998).
[23] H. Dai, J. Kong, C. Zhou, N. Franklin, T. Tombler, A. Cassell, S. Fan, M. Chapline, *J. Phys. Chem*. **103,** 11246 (1999).
[24] S. Fan, M. Chapline, N. Frankline, T. Tombler, A. Cassell, H. Dai, *Science* **283**, 512 (1999).
[25] K.B. Jirage, J. C. Hulteen, C. R. Martin, *Science* **278,** 655 (1997).
[26] J. Li, C. Papadopoulos, J. M. Xu, M. Moskovits, *Appl. Phys. Lett*. **75,** 367 (1999).
[27] P. Yu, Z. K. Tang, G. K. L. Wong, Eds M. Scheffler, R. Zimmermann. *23th International Conf. on the Physics of Semiconductor*, World Scientific, 1996, p. 1453.