Optimization of 1700-V 4H-SiC Superjunction Schottky Rectifiers With Implanted P-Pillars for Practical Realization

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***Abstract*— A class of vertical 1700-V 4H-SiC superjunction (SJ) Schottky diodes have been simulated and optimized, producing results that are below the unipolar limit, while also ensuring practical and cost-effective realization. A conventional vertical SJ is obtained in T-CAD software, using an n-type drift region of 9-μm and etching trenches through this region to the substrate to leave isolated mesa structures. P-columns are then created through implantation into the trench sidewalls. The charge-balanced SJ diode maximizes the breakdown voltage (V_{BD}) and minimizes the specific ON-resistance ($R_{ON,SP}$). However, a narrow implantation window would make the vertical structure hard to fabricate. Therefore, by introducing an angled trench sidewall (α), 10° off vertical, a graded charge profile is introduced reducing V_{BD} by 2.5% and increasing $R_{ON,SP}$ by 9%. However, the implantation window is widened by 20% compared with the vertical device, making the successful production of the devices more likely. To rebalance the 10° structure, a 1-μm region of increased n-type doping is introduced at the top of the n-pillar. This partially recovers the lost V_{BD} and $R_{ON,SP}$ while maintaining an implantation window wider than the vertical SJ. The balance between $R_{ON,SP}$ and implantation window can be tuned depending on the doping of the 1-μm top region. The 10° structure can also be rebalanced by introducing a second 4-μm region of intermediate n-type doping, underneath the 1-μm surface region. This recovers $R_{ON,SP}$, while maintaining an implantation window that is 7% wider.**

***Index Terms*— Schottky diode, silicon carbide, superjunction (SJ).**

I. Introduction

SiC continues to draw attention as a wide bandgap (WBG) power semiconductor due to its superior material properties and continuing maturity. Thus, it is widely recognized as a material that has the potential to revolutionize the future power electronics field [1]. With a critical electric field 10 times higher than silicon (Si), high-voltage unipolar Schottky and MOSFET devices offer fast, low-loss switching compared with Si p-i-n diodes and IGBTs in the 600–1700-V class. Therefore, adoption of SiC power devices results in converter operation at higher power, frequency, temperature, and with improved efficiency compared with legacy Si power devices. Despite lower switching losses, ON-state losses in unipolar SiC devices remain equivalent to bipolar Si counterparts, with $R_{ON,SP}$ of SiC proportional to its $V_{BD}^{2.5}$ [2]. Therefore, a small increase in V_{BD} results in a significant rise in $R_{ON,SP}$. As one considers scaling up SiC devices to higher voltages, techniques to go beyond the unipolar limit must be considered to reduce $R_{ON,SP}$ [3].

Superjunction (SJ) theory [4] is one such method and takes advantage of the charge compensation principle, which improves the trade-off between V_{BD} and $R_{ON,SP}$, compared with the traditional power devices. Device concepts that implement this principle utilize 2-D and 3-D nonplanar p-n junctions for field shaping. To achieve a high V_{BD} and to capitalize on the improved trade-off that SJ structures offer, high aspect ratios (the ratio of column depth to column width) between n- and p-pillars should be realized. However, increasing the aspect ratio increases the fabrication challenges. The SJ principle can be applied to WBG materials, such as SiC; however, traditional methods for fabrication including multiepitaxial growth and deep-trench-filling epitaxy along with the control of dopant diffusion are processes that are not yet fully developed [5]. Previously, we proposed an SiC SJ diode that was optimized to overcome some of the difficulties associated with fabrication, utilizing a trench-etch and sidewall implantation [6]. These structures revealed an improved implantation window; however, they required further optimization to improve the trade-off between V_{BD} and $R_{ON,SP}$.

This work builds upon this study by offering an in-depth investigation and optimization of 4H-SiC SJ Schottky diodes at a voltage class of 1700 V, aiming for V_{BD} above 2 kV. The work further emphasizes widening the ion implantation processing window via a graded charge profile to ensure the device is practically realizable. The first practical realization of an SiC SJ was demonstrated by Kosugi *et al.*, who demonstrated V_{BD} of 1545 V with $R_{ON,SP}$ of 1.06 m$\Omega \cdot$ cm^2 via a 5.5-μm charge balanced SiC drift layer. This was produced

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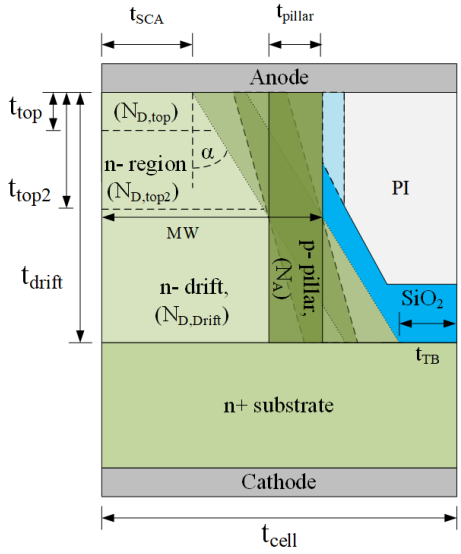

Fig. 1. Half-cell SiC SJ structure with key dimensions and parameters.

via two stages of epitaxial growth and implantation [7]. Zhong *et al.* [8] demonstrated the first SiC SJ fabricated via trench-etching and sidewall implantation, while exploring a semi-SJ configuration—these devices were characterized at 1.35 kV. More recently, Harada *et al.* [9] demonstrated a 1.2-kV SiC SJ trench MOSFET, developed using seven-stage epitaxial growth and implantation stages. Unfortunately, despite this complex (and expensive) fabrication procedure, the SJ structures showed little improvement over equivalent non-SJ trench MOSFETs. Furthermore, Kosugi *et al.* [10] demonstrated a 7.8-kV SiC SJ MOSFET via trench-filling epitaxial growth. This work established void-free, high aspect ratio (9–10) trench-filling with $R_{ON,SP}$ of 17.8 m$\Omega \cdot$ cm^2—overcoming the unipolar limit of SiC.

In this article, the device geometry of the proposed SiC SJ Schottky diodes is investigated to observe the effects on the electrical characteristics. Throughout the study, the traditional SJ trade-off of maximizing V_{BD} while minimizing $R_{ON,SP}$ is kept in balance with a realizable ion implantation window. This method overcomes some of the complex fabrication challenges associated with the conventional SJ structures, and thus ensures practical realization of a future device.

II. Simulated SiC Structures

Fig. 1 shows the simulated SJ Schottky diode configuration, which could be realized using a trench-etch and tilted implantation. Table I summarizes the key dimensions.

4H-SiC is used as the substrate material with a doping concentration of 1×10^{19} cm^{-3}. The substrate is 100 μm in thickness, as if it had been thinned after being processed. A drift region thickness (t_{drift}) of 9 μm is defined to achieve V_{BD} greater than 2 kV, with a doping ($N_{D,Drift}$) of 3.5×10^{16} cm^{-3}. Regions of increased doping, $N_{D,top}$ and $N_{D,top2}$, of thickness t_{top} and t_{top2} are later introduced at the top of the drift region—all of which could be grown epitaxially. The half-cell mesa-width (MW) is measured at the trench midpoint and fixed throughout the study at 2.1 μm. The trench sidewall angle (α) is pivoted about the midpoint to keep the device area, and hence the dose, constant. The trench sidewall angle is incremented from 0°, to 10° and 20°, with a respective p-pillar doping concentration (N_A) of 3.25, 4.0, and 4.5×10^{17} cm^{-3}. A tilted implantation would form the p-pillars along the trench sidewall at an implantation depth of 200 nm. A box-shaped implantation profile is assumed, using aluminum ions. The trenches are formed by ICP-RIE-etching and are passivated before being refilled with encapsulating dielectrics. A first grown layer of SiO_2 is used on the trench sidewall to form a high-quality interface. The trench is filled using polyimide (PI). Metal contacts are formed on the top and bottom of the device. The device pitch is fixed at 4.2 μm to ensure that the devices have comparable current densities.

TABLE I
Key Dimensions and Parameters of Proposed SJ Structure

Symbol	Definition	Value	Units
t_{drift}	Thickness of drift-region	9.0	µm
t_{top}	Thickness of surface region	1.0	
t_{top2}	Thickness of 2nd stage surface region	4.0	
t_{cell}	Cell pitch	4.2	
t_{SCA}	Min. Schottky contact area	0.3	
t_{pillar}	Thickness of p-pillar	0.2	
MW	Mesa-width	2.1	
t_{TB}	Min. Trench Bottom	0.5	
$N_{D,top}$	Surface region doping	3.5×10^{16} – 1.0×10^{17}	cm^{-3}
$N_{D,top2}$	2nd stage surface region doping	4.0×10^{16}	
$N_{D,Drift}$	Drift region doping	3.5×10^{16}	
N_A	P-pillar doping	$3.25 - 4.5\times10^{17}$	
α	Trench sidewall angle	0, 10, 20	°

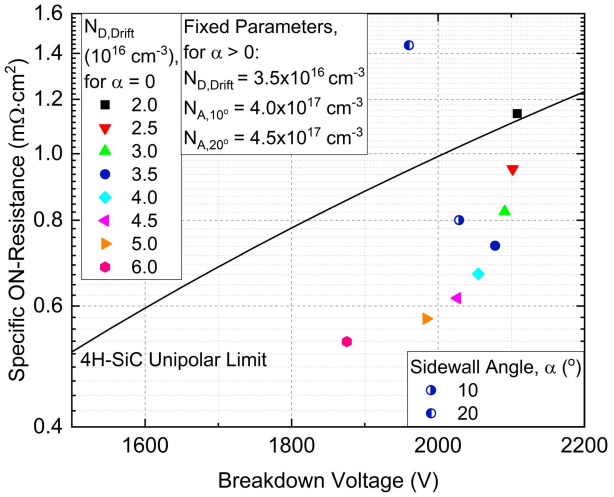

Fig. 2. Effect of $N_{D,Drift}$ on V_{BD} and $R_{ON,SP}$ on vertical (0°) SJ devices, with reference to SJ devices where $\alpha > 0°$.

III. Benchmarking and Simulation Models

The SiC SJ devices described in Section II were simulated using Sentaurus. A benchmarking exercise was performed, validating the simulation and the models therein, by comparing them with prior studies. To this end, both the experimental and

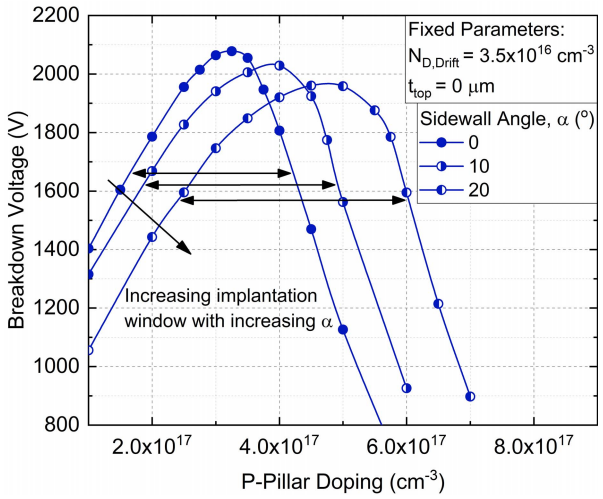

Fig. 3. Effect of α on charge balancing against V_{BD} in SJ structures with varying degrees of α.

simulation results demonstrated by Zhong *et al.* [8], [11] were faithfully reproduced.

The anode is defined as a Schottky contact with a metal work function of 5.2 eV, similar to that of nickel (Ni). Ni is selected due to its relatively high work function. Tunneling and barrier lowering models are used in the simulation of the Schottky contact. The cathode is grounded. Carrier lifetimes decrease with increased impurity concentration.

In the OFF-state, isothermal simulations at 27 °C are used as the reverse current is deemed too low to consider self-heating. The impact of barrier tunneling and avalanche mechanisms on leakage current and V_{BD} is investigated. In the ON-state, the dc characteristics of the devices are analyzed using an anode voltage ranging from 0 to 5 V.

IV. Results and Discussion

A. Determination of Charge Balance in SJ

Simulations were performed to identify the maximum V_{BD} for devices with $\alpha = 0°$, which are to be used as a benchmark for device design iterations. A discrete set of $N_{D,Drift}$ values are used, ranging from 2.0 to 6.0 $\times$ 10^{16} cm^{-3}. The maximum V_{BD} for each $N_{D,Drift}$ value is found by sweeping the p-pillar doping, N_A. Fig. 2 illustrates the maximum V_{BD} plotted against $R_{ON,SP}$ for each $N_{D,Drift}$. These are benchmarked to Kimoto's recently updated 4H-SiC unipolar limit [12]. One can observe a trend in which the maximum achievable V_{BD} and $R_{ON,SP}$ both reduce with increasing $N_{D,Drift}$. The reduction in V_{BD} is the result of nonfull depletion occurring throughout the drift region at higher values of $N_{D,Drift}$. The device with $N_{D,Drift}$ = 3.5 $\times$ 10^{16} cm^{-3} was optimized using $N_A = 3.25 \times 10^{17}$ cm^{-3}. This device maintains a high V_{BD}(~2.1 kV), approaching full depletion, while also achieving $R_{ON,SP}$ under the unipolar limit. This device was selected to be studied hereafter, prioritizing its optimal charge balance in the drift region.

The effects of tilt angle on the p-pillar ion implantation window were investigated next. These results are shown in Fig. 3 in which V_{BD} of each simulation is plotted against its p-pillar doping. These plots are used to determine the implantation processing window (defined herein as the full width of the doping response at 80% of the peak V_{BD}), as illustrated in Fig. 3 with double arrows. Here, the implantation window increases with α, by 20% at 10° and 42% at 20°, when compared with the 0° device. However, it can also be seen from Fig. 3 that as α increases, the maximum V_{BD} decreases.

This V_{BD} versus implantation window trade-off can be understood by analyzing the distribution of charge in the pillars and thus the electric field profile throughout the device. Charge balance is realized when the charge of the n- and p-pillars is perfectly compensated, such that $Q_n = Q_p$. When the charge balance condition is satisfied, the structure is fully depleted and the maximum V_{BD} is achieved due to the flat electric field distribution. This is represented by the vertical SJ throughout this study. The introduction of α produces a varying charge distribution across the n-pillar in the 10° and 20° devices. With α pivoted about the midpoint of the device, the dose of the n-drift region remains constant, regardless of α. Therefore, when $\alpha > 0$, the charge balance condition is only satisfied at the midpoint of the device, and charge imbalance is induced within the structure due to the graded charge profile. In the top half of the n-drift region and at its surface, the drift region is in effect under-doped as there is an excess of charge within the p-pillar ($Q_n < Q_p$). Likewise, in the bottom of the device, the drift region is in effect over-doped as there is an excess of charge within the n-region ($Q_n > Q_p$). Thus, electric field profiles within the 10° and 20° devices are no longer flat across the n-pillar (with the depletion expanding from the narrow anode area first). Thus, the tilted sidewalls produce a deviation from the charge balance condition at all points excluding the midpoint of the drift region. This results in a non-rectangular electric field profile and thus lowers the V_{BD} [13]. The reduction in V_{BD} between the vertical SJs and V_{BD} of the 10° and 20° devices can be calculated using the analytical models for graded doping profiles within SJs developed by Saito [14]. V_{BD} lowering is given by

$$V_{BD} = \frac{q\gamma N_{D,Drift}}{24\varepsilon} \cdot t_{drift}^2 \quad (1)$$

where q is an electron charge, ε is the permittivity, and γ is the gradient coefficient of the p-pillar doping. In this study, the doping of pillars is fixed, and thus the γ coefficient is considered to be the reduction in the n-drift area. The result is similar to the effect observed by Saito, who considers a fixed area but a reduction in doping. Thus, utilizing a γ coefficient of 0.21 and 0.43 for the 10° and 20° devices, respectively, V_{BD} lowering can be calculated at 50 and 100 V. The result of the 10° device aligns with the result shown in Fig. 3. The result of the 20 device is 20 V lower than the result shown in Fig. 3; the discrepancy is due to pinching at the surface of the device.

The increase in implantation window in structures where $\alpha > 0$ results from the imbalanced charge distribution. The increase in the implantation window can be explained using the classical SJ explanation [2], [14]. The decrease in charge concentration in the SJ pillars results in less sensitivity of the breakdown voltage response as a function of the pillars' charge. In our case, the reduction in the pillars' area at the anode side of the device results in an equivalent reduction in pillar charge concentration. As a result, an increase in the implantation window was observed as the sidewall angle increased.

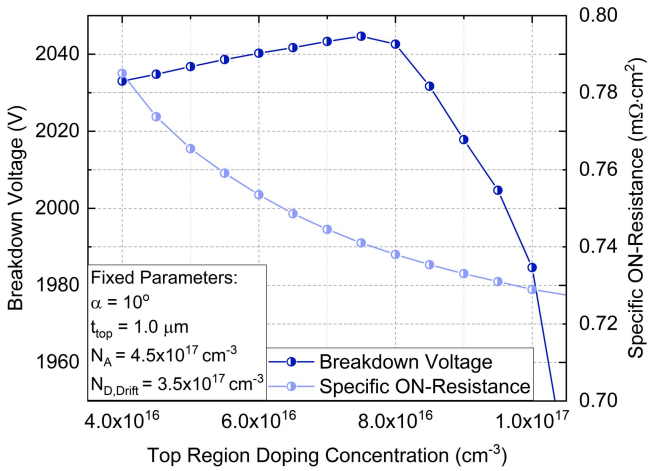

Fig. 4. Influence of the top region doping, $N_{D,top}$ on V_{BD} and R_{ON}.

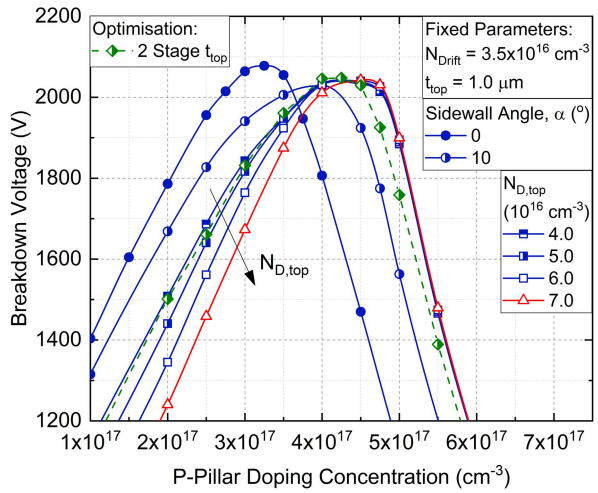

Fig. 5. Effect of top region on the charge balance against V_{BD} in SJ structures.

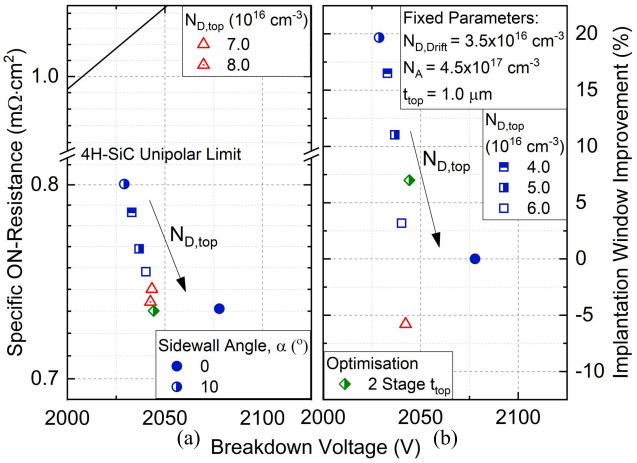

Fig. 6. Effect of a highly doped surface region with a fixed depth, $t_{top} = 1.0\ \mu$m, and varied doping on (a) $R_{ON,SP}$ and (b) implantation window (at 80% of $V_{BD,PEAK}$), shown as the relative improvement in comparison to the 0° SJ structure.

Furthermore, at the top of the drift region in devices with $\alpha > 0°$, the effect of the sidewall geometry results in a JFET effect, the top region becoming pinched, so increasing $R_{ON,SP}$. The increased $R_{ON,SP}$ can be seen in Fig. 2. with $R_{ON,SP}$ of the 10° and 20° devices increasing by 10% and 92%, respectively, when compared with the vertical device.

In summary, increasing α results in a wider implantation window, but the electrical performance of these devices is degraded due to both the charge imbalance brought about by the sidewall geometry and the increased amounts of pinching at the surface—V_{BD} decreasing and $R_{ON,SP}$ increasing. These effects can be observed for the 10° and 20° devices in Fig. 2, where the 20° structure is degraded to within the unipolar limit of SiC. A series of investigations that attempt to rebalance the 10° SJ device are hereafter discussed.

B. Optimizing the $\alpha = 10°$ SJ Structures

To reduce $R_{ON,SP}$ of the structures with sidewall angles of 10°, a second n-type region with a higher n-type doping than $N_{D,Drift}$ is introduced beneath the Schottky contact, at the top of the drift region. As shown in Fig. 1, this region has a depth t_{top} from the surface, with doping $N_{D,top}$. Following optimization, the depth of t_{top} was fixed at 1.0 μm, and the sidewall doping, N_A, was increased to 4.5×10^{17} cm^{-3} to rebalance the SJ structure. A range of $N_{D,top}$ values from 4×10^{16} up to 1×10^{17} cm^{-3} were trialed, and the new V_{BD} and $R_{ON,SP}$ are plotted in Fig. 4. In this Fig. 4, both V_{BD} and $R_{ON,SP}$ are improved by increasing $N_{D,top}$ up to a value of 7.5×10^{16} cm^{-3}. As a result, a V_{BD} of over 2040 V is achieved over a wide range of $N_{D,top}$, which is within 30 V of the original vertical device. This occurs because the additional charge within the t_{top} region rebalances the charge imbalance condition brought about in the top half of the device by the narrow sidewalls, so increasing V_{BD}. This also helps reduce the effects of pinching, reducing $R_{ON,SP}$. Above 7.5×10^{16} cm^{-3}, the maximum achievable breakdown voltage sharply decreases, the result of excess drift region charge that prevents full depletion.

The impact of $N_{D,top}$ on the implantation window can be seen in Fig. 5, in which they are compared with both the vertical SJ and the 10° SJ. To aid comparison, $R_{ON,SP}$ and implantation window for the given structures are plotted in Fig. 6(a) and (b), respectively, both against V_{BD}. The ion implantation window is represented as the percentage change relative to the 0° SJ structure. It can be seen that the values of $N_{D,top}$ greater than 6.0×10^{16} cm^{-3}, presented in red, negate any benefit of introducing the sidewall angle, as the implantation window becomes smaller than that of the vertical SJ.

In summary, the inclusion of a $t_{top} = 1.0\ \mu$m layer in the SiC SJ structures with sidewall angles of 10° results in greater charge balance, and hence improves V_{BD}. The additional doping within the region reduces pinching and lowers $R_{ON,SP}$. However this results in a reduction in the processing tolerance due to the increased charge within the structure. The two therefore remain a trade-off, but now, through the introduction of a top layer, the device can be fine-tuned between the two extremes that the 0° and 10° structures offer. In Sections IV–VI, the structure with $t_{top} = 1.0\ \mu$m and $N_{D,top} = 5.0 \times 10^{16}$ cm^{-3}will be used to represent the optimized 10° device. The resistance of this structure is 3% higher than the original 0° device, but the implantation window is 11% wider.

A similar study was performed on another $\alpha = 10°$ structure, in which a two-stage t_{top} region was introduced in

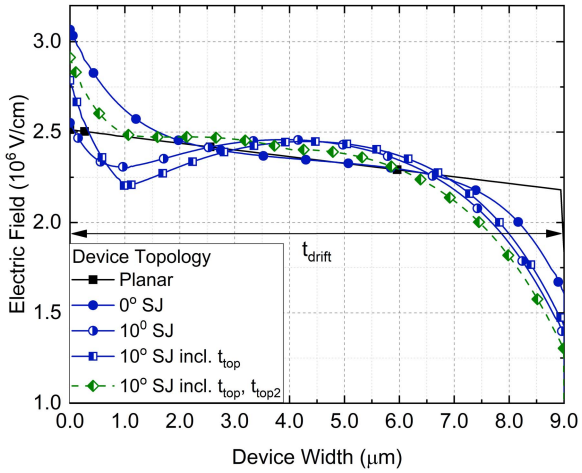

Fig. 7. Electric field distribution, at the onset of V_{BD}, through the center of the n-drift region of SJ structures with varying degrees of α, in reference to a planar SBD optimized to 2.1 kV.

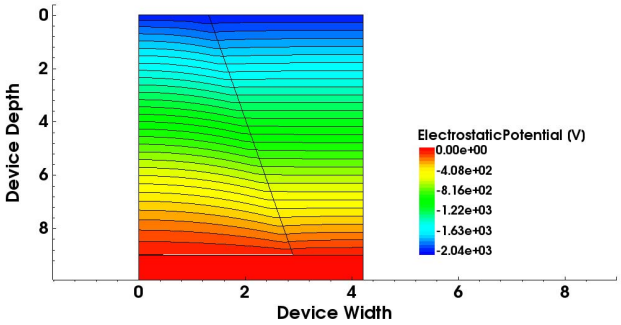

Fig. 8. Potential distribution at the onset of V_{BD} at 2040 V, for an optimized 10° SJ (axes units: μm).

an attempt to rebalance a greater proportion of the device. This structure consisted of a surface region of $t_{top} = 1.0$ μm and $N_{D,top} = 4.5 \times 10^{16}$ cm^{-3}, and an additional region beneath this with $t_{top2} = 4.0$ μm and $N_{D,top2} = 4.0 \times 10^{16}$ cm^{-3}. The introduction of a two-stage top layer led to the same trend as that of the 10° structure, with $R_{ON,SP}$ being recovered at the cost of the implantation window. The two-stage t_{top} structure (colored green in Figs. 5 and 6) displays a processing window 7% wider than the 0° device for an equivalent $R_{ON,SP}$. The fabrication of this structure remains viable, with the two surface regions being formed via epitaxy, in which the doping can be controlled with greater precision than through implantation.

V. Device Physical Analysis

A. Breakdown Mechanics

Analysis of the electric field can give an insight into the effects of charge imbalance on the reverse blocking voltage. In Fig. 7, the electric field cut lines are taken through the center of the mesa ($x = 0$) at the onset of breakdown for the SJ devices, with α ranging from 0° to 10° and a planar device of the same t_{drift}, optimized to ~2.1 kV. It should be noted that while the planar device achieves the same V_{BD} as the SJ devices, its $R_{ON,SP}$ is 5× higher. A defining feature of an SJ device is its characteristic rectangular electric field when the structure is charge-balanced. This can be seen on the vertical SJ in Fig. 7. Deviations away from this rectangular field indicate a charge imbalance within the structure, which can occur due to a charge difference between the drift region and the p-pillar, asymmetrical pillar geometry, pillar doping variation, or a combination of the three [15]. Before rebalancing the 10° structure, the graded charge profile results in the maximum electric field occurring near the device midpoint. A single t_{top} region at the surface of the device only partially recovers the charge imbalance in the top half of the structure. This introduces a region with an equivalent dose to that which is lost as a result of the asymmetrical pillar geometry. The two-stage t_{top} region takes this further, returning the electric field distribution to a rectangular profile close to that of the 0° SJ. However, the electric field intensity tapers away from the vertical SJ profile in the lower half of the drift region, due to the remaining charge imbalance ($Q_n < Q_p$) in the widest part of the pillar. Fig. 8 demonstrates the potential distribution contour plot of the 10° SJ, with $t_{top} = 1.0$ μm and $N_{D,top} = 5.0 \times 10^{16}$ cm^{-3}, at the onset on V_{BD} at 2035 V. Fig. 8 further confirms the near-rectangular electric field of the device, with the uniformly distributed potential throughout the drift layer. The rectangular field occurs at a relatively low reverse bias, the depletion region forming first vertically, from the metal–semiconductor interface, and then laterally from the p-n-junction. In an optimal SJ structure, the rectangular electric field would then increase uniformly until the critical electric field, E_{Crit}, is reached simultaneously at both the top of the n-pillar and at the bottom of the p-pillar, at which point impact ionization occurs [16]. Here, however, it was found that E_{Crit} is reached at the bottom of the p-pillar. As mentioned before, despite the net doping of the device being balanced and the top and mid-points of the drift region being in a charge balance condition, there remains local charge imbalance ($Q_n > Q_p$) in the bottom half of the drift region. This wide region does not completely deplete and results in premature breakdown. Analysis of the charge carriers at the onset of breakdown gives an insight into the breakdown mechanics. There was found to be a surplus of electrons toward the center and bottom of the drift region; likewise, there was found to be an excess of holes toward the top of the p-pillar—although the quantity of these carriers was greatly reduced by the inclusion of the top region. At the onset of V_{BD}, these surplus carriers gain enough energy to short diagonally from the bottom of the drift region to the top of the p-pillar.

The reverse leakage current density can be seen in Fig. 9. It is evident that all devices, both SJ and planar, achieve V_{BD} greater than 2 kV with acceptable levels of leakage current. A correlation exists between the leakage current level through these devices and the surface electric field, as shown in Fig. 7. This suggests that the increasing electric field promotes tunneling through the Schottky interface, as seen elsewhere [17]. It can be seen that devices where $\alpha > 0°$ achieve lower levels of leakage than the vertical structure, due to the reduced surface electric field and their smaller contact area. The planar device has a low leakage current given its lower electric field at the interface and the very low drift region doping compared with the SJ devices.

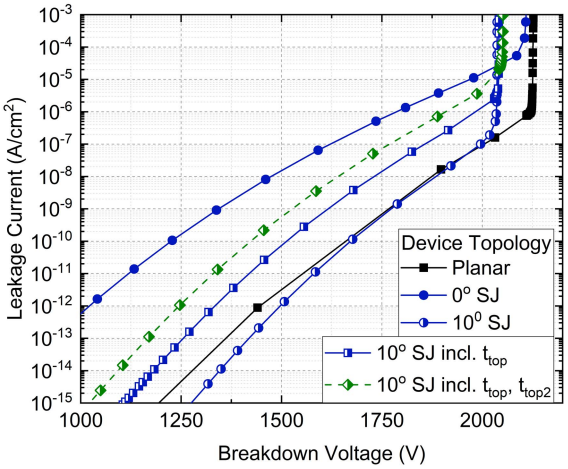

Fig. 9. Reverse leakage characteristics of SiC SJ SBD, with reference to a planar SJ optimized to 2.1 kV.

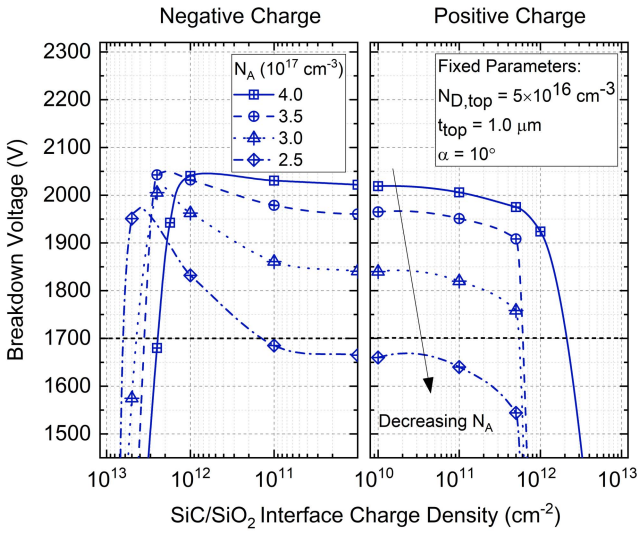

Fig. 10. Influence of SiC/SiO_2 interface charge density on V_{BD}.

B. Interfacial Charge

Similar to an SiC MOS interface [18], [19], trapped charge will form at the SiO_2/SiC interface regardless of the oxide formation method [20]. With a SiO_2/SiC interface running the full length of the drift region on both sides, the impact of interface states on this carefully charge-balanced region must be investigated, and an acceptable trap density is identified. The results of simulation, which modeled fixed charge at the interface, can be seen in Fig. 10, in which the interface charge density was varied for the 10° SJ, with $t_{top} = 1.0\ \mu$m, $N_{D,top} = 5.0 \times 10^{16}$ cm^{-3}, and $N_A = 4.0 \times 10^{17}$ cm^{-3}. The results show that to maintain V_{BD} over 1700 V, the interface density must remain in the range from -2.5×10^{12} to $+2 \times 10^{12}$.

Negative charge is often observed at the SiO_2/SiC interface [21]. Fig. 10 demonstrates that this negative charge window can be increased by reducing the p-pillar doping to $N_A = 3.0 \times 10^{17}$ cm^{-3}. This results in a charge window from -4.5×10^{12} to $+5 \times 10^{11}$. Simulations show that additional negative charge at the interface results in a charge imbalance ($Q_n < Q_p$) at the surface and at the device midpoint. However, up to a critical point, the increasing negative charge assists the bottom half of the device, balancing out this wide base region which did not fully deplete. Hence, the additional negative charge shifts the peak electric field toward the bottom of the device, and the interface charge window to -4.5×10^{12} increasing V_{BD}. Conversely, positive charge exacerbates the pre-existing charge imbalance at the wide base of this region. Maintaining interface charge below 4.5×10^{12} is in line with the state-of-the-art nitridation processes [18]–[20].

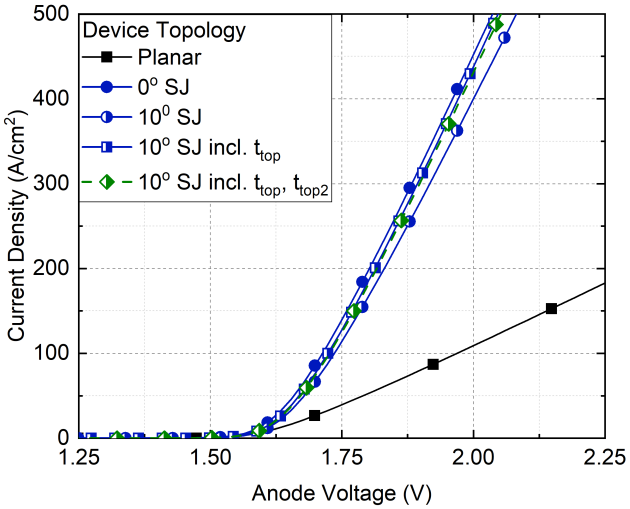

Fig. 11. Forward characteristics of the SJ and planar devices.

C. ON-State Performance

In the ON-state, current passes only through the central n-drift region, and the p-pillar does not contribute to the conduction of the device. As per SJ theory [4], $R_{ON,SP}$ is minimized by maximizing the doping of the n-pillar. Ideally, ever thinner n- and p-pillar widths could be used to further increase the doping, yet fabrication limitations in processing small features impose geometric limits. Another way to reduce total resistance is to minimize the minimum trench bottom width (t_{TB}) increasing the active proportion of the device. However, a geometrical limit also applies to this due to the need to use an angled sidewall implant right down to the bottom of the mesa. Therefore, the proposed geometries in Table I are considered the minimum values that can be practically realized. Within these limits, increased sidewall angles significantly impact $R_{ON,SP}$ by causing a parasitic JFET—occurring from converging depletion regions between the p-pillars and narrowing the n-pillar width.

The effects of device geometry and topology are therefore considered in the ON-state simulations. In Fig. 11, the forward characteristics of the vertical and $\alpha = 10°$ SJ structures can be compared with each other and with a planar device with an equivalent t_{drift}. The total resistance of each device is the sum of their substrate and drift region resistance. It is clear that all the SJ structures have a very comparable ON-state resistance. This is due to the top region mitigating the effects of pinching and reducing the parasitic JFET within the SJ devices with $\alpha > 0°$. It should be noted that the planar device has approximately 1 order of magnitude less doping, which has a significant impact on these characteristics. The turn-on voltage of all the devices is almost 1.6 V, consistent with the work function of Ni, used as a Schottky contact. It can be seen from Fig. 11 that an equivalent ON-state resistance

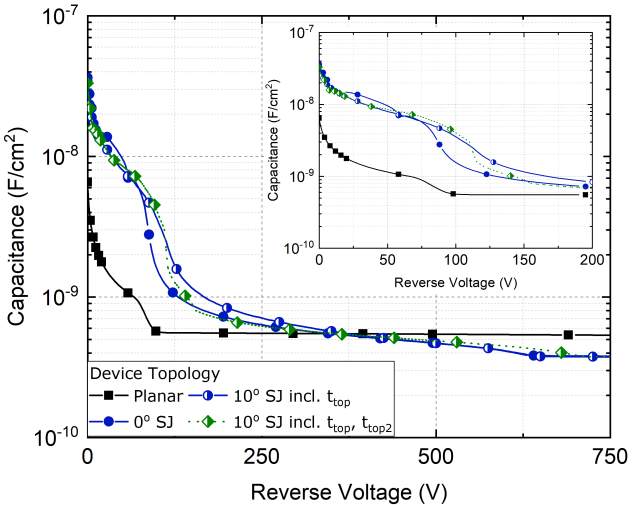

Fig. 12. *C–V* characteristics of SiC SJs with varying device topologies.

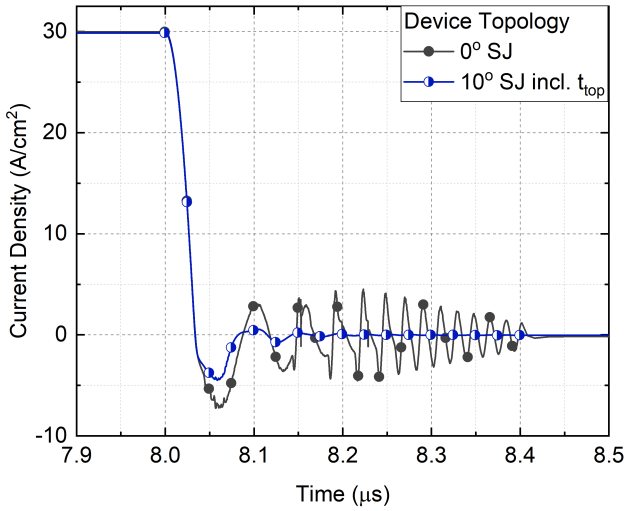

Fig. 13. Reverse recovery characteristics for both the vertical SJ and the proposed SJ.

and an improved processing window can be achieved without degradation of the forward characteristics.

D. Capacitance–Voltage Characteristics

The C–V analysis of the SiC SJ structures was performed and compared with the planar Schottky diode with comparable V_{BD}. The results can be seen in Fig. 12. All the SJ structures exhibit the characteristic nonlinear capacitance, similar to the output capacitance of Si SJ MOSFETs [3]. This results from the lateral expansion of the drift region from the p-pillars, which means that at low voltages up until the device is fully depleted, the depletion region area is very large, inflating the capacitance. Furthermore, the vertical, $\alpha = 0°$ devices display a very steep dC/dV at around 80 V. This can result in "snappy" switching characteristics, the results of the output capacitance sharply decreasing during turn-off, with an equally abrupt reduction in current. This can result in both reliability and efficiency problems without careful consideration at the circuit level [16]. However, as can be seen in Fig. 12, the proposed SJ structures with an $\alpha = 10°$ reduce dC/dV when compared with the vertical structure. This is because of the graded charge profile that occurs throughout the drift region when $\alpha > 0°$, which causes the SJ pillars to deplete more gradually, as shown in the inset of Fig. 12.

E. Switching Characteristics

A simulation of the reverse recovery characteristics was performed for the proposed SJ structure and compared with a vertical SJ, and the results can be seen in Fig. 13. In the simulation, dI/dt was 1000 A/cm^2 · μs, which is comparable with the experimental results shown by Kimoto *et al.* [22]. It can be seen that the proposed SJ with an $\alpha = 10°$ and $t_{top} = 5.0 \times 10^{16}$ cm^{-3} has a reduced maximum reverse recovery current density (I_{RR}) and significantly reduced oscillations compared with the vertical SJ. The calculated I_{RR} for the vertical SJ and the proposed SJ are 7.5 and 4.5 A/cm^2, respectively, as shown in Fig. 13. In this graph, the vertical SJ displays a "snappy" reverse recovery response. Whereas the proposed SJ structure displays a softer reverse recovery. The softer reverse recovery response is a result of the graded charge profile within the drift region. Similarly, as discussed in the previous paragraph, the drift region is gradually depleted and in turn the junction capacitance decreases gradually, and the reverse recovery characteristics become softer. This phenomenon is similar to the softer reverse recovery characteristic demonstrated by semi-SJ structures [23].

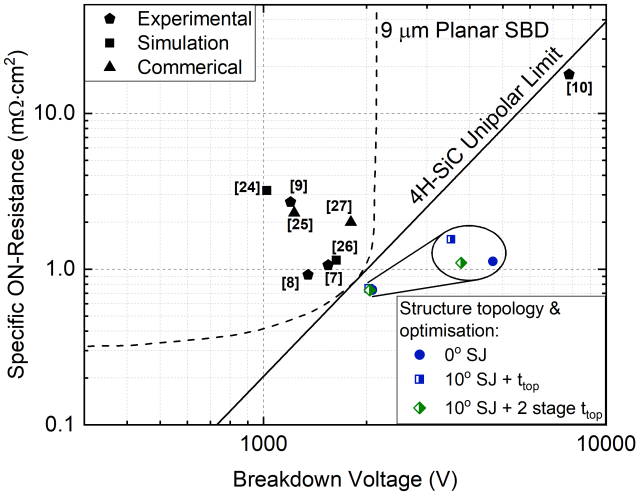

Fig. 14. SJ devices with comparable $R_{ON,SP}$ [7]–[10], [24]–[27] plotted against the 1-D limit of 4H-SiC and an ideal 9-μm planar device. The graph includes the optimized device from this study.

TABLE II
SUMMARY OF KEY DEVICE CHARACTERISTICS

Device	V_{BD} (V)	$R_{ON,SP}$ (mΩ·cm^2)	Relative Implantation Window (cm^{-3}) *
0°	2080	0.73	-
10°	2030	0.80	+20 %
10° incl. t_{top}	2035	0.75	+11 %
10° incl. t_{top}, t_{top2}	2045	0.73	+7 %

* Percentage improvement relative to the 0° structure

F. Benchmarking to Fabricated Devices

The optimized SiC SJ devices with varying sidewall angles have been compared with SJ devices with comparable $R_{ON,SP}$

from other experimental and commercial demonstrations as well as other computational studies, as shown in Fig. 14. These devices are plotted against the recently updated unipolar limit [12], which takes into account punchthrough device geometries and the latest studies of the intrinsic physical properties of the material. Also plotted are the best achievable simulations using a 1-D planar Schottky diode with a 9-μm drift region. The dashed line denotes a sweep of the drift region doping. Fig. 14 demonstrates that the optimized SJ devices in this study offer an improved relationship between V_{BD} and $R_{ON,SP}$, overcoming the unipolar limit while also improving the p-pillar implantation window. The key simulation outputs can be seen in Table II.

VI. Conclusion

In this article, SJ structures with a drift region thickness of 9 μm and varying sidewall angles have been compared as a guide for SiC SJ diode fabrication. It was found that introducing a sidewall angle greater than 0 resulted in a wider implantation window, making successful fabrication more likely. However, the charge imbalance brought about by the asymmetrical n- and p-pillars reduced V_{BD} and increased $R_{ON,SP}$. For a device with a trench sidewall angle of 10°, the introduction of a 1.0-μm surface region with increased doping of 5.0×10^{16} cm^{-3} partially recovered the lost V_{BD} and reduced $R_{ON,SP}$ to values comparable with that of a vertical SJ. Furthermore, a stable V_{BD} of >2030 V could be achieved over a wide range of $N_{D,top}$ between 3.5 and 6.0×10^{16} cm^{-3}. However, the trade-off remained between $R_{ON,SP}$ and implantation window, with both parameters decreasing as $N_{D,top}$ was increased.

In conclusion, $\alpha = 10°$ including a t_{top} region structure offers the designer control over the trade-off between $R_{ON,SP}$ and the implantation window. The device can be tailored with up to a 20% improvement in implantation window while minimizing the effect on V_{BD} and $R_{ON,SP}$ when compared with the vertical SJ.

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