March 1996 LIDS-P-2321

Full Utilization, Fairness and Bounded Access Delay on High Speed Bus Networks *

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March, 1996

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Abstract

Many existing protocols indicate that full utilization and fairness might be incompatible in high-speed-high-latency MANs or LANs. The purpose of this paper is to study the fundamental limitations of dual bus networks, in terms of full utilization, fairness and bounded access delay. A new protocol called FUFA (fully utilized and fair) is used to demonstrate some of these basic properties. We define full utilization, and fairness precisely, and show that both are achieved together in the FUFA protocol. In addition, the protocol provides bounded access delay that is linear in the round trip propagation delay, and at most a constant away from its minimum possible value for any bus protocol that is both fully utilized and fair. The main idea is to compute, for each station, the latest estimate on the number of active downstream stations, according to the information available, and serve them in a round robin scheme.

Key words: dual bus network, propagation delay, full utilization, fairness, bounded access delay

*This research is supported by ARPA under grant MDA972-92-J-1038.

1 Introduction

During the last fifteen years, we have witnessed a proliferation of proposals for high-speed-high-latency bus networks. In many of these previous networks [4-7, 13, 16-19], full utilization and fairness are incompatible. The well known distributed queue dual bus (DQDB) protocol with bandwidth balancing (the IEEE 802.6 standard for metropolitan area networks) achieves a fair distribution of the bandwidth by requiring each station to use only a fraction of the available bandwidth for transmissions [6]. Thus, the protocol does not provide full utilization of the bandwidth. Moreover, the protocol converges slowly to a fair distribution of the bandwidth to the active stations. Many efforts have been made in the past to improve the fairness and bandwidth utilization in dual bus network protocols, [1-3, 8-12, 14, 15], and simulation results and analysis show that improvements are possible.

The objective of this research is to study the fundamental limitations of dual bus networks, in terms of full utilization, fairness and bounded access delay. A new protocol called FUFA (fully utilized and fair) is used to demonstrate that full utilization and fairness are in fact compatible. Full utilization means that a station with traffic to send never releases an idle slot that is not used by some further downstream station. Fairness is defined precisely later. We show that full utilization and fairness are achieved in the proposed protocol. Additionally, the protocol provides a bounded access delay that is linear in the round trip propagation delay, and only a constant away from its minimum value for any bus protocol that is both fully utilized and fair. The main feature of this protocol is that each station takes account of the idle slots propagated previously to interpret the information from downstream (i.e., estimated total number of packets in queue downstream and estimated number of active downstream stations), and serve the active downstream stations in a round robin scheme according to the updated information. The protocol is designed primarily to demonstrate these properties rather than as a practical strategy.

The remainder of this paper is organized as follows. In section II we describe the basic dual bus topology. In section III we state some simple facts on full utilization, fairness, and bounded access delay, starting with the definitions. Then a lower bound on the maximum access delay is provided for any protocol that is both fully utilized and fair. In section IV, we describe the FUFA protocol. We start with the basic concept, and then give a full description of the FUFA protocol, followed by some basic properties of the protocol. In Section V we prove the full utilization, fairness and bounded access delay properties of FUFA. Finally we conclude our results in Section VI.

2 Basic Dual Bus Network

The dual bus topology we consider here is identical to that used in DQDB (see Figure 1). The two buses support unidirectional communications in opposite directions. Stations are connected to both buses and communicate by selecting the proper bus. A special unit at the head-end of each bus generates one slot at each unit of time. The stations are numbered from left to right as stations 1, 2, ..., K. Because of the

symmetry of the dual bus topology, we can consider only transmission on one bus. The bus from station 1 to station K is used to transfer data and is referred as the data bus or downstream bus. The bus from station K to station 1 is used to make reservations and is referred as the reservation bus or upstream bus. Therefore station 1 is the most upstream station, and station K is the most downstream station. For each station $i \in [1,\ K]$, denote D_u^i as the propagation delay measured in slots between station i and its upstream station $i-1$ and D_d^i as the propagation delay between station i and its downstream station $i+1$, where D_u^i and D_d^i are integers [1]. Each station has a local FIFO (first-in-first-out) queue to store data segments by local users while these segments wait for assignment to appropriate idle slots on the data bus. Notice that the protocol also works in principle on a folded bus, where one fold of the bus can be viewed as the date bus and the other fold as the reservation bus.

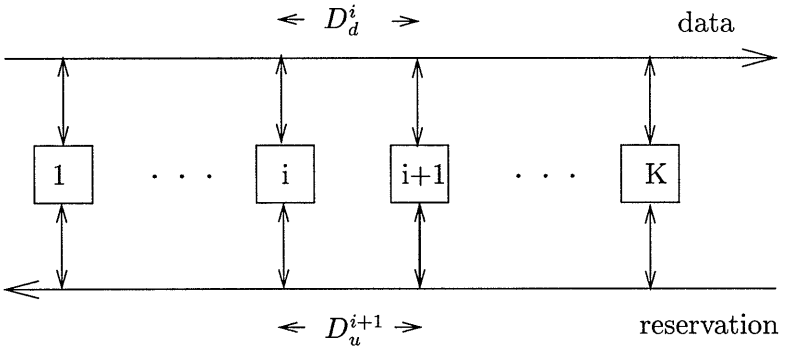

Figure 1: Dual Bus Topology

3 Simple Facts about Full Utilization, Fairness, and Bounded Access Delay

3.1 Definitions of Full Utilization, Fairness, and Bounded Access Delay

Definition 1: A protocol has *full utilization* if whenever a station with a non-empty queue propagates an idle slot, that idle slot is used by some further downstream station.

That is, full utilization means that an idle slot is never wasted. It must be used if it could be used by one of the stations with non-empty queues.

Definition 2: Let $S_n = \{i_1 < i_2 < ... < i_n\}$ be the set of some n stations that have been "very active" since t_0, where being "very active" is defined in Section 5.2. A protocol is *fair* if each station $i_k \in S_n$, $k = 1,\ ...,\ n$, starting from $t_0 + \sum_{h=i_1}^{i_k-1} D_d^h$, transmits one data segment in every n time slots for as long as S_n remains the set of "very active" stations and all the other stations remain idle (i.e., with empty queues).

Definition 3: An algorithm has the bounded access delay property if for each station i, $i \in [1,\ K]$, there exists a finite constant B_i such that the access delay of the first data segment in queue is bounded by B_i.

[1] the integer assumption is for notation simplicity, but each can be non-integer as shown in Appendix A

Let P_i be some data segment at station i, $i \in [1,\ K]$, denote t_a^i as the time that P_i becomes the first segment in the queue, and t_d^i as the time that P_i departs from the queue. Then an algorithm has the bounded access delay property if and only if $t_d^i - t_a^i \leq B_i$ for each i and each P_i with some constant B_i.

3.2 Greedy Algorithm: Fully Utilized But Not Fair

Greedy algorithm is fully utilized since it allows stations to use idle slots whenever there are data segments waiting in queues. However, it is not fair since it prioritizes stations from the most upstream to the most downstream.

3.3 An Algorithm with Full Utilization and Fairness

An algorithm that is both fully utilized and fair must be non-greedy. A non-greedy algorithm means that some non-empty station is allowed to propagate idle slots. In order to have the full utilization property, feedback information is necessary. This can be shown with a simple contradiction argument. The feedback information carried by the reservation bus can be the queue length status of downstream stations, the arrival information, etc..

From the definition of fairness, we can see that with a set of "very active" stations and all others being idle, each station must know exactly the number of active stations downstream and apply a round robin scheme.

3.4 Bounded Access Delay of An Algorithm with Full Utilization and Fairness

Here, we study the bounded access delay of a non-greedy algorithm that is both fully utilized and fair. Denote B_i as an upper bound of the access delay for the first data segment at station i, and B_i^{min} as the minimum value of all the upper bounds of the access delay, thus the maximum access delay. Due to the full utilization property, idle slots are propagated by a non-empty station based on only the information that has been received. Therefore, the access delay of the first data segment at station i can be as large as the round trip propagation delay between station i and the most upstream station, station 1, i.e.,

$$B_i^{min} \geq \sum_{k=1}^{i-1} (D_u^{k+1} + D_d^k) \tag{1}$$

This is shown through a contradiction argument in section 5.3.

Besides the round trip propagation delay, the round robin cycle under the condition in the definition of "fairness" can result in extra delay for a station to get access to the idle slot. This extra delay varies between 0 and $K - 1$, depending on the position of the station in the cycle. Re-number the stations according to

their positions in the round robin cycle as $i' = 1, \ ..., \ K$. Then,

$$B_{i'}^{min} \geq \sum_{k=1}^{i'-1} (D_u^{k+1} + D_d^k) + i' - 1 \tag{2}$$

A protocol called FUFA (fully utilized and fair) is used to demonstrate that both full utilization and fairness can be achieved. It is shown in section 5.3 that FUFA protocol provides maximum access delay that meets the lower bound in (2) for at least one of the stations, and at most a constant $K - 1$ away from it for each of the other stations.

4 Fully Utilized and Fair (FUFA) Protocol

4.1 Basic Concept

Since all the idle slots on the data bus are generated from the head-end, station 1, which is the most upstream station, has first access to idle slots. The basic concept of the protocol is to give equal access to all the stations, according to the most updated information available through the reservation bus. In particular, according to the information available, each station computes the latest estimate of the number of active downstream stations, and uses a counter to serves them in a round robin scheme. The novel feature of this protocol is that each station takes account of the idle slots propagated previously to interpret the information from downstream (i.e., estimated total number of packets in queue downstream and estimated number of active downstream stations).

4.2 Parameters

Next, we define the parameters used in the protocol. At time t, the information available at station $i \in [1, \ K]$ is,

- $n_i(t)$: number of idle slots propagated by station i during the past $D_u^{i+1} + D_d^i$ time slots, also written as $n_i(t - D_u^{i+1} - D_d^i, \ t)$. Note that $D_u^{i+1} + D_d^i$ needs to be an integer. See Figure 2.
- $Q_i(t)$: number of data segments in the FIFO queue of station i,
- $I_i(t)$: indicator function whether station i is busy or not, i.e.,

$$I_i(t) \triangleq 1 \text{ if } Q_i(t) > 0, \ 0 \text{ otherwise.} \tag{3}$$

The information sent by station i to the upstream station $i - 1$ is,

- $M_i(t)$: estimated current number of active stations downstream from station i (including i itself),

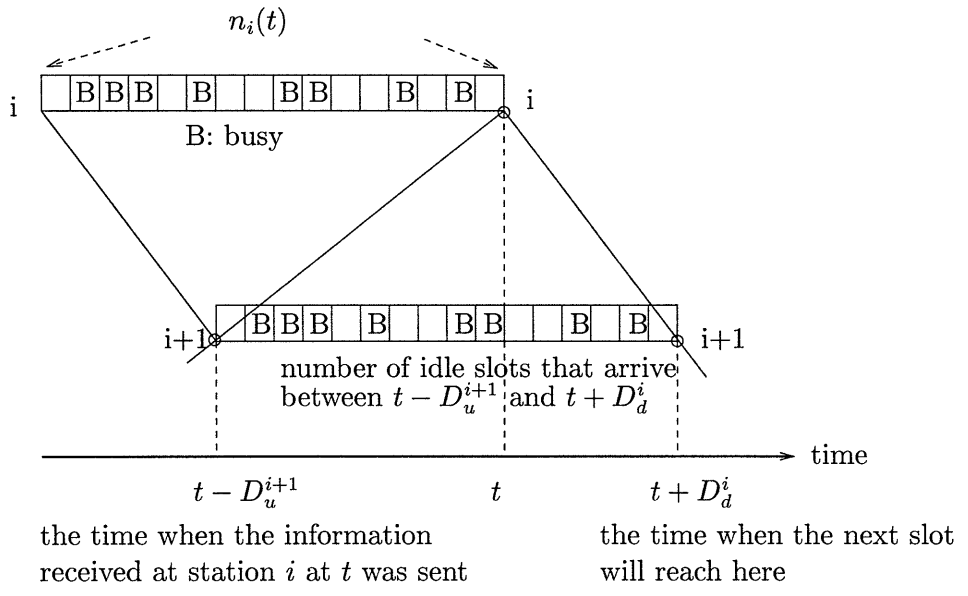

Figure 2: $n_i(t)$: the number of idle slots that have arrived at $i+1$ before the next slots arrives

- $m_i(t)$: estimated aggregate number of data segments in the FIFO queues of all stations downstream from station i (including i).

4.3 Distributed Algorithm

The algorithm is described in discrete time with the assumption of zero processing delay [2]. At time t, the information available at station i, $i \in [1,\ K]$, is $Q_i(t)$, $I_i(t)$, and $n_i(t)$. Before station i receives any information from downstream, it uses idels slots whenever it can with round robin counter $C_i(t)$ being 0. This is also the algorithm for the most downstream station K at all t, and,

$$m_K(t) = Q_K(t), \tag{4}$$

$$M_K(t) = I_K(t), \tag{5}$$

$$C_K(t) = 0.$$

In general, for time t, and station $i \in [1,\ K-1]$, the algorithm runs as follows:

1. receive $m_{i+1}(t - D_u^{i+1})$ and $M_{i+1}(t - D_u^{i+1})$ sent by station $i+1$ at $t - D_u^{i+1}$,

2. obtain the updated information $m_i^s(t)$ and $M_i^s(t)$ which correspond to $m_{i+1}(t - D_u^{i+1})$ and $M_{i+1}(t -$

[2] Appendix A illustrates the case with non-discrete time and non-zero processing delay

D_u^{i+1}) as follows,

$$m_i^s(t) = [m_{i+1}(t - D_u^{i+1}) - n_i(t)]^+, \tag{6}$$

$$M_i^s(t) = \min\{M_{i+1}(t - D_u^{i+1}),\ m_i^s(t)\}, \tag{7}$$

where $m_i^s(t)$ is the estimated current number of data segments in the FIFO queues of all stations strictly downstream from station i, and $M_i^s(t)$ is the estimated current number of active stations strictly downstream from station i.

3. update the counter and make a decision as follows:

$$C_i(t) = \min\{\tilde{C}_i(t-1),\ M_i^s(t)\}, \tag{8}$$

- if $I_i(t) = 1$, the slot passing by is idle, and $C_i(t) = 0$,
  then occupy it, and $\tilde{C}_i(t) = K - i$,
- if $I_i(t) = 1$, the slot passing by is idle, and $C_i(t) > 0$,
  then propagate it, and $\tilde{C}_i(t) = C_i(t) - 1$,
- if $I_i(t) = 1$, and the slot passing by is busy,
  then propagate it, and $\tilde{C}_i(t) = C_i(t)$,
- if $I_i(t) = 0$,
  then propagate the slot passing by, and $\tilde{C}_i(t) = K - i$.

4. obtain $M_i(t)$ and $m_i(t)$ as below, and send them to station $i - 1$,

$$m_i(t) = Q_i(t) + m_i^s(t), \tag{9}$$

$$M_i(t) = I_i(t) + M_i^s(t). \tag{10}$$

In review, the parameters used in the algorithm are, $n_i(t)$, $Q_i(t)$, $I_i(t)$, $M_i(t)$, $m_i(t)$, $M_i^s(t)$, $m_i^s(t)$, $C_i(t)$, and $\tilde{C}_i(t)$, for $i \in [1,\ K]$.

Notice that the core of the algorithm is the second step where station i uses the extra piece of information $n_i(t)$ to update $m_{i+1}(t - D_u^{i+1})$ and $M_{i+1}(t - D_u^{i+1})$. Take an example as in Figure 3. At time t, station i receives the information that there are 10 data segments and 5 active stations downstream ($m_{i+1}(t-D_u^{i+1}) = 10$ and $M_{i+1}(t - D_u^{i+1}) = 5$). On the other hand, station i needs to take consideration of $n_i(t) = 3$. In the absence of new arrivals, station i knows that there are 7 data segments left at the queues of at most 5 downstream stations (i.e., $m_i^s(t) = 7$ and $M_i^s(t) = 5$). Consider the same example except that $n_i(t) = 7$. Again, without new arrivals, station i knows that there are only 3 data segments left at the queues of at most 3 downstream stations (i.e., $m_i^s(t) = 3$ and $M_i^s(t) = 3$).

In order to guarantee the full utilization property, the decision made on idle slots should be based solely on the information received, not the probabilistic estimates of future arrivals. As a consequence, downstream

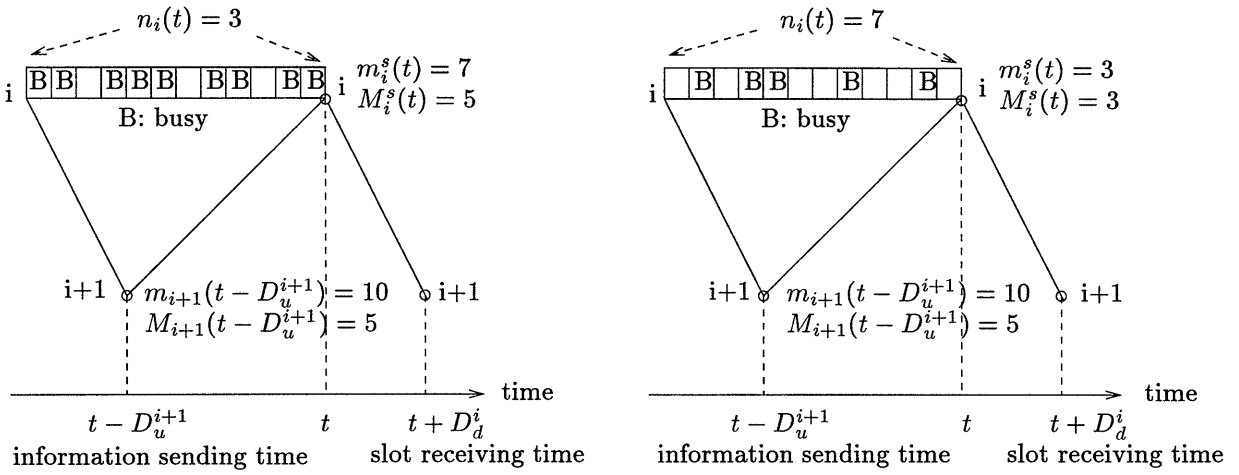

Figure 3: an example for the information updating step

stations still suffer from propagation delays. In order to compensate for this disadvantage, the protocol is designed with a bias towards downstream stations in the updating equation (7), where $M_i^s(t)$ takes its maximum possible value in the absence of new arrivals. This can be seen in the second example above. The 3 data segments left can be distributed at one station, or at most 3 stations, and $M_i^s(t) = 3$. On the other hand, the estimate $m_i^s(t)$, the total number of data segments downstream, is the true value in the absence of new arrivals. This ensures the full utilization property which is proved in Section 5.1.

4.4 Properties of the FUFA Protocol

In order to describe some basic properties, we first define the following parameters, for time t, s, and station i, $k \in [1, K]$,

- $A_i[t, t+s]$: number of arrivals at station i during the interval $[t, t+s)$; which is the time interval starting at the t-th time slot and ending right before the $(t+s)$-th time slot,
- $n_i[t, t+s]$: number of idle slots that station i propagates during the $[t, t+s)$; for a special shorthand notation with $s = D_u^{i+1} + D_d^i$,

$$n_i[t, t + D_u^{i+1} + D_d^i] = n_i(t + D_u^{i+1} + D_d^i),$$

- $N_i[t, t+s]$: number of idle slots that station i uses during $[t, t+s)$; thus,

$$n_{i+1}[t, t+s] = n_i[t - D_d^i, t + s - D_d^i] - N_{i+1}[t, t+s], \tag{11}$$

- $\tau_k^i(t)$: time when the information arriving at station i at t was sent from downstream station k, for $k > i$, or time when the information arrives at upstream station k, for $k \leq i$,

$$\tau_k^i(t) \triangleq t - \sum_{h=i+1}^{k} D_u^h \quad \text{for } k > i \qquad\qquad \tau_k^i(t) \triangleq t + \sum_{h=k+1}^{i} D_u^h \quad \text{for } k \leq i \tag{12}$$

- $T_k^i(t)$: time when the slot sent by station i at t arrives at downstream station k for $k > i$, or time when the slot was propagated from upstream station k, for $k \leq i$,

$$T_k^i(t) \triangleq t + \sum_{h=i}^{k-1} D_d^h \quad \text{for } k > i \qquad\qquad T_k^i(t) \triangleq t - \sum_{h=k}^{i-1} D_d^h \quad \text{for } k \leq i \tag{13}$$

See Figure 4 for the case when $k > i$.

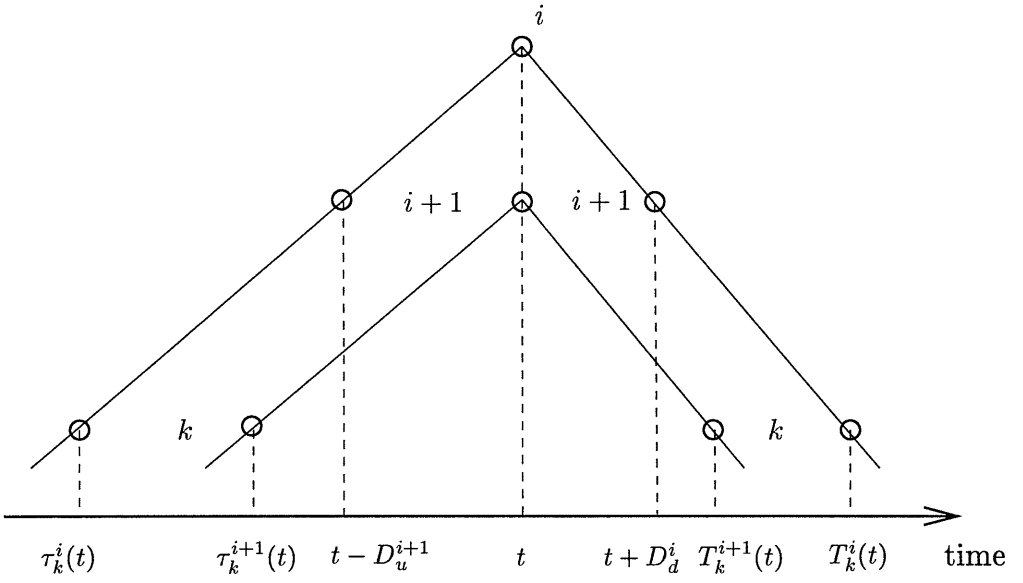

Figure 4: illustration of $\tau_k^i(t)$ and $T_k^i(t)$ for $k > i$

Propositions: For all t, s, and all $i \in [1,\ K-1]$, we have the following propositions.

Proposition 1: $Q_i(t) \geq I_i(t) \geq 0$.

Proof: By definition in (3), $I_i(t) = 1$ if $Q_i(t) > 0$, 0 otherwise. ■

Proposition 2: $m_i^s(t) \geq 0,\ m_{i+1}(t - D_u^{i+1}) \geq 0,\ M_i^s(t) \in [0,\ K-i],\ M_{i+1}(t - D_u^{i+1}) \in [0,\ K-i]$.

Proof: Use induction on i, from $i = K$ up to $i = 1$. ■

Proposition 3: $m_{i+1}(t - D_u^{i+1}) \geq m_i^s(t)$.

Proof: This is based on the updating equation (6) in the algorithm. ■

Proposition 4: $M_{i+1}(t - D_u^{i+1}) \geq M_i^s(t)$.

Proof: This is based on the updating equation (7) in the algorithm. ■

Proposition 5: $m_i^s(t) \geq M_i^s(t)$.

Proof: This is based on the updating equation (7) in the algorithm. ■

Proposition 6: $m_i(t) \geq M_i(t)$.

Proof: From Proposition 1 and Proposition 5,

$$Q_i(t) + m_i^s(t) \geq I_i(t) + M_i^s(t).$$

The result thus follows from (9) and (10). ■

Proposition 7: $M_i^s(t) \geq C_i(t) \geq 0$.

Proof: This comes from (8) in the counter updating step. ■

Proposition 8: $n_{i+1}[t,\ t+s] = n_i[t - D_d^i,\ t+s-D_d^i] - Q_{i+1}(t) - A_{i+1}[t,\ t+s] + Q_{i+1}(t+s)$.

Proof: From (11),

$$n_{i+1}[t,\ t+s] = n_i[t - D_d^i,\ t+s-D_d^i] - N_{i+1}[t,\ t+s].$$

The result follows since the change in queue size during an interval is the difference of arrivals and departures. ■

Proposition 9: $\sum_{k=i+2}^{l} N_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)] = n_{i+1}[t - D_u^{i+1},\ t + D_d^i] - n_l[T_l^{i+1}(t-D_u^{i+1}),\ T_l^i(t)]$.

Proof: Using (11) with $k-1$, $T_k^{i+1}(t-D_u^{i+1})$, and $T_k^i(t)$ in places of i, t, and $t+s$,

$$\begin{aligned} N_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)] &= n_{k-1}[T_k^{i+1}(t-D_u^{i+1}) - D_d^{k-1},\ T_k^i(t) - D_d^{k-1}] - n_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)] \\ &= n_{k-1}[T_{k-1}^{i+1}(t-D_u^{i+1}),\ T_{k-1}^i(t)] - n_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)]. \end{aligned} \quad (14)$$

Summing both side of (14) from $i+2$ to l, we have,

$$\begin{aligned} \sum_{k=i+2}^{l} N_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)] &= \sum_{k=i+2}^{l} (n_{k-1}[T_{k-1}^{i+1}(t-D_u^{i+1}),\ T_{k-1}^i(t)] - n_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)]) \\ &= n_{i+1}[T_{i+1}^{i+1}(t-D_u^{i+1}),\ T_{i+1}^i(t)] - n_l[T_l^{i+1}(t-D_u^{i+1}),\ T_l^i(t)] \\ &= n_{i+1}[t - D_u^{i+1},\ t + D_d^i] - n_l[T_l^{i+1}(t-D_u^{i+1}),\ T_l^i(t)], \end{aligned}$$

with $T_{i+1}^i(t) = t + D_d^i$. ■

Proposition 10: If station i has a non-empty queue and propagates all the idle slots arriving during $[t,\ t+s)$, then

$$C_i(t) - C_i(t+s) \geq n_i[t,\ t+s] \geq 0. \quad (15)$$

Proof: This follows from the counter updating step. While a station has a non-empty queue, its counter is decremented by at least one each time it propagates an idle slot. ■

Proposition 11: $M_i^s(t) \geq [M_{i+1}(t - D_u^{i+1}) - n_i(t)]^+$.

Proof: According to the updating equation (7) in the algorithm, we can break the proof into two cases.

- $M_i^s(t) = M_{i+1}(t - D_u^{i+1})$. We have

$$M_{i+1}(t - D_u^{i+1}) \geq [M_{i+1}(t - D_u^{i+1}) - n_i(t)]^+.$$

- $M_i^s(t) = m_i^s(t)$. We have

$$\begin{aligned} m_i^s(t) &= [m_{i+1}(t - D_u^{i+1}) - n_i(t)]^+ \\ &\geq [M_{i+1}(t - D_u^{i+1}) - n_i(t)]^+, \end{aligned}$$

which follows from the updating equation (6) in the algorithm and Proposition 6. ■

Next, we prove two lemmas here and two later in Section 5.2, which are useful in the proofs of full utilization, fairness and bounded access delay.

Lemma 1: For any given $i \in [1,\ K-1]$, any t,

$$m_i^s(t) \leq \sum_{k=i+1}^{K} Q_k(T_k^i(t)). \tag{16}$$

Remark: The main point of Lemma 1 is as follows. At time t, station i decides whether to use or propagate the slot passing by based on the estimated number $m_i^s(t)$ of data segments that will be waiting at downstream stations $i+1$, $i+2$, ..., K. Then the total number of data segments that the slot sees when it arrives at each downstream station $k \in [i+1,\ K]$ at $T_k^i(t)$ should be at least as large as the estimation $m_i^s(t)$. It might be larger due to the new arrivals at all the downstream stations $i+1$, $i+2$, ..., K. Thus, the lemma is useful in the proof of full utilization.

Proof: We use induction on i from $K-1$ to 1.

1. Let $i = K-1$. We have,

$$\begin{aligned} m_{K-1}^s(t) &= (m_K(t - D_u^K) - n_{K-1}(t))^+ \\ &= (Q_K(t - D_u^K) - n_{K-1}(t))^+ \\ &= (Q_K(t + D_d^{K-1}) - A_K[t - D_u^K,\ t + D_d^{K-1}] - n_K[t - D_u^K,\ t + D_d^{K-1}])^+ \\ &\leq Q_K(t + D_d^{K-1}). \end{aligned} \tag{17}$$

The first three equalities follow from (6), (4), and Proposition 8. The inequality is due to the nonnegativity of $Q_K(t + D_d^{K-1})$, $A_K[t - D_u^K,\ t + D_d^{K-1}]$, and $n_K[t - D_u^K,\ t + D_d^{K-1}]$.

2. Assume the inequality (16) is true for a given $i+1$, i.e.,

$$m_{i+1}^s(t - D_u^{i+1}) \leq \sum_{k=i+2}^{K} Q_k(T_k^{i+1}(t - D_u^{i+1})). \tag{18}$$

According to (6), (9), Proposition 8, nonnegativity of $A_{i+1}[t - D_u^{i+1},\ t + D_d^i]$, and (18),

$$\begin{aligned} m_i^s(t) &= [m_{i+1}(t - D_u^{i+1}) - n_i(t)]^+ \\ &= [Q_{i+1}(t - D_u^{i+1}) + m_{i+1}^s(t - D_u^{i+1}) - n_i(t)]^+ \\ &= [Q_{i+1}(t + D_d^i) - A_{i+1}[t - D_u^{i+1},\ t + D_d^i] - n_{i+1}[t - D_u^{i+1},\ t + D_d^i] + m_{i+1}^s(t - D_u^{i+1})]^+ \quad (19) \\ &\leq [Q_{i+1}(t + D_d^i) - n_{i+1}[t - D_u^{i+1},\ t + D_d^i] + \sum_{k=i+2}^{K} Q_k(T_k^{i+1}(t - D_u^{i+1}))]^+ \end{aligned}$$

Combining with the fact that,

$$\begin{aligned} Q_k(T_k^{i+1}(t - D_u^{i+1})) &= Q_k(T_k^i(t)) - A_k[T_k^i(t - D_u^{i+1}],\ T_k^i(t)) + N_k[T_k^{i+1}(t - D_u^{i+1}),\ T_k^i(t)] \\ &\leq Q_k(T_k^i(t)) + N_k[T_k^{i+1}(t - D_u^{i+1}),\ T_k^i(t)], \end{aligned}$$

we have,

$$\begin{aligned} m_i^s(t) &\leq \{Q_{i+1}(t + D_d^i) - n_{i+1}[t - D_u^{i+1},\ t + D_d^i] + \sum_{k=i+2}^{K} [(Q_k(T_k^i(t)) + N_k[T_k^{i+1}(t - D_u^{i+1}),\ T_k^i(t)]]\}^+ \\ &= \{ \sum_{k=i+1}^{K} Q_k(T_k^i(t)) - n_{i+1}[t - D_u^{i+1},\ t + D_d^i] + \sum_{k=i+2}^{K} N_k[T_k^{i+1}(t - D_u^{i+1}),\ T_k^i(t)] \}^+ \\ &= \{ \sum_{k=i+1}^{K} Q_k(T_k^i(t)) - n_K[T_K^{i+1}(t - D_u^{i+1}),\ T_K^i(t)] \}^+ \quad (20) \\ &\leq \sum_{k=i+1}^{K} Q_k(T_k^i(t)) \quad (21) \end{aligned}$$

where (20) is based on Proposition 9 with $l = K$. (21) is based on the nonnegativity of $Q_k(T_k^i(t))$ and $n_K[T_K^{i+1}(t - D_u^{i+1}),\ T_K^i(t)]$. ■

Lemma 2: For all t, and all $i \in [1, K-1]$, the following two statements are true:

$$m_i^s(t) > 0 \text{ iff } M_i^s(t) > 0.$$

$$m_i(t) > 0 \text{ iff } M_i(t) > 0$$

Remark. Lemma 2 formalizes the intuitive fact that the estimated number of downstream data segments is positive if and only if the estimated number of active downstream stations is positive.

Proof: The backward statements can be seen from Proposition 5 and Proposition 6. We prove that the pair of forward statements are true by induction on $i = K-1, ..., 1$.

1. $i = K-1$. Based on (4) and (5),

$$Q_K(t) = m_K(t) > 0 \Rightarrow M_K(t) = I_K(t) > 0. \tag{22}$$

Then,

$$\begin{aligned} m^s_{K-1}(t) > 0 &\Rightarrow m_K(t - D^K_u) > 0 \\ &\Rightarrow M_K(t - D^K_u) > 0 \\ &\Rightarrow M^s_{K-1}(t) = \min\{M_K(t - D^K_u),\ m^s_{K-1}(t)\} > 0 \end{aligned} \tag{23}$$

according to Proposition 3, (22), and (7) in the updating step respectively. Based on (9) in the algorithm, i.e.,

$$m_{K-1}(t) = Q_{K-1}(t) + m^s_{K-1}(t),$$

we have

$$\begin{aligned} m_{K-1}(t) > 0 &\Rightarrow \text{at least one of } Q_{K-1}(t) \text{ and } m^s_{K-1}(t) \text{ is positive} \\ &\Rightarrow \text{at least one of } I_{K-1}(t) \text{ and } M^s_{K-1}(t) \text{ is positive} \\ &\Rightarrow M_{K-1}(t) = I_{K-1}(t) + M^s_{K-1}(t) > 0. \end{aligned}$$

Thus we have established the basis for the pair of statements.

2. Assume that the pair of statements are true for a given $i+1$, so that, in paticular,

$$m_{i+1}(t - D^{i+1}_u) > 0 \Rightarrow M_{i+1}(t - D^{i+1}_u) > 0.$$

As in (23), we have

$$\begin{aligned} m^s_i(t) > 0 &\Rightarrow m_{i+1}(t - D^{i+1}_u) > 0 \\ &\Rightarrow M_{i+1}(t - D^{i+1}_u) > 0 \\ &\Rightarrow M^s_i(t) = \min\{M_{i+1}(t - D^{i+1}_u),\ m^s_i(t)\} > 0 \end{aligned}$$

Thus, the first statement is true given the induction hypothesis.

Based on (9) in the algorithm, i.e., $m_i(t) = Q_i(t) + m_i^s(t)$,

$$\begin{aligned} m_i(t) > 0 \quad &\Rightarrow \quad \text{at least one of } Q_i(t) \text{ and } m_i^s(t) \text{ is positive} \\ &\Rightarrow \quad \text{at least one of } I_i(t) \text{ and } M_i^s(t) \text{ is positive} \\ &\Rightarrow \quad M_i(t) = I_i(t) + M_i^s(t) > 0. \end{aligned}$$

Thus, the induction proof is complete. ■

5 Proof of Full Utilization, Fairness and Bounded Access Delay

5.1 Proof of Full Utilization

Theorem 1: The protocol FUFA has full utilization according to Definition 1 in section 3.1.

Proof: For the most downstream station K, an idle slot is allowed to pass by only if the FIFO queue is empty. Therefore, we only need to prove the full utilization statement for station $i \in [1,\ K-1]$. At time t if an idle slot gets propagated by a station i with a non-empty FIFO queue, then according to the algorithm, we must have $M_i^s(t) \geq C_i(t) > 0$, which implies that $m_i^s(t) > 0$ from Lemma 2. Then based on Lemma 1, we must have

$$\sum_{k=i+1}^{K} Q_k(T_k^i(t)) > 0. \tag{24}$$

Therefore, it is sufficient to show the following statement.

Statement 1: if an idle slot arrives at station $i \in [1, K-1]$ at t with $\sum_{k=i+1}^{K} Q_k(T_k^i(t)) > 0$, and gets propagated, then the idle slot must be used by one of the downstream stations.

We prove Statement 1 by induction on i from $K-1$ to 1.

1. Let $i = K-1$. We have
$$Q_K(t + D_d^{K-1}) = Q_K(T_K^{K-1}(t)) > 0.$$
According to the algorithm, station K uses the idle slot.

2. Assume that the statement is true for a given $i+1$. The idle slot propagated at time t by station i with $\sum_{k=i+1}^{K} Q_k(T_k^i(t)) > 0$ arrives at station $i+1$ at $t + D_d^i$. There are three cases to consider at station $i+1$.

   Case 1: $Q_{i+1}(t + D_d^i) > 0$ and the idle slot is occupied by a data segment at station $i+1$.

   Case 2: $Q_{i+1}(t + D_d^i) > 0$ and the idle slot is propagated downstream. According to the algorithm, we have a similar argument as in (24) for station $i+1$, i.e., $\sum_{k=i+2}^{K} Q_k(T_k^{i+1}(t + D_d^i)) > 0$. Based on

the induction assumption for station $i+1$, the idle slot will be used by one of the downstream stations $k \in [i+2,\ K]$.

Case 3: $Q_{i+1}(T^i_{i+1}(t)) = Q_{i+1}(t + D^i_d) = 0$, so that the idle slot is propagated downstream. Then, based on (13),

$$\sum_{k=i+2}^{K} Q_k(T^{i+1}_k(t + D^i_d)) = \sum_{k=i+2}^{K} Q_k(T^i_k(t)) = \sum_{k=i+1}^{K} Q_k(T^i_k(t)) > 0.$$

According to the induction assumption for station $i+1$, the idle slot will be used by one of the downstream stations $k \in [i+2,\ K]$.

Hence the idle slot is used by one of the downstream stations from i in all three cases. ■

5.2 Proof of Fairness

In order to prove the fairness property of the FUFA protocol, we first need to prove Lemmas 3 and 4 below.

Lemma 3: For any given $i \in [1,\ K-1]$, any t,

$$m^s_i(t) \geq [\ \sum_{k=i+1}^{K} (Q_k(T^i_k(t)) - A_k[\tau^i_k(t),\ T^i_k(t)])\ ]^+. \tag{25}$$

Remark: The main point of Lemma 3 is as follows. At time t, station i decides whether to use or propagate the slot passing by based on the estimated number $m^s_i(t)$ of data segments that will be waiting at downstream stations $i+1$, $i+2$, ..., K. Then the total number of data segments that the slot sees when it arrives at each downstream station $k \in [i+1,\ K]$ at $T^i_k(t)$ should be no larger than that estimate $m^s_i(t)$ plus all the new arrivals.

Proof: We use induction on i from $K-1$ to 1.

1. Let $i = K-1$. From (17), we have,

$$\begin{aligned} m^s_{K-1}(t) &= (Q_K(t + D^{K-1}_d) - A_K[t - D^K_u,\ t + D^{K-1}_d] - n_K[t - D^K_u,\ t + D^{K-1}_d])^+ \\ &= (Q_K(t + D^{K-1}_d) - A_K[t - D^K_u,\ t + D^{K-1}_d])^+ \qquad (26) \\ &= (Q_K(T^{K-1}_K(t)) - A_K[\tau^{K-1}_K(t),\ T^{K-1}_K(t)])^+. \end{aligned}$$

where (26) follows from full utilization, which implies that $n_K(t + D^{K-1}_d) > 0$ only if $Q_K(t + D^{K-1}_d) - A_K[t - D^K_u,\ t + D^{K-1}_d] \leq 0$.

2. Assume the inequality (25) is true for a given $i+1$, i.e.,

$$m^s_{i+1}(t - D^{i+1}_u) \geq \{\ \sum_{k=i+2}^{K} (Q_k(T^{i+1}_k(t - D^{i+1}_u)) - A_k[\tau^{i+1}_k(t - D^{i+1}_u),\ T^{i+1}_k(t - D^{i+1}_u)])\}^+. \tag{27}$$

Combining (19) and (27), we have

$$\begin{aligned} m_i^s(t) \geq\ & \{Q_{i+1}(t+D_d^i) - A_{i+1}[t-D_u^{i+1},\ t+D_d^i] - n_{i+1}[t-D_u^{i+1},\ t+D_d^i] \\ & +[\sum_{k=i+2}^{K}(Q_k(T_k^{i+1}(t-D_u^{i+1})) - A_k[\tau_k^{i+1}(t-D_u^{i+1}),\ T_k^{i+1}(t-D_u^{i+1})])]^+\}^+ \end{aligned}$$

Combining with the fact that,

$$\begin{aligned} & Q_k(T_k^{i+1}(t-D_u^{i+1})) - A_k[\tau_k^{i+1}(t-D_u^{i+1}),\ T_k^{i+1}(t-D_u^{i+1})] = \\ & \qquad Q_k(T_k^i(t)) - A_k[\tau_k^i(t),\ T_k^i(t)] + N_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)], \end{aligned}$$

we have,

$$\begin{aligned} m_i^s(t) \geq\ & \{Q_{i+1}(t+D_d^i) - A_{i+1}[t-D_u^{i+1},\ t+D_d^i] - n_{i+1}[t-D_u^{i+1},\ t+D_d^i] \\ & +[\sum_{k=i+2}^{K}(Q_k(T_k^i(t)) - A_k[\tau_k^i(t),\ T_k^i(t)] + N_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)])]^+\}^+ \\ =\ & \{\sum_{k=i+1}^{K}(Q_k(T_k^i(t)) - A_k[\tau_k^i(t),\ T_k^i(t)]) - n_{i+1}[t-D_u^{i+1},\ t+D_d^i] \\ & +\sum_{k=i+2}^{K} N_k[T_k^{i+1}(t-D_u^{i+1}),\ T_k^i(t)]\ \}^+ \\ =\ & \{\sum_{k=i+1}^{K}(Q_k(T_k^i(t)) - A_k[\tau_k^i(t),\ T_k^i(t)]) - n_K[T_K^{i+1}(t-D_u^{i+1}),\ T_K^i(t)]\ \}^+ \qquad (28) \end{aligned}$$

where (28) is based on Proposition 9 with $l = K$. If $Q_k(T_k^i(t)) - A_K[\tau_k^i(t),\ T_k^i(t)] > 0$ for some $k \in [i+1,\ K]$, then station K has a non-empty queue from $\tau_k^i(t)$ to $T_k^i(t)$, and then, by full utilization, $n_K[T_K^{i+1}(t-D_u^{i+1}),\ T_K^i(t)] = 0$. Therefore, $n_K[T_K^{i+1}(t-D_u^{i+1}),\ T_K^i(t)] > 0$ only if $\sum_{k=i+1}^{K}(Q_k(T_k^i(t)) - A_k[\tau_k^i(t),\ T_k^i(t)]) \leq 0$. Combining with (28),

$$m_i^s(t) \geq [\sum_{k=i+1}^{K}(Q_k(T_k^i(t)) - A_k[\tau_k^i(t),\ T_k^i(t)])\ ]^+.$$

■

Lemma 4: For any $i \in [1,\ K-1]$, and any t,

$$\sum_{k=i+1}^{K} I_k(\tau_k^i(t)) \geq M_i^s(t). \qquad (29)$$

Remark. Lemma 4 is intuitive based on the fact that taking extra idle slots into consideration in the information updating can only reduce the estimated number of active downstream stations among $i+1$,

$i+2$, ..., K.

Proof: We use induction on i from $K-1$ to 1.

1. Let $i = K-1$. We have $I_K(\tau_K^{K-1}(t)) = I_K(t-D_u^{i+1}) = M_K(t-D_u^{i+1}) \geq M_i^s(t)$ according to Proposition 4, which establishes the basis.

2. Assume the statement is true for a given $i+1$. Using $i+1$ and $t - D_u^{i+1}$ in place of i and t, (29) becomes,

$$\sum_{k=i+2}^{K} I_k(\tau_k^{i+1}(t - D_u^{i+1})) \geq M_{i+1}^s(t - D_u^{i+1}) \tag{30}$$

Therefore,

$$\begin{aligned}
\sum_{k=i+1}^{K} I_k(\tau_n^i(t)) &= I_{i+1}(t - D_u^{i+1}) + \sum_{k=i+2}^{K} I_k(\tau_k^{i+1}(t - D_u^{i+1})) \\
&\geq I_{i+1}(t - D_u^{i+1}) + M_{i+1}^s(t - D_u^{i+1}) \\
&= M_{i+1}(t - D_u^{i+1}) \\
&\geq M_i^s(t)
\end{aligned}$$

according to (30), (10), and Proposition 4 respectively.

Thus, we have completed the induction. ■

Definition 4: The set $S_n = \{i_1 < i_2 < ... < i_n\}$ has been "very active" since t_0 if, for each station $i_k \in S_n$, and each $t \geq T_{i_k}^{i_1}(t_0) = t_0 + \sum_{h=i_1}^{i_k-1} D_d^h$, the queue length at time t exceeds the number of new arrivals in the interval from t back to the past round trip delay between i_k and i_1 (i.e., some packet in queue at $\tau_{i_k}^{i_1}(t)$ is still in queue at $T_{i_k}^{i_1}(t)$), i.e.,

$$Q_{i_k}(T_{i_k}^{i_1}(t)) > A_{i_k}[\tau_{i_k}^{i_1}(t),\ T_{i_k}^{i_1}(t)]. \tag{31}$$

See Figure 5 for an illustration.

Theorem 2: The protocol FUFA is fair according to Definition 2 in Section 3.1.

Proof: For any station $i_k \in S_n$ that is "very active" at any $t \geq T_{i_k}^{i_1}(t_0)$, (31) implies that

$$I_{i_k}(s) = 1\ \forall s \in [\tau_{i_k}^{i_1}(t),\ T_{i_k}^{i_1}(t)], \tag{32}$$

$$Q_{i_k}(s_2) > A[s_1,\ s_2],\ \text{for any } [s_1,\ s_2) \subseteq [\tau_{i_k}^{i_1}(t),\ T_{i_k}^{i_1}(t)). \tag{33}$$

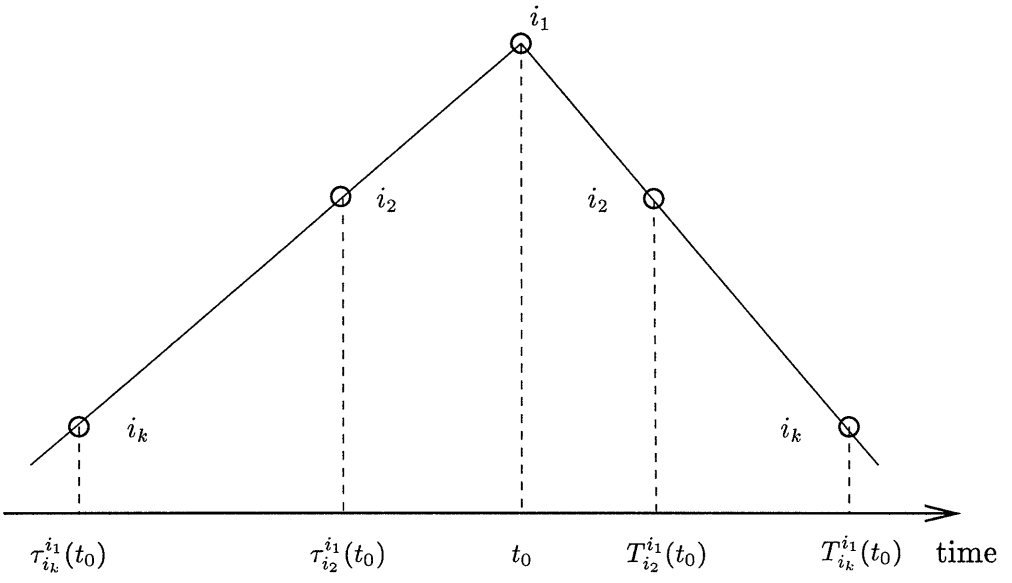

Figure 5: illustration of $\tau_{i_k}^{i_1}(t_0)$ and $T_{i_k}^{i_1}(t_0)$ for $i_k \in S_n$

With the assumption that all the other stations remain idle as in Definition 2, we have

$$M_{i_k}^s(t) \leq \sum_{l=i_k+1}^{K} I_l(\tau_l^{i_k}(t)) = n - k, \tag{34}$$

according to Lemma 4 and (32) with $\tau_l^{i_k}(t) \geq \tau_l^{i_1}(t)$, respectively.

Next, we show that for any $i \geq i_1$, and $t \geq T_i^{i_1}(t_0)$, the following inequality is true,

$$M_i^s(t) \geq \sum_{k=i+1}^{K} I_k(T_k^i(t)) \tag{35}$$

by induction on $i = K-1, \ ..., \ i_1$.

1. Let $i = K-1$. We need to prove that

$$M_{K-1}^s(t) \geq I_K(t + D_d^{K-1}). \tag{36}$$

This leads to two cases.

- Station K is one of the idle stations, i.e., $I_K(t + D_d^{K-1}) = 0$, and (36) follows from Proposition 2.
- Station $K \in S_n$. Based on (5) and (32) with $t - D_u^K \geq \tau_K^{i_1}(t_0)$,

$$M_K(t - D_u^K) = I_K(t - D_u^K) = 1.$$

And, based on (26) and (33) with $[t - D_u^K,\ t + D_d^{K-1}) \subseteq [\tau_K^{i_1}(t),\ T_K^{i_1}(t))$,

$$m_{K-1}^s(t) = (Q_K(t + D_d^{K-1}) - A_K[t - D_u^K,\ t + D_d^{K-1}])^+ \geq 1.$$

Therefore, according to the updating step (7) in the algorithm,

$$M_{K-1}^s(t) = \min\{M_K(t - D_u^K),\ m_{K-1}^s(t)\} \geq 1 = I_K(t + D_d^{K-1}).$$

2. Assume (35) is true for any given $i + 1$. Therefore,

$$M_{i+1}^s(t - D_u^{i+1}) \geq \sum_{k=i+2}^{K} I_k(T_k^{i+1}(t - D_u^{i+1})). \tag{37}$$

Then,

$$\begin{aligned} M_{i+1}(t - D_u^{i+1}) &= I_{i+1}(t - D_u^{i+1}) + M_{i+1}^s(t - D_u^{i+1}) \\ &\geq I_{i+1}(t - D_u^{i+1}) + \sum_{k=i+2}^{K} I_k(T_k^{i+1}(t - D_u^{i+1})) \\ &= I_{i+1}(t + D_d) + \sum_{k=i+2}^{K} I_k(T_k^i(t)) \\ &= \sum_{k=i+1}^{K} I_k(T_k^i(t)) \end{aligned}$$

according to (10), (37), (32) with the fact that $T_k^{i+1}(t - D_u^{i+1}) \in [\tau_k^i(t),\ T_k^i(t)] \subseteq [\tau_k^{i_1}(t),\ T_k^{i_1}(t)]$, and idle stations stay idle during $[\tau_k^{i_1}(t),\ T_k^{i_1}(t)]$. Moreover, based on Lemma 3,

$$m_i^s(t) \geq \{ \sum_{k=i+1}^{K} (Q_k(T_k^i(t)) - A_k[\tau_k^i(t)),\ T_k^i(t)]) \}^+ \geq \sum_{k=i+1}^{K} I_k(T_k^i(t))$$

where the second inequality is due to the fact that,

$$\begin{aligned} &\text{for any } k \notin S_n,\ Q_k(T_k^i(t)) - A_k[\tau_k^i(t)),\ T_k^i(t)] = 0 = I_k(T_k^i(t)), \\ &\text{for any } k \in S_n,\ Q_k(T_k^i(t)) - A_k[\tau_k^i(t)),\ T_k^i(t)] \geq 1 = I_k(T_k^i(t)). \end{aligned}$$

Therefore, according to the updating step (7) in the algorithm,

$$M_i^s(t) = \min\{M_{i+1}(t - D_u^{i+1}),\ m_i^s(t)\} \geq \sum_{k=i+1}^{K} I_k(T_k^i(t)).$$

Thus, we have completed the induction proof for (35).

Based on (35), for any $i_k \in S_n$, and any $t \geq T_{i_k}^{i_1}(t_0) = t_0 + \sum_{h=i_1}^{i_k-1} D_d^h$

$$M_{i_k}^s(t) \geq \sum_{l=i_k+1}^{K} I_l(T_l^{i_k}(t)) = n - k.$$

Combining with (34), we have,

$$M_{i_k}^s(t) = n - k.$$

Hence, starting from $t_0 + \sum_{h=i_1}^{i_k-1} D_d^h$, each station $i_k \in S_n$ propagates an idle slot passing by when the counter $C_i(t)$ is positive, and decrements it by one until the counter gets to zero. When the counter gets to zero, station i_k occupies the next idle slot with its own data segment in queue, and resets the counter to $n - k$. This is a perfect round robin cycle, where during each n time units,, the most upstream station i_1 uses one of the idle slots and propagates the remaining $n-1$ idle slots. The station i_2 uses one of these $n-1$ idle slots and propagates the remaining $n-2$, and so forth to station i_n. Then each station gets one of the n slots for its own transmission. ■

5.3 Proof of Bounded Access Delay

Theorem 3: The protocol FUFA has the bounded access delay property; for each station $i \in [1,\ K]$ and each first data segment P_i in queue, the access delay $t_d^i - t_a^i \leq B_i = \sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k) + K - 1$.

Proof: For any $i \in [1,\ K]$, any packet P_i, and any $k,\ h$ satisfying $1 \leq k \leq h < i$, and any t, define the following parameters,

- $t_k \triangleq \tau_k^i(t_a^i) = t_a^i + \sum_{h=k}^{i} D_u^{h+1}$. Note that $t_i = t_a^i$,
- r_k: the first time that counter $C_k(t)$ is set to $M_k^s(t)$ by (8) after t_k, i.e.,

$$r_k \triangleq \min\{t \geq t_k \mid C_k(t) = M_k^s(t)\} \tag{38}$$

- $J_h^k(t)$: $J_h^k(t) \triangleq 1$ if $I_h(\tau_h^k(t)) = 1$ and $N_h(\tau_h^k(t),\ T_h^k(t)) = 0$; 0 otherwise.

  Based on the definition, we have,

$$1 \geq I_h(\tau_h^k(t)) \geq J_h^k(t) \geq 0 \tag{39}$$

$$J_h^{k+1}(t - D_u^{k+1}) \geq J_h^k(t) \tag{40}$$

Part One: Show that the statement is true for $i = 1$, i.e., $t_d^1 - t_a^1 \leq K - 1$.

Since station 1 propagates all the $(t_d^1 - t_a^1)$ idle slots during $[t_a^1,\ t_d^1 - 1]$ while data segment P_1 is waiting at the queue, according to (15) in Proposition 10, we have,

$$C_1(t_a^1) - C_1(t_d^1) \geq n_1(t_a^1,\ t_d^1) = t_d^1 - t_a^1 \tag{41}$$

Based on Proposition 2 and Proposition 7, we have,

$$C_1(t_a^1),\ C_1(t_d^1) \in [0,\ K-1] \tag{42}$$

Combining (41) with (42), we obtain,

$$t_d^1 - t_a^1 \leq K - 1.$$

Part Two: Show the statement is true for any station $i \in [2,\ K]$.

With similar arguments as in Part One, we can conclude that at most $K-i$ idles slots can be propagated to downstream stations before data segment P_i fills an idle slot. This leaves us to show that each upstream station k, $k \in [1,\ i-1]$, can use at most one idle slot between t_k and $T_k^i(t_d^i)$. Since the round robin counter $C_k(t)$ is set to $M_k^s(t)$ after each time station k uses an idle slot, it is sufficient to show that each station $k \in [1,\ i-1]$ uses no idle slot between r_k and $T_k^i(t_d^i)$. Here, we prove the following two stronger statements. For any upstream station $k \in [1,\ i-1]$, for any $t \in [r_k,\ T_k^i(t_d^i)]$, we have,

Statement 1: $M_k^s(t) > \sum_{h=k+1}^{i-1} J_h^k(t) + C_i(T_i^k(t))$,

Statement 2: $N_k[r_k,\ T_k^i(t_d^i)+1] = 0$.

We prove both statements using induction on $k = i-1,\ ...,\ 1$.

Part A: Let $k = i-1$. Show that both statements are true.

Part A1: Show that Statement 1 is true, i.e.,

$$M_{i-1}^s(t) > C_i(T_i^{i-1}(t)). \tag{43}$$

Based on (7),

$$M_{i-1}^s(t) = \min\{M_i(t-D_u^i),\ m_{i-1}^s(t)\}. \tag{44}$$

We now lower bound the first term in the minimum above.

$$\begin{aligned} M_i(t-D_u^i) &= I_i(t-D_u^i) + M_i^s(t-D_u^i) \\ &\geq 1 + C_i(t-D_u^i) \\ &\geq 1 + C_i(T_i^{i-1}(t)) \end{aligned}$$

according to (10), the fact that station i has data segment P_i in queue and Proposition 7, Proposition 10, respectively.

We now lower bound the second term in the minimum of (44). Based on (6) and (9),

$$\begin{aligned} m_{i-1}^s(t) &= [m_i(t-D_u^i) - n_{i-1}(t)]^+ \\ &= [Q_i(t-D_u^i) + m_i^s(t-D_u^i) - n_{i-1}(t)]^+. \end{aligned} \tag{45}$$

Note that

$$n_{i-1}(t) = n_i[t - D_u^i,\ t + D_d^{i-1}] + N_i[t - D_u^i,\ t + D_d^{i-1}] = n_i[t - D_u^i,\ t + D_d^{i-1}] \tag{46}$$

from (11) with $N_i[t - D_u^i,\ t + D_d^{i-1}] = 0$. Combining (45) with Proposition 5 and (46), we have,

$$\begin{aligned} m_{i-1}^s(t) &\geq (Q_i(t - D_u^i) + M_i^s(t - D_u^i) - n_i[t - D_u^i,\ t + D_d^{i-1}])^+ \\ &\geq (Q_i(t - D_u^i) + C_i(t - D_u^i) - n_i[t - D_u^i,\ t + D_d^{i-1}])^+ \\ &\geq 1 + C_i(T_i^{i-1}(t)) \end{aligned}$$

where the last two inequalities are based on Proposition 7, the fact that station i has data segment P_i in queue, and Proposition 10, respectively.

Part A2: Show that Statement 2 is true, i.e.,

$$N_{i-1}[r_{i-1},\ T_{i-1}^i(t_d^i) + 1] = 0.$$

According to the algorithm, station $i-1$ uses no idle slot if $C_{i-1}(t)$ is positive for all $t \in [r_{i-1},\ T_{i-1}^i(t_d^i)]$. Therefore, it is sufficient to prove the following inequality,

$$C_{i-1}(t) > C_i(T_i^{i-1}(t)) \qquad \forall t \in [r_{i-1},\ T_{i-1}^i(t_d^i)] \tag{47}$$

since the right hand side is nonnegative.

We prove this by induction on $t = r_{i-1},\ ...,\ T_{i-1}^i(t_d^i)$.

1. Let $t = r_{i-1}$. Based on the definition (38),

$$C_{i-1}(r_{i-1}) = M_{i-1}^s(r_{i-1}) > C_i(T_i^{i-1}(r_{i-1}))$$

where the second inequality is based on (43). Thus, we have established the basis.

2. Assume (47) is true for a given t, $t \in [r_{i-1},\ T_{i-1}^i(t_d^i) - 1]$, i.e.,

$$C_{i-1}(t) > C_i(T_i^{i-1}(t)). \tag{48}$$

We need to prove that it is also true for $t+1$, i.e.,

$$C_{i-1}(t+1) > C_i(T_i^{i-1}(t+1)). \tag{49}$$

Consider the following two cases:

Case one: the slot passing by station $i-1$ at t is not idle. Thus,

$$C_{i-1}(t+1) = \min\{C_{i-1}(t),\ M^s_{i-1}(t+1)\}. \tag{50}$$

Based on the induction assumption (48) and Proposition 10,

$$C_{i-1}(t) > C_i(T_i^{i-1}(t)) \geq C_i(T_i^{i-1}(t+1)). \tag{51}$$

Based on (43) with $t+1$ in place of t, we have,

$$M^s_{i-1}(t+1) > C_i(T_i^{i-1}(t+1)) \tag{52}$$

Combining (50) with (51) and (52), we obtain inequality (49) for case one.

Case two: the slot passing by station $i-1$ at t is idle. Due to the induction assumption (48), $C_{i-1}(t) > 0$. Thus, the idle slot is propagated downstream. Thus,

$$C_{i-1}(t+1) = \min\{C_{i-1}(t) - 1,\ M^s_{i-1}(t+1)\}. \tag{53}$$

The idle slot must be propagated by station i at $T_i^{i-1}(t)$ since $T_i^{i-1}(t) < t_d^i$, which results in

$$C_i(T_i^{i-1}(t)) - C_i(T_i^{i-1}(t+1)) \geq n[T_i^{i-1}(t),\ T_i^{i-1}(t+1)] = 1 \tag{54}$$

according to Proposition 10.

Therefore, according to (48) and (54),

$$C_{i-1}(t) - 1 \quad > \quad C_i(T_i^{i-1}(t)) - 1 \geq C_i(T_i^{i-1}(t+1)). \tag{55}$$

Combining (53) with (55) and (52), we obtain inequality (49) for case two.

Thus, the induction proof on (47) is complete. We have established the basis for both statements 1 and 2.

Part B: For a given $k \in [1,\ i-2]$, assume both statements 1 and 2 are true for upstream stations $i-1$, $i-2$, ..., $k+1$. We need to show that they are also true for station k, i.e., for any $t \in [r_k,\ T_k^i(t_d^i)]$,

$$M^s_k(t) > \sum_{h=k+1}^{i-1} J^k_h(t) + C_i(T_i^k(t)), \tag{56}$$
$$N_k[r_k,\ T_k^i(t_d^i) + 1] = 0.$$

Part B1: Prove (56) with the induction assumption.

According to (7),

$$M_k^s(t) = \min\{M_{k+1}(t - D_u^{k+1}),\ m_k^s(t)\}. \tag{57}$$

We now lower bound the first term in the minimum above. Using (10),

$$M_{k+1}(t - D_u^{k+1}) \quad = \quad I_{k+1}(t - D_u^{k+1}) + M_{k+1}^s(t - D_u^{k+1}). \tag{58}$$

From (39),

$$I_{k+1}(t - D_u^{k+1}) = I_{k+1}(\tau_{k+1}^k(t)) \geq J_{k+1}^k(t). \tag{59}$$

Based on the induction assumption on Statement 1 for $k+1$ with $t - D_u^{k+1}$ in place of t,

$$M_{k+1}^s(t - D_u^{k+1}) \quad > \quad \sum_{h=k+2}^{i-1} J_h^{k+1}(t - D_u^{k+1}) + C_i(T_i^{k+1}(t - D_u^{k+1})) \tag{60}$$

$$\geq \quad \sum_{h=k+2}^{i-1} J_h^k(t) + C_i(T_i^k(t)) \tag{61}$$

where (61) is based on (40) and Proposition 10. Combining (58) with (59) and (61), we have,

$$M_{k+1}(t - D_u^{k+1}) > \sum_{h=k+1}^{i-1} J_h^k(t) + C_i(T_i^k(t)). \tag{62}$$

We now lower bound the second term in the minimum of (57). Based on (6) and (9),

$$\begin{aligned} m_k^s(t) \quad &= \quad [m_{k+1}(t - D_u^{k+1}) - n_k(t)]^+ \\ &= \quad [m_{k+1}^s(t - D_u^{k+1}) + Q_{k+1}(t - D_u^{k+1}) - n_k(t)]^+. \end{aligned} \tag{63}$$

Note that from (11) and (11),

$$n_k(t) = n_k[t - D_u^{k+1} - D_d^k,\ t] = n_{k+1}[t - D_u^{k+1},\ t + D_d^k] + N_{k+1}[t - D_u^{k+1},\ t + D_d^k]. \tag{64}$$

Combining (63) with Proposition 5, Proposition 1 and (64), we have,

$$\begin{aligned} m_k^s(t) \quad &\geq \quad (M_{k+1}^s(t - D_u^{k+1}) + I_{k+1}(t - D_u^{k+1}) - n_{k+1}[t - D_u^{k+1},\ t + D_d^k] - N_{k+1}[t - D_u^{k+1},\ t + D_d^k])^+ \\ &> \quad (\sum_{h=k+2}^{i-1} J_h^{k+1}(t - D_u^{k+1}) + C_i(T_i^{k+1}(t - D_u^{k+1})) + I_{k+1}(t - D_u^{k+1}) \\ &\quad -n_{k+1}[t - D_u^{k+1},\ t + D_d^k] - N_{k+1}[t - D_u^{k+1},\ t + D_d^k])^+ \triangleq [RHS]^+ \end{aligned} \tag{65}$$

where the second inequality is based on (60) and only valid when $RHS \geq 0$.

According to Proposition 9 with k and i in place of i and l, we have,

$$\begin{aligned} n_{k+1}[t - D_u^{k+1},\ t + D_d^k] &= \sum_{h=k+2}^{i} N_h[T_h^{k+1}(t - D_u^{k+1}),\ T_h^k(t)] + n_i[T_i^{k+1}(t - D_u^{k+1}),\ T_i^k(t)] \\ &= \sum_{h=k+2}^{i-1} N_h[T_h^{k+1}(t - D_u^{k+1}),\ T_h^k(t)] + n_i[T_i^{k+1}(t - D_u^{k+1}),\ T_i^k(t)] \end{aligned} \quad (66)$$

where (66) is due to the fact that $N_i[T_i^{k+1}(t - D_u^{k+1}),\ T_i^k(t)] = 0$.

From Proposition 10,

$$C_i(T_i^{k+1}(t - D_u^{k+1})) - n_i[T_i^{k+1}(t - D_u^{k+1}),\ T_i^k(t)] \geq C_i(T_i^k(t)). \quad (67)$$

Based on the induction assumption on Statement 2 for $k+1$, we have,

$$I_{k+1}(t - D_u^{k+1}) - N_{k+1}[t - D_u^{k+1},\ t + D_d^k] \geq J_{k+1}^k(t). \quad (68)$$

Similarly for each station $h \in [k+1,\ i-1]$, we have

$$J_h^{k+1}(t - D_u^{k+1}) - N_h[T_h^{k+1}(t - D_u^{k+1}),\ T_h^k(t)] \geq J_h^k(t). \quad (69)$$

Combining (65), (66), (67), (68), and (69), we have

$$RHS \geq \sum_{h=k+1}^{i-1} J_h^k(t) + C_i(T_i^k(t)) \geq 0. \quad (70)$$

Since $RHS \geq 0$, (65) is valid in general. Combining (65) and (70), we have,

$$m_k^s(t) > \sum_{h=k+1}^{i-1} J_h^k(t) + C_i(T_i^k(t)). \quad (71)$$

Combining (57) with (62) and (71), we obtain (56).

Part B2: Show that Statement 2 is true, i.e.,

$$N_k[r_k,\ T_k^i(t_d^i) + 1] = 0.$$

Based on the induction assumption on Statement 2 for each station $h \in [k+1,\ i-1]$, we have,

$$J_h^k(t) \geq J_h^k(r_k) - N_h[T_h^k(r_k),\ T_h^k(t)] \geq 0 \qquad \forall t \in [r_k,\ T_k^i(t_d^i)]. \quad (72)$$

See Figure 6 for the timing.

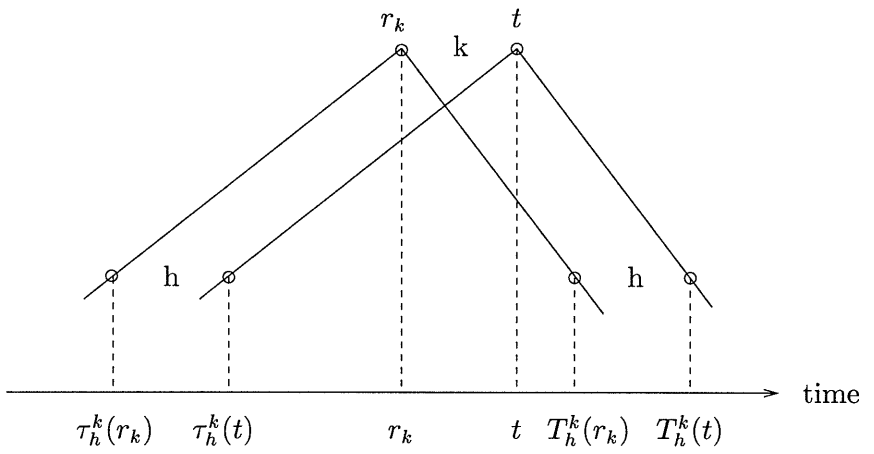

Figure 6: an illustration of the timing

Notice that each of the three parameters in (72) can be either 0 or 1. Thus, to show that the first inequality of (72) is true, we only need to show that,

$$\text{if } J_h^k(r_k) = 1, \text{ and } N_h[T_h^k(r_k),\ T_h^k(t)] = 0, \text{ then } J_h^k(t) = 1. \tag{73}$$

According to the definition, $J_h^k(r_k) = 1$ means that,

$$\begin{aligned} I(\tau_h^k(r_k)) &= 1, \\ N_h[\tau_h^k(r_k),\ T_h^k(r_k)] &= 0. \end{aligned} \tag{74}$$

Combining with the assumption $N_h[T_h^k(r_k),\ T_h^k(t)] = 0$ in (73), we have

$$N_h[\tau_h^k(r_k),\ T_h^k(t)] = N_h[\tau_h^k(r_k),\ T_h^k(r_k)] + N_h[T_h^k(r_k),\ T_h^k(t)] = 0.$$

Since

$$N_h[\tau_h^k(r_k),\ T_h^k(t)] = N_h[\tau_h^k(r_k),\ \tau_h^k(t)] + N_h[\tau_h^k(t),\ T_h^k(t)],$$

we have,

$$N_h[\tau_h^k(r_k),\ \tau_h^k(t)] = 0, \tag{75}$$

$$N_h[\tau_h^k(t),\ T_h^k(t)] = 0. \tag{76}$$

Combining (75) with (74), we have

$$I(\tau_h^k(t)) = 1. \tag{77}$$

According to the definition, (77) with (76) means that $J_h^k(t) = 1$. Therefore, we have shown the first part of

(72).

Again, to show that the second inequality of (72) is true, we only need to show that,

$$\text{if } N_h[T_h^k(r_k),\ T_h^k(t)] = 1,\ \text{then } J_h^k(r_k) = 1. \tag{78}$$

Combining the assumption $N_h[T_h^k(r_k),\ T_h^k(t)] = 1$ in (78) with the fact that,

$$1 \geq N_h[\tau_h^k(r_k),\ T_h^k(t)] = N_h[\tau_h^k(r_k),\ T_h^k(r_k)] + N_h[T_h^k(r_k),\ T_h^k(t)] \geq 0,$$

we have,

$$N_h[\tau_h^k(r_k),\ T_h^k(r_k)] = 0. \tag{79}$$

According to the induction assumption on Statement 2 on h and the assumption $N_h[T_h^k(r_k),\ T_h^k(t)] = 1$ in (78), we have $r_h \geq T_h^k(r_k) \geq \tau_h^k(r_k)$. Thus, according to definition of r_h, $I_h(\tau_h^k(r_k))$ has to be 1. Combining with (79), this means that $J_h^k(r_k) = 1$. Hence, we have shown the second part of (72).

According to the algorithm, station k would not use any idle slot if the counter $C_k(t) > 0$ for all $t \in [r_k,\ T_k^i(t_d^i)]$. Therefore, it is sufficient to prove the following inequality,

$$C_k(t) > \sum_{h=k+1}^{i-1} (J_h^k(r_k) - N_h[T_h^k(r_k),\ T_h^k(t)]) + C_i(T_i^k(t)) \geq 0 \qquad \forall t \in [r_k,\ T_k^i(t_d^i)] \tag{80}$$

where the nonnegativity is based on (72) and Proposition 7.

We prove this by induction on $t = r_k,\ ...,\ T_k^i(t_d^i)$.

1. Let $t = r_k$. Based on the definition (38),

$$C_k(r_k) = M_k^s(r_k) > \sum_{k+1}^{i-1} J_h^k(r_k) + C_i(T_i^k(r_k))$$

   where the second inequality is based on (56) with $t = r_k$. Since the interval $[T_h^k(r_k),\ T_h^k(t))$ is empty in this case, this establishes the basis for (80).

2. Assume (80) is true for a given t, $t \in [r_k,\ T_k^i(t_d^i) - 1]$, we need to prove that it is also true for $t+1$, i.e.,

$$C_k(t+1) > \sum_{h=k+1}^{i-1} (J_h^k(r_k) - N_h[T_h^k(r_k),\ T_h^k(t+1)]) + C_i(T_i^k(t+1)). \tag{81}$$

   Consider the following two cases:

Case one: the slot passing by station $i-1$ at t is not idle, thus,

$$N_h[T_h^k(r_k),\ T_h^k(t)] = N_h[T_h^k(r_k),\ T_h^k(t+1)]. \tag{82}$$

According to the updating equation (8),

$$C_k(t+1) = \min\{C_k(t),\ M_k^s(t+1)\}. \tag{83}$$

Based on the induction assumption on (80) for t,

$$C_k(t) > \sum_{h=k+1}^{i-1} (J_h^k(r_k) - N_h[T_h^k(r_k),\ T_h^k(t)]) + C_i(T_i^k(t)). \tag{84}$$

Combining (84), (82), and the fact that $C_i(T_i^k(t)) \geq C_i(T_i^k(t+1))$ by Proposition 10, we have

$$C_k(t) > \sum_{h=k+1}^{i-1} (J_h^k(r_k) - N_h[T_h^k(r_k),\ T_h^k(t+1)]) + C_i(T_i^k(t+1)). \tag{85}$$

Based on (56) with $t+1$ in place of t,

$$M_k^s(t+1) > \sum_{h=k+1}^{i-1} J_h^k(t+1) + C_i(T_i^k(t+1)). \tag{86}$$

Combining (86) and (72) with $t+1$ in place of t, we have,

$$M_k^s(t+1) > \sum_{h=k+1}^{i-1} (J_h^k(r_k) - N_h[T_h^k(r_k),\ T_h^k(t+1)]) + C_i(T_i^k(t+1)). \tag{87}$$

Combining (83) with (85) and (87), we obtain inequality (81) for case one.

Case two: the slot passing by station k at t is idle. Due to the induction assumption on (80), $C_k(t) > 0$. Thus, the idle slot is propagated downstream. Therefore,

$$C_k(t+1) = \min\{C_k(t) - 1,\ M_k^s(t+1)\}. \tag{88}$$

Based on the induction assumption on Statement 2 for each station $h \in [k+1,\ i-1]$, the idle slot is either taken by one of the station $h \in [k+1,\ i-1]$, which results in that,

$$\sum_{h=k+1}^{i-1} N_h[T_h^k(r_k),\ T_h^k(t)] + 1 = \sum_{h=k+1}^{i-1} N_h[T_h^k(r_k),\ T_h^k(t+1)], \tag{89}$$

$$C_i(T_i^k(t)) - C_i(T_i^k(t+1)) \geq n[T_i^k(t),\ T_i^k(t+1)] = 0; \tag{90}$$

or propagated by station i at $T_i^k(t)$, which results in that,

$$N_h[T_h^k(r_k),\ T_h^k(t)] = N_h[T_h^k(r_k),\ T_h^k(t+1)], \tag{91}$$

$$C_i(T_i^k(t)) - C_i(T_i^k(t+1)) \geq n[T_i^k(t),\ T_i^k(t+1)] = 1 \tag{92}$$

where the inequality is based on Proposition 10.

Combining (84) with (89), (90), (91), and (92), we have,

$$C_k(t) - 1 > \sum_{h=k+1}^{i-1} (J_h^k(r_k) - N_h[T_h^k(r_k),\ T_h^k(t+1)]) + C_i(T_i^k(t+1)). \tag{93}$$

Combining (88) with (93) and (87), we obtain inequality (81) for case two.

Thus, the induction proof on (80) is complete. So is the proof of bounded access delay. ■

Remark. Theorem 3 states that the access delay for the first data segment in queue P_i at station i is upper bounded by $\sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k) + K - 1$, the round trip propagation delay between station i and the most upstream station 1, plus a constant $K-1$, where K is the total number of stations in the network. Another nice property stated by Statement 2 in the proof is that any station k upstream from station i that is active at t_k (the time when the information on P_i arrives at station k) can take at most one idle slot before it propagates the idle slot that is used by data segment P_i. Also for those upstream stations that are idle at t_k, no idle slots are taken by them during this period. In fact,

$$t_d^i - t_a^i \ \leq \ \sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k) + \sum_{k=1}^{i-1} N_k[T_k^1(t_1),\ T_k^i(t_d^i)+1] + n_i[T_i^1(t_1),\ t_d^i+1]. \tag{94}$$

According to Statement 2, for each $k \in [1,\ i-1]$, we have

$$N_k[T_k^1(t_1),\ T_k^i(t_d^i)+1] \leq N_k[t_k,\ T_k^i(t_d^i)+1] \leq I_k(t_k). \tag{95}$$

On the other hand,

$$n_i[T_i^1(t_1),\ t_d^i+1] \leq n_i[t_i,\ t_d^i+1] \leq C_i(t_i) \leq M_i^s(t_i) \leq \sum_{k=i+1}^{K} I_k(t_k) \tag{96}$$

where the last inequality is based on Lemma 4. Combining (94) with (95) and (96), we have

$$t_d^i - t_a^i \ \leq \ \sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k) + \sum_{k=1,\ k\neq i}^{K} I_k(t_k)$$

where $\sum_{k=1,\ k\neq i}^{K} I_k(t_k)$ is bounded by $K-1$.

For any general bus protocol with the full utilization property, any upper bound B_i to the access delay for the first data segment in queue at station i ($i \in [1,\ K]$) is at least as large as the round trip propagation delay, i.e., $B_i \geq \sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k)$. This can be shown through a contradiction argument as below.

Assume the access delay of the first data segment in queue at station i is upper bounded by the round trip propagation delay minus one, i.e.,

$$t_d^i - t_a^i \leq \sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k) - 1. \tag{97}$$

Consider the case where all the stations are idle except station 1 and station i. Station i is idle until t_a^i when data segment P_i arrives at the empty queue. Meanwhile, station 1 has a long queue and uses all the idle slots generated from the head-end except IS_{P_i}, the one used by data segment P_i. In order to satisfy condition (97), idle slot IS_{P_i} must be propagated by station 1 before the information on P_i reaches station 1. In other words, station 1 propagates an idle slot without knowing that any downstream station is active. Now, let's consider another case which is exactly the same as the previous one except that station i is always idle instead. Then the idle slot IS_{P_i} propagated by station 1 is wasted since there is no active downstream station. This is a contradiction to the full utilization property.

For any general bus protocol that is both full utilized and fair, an extra term can added to the lower bound of the maximum access delay. Consider the following scenario. The most upstream station 1 is always active with a long queue. All the other stations $i > 1$ stay idle until $\tau_i^1(t)$ when many data segments arrive at the same time. Based on the full utilization property, station 1 will not propagate idle slots until time t when the information of downstream stations being active first arrives. Therefore, idle slots will not arrive at station $i > 1$ earlier than $T_i^1(t)$, a round trip propagation delay away from $\tau_i^1(t)$. Hence,

$$B_i^{min} \geq \sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k)$$

Notice that starting from t, all the stations are in the set of "very active" stations. According to the definition of "fairness", a round robin cycle starts at $T_i^1(t)$ at each station $i \in [1,\ K]$. Re-number the stations according to their positions in the round robin cycle as $i' = 1,\ ...,\ K$. Then,

$$B_{i'}^{min} \geq \sum_{k=1}^{i'-1}(D_u^{k+1} + D_d^k) + i' - 1 \tag{98}$$

Comparing (98) with the upper bound of the access delay in FUFA protocol $B_i = \sum_{k=1}^{i-1}(D_u^{k+1} + D_d^k) + K - 1$, we can see that with FUFA protocol, the station with $i' = K$ has exactly the minimum possible value of the maximum access delay, while each of the other stations has a maximum access delay that is at most $K - 1$ away from its minimum possible value.

6 Conclusion

In this paper, we have designed and analyzed a fully utilized and fair (FUFA) dual bus protocol to demonstrate some of the fundamental limitations of dual bus networks, in terms of full utilization, fairness and bounded access delay. The basic concept of the protocol is to give equal access to all the stations according to the most updated information available through the reservation bus. In particular, according to the information from downstream and the idle slots propagated previously, each station computes the latest estimate on the number of active downstream stations, and serves them in a round robin scheme. It was shown that FUFA achieves fairness with full utilization. Additionally, the protocol provides a bounded access delay which is linear in the round trip propagation delay, and at most a constant $K-1$ away from its minimum possible value for any bus protocol that is both fully utilized and fair.

This research represents a new direction in the design and study of multiaccess protocols in high-speed-high-latency networks. The following issues warrant further research.

- Simulation results would be useful to analyze both steady state and transient state behaviors.
- The fairness defined here is for steady state behavior. It is desirable to analyze the protocol in transient states, where a protocol is defined to be "fair" if the number of idle slots used by any heavily loaded station during some interval T is at least as large as the number used by any other station, less some constant independent of T.
- Modifications of the protocol to make it more practical should be investigated.

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Appendix A: Timing Issues in A Non-Discrete Time System with Processing Delays

Here, we remove the assumption of zero processing delay and discrete time. When a slot on the data bus arrives at a station, the busy bit is read. If it is 1, meaning that the slot is busy, it stays 1. Otherwise, the

bit is set to 1 if the station decides to use the idle slot according to the algorithm, or stays 0 if the station decides to propagate the idle slot. Then the processed busy bit is written back to the bus, followed by either the old data segment from upstream or a new one from the station, which results in a queue length change at the station. This change of queue length is assumed to take place at the time right after the busy bit leaves the station. The delay parameter D_d^i, $i \in [1,\ K-1]$, used in the algorithm can be defined as the time starting when the busy bit of a slot on the data bus leaves station i and ending when the same busy bit leaves station $i+1$. Denote $D_{c_d}^i \geq 0$ as the delay between reading and writing the busy bit as a slot passes by station i. It is easy to see that this delay is equivalent of having slots going through an extra loop around the station which generates the same amount of delay. Denote $D_{g_d}^i \geq 0$ as the propagation delay downstream from i. Then,

$$D_d^i = D_{g_d}^i + D_{c_d}^i. \tag{99}$$

In practice, there are cases where the busy bit is placed a few slots ahead of the slot that it indicates. For example, data segments are not stored in the queue, and it takes time to get them ready to be sent. Still, the decision has to be made after the busy bit is read by a station according to the information available at the time. Then the queue length has to be changed accordingly when the busy bit is written. Since all the decisions are based on the busy bits, delaying the data segments by k slots changes nothing in the algorithm and simply increases the overall delay by k slots.

To analyze the other delay parameter D_u^i, $i \in [2,\ K]$, recall from the algorithm that the information $m_{i-1}(t+D_u^i)$ is generated as follows,

$$\begin{aligned} m_{i-1}(t+D_u^i) &= Q_{i-1}(t+D_u^i) + m_{i-1}^s(t+D_u^i) \\ &= Q_{i-1}(t+D_u^i) + [m_i(t) - n_{i-1}(t+D_u^i)]^+ \\ &= Q_{i-1}(t+D_u^i) + [Q_i(t) + m_i^s(t) - n_i(t+D_u^i)]^+ \end{aligned}$$

Notice that information $m_{i-1}(t+D_u^i)$ takes into consideration of both the queue length of station $i-1$ at $t+D_u^i$ and the queue length of station i at t, and D_u^i is the difference between the two time instances. D_u^i consists of the following three parts of delay,

$$D_u^i = D_{c_u 1}^i + D_{g_u}^i + D_{c_u 2}^i, \tag{100}$$

where

- $D_{c_u 1} \geq 0$ is the time from t when the busy bit of a slot on data bus leaves station i till the time when the combined information $m_i(t)$ leaves station i with a slot on the reservation bus. Note that $m_i(t)$ is obtained by combining $Q_i(t)$, the queue length of station i right before t, with $m_i^s(t)$, the most recent updated information available up to t,

- $D^i_{g_u} \geq 0$ is the propagation delay from station i to the upstream station $i-1$,
- $D_{c_u 2} \geq 0$ is the time starting when the information $m_i(t)$ arrives at station $i-1$ ending right before the busy bit of the next slot on the data bus leaves station $i-1$, which is also the time that the updated information $m^s_{i-1}(t+D^i_u)$ starts being combined with $Q_{i-1}(t+D^i_u)$. Thus, this later time instance is $t+D^i_u$.

Note that slots on the data bus and the reservation bus can arrive at or leave a station at different time.

In the algorithm, station i uses $n_i(t)$, which includes the the most recent slot propagated at $t-1$, to make decision on the slot passing by at t. This is essential to guarantee the full utilization property. Denote $S_i(s)$ as the slot with its busy bit leaving station i at time s. At time $t-1$ when the busy bit of slot $S_i(t-1)$ leaves station i, the information $n_i(t)$ becomes available. Then the decision on slot $S_i(t)$ has to be made before t when the busy bit of slot $S_i(t)$ leaves the station.

Appendix B: Overhead

In this section, we study how much overhead is needed for FUFA protocol to be implemented. We want to remind readers that the purpose of this paper is not to introduce a protocol to be used in practice, but rather to provide a machinery to illustrate some principles in dual bus networks.

According to the algorithm, a busy bit is needed in every slot of the data bus. It is 0 if the slot is idle, 1 otherwise. In the reservation bus, two parameters, $M_i(t)$ and $m_i(t)$, $i \in [2,\ K]$ are carried in every slot. We want to find out how many bits are needed to represent $M_i(t)$ and $m_i(t)$ individually.

Since $M_i(t)$ is upper bounded by $K-1$, total $\lceil log_2(K-1) \rceil$ bits are needed for $M_i(t)$.

As for $m_i(t)$, according to Lemma 1, $m_i(t) = Q_i(t) + m^s_i(t) \leq \sum_{k=i}^{K} Q_k(T^i_k(t))$. Since the queue length of station i can not be greater than the buffer size of the station, denoted as BS_i, $m_i(t) \leq \sum_{k=i}^{K} BS_k \triangleq BS^i \leq BS^2$, where BS^2 is the sum of the buffer sizes of all stations except station 1. Hence, total $\lceil log_2 BS^2 \rceil$ bits are needed for $m_i(t)$.

Next, we present a method that provides a possible better upper bound for $m_i(t)$. As we can see, the decision making at station k at time t in the algorithm is controlled by the round robin counter $C_k(t)$, thus by $M^s_k(t)$. Therefore, we want to find the least upper bound for $m_i(t)$, denoted as $m^{UB}_i(t)$, such that $M^s_k(t)$ is not affected for all $k \in [1,\ K-1]$. Based on the algorithm and Proposition 5,

$$m^s_{i-1}(t+D^i_u) = [m_i(t) - n_{i-1}(t+D^i_u)]^+ \geq M^s_{i-1}(t+D^i_u).$$

Therefore,

$$m^{UB}_i(t) \geq \max M^s_{i-1}(t+D^i_u) + \max n_{i-1}(t+D^i_u) = K - i + 1 + D^i_u + D^{i-1}_d. \tag{101}$$

On the other hand,

$$m_i(t) = Q_i(t) + m_i^s(t) = Q_i(t) + [m_{i+1}(t - D_u^{i+1}) - n_i(t)]^+$$

Then,

$$m_{i+1}^{UB}(t - D_u^{i+1}) \geq m_i^{UB}(t) + \max n_i(t) - \min Q_i(t) = m_i^{UB}(t) + D_u^{i+1} + D_d^i. \tag{102}$$

Combining (101) and (102), for $i \in [2,\ K]$, we have

$$m_i^{UB}(t) \leq K - 1 + \sum_{k=2}^{i}(D_u^k + D_d^{k-1}). \tag{103}$$

This implies that, at most $\lceil K - 1 + \sum_{k=2}^{K}(D_u^k + D_d^{k-1})\rceil$ bits are needed for $m_i(t)$, where $\sum_{k=2}^{K}(D_u^k + D_d^{k-1})$ is the round trip delay between station 1 and station K.