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LINEAR AVERAGED AND SAMPLED DATA MODELS FOR LARGE SIGNAL CONTROL OF HIGH POWER FACTOR AC-DC CONVERTERS

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Abstract

This paper shows that the *large* signal behavior of a popular family of high power factor ac to dc power conditioners can be analyzed via *linear* models, by using *squared* output voltage as the state variable. The state equation for a general (constant power plus resistive) load is obtained by a simple dynamic power balance. Time invariant or periodically varying controllers, acting at the time scales of the line or switching periods respectively, can then be designed from the resulting averaged or sampled data models. Simulations and experiments corroborate the results.

1. Introduction

Recently, there has been much work on designing control schemes for high power factor ac to dc converters. Schlecht [1]-[3] discusses various topologies and control schemes for such converters. Subsequent work has largely focused on the scheme shown in Fig.1, using a boost converter whose input voltage $v_{in}(t)$ is the rectified ac waveform. The inner current loop specifies the switching sequence for the transistor to regulate the input current $i_{in}(t)$ around a reference $i_{cmd}(t)$ that is proportional to the input voltage. The outer voltage loop varies the proportionality constant k from cycle to cycle, to regulate the output voltage $v_o(t)$ about the desired level, V_d.

Several recent papers discuss different approaches to designing the inner and outer loops. Henze and Mohan [4] use a hysteretic current control loop, and implement the voltage control loop digitally, using a simple PI (proportional-integral) controller, but some modeling aspects are left unclear. Williams [5] designs a controller using the small signal 'transfer function' between commanded input current and output voltage. While his analysis contains insight into the operation of the circuit, it is mathematically incorrect since it is based on Laplace transform operations on equations with time varying coefficients, even though the conditions for quasistatic analysis do not hold. A correct small signal averaged model and associated control design are provided by Ridley [6].

The present paper develops *large* signal *linear* models for the voltage loop. Specifically, we develop continuous time averaged models at the time scales of the switching period and the input period, and also derive their sampled data counterparts. These models yield efficient simulations, and enable the simple design of control schemes that permit recovery from large perturbations away from the operating point. Section 2 describes the operation of the inner current loop shown in Fig. 1. Section 3 presents continuous time averaged and sampled data models for the dynamics of the outer voltage control loop. The continuous time averaged models are verified in Section 4 by comparison with both the results of SPICE implementations of the models and experimental results for an actual ac-dc converter. Section 5 discusses the use of a sampled data model to design a digital controller for the outer loop, including PI control, and presents simulation results for the behavior of the full closed loop system.

2. Current Loop Operation

The current loop is responsible for obtaining the high power factor by drawing a resistive current from the ac line. Any current mode control scheme may be used. The operation of one such scheme is illustrated by the simulation in Fig. 2. At the beginning of every switching period, every T_S seconds, a decision is made to have the transistor on or off, as required to force the inductor current towards the switching boundary, $i_{cmd}(t)$. This is a compromise between the usual constant frequency discipline and hysteresis band control. It provides a natural control implementation, given that the control is exercised periodically, and was shown in [7] to be effective in digital sliding mode control of the buck-boost converter. The commanded input current, $i_{cmd}(t)$, is set according to:

$$i_{cmd}(t) = k(t)v_{in}(t) \qquad (1)$$

where $k(t)$ is determined by the voltage control loop. In usual practice, $k(t)$ is held constant (or approximately

constant) for the duration of the rectified input's period, T_L.

For the simulation in Fig. 2, we have assumed a constant power load, P and chosen parameter values as follows:

$$L = 600\mu H \qquad C = 940\mu F \qquad P = 1100W$$
$$T_S = 10\mu sec \qquad v_{in}(t) = V|sin(120\pi t)| \qquad V = 200volts$$

The value of $k(t)$ in Fig. 2 equals 0.055. The power factor during this line cycle is calculated to be 0.977.

The running average, $i(t)$, of the input current over an interval T_S is defined by $i(t) = \frac{1}{T_S}\int_{t-T_S}^{t} i_{in}(\sigma)d\sigma$. It is reasonable to assume, when the current loop is working well, that $i(t) = i_{cmd}(t) = k(t)v_{in}(t)$. This will be a standing assumption in what follows.

3. Voltage Loop Dynamics

In this section, we obtain dynamic models for the outer control loop. We assume the load comprises a parallel combination of a constant power load P and a resistor R.

Continuous Time T_S-Averaged Model

Ignoring *switching* frequency ripple in the output voltage, $v_o(t)$, and assuming that the inner current loop maintains $i(t) = k(t)v_{in}(t)$, conservation of power for the boost converter yields:

$$\frac{1}{2}Cd[v_o^2(t)]/dt = k(t)v_{in}^2(t) - \frac{1}{2}Ld[k^2(t)v_{in}^2(t)]/dt - P - \frac{1}{R}v_o^2(t) \qquad (2)$$

This already shows that the use of $v_o^2(t)$ as the state variable, instead of the more common $v_o(t)$, leads to an essentially *linear* first-order model for *large* signal behavior. This observation has also been made by Sanders [8].

The model (2) corresponds, in effect, to averaging a switched model over the switching period, and we shall refer to it as the "T_S-averaged" model. Other averaged and sampled data models (SDM's) can be obtained from (2). If $v_o(t)$ is taken as the state variable, (2) is a nonlinear description; linearization yields a small signal periodically varying model, which is the starting point for Williams' discussion of control possibilities [5].

Continuous Time T_L-Averaged Models

To obtain an averaged model on the time scale of the *input* period, average (2) over T_L, using the running average defined by $\bar{w}(t) = \frac{1}{T_L}\int_{t-T_L}^{t} w(\sigma)d\sigma$. Denote $\bar{v}_o^2$ by y. If the input frequency ripple in $v_o(t)$ is small, then $y \approx \bar{v}_o{}^2$. Assuming that $k(t)$ varies slowly enough to be considered constant over any interval of length T_L, the resulting "T_L-averaged" model is given by the linear first-order description

$$dy(t)/dt = -\frac{2}{RC}y(t) + \frac{1}{C}(V^2k(t) - 2P) \qquad (3)$$

The block diagram in Fig. 3(a) shows the transfer function representation of (3). Notice that the term involving $k^2(t)$ in (2) has disappeared, because our assumption of slowly varying $k(t)$ causes the average value of $d[k^2(t)v_{in}^2]/dt$ to be negligible. Even if $k(t)$ is not slowly varying and this average is not negligible, it is often true that the term $Ld[k^2(t)v_{in}^2]/dt$ contributes little to the power balance in (2), because L is small. The model (3) already suffices to design linear controllers (e.g. PI controllers) for *large* deviations in $y(t)$ or $\bar{v}_o$.

To exploit the linear model above, the linear controller needs to operate on the *squared* output voltage. Otherwise a linear controller that acts on $\bar{v}_o$ itself can be designed on the basis of a small-signal linearization of (3), as in Ridley [6] and Williams [5], but then good control is only guaranteed for small perturbations of $\bar{v}_o$ from its desired nominal value, V_d. The linearized model is easily derived from (3) and is shown in Fig. 3(b). The tildes ($\sim$) denote perturbations from nominal. We have not represented the effects of perturbations in the line voltage amplitude V, since these are normally compensated for by a feedforward that makes k proportional to $1/V^2$.

Sampled Data Models

To maintain sinusoidal waveforms in each input cycle, we must keep $k(t)$ constant over each cycle. Under this condition, it is natural to look for sampled data models and controllers. To obtain an SDM on the time scale of the input period T_L, we can integrate (2) or (3) over T_L, assuming that $k(t)$ is essentially constant over intervals of length T_L. The "T_L-SDM" that results from (3) under the assumption that $RC >> T_L$ is shown below, with $k(t)$ in the n^{th} cycle denoted by $k[n]$ and $y(t)$ at the beginning of the n^{th} cycle by $y[n]$:

$$y[n+1] = \left(1 - \frac{2T_L}{RC}\right)y[n] + \frac{T_L}{C}(V^2k[n] - 2P) \qquad (4)$$

Hence, assuming that the inner control loop successfully maintains $i(t)$ at its commanded value $i_{cmd}(t)$, the dynamics of the boost converter is completely described by the single linear, time invariant difference equation (4), with state $y[n]$ and control $k[n]$. If the input frequency ripple in $v_o(t)$ is small, then $y[n] \approx v_o^2[n]$, the squared output voltage at the beginning of the n^{th} cycle. If $v_o[n]$, rather than $v_o^2[n]$, is taken as the variable to be modeled, we obtain a nonlinear model. Its linearization is a small signal time invariant model that turns out to be the same

as what Williams [5] obtains through heuristic and not very satisfying arguments.

The regulation of v_o about V_d can be accomplished by regulating v_o^2 about V_d^2, as we show in Section 5. For our purposes there, it is useful to develop an alternative model, using the state variable $x[n]$ defined by

$$x[n] = v_o^2[n] - V_d^2 \tag{5}$$

Combining (4) and (5) yields

$$x[n+1] = \left(1 - \frac{2T_L}{RC}\right) x[n] + \frac{V^2 T_L}{C} k[n] - \frac{2T_L}{C}\left(P + \frac{V_d^2}{R}\right) \tag{6}$$

Note that $x[n]$ is *not* restricted to be small.

An SDM at the time scale of the switching period is derived in a similar manner, by integrating (2) over the switching period T_S. Assuming that $k(t)$ is constant over T_S, and that $RC >> T_S$, we get the "T_S-SDM" shown below. The time index η denotes the switching period, whereas the time index n in the T_L-SDM denotes the input period

$$x[\eta+1] = x[\eta] + b_1[\eta]k[\eta] + b_2[\eta]k^2[\eta] - \frac{2PT_S}{C} \tag{7}$$

where the time varying input gains are given by:

$$b_1[\eta] = \frac{V^2}{C} T_S - \frac{V^2}{C}\left\{\frac{T_L}{2\pi}[\sin(2\pi(\eta+1)T_S/T_L) - \sin(2\pi\eta T_S/T_L)]\right\} \tag{8}$$

$$b_2[\eta] = \frac{V^2 L}{C}\left\{\sin^2(\pi(\eta+1)T_S/T_L) - \sin^2(\pi\eta T_S/T_L)\right\}$$

Note that in steady state, the T_L-SDM satisfies $x[n+1] = x[n]$. However, the T_S-SDM has a cyclic steady state and does *not* satisfy $x[\eta+1] = x[\eta]$.

4. Model Verification

In this section we compare the continuous time averaged models (2) and (3) with each other and with experimental data from a test circuit.

The test circuit uses a Micro Linear ML 4812 power factor controller chip to implement the control functions shown in Fig. 1. The parameters of the test circuit are

$$L = 1mH \qquad C = 410\mu F \qquad V = \sqrt{2} \times 120volts$$

The load is a square-wave current source switching between 0.2A and 0.4A at a frequency of 0.5Hz. The output voltage is to be regulated at $V_d = 386$volts.

Using the models we have developed, it is quite straightforward to design a good PI compensator for this circuit, using either $v_o^2(t)$ or $v_o(t)$ as the feedback signal. The particular test results shown in Fig. 4, however, correspond to using only integral compensation, with $\tilde{k} = -.076 \int \tilde{v}_o dt$. Integral control contributes nothing to the damping of transients here, and is a very poor control choice in this case, even though it provides insensitivity to constant disturbances (such as load uncertainties). However, the large oscillatory transients that result allow us to make a clearer comparison with the predictions of our models than would have been possible with the small transients produced by good PI compensation.

Our linear averaged models (2) and (3) were derived assuming a load comprising a constant power component P in parallel with a resistor R. The models can easily be extended to handle a current source load, as in the test circuit, but then would no longer be linear. This is because a constant current load I_o contributes the term $-I_o v_o(t)$ to the right side of the power balance equation (2), and this term involves $\sqrt{v_o^2(t)}$ rather than $v_o^2(t)$. For the transients in Fig. 4, however, $v_o^2(t)$ does not deviate excessively from V_d^2, so not much error would be incurred if we replaced $-I_o\sqrt{v_o^2(t)}$ by its linearization at $v_o^2(t) = V_d^2$:

$$-I_o\sqrt{v_o^2(t)} \approx -I_o V_d - \frac{I_o}{2V_d}(v_o^2(t) - V_d^2) = -\frac{I_o V_d}{2} - \frac{I_o}{2V_d} v_o^2(t) \tag{9}$$

The current source therefore behaves, to a first order approximation, as the parallel combination of a constant power load $I_o V_d/2$ and a resistor $2V_d/I_o$.

Linearity of the model is not as important for simulation as for control design, so for the simulations in Figs. 5 and 6 we have used the nonlinear extensions of (2) and (3) that incorporate the current source load. However, no significant differences are expected if the substitution in (9) is used instead, with a linear model. The results in Figs. 5 and 6 were obtained using SPICE implementations of the (extended) models; their listings are given in the Appendix. The output voltage $v_o(t)$ is fed back, in both cases, through the same integral compensator used for the test circuit.

The match between the responses of the T_S-averaged model in Fig. 5 and the T_L-averaged model in Fig. 6 is excellent. Unlike Fig. 2, neither of these simulations represents the details of the switching frequency ripple, so they are very efficient to run. The T_L-averaged model does not model the input frequency ripple either, so the corresponding simulation can take larger time steps than the T_S-averaged model, for the same accuracy. The damping and oscillation frequency are what we would expect from (3) for a resistive load of value

$R = 2V_d/I_o = 3.86K\Omega$. For this load, the decay time constant for $v_o(t)$ under integral compensation is computed to be 0.63 sec, and the oscillation period is 75.5 ms, which are consistent with Figs. 5 and 6.

The frequency of the oscillatory transients in Figs. 5 and 6 matches that of the test circuit transient in Fig. 4, but the damping is larger for the test circuit. This is probably the result of losses in the test circuit that have not been modeled.

5. Control Design

The design of an analog control (e.g. PI control) for the model (3) or its linearization is routine. For example, it is not hard to see that the PI control law $\tilde{k} = -.013[0.1\tilde{v}_o + \int \tilde{v}_o dt]$ will perform much better than pure integral control on the circuit in Section 4. The response to the same square-wave current source load as before is shown in the T_L-averaged simulation in Fig. 7. Since analog control design is relatively familiar, we do not discuss it further here. Instead, we now illustrate the design of digital control schemes, using the T_L-SDM in (6) with a constant power load and the parameter values in Section 2. The controllers will feed back and regulate v_o^2 rather than v_o. In steady state, $x[n+1] = x[n] = 0$, so the constant control $k[n] = K$ required to maintain equilibrium in steady state is seen from (6) to be:

$$K = 2P/V^2 \tag{10}$$

which varies as $1/V^2$. However, we only know the nominal load power P_N and the actual power is $P = P_N + \tilde{P}$. Consequently, let $K = 2P_N/V^2$. Rewriting the control as $k[n] = K + \tilde{k}[n]$ reduces the state equation (6) to:

$$x[n+1] = x[n] + \frac{V^2 T_L}{C}\tilde{k}[n] - (\frac{2T_L}{C})\tilde{P} \tag{11}$$

State Feedback

Specifying the control to be in state feedback form,

$$\tilde{k}[n] = -\left(\frac{Cb}{V^2 T_L}\right) x[n] \tag{12}$$

yields the closed loop model

$$x[n+1] = (1-b)x[n] - \left(\frac{2T_L}{C}\right)\tilde{P} \tag{13}$$

Note that $\tilde{k}[n]$ is inversely proportional to V^2. The solution for $x[n]$ is given by the standard variation of constants formula in discrete time:

$$x[n] = (1-b)^n x[0] + \left[\sum_{l=0}^{n-1}(1-b)^{n-l-1}\right]\left(\frac{2T_L}{C}\right)\tilde{P} \tag{14}$$

The constant b is chosen to place the pole $z_p = 1 - b$ at a desired location.

Placing the pole at $z_p = 1/2$ and initiating the output voltage with a 50% initial perturbation away from equilibrium results in the sampled output voltage transient shown in Fig. 8 for the model (13). The output voltage starts at $v_o = 173$ volts and requires approximately 8 input periods to attain the desired level of $V_d = 346$ volts. The corresponding control signal $\tilde{k}[n]$ is also shown.

Before connecting the voltage loop to the current loop, the range of values of $k[n]$ specified by the voltage loop must be checked for consistency with the range allowed by the current loop. If $k[n]$ is too large, then the inductor current will be unable to rise fast enough to follow the commanded current $i_{cmd}(t) = k(t)v_{in}(t)$. In this example $k[n] = K = .055$ results in the current response shown in Fig. 2. Further simulations demonstrate that for $k[n] < .5$, the input current is able to follow its commanded value $i_{cmd}(t)$. Consequently, for $k[n]$ in the vicinity of K the full closed loop system will perform as expected. In particular, for the transient in Fig. 8, the current loop will perform as desired.

Figure 9 shows a detailed simulation of the response of the full closed loop system to an initial 50% perturbation away from the desired output voltage level, $V_d = 346$ volts. As predicted by the sampled data voltage loop simulation in Fig. 8, the transient has decayed in about 8 input periods. In Fig. 9, each input period T_L is approximately equal to 830 switching periods T_S. The power factor corresponding to each cycle of the current response in Fig. 9 is shown in Fig. 10. The power factor in steady state is close to the power factor of the open loop response in Fig. 2.

Figure 11 illustrates the response of the full closed loop system to an unanticipated step change in output power at $t = 2000$. At that time, $\tilde{P}$ is stepped from 0 to $\frac{1}{2}P_N$, so that the power in the load steps by 50% from 1100 watts to 1650 watts. The output voltage attains a new cyclic steady state, but exhibits a dc offset of approximately 30 volts, or 9%.

State Feedback with Integral Control

In order to correct for the effect of such uncertainties in the load power, integral control must be incorporated into the voltage loop control scheme, as shown in Fig. 12. The state equations for the outer loop are given by:

$$q[n+1] = q[n] + x[n] \tag{15}$$

$$x[n+1] = -b_I q[n] + (1-b_P)x[n] - (\frac{2T_L}{C})\tilde{P} \tag{16}$$

The pole locations of this system are given by:

$$z_p = (1 - b_P/2) \pm \sqrt{(b_P/2)^2 - b_I} \tag{17}$$

Selecting the "best" b_P and b_I is complicated by the limitations on the control $k[n]$ noted earlier. For the purpose of demonstrating the performance of the outer loop with integral control, the poles will be placed at $z_p = \frac{1}{2}, \frac{1}{2}$. This choice results in a small enough $k[n]$ and a reasonably fast response. The response of the preceding second order sampled data model for the voltage loop, after a 50% perturbation in output voltage, is shown in Fig. 13. It has approximately the same settling time and a slightly greater overshoot than the first order voltage loop response in Fig. 8.

The response of the full closed loop system with integral control to a 50% initial perturbation in output voltage is shown in Fig. 14 and is consistent with the sampled data outer loop response in Fig. 13. The output voltage reaches its desired level of 346 volts in approximately 8 line periods with a peak overshoot of about 40 volts. The response to a 50% step change in load power at $t = 2000$ is shown in Fig. 15. With integral control, the output now recovers and requires a settling time of only 8 line periods.

6. Conclusions

The models we have developed suggest that there might be value in feeding back and regulating the *squared* output voltage of high power factor ac-dc converters. This would permit *linear* controllers to handle *large* perturbations in the output voltage, as demonstrated in Section 5. The required control functions would compare in style and complexity with what is presently available on single-chip controllers. It may also be of interest in future work to study the use of periodic controllers [2], using the models (2), (7) or (8).

Apart from suggesting new control possibilities, our development clarifies the relationships among different modeling and simulation approaches for such converters.

Acknowledgment

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References

[1] M.F. Schlecht, "A Line Interfaced Inverter with Active Control of The Output Current Waveform", PESC, 1980, pp.234-241.

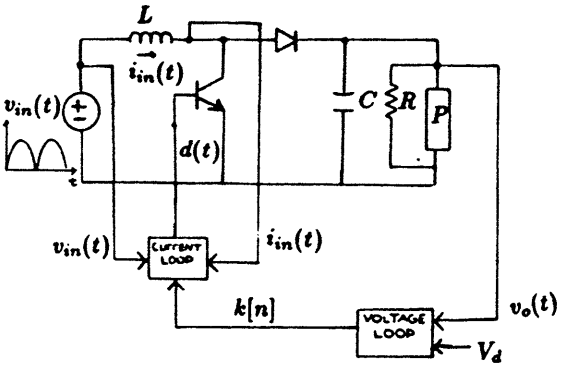

Figure 1: Boost Converter with Current and Voltage Control Loops

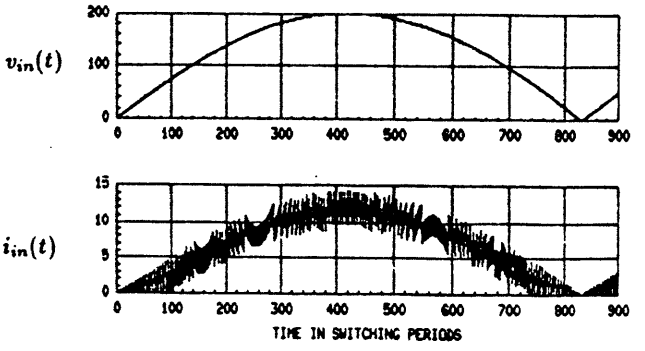

Figure 2: Current Loop

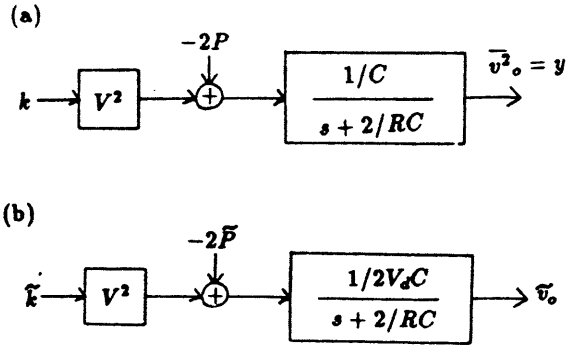

Figure 3: Transfer Function Representation of T_L-Averaged Model (a) Large Signal (b) Small Signal

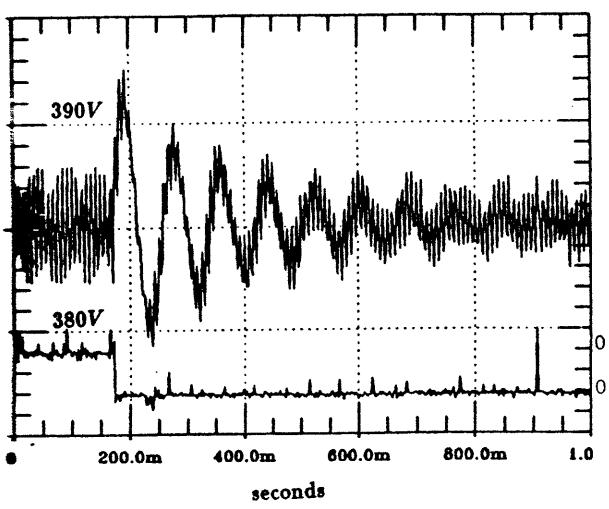

Figure 4: Transient Response of Test Circuit with Integral Control

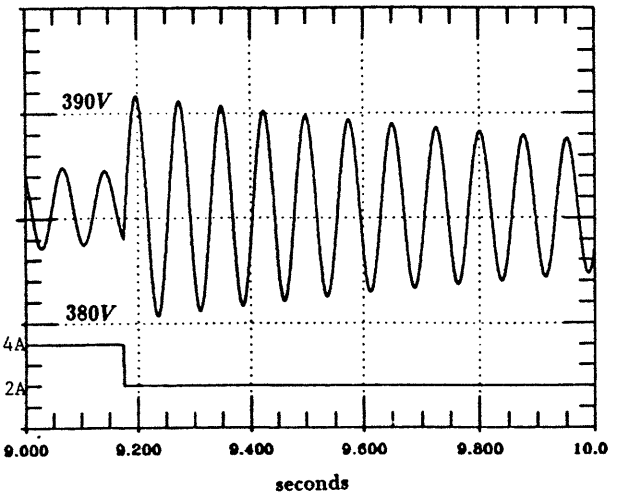

Figure 6: SPICE Simulation of Transient in T_L-Averaged Model

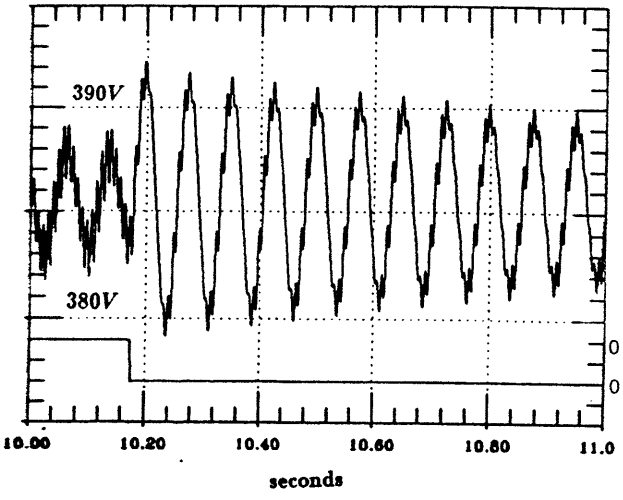

Figure 5: SPICE Simulation of Transient in T_S-Averaged Model

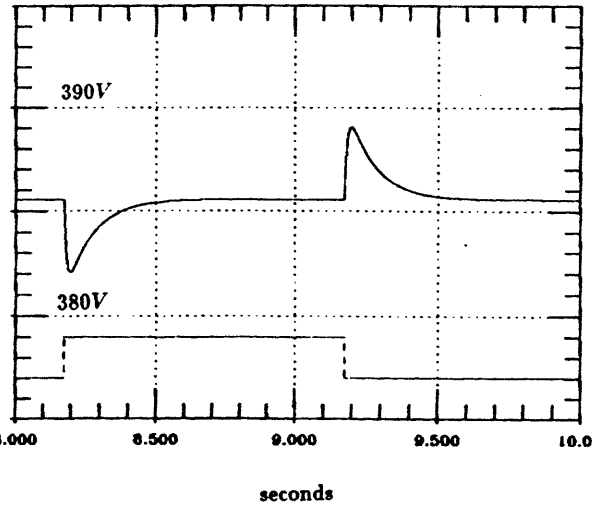

Figure 7: SPICE Simulation of Transient in T_L-Averaged Model with PI Control

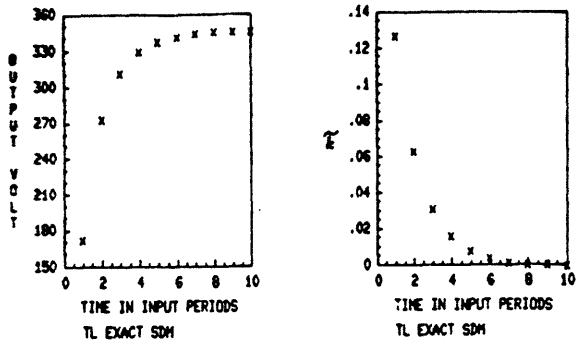

Figure 8: Sampled Voltage Loop Response to Initial Perturbation

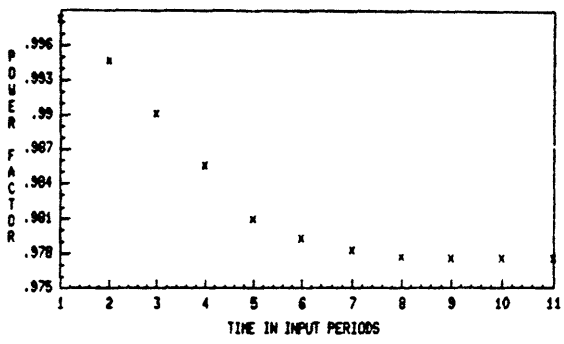

Figure 10: Power Factor

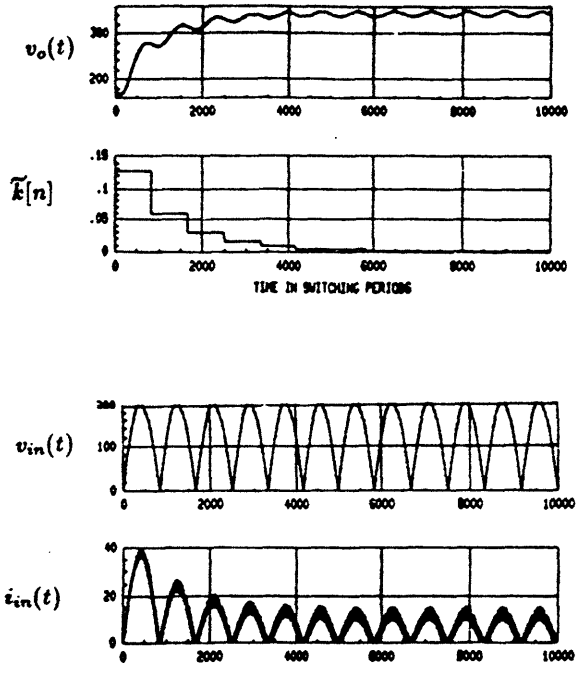

Figure 9: Response of Full Closed Loop System to Initial Perturbation

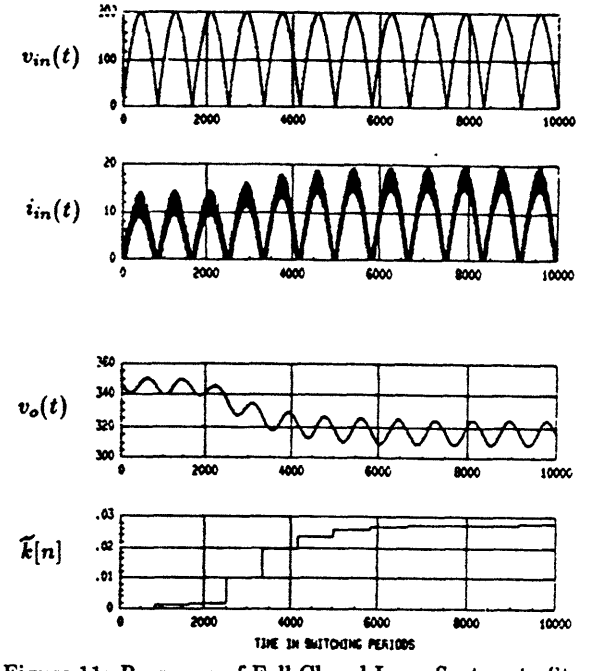

Figure 11: Response of Full Closed Loop System to Step Change in Constant Power Load

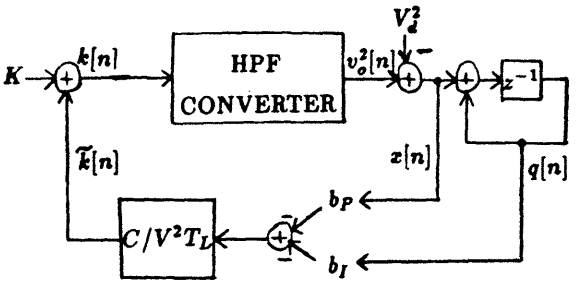

Figure 12: Voltage Loop with Integral Control

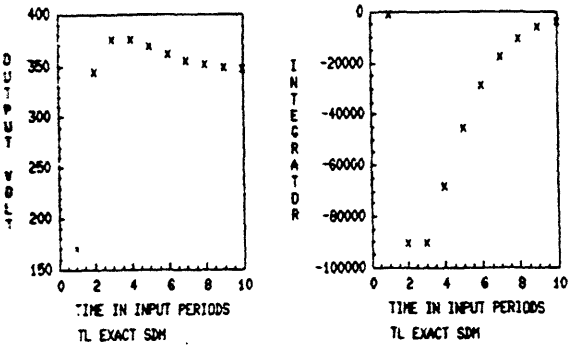

Figure 13: Sampled Voltage Loop Response with Integral Control

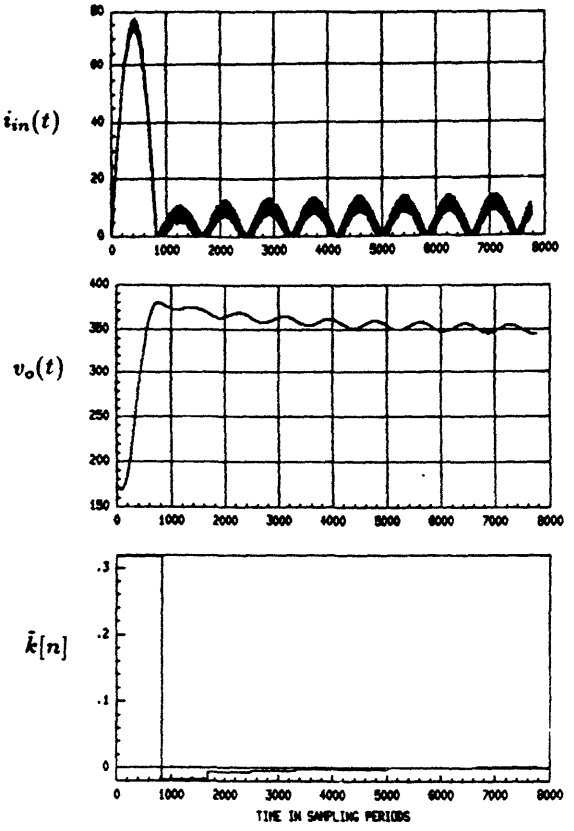

Figure 14: Response of Full Closed Loop System with Integral Control to Initial Perturbation

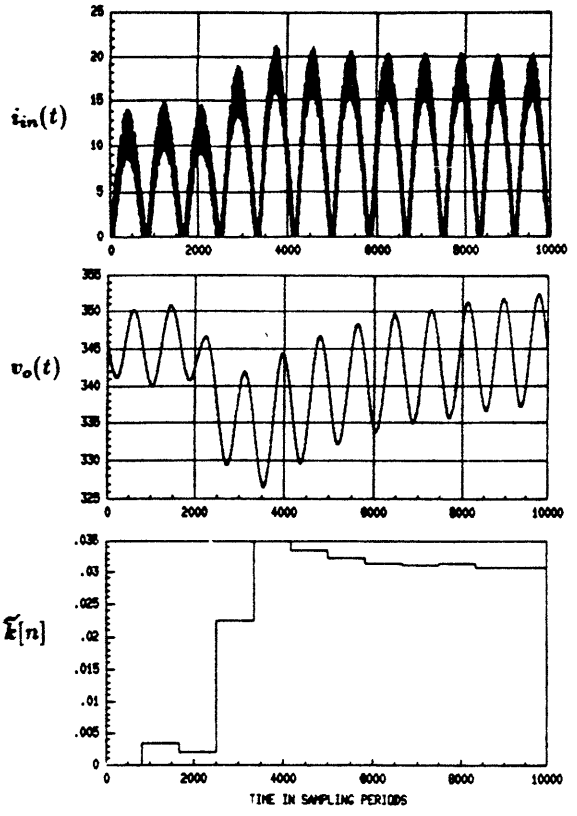

Figure 15: Response of Full Closed Loop System with Integral Control to Step Change in Load

[2] M.F. Schlecht, "Time-Varying Feedback Gains for Power Circuits with Active Waveshaping", PESC, 1981, pp.52-59.

[3] M.F. Schlecht, "Novel Topological Alternatives to the Design of a Harmonic-Free Utility/DC Interface", PESC, 1983, pp.206-216.

[4] C.P. Henze and N. Mohan, "A Digitally Controlled AC to DC Power Conditioner that Draws Sinusoidal Input Current", PESC, 1986, pp 531-540.

[5] J.B. Williams, "Design of Feedback Loop in Unity Power Factor AC to DC Converter", PESC, 1989, pp.959-967.

[6] R.B. Ridley, "Average Small-Signal Analysis of the Boost Power Factor Correction Circuit", VPEC Seminar, 1989, pp.108-120

[7] S.R. Sanders, G.C. Verghese, and D.F. Cameron, "Nonlinear Control Laws for Switching Power Converters", 25th IEEE Conference on Decision and Control, Athens, December, 1986, also in Control-Theory and Advanced Technology, 5, pp.601-627, Dec. 1989.

[8] S.R. Sanders, "Effects of Nonzero Input Source Impedance on Closed-Loop Stability of a Unity Power Factor Converter", PCIM-Power Conversion, Los Angeles, Oct. 1989.

APPENDIX

SPICE Input Listing of T_S-averaged Model

```
TS-AVERAGED MODEL FOR HPF POWER STAGE
* Simulation of Microlinear test circuit (with modified
* values) - constant current load
VINAC 5 6 SIN 0.  170.  60.
D1 5 1 DS
D2 0 5 DS
D3 6 1 DS
D4 0 6 DS
RIN 1 0 1G
* vIN**2
EVIN2 10 0 poly(1) 1 0 0.  0.  1.
REVIN2 10 0 1G
* k*vIN**2
GKVIN2 0 21 POLY(2) 10 0 2 0 0.  0.  0.  0.  1.
* I**2
EI2 12 0 POLY(1) 2 0 0.  0.  1.
REI2 12 0 1G
* (K**2)(VIN**2)
GK2VIN2 0 13 POLY(2) 12 0 10 0 0.  0.  0.  0.  1.
L 13 0 1M
GK2DVIN2 21 0 13 0 0.5
* For constant-current load, use vccs, with gain = I
GILOAD 21 0 poly(2) 40 0 30 0 0.  0.  0.  0.  1.
VILOAD 30 0 PULSE 0.2 0.4 3.175 100U 100U 1.  2.
RVILOAD 30 0 1K
VSENSE 21 0 DC 0.
FDVO2 0 25 VSENSE 2.
RDUM1 25 0 1G
C 25 0 410U IC=148.225K
* Square root of v0**2
EFWD 40 0 POLY(2) 25 0 41 0 0.  1MEG -1MEG
RFWD 40 0 1MEG
EREV 41 0 POLY(2) 40 0 40 0 0.  0.  0.  0.  1.
RREV 41 0 1MEG
* Output feedback
EOUT 44 0 40 0 1.
R1 44 50 360K
R2 50 0 4.73K
CF 50 52 0.47UF IC=4.91
X1 51 50 0 52 53 0 ML4812EA
VREF 51 0 DC 5.0
VPOS 53 0 DC 6.0
* Gain of EK is
* [multiplier gain * Rmult]/[Rsine * (N1/N2) * Rsense]
* where, Rmult = termination resistor for multiplier,
* Rsine = resistance used to derive current reference
* from line, N1/N2 = current transformer primary to
* secondary turns ratio, and
* Rsense = current-transformer burden resistor
EK 2 0 52 0 0.0129
REK 2 0 1G
* k*vIN (to get input current waveform)
EKVIN 60 0 poly(2) 2 0 1 0 0.  0.  0.  0.  1.
REKVIN 60 0 1G
.SUBCKT ML4812EA 1 2 3 4 5 6
* 1 is non-inverting input, 2 is inverting input,
* 3 is ground, 4 is output, 5 is +VCC, 6 is -VCC
* Input stage
RIN 1 2 150MEG
* Gain, slew rate limiting and dominant pole stage
* open-loop gain is 90 dB (31622), dominant pole
* is 30 Hz [C1 = 1/(w*R1)] GVI 3 8 1 2 1.
C1 8 3 167.8NF
R1 8 3 31.62K
* output clamping
VLOW 11 6 DC 0.01
DLOW 11 8 DS
VHIGH 5 12 DC 1.0
DHIGH 8 12 DS
* Unity gain and output stage
E1 10 3 8 3 1.
RO 10 4 150
.MODEL DS D(N=1U)
.ENDS ML4812EA
.MODEL DS D(N=1U)
.TRAN 250U 11.3 10.0 250U UIC
.OPTIONS NUMDGT=8, ITL5=0, ITL4=10000
.PRINT TRAN V(40) V(1) V(30) V(2) V(25) V(52) V(50,52)
.END
```

SPICE Input Listing of T_L-averaged Model

```
TL-AVERAGED MODEL FOR HPF POWER STAGE
* Simulation of Microlinear test circuit (with modified
* values) - constant-current load
VIN 1 0 DC 120
RIN 1 0 1G
* vIN**2 (rms value)
EVIN2 10 0 poly(1) 1 0 0.  0.  1.
REVIN2 10 0 1G
* k*vin**2
EKVIN2 11 0 POLY(2) 10 0 2 0 0.  0.  0.  0.  1.
* for constant-current load, use vcvs, with gain = I
EILOAD 11 12 POLY(2) 15 0 30 0 0.  0.  0.  0.  1.
VILOAD 30 0 PULSE 0.2 0.4 175M 100U 100U 1.  2.
RVILOAD 30 0 1K
REKVIN2 12 0 1G
* [(k*vIN(rms)**2) - P]/V0
EFWD 20 0 POLY(2) 12 0 21 0 0.  1G -1G
RFWD 20 0 1MEG
EREV 21 0 POLY(2) 20 0 15 0 0.  0.  0.  0.  1.
RREV 21 0 1MEG
C 15 0 410U
RDUM1 15 0 100G
GCDV0 0 15 20 0 1.
DCL1 0 16 DS
VDCL1 15 16 DC 10.
* Output feedback VAC 15 44 AC 0.01
RVAC 15 44 50
R1 44 50 360K
R2 50 0 4.73K
CF 50 52 0.47UF
X1 51 50 0 52 53 0 ML4812EA
VREF 51 0 DC 5.0
VPOS 53 0 DC 6.0
* Gain of EK is
* [multiplier gain * Rmult]/[Rsine * (N1/N2) * Rsense]
* where, Rmult = termination resistor for multiplier,
* Rsine = resistance used to derive current reference
* from line, N1/N2 = current transformer primary to
* secondary turns ratio, and
* Rsense = current-transformer burden resistor
EK 2 0 52 0 0.0129
REK 2 0 1G
*** For ML4812A subcircuit listing, see earlier SPICE
*** Listing
.MODEL DS D(N=1U)
.TRAN 500U 10.3 9.0 500U
.OPTIONS NUMDGT=8, ITL5=0, ITL4=10000
.PRINT TRAN V(15) V(30) v(2)
.END
```