Narrowband PLC Channel Modeling using USRP and PSK Modulations

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***Abstract*—The indoor narrowband power line communication (NB-PLC) suffers from noise impairments, which emanate from several end-user electrical devices connected across the PLC channel. These noise impairments result into burst errors, which consequently lead to data corruption. Therefore, in order to implement robust communication techniques that will thrive on the noisy PLC channel, a full knowledge and modeling of the noise that exists on the NB-PLC channel is inevitable. This paper thus reports a First-order Markov modeling of NB-PLC channel noise, based on experimental measurements. For the modeling, BPSK, DBPSK, QPSK and DQPSK modulation schemes were implemented using Universal Software Radio Peripheral (USRP). The resulting channel models are useful for improving the robustness of the above modulation schemes as well as designing forward error correction techniques for mitigating the effect of noise impairments. The results are also useful in optimizing NB-PLC system design, thereby, enhancing the accuracy and improving the overall PLC system performance.**

***Index Terms*—Baum-Welch Algorithm, CENELEC, Fritchman model, noise measurement, power line communications, USRP**

I. Introduction

PLC technology utilizes the ubiquitous network of existing power lines that are universally accessible in almost every room in homes and offices across the globe for data communication purposes. The low-voltage in-house CENELEC A-band is one of the sub-bands of the four classified European CENELEC standard with frequency bandwidth between 3-95 kHz for narrowband applications [1]. The power line network was originally meant for electrical energy distribution to end-user devices. Its recent use as a medium of data communication inherits the harsh intrinsic attributes of power line accompanied by noise and disturbances that originate from un-coordinated use of end-user electrical devices connected onto the network. External noise sources such as broadcast stations and other devices sharing the same frequency as the PLC modulating frequency also introduce noise and disturbances onto the network. Thus, the CENELEC A-band is plagued with a lot of noise impairments, which result in burst errors that can corrupt the transmitted data, thereby, making reliable data communication almost impossible. To achieve a reliable communication as well as mitigate the performance degradation caused by the effect of noise impairments on the channel, modeling of the channel is vital.

In modeling other communication channels such as wireless, twisted pair, co-axial cables, an Additive White Gaussian Noise (AWGN) is usually assumed. However, such is not the case for PLC channel in general. The attributes of the noise existing on the NB-PLC channel are characterized and modeled as non-white, non-Gaussian and unstable. Therefore, this work is motivated by the need to model NB-PLC noise and disturbances, by using USRP to implement the modulation schemes specified in the NB-PLC standards. The USRP is a computer-hosted software defined radio designed by Ettus Research.

The two NB-PLC narrowband standards (i.e. PLC G3 and PRIME) have suggested Phase-Shift Keying (PSK) as the OFDM component in their specifications [2]. As such, this work has chosen to implement M-ary Phase-Shift Keying (M-PSK) and M-ary Differential Phase-Shift Keying (M-DPSK). In this work, Binary Phase Shift Keying (BPSK), Differential BPSK (DBPSK), Quadrature Phase Shift Keying (QPSK) and Differential QPSK (DQPSK) were implemented to be used for first-order Markov modeling of NB-PLC channel, using USRP. A single-error state first-order Fritchman model is used in this work. The resulting models for each modulation schemes were analyzed and hereby presented in this paper. These can be employed to improve the robustness of modulation schemes and, in addition, used to design forward error correction techniques for mitigating the effect of noise impairments on NB-PLC channels. Furthermore, the results can be used to optimize NB-PLC system design, thus enhancing PLC systems' overall performance.

The remaining part of this paper is structured thus. In Section II, a concise discussion of the following is presented: PLC noise classifications, PSK modulation schemes, Fritchman model and Baum-Welch algorithm. A detailed discussion of the experimental setup and methodology is done in Section III. In Section IV, a statistical analysis of the modeling results is carried out under the following headings: error sequence generation, estimated state transition matrix, log-likelihood ratio plots, and error-free run distribution plots. Finally, Section V concludes the paper.

II. Background

A. PLC Noise Classification

The noise associated with the PLC channel has been classified into background noise, impulsive noise and frequency disturbance (or narrowband noise) [3]–[5]. Background noise results from various sources of low power noise, which are usually household devices like computers, hair dryers and light dimmers. This noise category has increasing effect, as the frequency of transmission reduces and vice versa. Frequency disturbance, otherwise known as narrowband noise (NBN), is caused by interference from foreign signals in the spectrum of interest. The amplitude of this class of noise is usually time dependent, and it only dominates a narrow portion of the spectrum of interest [5]. As demonstrated in [5], NBN can be expressed as modulated sinusoidal signals, whose amplitude is coupled to the network. This noise class majorly originates from TV vertical scanning frequency and harmonics, AM transmissions and amateur radio connected to the same network as the transmitter [6]. Impulsive noise is the type with flat PSD (power spectrum density) which can affect all frequency components at a particular duration [7].

B. PSK Modulation Scheme

PSK is the process of encoding digital data bits onto an analogue form, by altering the phase of a sinusoidal carrier signal. It is possible to map more than one digital bit onto a sinusoidal carrier wave. Binary phase shift keying (BPSK) is the fundamental type of PSK, which maps only one bit of data onto the carrier, using two possible phases- bit 0 for 0 radian and bit 1 for π radians. Quadrature phase shift keying (QPSK) maps two bits onto a sinusoidal carrier phase, using four possible phases $-\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$. As described in [8], BPSK has one-dimensional constellation point ($N = 1$), having two equally spaced message points ($M = 2$) as the signal constellation. With QPSK, $N = 2$ and $M = 4$. As such, QPSK (or 4-PSK) is said to be a special case of M-ary PSK, in which the carrier phase has $M = 4$ possible values described by $2(i-1)\pi/M$, with i being $1, 2, \ldots, M$. In order to demodulate any PSK modulated symbol, a coherent reference signal is needed at the receiving end, for ensuring carrier recovery, which computes and equalizes phase and frequency imbalances between the received carrier wave and the local oscillator of the receiver. Symbol synchronization is achievable by using a suitable timing recovery algorithm.

DPSK is a non-coherent version of PSK modulation, which does not require coherent demodulation. However, to achieve symbol synchronization, there is need for timing recovery [9]. As such, it is relatively easy and cheap to implement DPSK receivers, as compared to those of ordinary PSK receivers. When a modulated DPSK symbol is received, it is more or less equivalent to a signal with unknown phase information, due to the way it is being modulated. Detailed information about M-PSK and M-DPSK modulation schemes can be accessed in any digital communication literature like [8], [9].

C. Fritchman Model

Hidden Markov models (HMMs), are usually utilized in several applications such as automatic speech recognition, digital signal processing, queuing theory, control theory, weather prediction, modeling of burst error channels, and a host of other interesting applications. Gilbert and Elliot [10], [11] proposed a HMM type regarded as the Gilbert-Elliot model. They assumed a two-state Markov model grouped into a good and a bad state, but this model does not depict the bursty nature of the NB-PLC channel. However, Fritchman, in [12], proposed a more advanced channel model which better depicts the actual long burst error nature of the NB-PLC channel.

For a binary channel, Fritchman grouped the state space into k good states and $N-k$ bad states. An error-free transmission occurs in a good state, while a bad state is characterized by a frequently occurring transmission error.

According to Vogler [13], a single-error state Fritchman model offers a fair compromise between the analytic intractability of sophistication and the non-realism of a two-state Markov model. Hence, a single-error state Fritchman model with two error-free states is assumed in this work as shown in Figure 1.

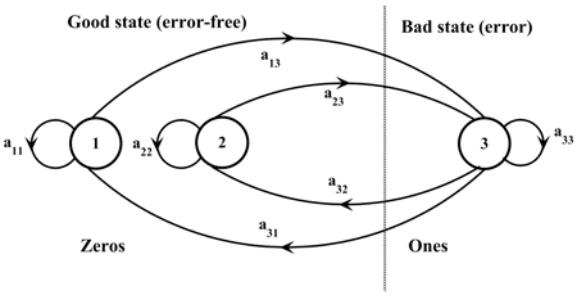

Fig. 1. A Three-state Fritchman Markov model.

In Figure 1, it is evident that for the three-state partitioned Fritchman model, transitions are not permissible between states of the same group. This implies the availability of multiple degrees of memory. Hence, modeling of real communication channels is made possible. The assumption of a single-error state Fritchman model allows for the models error-free distribution $Pr(0^m|1)$ to distinctively indicate the single-error state. Hence, the model parameters are obtainable from the error-free run distributions and vice versa [14]. In general, the state transition probabilities, A for Figure 1 can be expressed in matrix form as:

$$\mathbf{A} = \begin{bmatrix} a_{11} & 0 & a_{13} \\ 0 & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix}.$$

The values of elements a_{12} and a_{21} are zeros. This is based on the fact that transitions are not permissible between states of the same group. The output symbol probability matrix, B is expressed as:

$$\mathbf{B} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}.$$

The elements of the B matrix contains zeros and ones, because no transitions is allowed between states of the same group, hence an error only occurs in the bad state, while the good states are error-free. Therefore, the entries are not to be estimated [15]. The prior or initial state probabilities is denoted by π and expressed as:

$$\pi = [\pi_1,\ \pi_2,\ \ \ldots, \pi_N].$$

where, N is the number of states which is three for this work.

D. Baum-Welch Algorithm

Baum-Welch algorithm [15], [16] is a method that uses the maximum likelihood estimation approach to estimate the model parameters, $\Gamma = (A, B, \pi)$, such that the likelihood of the observed sequence O is maximized. The expectation maximization (EM) method is used to solve the maximum likelihood estimation problem. The EM approach is an iterative method that begins with an initial assumption of the model parameters, Γ and updates of these model parameters are carried out iteratively in such a manner that the likelihood does not decrease for each step. For detailed steps of how the model parameters are re-estimated, refer to [17] and [15].

III. Experimental setup and Methodology

Figure 2 shows the schematic of the experimental setup involved in this work. The experiment was setup in the Convergence Laboratory at the University of the Witwaterstrand, Johannesburg. The power line topology used is 7-meters long, with 4 load points in-between and the feeding end was initially connected to the mains (230 V) power line in the laboratory and latter connected to an isolated UPS (uninterrupted power supply), so as to form two scenarios of operations. The USRP hardware at the right hand side of the topology was configured as the transmitter, whose RF (radio frequency) output is connected to a PLC coupling circuit, and the receiving USRP sits at the left hand side of the topology. The two PCs connected to the USRPs are equiped with a software capable of some functionalities (like modulation, filtering and amplification, etc.), which are normally carried out by electronic components. This therefore provides flexibility in the sysetm, and as well, gives room for experimenting some new concepts like forward error correction schemes (e.g., Permutation Trellis coding).

For the practical analysis, measurements were taken for two scenarios. For scenario 1, the topology was powered through an uninterruptible power supply (UPS), to isolate it from the laboratory topology, with a flickering incandescent light bulb (100 W) introduced in-between the Tx and Rx. The bulb was used to simulate the effect of impulsive noise on the topology. However, for scenario 2, the topology was directly connected to one of the laboratory's 230 V power outlets, but without introducing the flickering light bulb.

Figure 3 shows a photograph of the experimental setup and the different devices used.

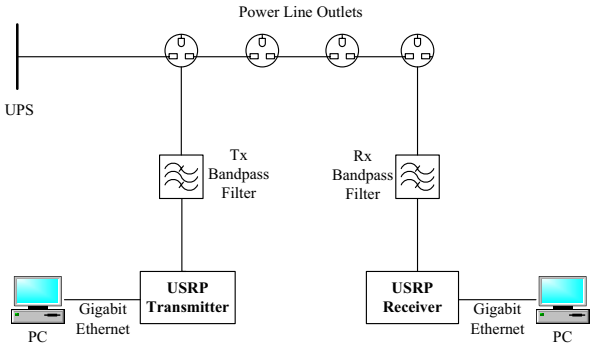

Fig. 2. Block diagram of the experimental setup showing the end-to-end connection

Fig. 3. Picture of the experimental setup

A. Host-based Software description

The SDRU (Software Defined Radio uhd) Simulink Target and communication toolbox, developed by Mathworks, are the software components used in this work. The toolbox is equipped with some signal processing blocks, which can either be used directly or developed from scratch, depending on the user's application requirements. These blocks can be connected together to form the signal processing flow graph. The SDRU Target contains two main boxes, which are either used as the signal sink (for the USRP Tx) or source (for the USRP Rx). The SDRU boxes are what are used to configure the hardware's parameters like the signal level, operating frequency, decimation and interpolation. USRPs are loaded with FPGA and firmware images to provide compatibility with the software version to be used. Table I contains the important modulation and configuration parameters used in our implementation.

B. Hardware description

The USRP hardware used is the Ettus-USRPs (as transmitter, Tx and receiver, Rx). USRP generally has digital to analogue (D/A) and analogue to digital (A/D) converters for respectively up-converting and down-converting the signals,

TABLE I
SOFTWARE CONFIGURATION

PARAMETER	VALUE
Tx gain & Rx gain	Default (not tunable)
USRP Firmware revision	usrp2_fw (003.002.003)
USRP FPGA revision	usrp2_fpga (003.002.003)
Centre frequency	92 kHz
Sample time	5 μs
Sampling frequency	0.2 MHz
Transmitted bits	5256
Decimation & Interpolation factors	1e8/Sampling frequency
Modulation schemes	BPSK, DBPSK, QPSK & DQPSK
Host Tx & Rx Operating System	Windows 7, 64 bits, Ver. 6.1
Host-based Software Version	Matlab R2012b (8.0.0.783)

TABLE II
HARDWARE CONFIGURATION

ITEMS	CONFIGURATION
Tx and Rx USRP Hardware Rev. no.	USRP2, ver 4.0
Tx daughterboard model	LFTX, rev 2.2 (0-30 MHz)
Rx daughterboard model	LFRX, rev 2.2 (0-50 MHz)
Host Tx IP & USRP Tx IP	192.168.10.1 & 192.168.10.2
Host Rx IP & USRP Rx IP	192.168.30.1 & 192.168.30.2

FPGA (field programmable gate array) which is used for interpolation and decimation, and Ethernet interface for interfacing the hardware with the computer. The Cat 5E Ethernet cable used is capable of handling 1000 Mbps of data speed from the PC's Ethernet controller, and it can handle full-duplex operation. USRP also contains daughterboards (RF front ends), whose specifications determine the frequency of operation of the hardware setup. The Tx and Rx daughterboards used are respectively LFTX and LFRX, each with respective operating frequency range of 0-30 MHz and 0-50 MHz.

For good performance, it is advised to ensure that the hardware sample time and the source block (the software block that conveys the data received by the Rx hardware to other software processing blocks) are matched [18]. As such, the sample time used is calculated as Decimation rate/1e8, where 1e8 is the hardwares A/D sampling rate (in Hz). The Tx gain value determines the amplitude level of the signal sent into the channel, from the transmitting USRP. Table II shows the hardware parameters and configurations used for the implementation.

C. First-order Markov Model Parameters

The initially assumed model parameters for the three-state Fritchman model are expressed in matrix form as:

$$A = \begin{bmatrix} 0.9 & 0 & 0.1 \\ 0 & 0.8 & 0.2 \\ 0.1 & 0.2 & 0.7 \end{bmatrix}, \qquad B = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}.$$

$$\pi = [0.3\ 0.3\ 0.4].$$

From the state transition matrix defined for this work, the diagonal elements were uniquely chosen, such that when a transition to a new state occurs, the probability of the channel remaining in the same state before transitioning into another one is high. The above defined model parameters are fed as input into the Baum-Welch algorithm, together with the training error sequence.

IV. RESULTS

This section presents the experimental and modeling results of work done in this researh.

A. Error sequence generation

The error sequence for each modulation scheme implemented on the NB-PLC channel was generated. These sequences were generated based on correlation between the sent and received bits. "0" denotes a correct bit received at the receiver, while "1" denotes an incorrect bit. The length of each error sequence is 5256, which is the same as the length of the transmitted bits.

Figure 4 and Figure 5 show the error bit locations for scenario 1 and 2, respectively. As seen in Figure 4, the long burst error is well pronounced. This is as a result of noise impulses emanating from the flickering light bulb introduced. Due to the absence of the flickering light bulb in scenario 2, the presence of long burst error is not well pronounced, as visible in scenario 1.

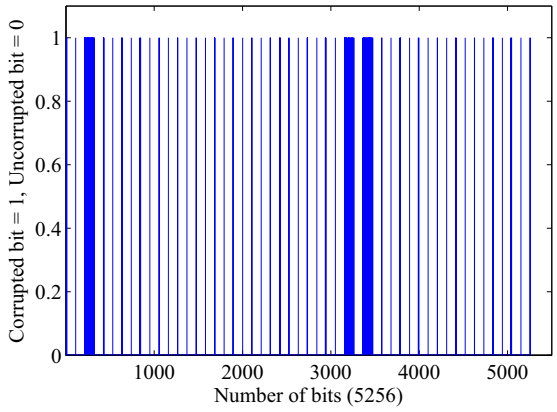

Fig. 4. Error bit locations for Scenario 1 (for DBPSK modulation).

B. Estimated State Transition Matrix

Table III and Table IV show the estimated state transition vectors for the four models generated for each modulation scheme implemented in both scenarios 1 and 2. The Fritchman model parameters computed depict the error statistics of the NB-PLC channel in each scenario. The parameters describe the distribution of the transmission errors as measured on the channel. The distribution of these errors are non-uniform which is typical of a PLC channel and evident in Table III

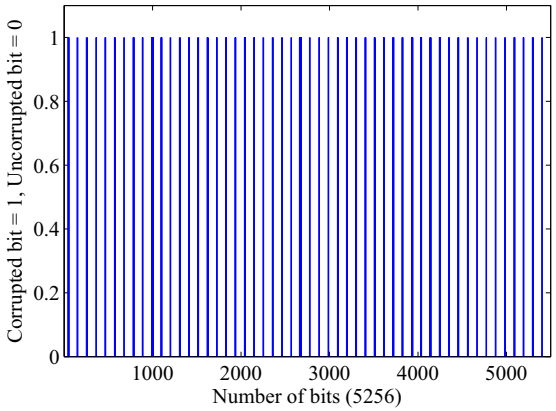

Fig. 5. Error bit locations for Scenario 2 (for DQPSK modulation).

TABLE III
ESTIMATED STATE TRANSITION MATRIX FOR SCENARIO 1.

a	BPSK	DBPSK	QPSK	DQPSK
a_{11}	0.9882	0.9896	0.9893	0.9887
a_{13}	0.0118	0.0104	0.0107	0.0113
a_{22}	0.6496	0.4552	0.6092	0.4404
a_{23}	0.3504	0.5448	0.3908	0.5596
a_{31}	0.3874	0.1247	0.6059	0.3779
a_{32}	0.4057	0.4129	0.2456	0.2895
a_{33}	0.2069	0.4624	0.1485	0.3326

TABLE IV
ESTIMATED STATE TRANSITION MATRIX FOR SCENARIO 2

a	BPSK	DBPSK	QPSK	DQPSK
a_{11}	0.9875	0.9894	0.9882	0.9879
a_{13}	0.0125	0.0106	0.0118	0.0121
a_{22}	0.7198	0.5517	0.6211	0.6360
a_{23}	0.2802	0.4483	0.3789	0.3640
a_{31}	0.4132	0.2106	0.4217	0.2920
a_{32}	0.3206	0.3663	0.2343	0.3020
a_{33}	0.2663	0.4231	0.3440	0.4060

and IV, where the values of the state transition matrix for each model differ from one another. The non-uniformity in the error distribution can also be attributed to the differing channel characteristics at the time of transmission, the type of noise encountered on the channel and several other factors.

C. The Log-likelihood Ratio Plots

There is need to solve the problem of numerical underflow that occurs due to large data sets used in the computation of the forward and backward variables. This problem causes the values of the forward and backward variables to exponentially tend to zero, hence, the need for proper scaling. For a detailed literature on scaling, refer to [15]. Figure 6 and Figure 7 show the log-likelihood plots for each model generated for the four modulation schemes implemented (scenario 1 and 2). Taking a closer look at the Figure 6 and Figure 7, it can be seen that the model parameters start to converge at the 2nd iteration, but the desired level of accuracy is reached at the 4th iteration, and the algorithm terminated at the 20th iteration. Also, it is obvious from the two figures that the log-likelihood values differ from each other with the exception of Figure 7, where the model parameters for QPSK and DBPSK converge with similar log-likelihood ratio values, due to similar error pattern. The difference in the log-likelihood values for the other models is as a result of differing error pattern and the number of errors that exist in each error sequence. These differing pattern are as a result of the disimilarities in the characteristics (e.g symbol energy and euclidean distance on the constellation graph) of the modulation schemes used [19].

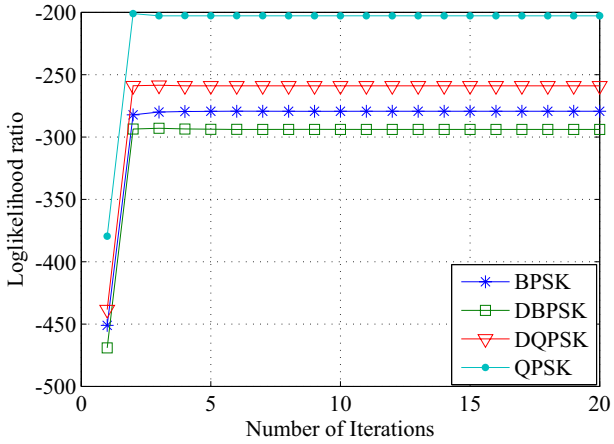

Fig. 6. Loglikelihood ratio vs. iteration for scenario 1

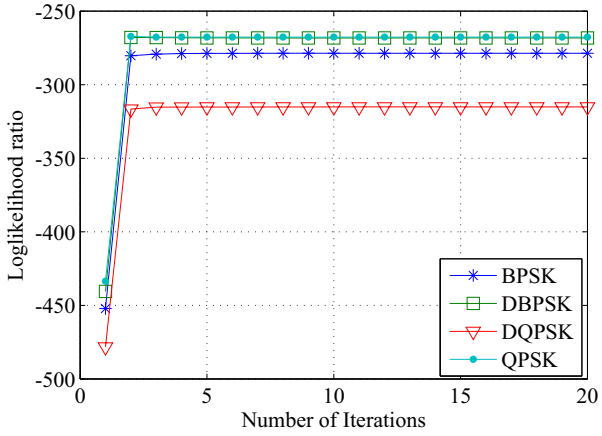

Fig. 7. Loglikelihood ratio vs. iteration for scenario 2

D. Error-free run Distribution Plots

Figure 8 and 9 present the error-free run distribution plot for the four models generated for the four modulation schemes for both scenarios. The error-free run distribution is denoted

TABLE V
LENGTH OF INTERVAL "m" FOR SCENARIOS 1 AND 2

	BPSK	DBPSK	QPSK	DQPSK
m (*Scenario* 1)	97	104	104	102
m (*Scenario* 2)	98	106	102	97

by $Pr(0^m|1)$. This implies the probability of transitioning to m-consecutive error-free states, after exiting an error state. The length of interval, m for scenarios 1 and 2, is shown in Table V.

A comparison between length of interval for scenarios 1 and 2, in Table V, shows similar interval length, attributed to similar channel characteristics, with the exception of DQPSK, which is attributed to differing channel characteristics at the time of experiment.

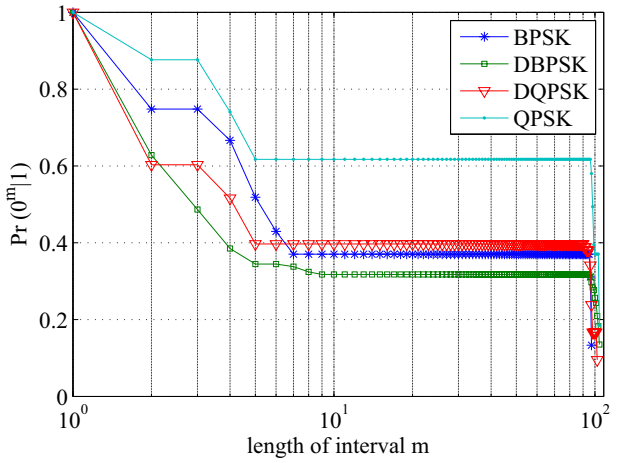

Fig. 8. $Pr(0^m|1)$ vs. interval m for scenario 1

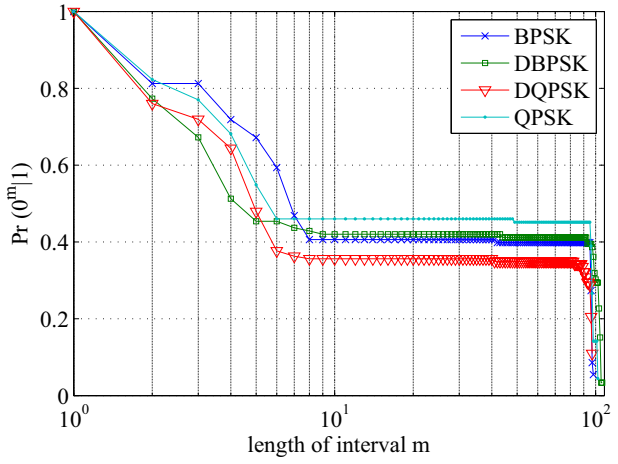

Fig. 9. $Pr(0^m|1)$ vs. interval m for scenario 2

V. CONCLUSION

Implementation of PSK modulation for NB-PLC channel modeling using USRP has been presented in this work. A three-state Fritchman model was employed to model the NB-PLC channel and the resulting statistical models are precise channel models obtained from experimental measurements. The error bit locations, showing the pattern of errors were also presented, with the presence of long burst errors more pronounced in scenario 1. The resulting model for each modulation scheme were analyzed and presented. These are useful for improving the robustness of the modulation schemes. Also, the results are vital in evaluating and designing robust channel coding schemes (e.g permutation trellis coding) that will improve transmission performance over NB-PLC channel, thereby enhancing the overall PLC system performance.

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