Noise Reduction by Pixel Circuit Optimization in 4-T Pixel Structure Detectors Using Integrated Circuit Technologies

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***Abstract*—The most commonly used pixel structure in integrated circuit technologies is the three-transistor pixel structure (3-T). This structure consists of a pixel, a reset transistor, a source follower and a pixel select transistor. An extension to this is the 4-T pixel structure where an extra transistor is included to enable current steering in the readout phase and reset phase. This greatly reduces current consumption compared to the conventional 3-T pixel structure. Simulation results depicting this optimization is provided to support the technical contribution of this paper.**

***Index Terms* — CMOS technology, Active pixel sensors, threshold voltage, current, photonic integrated circuits, dark current.**

I. Introduction

Charged coupled devices (CCD), in the application of imaging, exhibits excellent performance in terms of dynamic range, sensitivity and noise performance. However this technology lacks integration capability with silicon electronics.

Integrated circuit (IC) technology presents attractive features to detector development, such as repeatability and rapid prototyping.

There are several sources of noise in detectors, ranging from thermal noise to on-chip switching noise when using IC technology. CCD has reduced on-chip switching noise, in comparison to IC technology, owing to the movement of photons from the pixel to the outside of the chip, where all the post-processing takes place, without any conversion or "latches" being used. The photon-to-electron-to-voltage conversion takes place off-chip. This conversion process takes place on the chip itself in the case of an IC. This limits the performance of IC detectors because of the decrease in signal-to-noise ratio (SNR) of the detector, which is a major disadvantage – it reduces the dynamic range and sensitivity of detectors, which are the most important parameters concerning detector developers.

In this paper, which builds on a previous conference publication [1], a summary of the different types of noise inherent to IC detectors and different methods to reduce these noise currents will be presented as a basis for the work. Of these methods, the double gate device concept is selected and simulated for the 4-T current-mediated pixel structure [2] [3] [4]. This structure is given in Fig. 1

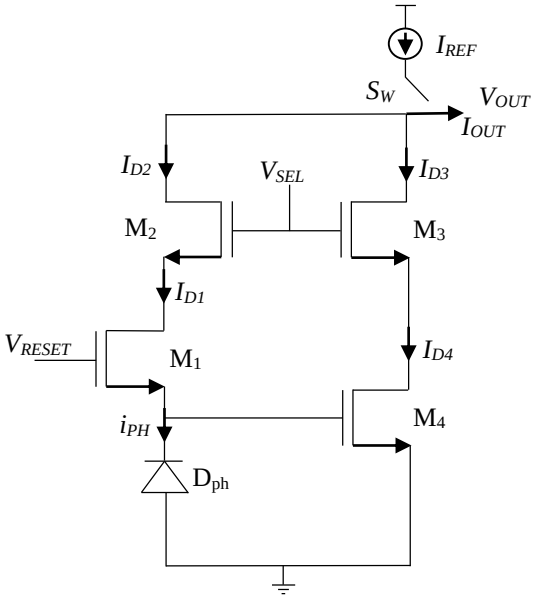

Fig. 1: 4-T Pixel structure

Thereafter these noise results will be compared to a previous conference publication where the 3-T pixel structure was presented with the double gate device concept implemented [1]. It is not possible simply to increase the number of components (e.g. the addition of the extra transistor to implement the double gate concept) without compromising other parameters, such as fill-factor. These trade-offs will be taken into account in this work.

A novel method of optimising 3-T voltage mode pixel circuits have been documented where the different voltage points have been simulated for a specific set of parameters [5]. The same concept will be followed for this work.

The kTC noise inherent to detectors is the determining factor with regard to the operating temperature. The operating temperature also affects the dark current of the detectors. Uncooled detectors are selected for this work, since cryogenic

cooling is very expensive, maintenance-intensive, and uncooled detectors have lower power consumption. A summary of typical operating temperatures of detector materials used in IC technology will be presented. Mercury cadmium telluride exhibits the best noise performance but it requires cooling. However, silicon (Si) or silicon germanium (SiGe) materials exhibit relatively good noise performance in comparison to other materials, yet requires no cooling.

II. Effect of Noise in Detectors

Several contributors to noise exist in IC detectors. These contributors range from flicker noise to shot noise to fixed pattern noise (FPN). Among all the different methods to reduce noise, reducing readout noise has the greatest impact on detector performance [1]. In [1], published noise values are provided.

The use of SiGe heterojunction bipolar transistors (HBT) will reduce noise generated when used as a pixel because of the lower base resistance and increased speed [6]. The overall SNR increases owing to the increased gain.

Thermal and flicker noise are heavily dependent on transconductance and drain current. Both of these are heavily dependent on the aspect ratio. By altering the aspect ratio, one can tune or optimize the detector noise content. It is for this reason that the aspect ratio is varied to determine the noise output.

Dark current inhibits the performance of detectors since the induced photon current must be larger than the dark current. By decreasing the operating temperature, dark current can be reduced [7]. Uncooled detectors have received significant attention because of their simpler integration and operating conditions [8].

III. Velocity Saturation

Velocity saturation causes deviations in measured data [9]. This can be modelled by inserting a resistor in series with the source of the metal-oxide-semiconductor (MOS) device. Fig. 2 depicts the placement of this resistor, R_{sx}.

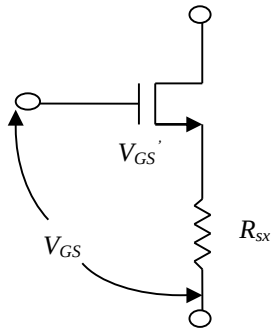

Fig. 2: Resistor used to model velocity saturation in a normal transistor circuit [10].

As shown in Fig. 2, the resistor is in series with the source. The value of this resistor changes as the width of the transistor changes, which is given in (1).

$$R_{sx} = \frac{1 * 10^4}{\mu_n * C_{ox} * W * \varepsilon_c} \tag{1}$$

where μ_n is the mobility of the electrons $(\mathrm{m^2/V-s})$
C_{ox} is the oxide thickness $(\mathrm{fF/\mu m^2})$
W is the width of the transistor $(\mu\mathrm{m})$
ε_c is the critical electrical field $(\mathrm{V/cm})$.

Parameter extraction was performed to determine R_{sx}. For a MOS device operating in the triode region, the value of R_{sx} can be calculated using (2).

$$R_{sx} = \frac{L}{V_{DS} \times k \times W} - \frac{V_{DS} - 2 \times V_T}{2 \times I_D} \tag{2}$$

where $k = \mu_n \times C_{ox}$. For a MOS device operating in the linear region, the value of R_{sx} can be calculated using (3).

$$R_{sx} = \frac{V_{GS} - V_T}{2 \times I_D} - \frac{L}{k \times W \times (V_{GS} - V_T)} \tag{3}$$

As seen in (1) – (3), the value of R_{sx} is proportional to W and V_{DS}. The physical reason for this is that the carrier velocity is proportional to the applied voltage, V_{DS} of the transistor.

IV. Basic Pixel Operation

As shown in Fig. 1, the actual pixel element is a reversed biased diode. The main function of this diode is to block any current flowing from the supply under no illumination. Practically, this is not possible. There will be some leakage current flowing, which is commonly known as the dark current [11].

The current flow that occurs when a pixel is illuminated is known as the photon generated current, which is given by (4).

$$i_{PH} = \eta * e * \Phi * A \tag{4}$$

where η is the quantum efficiency, e is the charge of an electron (C), Φ is the photon flux density $(\mathrm{electrons/cm^2-s})$ and A is the junction area $(\mu\mathrm{m^2})$.

There are two modes of operation for the current-mediated 4-T pixel structure. In the reset mode, the V_{SEL} port is ON and the V_{RESET} port is ON. In this case the output current is given as follows

$$I_{OUT} = I_{REF} - I_{D2} - I_{D3} \tag{5}$$

The second mode is the readout mode where the V_{SEL} is ON and the V_{RESET} is OFF. In this case the output current is given as follows

$$I_{OUT} = I_{D3} \tag{6}$$

V. Detector Operation

A previous publication is used as the basis for the discussion in this section [5]. Transistor M_1 operates in the triode region of operation. The gate is connected to the reset pin. When the reset pin is HIGH, the source voltage of M_1 is given as follows:

$$V_{S1} = V_{D1} - V_{T1} - i_{PH}R_{SX1} - \sqrt{V_{T1}^2 + \frac{2i_{PH}L_1}{k_1 W_1}} \quad (7)$$

When the reset pin is low, V_{D1} is given as

$$V_{D1} = V_{T1} + i_{PH}R_{SX1} + \sqrt{V_{T1}^2 + \frac{2i_{PH}L_1}{k_1 W_1}} \quad (8)$$

For transistor M_2, when V_{SEL} is OFF, the pixel is not selected due to M_2, which is in the cutoff region of operation. When V_{SEL} is ON, V_{S2} is given as:

$$V_{S2} = V_{D2} - V_{T2} - I_{D2}R_{SX2} - \sqrt{V_{T2}^2 + \frac{2I_{D2}L_2}{k_2 W_2}} \quad (9)$$

Since $V_{D2} = V_{OUT}$, (9) with rearranging changes to

$$V_{OUT} = V_{S2} + V_{T2} + I_{D2}R_{SX2} + \sqrt{V_{T2}^2 + \frac{2I_{D2}L_2}{k_2 W_2}} \quad (10)$$

Transistor M_3 operates in the same region of operation as M_2. Thus output voltage w.r.t. M_3 is given as:

$$V_{OUT} = V_{S3} + V_{T3} + I_{D3}R_{SX3} + \sqrt{V_{T3}^2 + \frac{2I_{D3}L_3}{k_3 W_3}} \quad (11)$$

For transistor M_4, M_1 will have a significant influence. This also includes the photon-generated current. If short-channel devices are chosen, I_{D4} is thus given by

$$I_{D4} = \frac{k_4}{2\left[1 + k_4 \frac{W_4}{L_4} R_{SX4} V_{OV4}\right]} \frac{W_4}{L_4} V_{OV4}^2 \quad (12)$$

where $V_{OUT4} = V_{T4} + V_{D4} - V_{G4}$.

Since $V_{G4} = V_{S1}$, V_{G4} is given as

$$V_{G4} = V_{D1} - V_{T1} - i_{PH}R_{SX1} - \sqrt{V_{T1}^2 + \frac{2i_{PH}L_1}{k_1 W_1}} \quad (13)$$

If long-channel devices are chosen, I_{D4} reduces to:

$$I_{D4} = \frac{k_4}{2} \frac{W_4}{L_4} V_{OV4}^2 \quad (14)$$

Several factors that influence the analysis in [5] also influence the detector discussed in this paper.

VI. Effect Of Double Gate Devices

Double gate devices are used to reduce noise content. This is done by connecting the gates of two MOS field effect transistors (MOSFETs) to effectively double the oxide capacitance (C_{OX}). This increase in capacitance effects each MOSFET. There are several methods to implement double gate devices. Some methods are difficult to implement in CMOS technologies. For this work, the chosen double gate MOSFET configuration is given in [1]

Since $k = \mu_n C_{ox}$, the source voltage of M_1, as a result of this configuration, becomes:

$$V_{S1} = V_{D1} - V_{T1} - i_{PH}R_{SX1} - \sqrt{V_{T1}^2 + \frac{i_{PH}L_1}{k_1 W_1}} \quad (15)$$

When the reset pin is low:

$$V_{D1} = V_{T1} + i_{PH}R_{SX1} + \sqrt{V_{T1}^2 + \frac{i_{PH}L_1}{k_1 W_1}} \quad (16)$$

For transistor M_2:

$$V_{OUT} = V_{S2} + V_{T2} + I_{D2}R_{SX2} + \sqrt{V_{T2}^2 + \frac{I_{D2}L_2}{k_2 W_2}} \quad (17)$$

Again (17) holds for M_3.

For transistor M_4, I_{D4} becomes:

$$I_{D4} = \frac{2k_4}{2\left[1 + 2k_4 \frac{W_4}{L_4} R_{SX4} V_{OV4}\right]} \frac{W_4}{L_4} V_{OV4}^2 \quad (18)$$

VII. Simulation Results

The mathematical equations were plotted in MATLAB. While the MATLAB plots do not include any parasitic components, the same is not true for simulations done using Cadence Virtuoso. The simulation results are based on the process design kit (PDK) allowing inclusion of relevant non-ideal parasitic values. Parameters such as the V_T, V_{DD} and k values were taken from the PDK; however, this is not repeated here due to a non-disclosure agreement (NDA) with the foundry. This is a 3.3 V process.

The typical photon-induced current in CMOS pixel technology, with a high fill factor, is in the nA range.

The simulation given in Fig. 3 shows the source voltage of M_1 for different widths of M_1 when sweeping the photon-induced current.

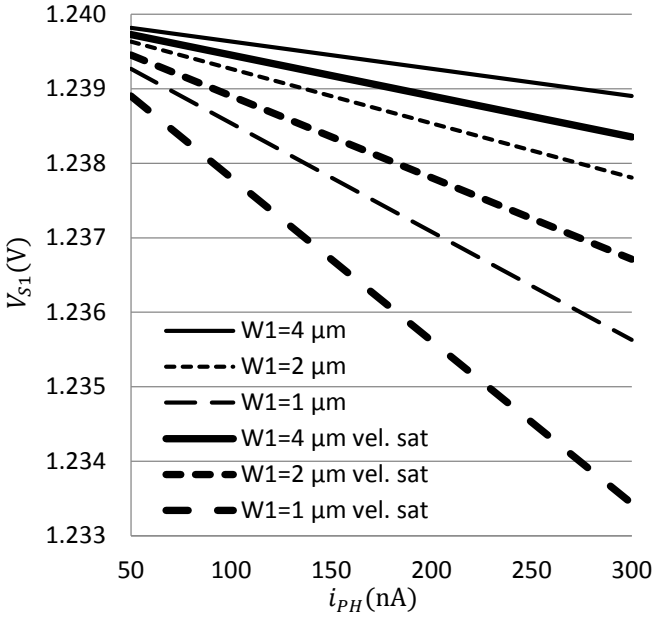

Fig. 3: Source voltage of M_1 vs. photon-generated current for various transistor widths.

As shown in Fig. 3, the source voltage increases as the aspect ratio increases. When velocity saturation is taken into account, since the length is taken as 1 µm, the source voltage is slightly lower. The actual output is expected to be between these two graphs.

The source voltage is then fed into M_4's gate voltage to regulate the current flow through M_4. This drain voltage (V_{D1}) regulates the source voltage of M_2. Together with the V_{SEL} pin connected to the gate of M_2, the current through M_2 is regulated. There is, however, one requirement here, which is the allowed limit of current flow must be more than the current through M_1. Errors will occur in the read-out phase if this limit is too small.

To illustrate the effect the aspect ratio has on the source voltage of M_2, (9) is plotted in Fig. 4.

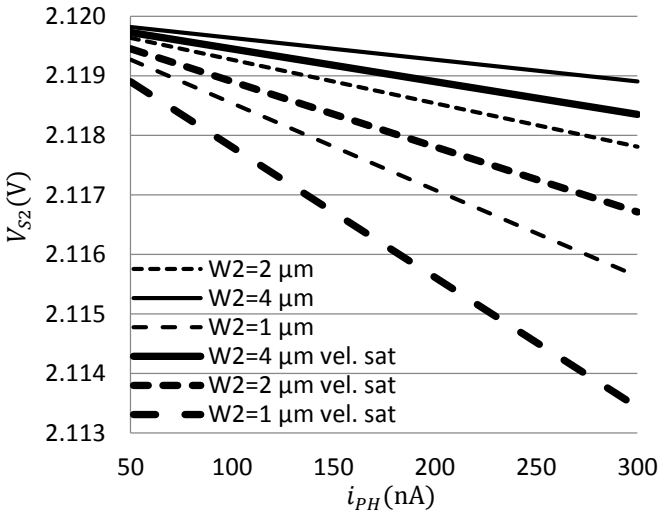

Fig. 4: Source voltage of M_2 vs. photon-induced current for various transistor widths.

In Fig. 4, the source voltage is shown for various transistor widths. This is plotted versus induced photon current, the lower limit of the allowed current flow to eliminate possible captured radiation errors. In reset mode, this current will flow through to the output line, whereas in readout mode this current will not reach the output port since M_2 is in cutoff and acts as a large resistor blocking the flow of current.

When the detector is in readout or in reset phase, current will be flowing through M_3 and M_4. However since M_2 is in cutoff when in readout mode, the current flow through M_1 will regulate the gate voltage of M_4.

For M_3, the mode of operation will be the same as with M_2 since the gates and drains are connected. The source voltage will differ in this case, but not so much that it will change the mode of operation. The minimum current flow here again should be more than the current flow through the pixel. Therefore this is chosen as the lower limit and simulated accordingly. Consequently the simulation results are exactly the same as with M_2 and are shown in Fig. 4.

The last transistor is M_4. The regulator in this case is the gate voltage, which is connected to the source of M_1. Using the same argument as with transistor M_2 in [5], the drain current with respect to gate voltage is given in Figs. 5, 6 and 7.

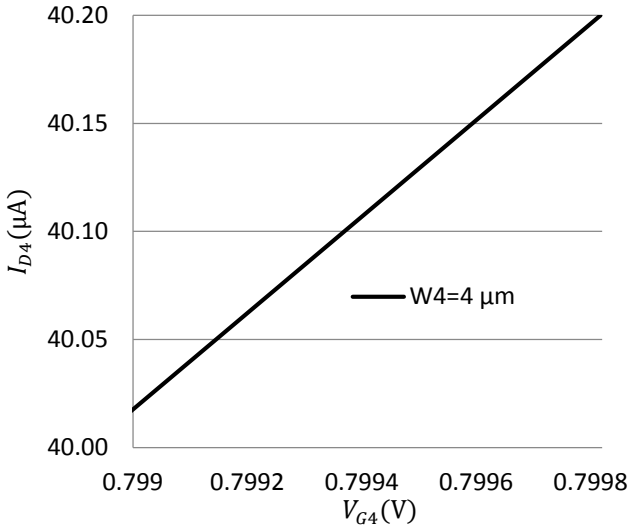

Fig. 5: Drain current of M_4 versus gate voltage for W=4 μm.

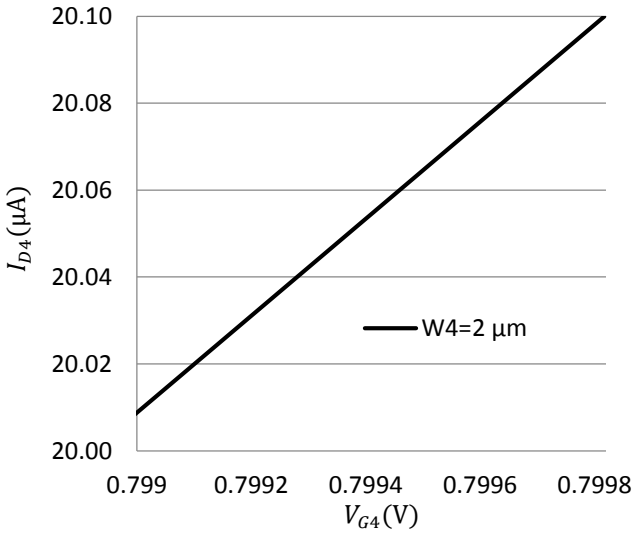

Fig. 6: Drain current of M_4 versus gate voltage for W=2 μm.

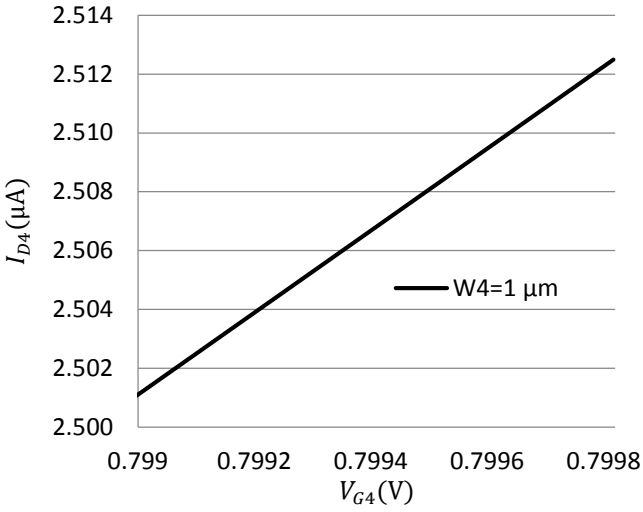

Fig. 7: Drain current of M_4 versus gate voltage for W=1 μm

In all three cases for M_4's gate voltage, the drain current through the MOSFET increases as the gate voltage increases. The current flow is around 40 μA, 20 μA and 2 μA for W = 4 μm, 2 μm and 1 μm respectively. This provides a realistic indication of current levels that can flow for the given set of specifications. This is, however, without the inclusion of velocity saturation. Since the velocity saturation "resistor" includes the drain current, it will be difficult to isolate the gate voltage and drain current to simulate alone. Therefore the gate voltage is assumed as constant and then the velocity saturation "resistor" is simulated versus the drain current in Fig. 8.

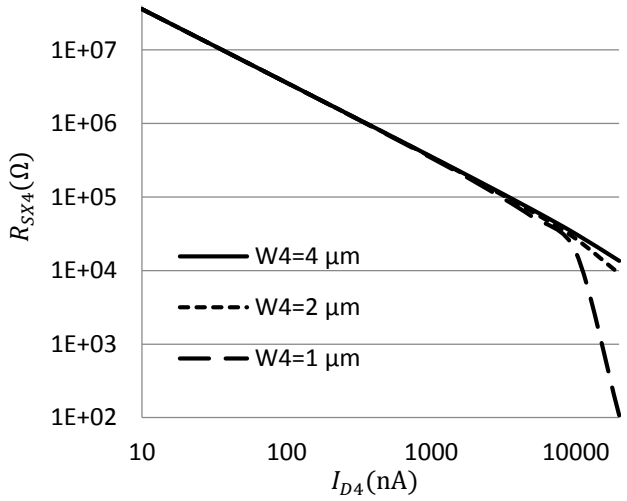

Fig. 8: Velocity saturation "resistor" versus drain current of M_4

In Fig. 8, the velocity saturation "resistor" versus the drain current of M_4 is shown for various transistor widths. For drain currents below 5 μA, the transistor widths do not make a significant difference in the velocity saturation "resistor" value.

Above 5 μA, the widths have a significant influence on this "resistor" value and will therefore influence other voltage points around transistor M_4. This is a critical design point for these detectors.

VIII. Conclusion

A novel method of designing 4-T pixel circuitry for a current-mediated detector has been conceptualised and evaluated using simulations. For this paper, the effect of velocity saturation was included; however, by including other non-ideal effects such as noise and short-channel effects due to electron drift and threshold voltage modifications, this error can be reduced further in a future contribution.

By choosing the aspect ratio of the different transistors, the different voltages and currents can be accurately calculated with the equations derived in this paper. Transistors M_2 and M_3's width must be chosen large enough to accommodate all the current flowing through M_1 and M_4. For the given parameters, M_1, M_2, M_3 and M_4's width is preferred to be large. The fill factor should be taken into account at all times.

The method introduced in this paper reduces FPN [12]. Much the same method can also be used in the voltage mode detector.

Possible future work as a result from this article is the implementation of a set of parameters to determine noise content of a specific detector design and implement accordingly

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