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Leakage Current Minimisation and Power Reduction Techniques using Sub-threshold Design

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***Abstract*— Low power IC solutions are in great demand with the rapid advancement of handheld devices, wearables, smart cards and radio frequency identification bringing a massive amount of new products to market that all have the same primary need: Powering the device as long as possible between the need to re-charge the batteries while at the same time dramatically decreasing the device leakage currents. The use of sub-threshold techniques can be a powerful way to create circuits that consume dramatically less energy than those built using standard design practices. In this research, a SOI device was built to compare their electrical characteristics using Silvaco software. The comparisons were focused on three main electrical characteristics that are threshold voltage, sub-threshold voltage and leakage current. It was found that SOI devices are ideal candidates for low power operation.**

Keywords- Power dissipation, Weak inversion, Ultra-low-power, Leakage currents, power analysis

I. INTRODUCTION

Low energy consumption and minimal leakage current emissions are slowly replacing performance as the foremost challenge in electronic design. Performance is important; however it must now accede to the energy capacity of batteries and even the minimal output of power harvesters. Performance at all costs no longer works; efficient energy consumption and reduced leakage current are now the dominant requirements. While reducing energy consumption and leakage current are vitally important within the electronics industry, the question is: how should those goals be achieved?

In today's electronic circuits, energy is dissipated in two fundamental forms: as leakage, when a circuit's state is not changing, and dynamically as internal nodes are charged up and down. In most cases, for realistic circuits in operation, dynamic power dominates; especially for higher power supply voltages used in most designs today as shown in (1) [9 , 10].

$$P = ACV^2f + VI_{leak} \quad (1)$$

Because electronic circuit's dynamic energy varies as the square of the operating voltage, that entity becomes the most important component for reducing dynamic energy consumption (while at the same time also having a distinct, but less dramatic, impact on leakage). For instance, a near-threshold electronic circuit operating at 0.5V can achieve up to a 15 times improvement in dynamic energy in comparison with a typical circuit operating at 18V. An even more aggressive "sub-threshold" circuit operating at 0.3V can achieve up to a 36 times improvement!

It is worth mentioning that in (1) we have ignored power lost to the momentary short circuit at a gate's output whenever the gate switches. That loss is relatively small and mostly contributes to dynamic power loss; the equation's first term can absorb it if necessary. Conventional digital electronic circuits' designs techniques use transistor states (on or off) as a critical theory for implementing logic. Analog designs moreover assume that a transistor is in the "on" state to some controlled degree, using it for amplification purposes. In chip design techniques, sub-threshold operation implies that none of the voltages in the chip rise above the threshold voltage (V_{th}), so the transistors technically never goes "on". Even a logic "high" voltage keeps the transistors "off." This implies that improved design approaches are required.

This paper examines the challenges of sub-threshold design, with a focus on what's required to overcome the differences from conventional super-threshold design. These considerations may help in driving the development and commercialization of Sub-threshold power optimized technologies that can lead to the building of reliable, robust circuits that dissipate dramatically less energy on a cost-effective, mainstream manufacturing process.

II. THE SUB-THRESHOLD CONCEPT

Sub-threshold design isn't a new concept. As early as the 1970s, Swiss watchmakers realized the potential of operating selected transistors in the sub-threshold regime. The idea was devised and tested on pacemakers and RFID tags, but never saw much acceptance beyond that in the chip manufacturing industry [1]. After a hush that lasted a few decades, the topic regained some academic interest around late 1990s and early 2000s. By that time, the upcoming domination of energy

consumption was evident, and research started investigating economical ways that commercial circuit designers could reduce energy dissipation. Sub-threshold design techniques were among those initial ideas. It then becomes obvious to ask why such a technology that was developed in the 70s, never caught on. One might even suspect that technical flaws might have been uncovered in that technology which kept sub-threshold out of the mainstream.

One might also ask what has changed since the 70s, when the first commercial sub-threshold devices were created. A simple answer to question is related to scale: Early designs only used a few critical sub-threshold transistors; in the magnitude of 10 or less. It is clear that at that scale, each transistor in the design can be optimized by hand. In contrast, present day's technology creates entire microprocessors that primarily use sub-threshold transistors. That makes manual optimization impractical. Designing millions of such transistors is only feasible by using standard design tools and flows, preferably identical to those that have been utilized in the making of super-threshold design.

A. *Sub-threshold Leakages*

From the early days of the CMOS transistor manufacturing, its switching capability has been exploited by a wide range of applications. Simply applying a high or low voltage on the gate contact, the current flow between source and drain contact can be switched on or off, respectively. Initially, the off-state current was designed to be very small; in fact, early analytical models for the electrical behavior of CMOS transistors like the low-level SPICE models were even assuming a zero off-state current [2]. Commonly used equations for deriving the drain current were based on the famous quadratic transfer curve of a CMOS transistor. Beneath a certain gate-source voltage, called threshold voltage, the drain current was designed to be zero.

Certainly, this approximation has been a good one for some time especially when long channels and high supply voltages were utilised. A few years ago, the semiconductor industry began shrinking the devices to increase their density on a chip; this lead to a higher power dissipation since the active chip area stayed the same or was even increased to benefit from a higher system complexity. Also, the electric fields in the device were continually augmented because the voltage drops over the gate oxide and the channel remained the same while their sizes were scaled down, leading to reliability issues. Consequently, the supply voltage was scaled down to overcome these issues although the scaling method applied to the supply voltage remained more conservative than that of the device geometry [3, 4]. The device threshold voltage was scaled down, accordingly to maintain good driving capabilities. As a result, the off-state current increasingly became a bottleneck for decreasing the threshold voltage since it determines the power dissipation of a chip in its idle state. It could not be overlooked anymore and new physical models had to be implemented to correctly describe the device behaviour in the so-called sub-threshold or weak-inversion mode [5, 6, and 7].

Three distinct regimes can be identified for the operation of a CMOS transistor. Based on the inversion condition of the channel, these regimes are known as weak inversion, moderate inversion, and strong inversion. In the CMOS technology, two mechanisms are responsible for the flow of current; there are: drift and diffusion.

Under weak inversion regime, the channel surface potential is nearly constant across the channel and the flow of current is determined by diffusion of minority charge carriers due to a lateral concentration gradient. Under strong inversion regime, there exists a narrow layer of minority charge carriers at the channel surface and a lateral electric field which create a drift current. The moderate inversion regime is usually viewed as a transition region between weak and strong inversion regimes where both current flow mechanisms coincidentally exist [8].

In the weak-inversion (or sub-threshold) regime, the drain current is exponentially related to the gate-source voltage by the relation shown in (2) below [8].

$$\mathrm{I_{d,weak}} \propto \exp\left(\frac{\mathrm{V_{gs}}}{\mathrm{n}\cdot\mathrm{V_T}}\right) \tag{2}$$

Where V_T is the temperature voltage derived from:

$$\mathrm{V_T} = \frac{\mathrm{kT}}{\mathrm{q}} \tag{3}$$

Where k is the Boltzmann constant, T is the absolute temperature, and q the electron charge.

The sub-threshold slope factor q of a long-channel uniformly doped CMOS device can be determined using simple expressions for the gate and bulk capacitances C_g and C_b, respectively as shown in (4)

$$\mathrm{n} = 1 + \frac{\mathrm{C_b}}{\mathrm{C_g}} \tag{4}$$

With

$$\mathrm{C_b} = \frac{\epsilon_{\mathrm{si}}}{\mathrm{w_d}} \tag{5}$$

$$\mathrm{C_g} = \frac{\epsilon_{\mathrm{ox}}}{\mathrm{t_{ox}}} \tag{6}$$

In (6) and (7), ϵ_{ox} and ϵ_{si} represents the dielectric constants of the oxide and silicon, respectively while $\mathrm{w_d}$ is the depletion width under the channel, and $\mathrm{t_{ox}}$ is the gate oxide thickness.

The exponential sub-threshold pattern can be justified by the exponential reliance of the minority charge carrier density on the surface potential which, itself, is commensurate to the gate voltage. On a semi-logarithmic graph, the transfer ($I_d\ Vs\ V_g$) curve in the sub-threshold regime will thus be shown as a straight line.

The slope of such a line is known as the "sub-threshold slope". The inverse of this slope is known as "sub-threshold swing" S given in units (mV/decade) and can be derived from (2) above.

$$\mathrm{S} = \mathrm{n}\cdot\ \mathrm{V_T}\ \cdot \ln(10) \tag{7}$$

In (7), the factor $ln(10)$ is the outcome of the logarithmic scale with base 10 used to extract the sub-threshold swing defined earlier. Due to the bulk effect, the sub-threshold swing of a conventional CMOS transistor in bulk technology will often be more than a defined optimal value which is approximately equal to *60 mV/dec (*at room temperature), and which can be derived by setting n equal to 1 in (7) which means that the bulk effect is fully suppressed.

$$S_{opt} = V_T \cdot \ln(10) \quad (8)$$

In real life instances, n will always be larger than 1. Thus, the actual sub-threshold swing S will always be larger than S_{opt} depending on how accurately the channel surface potential can be controlled by the gate contact.

A small sub-threshold swing is always highly desirable since it enhances the ratio between the *on* and *off* currents. This necessitates that the bulk charge in the depletion region under the channel changes as little as possible when the gate voltage changes; therefore C_b should be small. Any additional bulk charge increases the voltage drop between the channel surface and the bulk contact, and therefore decreasing the effect of the gate voltage on the surface potential.

A small C_b can be imposed by a light bulk doping N_{bulk} under the channel since the depletion width in (5) is proportional to the inverse square root of the doping level:

$$w_d = \sqrt{\frac{2 \cdot \epsilon_{si} \cdot \emptyset}{q \cdot N_{bulk}}} \quad (9)$$

With $\emptyset$ being twice the bulk Fermi potential.

B. Sub-threshold Design challenges

In recent years, there has been a huge demand for ultra-low-power devices to continue guarantee longer battery lifetime. Clearly, sub-threshold circuits are highly suitable for applications where the concept of minimization of energy per operation is of capital importance. Ultimately, the benefits from ultra-low energy operation have carved out a significant market for sub-threshold circuits. Furthermore, sub-threshold circuits show exceptional sensitivity to process and temperature variations. Therefore, sub-threshold operating region has transformed the design of ultra-low-power systems and energy constrained devices a highly challenging design task as shown below:

1. ***Poor Transistor models:*** The transistor model forms the basis of everything in a microprocessor design. All of the simulations, abstractions and automation, the very process of design closure: they all rely on a highly accurate transistor model. The bulk of transistor modeling to date has focused on the "on" characteristics of the device with little attention paid to the "off" characteristic of the device. The entire region between 0 V and V_{th} typically does not get modelled as accurately, and so existing models are not suitable for sub-threshold design.
2. ***Logic Swing and Noise:*** The output response of a CMOS transistor in the sub-threshold region is difficult to analyze or describe; detecting it requires excellent sensitivity. In that region, currents change exponentially in response to changes in voltages, but they are remarkably small amount of currents. In addition, the ratio of "on" to "off" current is on the range of 1000, orders of magnitude less than what is usually observed in the super-threshold designs experience. As expected, external noise can easily interfere with clean operation.
3. ***Sensitivity to operating conditions:*** Sub-threshold designs are also a lot more affected by process and environmental variation compared to super-threshold designs. For instance, the current in a slow process corner can be between 10 and 100 times less than that of a nominal process. Assuming that the on/off current ratio described earlier is just on the order of a thousand, this cannot be neglected however. Changes in temperature provide a clear example of how environmental conditions create a challenge for the designer. The threshold voltage $V_{th}$is closely related to temperature, and I_{on} the "on" current depends exponentially on V_{th}. As a result, the "off" current at heighten temperature is similar in value to the "on" current at lowered temperature for an uncompensated circuit. Therefore sub-threshold circuit design requires extra effort to ascertain that the designed circuit will operate as expected under all specified operating conditions.
4. ***Logistical Challenges:*** Much of the manufacturing process is based on assumptions that are acceptable for super-threshold designs but fail for sub-threshold designs techniques. One such challenge can be identified in the testers used to validate the silicon during production. The parametric measurement units that test voltages and currents are designed to measure micro amps, not nano or Pico amps quantities. Even techniques as straightforward as device characterization has to be rethought simply because of the sensitivities issues associated with sub-threshold circuits which are completely foreign to super-threshold circuits. Classic characterization flows may not be accurate enough to prove that the circuits operate properly under all conceivable conditions.

The fundamental nature of such challenges, combined with the fact that few design engineers are skilled in dealing with sub-threshold issues, explains the reason for the difficulties associated with the commercializing of sub-threshold based circuits.

III. SUB-THRESHOLD DEVICE SIMULATION

A 2-D ATLAS simulator of Silvaco is used as a semiconductor simulator. Our design simulates the I_{ds} / V_{gs} characteristics of a thick film SOI MOSFET and from these

results extracts the threshold voltage and sub-threshold slope. These are two key parameters involved in the design of any SOI MOSFET. Thin film fully depleted SOI MOSFETs have been shown to achieve low threshold voltages and near ideal inverse sub-threshold slopes. This makes them ideal for low power operation.

The designed SOI device is a partially depleted device composed of a 0.2 micron layer of silicon (S_i) on a 0.4 micron silicon dioxide (S_iO_2) substrate. The device has a 17 nm thick gate oxide and a gate length of 1.0 microns. For simplicity there is no silicon below the back oxide. The device mesh, region specification and electrode definition are performed using the **mesh, region** and **electrode** statements at the start of the input file. The doping is added as simple analytical functions. The channel doping in this design is presumed a constant. Gaussian source and drain profiles are used. No LDD or spacer is considered in this case.

After the structure description, the interface statement is used to define fixed oxide charges on both silicon and silicon dioxide interfaces. Next the contact statement is used to specify the work-function on the poly-silicon gate. The model statement is used to specify a reasonable set of physical models for SOI simulation. In this case, concentration dependent mobility, SRH recombination, Auger recombination, band-gap narrowing, and parallel electric field dependent mobility are specified. After the initial solution, a negative gate voltage is applied followed by solutions at drain biases of 0.05 and 0.1 volts are obtained. The resultant plot is shown in Fig. 1 below.

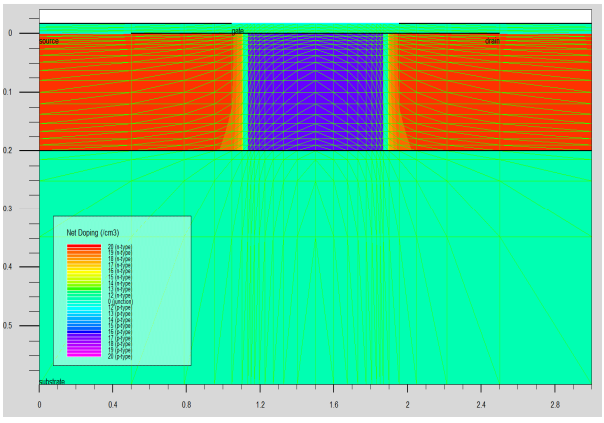

Figure 1. The Designed Structure

Next, the log statement is used to specify a file for collection of the I_{ds}/V_{gs} characteristics of the SOI device. These characteristics are captured with the following solve statement where the gate bias is ramped in 0.1 volt increments from -0.2 volts up to 1.5 volt. After the voltages have been solved extract statements are used to find the threshold voltage and the sub-threshold slope of the SOI MOSFET. Finally, the resultant I_{ds}/V_{gs} curve is plotted using TonyPlot.

IV. Results and Discussion

The electrical characteristics of the device were simulated using the ATLAS module of the Silvaco simulation tool. The tool enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time domain responses of all semiconductor based technologies in two and three dimensions.

A. Drain Current Versus Gate Voltage (I_d Vs V_{gs})

To plot the I_d Vs V_{gs} graph, the drain voltage must be constant in order in order to have a DC bias at drain electrode. The gate voltage is ramped from zero to a final value in steps. Also, the source electrode is grounded. In this project, the gate voltage is increased from 0V to 3.0V in steps of +0.1V. The drain is biased at two different values, 0.1V and 1.0V. These two values indicate a low voltage and high voltage bias of the transistor. Clearly, both of the NMOS devices are biased with positive value. This is because electrons flow from source to drain terminal to produce drain current which flows in opposite direction with the electrons flow. The I_d Vs V_{gs} characteristics of the fabricated device are shown in Fig. 2 below.

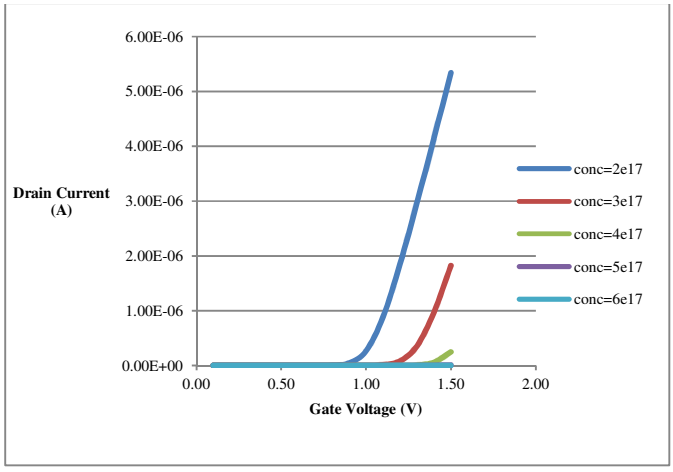

Figure 2. Gate voltage Vs drain voltage at different bulk doping levels

Fig. 2 shows series of transfer curves of a quarter-micron MOS transistor for different bulk doping levels. There exists a doping for which the sub-threshold swing has an optimum value. For higher doping levels the bulk effect becomes stronger like described above. Table1 below summarizes the values obtained for both threshold and sub-threshold voltage for different doping levels

TABLE I. THRESHOLD AND SUB-THRESHOLD VALUES AT DIFFERENT CONCENTRATION LEVELS

Doping Concentration (cm^{-3})	*Threshold voltage (V)*	*Sub-threshold voltage (V/decade)*
2.00E+17	1.00232	0.107718
3.00E+17	1.23583	0.11485
4.00E+17	1.31909	0.120773
5.00E+17	1.32881	0.114239
6.00E+17	1.3245	0.129118

The threshold voltage dependency on doping density is illustrated as follows:

$$V_T = V_{FB} + 2\emptyset_F + \frac{\sqrt{2\varepsilon_s q N_A (2\emptyset_F + V_{SB})}}{C_{ox}} \quad (10)$$

Where the flat band voltage V_{FB} is given by:

$$V_{FB} = \Phi_{MS} - \frac{Q_F}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{x_{ox}} \rho_{ox}(x)\, dx \quad (11)$$

With

$$\Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - \left(x + \frac{E_g}{2q} + \emptyset_F\right) \quad (12)$$

And

$$\emptyset_F = V_T \ln\left(\frac{N_a}{n_i}\right) \text{ p-substrate} \quad (13)$$

The threshold voltage of a *p*-type MOSFET with an *n*-type substrate is computed using the following equations:

$$V_T = V_{FB} - 2\emptyset_F - \frac{\sqrt{2\varepsilon_s q N_A (2\emptyset_F - V_{SB})}}{C_{ox}}$$

Where the flat band voltage V_{FB} is given by:

$$V_{FB} = \Phi_{MS} - \frac{Q_F}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{x_{ox}} \rho_{ox}(x)\, dx \quad (14)$$

With

$$\Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - \left(x + \frac{E_g}{2q} + \emptyset_F\right) \quad (15)$$

And

$$|\emptyset_F| = V_T \ln\left(\frac{N_d}{n_i}\right) \text{ n-substrate}$$

The threshold voltage of both types of devices is slightly negative at low doping densities and differs by 4 times the absolute value of the bulk potential. The threshold of n-MOSFETs increases with doping while the threshold of p-MOSFETs decreases with doping in the same way. A variation of the flat-band voltage due to oxide charge will cause a reduction of both threshold voltages if the charge is positive and an increase if the charge is negative.

CONCLUSION

The use of sub-threshold techniques can be a powerful way to create circuits that consume dramatically less energy than those built using standard design practices and at the same time emitting less leakage currents. It's a fact that sub-threshold design is difficult. But, given the right experience and diligence, it is a solvable problem. The results of these efforts are circuits that provide the same functions as more traditional ones using a fraction of the energy. There is no compromise in performance, robustness, or reliability. It was shown that chips can operate alongside their traditional counterparts with no externally-visible difference except for the amount of energy required to drive them. They can provide important energy savings to designers building energy-efficient systems. Because of the fundamental nature of these innovations, sub-threshold design techniques can be applied to virtually any type of IC device.

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