OPERATING STRATEGIES AND CAPACITOR VOLTAGE BALANCE STRATEGIES FOR A CASCADED "3-5-9" HYBRID INVERTER FOR GRID INTERFACE APPLICATION

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Abstract

The paper presents a novel phase shifted SPWM control scheme for cascading two cells to form a "3-5-9" hybrid inverter with improved harmonic suppression. Modeling of the hybrid inverter from first principle is introduced and a standard control law is derived for further analysis and development of the model. A new balance circuit for DC link voltage control is designed and tested. Combined with individual voltage control, a complete control scheme is developed. Detailed MATLAB simulation and experimental results are obtained for further validation of the adopted topology and the control scheme.

Key Words

3-5-9 Cascaded hybrid inverter, DC link voltage balance, phase shifted PWM control

Nomenclature

a, b	two NPC/H-Bridge inverter legs
C_{f}	output filter capacitance
C_i	DC link capacitance for each NPC/H-Bridge inverter ($C_1 = C_2$)
$V_{\mathrm{dc}i}$	DC bus voltage of the ith NPC/H-Bridge inverter
L_{f1}	inverter-side filter inductance
L_{f2}	grid-side filter inductance
m_{a}	amplitude modulation index
m	number of voltage levels
R_{f1}	inverter-side filter resistance
R_{f2}	grid-side filter resistance
N	number of series connected NPC/H-Bridge inverter
V_i	upper and lower DC link bus voltage for each NPC/H-Bridge inverter ($V_1 = V_2$)
$V_{\mathrm{s\_}x}$	grid voltage
x	phases a, b and c
$K(t)$	switching function
δ_{p}	duty cycle
$I_{\mathrm{f\_}x}$	inverter current
$I_{\mathrm{s\_}x}$	grid current
j	series connected NPC/H-Bridges ($j = 1, \ldots, N$)
D	quiescent operating point of δ
J_n	nth-order Bessel function of the first kind
M	modulation index

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1. Introduction

Increasing restrictive regulations on power quality have significantly stimulated the development of power quality mitigation equipments. For high-power grid connected systems, the classical 2-level or 3-level converter topology is insufficient due to the rating limitations imposed by the power semiconductors [1], [2]. Hence considerable attention has been focused on multilevel inverter topologies.

Multilevel converters offer several advantages compared to their conventional counterparts [3]–[8]. By synthesizing the AC output terminal voltage from several voltage levels, staircase waveforms can be produced, which in their turn approach the sinusoidal waveform with low harmonic distortion, thus reducing filter requirements. However, the several sources on the DC side of the converter make multilevel technology difficult to control by the need to balance the several DC voltages.

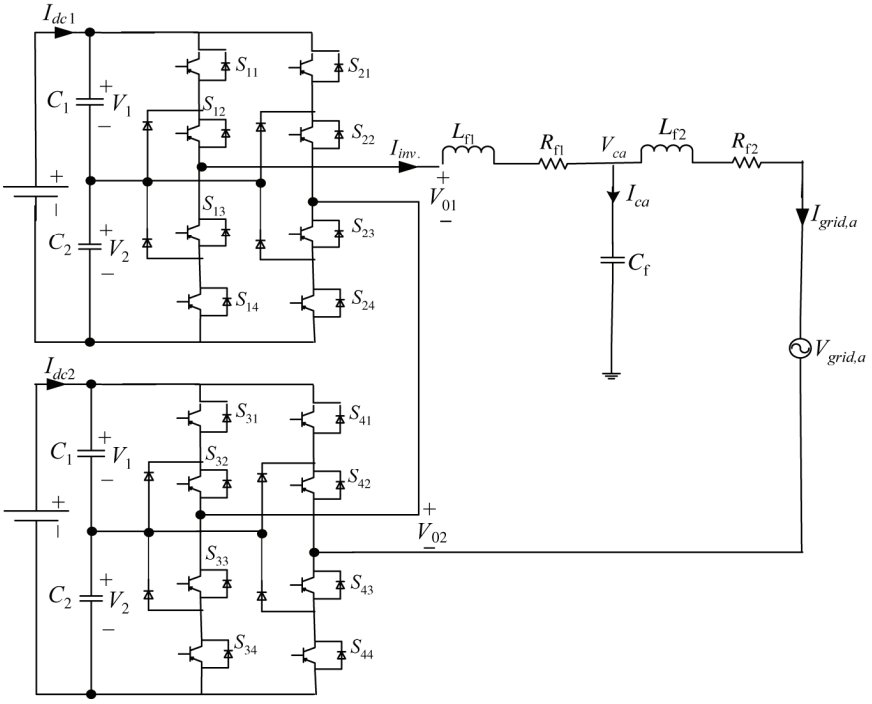


Figure 1. Schematic diagram of the proposed grid interface system based on hybrid inverter.

Past research on this hybrid converter has concentrated on modeling and control of a one cell of a 5-level hybrid inverter model without cascading the cells [9], [10]; this fails to address the principle of realizing a general cascaded N-level hybrid model. Because of the modularity of the model, two cells have been chosen to provide the technology of cascading of the model.

A new and improved phase shifted SPWM control algorithm for hybrid inverter model is proposed. Investigation of its superior harmonic suppression is verified using double Fourier analysis. To enhance the modularity and switching flexibility of the cascaded hybrid model, a standard control law is developed.

Finally, a controller is designed for grid interface application of the inverter. The components of the controller are grid voltage regulation and capacitor DC link voltage control. It is shown that from the new balance circuit designed, DC balance technique developed can be used for any number of voltage levels which has been a problem to achieve especially for converters with higher levels (more than five).

2. The "3-5-9" Grid Connected Inverter Model

2.1 Main System Configuration

Figure 1 shows a "3-5-9" hybrid topology connected to the grid, only one phase of the model is shown. The system consists of DC capacitors, N-inverter cells, LCL filters, and the grid. The output waveform is synthesized by adding each of converter output voltage. Assuming that each dc source has the same dc voltage, $V_{\rm dc}$. Based on switch combinations, five voltage levels can be synthesized from each cell viz.$+2V_{\rm dc}$, $+V_{\rm dc}$, 0, $-V_{\rm dc}$ and $-2V_{\rm dc}$. This implies that for an m-level cascaded hybrid model, the number of cells connected in series is determined as:

$$N = \frac{m-1}{4} \tag{1}$$

The "3-5-9" hybrid topology means the inverter has been decomposed into four legs and each leg is modulated independently giving 3-level/leg. The output of the two legs added together gives 5-level and the two 5-level cells cascaded together with proper phase shifted PWM control technique will realize a 9-level output. Hence the output voltage of the two cells V_{an} is the combination of two cells given by (2), where n is the node between points S_{42} and S_{43}:

$$V_{an} = V_{01} + V_{02} \tag{2}$$

2.2 System Operation

One cell of the model as shown in Fig. 2 is used for analysis. To prevent the top and bottom power switched in each inverter leg from conducting at the same time, the constraints of power switches can be expressed as:

$$S_{i1} + S_{i3} = 1; \quad S_{i2} + S_{i4} = 1 \tag{3}$$

where $i = 1, 2$. Let's define the switch operator as $T_1 = S_{11}$ & S_{12}; $T_2 = S_{13}$ & S_{14}; $T_3 = S_{21}$ & S_{22}; $T_4 = S_{23}$ & S_{24}.

The four valid expressions are given by:

$$T_1 = \begin{cases} 1 & \text{if both } S_{11} \text{ \& } S_{12} \text{ are ON} \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

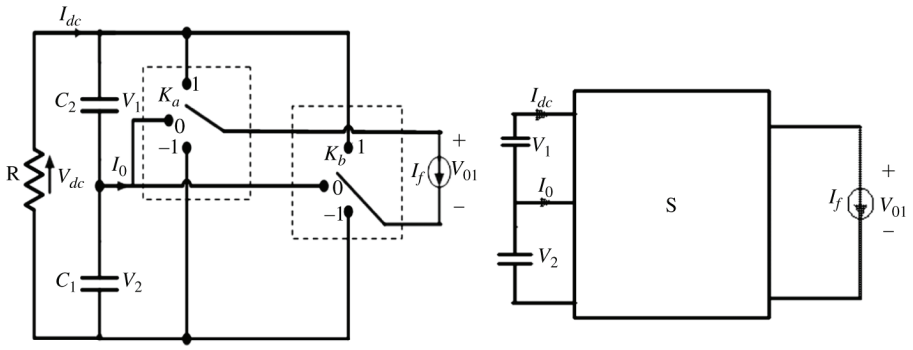


Figure 2. Simplified representation of a one cell of the model.

Table 1
Switching States and Corresponding Voltage(s) for One Cell of the Hybrid Inverter

K_a	K_b	T_1	T_2	S_{12}	T_3	T_4	S_{21}	V_a	V_b	V_{01}	Mode
1	−1	1	0	1	0	1	0	V_1	$-V_2$	V_1+V_2	1
0	−1	0	0	1	0	1	0	0	$-V_2$	V_2	2
−1	0	0	1	0	0	0	1	0	V_2	$-V_2$	3
1	0	1	0	1	0	0	1	V_1	0	V_1	4
0	1	0	0	1	1	0	1	$-V_1$	0	$-V_1$	5
1	1	1	0	1	1	0	1	$-V_1$	$-V_2$	0	6
−1	−1	0	1	1	0	1	1	V_1	V_2	0	7
−1	−1	0	1	0	1	0	1	$-V_1$	V_2	$-V_1-V_2$	8

$$T_2 = \begin{cases} 1 & \text{if both } S_{13} \text{ \& } S_{14} \text{ are ON} \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

$$T_3 = \begin{cases} 1 & \text{if both } S_{21} \text{ \& } S_{22} \text{ are ON} \\ 0 & \text{otherwise} \end{cases} \tag{6}$$

$$T_4 = \begin{cases} 1 & \text{if both } S_{23} \text{ \& } S_{24} \text{ are ON} \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

From Fig. 2 taking two legs for each cell to be a and b, the equivalent switching function for each NPC-leg is given by:

$$K_a = \begin{cases} 1 & \text{if } T_1 = 1 \\ 0 & \text{if } S_{12} = 1\,; \\ -1 & \text{if } T_2 = 1 \end{cases} \quad K_b = \begin{cases} 1 & \text{if } T_3 = 1 \\ 0 & \text{if } S_{22} = 1 \\ -1 & \text{if } T_4 = 1 \end{cases} \tag{8}$$

Assuming that $V_1 = V_2 = V$, the voltage V_{01} generated by the inverter can be expressed as:

$$V_{01} = V_a + V_b \tag{9}$$

For leg 'a' of the cell which gives V_a, the voltage is represented as:

$$V_a = K_a\left(\frac{K_a+1}{2}\right)V_1 - K_a\left(\frac{K_a-1}{2}\right)V_2 \tag{10}$$

Similarly for leg 'b', the expression is given by:

$$V_b = K_b\left(\frac{K_b+1}{2}\right)V_1 - K_b\left(\frac{K_b-1}{2}\right)V_2 \tag{11}$$

Using (3)–(7), a switching state and corresponding voltage output V_{01} for one cell can be generated as shown in Table 1. This clearly indicates that there are eight valid switching for a 5-level hybrid inverter model. From (9), the voltage output for one cell of the model can be deduced as:

$$V_{01} = \frac{K_a - K_b}{2}(V_1 + V_2) + \frac{K_a^2 - K_b^2}{2}(V_1 - V_2) \tag{12}$$

2.3 Mathematical Analysis

This section analyses eight valid operating modes of one cell of the proposed topology and hence validates the principle of operation of the model covered in Section 2.2. The following assumptions are made for deriving the mathematical model of the cascaded H-bridge inverters.

- All components (power switches and capacitors) are ideal.
- Switches being ideal, dead times are zero.
- The DC link capacitors V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} have the same capacitance.
- The reference phase voltage is assumed to be a constant value during one switching period.

There are eight valid operating modes as shown in Table 1. In mode 1, the power switches S_{11} & S_{12} and S_{23} & S_{24} are turned on to supply voltage at the output of first NPC/H-bridge cell that is equal to $V_{01} = V_1 + V_2$. The capacitors C_1 and C_2 are discharged as they supply power to the utility. Mode 1 from Fig. 2 can be obtained by connecting both K_a and K_b to 1.

The differential equations describing the dynamics of the coupling inductor between the cascaded hybrid inverter and the grid of the model shown in Fig. 1 can be derived as:

$$\begin{cases} L_{\mathrm{f1}}\dfrac{\mathrm{d}i_{\mathrm{f}}}{\mathrm{d}t} = -R_{\mathrm{f1}}I_{\mathrm{f}} + V_1 + V_2 - V_{\mathrm{cm}} \\ L_{\mathrm{f2}}\dfrac{\mathrm{d}i_{\mathrm{s}}}{\mathrm{d}t} = V_{\mathrm{C}} - R_{\mathrm{f2}}I_{\mathrm{g}} - V_{\mathrm{s}} \\ C\dfrac{\mathrm{d}V_{\mathrm{cm}}}{\mathrm{d}t} = I_{\mathrm{f}} - I_{\mathrm{s}} \\ C_1\dfrac{\mathrm{d}V_1}{\mathrm{d}t} = I_{\mathrm{f}} + \left(\dfrac{V_1}{R} + \dfrac{V_2}{R}\right) \\ C_2\dfrac{\mathrm{d}V_2}{\mathrm{d}t} = -I_{\mathrm{f}} + \left(\dfrac{V_1}{R} + \dfrac{V_2}{R}\right) \end{cases} \tag{13}$$

Equation (13) can be written in the format of:

$$Z\dot{x} = Ax + B \tag{14}$$

Capacitor current, inverter current and utility line current and DC link capacitors are taken as state variables:

$$x = \begin{bmatrix} i_{fx} & i_{sx} & V_c & V_1 & V_2 \end{bmatrix}^{\mathrm{T}} \tag{15}$$

$$B = \begin{bmatrix} 0 & -V_s & 0 & 0 & 0 \end{bmatrix}^{\mathrm{T}} \tag{16}$$

$$Z = \begin{bmatrix} L_{\mathrm{f1}} & 0 & 0 & 0 & 0 \\ 0 & L_{\mathrm{f2}} & 1 & 0 & 0 \\ 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & 0 & C_2 \end{bmatrix} \tag{17}$$

Matrix A depends on each operating mode as such:

$$A_1 = \begin{bmatrix} -R_{\mathrm{f1}} & 0 & -1 & 0 & 1 \\ 0 & -R_{\mathrm{f2}} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & R^{-1} & R^{-1} \\ -1 & 0 & 0 & R^{-1} & R^{-1} \end{bmatrix} \quad (\text{for } V_{01} = +V_2) \tag{18}$$

$$A_5 = A_1^{\mathrm{T}} \quad (\text{for } V_{01} = -V_2) \tag{19}$$

$$A_2 = \begin{bmatrix} -R_{\mathrm{f1}} & 0 & -1 & 1 & 0 \\ 0 & -R_{\mathrm{f2}} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & R^{-1} & R^{-1} \\ 0 & 0 & 0 & R^{-1} & R^{-1} \end{bmatrix} \quad (\text{for } V_{01} = +V_1) \tag{20}$$

$$A_6 = A_2^{\mathrm{T}} \quad (\text{for } V_{01} = -V_1) \tag{21}$$

$$A_4 = A_3^{\mathrm{T}} \tag{22}$$

$$A_4 = \begin{bmatrix} -R_{\mathrm{f1}} & 0 & -1 & -1 & -1 \\ 0 & -R_{\mathrm{f2}} & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (\text{for } V_{01} = 0) \tag{23}$$

Then the simplified 'A' matrix given in (24) validates the 5-level topology.

$$A' = \begin{bmatrix} -R_{\mathrm{f1}} & 0 & -k & k \\ 0 & -R_{\mathrm{f2}} & k & 0 \\ k & -1 & 0 & 0 \\ -k & 0 & 0 & 0 \end{bmatrix} \tag{24}$$

where k depends on the operating mode and can take five different values: 1, 0.5, 0, −0.5, and 1.

For a three phase system, V_{s} is replaced by $V_{\mathrm{s}}\cos(\omega_{\mathrm{o}}t)$, $V_{\mathrm{s}}\cos(\omega_{\mathrm{o}}t - 2\pi/3)$ and $V_{\mathrm{s}}\cos(\omega_{\mathrm{o}}t + 2\pi/3)$; similarly the Z, A and B matrices are expanded accordingly to three phases, where V_{s} is the grid voltage.

3. Open Loop Control Strategy for the Model

3.1 Theoretical Harmonic Analysis of a Cascaded "3-5-9" Hybrid Inverter Model

Based on the principle of double Fourier integral, the first modulation between triangular carrier v_{cr1} and the positive sinusoidal waveform realizes a naturally sampled PMW output $V_{\mathrm{p}}(t)$ as shown in Fig. 3(a). This is validated by (25). Using v_{cr2} which is the same carrier but displaced by minus unity, the naturally sampled PWM output V_{n} (negative leg) is as given in (26).

$$V_{\mathrm{p}}(t) = \begin{cases} \dfrac{V_{\mathrm{dc1}}}{2} + \dfrac{V_{\mathrm{dc1}}M}{2}\cos\,\omega_{\mathrm{s}}t + \dfrac{2V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=1}^{\infty}\frac{1}{m}J_0\Big(m\frac{\pi}{2}M\Big) \\ \sin m\dfrac{\pi}{2}\cos\omega_{\mathrm{s}}t + \dfrac{2V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ n\mp 0}}^{\infty}\frac{1}{m}J_n \\ \Big(m\dfrac{\pi}{2}M\Big)\sin(m+n)\dfrac{\pi}{2}\cos(n\omega_{\mathrm{c}}t + n\omega_{\mathrm{s}}t) \end{cases} \tag{25}$$

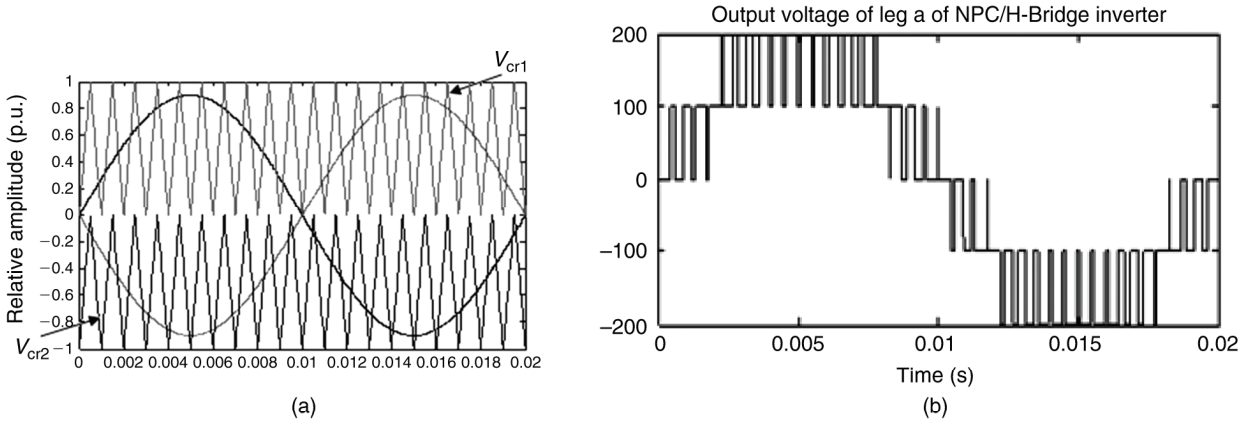


Figure 3. (a) PWM proposed scheme and (b) output voltage waveform for one "3-5" cell inverter model.

$$V_{\mathrm{n}}(t)=\begin{cases}\dfrac{V_{\mathrm{dc1}}}{2}-\dfrac{V_{\mathrm{dc1}}M}{2}\cos\omega_{\mathrm{s}}t-\dfrac{2V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=1}^{\infty}\frac{1}{m}J_0\left(m\frac{\pi}{2}M\right)\\ \sin m\dfrac{\pi}{2}\cos\omega_{\mathrm{s}}t+\dfrac{2V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty\\ n\mp 0}}^{\infty}\frac{1}{m}J_n\\ \left(m\dfrac{\pi}{2}M\right)\sin(m+n)\dfrac{\pi}{2}\cos(n\omega_{\mathrm{c}}t+n\omega_{\mathrm{s}}t)\end{cases}\tag{26}$$

The output of leg 'a' is given by $V_{\mathrm{a}}(t)=V_{\mathrm{p}}(t)-V_{\mathrm{n}}(t)$ which is:

$$V_{\mathrm{a}}(t)=\begin{cases}V_{\mathrm{dc1}}\cos(\omega_{\mathrm{s}}t)+\dfrac{4V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=2,4,6}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{1}{m}J_n\\ \left(m\dfrac{\pi}{2}M\right)\cos(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{s}}t)\end{cases}\tag{27}$$

The output of leg 'b' is realized by replacing ω_{s} with $\omega_{\mathrm{s}}+\pi$ and using v_{cr2} which is same as phase displacing v_{cr1} by minus unity which gives:

$$V_{\mathrm{b}}(t)=\begin{cases}-V_{\mathrm{dc1}}\cos(\omega_{\mathrm{s}}t)-\dfrac{4V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=2,4,6}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{(-1)^{m+n}}{m}J_n\\ \left(m\dfrac{\pi}{2}M\right)\cos(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{s}}t)\end{cases}\tag{28}$$

From (27) and (28), it can be clearly deduced that odd carrier harmonics and even sideband harmonics around even carrier harmonic orders are completely eliminated. Five-level obtained by taking the differential output between the two legs is given in (29). Similarly the output between the other two legs of the second cell of the hybrid model is achieved by replacing ω_{s} with $\omega_{\mathrm{s}}+\pi$ and ω_{c} with $\omega_{\mathrm{c}}+\pi/4$ which gives another 5-level inverter for equation given by (30).

$$V_{01}(t)=\begin{cases}2V_{\mathrm{dc1}}\cos(\omega_{\mathrm{s}}t)+\dfrac{8V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=4,8,12}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{1}{m}J_n\\ \left(m\dfrac{\pi}{2}M\right)\cos(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{s}}t)\end{cases}\tag{29}$$

$$V_{02}(t)=\begin{cases}-2V_{\mathrm{dc1}}\cos(\omega_{\mathrm{s}}t)-\dfrac{8V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=4,8,12}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{(-1)^{(m/4)+n}}{m}J_n\\ \left(m\dfrac{\pi}{2}M\right)\cos(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{s}}t)\end{cases}\tag{30}$$

Equations (29) and (30) clearly show that for 5-level inverter, the proposed control strategy has achieved; Suppression of carrier harmonics to multiples of four; Elimination of even side harmonics around multiples of four carrier harmonics and Multiples of four carrier harmonics. Finally, the output for a 9-level is achieved differentiating the output voltage between the two cells of the 5-level cells and this is given by (31). Given that for one cell ($m=4$) and two cells ($m=8$), it can be concluded that for a cascaded N-level inverter the carrier harmonic order is pushed up by factor of $4N$ where N is the number of cascaded hybrid inverters. The output voltages and spectral waveforms to confirm the validation of the control strategy using this approach of double Fourier transform will be discussed later.

$$V_{an}(t)=\begin{cases}4V_{\mathrm{dc1}}\cos(\omega_{\mathrm{s}}t)+\dfrac{8V_{\mathrm{dc1}}}{\pi}\displaystyle\sum_{m=8,16,24}^{\infty}\sum_{n=\pm1\pm3\pm5}^{\infty}\frac{1}{m}J_n\\ \left(m\dfrac{\pi}{2}M\right)\cos(m\omega_{\mathrm{c}}t+n\omega_{\mathrm{s}}t)\end{cases}\tag{31}$$

3.2 MATLAB Simulation for the Proposed Cascaded Model

The above section has illustrated in general the switching technique for one cell of the cascaded inverter model, because of the modularity of the model, two cells will be considered for modulation and analysis in this section. For the two cells, an improved strategy for realizing 9-level output is proposed in this paper. The article uses the principle of decomposition where each leg is treated independently and gives a 3-level output [11].

Positive and negative legs are connected together back to back and they share the same voltage source V_{dc}. PD

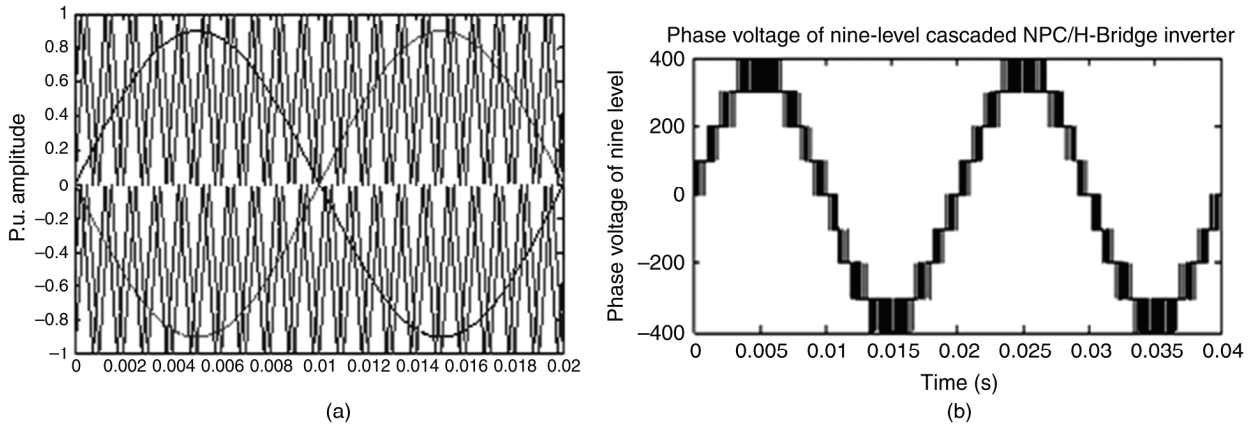


Figure 4. (a) PWM proposed scheme and (b) output voltage waveform for "3-5-9" inverter.

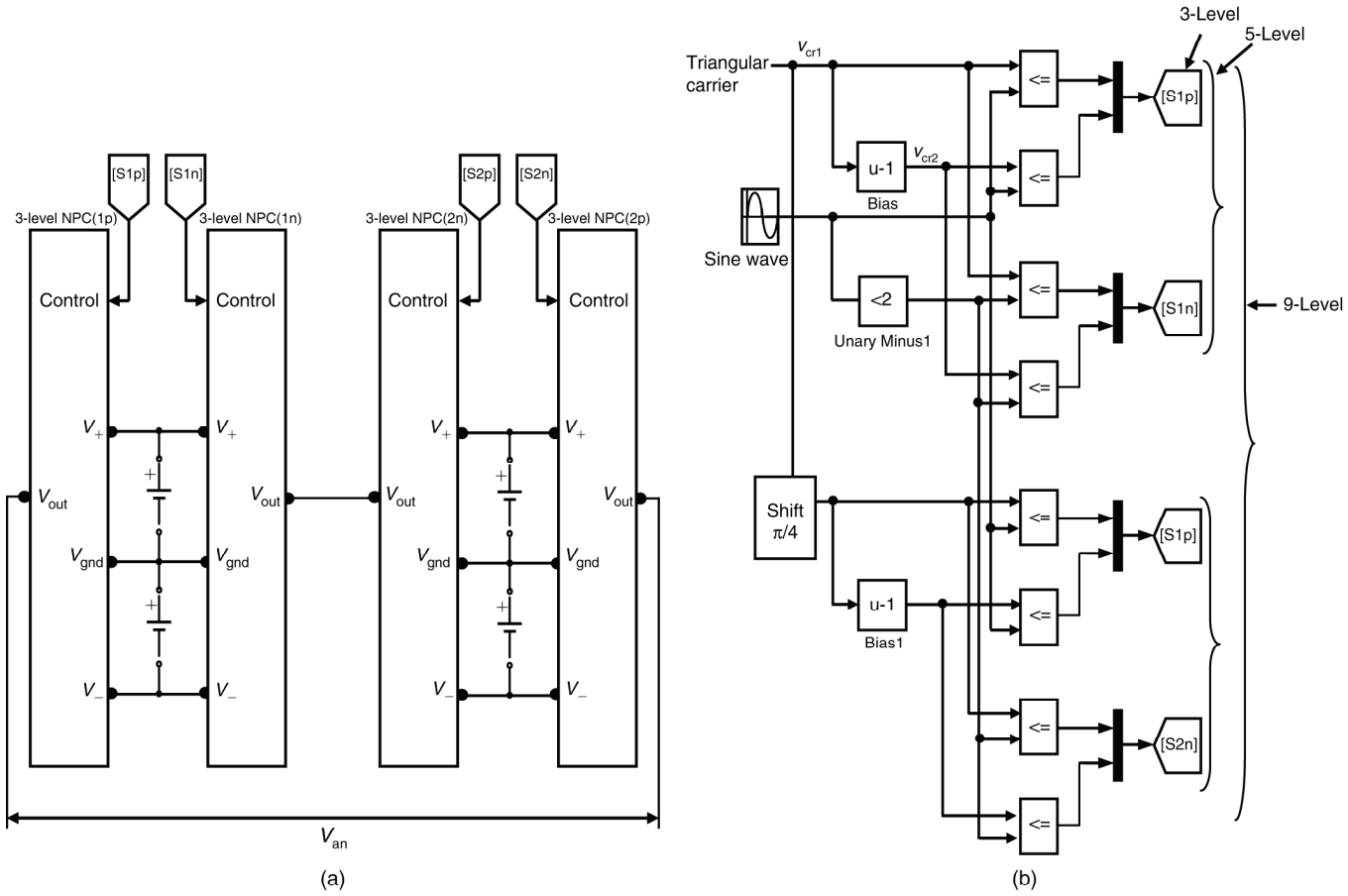


Figure 5. (a) Four legs of a nine-level cascaded "3-5-9" hybrid inverter and (b) control strategy for a cascaded "3-5-9" hybrid inverter.

modulation is used for achieving 3-level output [12]. To achieve a 5-level PWM output, two triangular carriers V_{cr1} and V_{cr2} in phase but vertically disposed and modulating wave phase shifted by π are used. The multilevel converter model is modulated using phase shifted PWM technique as illustrated in Fig. 3 for the two inverter cells. Finally, a 9-level PWM output is achieved by using the same two carriers but phase shifted by $\pi/4$ and modulating wave phase shifted by π as shown in Fig. 4. The model was designed and simulated in MATLAB. The operating conditions for the model are: $f_m = 50\,\text{Hz}$, $m_f = 20$ for a 5-level output and $m_a = 0.9$. The device switching frequency is found from $f_{sw,dev} = (m_f/2) \cdot f_m = 500\,\text{Hz}$.

The control strategy has two advantages as compared to multicarrier PWM approach [13]. First for "3-5-N"-level cascaded hybrid inverter model, we can use a switching frequency of $4N$ times less to achieve the same spectrum as multicarrier approach. This has an advantage of reducing the switching losses, which is an important feature in high-power application. Second, the multicarrier PWM approach requires eight carriers to achieve 9-level output, but the proposed control strategy requires only one carrier phase shifted by $(N-1)\pi/4$, where N is the number of series connected inverter cells.

MATLAB model shown in Fig. 5(a) was designed from schematic diagram shown in Fig. 1. The control strategy

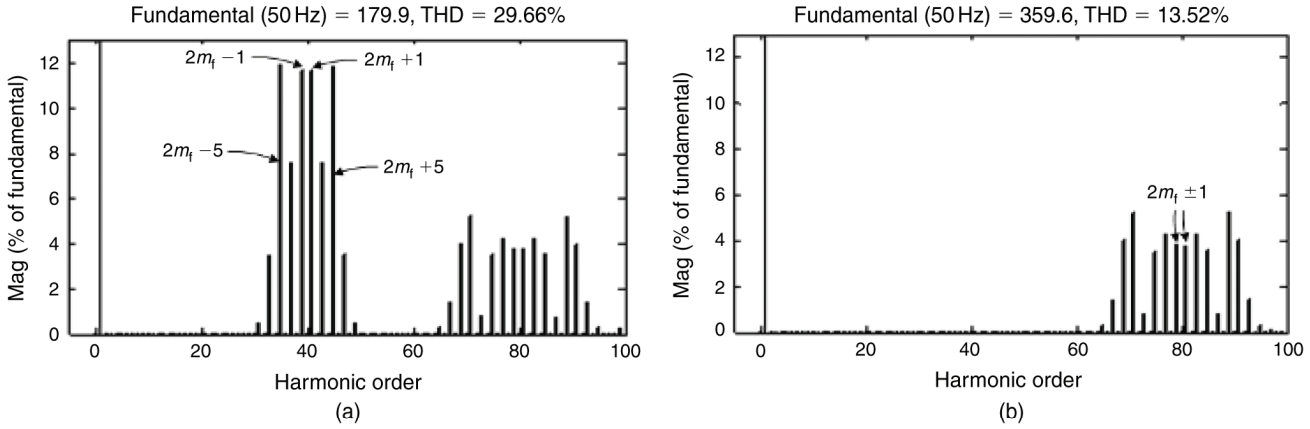


Figure 6. Output voltage spectrum for (a) "3-5" and (b) "3-5-9" inverters.

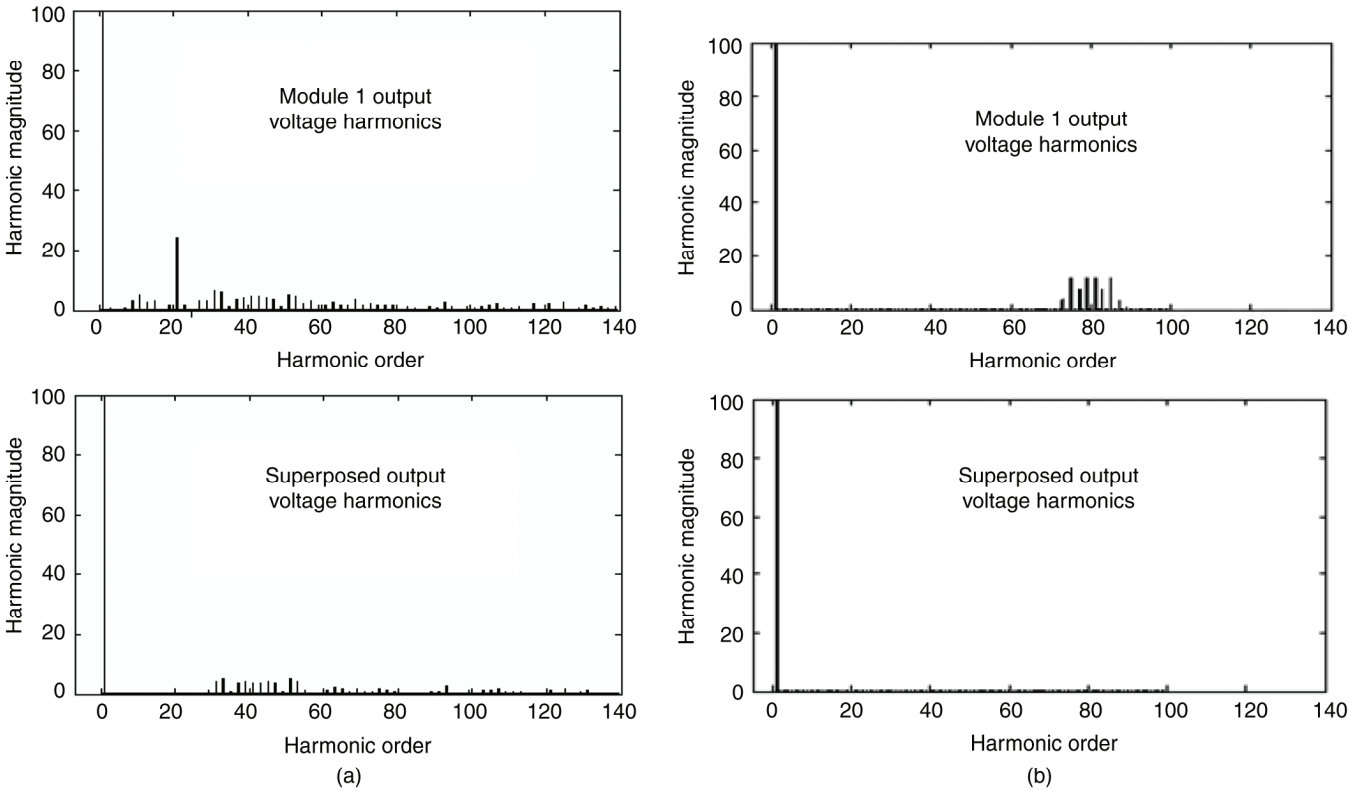


Figure 7. Voltage spectra for conventional and proposed multi-carrier PWM.

to minimize harmonics was designed and developed in MATLAB as shown in Fig. 5(b) [14]. It is assumed that the dc voltage input for each module is $V_{dc1} = V_{dc2} = 100\,\text{V}$.

3.3 Spectral Analysis of the Hybrid Model

Figure 6(a) shows the simulated spectral waveform for the phase voltage V_{01} of the one cell of the PWM inverter. The waveform V_{01} is a five voltage levels, whose harmonics appear as sidebands centered on $2m_f$ and its multiples such as $4m_f$, and $6m_f$. This simulation verifies analytical equation (29) which shows that the phase voltage does not contain harmonics lower than the 31st, but has odd order harmonics (*i.e.* $n = \pm 1 \pm 3 \pm 5$) centered on $m = 4$, 8, 12. Figures 9 and 10 show 5-level NPC/H-Bridge inverter output for device inverter switching frequency of 1000 and 200 Hz respectively.

Figure 6(b) shows the spectral waveform of the phase voltage of a cascaded "3-5-9" level PWM inverter. It has sidebands around $4m_f$ and its multiples, this shows further suppression in harmonic content.

This topology operates under the condition of $f_m = 50\,\text{Hz}$, $m_f = 40$ and $m_a = 0.9$. The device switching frequency is found from $f_{sw,dev} = (m_f/4) \cdot f_m = 500\,\text{Hz}$. This simulation verifies analytical equation (31) which shows that the phase voltage does not contain harmonics lower than the 67th, but has odd order harmonics (*i.e.* $n = \pm 1 \pm 3 \pm 5$) centered on $M = 8, 16, 32$.

3.4 Comparison of the MATLAB Simulation Results of the Two PWM Control Methods

To clearly investigate the superiority of the model under the proposed PWM control technique, simulated results for the proposed phase shifted PWM technique were compared with those of conventional PWM phase shifted approach under the same operating conditions. From Fig. 7(a) and (b), it is clearly shown there is further harmonic suppression for the proposed PWM technique [15].

4. Cascaded "3-5-9" Inverter Controller Design for Grid Application

4.1 Control Scheme

A whole control block diagram of the proposed scheme is shown in Fig. 8. The control strategies to be tested are the grid synchronization using the phase locked loop (PLL); the current reference scheme; the voltage balance technique for lower and upper DC capacitors, average voltage balance between the cells and robustness of the DC voltage balance technique under changing loads. Finally, robustness of the controller is tested under varying loads and DC source. As illustrated in Fig. 8, the phase angles are detected from the grid voltage V_{sa} to perform PLL and the sine and cosine terms which are synchronized with the grid voltage are achieved. The obtained current is used as grid reference current for d-channel.

For the grid current control, there are two main control loops, i_{sd} for the active power control and i_{sq} for the reactive power control. The tuning of the compensator is made for only one loop assuming that both of them have the same dynamics.

By tracking current signal using current reference generated by the phase voltage of the grid, grid voltage and current are in phase. The aim is to ensure maximum power injection to the grid at unit power factor.

4.2 Capacitor Voltage Balance Strategies

A lot of research of research has been done on balancing of DC capacitor voltage for multilevel converter with little success in converters with higher levels (more than five) [16], [17]. The general problem in the development of multilevel converter is the voltage unbalance of the dc link capacitors. This unbalance distorts the waveforms of the output voltage and current. In this paper, a new balance circuit is designed and developed as a DC-capacitor voltage balance scheme as shown in Fig. 9. It is an ideal balance technique for the proposed topology because it can be easily used to balance capacitor voltage for N number of cells. This implies that the technique can easily be applied to control DC capacitor voltage for output levels of more than five which has been a problem to achieve especially for diode clamped multilevel.

5. Simulation Analysis for a Cascaded "3-5-9" Level Inverter

To verify the performance of the proposed control technique, several simulations have been carried out using MATLAB-Simulink. The example shown in this paper is a 9-level cascaded hybrid inverter, based on two series connected hybrid inverter models connected to the grid through a coupling inductance L_{f} as shown in Fig. 1. Table 2(a) and (b) shows the values used to carry out the simulation. The selection of the type of inductors and capacitors is a compromise between performance, size and cost [18]. The equations describing the operation of voltage and current control loops have been already developed in [19] and adopted here for the sake of completeness.

5.1 Simulation Results

The validity and robustness of the proposed control scheme was tested by carrying out several simulations under various environmental conditions. First the model was simulated under normal condition with constant resistive load. Figure 10 shows the grid current and voltage operating under normal condition; it can be seen that a sinusoidal grid voltage that is in phase with grid current was achieved by adopting the proposed feedback control technique. This means maximum active power injection into the grid at unit power factor.

For the voltage balance circuit, Fig. 11(i)(a) and (b) shows the upper and lower DC link capacitor voltages without the balance circuit first at $m_{\mathrm{a}} = 0.8$, then m_{a} is reduced to 0.5 and (c) the capacitor voltages with the balance circuit at both $m_{\mathrm{a}} = 0.5$ and 0.8. The model is switched with a steady state load of 200 kW at $t = 0.7$ s. The two capacitor voltages are balanced clearly indicating that the proposed voltage balance works well in the modulation index range of 0.8–0.5.

The voltage unbalance was made by using two different resistances at the upper and lower capacitors. The resistive load of the upper capacitors changes from 500Ω to 10Ω while the lower one changes from 500Ω to 50Ω at $t = 2$ s.

Fig. 11(ii)(a)–(c) shows the DC link voltage of the upper and lower DC link voltage, individual cell DC voltage and the two DC link voltages for the two cells respectively with the conventional control scheme, *i.e.* without the DC link voltage balancing algorithm. Note from Fig. 11(ii), there are many ripples in the DC link voltage for one cell V_{dc1} in (b) and also both V_{dc1} and V_{dc2} in (c) due to the distortion in the voltage vector which comes from the unbalance of the upper and lower voltages. The upper DC link voltage reaches 650 V from the normal rating of 500 V. This high voltage can cause serious damage on the devices when the voltage ratings of the DC link capacitors or switches are <650 V.

The simulation results with the proposed DC link voltage balancing algorithm are shown in Fig. 12(i)(a)–(c). The lower and upper voltages are balanced well without ripples just as Fig. 11(ii)(c) and the total DC link voltage is without voltage distortion.

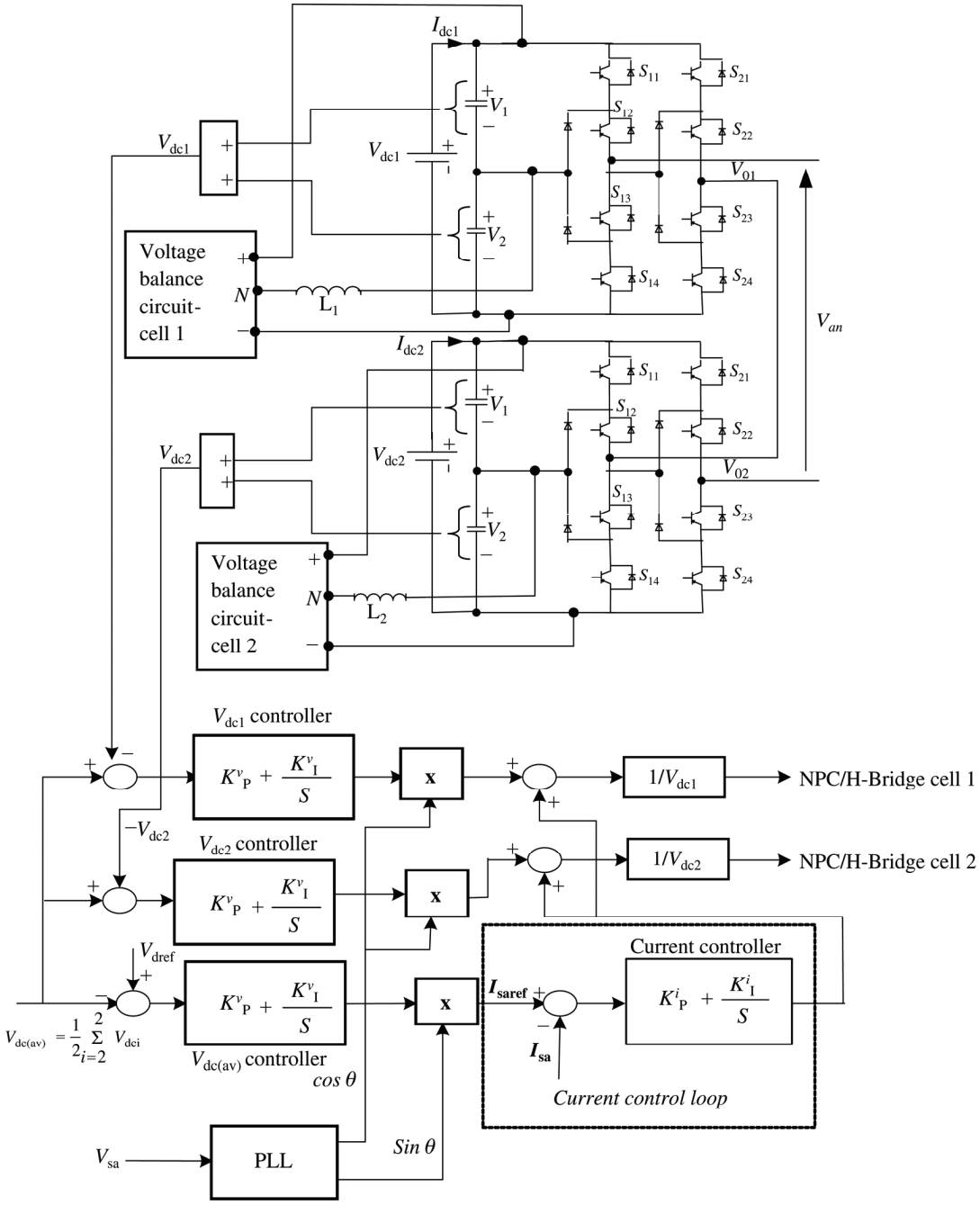


Figure 8. Control structure of a cascaded "3-5-9" hybrid inverter model.

Fig. 12(ii)(a) shows the DC capacitor voltages V_{dc1} and V_{dc2} for the two cells under load step change at $t = 0.08$ s. It is clearly seen that the individual per cell DC voltages track each other shortly after the disturbance and they are maintained constant. This is in contrast with Fig. 12(ii)(b), which is the same voltage but without the proposed balance algorithm. Ripples present result to unwanted harmonics.

5.2 Model Response to Load Changes

Fig. 13 shows the changes in power, grid voltage, and current under load change. In Fig. 13(a), it is observed that grid current is in phase with grid voltage both during steady state and transient conditions. The change in amplitude of current is because of active power drawn by the additional load. In Fig. 13(b), it is also observed that the net reactive power drawn from the source is zero in steady state and transient conditions; this is to ensure that maximum active power is injected into the grid.

6. Experimental Analysis

Experimental validation of simulation results of the model is carried out at reduced power levels. This adopts phase shifted PWM control technique on the model is discussed. Figure 14 shows the experimental setup for the whole system which consists of a single PICDEM 2 plus board which

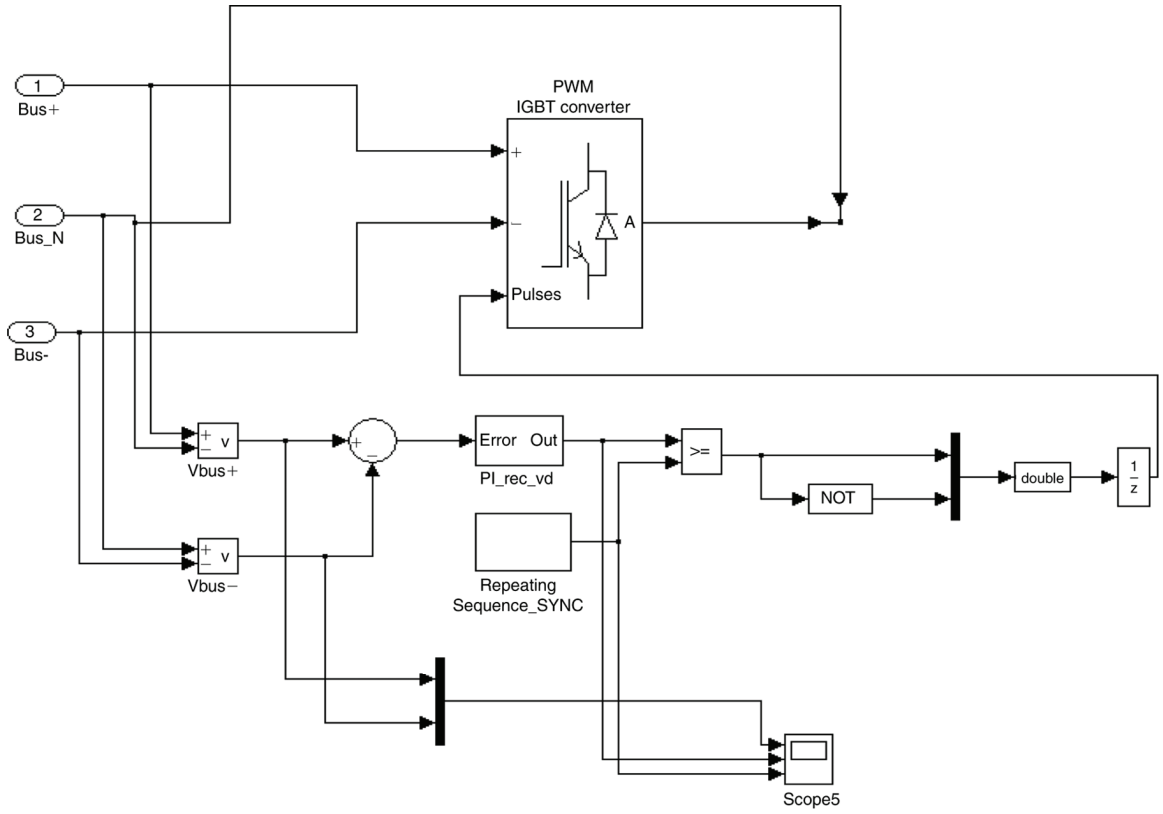


Figure 9. Voltage balance circuit for upper and lower DC link capacitor per inverter cell.

Table 2
(a) System Controller Parameters and (b) System Component Parameters

(a)

Symbol	Parameter	Value
T_{sample}	Sampling period	133 μsec
$K_P^v\_Inv\_Vx$	Voltage control gain (proportional gain)	4
$K_P^v\_Inv\_Vx$	Voltage control gain (integral element)	10
$K_I^i\_Inv\_Ix$	Current control gain (proportional gain)	0.5
$K_I^i\_Inv\_Ix$	Current control (integral element)	20
m_i	Modulation index	0.9

(b)

Symbol	Parameter	Value
$V_{\text{s\_x}}$	AC source voltage (grid voltage)	600 V, 50 Hz
L_{f1}	Inverter side inductance	0.45 mH
R_{f1}	intern resistance of L_{f2}, inverter side inductance	10 mΩ
C_{f}	Filter capacitance	9.4 μF
L_{f2}	Grid side inductance	0.5 mH
R_{f2}	intern resistance of L_{f2}, grid side inductance	1 mΩ
Rd	Damping resistor in series with C (not shown)	1.6 Ω
$C_1 = C_2$	DC link capacitors	0.042 F
$V_{\text{dc1}} = V_{\text{dc2}}$	DC bus voltage	500 V

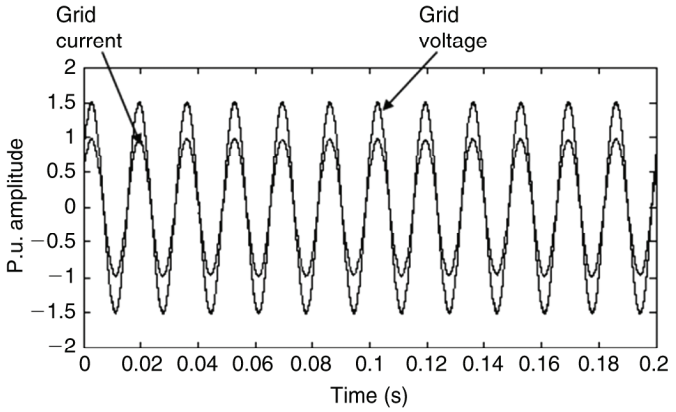


Figure 10. Grid current and voltage under normal condition.

houses a PIC microcontroller (PIC18F4550), two cells of the inverter model cascaded together and each consisting of power supply, switching devices (MOSFETS- IRFZ44V), protective devices, gate drivers (opto – couplers-PC925L), voltage regulators, DC bus and the load configuration.

The PIC microcontroller has been programmed to generate 16 pulses for the MOSFETS power circuit. Two ports *i.e.* port B and port D have been used to channel the signals to the MOSFTES. Port B is assigned to generate pulses for cell 1 and port D for cell 2.

6.1 Experimental Results

In this section, experimental results of model with modified phase shifted PWM control scheme are demonstrated using

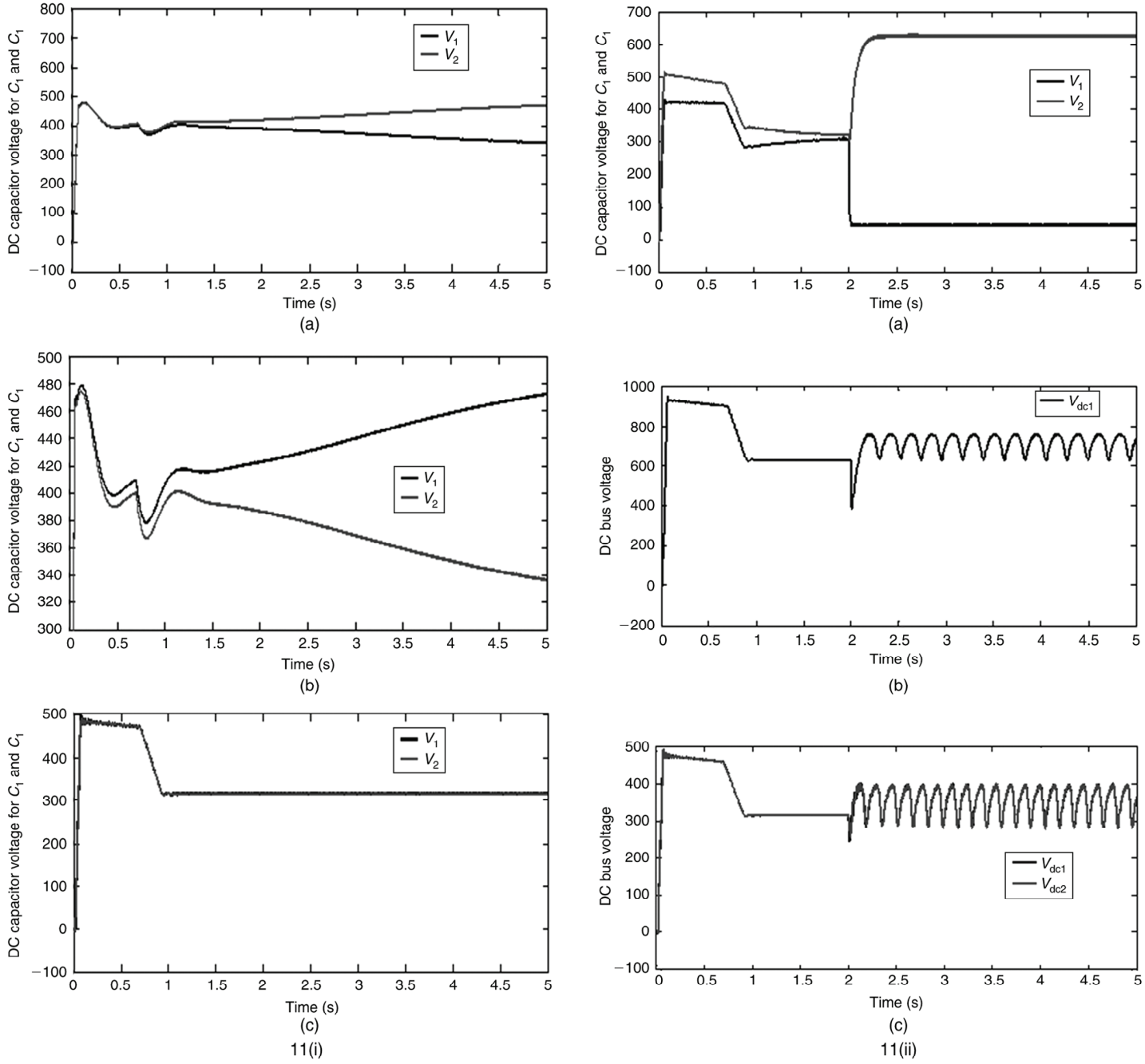
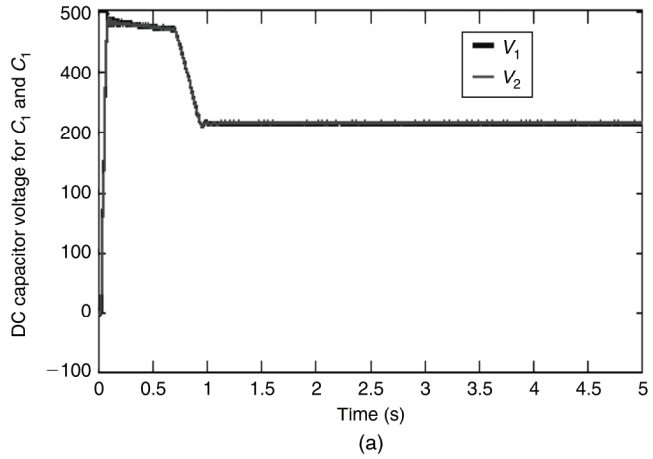
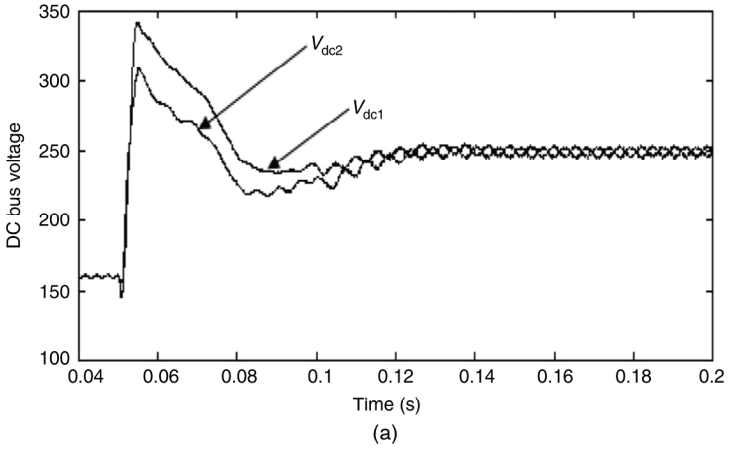
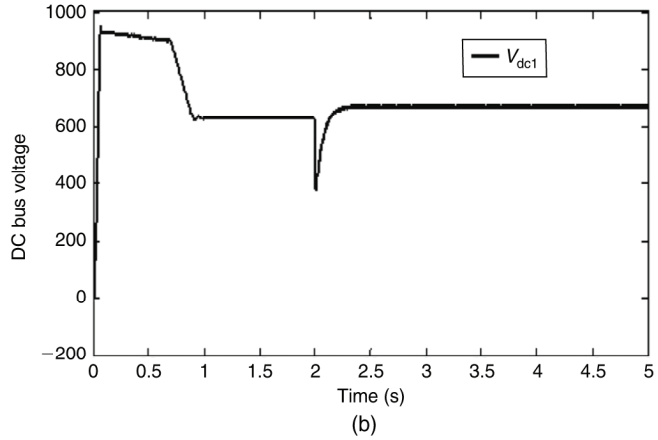
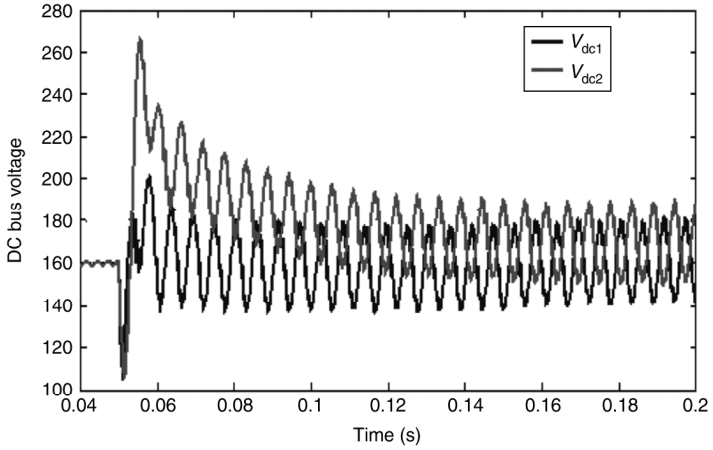


Figure 11. Capacitance voltage validation for various conditions.

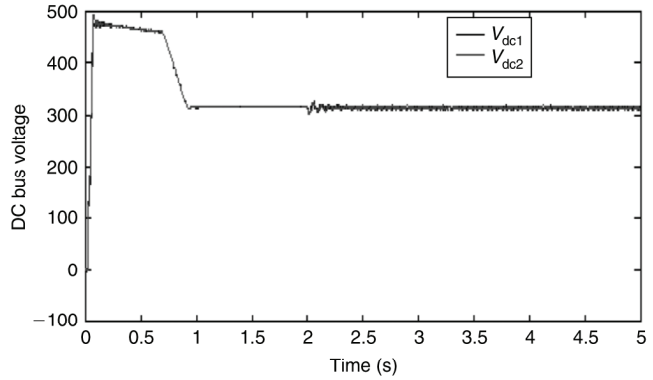






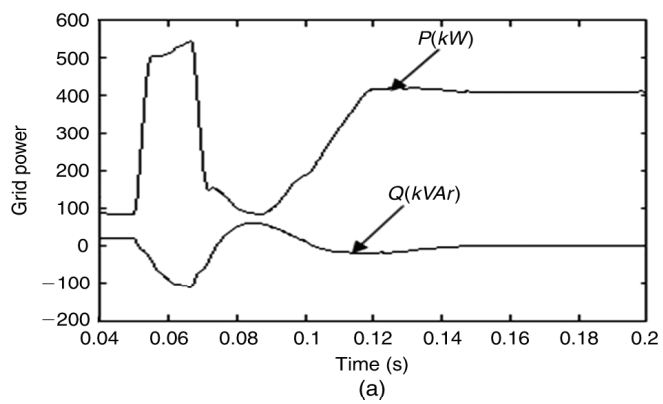


12(ii)



12(i)

Figure 12. DC link response for various load steps.



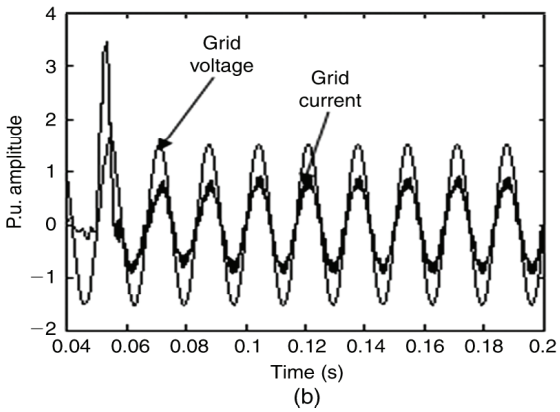


Figure 13. Transient response of the model.

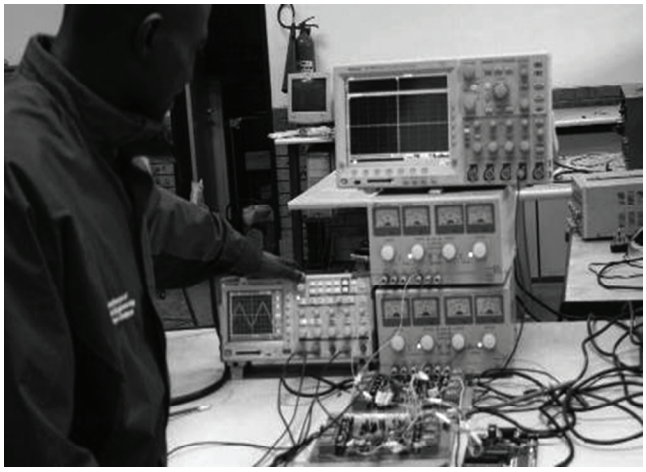


Figure 14. Experimental system setup.

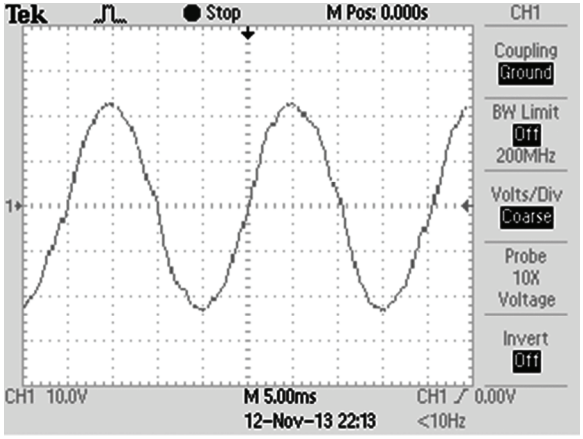


Figure 17. Output voltage for filtered "3-5-9" inverter.

scaled down parameters such as fundamental frequency of 50 Hz with carrier signal frequency of 500 Hz, resistive load of 3 kΩ and a DC supply of 12 V. Figure 15(a) shows the 5-level output waveform for cell one of the hybrid inverter and Fig. 15(b) shows the 9-level output using the proposed phase shifted PWM control cascading the two cells. As can be seen, these two experimental results validate simulation results in Figs. 3(b) and 4(b), respectively.

Figure 16(a) shows the voltage spectrum for 5-level output; it can be observed the first group of harmonic components around 1 kHz, 10 times the operating frequency as predicted via the simulation. Fig. 16(b) shows the voltage spectrum for 9-level output; it can be observed that the first group of harmonics diminished and in frequency shifted upwards. Thus the result of the output filter was a very good sinusoid, as could be seen in Fig. 17.

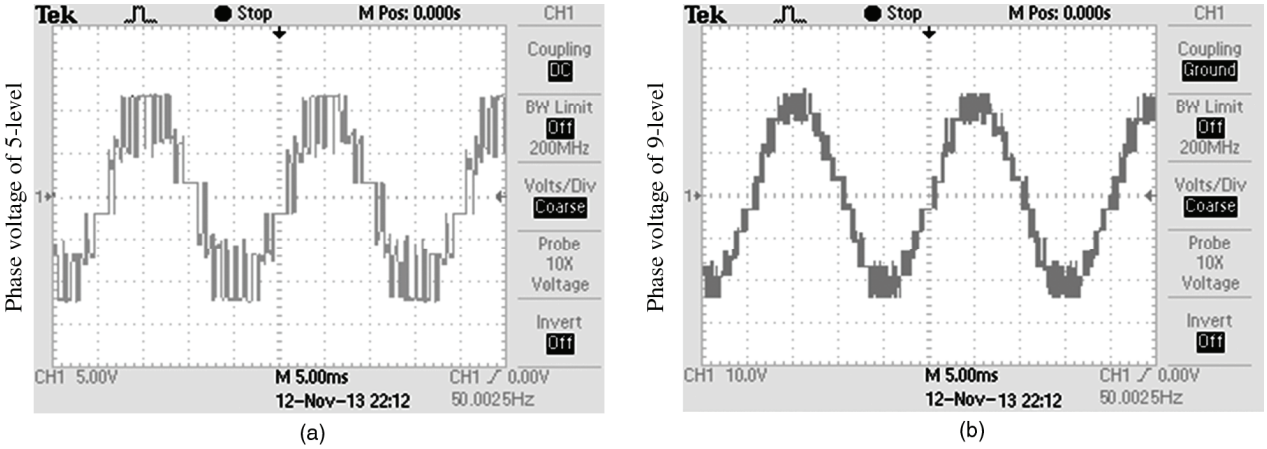


Figure 15. Output voltage for (a) "3-5" and (b) "3-5-9" inverters.

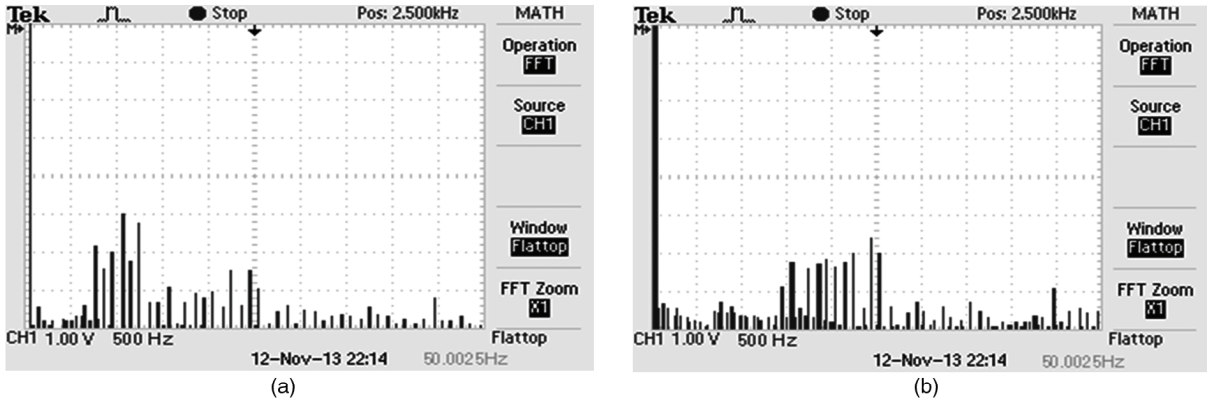


Figure 16. Spectrum for (a) "3-5" and (b) "3-5-9" inverters.

7. Conclusion

In this work, a hybrid inverter model with improved topology configuration in MATLAB is proposed. The superior performance of the model under a novel phase shifted PWM technique is verified using double Fourier transform. A standard model for the "3-5-9" model has been derived. Detailed simulation results have demonstrated that the scheme has fast dynamic response for generating or absorbing reactive power as demanded by the load. For varying DC voltages, the model's parameters retain their original values in the shortest time possible.

To validate the analytical and simulation results, a scaled down cascaded 9-level hybrid inverter hardware was implemented on open loop and experimental results analysed. The experimental results were very consistent with the simulation results. Moreover, the results demonstrated the accuracy of the model and the superior performance of the control technique.

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