Double-Boost DC to DC Converter

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***Abstract*-In this paper anew boost topology is proposed. The circuit is similar with two parallel boost dc-to-dc converters, but the two inductors are charged in parallel and release energy in series, thus enhancing the voltage boost ratio. After a short analysis of the circuit, a comparative study with other classic boost converter (single boost and two-cascade) is presented. The simulation results show a net improvement of the boost ratio for the new proposed topology.**

I. Introduction

An increased boost factor suits the many emerging applications in the automotive industry, telecommunications industry, IT industry as well as power generation via fuel cells, photovoltaic arrays and wind turbines [1-8]. The basic boost topology does not provide a high boost factor. This has led to many proposed topologies such as the tapped-inductor boost, cascaded boost and interleaved boost converters [5-8]. This paper introduces another variation which provides a higher boost factor and also provides for the possibility to gear up or down thus extending the control range.
Although control methods such as fuzzy logic [11], sliding mode control [14] and others [10, 12, and 14] are available, a simple IP controller is used to verify the proposed double -boost topology.

II. Proposed Model

Fig. 1 shows the proposed topology. The inductors L_1 & L_2 have the same values, the diodes D_1-D_3 are the same type and the same assumption was for the transistors (Q_1 & Q_2). Each inductor has its own switch and thus is similar with the paralleling of two single/classic converters.

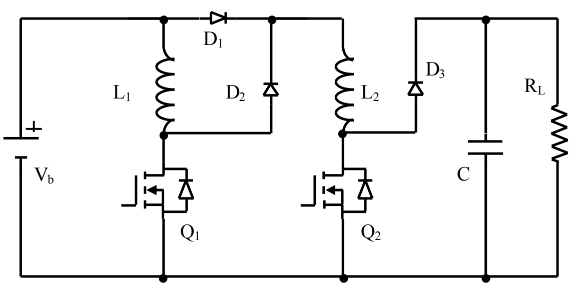

Fig. 1 Proposed Model

A. Equivalent Diagram in ON State

Let us firstly consider ideal components. When the transistors Q_1 & Q_2 are in ON state, the proposed topology transfers energy from the dc source (V_b) into the inductors L_1 & L_2 as can be seen in Fig.2, where i_1 is the current through inductor/transistor 1, i_2 is the current through inductor/transistor 2, i_o is the output current through load R_L and C is the smoothing capacitor.

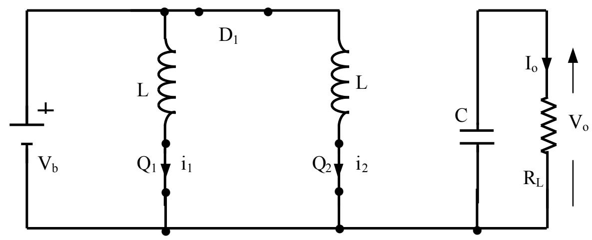

Fig.2 Equivalent diagram for $Q_1 = Q_2 = ON$

B. Equivalent Diagram in OFF State

During the OFF state, the two inductors are connected in series, as shown in the equivalent diagram (Fig. 3).

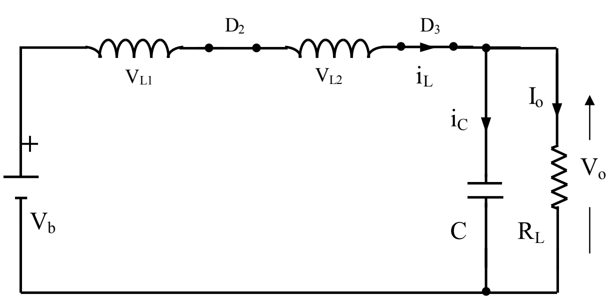

Fig.3 Equivalent diagram for $Q_1 = Q_2 = OFF$

C. Boost Factor

The switching frequency is high enough so the differential equations governing the circuit could be linearized. For the charging interval ($Q_1 = Q_2 = ON$), the voltage across each inductor is V_b and the currents $i_1(t)$ and $i_2(t)$ could be written as:

$$i_1(t) = i_2(t) = \frac{V_b}{L}t + I_L(0) \quad (1)$$

where $I_L(0)$ is the initial current through inductor at t = 0.
When the transistors are turned OFF at t = δT, the voltage across inductors is $V_o - V_b$ and the current $i_L(t)$ is:

$$i_L(t) = \frac{V_b - V_o}{2L}(t - \delta T) + I_L(\delta T) \quad (2)$$

Evaluating eq. (1) at t = δT and (2) at t = T, the system becomes:

$$I_L(\delta T) = i_1(t = \delta T) = i_2(t = \delta T) = \frac{V_b}{L}\delta T + I_L(0) \quad (3)$$

$$I_L(0) = i_L(t = T) = \frac{V_b - V_o}{2L}(T - \delta T) + I_L(\delta T) \quad (4)$$

The converter is design to operate in continuous mode and $I_L(0) = I_L(\delta T)$. From the system of (2) and (3) the boost factor M_p for the proposed circuit can be deducted:

$$M_p = \frac{V_o}{V_b} = \frac{2}{1-\delta} \quad (5)$$

As can be noticed, the boost factor of the proposed topology is double as regarded to the simple boost converter.

III. Boost Factor Comparison

In order to enhance the advantage of the proposed boost topology, a boost factor comparison with a single and two-cascaded converter is necessary. This should be done taking in consideration the real values of components.

A. Simple boost converter

As presented in [9], the boost factor (M_s) depends on inductor resistance (r_L) as:

$$M_s = 1/\left[(1-\delta) + \frac{r_L}{R_L(1-\delta)}\right] \quad (6)$$

When taking in consideration voltage drop across the diode (V_d) and transistor resistance in saturation (r_{dson}), the boost factor becomes:

$$M_s = 1/\left[(1-\delta) + \frac{\delta r_{swon}}{R_L(1-\delta)}\right] - \frac{V_d}{V_b} \quad (7)$$

B. Double cascaded boost converter

When two identical simple converters are connected in cascade (Fig. 4), the boost factor (M_c) is affected by the capacitor (C) in the first unit and switching frequency. The eq. (8) shows the boost factor for the cascade.

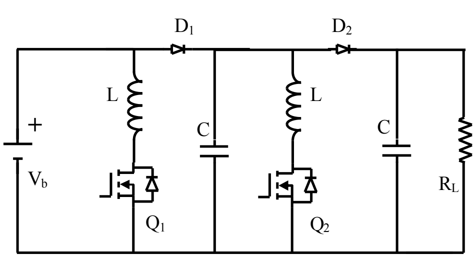

Fig.4 Double cascade boost converter

$$M_c = \left[2 - \frac{\delta T_s}{(1-\delta)R_L C}\right] / \left\{1/\left[(1-\delta) + \frac{r_L + \delta r_{swon}}{R_L(1-\delta)}\right] - \frac{V_d}{V_b}\right\} \quad (8)$$

C. Proposed double-boost converter

For this topology, all the real parameters should be taken in consideration at once. As can be noticed, the currents through inductors are slightly uneven, but for a good approximation they still can be considered equal. Then the boost factor could be written as:

$$M_p = 2/\left[(1-\delta) + \frac{r_L + \delta r_{swon}}{R_L(1-\delta)}\right] - \frac{2V_d}{V_b} \quad (9)$$

It can be seen that the inductance resistor and voltage across transistor resistor in ON state are considered with unity factor because the charging is parallel and independent one of each other, while the diode voltage drop has a coefficient two because they both are in series when the energy is transferred to the output.

IV. Control System

For this study, a simple PI controller has been used, as shown in Fig. 5.

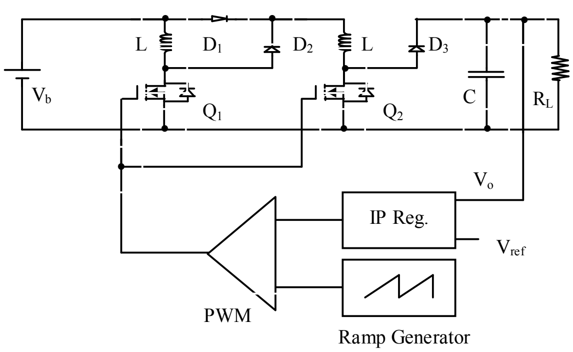

Fig.5 Double-boost converter, control system

In the steady state, the power balance between input and output can be written as:

$$V_b I_s = \frac{1}{C}\cdot\frac{d}{dt}\left(V_o^2\right) + V_o I_o \quad (101)$$

Based on this dynamic equation, majority of authors have proposed a classic PI regulator. But the closed-loop transfer function of this type of regulator has two zeros:

$$\frac{V_o^2}{V_{ref}^2} = \frac{(k_i + s \times k_p)(1 + s \times \tau_3)}{s^3 \times \left(\frac{\tau_3 C}{2}\right) + s^2 \times \frac{C}{2} + s \times k_p + k_i} \quad (11)$$

For this study an integral/proportional (Fig. 6) solution has been chosen as voltage regulator, where k_i, k_p are the integral and proportional coefficients respectively and τ_1 is the time constant of a noise-rejection low-pass filter.

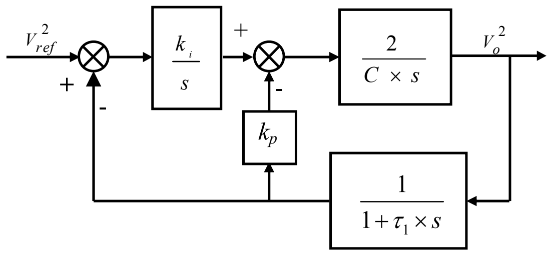

Fig. 6 IP Regulator

The close-loop transfer function of the system is:

$$\frac{V_o^2}{V_{ref}^2}=\frac{1+s\times\tau_1}{s^3\left(\frac{\tau_1\times C}{2k_i}\right)+s^2\left(\frac{C}{2k_i}\right)+s\left(\frac{k_p}{k_i}\right)+1} \tag{12}$$

The equation (12) shows that the IP solution cancels a slow zero from the transfer function improving the dynamics of the regulator.

If the poles of the system (s_0, s_1 and s_2) are placed on the Butterworth circle with the radius ω_o such as: s_o = - ω_o, $s_1=\omega_o e^{j\frac{3\pi}{4}}$ and $s_2=\omega_o e^{-j\frac{3\pi}{4}}$, then the coefficients k_p and k_i are:

$$k_p=\frac{C}{2\times\left(1+\sqrt{2}\right)\times\tau_3} \tag{13}$$

$$k_i=\frac{C}{2\times\left(1+\sqrt{2}\right)^3\times\tau_3^2} \tag{14}$$

If the load resistor is considered (R_L), then the coefficients become [12]:

$$k_i=\frac{\left(T+\tau_1\right)^3}{T^2\tau_1^2\left(1+\sqrt{2}\right)^3 R_L} \tag{15}$$

$$k_p=\frac{1}{R_L}\left(\frac{\left(T+\tau_1\right)^2}{\left(1+\sqrt{2}\right)T\tau_1}-1\right) \tag{16}$$

where $T=R_L\times C$.

V. Simulation Results

To validate the above study, the Simetrix 5.3 software platform has been used to simulate the proposed topology (Fig. 7) but also the simple and the two cascade boost converters. For all the above circuits, the values of the element have been very conservative chosen as: V_b =12 V, L = 100 µH, r_L = 0.1 Ω, C = 10 µF, V_d = 0.8 V, R_L = 50 Ω, r_{dson} = 50 mΩ and the switching frequency of f_s = 50 kHz.

Figures 7 & 8 show the simulation model for the proposed boost converter and the output voltage. The model has been tune to give the maximum output voltage of 122.1 V for a duty cycle of 85 percentages. This gives a boost factor of 10.1 compared to 11.9 estimated according to (9).

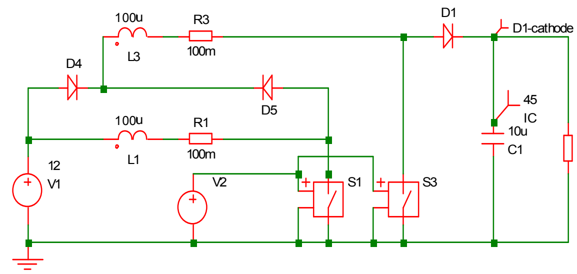

Fig.7 Double-boost converter- simulation model

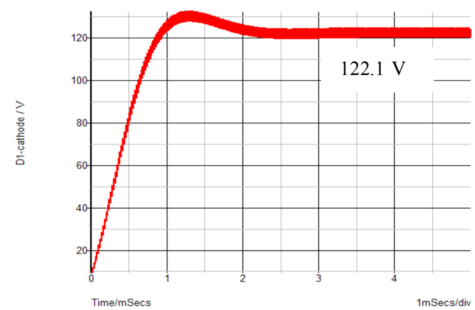

Fig.8 Double-boost converter- maximum output voltage

In figure 9 & 10, the simple boost simulation model and maximum output voltage are shown. The maximum output voltage achieved was 52.7 V for a duty cycle of 80 percentages. The boost factor is 4.4 compared with and estimated of 4.67.

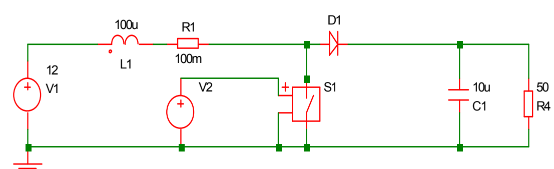

Fig.8 Simple-boost converter- simulation model

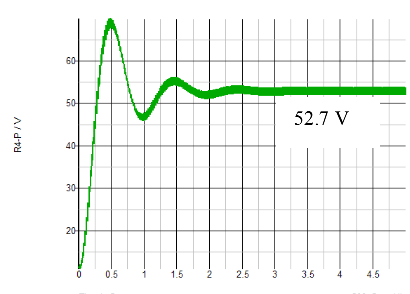

Fig.9 Simple-boost converter- maximum output voltage

The two-cascade boost converter simulation model is shown in figure 10 and the maximum output voltage in figure 11. The maximum output voltage of 82.1 V is achieved for 80 percentages duty cycle which represents a boost factor of 6.84 compared to 7.91. What can also be observed a very instable starting period, same conclusion as in [4].

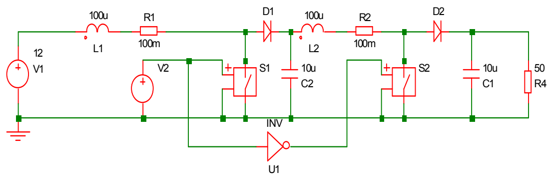

Fig.10 Two-cascaded boost converter- simulation model

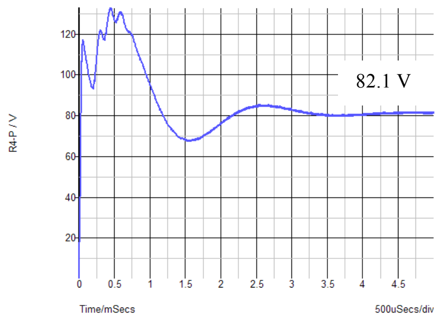

Fig.11 Two-cascade boost converter- maximum output voltage

Figures 12 & 13 show the comparative output voltages between the simple and two-cascade boost and between the simple and the proposed double-boost respectively, while figure 14 shows all three output voltages for a better comparison.

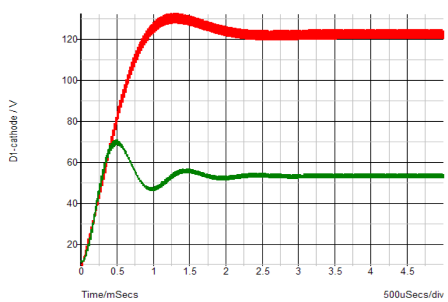

Fig.12 Double-boost and simple-boost comparison

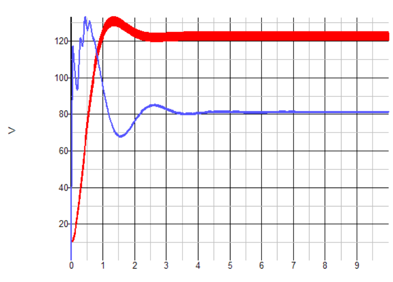

Fig.13 Double-boost and two-cascade comparison

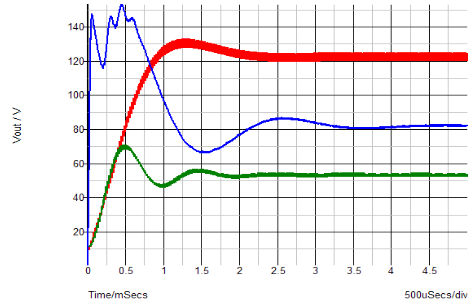

Fig.14 Output voltage of all studied converters

Another aspect studied was to verify the assumption that the charging currents through the two inductors could be considered equal. Fig, 15 shows the two current and the current through diode 3 on normal scale, while Fig. 16 shows the zoom of the moment when these entire three current joint together.

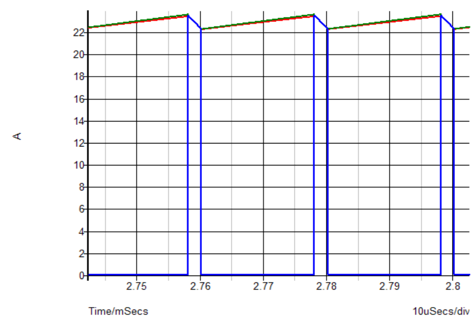

Fig. 15 Inductors and diode 3 currents

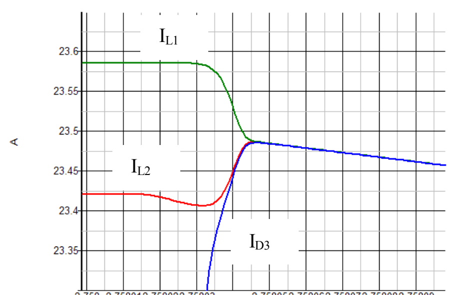

Fig. 16 Inductors and diode 3 currents-zoom

From Fig. 16 results a 0.68 percentage difference between the two inductor current, which makes very much acceptable the initial assumption.

VI. Experimental Results

An experimental model has been built. Fig. 17 shows the experimental set. For practical conveniences, the supply voltage (V_b) was 4 V. The other parameters of the experiment were: the inductors 100 μH, the load 680 Ω, the smoothing capacitor 47 μF, IRF613 as switching transistors, 10 CTQ150 as diodes and 50 kHz as switching frequency.

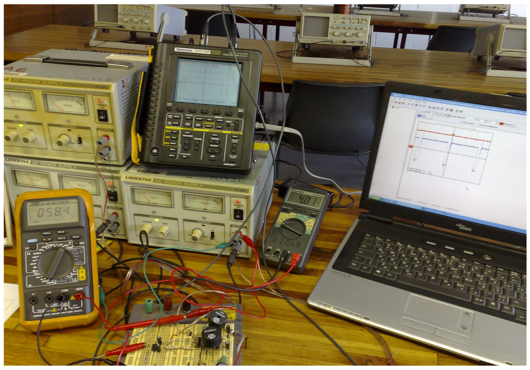

Fig. 17 Experimental set-up

For a duty cycle of 90 percentages, the output voltage was 55.3 V for the given 4 V input voltage (V_b). Fig. 18 shows the output voltage and the gates signal for a duty cycle of 90%. Figures 19, 20 show the voltage across transistor Q_1 and Q_2 and figure 21 show the voltage across the inductor L_1.

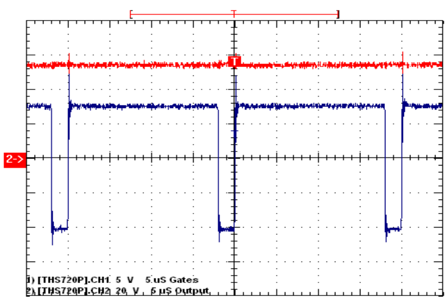

Fig. 18 Output voltage

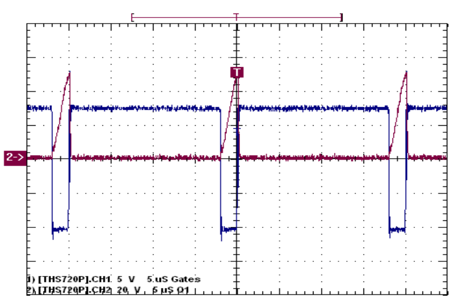

Fig. 19 Voltage across Q_1

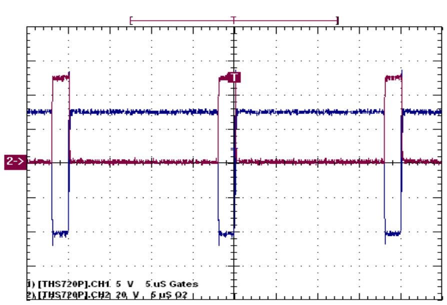

Fig. 20 Voltage across Q_2

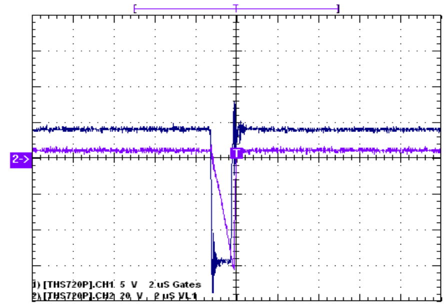

Fig. 21 Voltage across L_1

VII. Conclusions

The present paper has presented a new boost topology which ensures a significant improvement on boost factor. The new double-boost converter has been modeled and the simulation results are presented in comparison with classical known boost converters. The experimental results show an improved boost factor.

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