Active Power Control for Capacitive Divider Tapping Method

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Abstract— **Capacitive divider systems for tapping electric power from high voltage transmission lines are known to exhibit certain detrimental problems of stability, sub-resonance harmonic oscillations, and ferroresonance when coupled with non-linear loads. On the other hand, they can improve reactive power flow, power factor and contribute to improved harmonic filtration of the larger power system. This paper, therefore, proposes a controlled power flow conditioner as an essential integral component of a capacitive divider system to control power transfer between the high voltage transmission line, capacitive divider system, and the load. The ultimate objective of this conditioner is to mitigate or minimize the attendant problems associated with coupling the system to the load, and optimize the derivable benefits to the larger network.**

I. Introduction

One means of meeting electric power needs of most rural and remote areas is by direct tapping from the high voltage transmission lines. HV transmission lines traverse rural and remote areas. In some cases tapping power from HV lines to feed load areas could not only be economical and convenient, but of considerable secondary technical advantage to the network performance. Reference [1] presented a review of the state of the art of the methods for tapping power from the HV lines. One of these methods is capacitive divider technique.

The capacitor divider has been known for quite a while but using this technology to transform high voltage to medium voltage for delivering power is more recent [2]. In this method, a bank of capacitors is connected directly to the conductor line via a high voltage protective device as presented in Fig. 1.

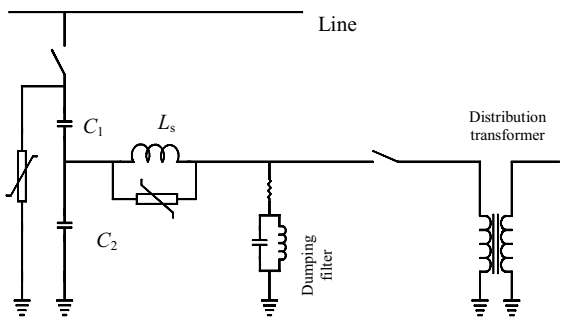


Fig. 1 Capacitive divider

The system is then brought to resonance by inserting an inductor (L_s):

$$L_s = 1/[\omega^2(C_1 + C_2)] \quad (1)$$

This system is used on transmission lines from 120 kV up to 345 kV and delivers power between 1,5 MVA and 4 MVA. An example of a practical application of this method is in Quebec, Canada, where a 3-phase, 1.5-MW, system has replaced the conventional Riviera-Ste-Anne substation of Hydro-Québec in 1994 [2].

Although, according to Gaétan Beaulieu [2] the practical system in Quebec has always operated correctly and there has been a good degree of satisfaction with the technology. Nonetheless, stability problem can occur depending on the nature of load connected. Sub-resonance harmonic oscillations can easily be produced by the presence of a strong non-linear load. There can also be ferroresonance problem with the distribution network-coupling transformer. On the other hand, however, capacitive divider system can positively impact the reactive power flow of the grid network, improve power factor, and assist to improve filtration or suppression of some harmonic components.

The foregoing, therefore, suggests the need for a controlled power flow conditioner as an essential integral element of a capacitive divider system. The ultimate purpose of the conditioner is to control power transfer between the high voltage transmission line, capacitive divider system, and the load. This is for mitigation or minimization of the attendant problems of the coupling of the capacitive divider to the load, and to optimize the benefits derivable from the use of the system in a grid. The novelty proposed by this study, therefore, consists of introducing an active device in order to control the power transferred between the high voltage transmission line, capacitive divider and load.

The paper is structured such that the proposed model is presented immediately after the introduction. A considerable effort is particularly given to explaining and analyzing the control system. Using typical practical scenario the model is then further analyzed and tested. The ensuing steady state and dynamic analysis results are presented in the section that followed. The paper ends with some concluding remarks.

II. PROPOSED MODEL

The principle of capacitive divider is not new as it was used in a passive mode [3-5]. The novelty proposed by this study consists of introducing an active device in order to control the power transferred between the high voltage transmission line, capacitive divider and load.

A. Basic model

Fig. 2 shows the proposed model.

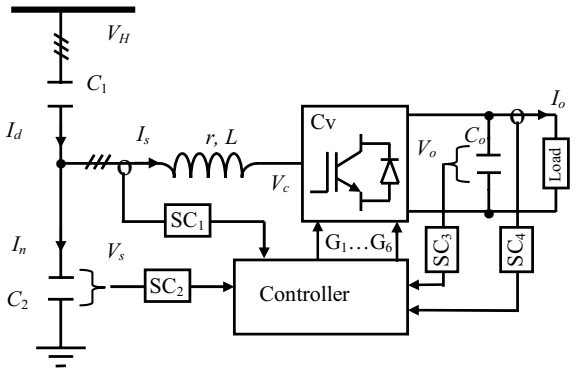


Fig.2 Basic model

The capacitive divider drops the voltage from the level of the high voltage transmission line (V_H) to a suitable level for the switching-mode boost-converter (V_s):

$$V_s = \frac{C_1}{C_1 + C_2} V_H \tag{2}$$

where C_1 and C_2 are capacitors of the divider.

The switching-mode converter (Cv.) acts as an active boost rectifier. Due to the current controller, the current drawn from the supply [i_s] is sinusoidal and can have a controlled phase-shift, thus being able to offer small adjustment of the reactive power. The controller also contains a voltage regulator in order to maintain constant value for the dc bus (V_o); SC_1 to SC_4 are signal conditioners.

B. Background

If the high voltage system is given as $v_{H1n} = \hat{V}_H \sin(\omega t)$, $v_{H2n} = \hat{V}_H \sin(\omega t - 2\pi/3)$ and $v_{H3n} = \hat{V}_H \sin(\omega t + 2\pi/3)$ where $\hat{V}_H$ is the amplitude of the high voltage, then the voltage system at the connection point of the converter is:

$$[v_s] = \begin{bmatrix} v_{s1} \\ v_{s2} \\ v_{s3} \end{bmatrix} = \begin{bmatrix} \hat{V}_s \sin(\omega t + \varphi) \\ \hat{V}_s \sin(\omega t + \varphi - 2\pi/3) \\ \hat{V}_s \sin(\omega t + \varphi + 2\pi/3) \end{bmatrix} \tag{3}$$

where V_s is the output voltage of the capacitive divider as given by (2) and φ is the phase-shift introduced by the capacitive divider.

Now, if the voltage system [v_s] is considered the supply for the converter, the ac side of it can be described as:

$$\dot{\boldsymbol{X}} = \boldsymbol{AX} + \boldsymbol{BK} + \boldsymbol{CU} \tag{4}$$

with:

$$\boldsymbol{X} = \begin{bmatrix} i_{s1} & i_{s2} & i_{s3} & V_o \end{bmatrix}^T \tag{5}$$

$$\boldsymbol{K} = \begin{bmatrix} k_a & k_b & k_c \end{bmatrix}^T \tag{6}$$

$$\boldsymbol{U} = \begin{bmatrix} v_{s1n} & v_{s2n} & v_{s3n} \end{bmatrix}^T \tag{7}$$

$$\boldsymbol{A} = \begin{bmatrix} -r/L & 0 & 0 & 0 \\ 0 & -r/L & 0 & 0 \\ 0 & 0 & -r/L & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{8}$$

$$\boldsymbol{B} = \begin{bmatrix} -V_o/3L & V_o/6L & V_o/6L \\ V_o/6L & -V_o/3L & V_o/6L \\ V_o/6L & V_o/6L & -V_o/3L \\ i_{c1}/2C_o & i_{c2}/2C_o & i_{c3}/2C_o \end{bmatrix} \tag{9}$$

$$\boldsymbol{C} = \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/L \end{bmatrix} \tag{10}$$

where i_{c1}, i_{c2} and i_{c3} is the input current system, r and L are the parameters of the input inductor, V_o is the voltage of the dc bus, C_o the capacitive storage element and k_a, k_b and k_c describe the state of the switches of the three legs of the $\boldsymbol{H}$ topology converter and their values are 0 or 1, see Table I; Fig. 3 shows the eight associated state space vectors.

TABLE I
SWITCHING MATRIX

States	k		
	k_a	k_b	k_c
0	0	0	0
1	1	0	0
2	1	1	0
3	0	1	0
4	0	1	1
5	0	0	1
6	1	0	1
7	1	1	1

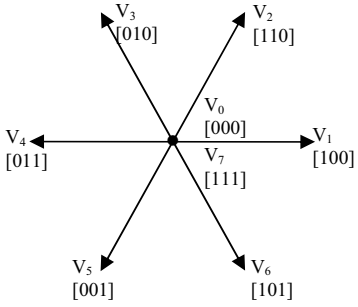


Fig. 3 State space vectors

This boost converter shapes the current drawn from the supply and controls the input active and reactive power. In order to perform adequately these functions, the dc bus voltage (V_o) must comply with controllability criteria [7]:

$$V_o > \sqrt{\hat{V}_s^2 + [r^2 + (\omega L)^2] \times \hat{I}_s^2} \tag{11}$$

where ω is the fundamental ($2\pi f$ rad/sec) and $\hat{I}_s$ is the maximum amplitude of current drawn by the converter.

After the current is shaped sinusoidal and neglecting the losses in the real switches, the power transferred though the converter can be written as:

$$\frac{3}{2}\hat{V}_s \times \hat{I}_s = \frac{1}{2C_o} \times \frac{d}{dt}\left(V_o^2\right) + V_o \times I_o \tag{12}$$

The left hand term represents the power drawn from the supply source, $V_o \times I_o$ is the power delivered to the dc load and the middle term represents the variation of the capacitor power; this (middle) term must be cancelled by the action of the voltage regulator.

C. Control system

As shown above, the dc bus must be kept constant by the voltage regulator. In Fig. 4 shows a very simple control system used for the validation of the proposed model; the voltage regulator is a simple PI controller which according to (11) compares the square of the dc bus to its square reference: V_o^{*2}. The time constant τ has an important effect on dynamic and on the harmonic content of the input current: a large value will determine a low THD and low dynamic response while a small one will increase THD. The recommended optimum value of the low- pass filter cut-off frequency is as in [8] and is in the interval of 1/3 to 1/2 from the line frequency e.g. (16 Hz - 25 Hz); for this application a value of 20 Hz has been chosen which gives an approximate time constant value of: $\tau = 0.008$.

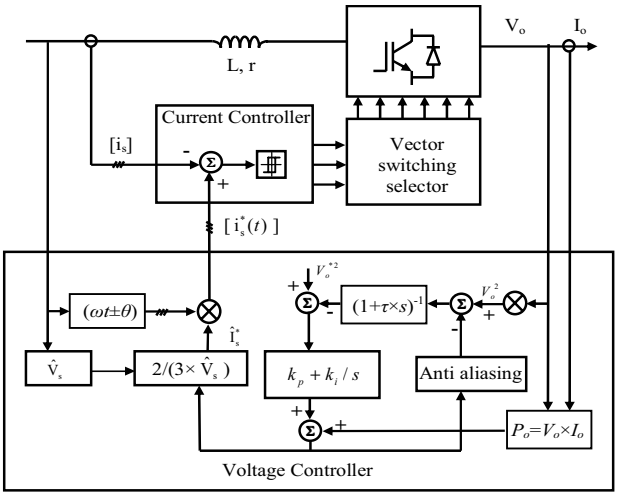


Fig. 4 Control system

The closed loop transfer function of this controller can be written as:

$$\frac{V_o^2}{V_o^{*2}} = \frac{\left(1 + s \times k_p / k_i\right)\left(1 + s \times \tau\right)}{s^3 \times \left(\frac{\tau C_o}{2k_i}\right) + s^2 \times \left(\frac{C_o}{2k_i}\right) + s \times \left(\frac{k_p}{k_i}\right) + 1} \tag{13}$$

The proportional (k_p) and integral (k_i) coefficients could be determined by placing the poles of the closed loop on the Butterworth circle [10]:

$$k_i = \frac{C_o}{2 \cdot \left(1 + \sqrt{2}\right)^3 \cdot \tau^2} \tag{14}$$

$$k_p = \frac{C_o}{2 \cdot \left(1 + \sqrt{2}\right) \cdot \tau} \tag{15}$$

In order to keep the coefficients of the regulator constant, a dc power estimator is introduced which feeds-forward the power delivered to the dc load for better dynamic response and thus making the coefficients independent upon the load [8-10]. The anti aliasing prevents saturation.

Equation (2) gives the pickup voltage for no-load situation, but when the load is changing, the voltage V_s varies, and hence $\hat{V}_s$ detection block must be introduced.

The block "$2/(3\times \hat{V}_s)$" produces the amplitude of the reference current which then is used to create the reference current system $[i_s^*(t)]$; the phase-shift θ is introduced for a small adjustment of the reactive power when necessary.

The current controller is of hysteresis type; in this application, a special care has been taken to limit the switching frequency. Further, the right combination of switching vectors is determined and accordingly, the converter is activated such as the input current to follow the reference.

III. Simulation Results

In order to validate the model a simulation model has been built based on Matlab (Fig.5). For this validation a dc power of 10 kW has been considered and a capacitor of 2200 µF. The dc bus voltage of 700 V was chosen, which complies with controllability criteria (11).

The capacitive divider is chosen such that the voltage V_H of 132 kV (line) to be reduced to a level of 230 V/phase in no dc load and the current through it of approximately 15 A. At maximum dc power delivered, the input current into the active converter is approximately the same 15 A that can create a small reactive power control. These conditions will be translated into $C_1 = 0.63$ µF and $C_2 = 200$ µF.

For this application, the input inductor L has been taken as high as 10 mH; this value helps for an accurate sinusoidal shape and does not contradict with the controllability condition (11). The dc capacitor C_o of 2200 µF has been chosen as a compromise between ripple and dynamic of the control system.

A. Steady state

Fig. 6 shows the input parameters I_{s1}, V_{s1} and the output dc voltage V_o in steady state for a maximum dc power of 10 kW. As one can notice, the phase current is in phase to the input phase voltage and quasi-sinusoidal, and the dc voltage is kept close to the reference within 0.5 percent. Fig. 7.a shows how closely the input current follows the reference and the very small harmonic content of the input current is shown in Fig. 7.b.

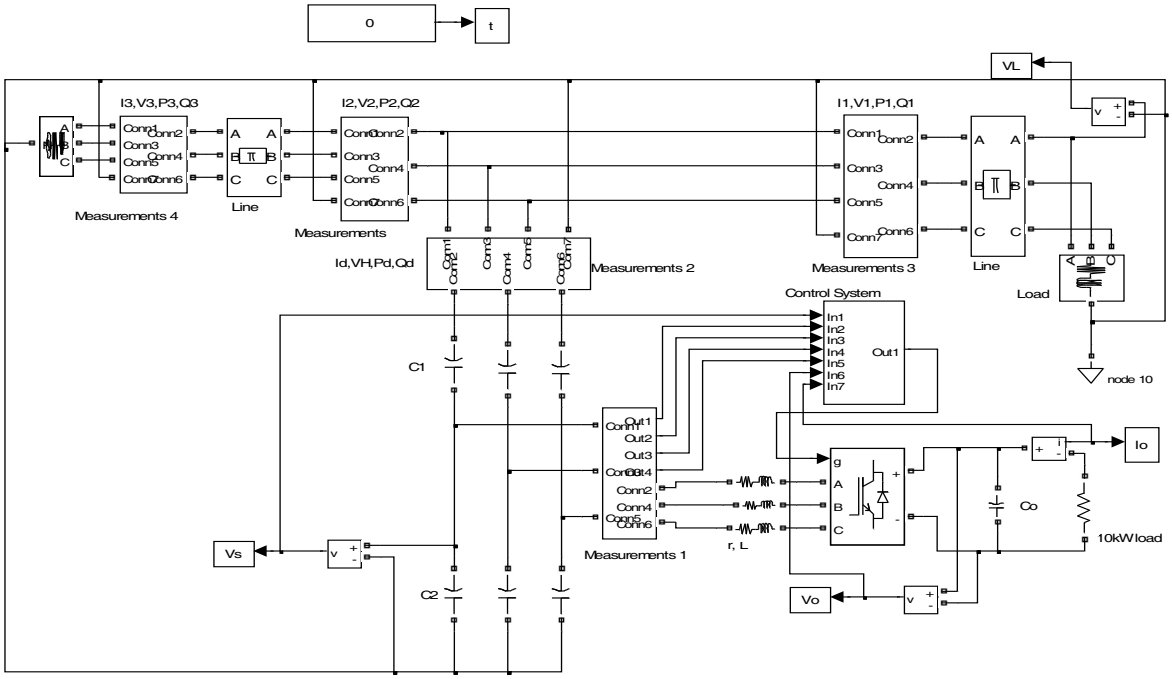


Fig. 5 Simulation model

As can be noticed from Fig. 7 a & b, the input current follows very accurately the reference and the total harmonics distortion is very small and this is basically due to the ripple. At a closer look, it can be noticed that the switching frequency is kept between 3 and 5 kHz (see Fig. 8).

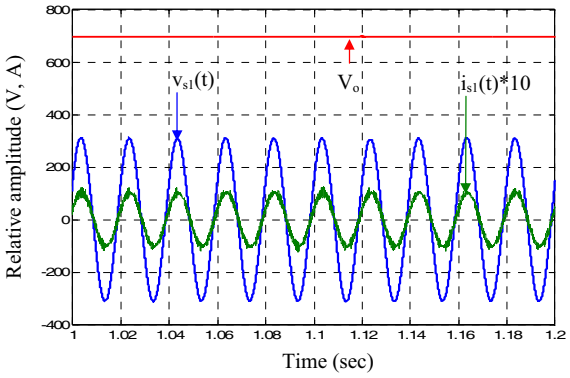
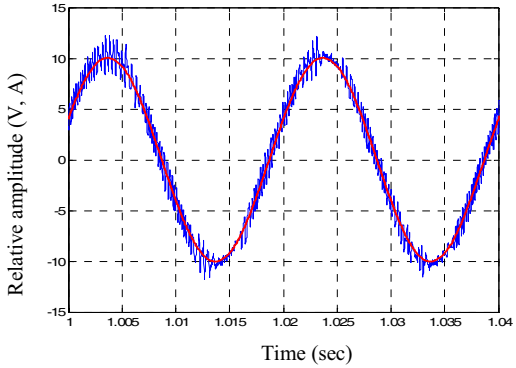


Fig. 6 Input/output parameters in steady state



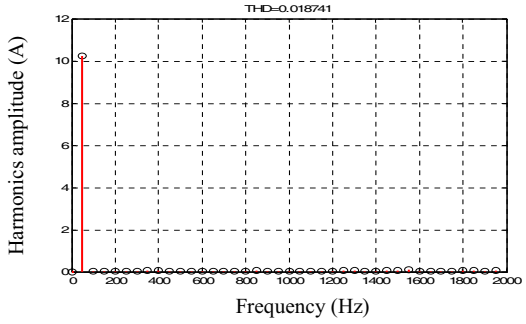


Fig.7 Input current versus reference (a), harmonics content (b)

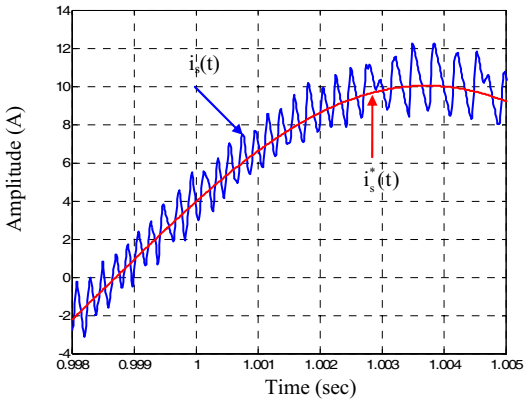


Fig. 8 Input current: switching frequency

It also can be noticed that the switching frequency is not fixed which creates less influence into the transmission line. Fig. 9 shows the harmonic content of

the total current drawn by the capacitive divider I_d (vertical axis is greatly expanded). It can be noticed that the level of harmonics is very low and is way below the range of frequencies used for communication, thus no interference should occur. Capacitor C_2 has a big contribution to this situation.

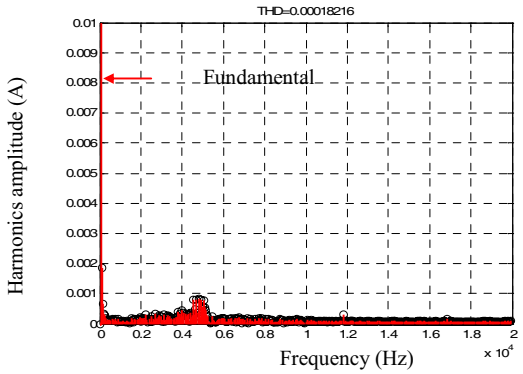


Fig. 9 Capacitive divider current: harmonics content

B. *Dynamic behavior*

The next step in this study was to evaluate the dynamic behavior of the proposed model. For this, few situations have been examined: a sudden step down in high voltage, a sudden step up of the dc load and a combination of step up and step down of the dc load.

Fig. 10 shows the system response for a 20 percentage drop in the transmission line voltage. As can be noticed the dc bus has a small shoot for a time that is necessary to evaluate the new supply voltage, then comes back to 700 V. The drop in supply voltage is compensated by increasing the supply current as requested by (11).

Next the system has been tested for load variation. Fig. 11 shows the reaction of the system when the dc power varies from 5 kW to 10 kW. In Fig. 12 is presented the dynamic response for a combination of variations of the dc power from half to full and back to half dc power.

As can be noticed the system response is fairly good, it needs only few cycles to reestablish the dc voltage.

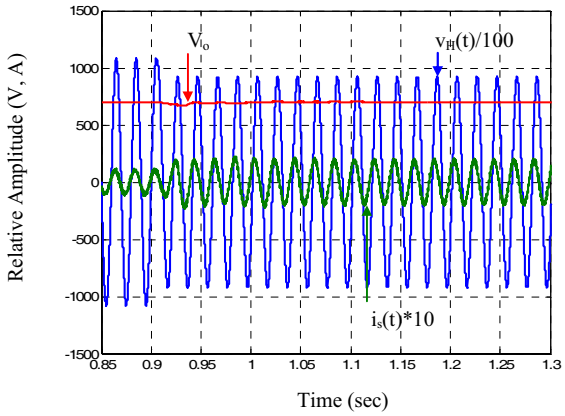


Fig. 10 Dynamic response for a step down in supply voltage

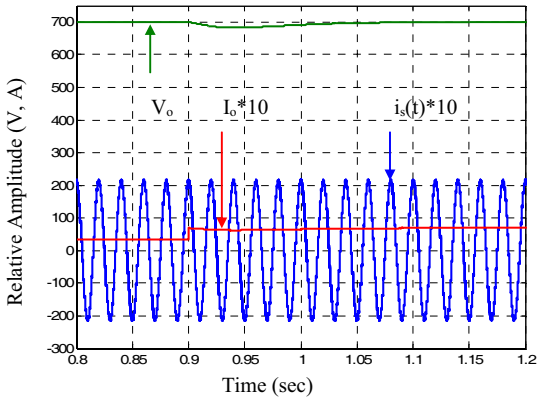


Fig. 11 Dynamic response for a step up in dc power

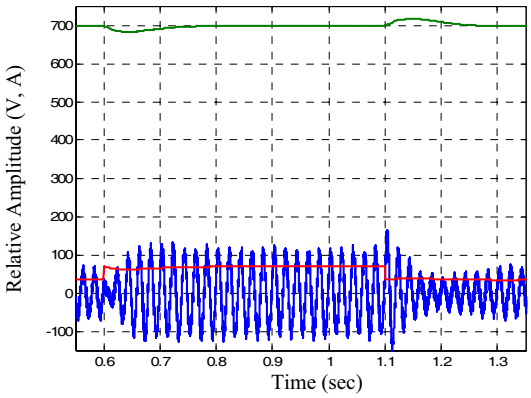


Fig. 12 Dynamic response for a step up/step down in dc power

IV. Conclusions

In this paper a new capacitive divider tapping method with active power control has been introduced. The novelty proposed by this study, consists of introducing an active device in order to control the power transferred between the high voltage transmission line, capacitive divider and load. Due to its control system, it strengthens the stability of the entire system especially when connected to strong non-linear loads. Thus, it minimizes the problems, which can normally occur when coupling the transmission line to such loads via the capacitive divider.

The simulation results show positive steady state parameters such as good sinusoidal shape for the current drawn from the main line with low harmonic content. The proposed model shows also a good dynamic response for few critical situations.

One other aspect, which can be underlined, is the input inductor which is much smaller (not only in value but also in size and price) than that used in the classical method: few miliHenry compared to tens of Henry.

Based on these positive results, it is intended to develop a much higher power model in the range of hundreds of kW. This will use a multi-level unity power factor rectifier in order to increase the voltage at the

capacitive divider pickup point and keep the current to reasonable levels for semiconductor devices.

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