GENERALISED VOLTAGE CONTROL FOR A MULTI-PURPOSE SWITCHING MODE CONVERTER

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Abstract: In this paper, a single-phase switching mode converter acting as a unity power factor rectifier and/or as active power filter with no alteration in the topology is studied. A generalised voltage control taking in consideration the output power of the DC bus is developed. To demonstrate the improved response of the voltage regulator, a battery charger as "unknown dc load" is used.

Key Words: Harmonics ; active filter ; power factor correction; control.

1. INTRODUCTION

The classical AC/DC converters draw a non-sinusoidal current from the source. The presence of wide band current harmonics produces high losses for transformers and power lines creating overvoltages, overheating and finally can destroy unprotected equipment. It has became more and more essential to reduce the harmonics to acceptable levels recommended by standards such as IEC 1000-3-2 or EN60555.

Passive LC filters have traditionally been used to attenuate harmonics and improve the input power factor. Due to the progress in power electronic devices and control, the pulse width modulation converters (PWM) working as shunt active power filters (APF) or as unity power factor rectifiers (UPFR) seem the right solution to reduce the harmonic level in the line current [1-4].

The integrated power quality has been studied in [8]. The problem of duality of APF/UPFR has not been very well clarified. In this paper a single-phase full bridge converter with a proper control for current and voltage is considered in order to simultaneously perform both functions of UPFR and APF without any alteration in the electric diagram.

2. SYSTEM CONFIGURATION

The proposed system is presented in Fig. 1. The central component of the system is a full bridge switching mode converter built with MOSFETs and designed for safe operation up to 2kW. The connection with the ac supply network is realised via the inductance Z_F (L_F, R_F). The condenser C represents the storage element.
If the non-linear load doesn't draw any current, the system acts as a unity power factor rectifier, supplying known (resistive) or unknown (dc pulsating current) loads.
As input parameters for the control system, a minimal solution was used: supply current, supply voltage, dc bus voltage and current.

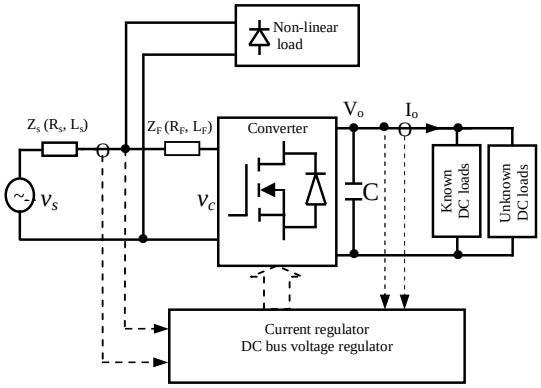

Figure 1. Block diagram of the proposed system

In the presence of a distorted current drawn by the non-linear load and with the dc load disconnected, the system performs as an active power filter, compensating current harmonics and the fundamental reactive power.

The system can simultaneously perform the both functions of APF and UPFR. To simulate the proposed solution, Matlab with Power System Blockset has been used.

3. CONTROL SYSTEM

The main structure of the control system is a current controller as an inner loop and a voltage controller that should keep the dc voltage constant across the storage element (C). As inner loop the resonant current regulator [5] was chosen. This is a variant of

PWM for current control, based on an analogue feedback loop linked with an oscillator. The advantages of this controller are: high dynamic current regulation loop, low sensitivity to the load's electrical parameters and the maximum switching frequency is controlled.

3.1. Power Balance Principle

The power balance is considered in order to analyze the variations of the voltage across the storage element C. From this analysis we can find the system' modeling related with the active power exchange between the supply, non-linear load and active power converter.

Neglecting the losses of the H converter we can write the relation between the instantaneous power delivered by the supply (p_s) and the instantaneous power drawn by the non-linear load (p_n) and the active converter (p_c):

$$p_s = p_n + p_c \tag{1}$$

After the harmonic content of the non-linear load is compensated (the supply current is sinusoidal and in phase with the voltage) we can write:

$$2\hat{V}_s\hat{I}_s = \frac{1}{C}\cdot\frac{d}{dt}\left(V_o^2\right) + V_o I_o \tag{2}$$

$$\Delta I_c = \frac{V_o}{4 f_c L_F} \tag{3}$$

$$v_s(t) = R_s i_s + L_s\frac{di_s}{dt} - R_F i_c - L_F\frac{di_c}{dt} + v_c \tag{4}$$

$$V_o \geq \sqrt{V_s^2 + (\omega L_F I_c)^2} \tag{5}$$

Where $\boldsymbol{v_c}$, $\boldsymbol{i_c}$ and ΔI_c are the voltage and current/ripple at the input of the active power converter, and V_o and I_o are the dc output parameters. The dc voltage V_o should comply with the controllability criteria (5).

3.2. Voltage Regulator

The power balance principle has been studied before [7]. In this paper a simpler controller is proposed with very good results. The basic structure of the voltage controller is presented in the figure 2.

The active power $P_L(s) = dI$ drawn by the non-linear load is considered as an internal perturbation of the system because its variation can influence the controlled dc bus $V_o^2(s)$. The term $\boldsymbol{d}E$ is regarded as an external perturbation and is the ripple created by the distorted power $\tilde{p}_L(t)$. The controller cannot reject the ripple due to the harmonic power. This ripple should be diminished by means of a low-pass filter.

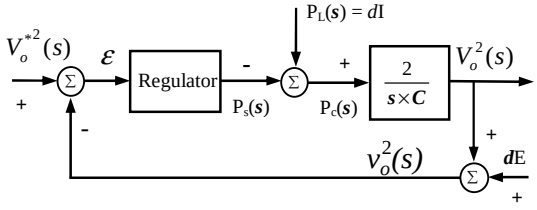

Figure 2. Voltage controller: basic structure

The majority of authors utilize a PI regulator. But the closed-loop transfer function of this type of regulator has two zeros:

$$\frac{V_o^2}{V_o^{*2}} = \frac{\left(k_i + s\times k_p\right)\left(1 + s\times\tau\right)}{s^3\times\left(\frac{\tau C}{2}\right) + s^2\times\frac{C}{2} + s\times k_p + k_i} \tag{6}$$

An integral/proportional (fig.3) solution was chosen for the regulator [6].

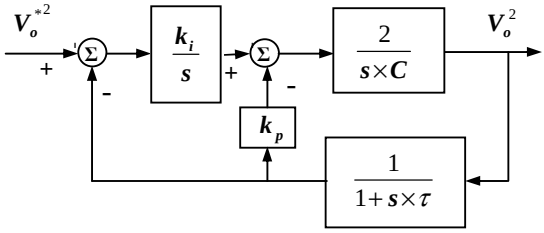

Figure 3. IP voltage regulator

The closed-loop transfer function of the system is:

$$\frac{V_o^2}{V_o^{*2}} = \frac{1 + s\times\tau}{s^3\left(\frac{\tau\times C}{2k_i}\right) + s^2\left(\frac{C}{2k_i}\right) + s\left(\frac{k_p}{k_i}\right) + 1} \tag{7}$$

The equation (7) shows that the IP solution cancels a slow zero from the transfer function improving the dynamics of the regulator.

If the poles of the system (p_0, p_1 and p_2) are placed on the Butterworth circle with the radius ω_o: $s_o = -\omega_o$, $s_1 = \omega_o e^{j\frac{3\pi}{4}}$ and $s_2 = \omega_o e^{-j\frac{3\pi}{4}}$, then the coefficients k_p and k_i are:

$$k_p = \frac{C}{2\times\left(1+\sqrt{2}\right)\times\tau} \tag{8}$$

$$k_i = \frac{C}{2\times\left(1+\sqrt{2}\right)^3\times\tau^2} \tag{9}$$

3.3. Generalised Voltage Regulator

The regulator presented in the figure 3 is very well applicable to the APF function. But when considering the UPFR function, then one should also consider the dc power delivered to the dc load, see equation (2). If an equivalent resistance R parallel to the capacitor C substitutes the dc load, then using the same procedure as for equations (6) to (9) the new coefficients of the IP regulator can be written:

$$k_i' = \frac{(T+\tau)^3}{T^2\tau^2\left(1+\sqrt{2}\right)^3 R} \quad (10)$$

$$k_p' = \frac{1}{R}\left(\frac{(T+\tau)^2}{\left(1+\sqrt{2}\right)T\tau} - 1\right) \quad (11)$$

Where T =RC and τ is the constant of the low-pass filter. The important aspect to be noticed for this approach is that the regulator coefficients should be corrected every time when the dc load is changed.

In order to address this drawback, a dc power estimator (using the dc bus voltage and current via a current sensor R_T) working as feed-forward is introduced in the diagram of the voltage regulator (figure 4). The principle of feed-forward was studied in [3] but only using current information.

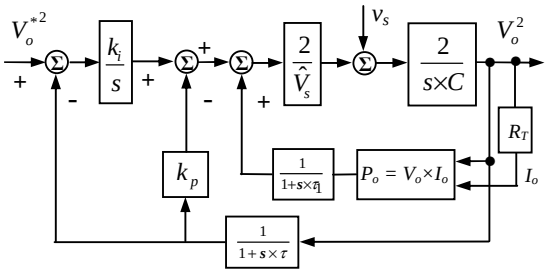

Figure 4. Block diagram for the generalized voltage regulator

As can be seen, the dynamic of the regulator depends on the capacitor C and the time constant τ, thus on the choice of the cut-off frequency of the low-pass filter. Since the main function is to force the input current to have a sinusoidal shape related to the line frequency, then the low pass filter cut-off frequency of the voltage regulator is recommended to be between 0.33 and 0.5 from the line frequency [3].

The time constant τ_1 does not affect the performance of the voltage regulator in the APF mode as will be shown.

A large value of the capacitor C can reduce the ripple of the dc bus, but also reduces the dynamic of the regulator. If the dynamic of the regulator is too slow, then the harmonic compensation will be affected. As a compromise between the ripple and dynamic, a value of C = 1000μF was chosen.

The other parameters of the platform are: V_s = 220V/50Hz, R_s = 1mΩ, R_F = 50mΩ, L_s = 0.1mH and L_F = 10mH.

4. APF FUNCTION

In the APF mode, the control system should determine the reference current, in this case i_s and to keep the dc voltage constant across the storage element C.

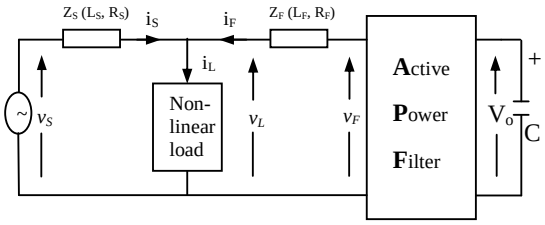

Figure 5. APF- block diagram

The converter must produce a current equal and in opposite phase with the harmonic current content in the non-linear current i_L. The input inductance L_F limits the approximation band of the current delivered by the APF (3).

As was mentioned before, in this application the source current is directly controlled. The output of the voltage regulator gives the information about the active part of the fundamental current ($\hat{I}_s^*$). Then, by means of multiplication with a sinusoidal signal of unity amplitude in phase with the supply voltage, we get the reference for the current regulator.

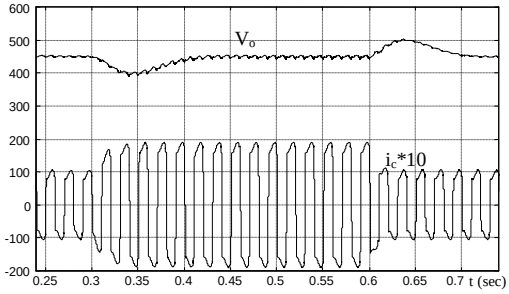

Figure 6. APF Dynamic response of the voltage regulator

The dynamic response of the voltage regulation in APF mode is presented in the figure 6. The simulation result shows a fairly small deviation of V_o (less than 7%) for a ΔI_L=10A impact of a non-linear current.

After compensation, the source current is sinusoidal and in phase with the supply voltage. Its THD decreases from 35% (before compensation) to less than 1% (after compensation) see figure 7. Figure 8 shows how the supply current i_s follow the reference i_{sref} and the waveform of the compensating current provided by the APF.

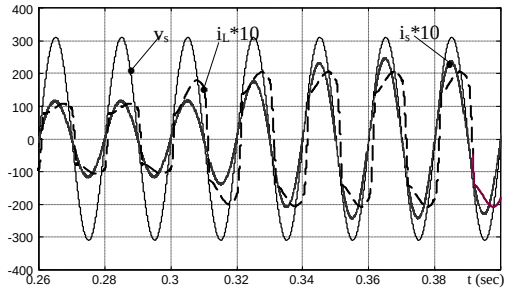

Figure 7. APF Non linear current impact

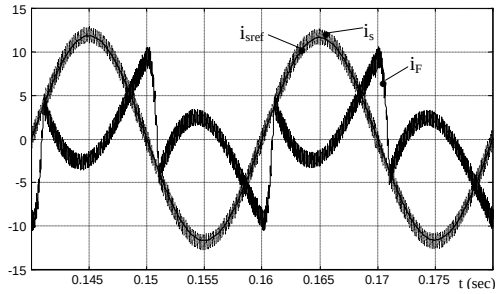

Figure 8. APF Current tracking in steady-state

5. UPFR FUNCTION

In the UPFR mode (figure 9), the converter transfers the electric energy from the ac supply to a dc load, but keeping a sinusoidal shape of the input current.

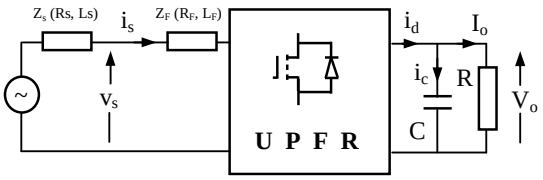

Figure 9. UPFR block diagram

The simulation results under transient conditions of the UPFR function using a simple IP regulator (figure 3 with coefficients given by eq.10 and 11) are presented in figures 10 and 11. The resistance R was modified from 100Ω to 200Ω.

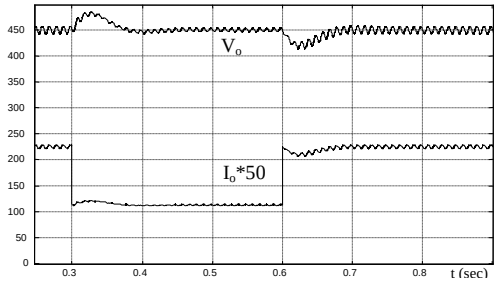

Figure 10. IP Regulator : dynamic response

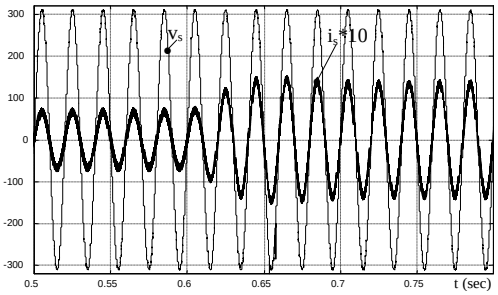

Figure 11. IP Regulator: supply current

The simulations were performed under the same conditions as before (the load resistor is modified from 100Ω to 200Ω) using the generalised voltage controller and the results are presented in figures 12 and 13.

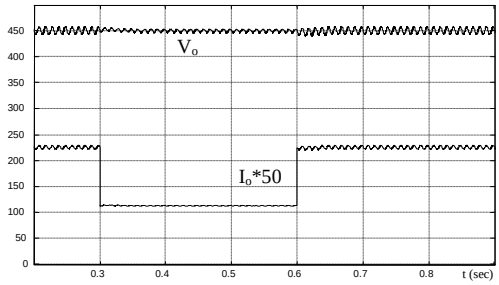

Figure 12. Generalised voltage regulator : dynamic response

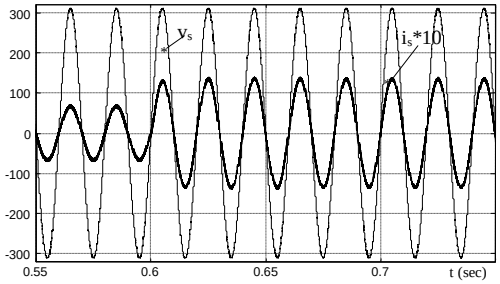

Figure 13. Generalised voltage regulator : supply current

The new waveforms of the UPFR are dramatically improved due to the feed-forward power compensation: the variation of Vo is reduced to nothing and the time response is quasi null (figure 12). The supply current is perfectly sinusoidal and in phase with the voltage (figure 13).

6. COMBINED MODE (APF/UPFR)

The main test of the proposed model was to prove the simultaneity of the operation as the active power filter and unity power factor rectifier.

Having the converter in APF function with a non-linear current of about 10A amplitude and 35% distortion contend, a step of 2.25A dc current was drawn from the output. The simulation results are presented in the figures 14 and 15 and prove the feasibility of this mode and the effectiveness of the control.

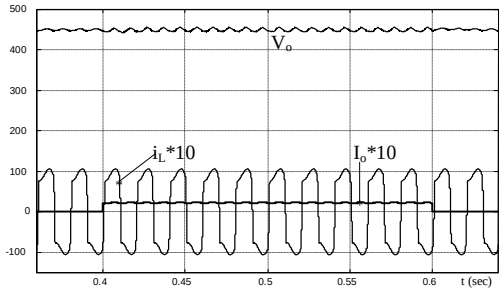

Figure 14. Generalised voltage controller : dynamic response

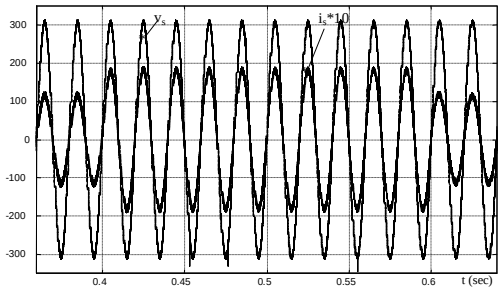

Figure 15. Generalised voltage controller : supply current

Apparently the bandwidth of the power estimator could influence the function of the APF. As can be seen in the figure 15, the shape of supply current is perfect sinusoidal and in phase with the supply voltage. The simultaneously functioning was obtained with no change in the parameters of the voltage controller.

7. BATTERY CHARGER MODE

In order to create an unknown very constraining current (I_o), a switching mode battery charger was implemented to work in conjunction with UPFR. The block diagram of the battery charger is presented in figure 16. The switch S and the current regulator force I_{ch} to be constant during the operation. For the battery, a very simple r_b, C, E series equivalent circuit is used.

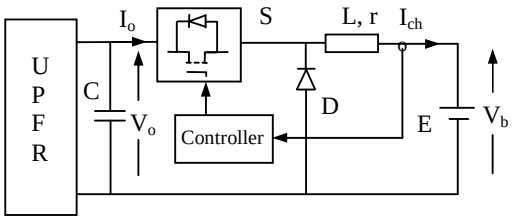

Figure 16. Battery charger-bloc diagram

The value of capacitance C was taken as 0.1F in order to have a reasonable simulation time, the voltage V_o is equal to 450V and E is fixed to 144V. The inductance used is L = 10mH, the resistance r = 1Ω (r includes the resistance of the switch and the internal resistance of the battery r_b) and the switching frequency was 10 kHz.

The charging current is kept constant using a simple PI regulator where the dominating pole of the smoothing inductance is compensated. A low-pass filter is used to reduce the influence of the switching frequency.

The behaviour of the UPFR in conjunction with a dc pulsating current provided by the battery charger is illustrated in figures 17 and 18. The graph of the voltage V_o (figure 17) shows a low under shoot and over-shoot for a step-change of the battery charging current, proving the positive influence of the feed-forward compensation. The supply current i_s keeps a good sinusoidal shape in phase with supply voltage v_s (figure 18).

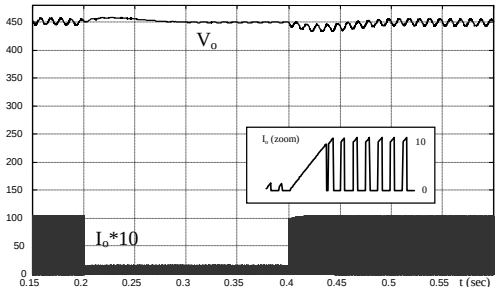

Figure 17. UPFR with 'dc pulsating load' : dynamic responce

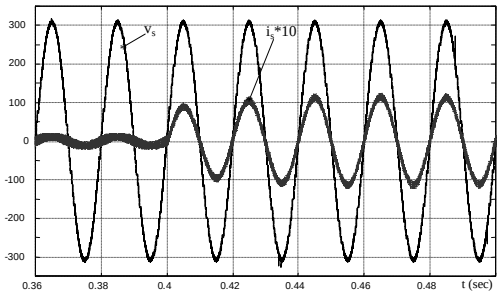

Figure 18. UPFR with 'dc pulsating load' : supply current

The performances of the battery charger are presented in figure 19. Due to the simple model used for the battery, V_b increase linearly. The charging current is constant and the source current is sinusoidal.

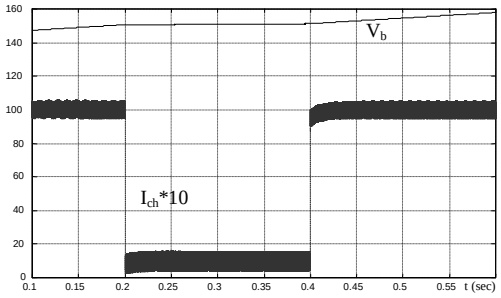

Figure 19. Charging parameters of the battery

8. CONCLUSIONS

The use of a switching mode converter as a front-end stage can ensure a sinusoidal source current in phase with the voltage. A proper control can make the converter operate in both modes of APF and/or UPFR without any alteration in the electric diagram. The source current is maintained sinusoidal and in phase with the voltage irrespective of the type of load current (linear or not) connected to the point of common connection or on the dc bus. The simulation results show good performances both in steady state and transient conditions.

9. ACKNOWLEGMENT

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