1 RF IC Performance Optimization by Synthesizing Optimum Inductors

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Abstract Even with optimal system design and careful choice of topology for a particular RF application, large amounts of energy are often wasted due to low-quality passives, especially inductors. Inductors have traditionally been difficult to integrate due to their inherent low quality factors and modelling complexity. Furthermore, although many different inductor configurations are available for an RF designer to explore, support for integrated inductors in electronic design automation tools and process design kits has been very limited in the past. In this chapter, a recent advance in technology-aware integrated inductor design is presented, where drawbacks of the integrated inductor design are addressed by introducing an equation-based inductor synthesis algorithm. The intelligent computation technique aims to allow RF designers to optimize integrated inductors, given the inductor center frequency dictated by the device application, and geometry constraints. This does not only lay down a foundation for system-level RF circuit performance optimization, but, because inductors are often the largest parts of an RF system, it also allows for optimal usage of chip real estate.

1.1 Introduction

With technology scaling, it has become possible to integrate an ever-increasing number of devices into the same integrated circuit (IC), thus making systems-on-chip more compact and affordable. Specific integrated radio-frequency (RF) circuits, particularly transmitters, are often power hungry, and therefore it is paramount to design these circuits so that they operate at the maximum attainable efficiency to conserve battery power and reduce heat emissions. Sub-optimal design is still one of the major problems in integrated circuits. Even with optimal system design and careful choice of topology for the particular application, large amounts of energy are often wasted due to low-quality passives, especially inductors.

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Inductors have traditionally been difficult to integrate due to their inherent low quality factors and modelling complexity. Furthermore, although many different inductor configurations are available for an RF designer to explore, support for integrated inductors in electronic design automation (EDA) tools and process design kits has been very limited in the past. Some vendors provide a library of several qualified integrated inductors for each RF-capable process. Each of these inductors operates at its peak efficiency only at a certain frequency, making the library impractical for many applications. Other vendors provide p-cells of spiral inductors, and although technology parameters are taken into account to calculate the resulting quality factors for a specific frequency, there is still a distinct lack of technology-aware optimization. It is more practical, yet tedious, to use such p-cells, owing to the cut-and-try nature of this approach to inductor selection and the lack of automated design flow. In this chapter, a recent advance in technology-aware integrated inductor design is presented, where designers are supported by an equation-based inductor synthesis algorithm. The computation technique aims to allow RF designers to optimize integrated inductors, given the inductor center frequency dictated by the device application, and the geometry constraints. This does not only lay down a foundation for system-level RF circuit performance optimization, but, because inductors are often the largest parts of an RF system, it also allows for optimal usage of chip real estate.

The chapter first introduces inductor theory and describes various integrated inductor options. The second part of the chapter introduces the theory of spiral inductor design, inductor modelling, and ways in which this theory can be used in inductor synthesis. In the central part of the chapter, a methodology for design, computation and optimization of planar spiral inductors is presented. The methodology provides for an intelligent search through inductor configurations fitting the initial choices. Based on the selected model, the algorithm will compute optimal inductors, together with inductance, quality factors, schematics and layouts and intelligently select the configuration with the best performance. The algorithm is only introduced as an illustration of an inductor synthesis methodology, the theory of which can be expanded to any integrated inductor configuration.

1.2 Inductor Theory

A real inductor is usually modelled as an ideal inductor L_S in series with a resistor R_S, both in parallel with capacitor C_S, as shown in Fig. 1.1 (Ludwig and Bretchko, 2000). Inclusion of the series resistor and parallel capacitor is necessary to model the losses of the inductor even at frequencies below RF because the quality or Q-factor is generally much lower for the inductor than for other passive components. The Q-factor of the inductor is defined as 2π times the ratio of energy stored in the device and energy lost in one oscillation cycle. If Z is defined as the impedance of an inductor, then the Q-factor is given by

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}. \tag{1}$$

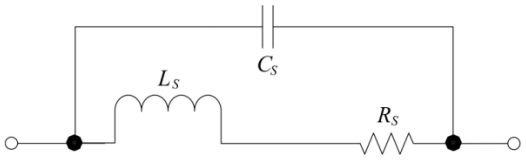


Fig. 1.1 General high-frequency model of an inductor (Ludwig and Bretchko 2000)

For the simple circuit in Fig. 1.1, (1) reduces to

$$Q = \frac{X}{R_S}, \tag{2}$$

where X is the total reactance of the inductor. The Q-factor is heavily dependent on the frequency and exhibits a peak Q_{max}.

While an ideal inductor exhibits a constant impedance value for all frequencies, every non-ideal inductor exhibits an impedance value dependent on frequency, as shown in Fig. 1.2. The frequency where magnitude of impedance ($|Z|$) peaks is called the resonant frequency of an inductor. The resonant frequency, $f_r = \frac{1}{2\pi\sqrt{L_S C_S}}$, should ideally peak at infinity, but the finite value of the peak is due to the resistance R_S. Similarly, capacitance C_S is the reason the inductor exhibits capacitive instead of inductive behavior at frequencies above the resonance.

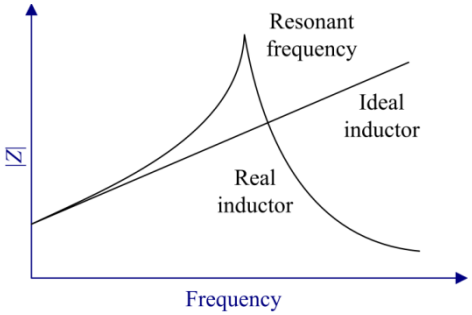


Fig. 1.2 Frequency response of the impedance of ideal and real inductors (Ludwig and Bretchko 2000)

1.2.1 Inductor Implementation Options

As will become apparent later in this chapter, the geometry of choice for the topic of this chapter is the integrated planar spiral inductor topology. Various factors, such as inductor size and lower Q-factor of integrated passive inductors, often result in one of the following inductor alternative implementations:

- External inductors,
- Active integrated inductors,

- Microelectromechanical systems (MEMS) inductors,
- Bond wires, or
- Other on-chip or on-package/in-package implementations.

Each of the above possibilities is discussed in more detail in the sections that follow.

External inductors

External or off-chip inductors are connected to a system outside of the integrated **e**circuit (IC) package. They are usually implemented as a solenoidal coil or a toroid. Their usage at high frequencies also implies careful printed-circuit board (PCB) modelling and design. Although high-quality inductors are widely available from suppliers, their inductance values are usually limited to standard values of 10 nH and higher. The frequency of the Q-factor peak (typically in the range of hundreds) is also predefined and is usually located in either the high-megahertz or the low-gigahertz range. Another drawback for integrated design is the fact that the value obtained upon PCB placement will differ from the rated value due to parasitics involving PCB tracks, IC bonding, and other factors.

Integrated Active Inductors

Integrated active inductors are a good alternative to their passive counterparts because of their higher Q-factor. Typical Q-factors that can be obtained for active configurations are between 10 and 100, which is up to ten times those of spiral inductors (Uyanik and Tarim 2007). Active inductors can also take up a smaller area on the chip than spiral inductors. The main disadvantages of active inductors include increased power consumption, presence of electrical noise from active devices and limited dynamic range. A design requiring only six transistors has been proposed in Ler *et al.* 2008.

MEMS Inductors

MEMS is an IC fabrication technique that empowers conventional two-dimensional (2-D) circuits to expand into the third dimension (3-D) (De Los Santos 2001). This principle becomes particularly useful in inductor fabrication, because the influence of substrate parasitics on the Q-factor can be reduced significantly when silicon below the inductor is effectively replaced by air or another material that has lower relative permittivity. Typical obtainable Qs range from 10 to 30 for 1 nH inductors at multi-gigahertz frequencies. An example of a high-Q silicon-based inductor using polymer cavity can be found in Khoo *et al.* (2012). As an alternative to spiral MEMS inductors, solenoidal inductors suspended on-chip can be used with various degrees of chip stability (Gu and Li 2007). Several advantages over conventional spiral inductors can be identified, which include a lower stray capacitance due to the fact that only a part of the inductor is lying on the silicon substrate, a simple design equation and greater possibilities for flexible layout. Out-of-plane inductors (Chua *et al.* 2003) are similar to MEMS inductors,

but their coils are fabricated using stress-engineered thin films. The stress gradient is induced by changing the ambient pressure during film deposition. When released, a stress-graded film curls up in a circular trajectory. The typical Q-factor of this configuration is over 70 at 1 GHz.

Although MEMS devices present an attractive alternative to conventional passive inductors, particularly because of the high Q-factors, their fabrication requires process changes or modifications to the wafer after fabrication. After these procedures, repeatability (Foty 2008) is not assured.

Bond Wires

Bond wires, which usually present a parasitic quantity for signals transmitted between systems inside and outside the packaged device, reflect inductive behavior (Murad *et al.* 2010) which can be used as an advantage in RF design. Electrical characteristics of bond wires depend on the material of which they are made and their cross-section, the height above the die plane, the horizontal length and the pitch between the adjacent wires (Khatri *et al.* 2008). Many of these characteristics are dependent on pad location and type of package, but if these parameters are known in advance of design, bond-wire models can be used accurately to determine bond-wire Q-factor and inductance. Although bond wires with Q-factors of 50 have been reported, their inductances will typically be less than 1 nH (Khatri *et al.* 2008). This limits their feasibility for gigahertz range where well-controlled inductances of 1 nH and more are often needed.

Other On-Chip Implementations

Masu *et al.* (2006) discusses two types of inductor not commonly found in literature. The first type of inductor is a meander inductor. It is a flat passive inductor consisting of a long piece of metal that is not wound as in the case of the spiral inductor which will be described in detail later, but meanders similarly to rivers in their lower watercourses. This inductor occupies a small area and no underpass is needed, but its measured Q-factor is quite low (about 2.1 for inductance of 1.3 nH). Such trade-off between the area and Q-factor is acceptable for matching network applications. The second type of inductor is a snake inductor that meanders into the third dimension.

Vroubel *et al.* (2004) discusses electrically tunable solenoidal on-chip inductors. Other tunable inductors are commonly seen as implemented in active configuration, such as in the case of the inductor in Seo *et al.* (2007).

Toroid inductors can also be implemented on-chip by means of micromachining (Zine-El-Abidine and Okoniewski 2007).

1.2.2 Spiral Inductor Theory

Although inductor implementations described in the previous section are widely used due to their advantages over passive integrated inductors, they are normally too complex to implement, due to process changes and post-fabrication requirements, which in turn increase total RF device manufacturing cost. Spiral integrat-

ed inductors present a viable option for practical RF implementations when designed with the aid of the inductor optimization technique described in this chapter. This is due to the deterministic models that can be used to accurately predict the inductance value and Q-factors of any inductive structure on chip, given the process parameters and geometry of that inductive structure.

Common Spiral Inductor Geometries

Several spiral inductor geometries are commonly used in RF circuits. These include square and circular inductors, as well as various polygons (Mohan *et al.* 1999). The square spiral has traditionally been more popular since some IC processes constrained all angles to 90° (Niknejad and Meyer 2000), but it generally has a lower Q-factor than the circular spiral, which most closely resembles the common off-chip solenoidal inductors but is difficult to layout. A polygon spiral is a compromise between the two. Drawings of square and circular inductors are shown in Fig. 1.3.

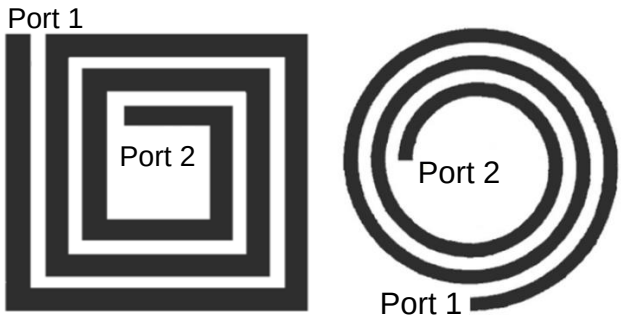


Fig. 1.3 The square (a) and circular (b) spiral inductors (Niknejad and Meyer 2000)

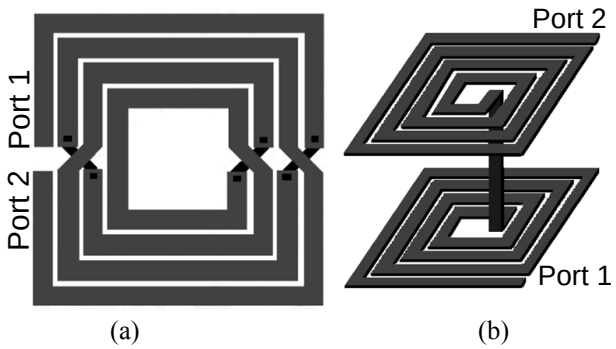


Fig. 1.4 The symmetrical (Niknejad and Meyer 2000) (a) and two-layer (b) (Xu *et al.* 2012) spiral inductor

The geometries shown in Fig 1.3 are asymmetric, and require only a single metal layer for fabrication. Additional layers are only needed to bring the signal lines to the outside of an inductor and are universally known as underpasses. Symmetrical inductors are also possible, but they require more than one underpass, in this case known as metal-level interchange, shown in Fig. 1.4 (a) (Niknejad and Meyer 2000). Alternatively, the second metal layer can be used as part of the core of the inductors. An example of such multilayer geometry is a two-layer square inductor shown in Fig. 1.4 (b) (Xu *et al.* 2012). The multi-layer geometries can deliver higher quality factors than a single layer inductor due to mutual inductance coupling of different spirals.

Another common geometry is a taper geometry, where inner spirals of inductors decrease in width in respect of the outer spirals (Pei *et al.* 2011) (Fig. 1.5). Tapering is done to suppress eddy current losses in the inner turns in order to increase the Q-factor, but it is most effective when substrate losses are negligible.

Spiral Inductor Geometry Parameters

For a given geometry, a spiral inductor is fully specified by the number of turns (n), the turn width (w) and two of the following: inner, outer or average diameter (d_{in}, d_{out} or $d_{avg} = (d_{in} + d_{out})/2$), as shown in Fig. 1.6 for the square and circular inductors. Spacing between turns, s, can be calculated from other geometry parameters. Another geometry parameter commonly used in equations is the fill ratio, defined as

$$\rho_{fill} = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \,. \tag{3}$$

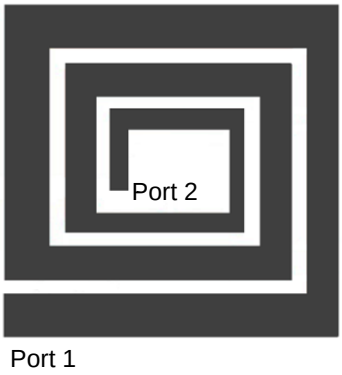
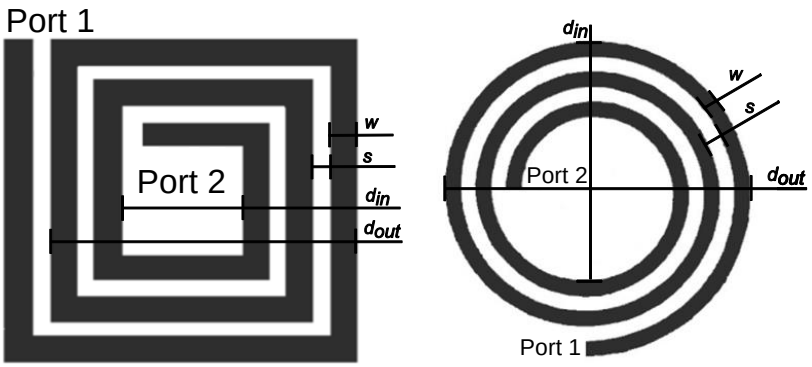


Fig. 1.5 A taper spiral inductor (Pei *et al.* 2011)

The total length of a spiral is also important for calculations. It is dependent on inductor geometry. For a square inductor, it can be calculated as

$$l = 4(d_{in} + w) + 2n(2n-1)(s+w) \,. \tag{4}$$



(a) (b)

Fig. 1.6 Geometry parameters of the (a) square and (b) circular spiral inductors

Spiral Inductor Models

Several spiral inductor models are widely used, depending on the required modelling complexity. In this section, single-π, segmented, double-π and third-order models will be described.

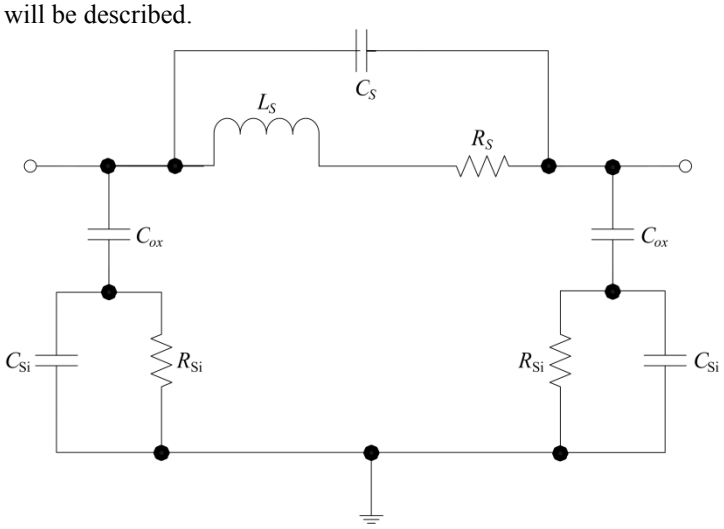


Fig. 1.7 A commonly used nine-component spiral inductor model (Mohan *et al.* 1999)

Single-π Model The most commonly used model is a lumped single-π nine-component configuration shown in Fig. 1.7 (Wang *et al.* 2013, Mohan *et al.* 1999). In this model, L_S is the inductance at the given frequency, R_S is the parasitic resistance and C_S is the parasitic capacitance of the spiral inductor structure. C_{ox} is the parasitic capacitance due to oxide layers directly under the metal inductor spi-

ral. Finally, C_{Si} and R_{Si} represent the parasitic resistance and capacitance due to the silicon substrate. This topology does not model the distributive capacitive effects, but it models correctly for parasitic effects of the metal spiral and the oxide below the spiral, as well as for substrate effects.

Segmented Model A somewhat more complicated model is the model presented by Koutsoyannopoulos and Papananos (2000). Each segment of the inductor is modelled separately with a circuit shown in Fig. 1.8. In this model, parasitics C_{ox}, C_{Si} and R_{Si} represent parasitics of only one inductor segment, L_S and R_S represent inductance and parasitic capacitance of one segment coupled to all segments, whilst capacitances C_{f1} and C_{f2} are added to represent coupling to adjacent segment nodes.

Double-π Distributed Model The standard single-π model can also be extended into a second-order, distributed double-π model shown in Fig. 1.9 (Wang *et al.* 2013, Watson *et al.* 2004). A second-order ladder (with third grounded branch) is used to model the distributive characteristics of metal windings. The interwinding capacitance (C_w) is included to model the capacitive effects between metal windings of the inductor. The transformer loops (M_{S1} and M_{S2}) represent the effects of frequency-dependent series loss.

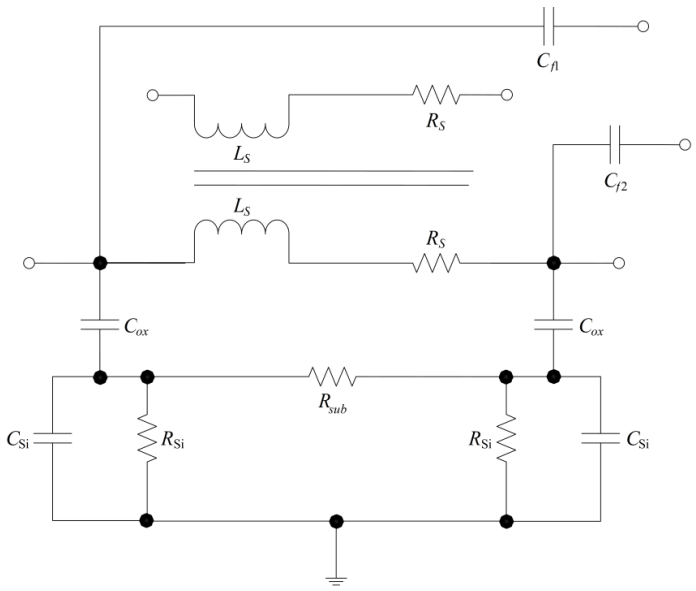


Fig. 1.8 An equivalent two-port model for one segment of a spiral inductor (Koutsoyannopoulos and Papananos 2000)

Third-Order Transmission-Line Model The second-order model shown in Fig. 1.9 is valid for the inductor up to the first resonance frequency. If a third-order model is used, it is possible to predict inductor behavior accurately, even beyond

the resonant frequency. One such model is presented by Lee *et al.* (2006). An equivalent circuit diagram for this configuration is shown in Fig. 1.10. Extrinsic admittances are used and all circuit components are self-explanatory from this figure.

Computation of Series Inductance and Parasitics for Single-π Model

The single-π inductor model of Fig. 1.7 is sufficient to model spiral inductors accurately for frequencies below resonance (Wang *et al.* 2012). This model can be used as proof of concept when developing a routine for spiral inductor design and optimization. In sections that follow, series inductance L_S, as well as parasitic capacitances and resistances shown in this figure, together with their influence of inductor performance, are described and explained.

Series Inductance (L_S) Various equations are commonly used in literature to represent the series inductance of spiral inductors with various levels of accuracy.

The modified Wheeler equation is based on the equation derived by Wheeler in 1928 (Mohan *et al*. 1999):

$$L_{mw} = K_1 \mu \frac{n^2 d_{avg}}{1 + K_2 \rho_{fill}}, \tag{5}$$

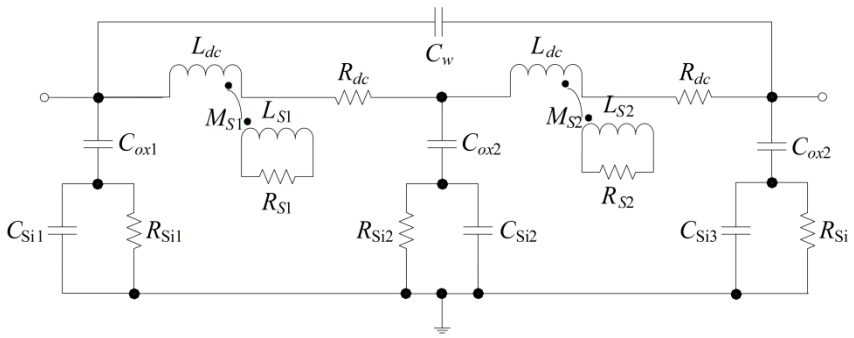


Fig. 1.9 A double-π distributed inductor model (Watson *et al.* 2004)

Here, K_1 and K_2 are geometry-dependent coefficients with values defined in Table 1.1 and μ is magnetic permeability of the metal layer.

Another expression can be obtained by approximating the sides of the spiral by symmetrical current sheets of equivalent current densities as described in (Mohan *et al.* 1999):

$$L_{gmd} = \mu \frac{n^2 d_{avg} c_1}{2} \left[\ln \frac{c_2}{\rho} + c_3 \rho_{fill} + c_4 \rho_{fill}^{\ 2} \right]. \tag{6}$$

Here, c_1, c_2, c_3 and c_4 are geometry-dependent coefficients with values defined in Table 1.2. This expression exhibits a maximum error of 8% for $s \leq 3w$.

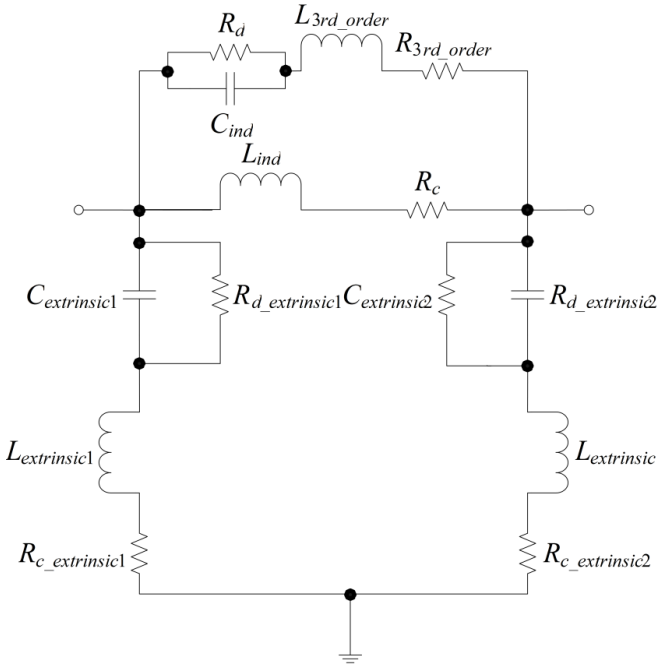


Fig. 1.10 A complete third-order inductor model (Lee *et al.* 2006)

Table 1.1. Coefficients for the modified Wheeler expression (Mohan et al. 1999)

Layout	K_1	K_2
Square	2.34	2.75
Octagonal	2.33	3.82
Hexagonal	2.25	3.55

Table 1.2 Coefficients for the current sheet expression (Mohan et al. 1999)

Layout	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circular	1.00	2.46	0.00	0.20

Bryan's equation is another popular expression for the square spiral inductance (Musunuri *et al.* 2005):

$$L = 0.00241\left(\frac{d_{out}+d_{in}}{4}\right)n^{\frac{5}{3}}\ln\left(\frac{4}{\rho_{fill}}\right). \tag{7}$$

The data-fitted monomial expression results in an error smaller than seen in the expressions given above (typically less than 3%). It is based on a data-fitting technique. Inductance in nanohenries (nH) is calculated as (Mohan *et al.* 1999, Musunuri *et al.* 2005):

$$L_{mon} = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}, \tag{8}$$

where coefficients β, α_1, α_2, α_3, α_4 and α_5 are once again geometry dependent, as presented in Table 1.3.

The monomial expression has been developed by curve fitting over a family of 19000 inductors (Mohan *et al.* 1999). It has better accuracy and higher simplicity than the equations described above, and is the equation of choice.

Table 1.3. Coefficients for the spiral inductor inductance calculation (Mohan et al. 1999)

Layout	β	α_1 (d_{out})	α_2 (w)	α_3 (d_{avg})	α_4 (n)	α_5 (s)
Square	$1.62 \cdot 10^{-3}$	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	$1.28 \cdot 10^{-3}$	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	$1.33 \cdot 10^{-3}$	-1.21	-0.163	2.43	1.75	-0.049

Parasitic Resistance (R_S) Parasitic resistance is dependent on the frequency of operation. At DC, this value is mostly determined by the sheet resistance of the material of which the wire is made. At high frequencies, this is surpassed by the resistance that arises due to the formation of eddy currents. It is governed by the resistivity of the metal layer in which the inductor is laid out (ρ), the total length of all inductor segments (l), the width of the inductor (w) and its effective thickness (t_{eff}) (Yue and Wong 2000):

$$R_S = \frac{\rho l}{w t_{eff}}. \tag{9}$$

Effective thickness, t_{eff}, is dependent on the actual thickness of the metal layer, t:

$$t_{eff} = \delta(1 - e^{-t/\delta}), \tag{10}$$

where δ is skin depth related to frequency f via relation

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}. \tag{11}$$

Parasitic Capacitance (C_S) Parasitic capacitance is the sum of all overlap capacitances created between the spiral and the underpass. If there is only one underpass and it has the same width as the spiral, then the capacitance is equal to (Yue and Wong 2000)

$$C_S = n w^2 \frac{\varepsilon_{ox}}{t_{oxM1-M2}}, \tag{12}$$

where $t_{oxM1\text{-}M2}$ is the oxide thickness between the spiral and the underpass and ε_{ox} is the dielectric constant of the oxide layer between the two metals.

Oxide and Substrate Parasitics (C_{ox}, C_{Si} and R_{Si}) The oxide and substrate parasitics are approximately proportional to the area of the inductor spiral ($l \cdot w$), but are also highly dependent on the conductivity of the substrate and the operating frequency. In order to calculate the oxide capacitance C_{ox} and substrate capacitance C_{Si}, the effective thickness (t_{eff}) and effective dielectric constant (ε_{eff}) of either oxide or substrate must be determined. The effective thickness is calculated as (Huo *et al.* 2006)

$$t_{eff} = w\left[\frac{w}{t} + 2.42 - 0.44\frac{t}{w} + \left(1 - \frac{t}{w}\right)^6\right]^{-1}, \text{ for } \frac{t}{w} \le 1, \tag{13}$$

or

$$t_{eff} = \frac{w}{2\pi}\ln\left(\frac{8t}{w} + \frac{4w}{t}\right), \text{ for } \frac{t}{w} \ge 1 \tag{14}$$

for both oxide and substrate. The effective dielectric constant is determined as

$$\varepsilon_{eff} = \frac{1+\varepsilon}{2} + \frac{\varepsilon - 1}{2}\left(1 + \frac{10t}{w}\right)^{-\frac{1}{2}} . \tag{15}$$

Then,

$$C_{ox} = \frac{wl\varepsilon_0\varepsilon_{effox}}{t_{effox}} \tag{16}$$

and

$$C_{Si} = \frac{wl\varepsilon_0\varepsilon_{effSi}}{t_{effoxSi}} . \tag{17}$$

In addition to the effective thickness (t_{eff}) given in (14), to calculate R_{Si}, the effective conductivity (σ_{eff}) of the substrate is needed. The effective conductivity can be obtained from

$$\sigma_{eff} = \sigma\left[\frac{1}{2} + \frac{1}{2}\left(1 + \frac{10t}{w}\right)^{-\frac{1}{2}}\right], \tag{18}$$

where $\sigma = \frac{1}{\rho}$ represents the substrate conductivity.

Therefore,

$$R_{Si} = \frac{t_{effSi}}{\sigma_{eff} wl} . \tag{19}$$

Quality Factor and Resonance Frequency for Single-π Model

As discussed at the beginning of the chapter, the quality factor is the measure of performance of any inductor. For the single-π model, if R_P and C_P are defined as

$$R_P = \frac{1}{\omega^2 C_{ox}{}^2 R_{\mathrm{Si}}} + \frac{R_{\mathrm{Si}}\left(C_{ox}+C_{\mathrm{Si}}\right)^2}{C_{ox}{}^2} \tag{20}$$

and

$$C_P = C_{ox}\cdot\frac{1+\omega^2\left(C_{ox}+C_{\mathrm{Si}}\right)C_{\mathrm{Si}}R_{\mathrm{Si}}{}^2}{1+\omega^2\left(C_{ox}+C_{\mathrm{Si}}\right)^2 R_{\mathrm{Si}}{}^2}, \tag{21}$$

then the Q-factor can be calculated as (Lee *et al.* 2005)

$$Q = \frac{\omega L_S}{R_S}\cdot\frac{R_P}{R_P+\left[\left(\frac{\omega L_S}{R_S}\right)^2+1\right]R_S}\cdot\left[1-\left(C_P+C_S\right)\cdot\left(\omega^2 L_S+\frac{R_S{}^2}{L_S}\right)\right], \tag{22}$$

where $\omega = 2\pi f$. Three different factors can be isolated in (20) (Sun *et al.* 2008). The first factor, $F_1 = \omega L_S / R_S$, is the intrinsic (nominal) Q-factor of the overall inductance. The second factor, $F_2 = \dfrac{R_P}{R_P+\left[\left(\omega L_S/R_S\right)^2+1\right]R_S}$, models the substrate loss in the semiconducting silicon substrate. The last factor, $F_3 = 1-\left(C_P+C_S\right)\cdot\left(\omega^2 L_S + R_S{}^2/L_S\right)$, models the self-resonance loss due to total capacitance $C_P + C_S$. This resonant frequency can be isolated by equating the last factor to zero, and solving for ω. This results in the formula for self-resonance frequency of the spiral inductor:

$$f_r = \frac{\omega_o}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{1}{L_S\cdot\left(C_P+C_S\right)}-\left(\frac{R_S}{L_S}\right)^2}\ . \tag{23}$$

At low frequencies, the loss of metal line (F_1) restricts the performance of inductors (Xue *et al.* 2008). In high-frequency ranges, the loss of substrate (F_2) prevails as the restricting factor. F_2 is greatly dependent on the conductivity of the substrate. As conductivity increases at a fixed frequency, the skin depth of the substrate also increases, leading to an increase of eddy currents in the substrate resulting in a decrease of the Q-factor of the inductor. Heavily doped substrates are usually used in a submicron process, with substrate resistivity usually lying in the range of 10 Ω·cm to 30 Ω·cm. As a result, in the traditional (Bi)CMOS process, the performance of spiral inductors is limited by the substrate. Inductors laid out in

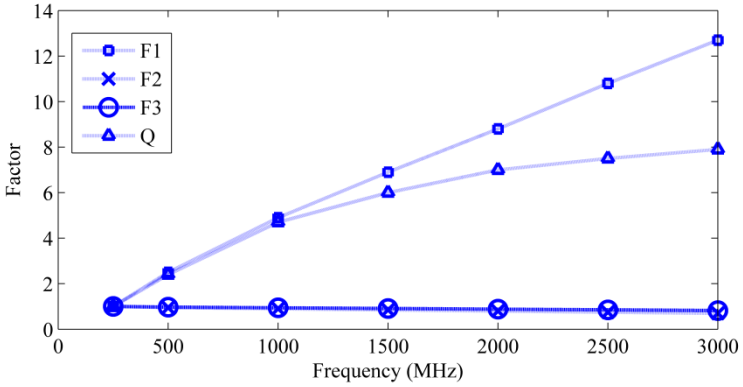
MEMS processes, as mentioned earlier in this chapter, strive to minimize the effects of this limitation.

Figure 1.11 shows the analysis of factors F_1, F_2 and F_3 defined in (20) for 1 nH and 5 nH sample spiral inductors optimized at different frequencies for their highest quality operation. It can be observed that, although the nominal Q-factor (F_1) increases with frequency, F_2 and F_3 decrease in the same range, resulting in the decrease of the overall Q-factor (Q) at frequencies above 1 GHz.

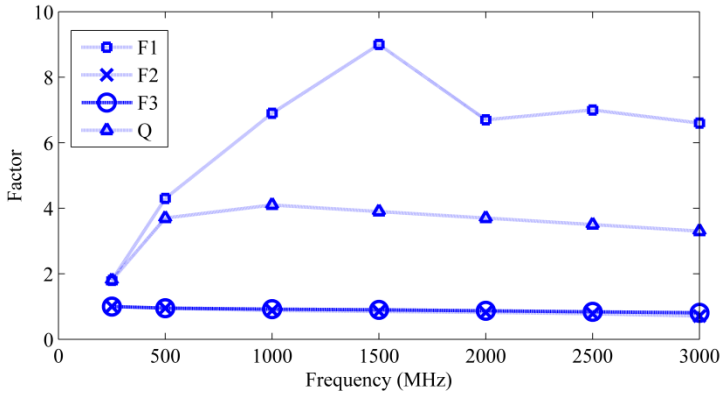
Close to resonant frequency, the frequency has some effect on the apparent inductance value, which can be calculated from (austriamicrosystems 2005)

$$L_{eff} = \frac{\mathrm{Im}(Z)}{2\pi f_r}, \tag{24}$$

where Z is the total impedance of the single-π-modelled inductor with its one port grounded.



(a)



(b)

Fig. 1.11 Analysis of the determining factors of the Q-factor equation for (a) 1 nH inductor and (b) 5 nH inductor

Current Approach to Spiral Inductor Design

When designing an integrated capacitor, a designer may simply increase or decrease the area of the component until the required capacitance is obtained. Although capacitance of the parallel plate capacitor does not solely depend on the area of its plates, but also on other factors such as fringing effects, a nearly linear relationship between the two is retained. A similar relationship between the length and total resistance holds for resistors. By modifying the length of a part of the process layer used for fabrication of the resistor, a designer can obtain the desired value of its resistance. However, this does not apply to the spiral inductors. Contrary to common sense, one cannot just simply increase the number of turns or the width of a single turn to change the inductance. The complicated inductance relationship given in (22) can illustrate this interdependency. This complexity of spiral inductor models is one of the reasons why various cut-and-try approaches are used in practice, such as the one illustrated by the flow chart in Fig. 1.12.

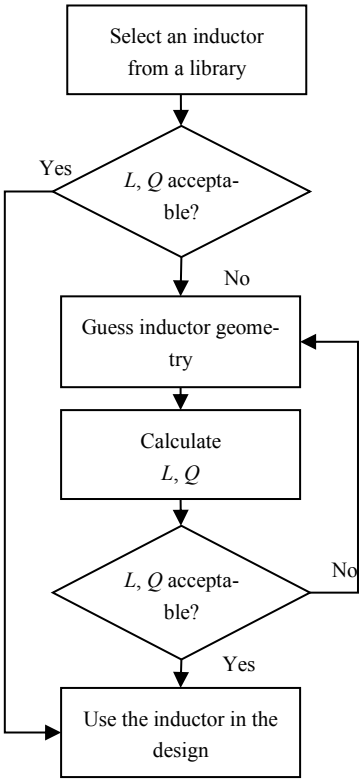


Fig. 1.12 A flow chart of conventional spiral inductor design procedure

In this typical approach, designer chooses an inductor from a library if it contains one with acceptable inductance and Q-factor. Most likely this inductor will not be available, in which case he or she has to guess inductor geometry then calculate its L and Q, decide on whether these parameters are acceptable, and if not, repeat the guessing process until a satisfactory inductor is found. This process, even if calculations are performed by means of software such as MATLAB[2] or inductors are simulated in electromagnetic (EM) simulation software, could take substantial amount of time.

Guidelines for Integrating Spiral Inductors

As detailed in the introductory section of this chapter, although spiral inductors are a good choice for exclusively on-chip RF circuits, their implementation is not as straightforward. The inductors occupy large areas on the chip, suffer from low-quality factors, and are difficult to design for low tolerance. Hastings (2006) isolates some general guidelines that can assist in increasing the quality of an inductor, irrespective of its geometry and its model. These guidelines were adhered to throughout this chapter:

1. Where possible, one should use the highest resistivity substrate available. This will reduce the eddy losses that reduce the Q-factor.
2. Inductors should be placed on the highest possible metal layers. In this way, substrate parasitics will have a less prominent role because the inductor will be further away from the silicon.
3. If necessary, parallel metal layers for the body of the inductor may be used to reduce the sheet resistance.
4. Unconnected metal should be placed at least five turn widths away from inductors. This is another technique that helps to reduce eddy current losses.
5. Excessively wide or narrow turn widths should be avoided. Narrow turns have high resistances, and wide turns are vulnerable to current crowding.
6. The narrowest possible spacing between the turns should be maintained. Narrow spacing enhances magnetic coupling between the turns, resulting in higher inductance and Q-factor values.
7. Filling the entire inductor with turns should be avoided. Inner turns are prone to the magnetic field, again resulting in eddy current losses.
8. Placing of unrelated metal plates above or under inductors should be avoided. Ungrounded metal plates will also aid the eddy currents to build up.
9. Placing of junctions beneath the inductor should be avoided. The presence of a junction close to the inductor can produce unwanted coupling of AC signals.

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[2] MATLAB is a technical computing language from MathWorks: http://www.mathworks.com/

10. Short and narrow inductor leads should be used. The leads will inevitably produce parasitics of their own.

1.3 Method for Designing Spiral Inductors

In this section, an improvement to the common iterative procedure described previously is proposed. The proposed software routine can find an inductor close to the specified value, with the highest possible Q-factor, occupying a limited area, and using predetermined technology layers (synthesis of the inductor structure). For completeness and verification purposes, inductances and Q-factor values of various spiral inductors can be calculated if the geometry parameters of such inductors are given (analysis of inductor structure). Analysis and synthesis concepts are developed for the single-square spiral inductor of Fig. 1.6 (a), using equations for single-π model, but they can be extended to other geometries and more complex models.

In the text that follows, input and output parameters of the routine are given, together with its flow.

1.3.1 Input Parameters

Parameters for accurate inductor modelling can be divided into two groups: geometry and process parameters. Process parameters are related to the fabrication process (technology) in which the IC is to be prototyped and the designer has very little, if any, control over them. Geometry parameters can be understood as user parameters because they are related to the specific application required by the designer. In addition, the frequency of operation of the inductor also needs to be known for applicable Q-factor calculation. When providing user parameters, general guidelines for the inductor design presented in the previous section need to be followed where possible.

The following subsections give a detailed description of the parameters needed for the spiral inductor design.

Geometry Parameters

For the analysis of an inductor structure, the following input geometry parameters are necessary:

- Outer diameter, d_{out} (μm);
- Inner diameter, d_{in} (μm);
- Turn width, w (μm); and
- Number of turns, n.

For the synthesis of the inductor structure, only constraints for the geometry should be specified (all in micrometer):

- Minimum value of inner diameter, $d_{in(min)}$;
- Maximum value of outer diameter, $d_{out(max)}$;

- Minimum value for turn spacing, s_{min}; and
- Minimum turn width, w_{min}.

Tolerance (in percentage) for the acceptable inductance values, as well as grid resolution (in micrometer), is also required for the synthesis part of the routine. For the inductor to pass design-rule-checks (DRC), design rules document provided by the foundry has to be consulted, with emphasis for maximum allowed grid resolution and minimum allowed metal spacings (including s_{min}) for all used metal layers (both in μm).

Table 1.4 summarizes the geometry input parameters.

Table 1.4 Geometry parameters for the spiral inductor design

Parameter	Units	Geometry/inductance known
Outer diameter (d_{out})	μm	Geometry
Inner diameter (d_{in})	μm	Geometry
Turn width (w)	μm	Geometry
Number of turns (n)	-	Geometry
Minimum value of the inner diameter	μm	Inductance
Maximum value of the outer diameter	μm	Inductance
Minimum value for turn spacing (s)	μm	Inductance
Minimum turn width	μm	Inductance
Inductance value tolerance	%	Inductance
Grid resolution	μm	Inductance

Process (Technology) Parameters

The inductance value of a high-Q structure is predominantly determined by its geometry. However, the silicon substrate introduces process-dependent parasitics, which are dependent on the process parameters. They decrease the Q-factor and add shift to the inductance value. The following substrate parameters need to be specified:

- Thickness of the metal in which the inductor spiral is laid out, t (nm);
- Resistivity of the metal used for the spiral, ρ (Ω·m);
- Permeability of the metal used for the spiral, μ (H/m);
- Thickness of the oxide between the two top metals, t_m (nm);
- Relative permittivity of the oxide between the two top metals, ε_{rm};
- Thickness of the oxide between the substrate and the top metal, t_{sm} (nm);
- Relative permittivity of the oxide between the substrate and the top metal, ε_{rs};
- Thickness of the silicon substrate, t_{Si} (μm);
- Relative permittivity of the silicon substrate, ε_{rSi}; and
- Resistivity of the silicon substrate, ρ_{Si} (Ω·m).

The process parameters can normally be obtained or calculated from parameters obtained in the datasheets supplied by the process foundry. Table 1.5 summarizes the technology input parameters.

Operating Frequency (f_0)

Operating frequency may be understood as the frequency at which the Q-factor will be highest for a particular geometry. For devices such as power amplifiers (PAs) or low-noise amplifiers (LNAs), the operating frequency is the center frequency of the channel.

Table 1.5. Process parameters for the spiral inductor design

Parameter	Unit
Thickness of metal in which the inductor spiral is laid out	nm
Resistivity of metal used for the spiral (ρ)	Ω·m
Permeability of metal used for the spiral (μ)	H/m
Thickness of oxide between the two top metals (t_m)	nm
Relative permittivity of oxide between the two top metals (ε_{rm})	-
Thickness of oxide between substrate and top metal (t_{sm})	nm
Relative permittivity of oxide between substrate and top metal (ε_{rm})	-
Thickness of the silicon substrate (t_{Si})	μm
Relative permittivity of the silicon substrate (ε_{rSi})	-
Resistivity of the silicon substrate (ρ_{Si})	Ω·m

1.3.2 Description and Flow Diagrams of Inductor Design Routine

The inductor design software routine consists of analysis and synthesis parts. Complete flow diagram of this routine is given in Fig. 1.13 (Božanić and Sinha 2009/I, Božanić and Sinha 2009/II).

Analysis part of the routine is selected when user decides to provide inductor geometry parameters. Following this choice, a set of calculations that utilizes equations for the single-π inductor model is performed. This model is simple yet accurate enough for the proof of concept. Nominal inductance is calculated by means of the data-fitted monomial equation as specified by (8), where coefficients are specified in Table 1.3. Parasitics are calculated by utilizing (9) to (19). Q-factor and resonance frequency are calculated by (20) to (23) and the apparent inductance at a particular frequency is calculated by (24).

Synthesis part of the routine is selected when user decides to provide inductance and required tolerance, constraining geometry detail as well as grid accuracy. In this case, an intelligent search algorithm shown in Fig. 1.13 is invoked. The search algorithm looks into a range of possible geometries and identifies a geometry that will result in the required inductance with high Q-factor within a certain tolerance.

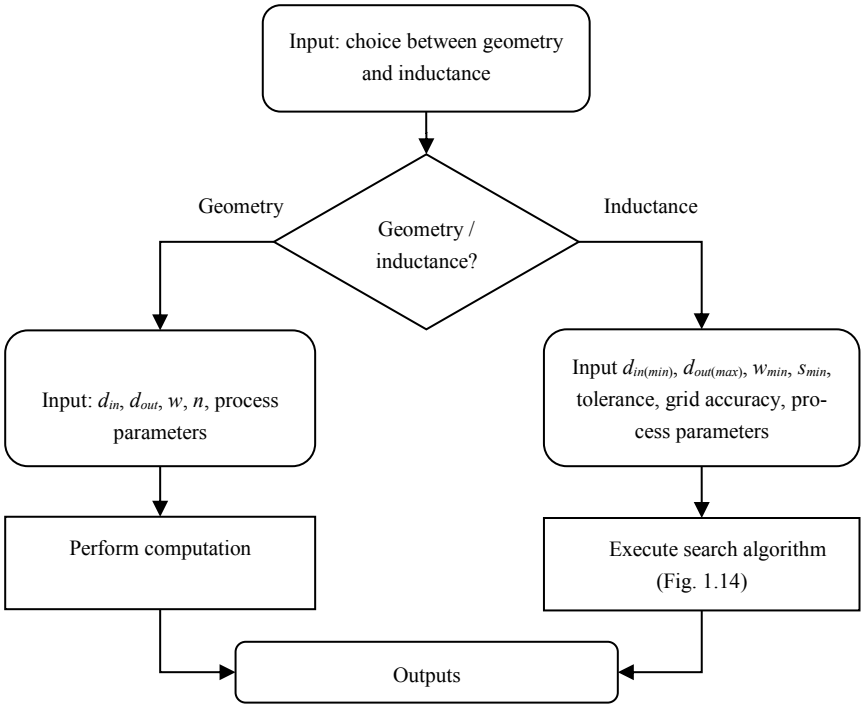

Fig. 1.13. Flow diagram of the inductor design routine

Synthesis algorithm in Fig. 1.13 commences by first computing constraints based on the geometry inputs, such as minimum and maximum number of turns (n), minimum and maximum inner (d_{in}) and outer (d_{out}) diameter values and spiral width (w) in order to minimize the search space. The same equations used in the analysis part of the routine, (9) to (24), are used to compute inductance and quality factors of the minimum inductor geometry. Spacing between the turns s is then set to the minimum spacing that is feasible because densely spaced spirals are known to have the highest inductance. This in turn decreases the number of degrees of freedom and therefore the number of loops in the algorithm. Grid resolution is set and search commences. Each of n, w and d_{in} are then increased in a specific order and L and Q are calculated for each step. Steps are chosen such that the whole allowed search space is covered but no unnecessary calculations are performed.

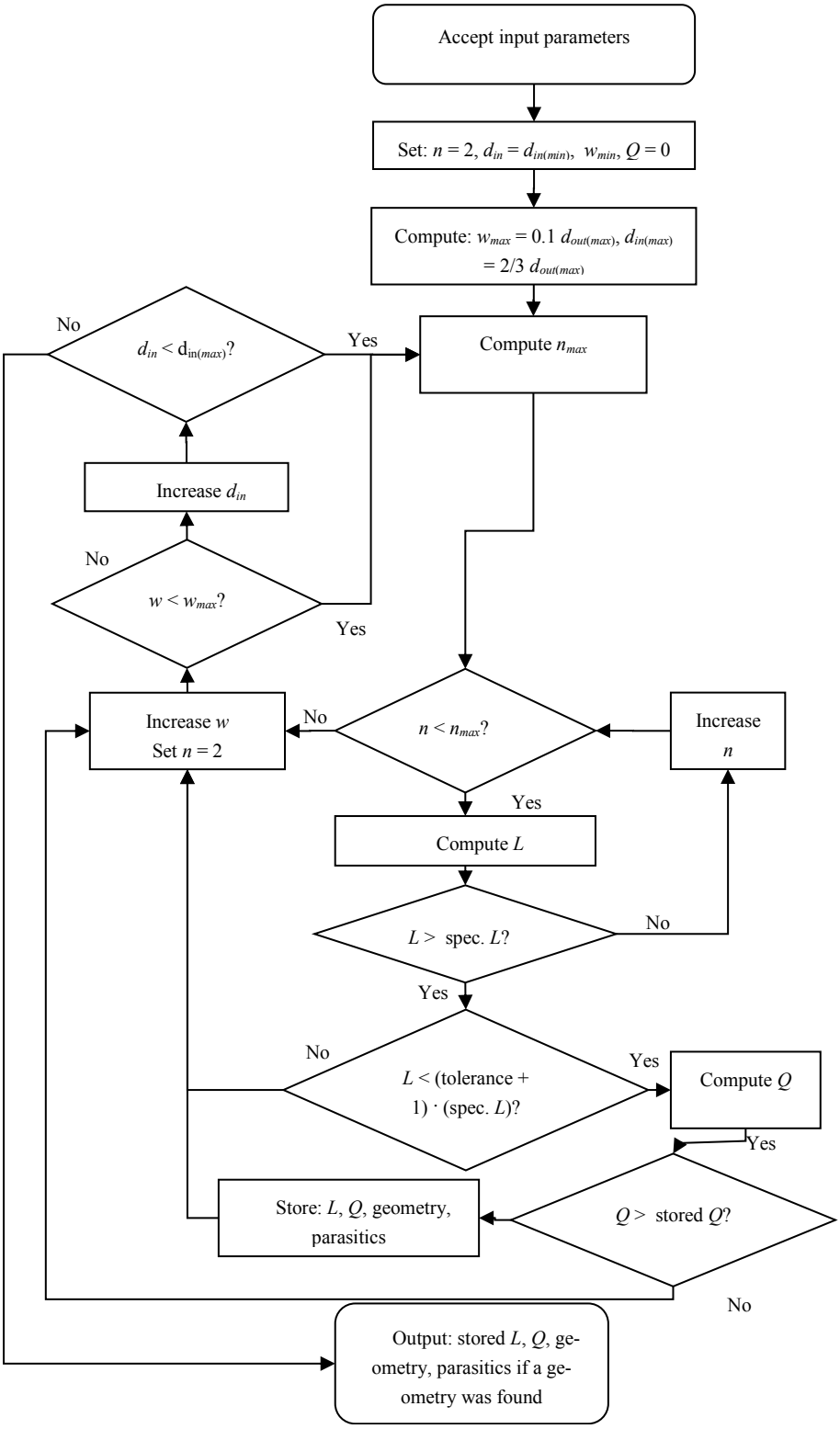

Fig. 1.14 Flow diagram of the inductance search algorithm

While more than one geometry will result in the tolerant inductance at a given frequency, each of these geometries will have a different Q-factor. The geometry that gives the highest Q-factor is chosen by the algorithm as its output. Accuracy of the algorithm depends on the tolerance for the required inductance values and on the search grid resolution. Although resolution is specified by the user, it cannot be chosen to be higher than allowed by the process design rules. Higher tolerance of the inductance value will result in less accurate inductance values, but there will be a greater probability that high-Q (or any) inductor geometry resulting in the particular inductance will be found with a lower grid resolution. This probability can again be increased by increasing the grid resolution, but with this increase, the time of execution and memory requirements of the search algorithm will also increase. It is up to users to decide which combination of inductance tolerance and grid resolution will be appropriate for a specific application. Time analysis of the calculation effort on two different systems for the synthesis of a typical 2 nH inductor in the ams AG (formerly austriamicrosystems) 0.35 μm BiCMOS S35 process, for various tolerances and grid resolutions, is given Table 1.6. This table also illustrates other trade-offs of different settings. It is clear from this analysis, that higher grid resolution (in this case resolution higher than 1 μm) does not add to the quality of synthesized inductors and therefore time consumed for the inductor synthesis is acceptable even for the older system.

To illustrate how a programming or scripting language can be used to automate the process, the MATLAB code for the inductance search algorithm is provided in Figures 1.15 and 1.16. MATLAB is only used as an example because the authors believe that many readers of this text would have at least a basic knowledge of the language. Alternatively, any programming or scripting language may be used for this purpose.

1.3.3 Design Outputs

The following quantities are numerical outputs of the inductor design routine that will be valuable for the RF designer:

1. Effective inductance value of the inductor at the operating frequency, L_S (nH);
2. Nominal inductance value of the inductor ($Q \rightarrow \infty$), L_{inf} (nH);
3. Q-factor of the inductor at the operating frequency, Q;
4. Resonant frequency of the inductor, f_r (GHz);
5. Width of the spiral (μm);
6. Spacing between the turns of the spiral (μm);
7. Input diameter of the spiral (μm);
8. Output diameter of the spiral (μm); and
9. Number of turns of the spiral.

Table 1.6 Analysis of computational efforts and trade-offs of different grid resolution and tolerance settings for the synthesis of a 2 nH inductor

Grid	Tolerance / System	0.1 % Time (s)	0.1 % Q-factor	0.5 % Time (s)	0.5 % Q-factor	1 % Time (s)	1 % Q-factor	5 % Time (s)	5 % Q-factor
0.1 µm	Core2duo	147	6.82	147	6.82	147	6.82	151	6.82
	i7	55.6		55.7		55.5		56.7	
0.2 µm	Core2duo	36.7	6.82	36.7	6.82	36.9	6.82	36.8	6.82
	i7	14.4		14.7		14.6		14.8	
0.5 µm	Core2duo	6.01	6.82	5.98	6.82	5.99	6.82	5.97	6.82
	i7	3.62		3.08		2.81		2.79	
1 µm	Core2duo	1.54	6.78	1.57	6.81	1.58	6.81	1.54	6.81
	i7	1.17		1.09		1.19		1.19	
2 µm	Core2duo	Not found	-	0.435	6.81	0.435	6.81	0.438	6.81
	i7	Not found		0.483		0.478		0.521	
5 µm	Core2duo	Not found	-	0.116	4.82	0.121	6.78	0.112	6.78
	i7	Not found		0.181		0.178		1.175	

1.1 Verification of the Spiral Inductor Model and the Inductance Search Algorithm

The inductance search algorithm was used to design ten metal-three (3M) and ten thick-metal (TM) inductors fabricated over a standard resistivity substrate at common frequencies of 1, 2, 2.4 and 5 GHz in the ams AG S35 process. The smallest inductor value designed for was 0.5 nH, followed by nine inductors in increments of 0.5 nH. Table 1.7 and Table 1.8 show geometric parameters, low-frequency inductance values and the Q-factor of each designed 3M and TM inductor respectively. To verify the predicted values, EM simulation on the designed inductors was performed in Virtuoso Spiral Inductor Modeler (Zhu 2000). The solver for the Spiral Inductor Modeler employs Partial Element Equivalent Circuit (PEEC) algorithm in the generation of macromodels for the spiral components. Electro-static and magneto-static EM solvers are invoked separately to extract the capacitive and inductive parameters of the spiral inductor structure. A process file with information on metal and dielectric layers was required by the modeler and it needed to be manually created.

```
%This procedure searches for the inductance geometry with the
%highest quality factor given the inductance
%Initialize all storage variables to zero
Qstored = 0; fostored = 0; Lcstored =0; Rsstored = 0; RSistored =
0; CSistored = 0; Coxstored = 0; Csstored = 0; wstored = 0;
sstored = 0; dinstored = 0; doutstored = 0; nstored = 0;
fprintf('\nLooking for geometry with highest Q-factor...\n\n');
%Initialize geometry parameters to default minimum/maximum values
Lc = 0;
dout = 0;
s = smin;
din = dinmin;
w = wmin;
n = 2;
%Inductance search algorithm
while (din < 2*doutmax/3)
  s = smin;
  w = wmin;
  while (w <= doutmax/10)
    n = 2;
    dout = 0;
    while (dout < doutmax)
      dout = din + 2*n*w + 2*(n-1)*s;
      if (dout > doutmax)
        break
      end%if
      davg = (din + dout) / 2;
      Lc = b * dout^a1 * w^a2 * davg^a3 * n^a4 * s^a5;
      calcParasitics; %Procedure to calc parasitics
      Lcc = Lc/1e9;
      Lzz = Lz*1e9;
      if (Lzz > Ls)
         if (Lzz < (1 + tolerance) * Ls)
           %Calculate Q-factor
           Rp = 1/(omega^2*Cox^2*RSi) + RSi*(Cox + CSi)^2/Cox^2;
           Cp = Cox*(1 + omega^2*(Cox + CSi)*CSi*RSi^2)/(1 +
omega^2*(Cox + CSi)^2*RSi^2);
           Q = omega*Lcc/Rs*Rp/(Rp + ((omega*Lcc/Rs)^2 +
1)*Rs)*(1 - (Cp + Cs)*(omega^2*Lcc + Rs^2/Lcc));
           fo = 1/(2*pi)*sqrt(1/(Lcc*(Cp + Cs)) - (Rs/Lcc)^2);
           if (Q > Qstored)
             Qstored = Q; fostored = fo; Lclfstored = Lc;
             Lcstored = Lzz; Rsstored = Rs; RSistored = RSi;
             CSistored = CSi; Coxstored = Cox; Csstored = Cs;
             wstored = w; sstored = s; dinstored = din;
             doutstored = dout; nstored = n;
           end%if
         end%if
         Lc = 0;
         n = 1;
         break
       end%if
       n = n + 1;
     end%while
     w = w + resolution;
```

Fig. 1.15 MATLAB code for the inductance search algorithm

```
  din = din + resolution;
end%while
%==== OUTPUT PARAMS ====%
if Qstored < 1
   fprintf('Could not find a geometry for %.2f nH\nlimited to
dinmin and doutmax with Q greater than 1 at %.2f MHz.\n', Ls,
f/1e6)
end%if
if Qstored >=1
  fprintf('Ls = %.2f nH \n', Lcstored);
  fprintf('Lslf = %.2f nH \n', Lclfstored);
  fprintf('Q = %.2f \n', floor(100 * Qstored + 0.5) / 100);
  fprintf('fo = %.2f GHz\n', floor(fostored/1e7 + 0.5) / 100);
  fprintf('w = %.2f um\n', floor(100*wstored + 0.5) / 100);
  fprintf('s = %.2f um\n', floor(100*sstored + 0.5) / 100);
  fprintf('din = %.2f um\n', floor(100*dinstored + 0.5) / 100);
  fprintf('dout = %.2f um\n', floor(100*doutstored + 0.5) / 100);
  fprintf('n = %d\n', floor(100*nstored + 0.5) / 100);
end%if
```

Fig. 1.16 MATLAB code for the inductance search algorithm (continued)

Aforementioned tables show that inductance values obtained using the inductor design routine correspond with simulated inductance values. Good correspondence between predicted and simulated values in terms of Q-factor values exists for 3M inductors as well, whereas in the case of TM inductors, simulated Q-factors are larger than those of the calculated Q-factors. This discrepancy can be explained: as the impedance of parasitic elements in the *RL* model of the spiral (with oxide and substrate effects ignored) approaches that of inductive reactance near the peak frequency, the model yields a pessimistic estimate of the actual Q-factor of the spiral (IBM Corporation 2008). 3M inductors lie closer to the substrate and have larger resistances than TM inductors, so this effect is less prominent. The fact that the Q-factor is underestimated rather than overestimated is an advantage, since the TM inductors designed by the inductor design routine will perform better than predicted, which will be acceptable in many cases. Where higher accuracy is needed, the use of one of the more detailed models may be explored.

Furthermore, inductance routine was used to predict inductances and Q-factors of several spiral inductor geometries provided and measured by ams AG. The measurement results showed that inductance values are correctly predicted (within 3.7 %) by the inductor models used for the inductance search algorithm with Q-factors exhibiting the same behavior as shown by EM simulations. Details of this study can be found in Božanić and Sinha (2009/I).

Table 1.7 Metal-3 inductors designed with inductance search algorithm

Frequency (GHz)	Nominal inductance (nH)	Calculated LF inductance (nH)	Calculated Q	EM inductance (nH)	EM Q	d_{out} (μm)	d_{in} (μm)	w (μm)	s (μm)	n
1	0.5	0.50	3.37	0.50	3.00	220	30	47	1	2
1	1	1.00	4.63	0.94	4.15	291	93	49	1	2
1	1.5	1.48	5.22	1.40	4.75	347	149	49	1	2
1	2	1.95	5.47	1.90	5.11	397	199	49	1	2
1	2.5	2.39	5.50	2.33	2.33	441	243	49	1	2
1	3	2.83	5.39	2.75	5.27	483	285	49	1	2
1	3.5	3.29	5.10	3.22	3.22	500	326	43	1	2
1	4	3.67	4.80	3.52	4.52	426	164	43	1	3
1	4.5	4.12	4.66	3.97	4.56	427	189	39	1	3
1	5	4.55	4.60	4.52	4.41	431	211	36	1	3
2	0.5	0.49	5.79	0.45	4.29	210	32	55	1	2
2	1	0.97	7.16	0.91	5.92	288	90	49	1	2
2	1.5	1.41	6.89	1.32	6.11	339	141	49	1	2
2	2	1.86	6.24	1.73	6.23	349	191	39	1	2
2	2.5	2.32	5.64	2.26	5.68	363	233	32	1	2
2	3	2.76	5.12	2.72	5.27	384	270	28	1	2
2	3.5	3.21	4.81	3.01	5.33	276	152	20	1	3
2	4	3.65	4.53	3.45	5.19	283	171	18	1	3
2	4.5	4.06	4.27	3.86	4.98	294	188	17	1	3
2	5	4.51	4.05	4.35	4.76	241	123	14	1	4
2.4	0.5	0.49	6.72	0.45	4.94	216	30	46	1	2
2.4	1	0.95	7.63	0.90	6.38	286	88	49	1	2
2.4	1.5	1.39	6.95	1.34	6.34	316	142	43	1	2
2.4	2	1.86	6.18	1.82	6.25	320	190	32	1	2
2.4	2.5	2.30	5.51	2.26	5.47	339	229	27	1	2
2.4	3	2.76	5.04	2.71	5.32	249	131	19	1	3
2.4	3.5	3.17	4.69	3.12	4.89	262	150	18	1	3
2.4	4	3.61	4.39	3.59	4.74	262	168	15	1	3
2.4	4.5	4.03	4.12	4.03	4.60	220	110	13	1	4
2.4	5	4.47	3.91	4.50	4.55	216	122	11	1	4
5	0.5	0.47	9.48	0.41	6.05	200	30	42	1	2
5	1	0.92	8.22	0.88	6.93	209	95	28	1	2
5	1.5	1.36	6.76	1.34	5.88	222	140	20	1	2
5	2	1.81	5.71	1.80	5.48	169	87	13	1	3
5	2.5	2.22	5.03	2.20	5.15	176	106	11	1	3
5	3	2.60	4.46	2.59	4.45	186	122	10	1	3
5	3.5	2.97	4.02	2.96	4.03	160	82	9	1	4
5	4	3.46	3.70	3.52	4.43	148	94	6	1	4
5	4.5	3.98	3.43	4.07	4.30	141	103	4	1	4
5	5	4.29	3.27	4.42	4.24	106	38	4	1	7

Table 1.8 Thick-metal inductors designed with inductance search algorithm.

Frequency(GHz)	Nominal inductance (nH)	Calculated LF inductance (nH)	Calculated Q	EM inductance (nH)	EM Q	d_{out} (μm)	d_{in} (μm)	w (μm)	s (μm)	n
1	0.5	0.50	7.43	0.38	4.71	216	30	48	2	2
1	1	0.99	10.1	0.93	8.13	299	95	50	2	2
1	1.5	1.47	11.1	1.39	9.96	355	151	50	2	2
1	2	1.95	11.5	1.84	11.1	406	202	50	2	2
1	2.5	2.39	11.4	2.30	11.7	451	247	50	2	2
1	3	2.81	10.9	2.70	12.0	493	289	50	2	2
1	3.5	3.29	10.3	3.20	11.6	499	331	41	2	2
1	4	3.71	9.78	3.49	9.62	403	173	37	2	3
1	4.5	4.17	9.49	3.95	9.89	409	197	34	2	3
1	5	4.60	9.21	4.40	9.99	418	218	32	2	3
2	0.5	0.49	11.4	0.43	9.17	222	30	47	2	2
2	1	0.96	13.0	0.88	13.4	295	91	50	2	2
2	1.5	1.42	11.9	1.35	14.6	316	148	41	2	2
2	2	1.88	10.8	1.82	14.2	324	196	31	2	2
2	2.5	2.33	9.80	2.27	13.8	348	236	37	2	2
2	3	2.79	9.08	2.66	11.6	268	134	21	2	3
2	3.5	3.21	8.55	3.10	11.6	276	154	19	2	3
2	4	3.64	8.05	3.54	11.6	283	173	17	2	3
2	4.5	4.09	7.59	3.96	11.4	294	190	16	2	3
2	5	4.49	7.25	4.39	10.3	240	124	13	2	4
2.4	0.5	0.49	12.4	0.43	10.7	219	31	46	2	2
2.4	1	0.94	13.0	0.86	14.4	286	90	48	2	2
2.4	1.5	1.41	11.6	1.36	15.3	289	149	34	2	2
2.4	2	1.88	10.3	1.83	14.7	302	194	26	2	2
2.4	2.5	2.34	9.25	2.24	11.8	229	113	18	2	3
2.4	3	2.78	8.61	2.69	12.0	238	134	16	2	3
2.4	3.5	3.18	8.01	3.08	12.0	256	152	16	2	3
2.4	4	3.63	7.47	3.56	11.7	256	170	13	2	3
2.4	4.5	4.54	7.04	4.00	10.6	213	113	11	2	4
2.4	5	4.46	6.67	4.36	10.6	223	123	11	2	4
5	0.5	0.47	14.4	0.41	17.3	200	32	41	2	2
5	1	0.93	12.1	0.89	18.9	199	99	24	2	2
5	1.5	1.38	9.83	1.35	17.0	215	143	17	2	2
5	2	1.82	9.37	1.74	14.0	163	89	11	2	3
5	2.5	2.26	7.31	2.18	13.5	170	108	9	2	3
5	3	2.70	6.74	2.62	10.6	123	47	6	2	5
5	3.5	3.09	6.23	3.04	12.0	182	138	6	2	3
5	4	3.42	5.88	3.32	10.4	137	61	6	2	5
5	4.5	3.79	5.44	3.70	10.8	163	103	6	2	4
5	5	4.07	5.02	3.98	9.65	149	73	6	2	5

1.2 IC Design Flow Integration

Simple programming techniques may be used to interpret numerical design outputs described previously to export the SPICE[3] netlist and layout (GDS[4] format) of the designed inductor structure. The SPICE netlist of the inductor struc-

[3] SPICE stands for Simulation Program with Integrated-Circuit Emphasis.

[4] GDS stands for Graphic Database System.

ture, complete with the inductance value and parasitics calculated for the chosen inductor model, may be used in SPICE simulations to avoid drawing of the schematic of the inductor with its parasitics in the schematic editor. Layout of the inductor may be imported into layout software to eliminate the need to draw any inductor layout structures. With this in place, minimum effort is needed to deploy inductors designed using this methodology in full system design.

To demonstrate complete design flow integration, several 2.4 GHz Class-E and Class-F PAs were designed and fabricated in the IBM 7WL (180 nm) process. Another set of developed software routines was used to first perform each amplifier design. The designs required several spiral inductors for both amplifier design and the design of the matching networks. All inductors were designed using the software routine presented together with netlist and layout extraction. This allowed for the complete system to be simulated in SPICE before layouts were completed and systems were sent for prototyping.

Detailed presentation of simulation and prototyping results is beyond the scope of this chapter and the reader is referred to Božanić *et al.* (2010).

1.3 Going Beyond RF Frequencies

As frequency of operation increases beyond about 20 GHz (micro-/millimeter-wave as opposed to RF frequencies), it becomes possible to utilize transmission lines instead of passive components. Transmission line theory may be applied in order to expand the algorithms presented in this chapter for use in millimeter-wave applications (Foty *et al*. 2010, Božanić and Sinha 2011).

1.4 Conclusion

The aim of this chapter was to introduce the reader to the concept of spiral inductor design and to show how optimum inductor design can aid performance optimization of RF devices. It was pointed out that due to the indeterministic behavior of inductance and parasitics of inductors, design using simple equations should be replaced by a more streamlined methodology even for very simple inductor geometries. A methodology for synthesis-based design of planar spiral inductors, where numerous geometries are searched through in order to fit the start conditions was conceptualized, but it was concluded that it becomes too tedious to do this by hand and that software-aided design is recommended. The readers were given an example of the algorithm implemented by using a MATLAB script for the simpler, single-π, model, and provided with sufficient information to probe further. Computational intelligence could be applied to the resulting algorithm, including the IC layout, and in this way, lead to further computer-aided design and optimization. As proof of the concept, several inductors were synthesized using this methodology and their inductances and quality factors were presented and evaluated against simulation and measurement results. Finally, the reader was referred to texts where optimum inductors have aided practical RF design.

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