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INDUSTRIAL AND ENGINEERING PAPER

Ultra-compact capacitively loaded evanescent half-mode SIW filters for LTE applications

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This paper presents a novel miniaturized substrate integrated waveguide filter by combining both half-mode resonators and capacitive loading on a conventional two-layer printed circuit board (PCB) process. The resulting synthesis is successfully demonstrated in an long-term evolution application by means of a third-order filter of <225 mm² in size while featuring 2.3 dB insertion loss over a 5.5% fractional bandwidth at 3.7 GHz. Good first-iteration agreement between simulated and measured results, both in center frequency and bandwidth, are achieved.

Keywords: Applications and standards (Mobile, Wireless, networks), Filters

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I. INTRODUCTION

With the large-scale commercial adoption of the long-term evolution (LTE) and IEEE 802.11y standards, there is a renewed drive to find compact, low-loss, and low-cost implementations of S- and C-band microwave filters on conventional soft substrates. Substrate integrated waveguide (SIW) [1] filters have the advantage of high resonator *Q*-factor whilst requiring only a conventional two-layer RF PCB process to manufacture. The technology does, however, occupy more board space than equivalent planar resonators [2] or off-board manufactured filters such as low-temperature co-fired ceramics (LTCC) [3]. Apart from using multiple metalized layer geometries [4] or alternative cavity geometries [5], SIW resonators have been miniaturized successfully by loading of the SIW cavities to create evanescent mode cavity (EMC) resonators (the operating theory of which is described in [6]). This loading has been accomplished with dielectric posts [7], defected ground structures [8], complementary split-ring resonators (CSRRs) [9], and capacitive posts [10]. This capacitive loading may be increased to the point where the area of the capacitive plate, and not the surrounding fencing, defines the resonator, as was shown with the TEM-SIW cavity [11]. Another way of decreasing the width of SIW resonators is using half-mode guide (HMSIW) [12] which, unlike folded SIW [4], does not require multiple metalized layers. HMSIW has been successfully combined with CSRR [13], external capacitive loading [14] (to create a second transmission band), and fractal pattern miniaturization [15], but not with internal capacitively loaded resonators.

This paper presents a novel combination of the miniaturization properties of both HMSIW and capacitively loaded EMC resonators (similar to TEM-SIW resonators). The filter size is reduced further by removing the via fences still used in [10, 11] that demarcate separate cavities, relying solely on the capacitive load plate to define the resonator area.

II. GEOMETRY

The structure of the capacitively loaded HMSIW is shown in Fig. 1. The first resonator is formed in a substrate of height h by a capacitive plate of width w_c and length l_{c1}, and is connected to ground by a post of diameter d_p. The plate is separated from the edge of the SIW cavity (defined by a via fence of

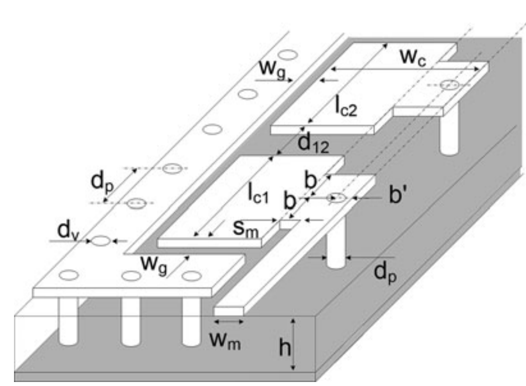

Fig. 1. Two cascaded resonators, with microstrip coupling to the first.

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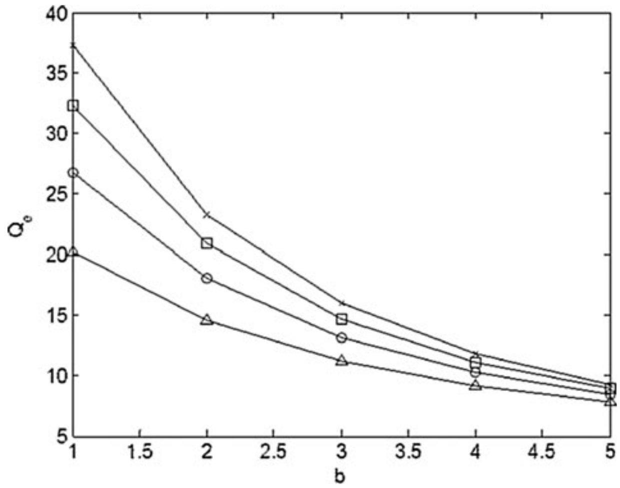

Fig. 2. *External Q-factor variation versus* b. $-\Delta-$: $s_m = 0.5$; $-\bigcirc-$: $s_m = 1$; $-\square-$: $s_m = 1.5$; $-\mathrm{X}-$: $s_m = 2$.

diameter d_v and pitch d_p) by a gap w_g. The resonator is tapped-fed externally by a 50 Ω microstrip line of width w_m, with the feed defined by a slot of width s_m terminating a distance b from the post. The capacitive plate is connected to the center post by a septum of width $2b$, with the post a distance b' from the edge of the metallization. The second resonator is formed by a plate of length l_{c2} and width w_c, which couples to the first across the gap d_{12}. It is important to note the absence of via fencing between the resonators, further reducing the length of the final filter. Major changes to the external Q-factor of the resonator is achieved by varying the septum width $2b$ (Fig. 2), while minor alterations may be accomplished by varying the slot width s_m. Coupling k between resonators is electric, with the distance separating them (d_{mn}) controlling capacitive coupling. Coupling values of $k = 0.01 \rightarrow 0.09$ are possible (Fig. 3).

III. SYNTHESIS AND SIMULATION

A third-order filter is synthesized with a passband to cover LTE channel 43 from 3.6 to 3.8 GHz, with −15 dB pass-band input reflection. This filter requires external resonator loading of

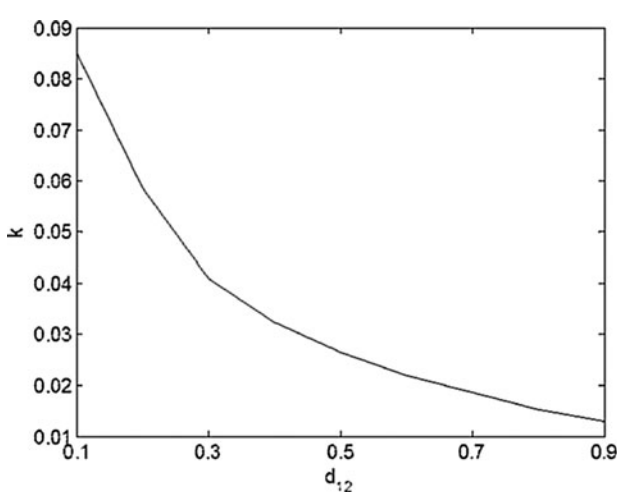

Fig. 3. Coupling k versus d_{mn}.

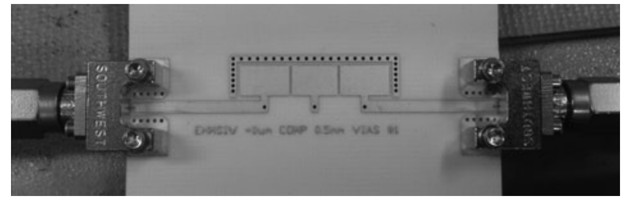

Fig. 4. Photographed filter under test.

$Q_e = 20.7$ and internal coupling of $k_{12} = k_{23} = 0.0476$. Both parameters are related to geometric dimensions through the use of full-wave eigenmode solvers provided in CST Microwave Studio. The external Q-factor is determined by varying s_m and b (with variation in l_{c1} to ensure resonance at $f_0 = 3.7$ GHz), and calculating the external Q-factor at the port of excitation. The even-mode and odd-mode eigenmode resonances f_e and f_o are used to calculate k in a simulation, with d_{12}varied to achieve the required value. After assembly and simulation of a full finite element method (FEM) model in CST, the filter is tuned to final dimensions in mm, as referenced to Fig. 1, of $w_m = 1.67$, $w_g = 0.50$, $w_s = 1.00$, $w_c = 7.00$, $b = 0.53$, $b' = 0.84$, $d_v = 0.50$, $d_p = 1.00$, $d_{12} = d_{23} = 0.32$, $l_{c1} = l_{c3} = 7.40$, $l_{c2} = 6.90$, and $s_m = 0.75$.

IV. MANUFACTURING AND MEASURED RESULTS

The prototypes were manufactured on Rogers RO4003C of thickness 0.813 mm, using 1 oz. copper deposition, as shown in Fig. 4. The artwork exported from CST Microwave Studio was compensated for +9 μm over-etch on the copper tracks and +50 μm over-drill on the vias. These changes resulted in a manufactured filter with negligible center frequency offset from the simulated result (Fig. 5). The additional 1.1 dB insertion loss is attributed to lower than expected resonator Q-factor, an assumption substantiated by the rounded filter response at the upper and lower cut-off frequencies. The lower Q-factor is attributed to the electroless nickel immersion gold surface finish, which is known to

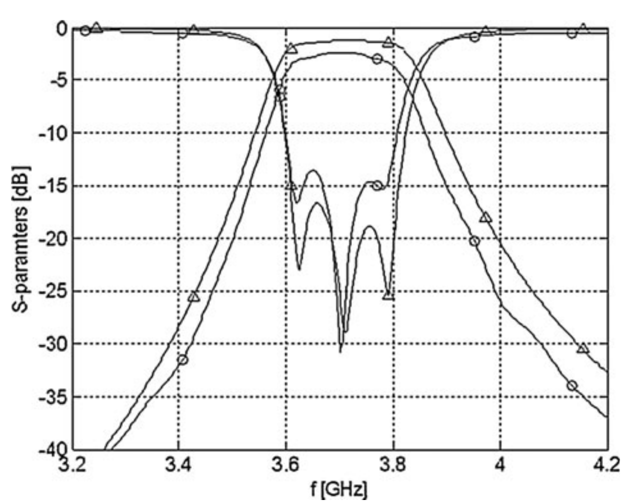

Fig. 5. Simulated $-\Delta-$ and measured $-\bigcirc-$ filter responses.

Table 1. Comparison of this work to the state-of-the-art in uni-planar LTE filters.

	ε_r	Size (mm^2)	f_o (GHz)	FBW (%)	Loss (dB)	Order
This work	3.55	225	3.7	5.5	2.3	3
[17]	3	528	3.5	6	1.45	4
[18]	2.55	203	3.1	10	2.8	3
[19]	3	255	3.45	8.7	1.7	3
[20]	2.65	1697	3.3	14.3	1.8	3

cause larger than anticipated insertion loss in planar filters [16].

This work is compared in Table 1 to the state-of-the-art in compact LTE filters on conventional RF substrates. For comparable filter order, fractional bandwidth (FBW), and frequency, the filter occupies less board space than state-of-the-art solutions at the expense of higher insertion loss.

V. CONCLUSION

A miniaturized SIW filter, suitable for LTE and IEEE 802.11y applications, has been presented. The filter measures 225 mm^2 and features 2.3 dB insertion loss across a 5.5% FBW for upper LTE channel frequencies. Good first-iteration agreement between simulated and measured results is obtained, both in center frequency and bandwidth.

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