# ELECTROMAGNETIC INTERFERENCE IN BALANCED CONVERTERS

**By**

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**2014**

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# ABSTRACT

In this dissertation, an investigation into reducing Electromagnetic Interference (EMI) through design is presented. Root generation mechanisms of Electromagnetic Interference are often neglected during the design process and later treated symptomatically. Mitigation of Electromagnetic Interference at source often reduces cost and physical size of electronics. This dissertation demonstrates the process and results by which schematic balance mitigates EMI. In addition, the introduction of Geometric Balance and physically designing circuits to be Geometrically Symmetrical are presented and tested to determine whether the design produces mitigating EMI results. Multiple Printed Circuit Boards (PCB's) were developed and tested against each other to demonstrate schematic balance and other EMI generation mechanisms. The final PCB was designed to be Geometrically Symmetrical and the test results compared. The results illustrate the varying performance of each PCB due to their differing design. The Geometrically Symmetrical PCB presented the best results due to various improvements which include physical layout size and semiconductor placement. An additional important phenomenon discovered was the amount of EMI generated during MOSFET Driver operation. This contributed to a significant amount of EMI during the no-load phase of testing.

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# LIST OF ACRONYMS

AC – Alternating Current

CM – Common Mode

DC – Direct Current

DM – Differential Mode

DUT – Device Under Test

EMC – Electromagnetic Compatibility

EMI – Electromagnetic Interference

EUT – Equipment Under Test

LISN – Line Impedance Stabilisation Network

NF – Noise Floor

PCB – Printed Circuit Board

PWM – Pulse Width Modulation

RF – Radio Frequency

SMPS – Switched Mode Power Supply

TCL – Transverse Conversion Loss

# 1 INTRODUCTION AND PROBLEM STATEMENT

## 1.1 INTRODUCTION

The increasing drive for energy efficiency in today's world brings about new challenges and obstacles especially within the domain of Industrial Electronics. These increasing demands for increased efficiency, reduced size (through increased frequency operation) and the lower cost of devices brings about the need to focus on new or previously unimportant phenomenon as they become ever more dominant. One such phenomenon in the Industrial Electronics field is the phenomenon of Electromagnetic Interference (EMI).

The need to advance is fundamental to human progress and hence the ever increasing efforts within the Industrial Electronics fraternity. With reference to the general timeline of Electrical Engineering and electricity, Electronics and specifically Industrial Electronics is a relatively new arena [1] [2] [3]. The relative infancy of Industrial Electronics and now the ever increasing improvements within the field exposes the previous lack of study of the EMI phenomenon. One such reason for the previous lack of concern with EMI is the state of the art of electronics (i.e. operating frequencies and size of devices). Operating modes of electronics never produced appreciable amounts of EMI or the ability to measure EMI was not evident at such a time.

Electromagnetic Interference is the phenomenon by which the operation of a device or system emits Electromagnetic Radiation via a cacophony of methods. The emitted radiation through propagation can then result in an undesirable operating effect on other operational equipment so as to cause the equipment to fail or malfunction. The equipment which falls victim to such interference is not only limited to other equipment but may include the generating equipment itself (the source).

EMI has generally been considered a difficult phenomenon to understand within the Engineering community and has often been labelled as a "*Black Art*" due to the complexities and unknown or abstract generation mechanism of EMI.

As the generation mechanisms of EMI are generally not well understood, operational devices are not normally designed with EMI in mind [2] [3] [4]. During development of electronic devices, a device is designed and developed until functional against preliminary design specifications. Once operating within the design specifications, the device is then sent to EMI testing. Based on the EMI results, an appropriately large EMI filter is then fitted to the front and back of the device to fall with EMI standards. These filters then add both cost, physical size and weight to the device. If the device were to be designed and developed with the generation mechanisms of EMI in mind, the EMI issues would be solved on a root level and hence automatically reduce cost and the required filter size for the device.

Due to the difficulty of understanding the sometimes abstract generation mechanisms or more often than not the lack of knowledge in understanding EMI, devices are not normally designed with EMI in mind. Therefore the knowledge of EMI from the beginning of the design process will substantially aid in the reduction of EMI from root causes and

automatically improve EMI results, a direct treatment of the issues on a root level and not just on a symptom level.

Gaining insight into the root generation mechanisms of EMI and discovering appropriate methods of reducing EMI through design, forms the foundation of the dissertation presented within.

## 1.2 SCOPE

The scope of this dissertation pertains to the design and development of multiple Printed Circuit Boards (PCB's) to investigate methods used to firstly demonstrate EMI and secondly to mitigate Electromagnetic Interference on a root level. Varying parameters shall be applied to observe the effects of these altered parameters on EMI generation mechanisms.

## 1.3 DOCUMENT OVERVIEW

Chapter 2:

- Defining Electromagnetic Interference
- Differentiating EMI Propagation Methods into subsequent modes
- Defining Conducted EMI
- Components of Conducted EMI and Generation mechanisms
- Measurement Methods and EMI
- Separation of Conducted EMI components into DM and CM

Chapter 3:

- Introduction of the Balanced Converter topology
- Unbalanced Converter theory and EMI generation mechanisms
- Conversion of an Unbalanced Converter to a Balanced Converter
- Balanced Converter Examples
- Investigation in Geometrically Balanced Converter
- Proposed Geometrically Balanced Converter

Chapter 4:

- Test Circuits design criteria
- Required circuit
- Dividing circuit into sub-circuits
- MOSFET Driver Circuit Design
- Varying PCB's Design
- Physical Implementation of Designed Circuits

Chapter 5:

- Equipment Required and Setup
- Experimental Setup

Chapter 6:

- Individual PCB results
- Comparative results
- Analysis of results

Chapter 7:

- Conclusion
- Future work

## 1.4 EXPERIMENTAL OVERVIEW

A brief outline of the Experimental setup is outlined below:

1. No load DM results: Non-Elevated and Elevated case
2. Loaded DM results: Non-Elevated and Elevated case
3. No load CM results: Non-Elevated and Elevated case
4. Loaded CM results: Non-Elevated and Elevated case

# 2 ELECTROMAGNETIC INTERFERENCE (EMI)

## 2.1 INTRODUCTION

Electromagnetic Interference (EMI) can be described as the undesirable effect due to an electromagnetic emission or disturbance from a source due to its operation regardless whether intentional or not upon another piece of operating equipment. The emissions may produce an undesirable or unwanted operating effect on the affected piece of equipment. Such effects in turn may cause the affected equipment to malfunction or cease to function entirely. The victim is not limited to other operational devices but may include the source itself.

Multiple categories of EMI exist based upon the method of propagation, which are discussed in Section 2.2.

## 2.2 ELECTROMAGNETIC INTERFERENCE CATEGORIES

Due to the multiple coupling methods of EMI (inductive, capacitive, conductive, radiated) [5], multiple standards have been developed to help classify the type of EMI experienced. These standards mainly dictate frequency ranges and noise thresholds.

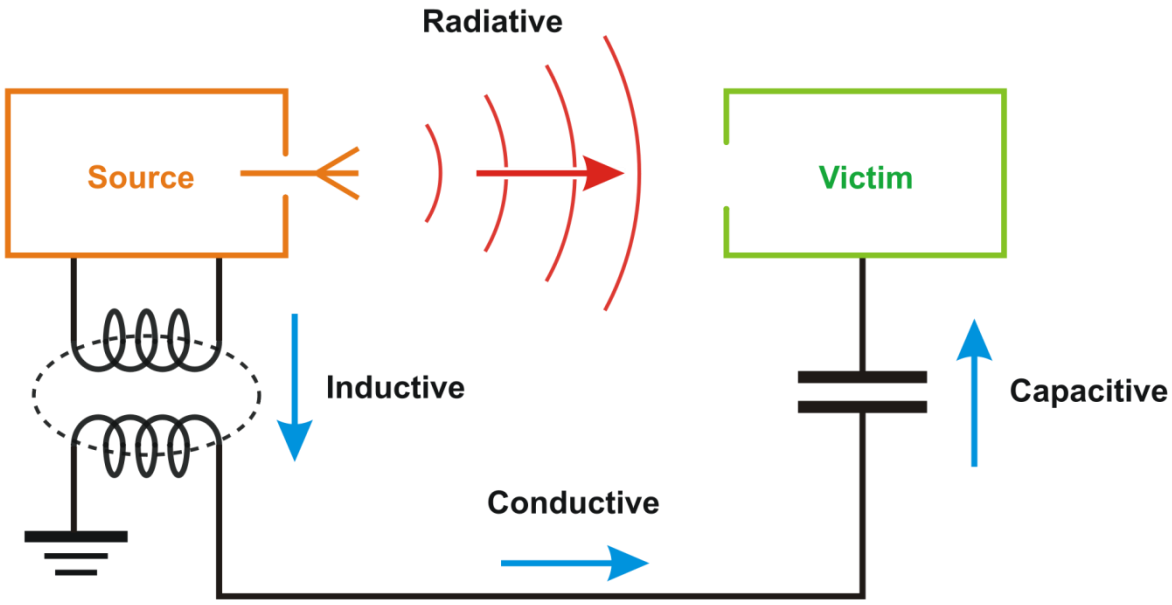



**Figure 2-1 Propagation Methods [6]**

### *2.2.1 Radiated EMI*

Referring to Figure 2-1, Radiated EMI is propagated through free space in the form of electromagnetic waves similar to radio waves. Any equipment in the path or vicinity of the radiated energy may be susceptible to interference from the radiated energy.

The official Radiated EMI frequency spectrum begins at 30 MHz and continues up to 10 GHz. At frequencies above 30 MHz circuit wire/track length becomes considerately small enough as to behave as an antenna and hence radiate energy, thus 30 MHz being the beginning of the Radiated EMI Standard.

### *2.2.2 Conducted EMI*

Referring to Figure 2-1, Conducted EMI is propagated through inductive, capacitive and conductive means. Conducted EMI therefore propagates through a physical means such as conductors being wire or traces from the source to the victim, including capacitive and inductively through a path such as ground between the source and victim.

Conducted EMI not only affects the source supply or other equipment directly connected, but can propagate through the power system upon which it's connected to, and affect other sensitive equipment.

Conducted EMI will be the category of focus within this dissertation, upon which the further subcategories within Conducted EMI will be discussed in section 2.3.

## 2.3 CONDUCTED EMI

The details pertaining to Conducted EMI, its standards and modes are discussed in section 2.3.

### *2.3.1 Scope (Specifications 150 kHz-30MHz) of Conducted EMI*

The conducted EMI spectrum is regulated from 150 kHz to 30 MHz [4].

Frequency measurements will be done from 100 kHz to 60 MHz as to ensure measurements are within the conducted EMI standards spectrum. Both modes of EMI will be measured and compared relative to a control circuit in order to determine efficacy. Frequency measurements are conducted from 100 kHz due to measurement equipment abilities.

Conducted EMI is broken down into two categories or modes being:

- Differential Mode (DM) EMI
- Common Mode (CM) EMI

These modes are subsequently discussed in detail respectively in Sections 2.3.2 and 2.3.3.

### *2.3.2 Differential Mode (DM) EMI*

Differential Mode (DM) EMI as its name implies is the component of the Conducted EMI spectrum in which the EMI currents flow in a differential manner (opposite in direction to each other) between the source and the victim, typically through planned conductors as illustrated in Figure 2-2. By definition they are equal in magnitude but opposite in direction and the return path is in absence of the use of "ground" [4].

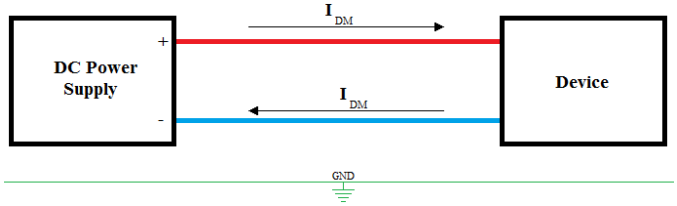



**Figure 2-2 Differential Mode (DM) EMI Conduction Path [4]**

#### *2.3.2.1 Theory of DM*

Differential Mode (DM) EMI is a function of the Differential Mode Current within the conductors of an operating circuit [1] [2] [4]. DM current is due to the fundamental operation of the source equipment which in many cases is a switch-mode converter [1] [2] [4], the switching function of which draws a non-DC current component regardless whether the source (and also the victim) is pure DC. There are thus frequency components within the DM current and thus DM EMI is present.

#### *2.3.2.2 Generation Mechanisms of DM*

The operational current drawn from the source by the switch-mode converter is not DC in which case differential alternating current is drawn and hence DM EMI is generated.

The generation mechanisms of DM EMI are, but not limited to:

- Switching - Creation of frequency content (AC)
- Inductance – Stray and leakage
- Absence of bus capacitance

The physical switching of a perfect source converter in theory would have perfect rise and fall times where $t_r$ and $t_f$ are infinitely small. The resultant current within the system produces a frequency spectrum with a fundamental switching frequency and related harmonics with a decreasing magnitude. The resulting spectrum is due to a perfect square wave being an infinite sum of sinusoids with decreasing amplitude according to Fourier Transform Theory [7]. The frequency content which results due to the switching action of a switch-mode converter therefore constitutes to DM EMI. It can be noted that a decrease or increase in $t_r$ and $t_f$ will change the outline of the frequency spectrum and hence influence the magnitude of the DM EMI [4].

Inductance and capacitance also have a secondary effect on DM EMI. Parasitics have the ability to form resonant circuits within a system or converter. The ringing constitutes to the generation of higher or additional frequency components which in turn generates additional DM EMI. Inductance and capacitance can also aid in coupling, thus spreading the generated EMI.

Sources of parasitic inductance can be physical layout inductance (self inductance) and leakage inductance caused by magnetic components (i.e. transformers) [4]. Parasitic capacitance can be in the form of inter-winding capacitance in magnetic sources (i.e. transformers) [4] and the capacitance's found within switching components such as semiconductor devices [4].

### *2.3.3 Common Mode (CM) EMI*

In contrast to DM EMI, where the EMI is conducted in a loop between the supply positive and negative rail (or live and neutral in AC systems) as in conventional current, CM EMI current is conducted down the positive and negative rails in the same direction with equal

magnitude normally with a capacitive return path to the supply through physical ground. Figure 2-3 illustrates the basic process of the CM EMI conduction path.

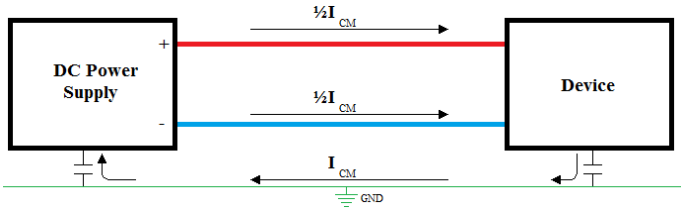



**Figure 2-3 Common Mode (CM) EMI Conduction Path [4]**

### *2.3.3.1 Theory of CM*

By definition CM EMI is the conducted component of EMI whereby the current flows from the source to the victim normally through a capacitive means to a plane normally called "ground" [4]. In most cases the ground reference is the Earth wire in a power supply system which is usually connected to the chassis of the supply and converter.

Parasitic components within a converter or circuit are the predominant cause of CM EMI in conjunction with high frequency DM Noise. The parasitic components provide a short circuit path to ground for the already present high frequency DM components and thus are allowed to travel through a ground plane. These parasitic components are often not considered or even aware of during circuit analysis.

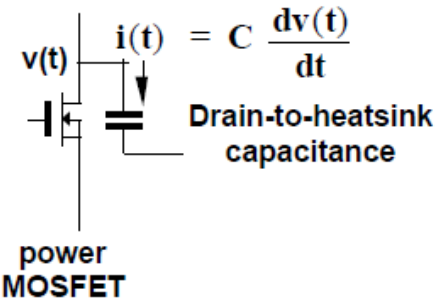



**Figure 2-4 MOSFET Parasitic Capacitance [8]**

Figure 2-4 illustrates the Drain to heat-sink capacitance normally found within an active switch such as a typical MOSFET and illustrates the current path used to sink current to ground as the heat-sink in a converter is usually connected to ground for safety reasons. The contact area of such a device is required to be large for cooling purposes, which in turn increases parasitic capacitance (parallel-plate area).

### *2.3.3.2 Generation of CM*

Generally, CM EMI cannot be present without the presence of DM currents or DM EMI [1] [2]. As no circuit or converter is ideal, parasitics exist. Figure 2-5 illustrates a simple boost converter with only a single parasitic present, the drain to heat-sink capacitance ($C_s$).

During normal operation of the circuit in Figure 2-5, the active switch *Q* will switch with a specific frequency *f*, which will draw a current through inductor *L*. As inductor *L* is not perfect and is a complex impedance and has a resistive component at frequency, a voltage drop will appear across inductor *L* and in turn will present an AC voltage at the node where the drain of the MOSFET is connected to the diode and $C_S$.

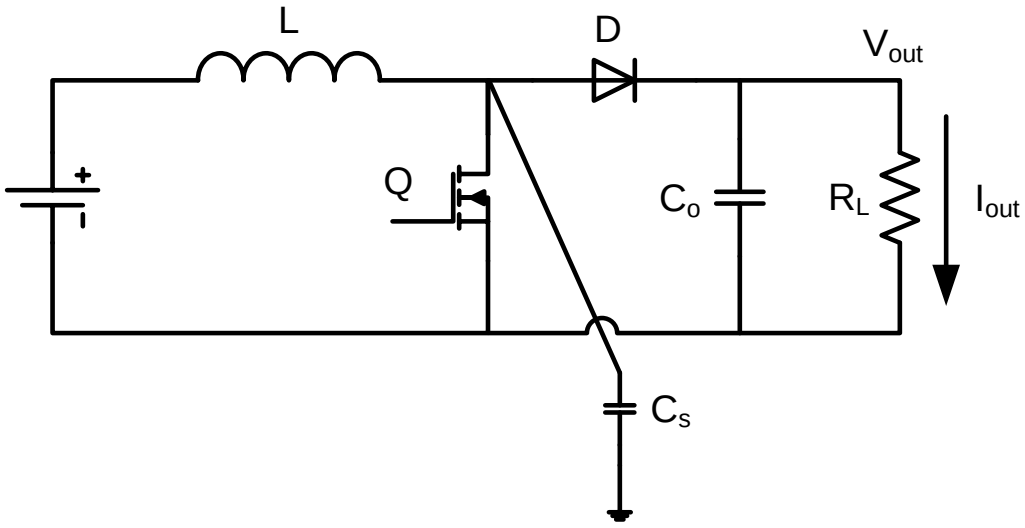



**Figure 2-5 Boost Converter illustrating parasitic $C_S$ [9]**

A high frequency voltage present across $C_S$ will conduct current to ground hence causing current to flow from the source to the victim or supply ground. CM EMI is thus generated through the abovementioned mechanism.

CM EMI is not only limited to being generated from a single capacitive component. Figure 2-6 illustrates the other parasitics present in a boost converter, which all influence CM EMI to some extent.

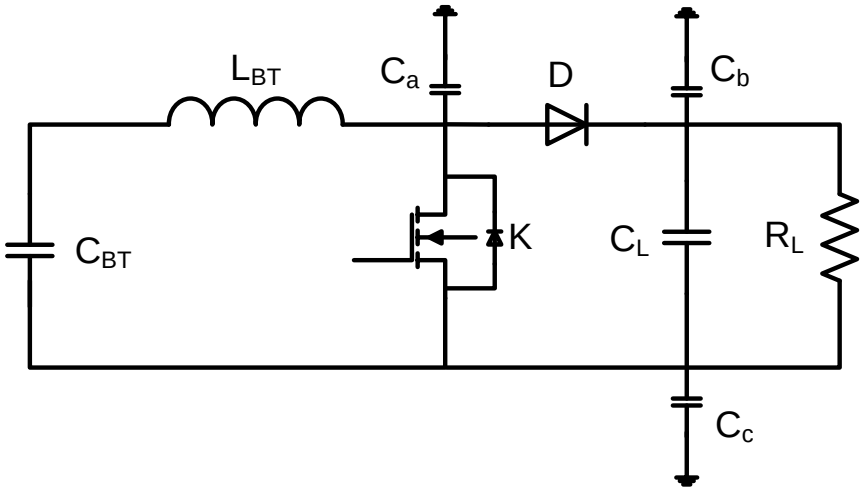



**Figure 2-6 Boost Converter with associated parasitic components [9]**

### *2.3.4 Relationship Between Common Mode (CM) and Differential Mode (DM) EMI*

According to [1] [2], a relationship exists between CM and DM EMI. [2] Further states CM EMI is a proportional function of the DM EMI and therefore a direct theoretical correlation exists.

#### *2.3.4.1 DM to CM conversion*

According to [1], using the Transverse Conversion Loss (TCL) theory, there is a predictable relationship between DM and CM.

The TCL definition in [1] simplifies the TCL into the following equation:

$$U_{TCL} = K_{TCL} \cdot U_1 \quad \text{.....(1)}$$

Where $U_1$ represents a DM quantity and $U_{TCL}$ represents a CM quantity. Equation (1) implies the CM EMI can be modelled as a proportional function of the DM EMI.

If there is either an increase or a decrease in the DM EMI (in magnitude or frequency), the CM EMI will either increase or decrease proportionally (in magnitude or frequency) as a result of the proportional relationship.

A second source of conversion illustrated in [1] is the conversion of a DM signal into CM current and hence CM EMI through DM unbalance.

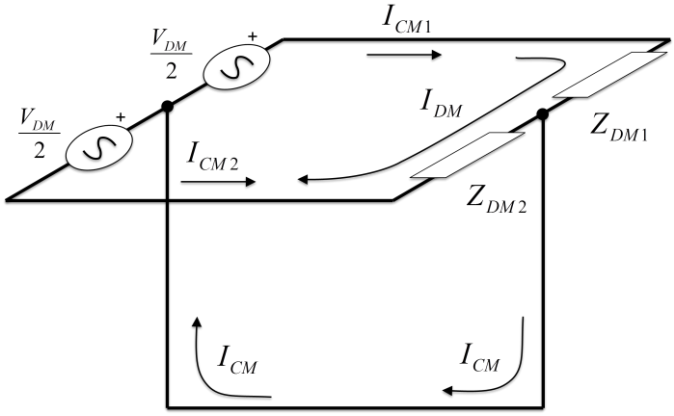



**Figure 2-7 CM EMI generation through DM Unbalance [2]**

In Figure 2-7 $I_{CM}$ would be zero only when $Z_{DM1}=Z_{DM2}$, however this seldom occurs even in special cases.

When there is an imbalance between $Z_{DM1}$ *and* $Z_{DM2}$ (they are not equal), a voltage divider is present in Figure 2-7 and $I_{CM} \neq 0$ thus creating CM currents and hence CM EMI.

An additional example of DM to CM conversion can be found in Figure 2-8.

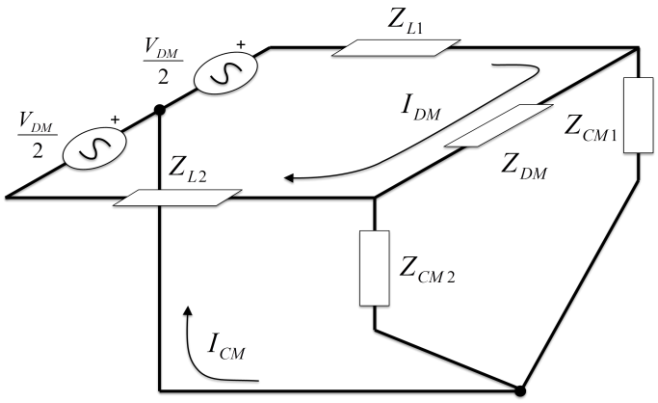



**Figure 2-8 CM generation through imbalance in the CM and DM impedances [2]**

An extensive explanation regarding the DM to CM conversion process is documented within [2] for Figure 2-8 which discusses the various mechanisms by which DM to CM conversion takes place, including the possibility of CM generation mechanisms through CM components solely. In essence an imbalance between either $Z_{L1}$ *and* $Z_{L2}$ or $Z_{CM1}$ and $Z_{CM2}$ results in the generation of CM currents which is generally the case within real-world circuits due to circuits being imperfect.

## 2.4 MEASURING EMI

Measurement theory, techniques and the associated equipment are discussed here within Section 2.4.

### *2.4.1 Theory*

When a converter operates, by the means discussed in previous sections, EMI is generated by the converter. Power drawn from the source as either DC or low frequency AC (50-60Hz) is converted normally through switching within the converter to a different level as required by the application, often where a DC output is required.

However, regardless of whether the input or output is DC, the high frequency activity of the converter presents high frequency components (harmonics, voltage and current components) to both the load and power source as illustrated in Figure 2-9.

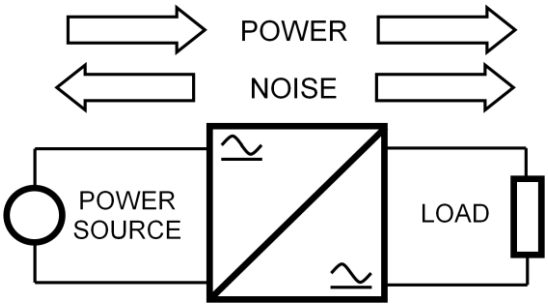



**Figure 2-9 Power and noise propagation directions [2]**

In order for the generated noise to propagate, by definition as either a current source or voltage source [2], an impedance (and current path) for the noise needs to be present in order for the noise currents to flow into. The noise load is discussed further in section 2.4.1.1.

### *2.4.1.1 Noise Source and Load Impedances*

The Noise Load is defined as the impedance seen by the noise source when looking into either the *Load* or *Supply*. Similarly the noise source is the noise (EMI) generated by the converter through operation. The *Supply* and *Load* provide an impedance for the noise to enter into.

To illustrate the propagation of EMI emanating from the converter, a convention is presented such that the converter is the noise source, from where the noise propagates from to both the supply and load impedances as illustrated in Figure 2-10 and Figure 2-11.

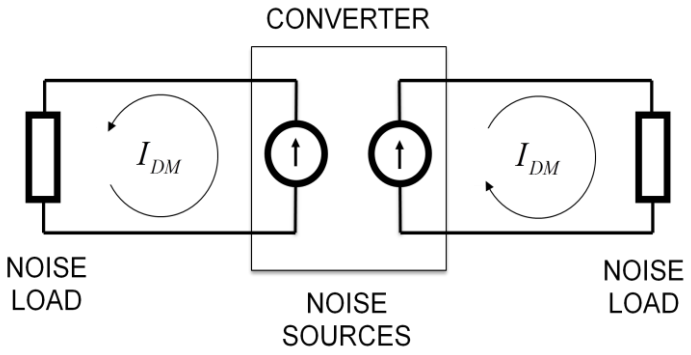



**Figure 2-10 Differential Mode (DM) Currents Flowing into Noise Loads [2]**

In Figure 2-10, conventional DM noise currents flow from the noise source (converter) to the noise load (*Supply, Load*) through conventional means. The DM noise propagates through the physical conductors from the source towards the load as for conventional current, through known and easily identifiable paths.

As can be seen in Figure 2-10 and Figure 2-2, DM current flow within a cable or circuit path is equal but opposite in direction.

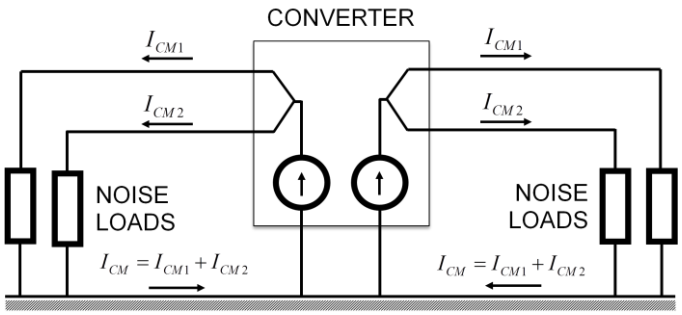



**Figure 2-11 Common Mode (CM) Currents Flowing into Noise Loads [2]**

CM noise in contrast to DM noise does not flow like conventional current convention but rather through other coupling mechanisms. The noise source and loads are similar to DM source and loads but not identical.

Figure 2-11 and Figure 2-3 illustrate that CM currents flow in the same direction along both conductors, to return via ground. The ground is connected via capacitive coupling effects whereby high frequency harmonics of the converter will couple to a heat-sink, ground-plane, ground-wire and etc to obtain a return path back to the converter. The capacitive coupling methods are mainly due to parasitic components.

### *2.4.1.2 CM and DM separation*

Mentioned earlier, DM and CM EMI Sources and Loads have been discussed and their relevant propagation methods have been discussed.

From Figure 2-2 and Figure 2-3 we can derive Figure 2-12 as the result of summing both DM and CM to produce the total Conducted EMI presented to the noise load.

Figure 2-12 also illustrates when measuring EMI, CM and DM EMI are present together within the measurement. In order to measure DM and CM individually, DM and CM EMI need to be separated by an appropriate measurement technique in order to evaluate each individually.

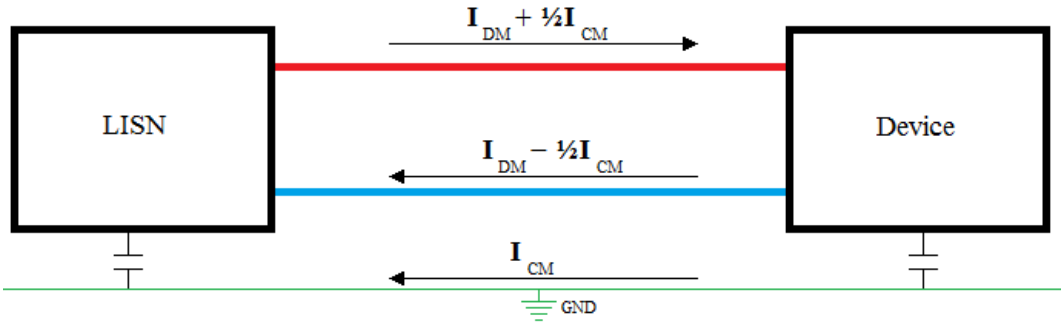



**Figure 2-12 DM and CM as Conducted EMI [4]**

In order to separate CM and DM the following equations can be formed based on Figure 2-12 and Figure 2-13. The voltages with reference to ground can be derived in terms of the DM and CM currents:

$$V_{LE}=50*(I_{DM}+\frac{1}{2}I_{CM})$$

Similarly

$$V_{NE}=50*(\frac{1}{2}I_{CM}\text{-}I_{DM})$$

Letting $V_{DM}=50\times I_{DM}$ and $V_{CM}=25\times I_{CM}$ and substituting:

$$V_{LE}+V_{NE}=2\times V_{CM}$$

$$V_{LE}\text{-}V_{NE}=2\times V_{DM}$$

Hence the Differential Mode (DM) voltage

$$V_{DM}=\frac{V_{LE}\text{-}V_{NE}}{2}$$

And the Common Mode (CM) voltage:

$$V_{CM}=\frac{V_{LE}+V_{NE}}{2}$$

Multiple methods are outlined in [4], [10] and [11] in order to separate DM and CM in order to measure them individually.

### *2.4.2 Measurement Equipment*

The following section outlines and describes the equipment and terminology relevant in the use of EMI measurements.

#### *2.4.2.1 LISN*

A Line Impedance Stabilisation Network (LISN) is a piece of measuring equipment used in EMI measurements to provide a standardised noise source impedance as illustrated in Figure 2-13.

A LISN is comprised of inductors, capacitors and resistors to form a multi-line low pass filter network [4] which provides a stabilised line impedance of 50Ω in order to measure conducted EMI.

In addition to providing a stabilised impedance, a LISN isolates the Equipment Under Test (EUT) from the source supply and vice versa, inhibiting noise emanating from the EUT to penetrate the supply network and to inhibit noise from the supply network entering the measurement setup.

For the purpose of this dissertation, an EMCO 3825/2 LISN was made available. According to [4] and [12] the LISN has a network inductance, impedance of 50 µH/250 µH, 50 Ω. The guaranteed frequency range at which the 50 Ω impedance is presented to the EUT is 10 kHz to 100 MHz for the EMCO 3825/2. Figure 2-13 below illustrates the circuit diagram of the available LISN and the location of the mentioned components.

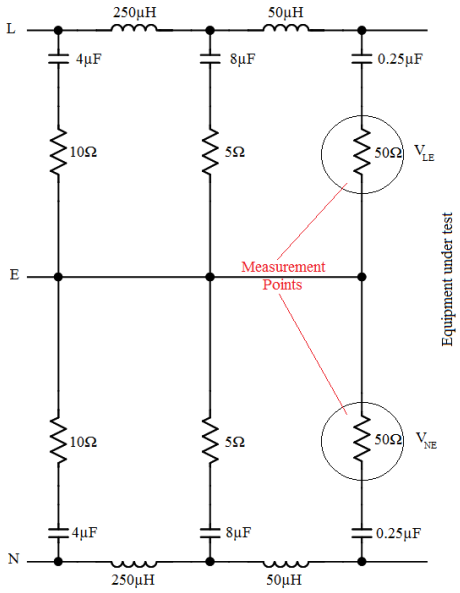



**Figure 2-13 EMCO 3825/2 Circuit Diagram [4] [12]**

The 50 Ω measurement points as indicated in Figure 2-13 are used to measure the total conducted EMI from the EUT. Using the combination of both measurement points, CM and DM EMI can be separated as per discussion in Section 2.4.1.2.

A LISN will usually provide an Earth point by which a ground-plane can be connected directly to the LISN, facilitating in a good coupling plane for CM EMI and a known return path for the measurement of CM EMI.

### *2.4.2.2 Spectrum Analyser*

A spectrum analyser is a specialised piece of measuring equipment, as the name suggests capable of measuring the frequency spectrum of a signal or input. A spectrum analyser measures the power or magnitude of an electrical input signal and plots it with reference to the frequency at which the individual frequency intensities are measured.

A spectrum analyser differs from an oscilloscope as it presents its results in the frequency domain and a major difference being its bandwidth and minimum measurement threshold.

An oscilloscopes minimum measurement threshold is typically in mV whereas a spectrum analyser is capable of measuring in the µV range. Conducted EMI values are typically in the µV range and hence the use of a spectrum analyser as a necessity.

For the purpose of the dissertation, a Rohde & Schwarz FSH3 spectrum analyser was available. The FSH3 has a frequency spectrum range of 100 kHz to 3 GHz and hence is adequate for measuring EMI in the Conducted EMI spectrum.

#### *2.4.2.3 Measurement Units*

Due to the extremely low measurement values, typically in the µV or µA range, Conducted EMI measurements are measured in a logarithmic scale represented as either dBµV or dBµA whether a voltage or current is measured.

Measuring in the dBµV range allows very small values to be easily interpreted and related against larger values that would seemingly be un-relatable. Another advantage in measuring with a dB scale in EMI is the ease in which it relates when applying EMI filters to a device as filters often give dB/decade roll-off values.

The *dBµV* scale is a relative voltage measurement value. It is relative to 1 µV, thus 0 dBµV = 1 µV (whereas 60 dBµV = 0 dBmV). [13]

### *2.4.3 Terminology*

The following section covers terminology commonly found in Conducted EMI Theory which has not been previously covered.

#### *2.4.3.1 Ground*

Ground, sometimes referred to as "Earth" is a return path for the CM portion of the Conducted EMI spectrum [14].

The ground is usually comprised of a conductive material normally within the vicinity of the EUT. Examples of which are heat sinks and equipment enclosures.

Ground is usually connected to the Earth wire within an electrical supply system for safety reasons and hence usually forms part of the noise source return path for an Earth-Leakage system.

### *2.4.4 Standards*

The Federal Communications Commission (FCC) of the USA and the Comité International Spécial des Perturbations Radioélectriques (CISPR - English: Special international committee on radio interference) provide many standards relating to EMI. These standards include measuring equipment, techniques and emission standards to mention a few.

Examples of the major standards relevant to the dissertation but not limited to are:

- CISPR 16-1
- CISPR 16-2
- FCC Part 15 Subpart A
- FCC Part 15 Subpart B

Figure 2-14 and Figure 2-15 below illustrate the FCC Part 15 A & B Conducted Noise Emission Limits. These emission limits illustrate the allowable spectrum for products that wish to go on sale to the public. These levels serve as a useful reference when comparing measured results within this dissertation.

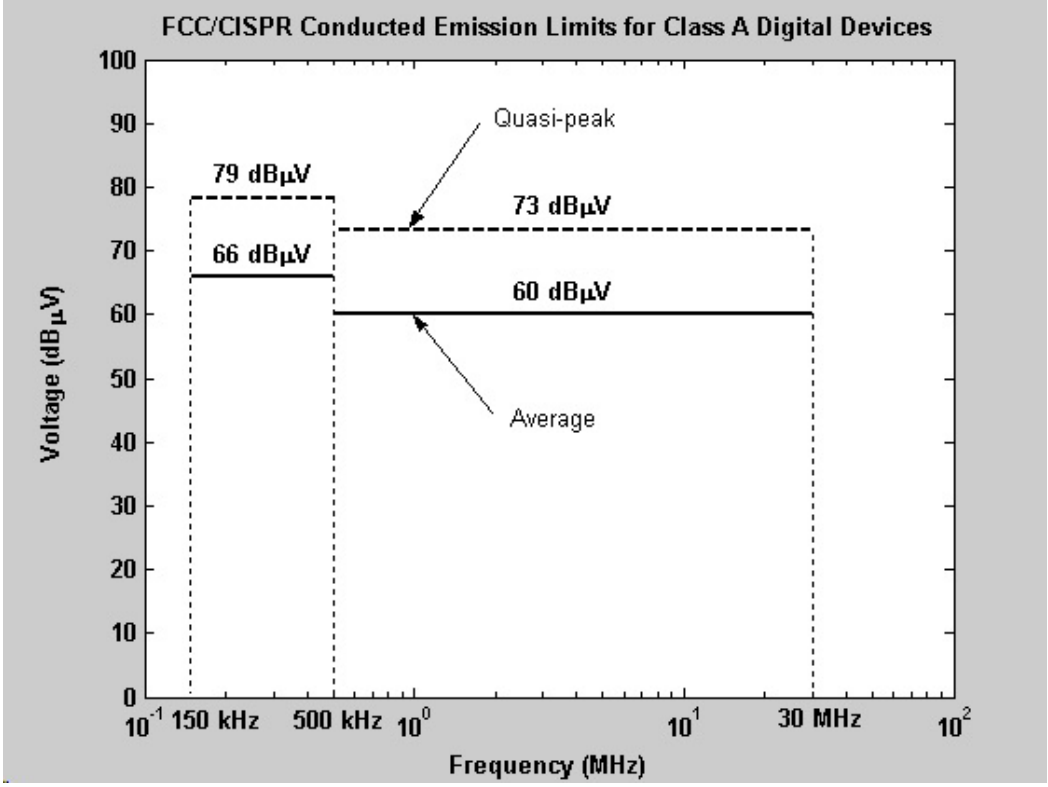



**Figure 2-14 FCC Part 15 Subpart A [15]**

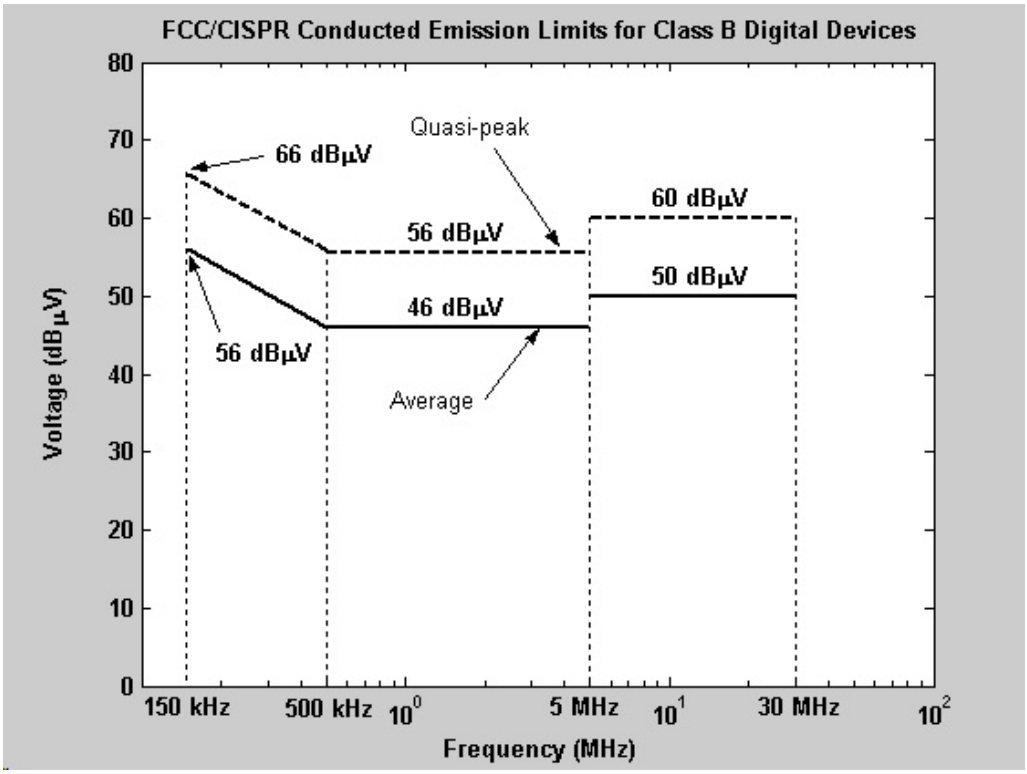



**Figure 2-15 FCC Part 15 Subpart B [15]**

## 2.5 CONCLUSION

Electromagnetic Interference and mechanisms by which EMI is generated have been introduced and discussed. The categories of EMI have been highlighted and the pertinent major category of Conducted EMI has been discussed. The two conduction modes (Differential-Mode and Common-Mode) within the Conducted EMI spectrum have been discussed and the mechanisms behind their generation highlighted. The measurement techniques of Conducted EMI have been presented including some of the essential measurement equipment required to perform the measurements. The relevant standards and terminology pertaining to measuring Conducted EMI have also been discussed. Methods pertaining to the mitigation of EMI through good design practices are subsequently presented in Chapter 3.

# 3 BALANCED CONVERTERS AND ELECTROMAGNETIC INTERFERENCE

## 3.1 INTRODUCTION

As discussed in Section 2, EMI is generated through the operation of electronic equipment. Multiple ways are available to mitigate the EMI produced by such equipment which includes the standard method of adding EMI filters to the entry-point (front-end) and exit (back-end) of the devices.

The alternate method of EMI mitigation is to employ good design techniques in order to reduce the production of EMI in the first place. This firstly includes addressing the generation mechanisms of DM and CM EMI as discussed in Section 2.3.2.2 and 2.3.3.2, which primarily addresses the physical contributors including methods to reduce EMI in terms of layout.

Secondly, the method to be investigated within this dissertation is the so called balancing of a converter, which incorporates the knowledge of how CM EMI is generated with reference to circuit parasitics unbalance. It incorporates the schematic balance of a circuit in order to reduce CM EMI. Schematic Balance as referred to henceforth describes the method by which a normally unbalanced circuit is then balanced on paper or on a circuit level to achieve in theory, identical parasitic components across active semiconductor components. The method by which schematic balance reduces EMI is documented in Section 3.2.

In addition to schematic balancing through circuit symmetry, an investigation into the physical circuit orientation and physical circuit symmetry shall be investigation to determine the efficacy on EMI mitigation. The investigation into physical orientation and achieving physical layout symmetry shall be noted as Geometric Symmetry henceforth.

## 3.2 BALANCED CONVERTER THEORY

The theory and methods to schematically balance a converter and the subsequent mitigating effects on EMI are discussed in this Section.

The theory covered within Section 3.2 covers schematic balance and the application to converters where schematic balance pertains only to balancing parasitic components by certain methods and disregards the physical construction or 3D layout of the circuit. Geometric balance in contrast, pertains to achieving Geometric Symmetry of the physical converter and is discussed further within Section 3.4. No reference to physical circuit balance (also called Geometric Symmetry or Geometric Balance) is presented within [9], nor the construction of a physically balanced circuit.

### *3.2.1 Principles of Operation of an Unbalanced Converter*

The processes by which an unbalanced converter generates EMI are discussed here.

### 3.2.1.1 Unbalanced Circuits and CM

To illustrate the method by which a foundation for predominantly CM EMI generation through unbalance is illustrated in Figure 3-1. Taking the example of a classic converter, the boost converter, which illustrates a single parasitic capacitance present (the Drain to ground capacitance), which is typically not considered or known of during normal design procedures.

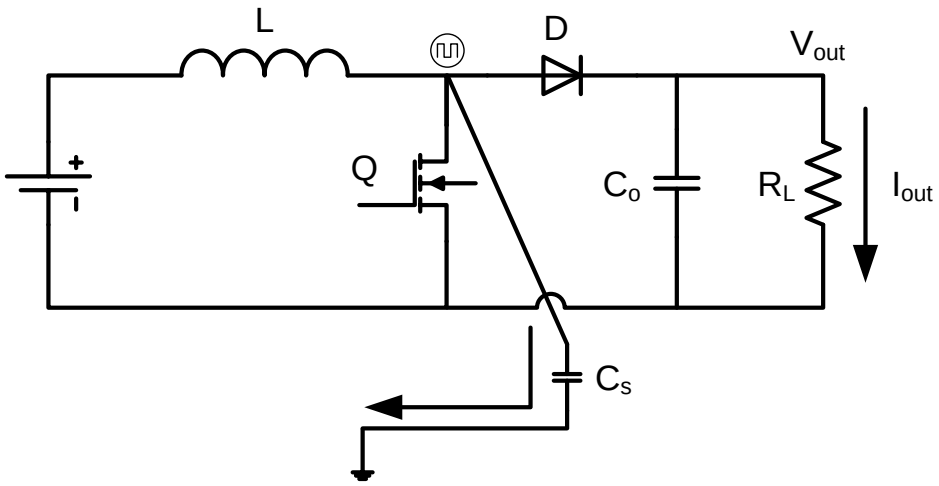



**Figure 3-1 Boost Converter Illustration CM EMI Generation [9]**

The presence of such parasitic components during the operation of a converter provides a conduction path for high frequency currents between the drain of the switch *Q* and ground as discussed in section 2.3.3. As is typical with boost converters, the Source of the switch is connected only to the negative of the supply. No parasitic component with reference to ground and the Source of switch *Q* are present.

The circuit within Figure 3-1 is said to be Unbalanced due to the absence of an identical parasitic capacitance between the Source of switch *Q* and ground, which would make the circuit schematically balanced.

### 3.2.1.2 Foundation for Common Mode EMI Generation process through Unbalance

As is present in Figure 3-1 and discussed within Section 3.2.1.1, an unbalance in voltage is present across switch *Q*.

The voltage present at the node (Drain) is due to the presence of the inductor *L* within the boost converter. The inductor naturally has a high frequency impedance and through the high frequency switching of the switch *Q*, a high frequency current is drawn through *Q* and hence through *L*. Due to the impedance of *L* and the high frequency current drawn through *L* a high frequency voltage across *L* is present.

As the Drain of *Q* is at the same node as the inductor *L*, a high frequency voltage is thus present at the drain of *Q*. The presence of the parasitic capacitance $C_s$ thus provides a path to ground and hence a Common Mode Current can flow through a ground return path to the supply.

Figure 3-2 illustrates a simplified representation of a boost converter circuit to highlight the CM Current path when connected to a LISN in order to measure CM currents.

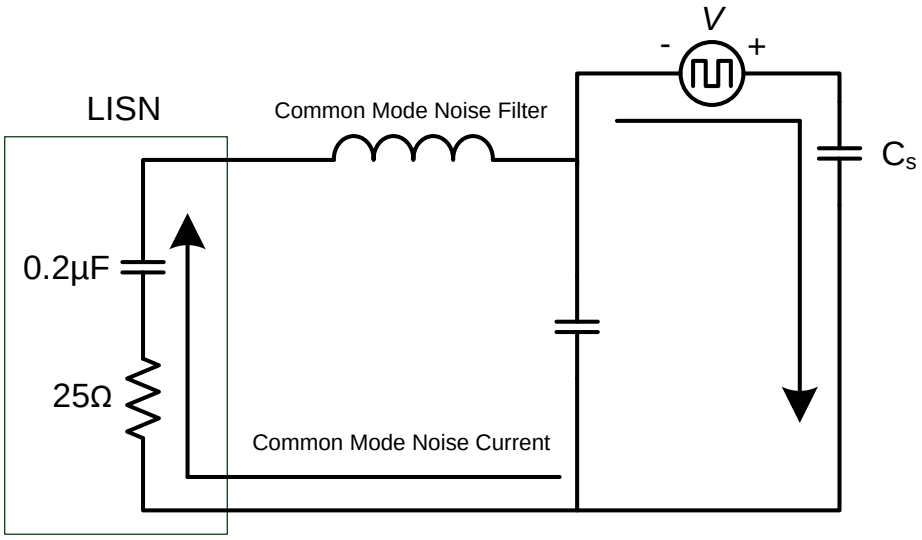



**Figure 3-2 Simplified Boost Converter CM Path [9]**

### *3.2.2 Balancing a Converter*

The process by which a converter is schematically balanced and the resulting reduction primarily in CM EMI is discussed. The method to achieve schematic balance is illustrated.

#### *3.2.2.1 Schematically Balancing a Converter*

As discussed, Figure 3-1 was said to be schematically unbalanced. Figure 3-3 illustrates the conduction path available in Figure 3-1 provided by the parasitic components as discussed in section 3.2.1.

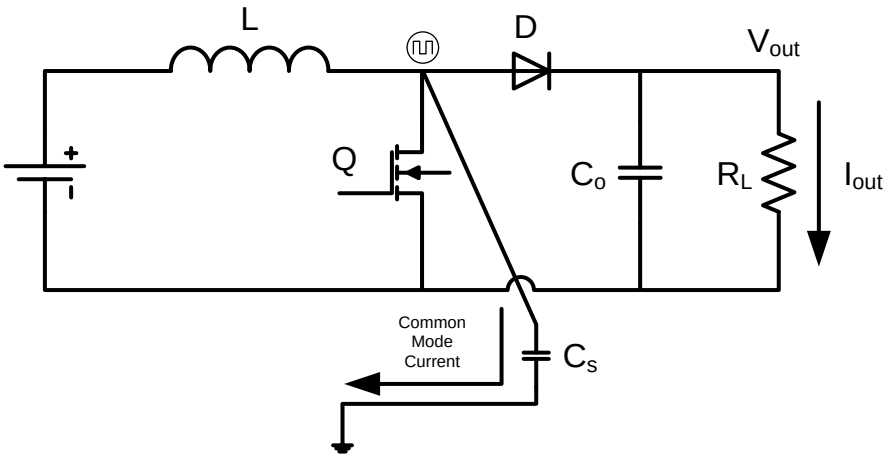



**Figure 3-3 Unbalanced Boost Converter [9]**

In order to mitigate the common mode EMI generated within the circuit illustrated in Figure 3-3, the method of schematically balancing a circuit is presented in Figure 3-4.

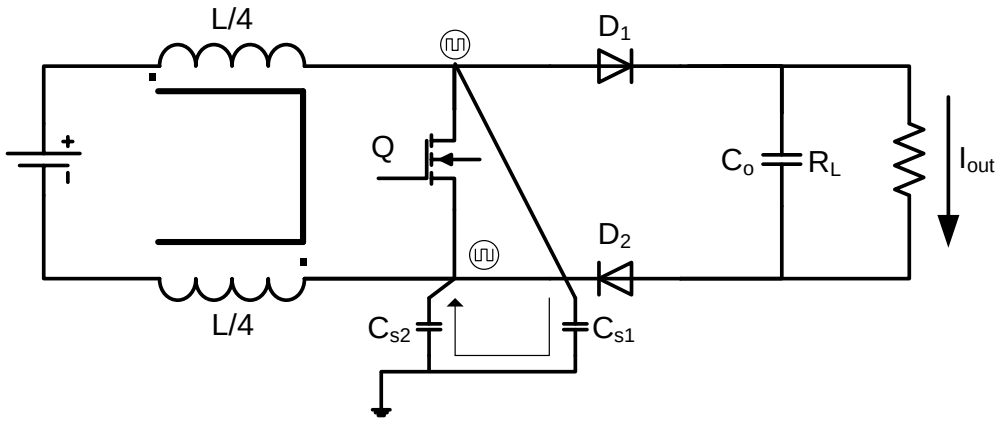



**Figure 3-4 Balanced Boost Converter [9]**

Figure 3-4 is said to be Schematically Balanced according to [1] and [9]. The balance of the boost converter is achieved by maintaining "symmetry" about an imaginary horizontal dividing line in the case of a boost converter. By maintaining said symmetry the converter becomes balanced. The reasoning behind how the process achieves said balance is discussed in section 3.2.2.2.

In the example of a boost converter, balance is achieved by the addition of *D2* to provide a mirroring diode to *D1*. The inductor for the boost converter is then split into two but kept on the same core. The total inductance however remains identical to the inductance in Figure 3-3 to maintain identical converter operation.

### *3.2.2.2 Process by which balancing has a mitigating effect on EMI*

In Figure 3-4, the process by which schematic balance is achieved has been shown, and in Section 3.2.1.2, the process by which EMI is generated through unbalance.

Figure 3-5 illustrates a simplified version of Figure 3-4 where the EUT (Equipment Under Test) is connected to a LISN.

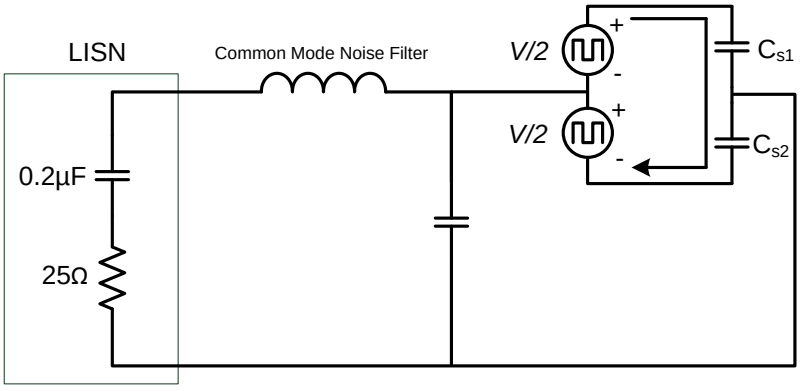



**Figure 3-5 Simplified Balanced Boost Converter CM Path [9]**

By creating a mirrored or symmetric circuit in Figure 3-4 there is now present an additional diode *D2* and inductor within the circuit. The converter operation as normal generates the voltages at the upper node to cause common mode currents to flow. The addition of the inductor on the negative rail introduces an inductance identical to the inductance of the positive rail.

Due to high frequency currents and impedances within the inductor, during normal operation of the converter, equal but opposite voltages across the inductors will be present as discussed in section 3.2.1.2. The addition of the diode *D2* within Figure 3-4 gives rise to the additional parasitic component $C_{s2}$.

The equal but opposite voltage waveforms present at the Drain of *Q* and Source of *Q* in conjunction with the addition of parasitic impedance $C_{s2}$ provides a conduction path for the common mode current in such a manner that the currents circulate within the converter circuit as illustrated, thus being short circuited within the converter and not allowed to circulate through a ground-path.

The process of containing the Common Mode currents within the converter reduces the Common Mode EMI generated by the converter through the action of prohibiting the Common Mode EMI from being emanating from the converter. Through the process of preventing Common Mode EMI emanation, Common Mode EMI is mitigated as conducted EMI is reduced which can lead to a reduction in Radiated EMI.

## 3.3 BALANCED CONVERTER EXAMPLES

The section within discusses other conventional converters and their schematically balanced counterpart circuits and how to modify such circuits to achieve schematic balance.

### *3.3.1 Boost Converter*

Figure 3-6 illustrates a conventional unbalanced boost converter.

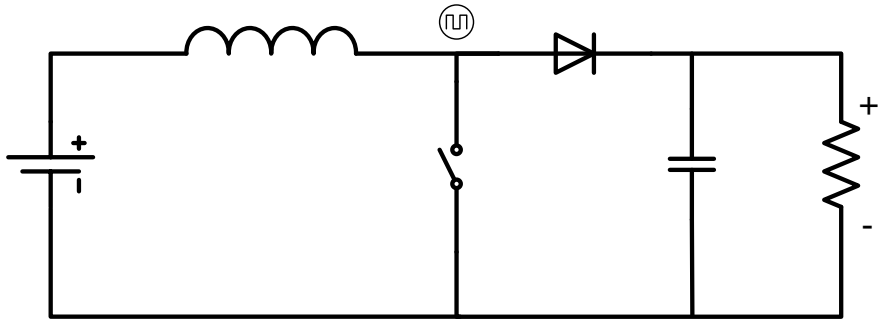



**Figure 3-6 Conventional Boost Converter [9]**

Figure 3-7 illustrates a schematically balanced boost converter.

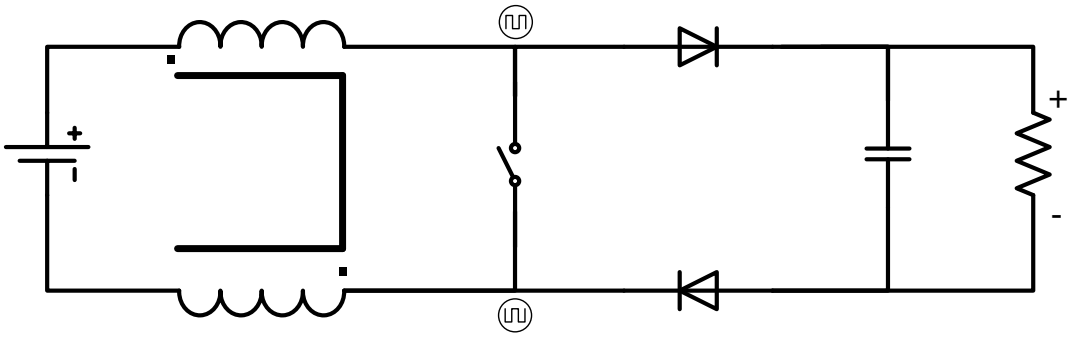



**Figure 3-7 Balanced Boost Converter [9]**

The schematic balance of a boost converter is achieved by the addition of an additional diode in the opposite direction to the original and by splitting up the boost inductor into two inductors on the same core, with orientation as illustrated to maintain normal operation of the original converter.

### *3.3.2 Buck-Boost Converter*

Figure 3-8 illustrates a conventional schematically unbalanced two winding buck-boost converter. In comparison to Figure 3-6 there are similarities in the circuit structure and hence the unbalance mechanisms which Common Mode EMI arises from, which includes a single switch and diode.

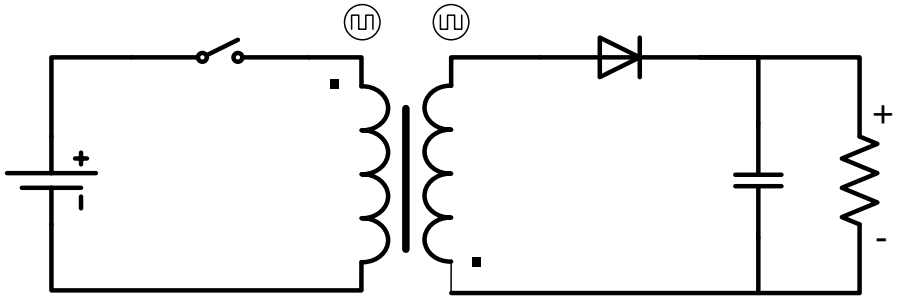



**Figure 3-8 Conventional Buck-Boost Converter (Two Windings) [9]**

Figure 3-9 illustrates the schematically balanced counterpart circuit to Figure 3-8, the balanced two – windings buck-boost converter.

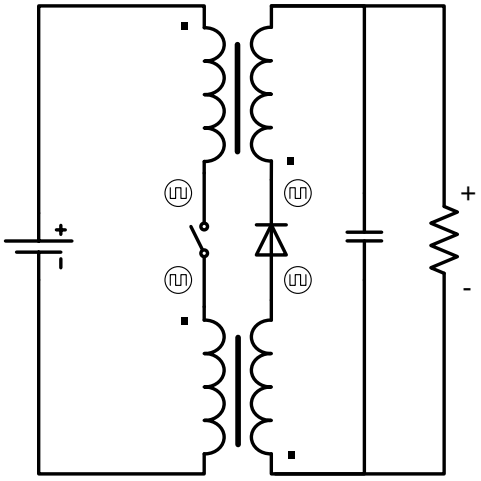



**Figure 3-9 Balanced Buck-Boost Converter (Two Windings) [9]**

Similarly with the conventional boost converter, the balance on the primary side of a buck-boost converter is achieved by the splitting of the primary side of the inductor into two separate inductors on the same core with the orientation as illustrated in Figure 3-9. The splitting of the inductor into two thus provides a complimentary voltage across the switch which in turn leads to the circulation of Common Mode currents within the parasitic components within the circuit and thus no Common Mode currents flow through the ground-path.

To achieve balance on the secondary side and to maintain identical converter operation, the inductor once again is split into two separate inductors on the same core oriented in a fashion as illustrated in Figure 3-9. Similarly with the secondary side of the buck-boost converter, the separation of the secondary inductor into two causes a complimentary voltage across the diode and hence allows the generated Common Mode currents to circulate within the secondary side rather than flowing through the ground return path.

In the case of a buck-boost converter, schematic balance is achieved without the addition of components but rather the winding scheme of the coupled inductor.

### *3.3.3 Naturally Balanced Converters (Schematically)*

Figure 3-10 illustrates a full bridge converter and a full bridge rectifier circuit.

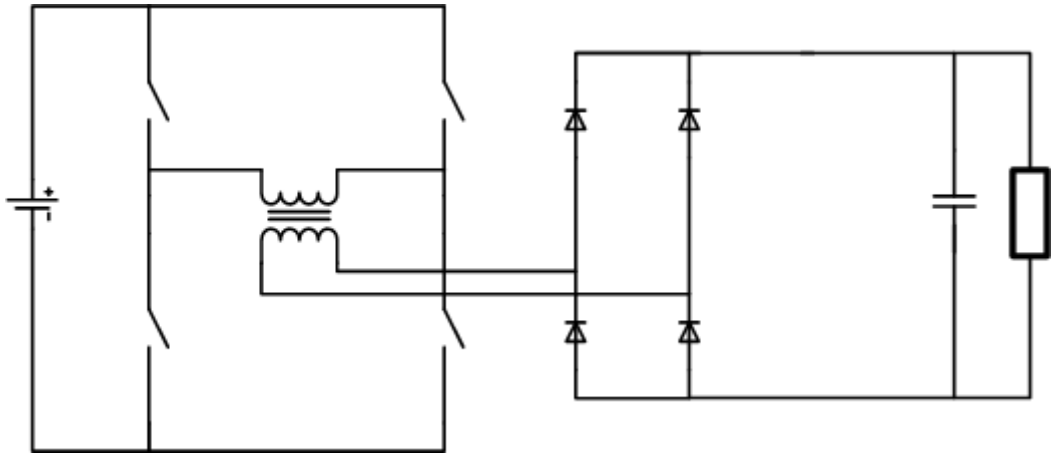


**Figure 3-10 H-Bridge Converter and Full-Bridge Rectifier**

A full-bridge (H-bridge) converter and a full-bridge rectifier circuit are naturally balanced such as they need zero additional components or modified inductor or transformer winding strategies to achieve schematic balance. The need for no additional components or winding strategies makes the circuits desirable candidates for circuits with naturally mitigated Common Mode EMI. Therefore this H-bridge topology will be used for experimental purposes in this study.

Section 3.5.1 thus discusses the details behind the natural circuit balance and the half-cycle analysis of an H-bridge converter and shows how it is naturally schematically balanced.

## 3.4 PHYSICAL LAYOUT BALANCE (GEOMETRIC SYMMETRY)

The following section discusses Geometric Balance or Geometric Symmetry, the physical layout symmetry and the application thereof to the converters and the possibility of EMI mitigation.

### *3.4.1 Hypothesis*

The evidence of Schematically Balancing a circuit shows theoretical promise to mitigate Common Mode EMI to some extent [9], however no reference is presented where the physical construction of a Geometrically Symmetrical implementation of any converter or the mitigating effects if any are discussed.

An investigation into balancing a circuit or converter physically by means of orientation of components within the layout is speculated to aid in the mitigating effect primarily of Common Mode but also Differential Mode EMI.

The physical layout balance shall be denoted as Geometric Symmetry henceforth.

#### *3.4.1.1 Physical Layout Symmetry*

Firstly in order to achieve Geometric Symmetry, the use of a Schematically Balanced circuit is to be used.

The physical placement of components within the physical circuit (circuit layout), shall be in such an orientation as to form a mirror image of the circuit if an imaginary mirror line is to be drawn through the circuit.

The symmetry is not limited to a single plane only as the circuit may be symmetrical in a vertical and horizontal plane.

### *3.4.2 Electromagnetic Perspective*

Through circuit Geometric Symmetry, it is speculated that through orientation of components, electromagnetically there is a possibility of electromagnetic cancellation through correct placement of components.

Switch pairs within a phase arm placed back to back on different sides of a Printed Circuit Board (PCB) are speculated to have a mitigating EMI effect, as this is speculated to reduce the effective coupling area presented to the ground plane.

In EMI, wires or traces are not just conductors and need to be considered holistically as they are a combination of inductance, capacitance and resistance [14].

## 3.5 PROPOSED DESIGN

The following section discusses the proposed design of multiple circuit layouts to evaluate the hypothesis of Geometric Symmetry and the mitigating effect on EMI.

### *3.5.1 H-Bridge Converter and Full Bridge Rectifier Circuit*

Figure 3-11 represents a Full-Bridge converter and Full-Bridge rectifier circuit with output filter and load.

The circuit in Figure 3-11 during operation is nearly naturally Schematically Balanced and therefore a good candidate for testing the hypothesis of Geometric Symmetry as minimal circuital change is required.

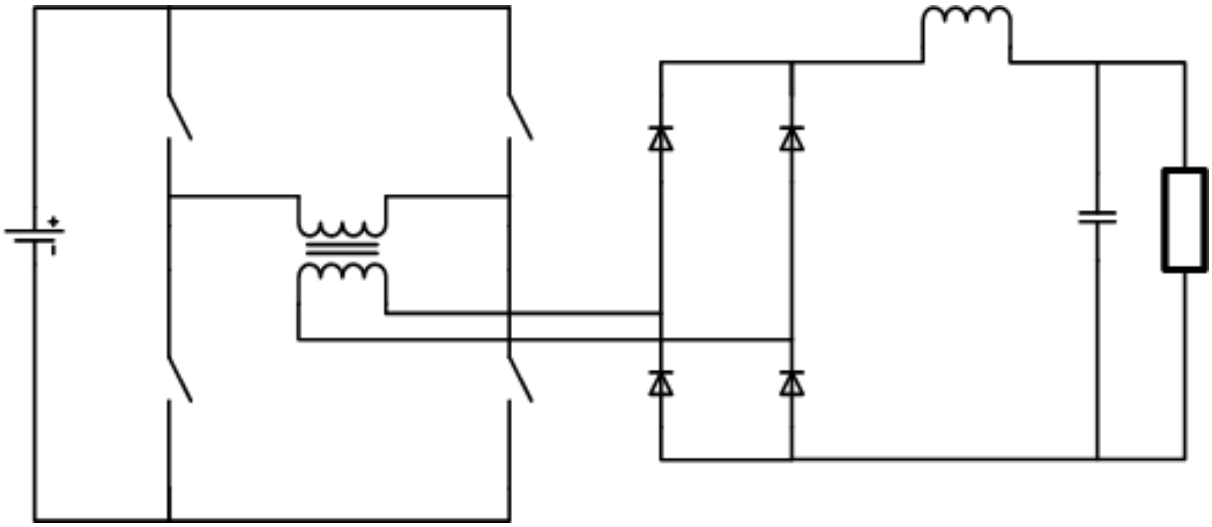


**Figure 3-11 H-Bridge Converter and Full-Bridge rectifier with output filter**

Section 3.5.1.1 discusses half cycle analysis to illustrate the inherent balance of the converter.

### *3.5.1.1 Naturally Balanced Circuit*

Figure 3-12 represents the half cycle analysis of the circuit in Figure 3-11.

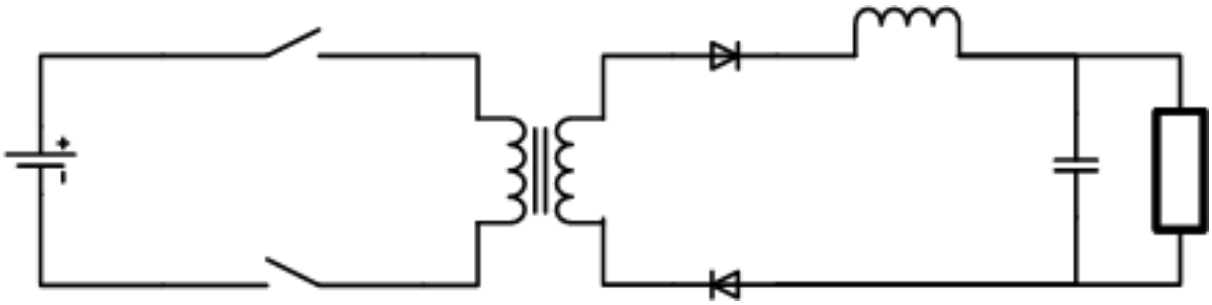


**Figure 3-12 Half -Cycle analysis of Full-Bridge converter and Full-Bridge rectifier**

During normal circuit operation, only a single diagonal phase arm operates and only two rectification diodes conduct to form the circuit as illustrated in Figure 3-12.

The circuit in Figure 3-12 is almost a Schematically Balanced circuit with the exception of the output filter inductor as highlighted in Figure 3-13.

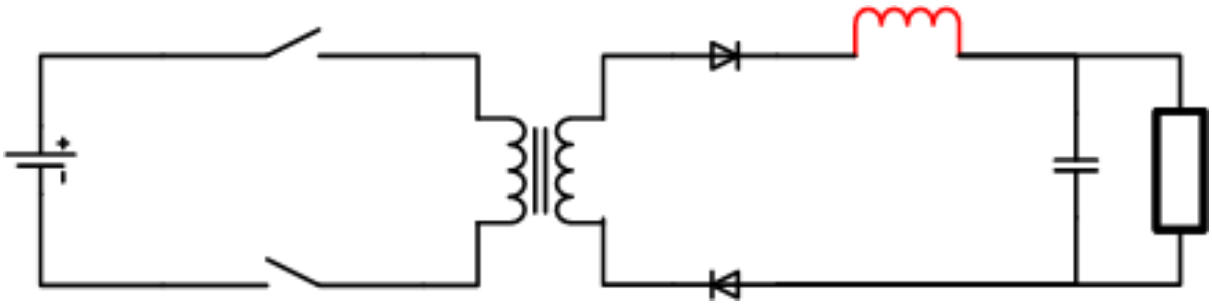


**Figure 3-13 Output Filter Unbalanced Component**

In order for Figure 3-13 to be Schematically Balanced, the output filter inductor needs to be changed in a manner to aid schematic balance.

Similarly as in section 3.3.1, the output inductor needs to be split into two but remain on the same core as to facilitate schematic balance. Figure 3-14 illustrates the half-cycle analysis with the split output filter inductor to achieve said schematic balance.

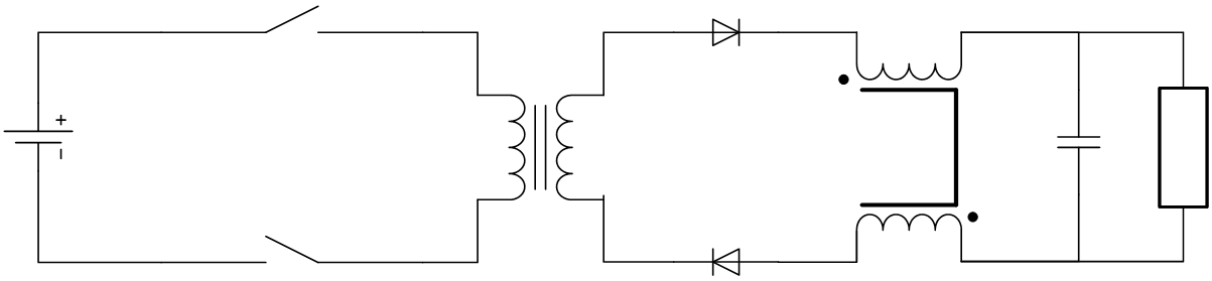


**Figure 3-14 Schematically Balanced Full-Bridge Converter with Full-Bridge Rectifier and output filter**

If the circuit in Figure 3-11 is absent of the output filter inductor as in Figure 3-10, the circuit is naturally Schematically Balanced and hence no further circuit modification is required to achieve said balance.

### *3.5.1.2 Symmetrical Physical Layout Potential*

The natural Schematic Balance of the circuit in Figure 3-10 aids itself in the requirement of testing the hypothesis in section 3.4.1. The natural Schematic Balance means there are no complicated components added or the need for complicated trace layouts.

Due to there being even multiples of components where more than a single component is present in the circuit facilitates Geometric Symmetry and the testing thereof as the ability to form a physically mirrored circuit is much more easily obtainable.

### *3.5.2 Physical Layout*

To test the hypothesis discussed in section 3.4.1, a selection of differing physical circuit implementation layouts of the circuit in Figure 3-10 are developed and discussed here.

#### *3.5.2.1 Circuit 1*

Circuit 1 forms the baseline circuit upon where no knowledge or consideration for circuit layout shall be demonstrated. Circuit 1 shall be constructed on Veroboard to demonstrate lack of layout consideration with particularly large track loops and MOSFET spacing.

Through-hole components are to be utilised.

#### *3.5.2.2 Circuit 2*

Circuit 2 forms the second baseline circuit where there is no major particular attention paid to layout symmetry, but rather a typical layout where the switching components in the circuit are laid out adjacent to each other on the same plane.

Circuit 2 is to be absent of a ground-plane or top copper pour layer. Surface mount semiconductors are to be used.

#### *3.5.2.3 Circuit 3*

Circuit 3 forms a test platform where the circuit is split into two circuit boards where a phase arm is present on one PCB and the other on a different PCB.

The PCBs are to be joined in such a way as to be perpendicular to each other. One PCB shall have a ground pour on the bottom plane and the second PCB to be absent of the ground pour. Both PCBs are to be absent of a top copper pour.

Circuit 3 is designed to illustrate more than just symmetry and the effects on EMI but to illustrate the phenomena of coupling and Common Mode EMI. Surface mount semiconductor devices are to be used for Circuit 3.

#### *3.5.2.4 Circuit 4*

Circuit 4 is the circuit with a Geometrically Symmetrical layout.

The circuit is to be designed such that the circuit is physically symmetrical in context of component locality and trace layout.

Circuit 4 shall be void of any ground pours or top copper pours. Circuit 4 shall use surface mount semiconductor devices.

## 3.6 CONCLUSION

The concept and introduction of balanced converters have been introduced. The theory pertaining to Schematically Balancing a converter and why a converter is termed schematically unbalanced from an EMI perspective. The process of Schematically Balancing a converter is presented and the mitigating effect which Schematic Balance has on EMI is presented. Examples of Schematically Balancing a converter have been presented, which includes naturally balanced examples. The concept of Geometric Symmetry has been introduced through physical layout symmetry of a circuit or PCB. The proposed design for the dissertation has been documented where four separate PCB's are to be designed and implemented to demonstrate various EMI mitigating or aggravating techniques. One of the said designs includes a Geometrically Symmetrical layout. The relevant design and implementation process is documented within Chapter 4.

# 4 DESIGN AND IMPLEMENTATION

## 4.1 INTRODUCTION

Section 4 entails the design and implementation of the Printed Circuit Boards as discussed in section 3.5.2. Design specifics pertaining to achieving a repeatable test setup and relevant supporting circuit specifications and their appropriate design are also detailed within this section.

Other peripheral circuits, facilitating components and equipment are required to facilitate the operation and thus allow the H-Bridge converters to function. The relevant components, equipment and associated specifications are highlighted within the following sections and the rationale behind the requirement of said components, circuits and equipment.

In order to test the hypothesis of Geometric Symmetry of the H-Bridge converter and solely the H-Bridge layout, it was decided to maintain consistency of all other circuit layouts by containing the H-Bridge converter to an isolated PCB only with relevant connections to the other assisting circuits.

Therefore a consistent setup was developed where the only changeable parameter is the Device Under Test (DUT), being the H-Bridge section, removing other influencing factors that would arise by combining the H-Bridge PCB's with the other relevant circuits in order to function.

A system by which to operate, test and evaluate the DUT's is hence described to evaluate the hypothesis and other phenomena associated with EMI.

## 4.2 GENERAL DESIGN SPECIFICATIONS

The equipment and circuit components used and their associated specifications pertinent to the setup are discussed here.

The supply to the DUT shall be a Linear DC Power Supply. A Linear DC Power Supply was chosen as the DUT requires a DC power source and a Linear power supply provides a much cleaner supply opposed to a switching power supply when EMI measurements are required.

The DUT's require switching semiconductor devices. MOSFET's were chosen to be used as the specified device.

In order to switch the MOSFET's within the DUT's, MOSFET drive circuitry is required, the rationale of which is discussed in section 4.3. The design of the MOSFET driver circuit is in accordance with the operating specifications of the DUT's.

The General Specifications for the H-bridge circuits were chosen as follows:

- $V_{IN}$ = 12V
- $I_{MAX}$ = 5A
- $V_{OUT}$ = 12V
- $f$ = 20kHz
- $P_{MAX}$ = 60W

## 4.3 MOSFET DRIVER CIRCUITS

As required in section 4.2, the rationale, and circuit design of the MOSFET Driver circuits are documented within.

### *4.3.1 Rationale*

A MOSFET requires a voltage to be applied between the Gate and Source of the device in order for the device to turn on, or in order to provide a conduction path between the Drain and the Source in the case of N-Type MOSFETS. The voltage named $V_{GS}$ is known as the Gate voltage and operates within a threshold where the threshold must be exceeded for the device to conduct and similarly to turn off.

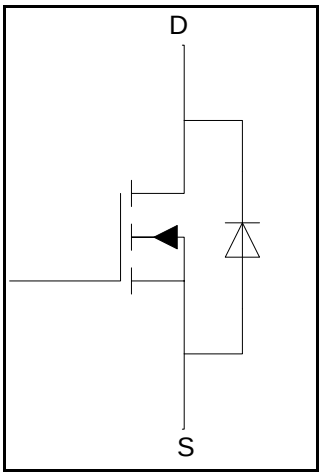



**Figure 4-1 MOSFET [16]**

A MOSFET driver is a device or combination of components to provide the required gate-source voltage and sufficient supply current to drive the MOSFET.

In the situation of an H-Bridge where there are two MOSFETs arranged in a so called phase arm pair, there is said to be a high side and low side MOSFET.

The low side MOSFET is typically connected with its Source to the ground potential of the circuit**.** In contrast the high side MOSFET is in the situation where the Source of the device is not connected to the ground of the circuit, but to the Drain of the low-side MOSFET and the load. The Source of the high-side MOSFET is said to be floating as the potential of the Source is not at ground potential due to impedance of the load during operation.

To provide a floating drive voltage to the high-side MOSFET a circuit or device is required to supply an isolated voltage across the high-side MOSFET. Such a device is called a high-side driver.

Multiple types of MOSFET drivers exist, of which two methods are presented in Sections 4.3.2 and 4.3.3, with the appropriate additional circuitry and devices to provide the required signals to the drivers according to the specifications outlined in Section 4.2.

The circuits highlighted in Sections 4.3.2 and 4.3.3 are referred to heron as the MOSFET Driver Boards and fulfils the requirement of supplying the DUT's with gate drive signals.

### *4.3.2 Optical Drive with Isolated Supplies*

The first MOSFET Driver Board is based on an optically coupled MOSFET Driver called a TLP250 Opto-Coupler.

The rationale behind using the TLP250 is the requirement of an isolated supply for each driver. Each TLP250 requires a floating supply and hence can be used for either a high side MOSFET or a low-side MOSFET. The TLP250 simply applies the isolated supply to the Gate of the MOSFET upon signal input. A major advantage of using the TLP250 is each isolated supply. The isolated supply should in theory provide isolation for Common Mode current return paths and hence inhibit transfer of Common Mode EMI into the DUT thereby providing false readings.

To facilitate EMI immunity from the source of drive signals, optical transmitters and receivers were used between the TLP250's and the clock source used to generate gate signals.

A TLP250 and an Optical Receiver are placed on a single PCB to form a TLP250 Drive module. Each MOSFET in the DUT requires a single TLP250 Drive module connected to it and hence 4 TLP250 Drive modules are required.

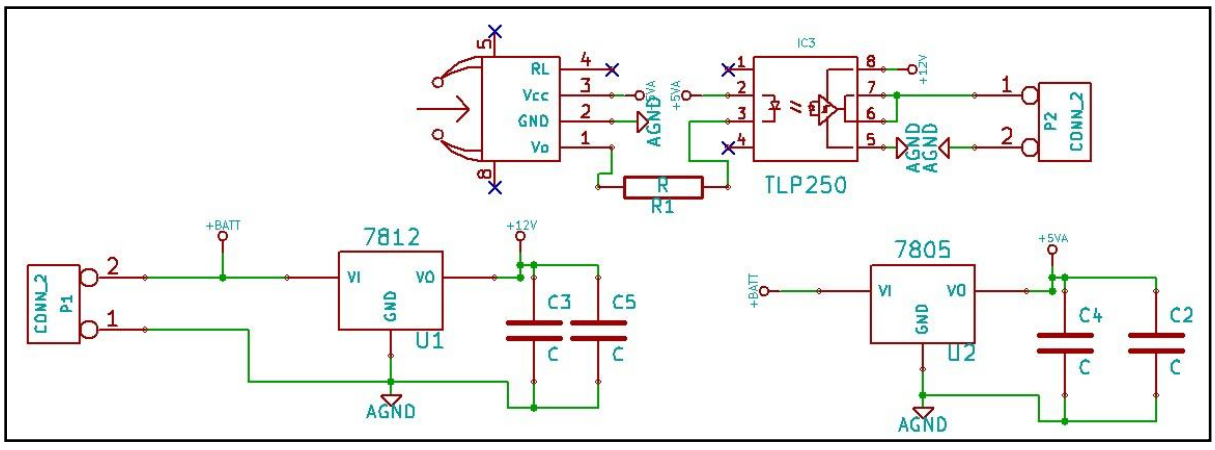



**Figure 4-2 TLP250 Drive Module**

Figure 4-2 represents the circuit diagram for each TLP250 Drive module. The isolated supply feeds the drive module with 12V DC and the optical cable delivers the required drive signal. The drive module is then directly connected across the Gate and Source of an

appropriate MOSFET in the DUT. The 12V DC isolated supply for each TLP250 Drive module is achieved through four separate isolation transformers and rectifier circuits as illustrated in Figure 8-2.

The TLP250 Drive modules are connected to the Optical Signal Generator Board through optical cable. The circuit for the Optical Signal Generator Board is illustrated in Figure 4-3.

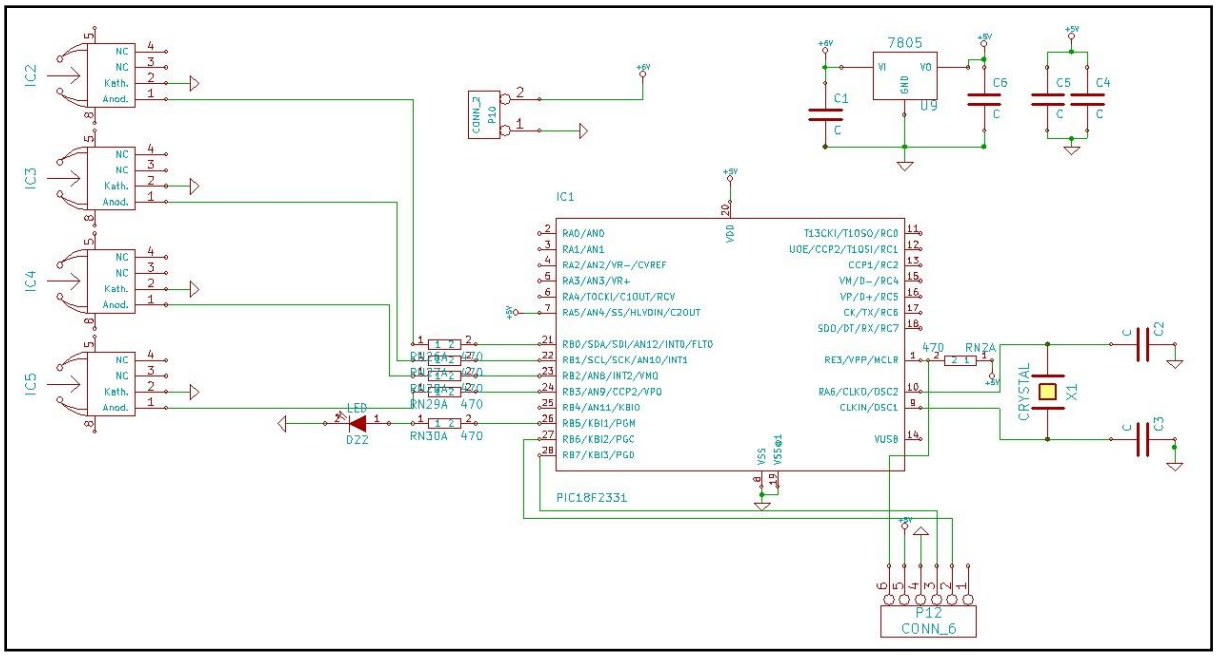



**Figure 4-3 Optical Signal Generator Board**

To provide the required signal waveforms to drive the H-Bridge with a 50% Duty-Cycle at 20 kHz, a Microchip PIC 18F2331 Microcontroller was used and programmed to deliver the drive signals. A Microcontroller was chosen as to facilitate change in drive frequency and duty cycle with no change in any physical hardware (e.g. resistor or capacitor values) should the need arise. A Microcontroller also generates drive signals accurately with relative immunity to temperature variance due to the use of crystal oscillators.

The signals from the PIC Microcontroller are fed to the optical transmitter of which there are four. All the components on the Optical Signal Generator Board provide the necessary optical drive signals for the TLP250 Drive Modules.

AVAGO HFBR-0501 Series Versatile Link Optical Transmitters and Receivers were used in the Optical Signal Generator Board and the TLP250 Drive Modules. These devices were chosen as the bandwidth of the devices are stated as 5 MBd and hence have sufficiently low rise and fall times as not to impede the 20 kHz and higher drive frequency of the DUT's.

### *4.3.3 Non-Isolated Drive (IR2113 Drivers)*

Figure 4-4 below represents the use of IR2113 MOSFET drivers to implement a non-isolated drive solution for the DUTs, henceforth noted as the IR2113 Driver Board.

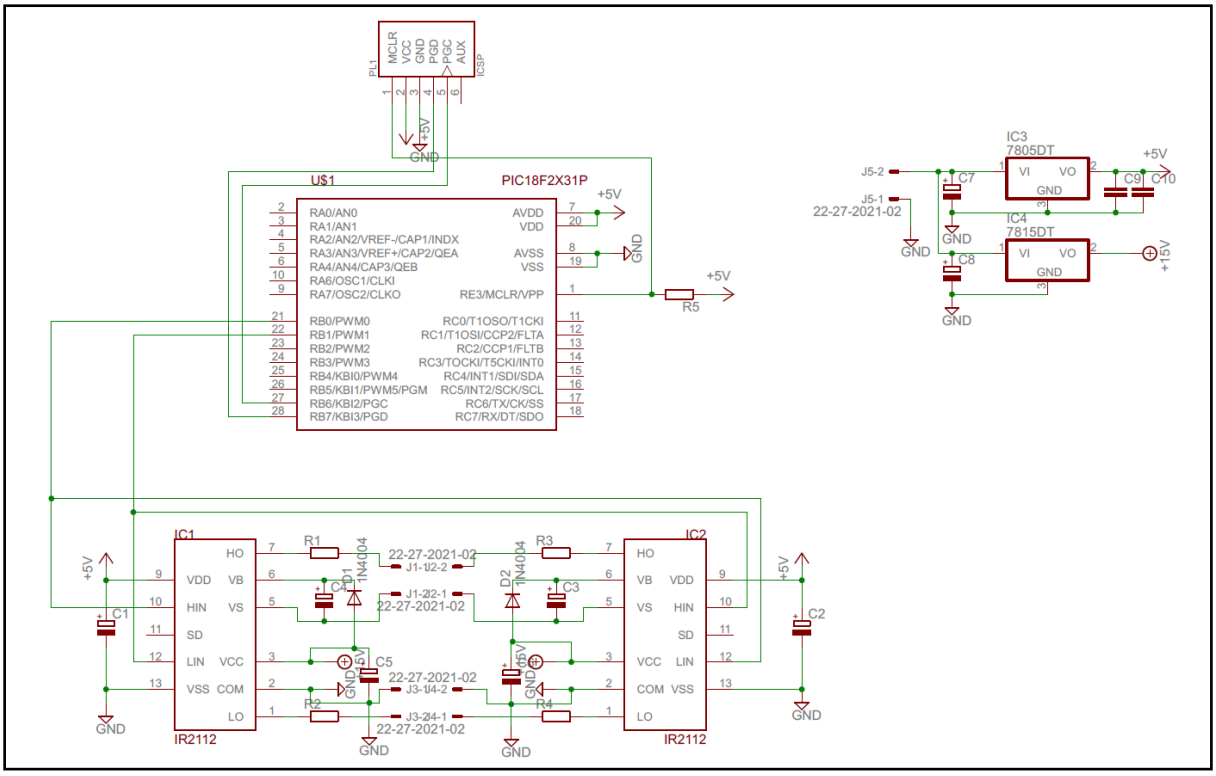



**Figure 4-4 IR2113 Driver Board**

The IR2113 MOSFET Driver is an integrated circuit comprising integrated components which provide a low side and high side MOSFET driving circuit. Each IR2113 is used to drive a phase arm.

The IR2113 differs from the TLP250 in there is no optical isolation or need for isolated or independent power supplies to service the Integrated Circuit (IC). The device relies on the bootstrapping principle to charge a capacitor to create a floating supply. The capacitor is used by the IC during turn on of the high side MOSFET by connecting the capacitor across the Gate and Source of the high side MOSFET.

Similarly to the Optical Signal Generator circuit, a Microchip PIC 18F2331 was used to generate the appropriate drive signals with the same advantages as discussed earlier.

The IR2113 Driver Board also includes the appropriate essential components to operate both the PIC Microcontroller and the IR2113's.

The IR2113 is capable of sourcing and sinking up to 2.5A, hence facilitating sufficient rise and fall times to achieve suitable switch-on and switch-off results of the MOSFETS.

## 4.4 COMPLETE BALANCED CIRCUIT SCHEMATIC

The following section presents the circuit schematics for the DUTs

### *4.4.1 H-Bridge Circuit*

Figure 4-5 represents the general schematic drawn up in EAGLE CAD software. The schematic forms the schematic baseline within the program for which the realisations of the PCB artwork for the differing DUTs within section 3.5.2.

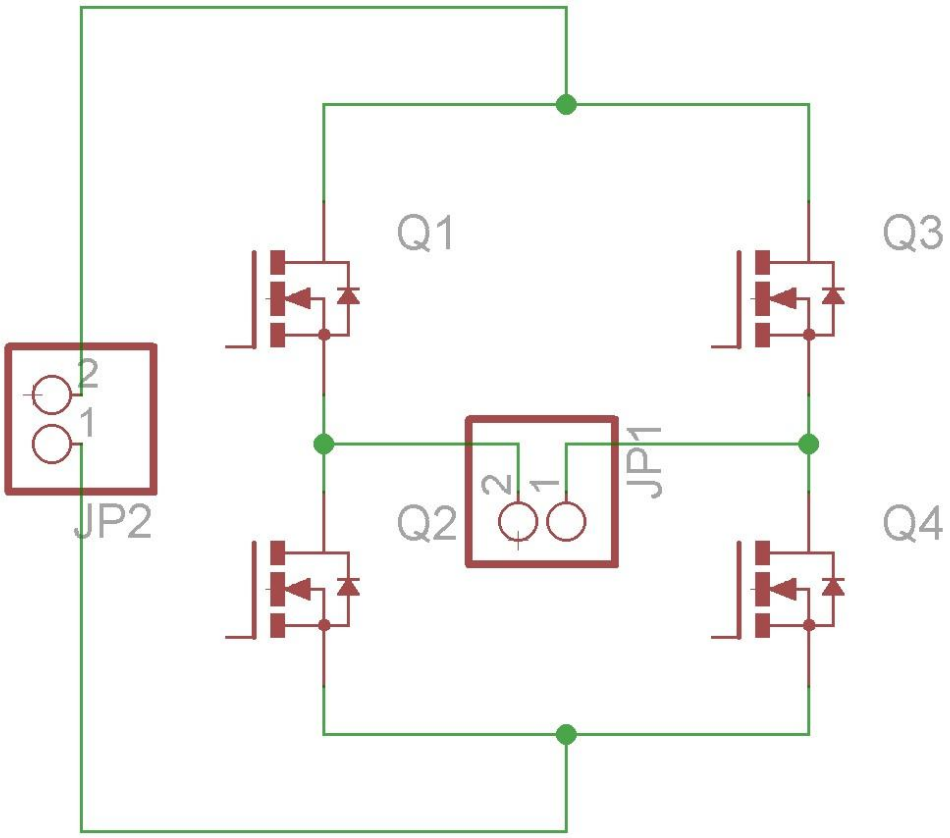



**Figure 4-5 H-Bridge Schematic**

To facilitate the connection of the various H-Bridges to both the LISN (Supply) and to the load, jumper connections were used as both the supply (J2) and load (J1) interface.

Q1 through Q4 represent the MOSFETS used within the H-Bridge circuit.

Interfacing to the Gate-Source on each MOSFET was chosen to be left out within the physical circuit, but rather a set of header pins soldered directly to the appropriate terminals on each MOSFET as to minimise the effect of track layout on the final PCB artwork.

### *4.4.2 Full Bridge Rectifier*

Figure 4-6 presents the Full-Bridge Rectifier circuit as drawn in EAGLE CAD. The Full-Bridge rectifier circuit is required for a DC output and consists of diodes D1 through D4.

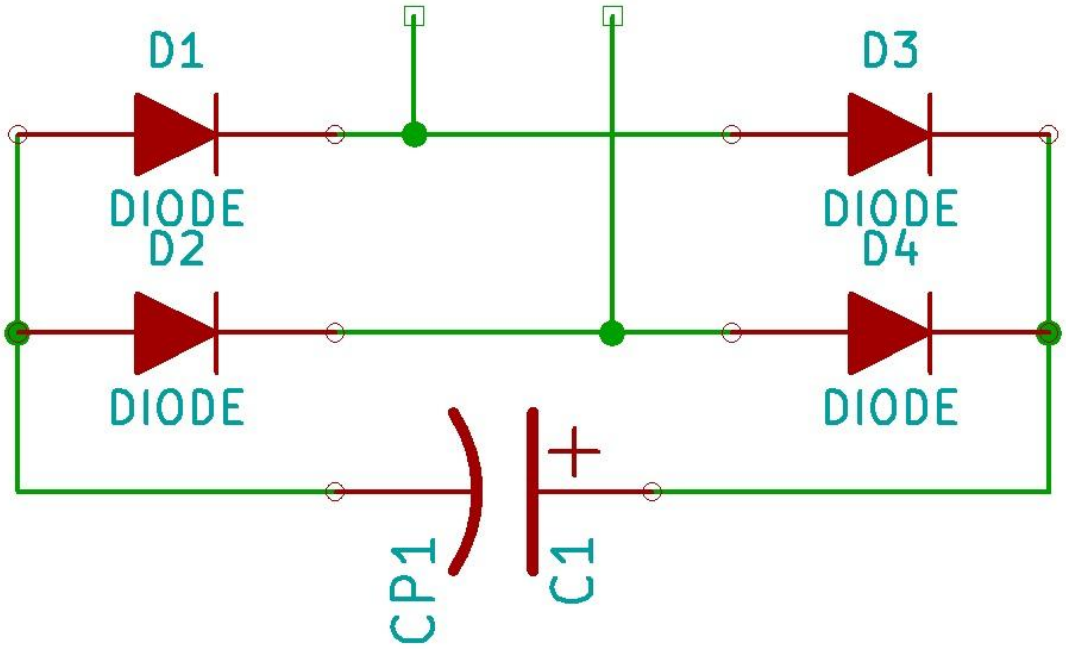



**Figure 4-6 Full-Bridge Rectifier Schematic**

Figure 4-6 was created separately from Figure 4-5 and Figure 4-7 initially as to facilitate the creation of multiple circuit layouts when designing with respect to geometric symmetry.

### *4.4.3 Entire Circuit*

Figure 4-7 presents the completed circuit represented in CAD software, the culmination of the H-bridge (Figure 4-5), full-bridge rectifier (Figure 4-6) and the step-up/step-down transformer, output filter and load.

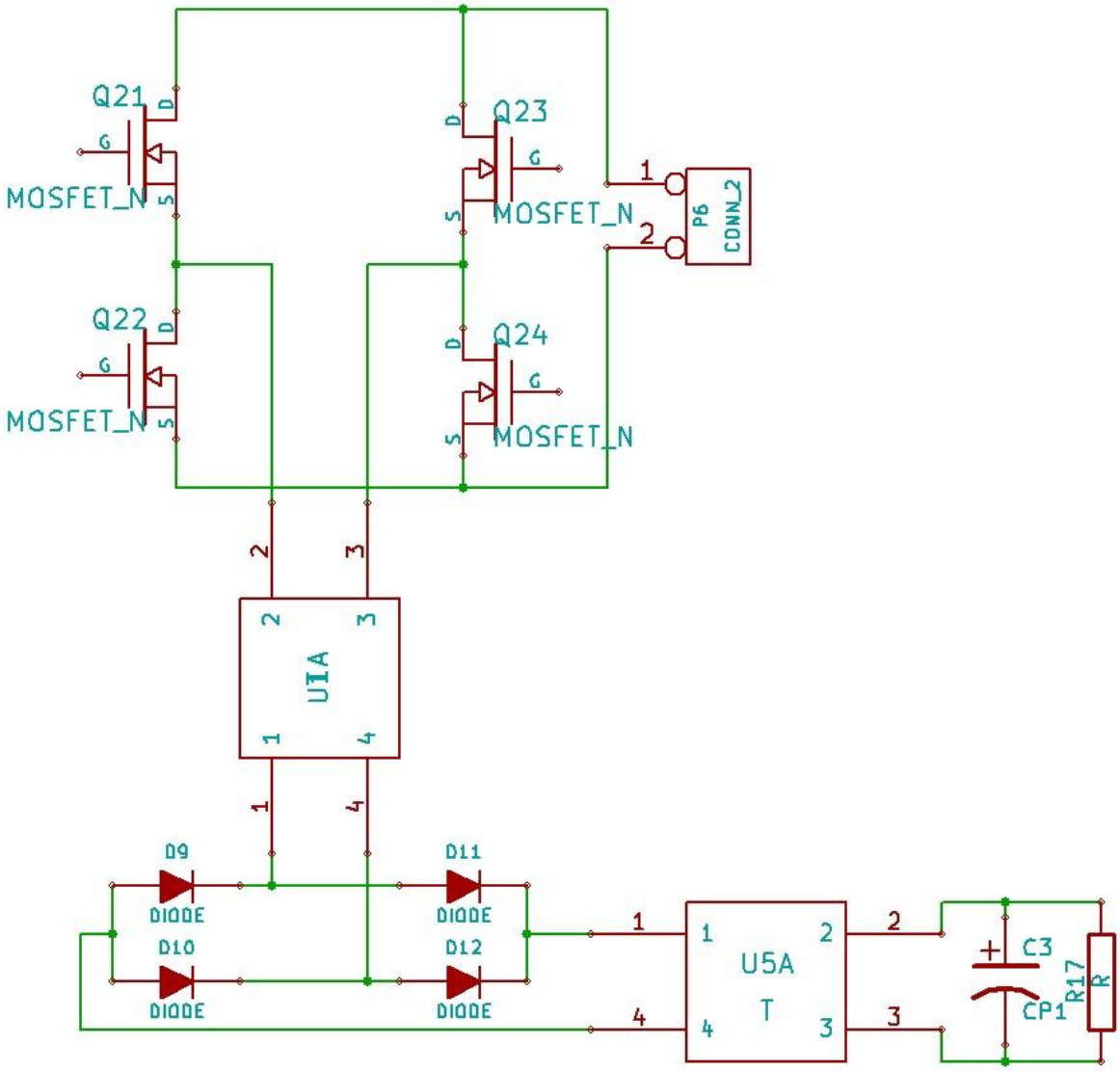



**Figure 4-7 Entire Circuit Schematic**

### *4.4.4 Final Circuit Under Test*

Due to reasons of complexity and multiple variables, investigation into the 3D symmetry of only the H-bridge circuit in section 4.4.1 is considered sufficient for the purpose of the dissertation.

Therefore Figure 4-5 is the final circuit to be realised into various 3D PCB orientations and evaluated within the dissertation.

## 4.5 PCB DESIGN

The following section presents the Printed Circuit Board artwork from the schematics presented in sections 4.3 and 4.4.

### 4.5.1 TLP250 Drive Module

Figure 4-8 represents the artwork developed for the TLP250 driver board. The artwork is derived from the schematic within Figure 4-2.

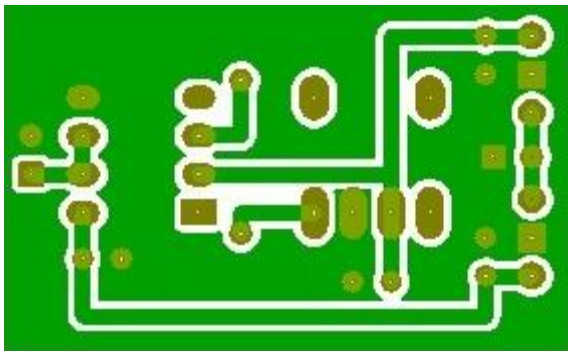


**Figure 4-8 TLP250 PCB artwork**

Similarly with the schematic, the PCB artwork was developed using the KICAD software. A photograph of the implementation of the PCB can be found in Figure 4-15.

### 4.5.2 Optical Signal Generator

The PCB artwork for the Optical Signal Generator is presented in Figure 4-9, which is the artwork corresponding to the schematic in Figure 4-3. As with the TLP250 drive module, the artwork was developed using the KICAD package. Figure 4-14 shows a photograph of the populated PCB of Figure 4-9.

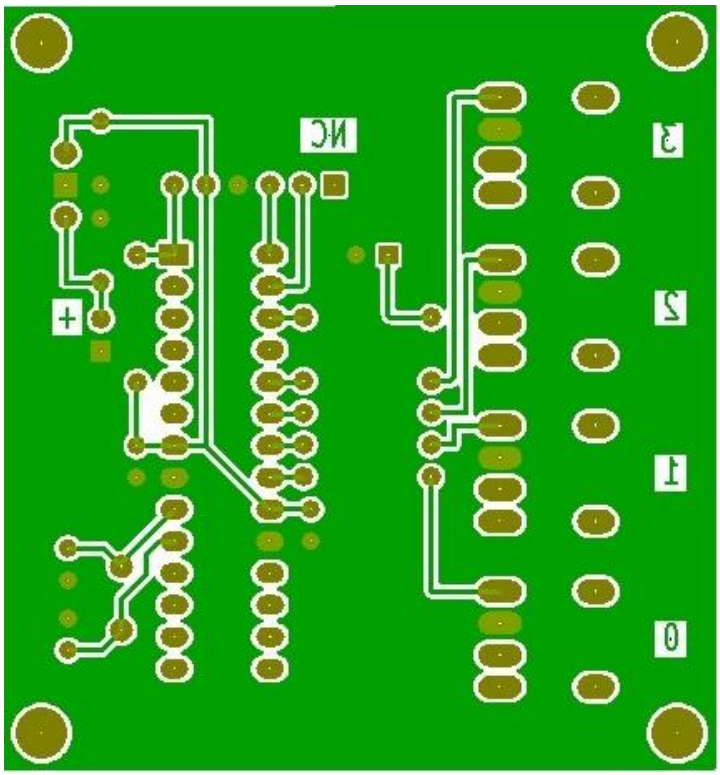



**Figure 4-9 Optical Signal Generator PCB artwork**

### 4.5.3 IR2113 Driver Board

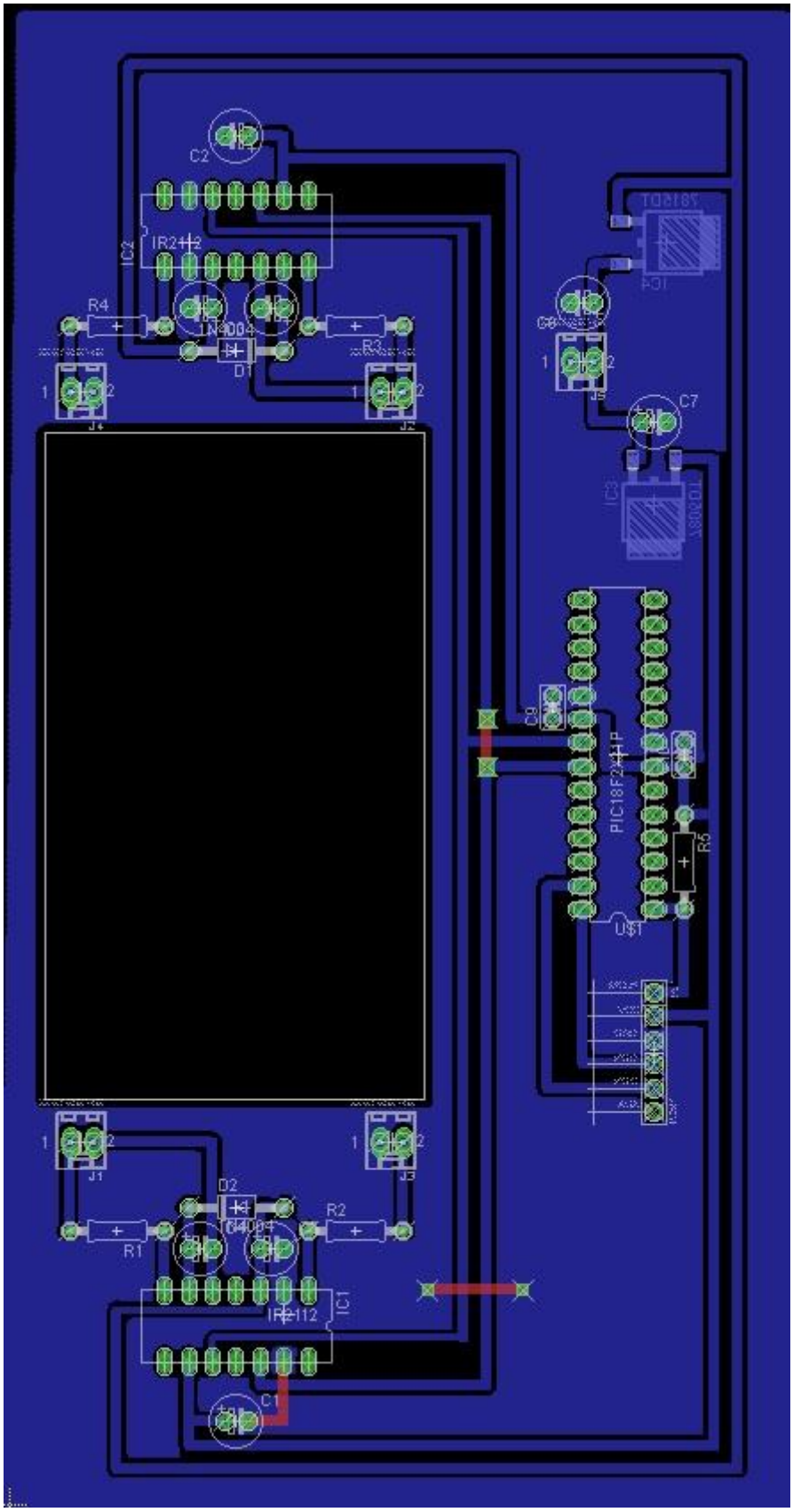



**Figure 4-10 IR2113 Driver Board PCB artwork**

The artwork in Figure 4-10 is that of the schematic in Figure 4-4. The artwork was developed in EAGLE CAD. EAGLE CAD was used to develop the artwork as the implementation or manufacturing of the PCB is substantially aided through the use of CNC equipment. PCB-G-CODE software was used to generate the G-Code within EAGLE CAD which is a free-to-use program.

A photograph of the physical implementation of Figure 4-10 is shown in Figure 4-16.

Various differing PCB layouts to be evaluated against EMI generation are presented below:

### *4.5.4 PCB1 – Baseline*

It was decided that for a baseline H-bridge, Veroboard would be used and thus no PCB artwork is required.

### *4.5.5 PCB 2 – Second Baseline*

The PCB artwork for the Second Baseline DUT is presented in Figure 4-11.

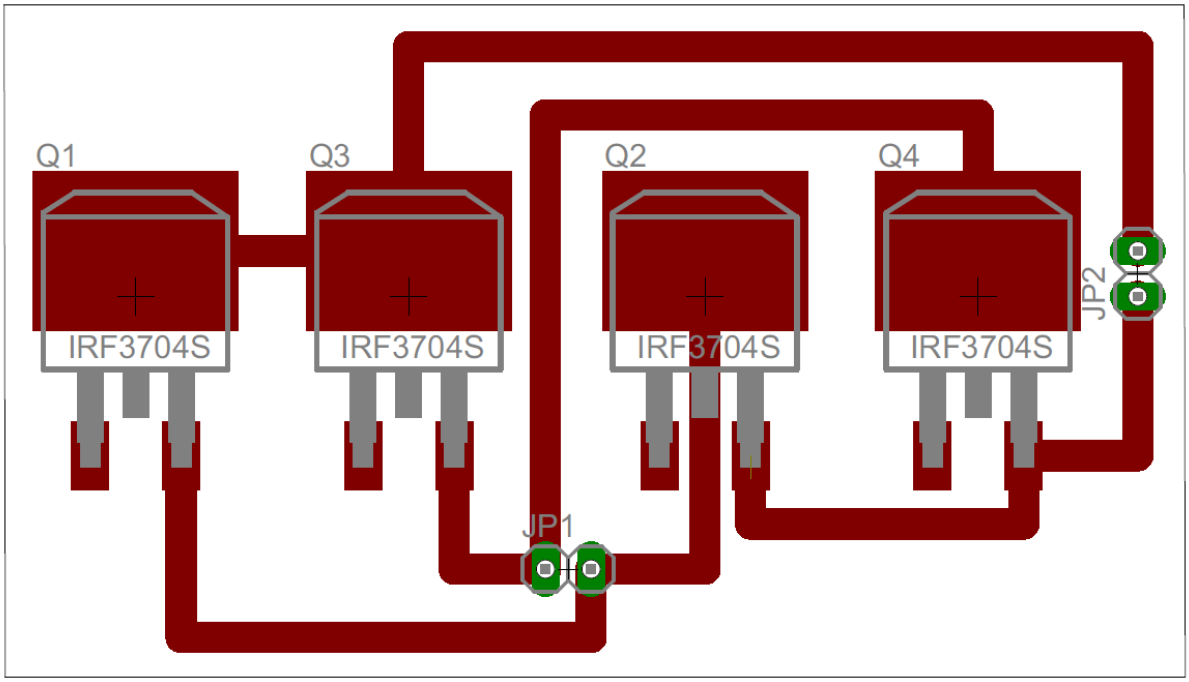



**Figure 4-11 PCB 2 (Second Baseline) artwork**

As required by section 3.5.2.2, the artwork depicts all four MOSFET's placed inline adjacent to each other on a single plane (component plane) without the presence of a copper pour plane. No particular attention was paid to trace routing.

The MOSFET's used are Surface Mount Devices (SMD) and are of the D2PAK footprint.

A photograph of the physical implementation of the artwork in Figure 4-11 can be found in Figure 4-18.

### 4.5.6 PCB 3 – 3 Dimensional Layout

The DUT PCB artwork for an improved 3D layout is illustrated in Figure 4-12. The artwork illustrates the separation of the circuit into two halves. Right-angle header pins shall connect the two halves through jumpers JP4 and JP5.

Both halves are absent of top copper pour planes whilst one half has a ground-plane present as discussed in Section 3.5.2.3. Such said ground-plane is only evident in the implementation as illustrated in Figure 4-19 and Figure 4-20.

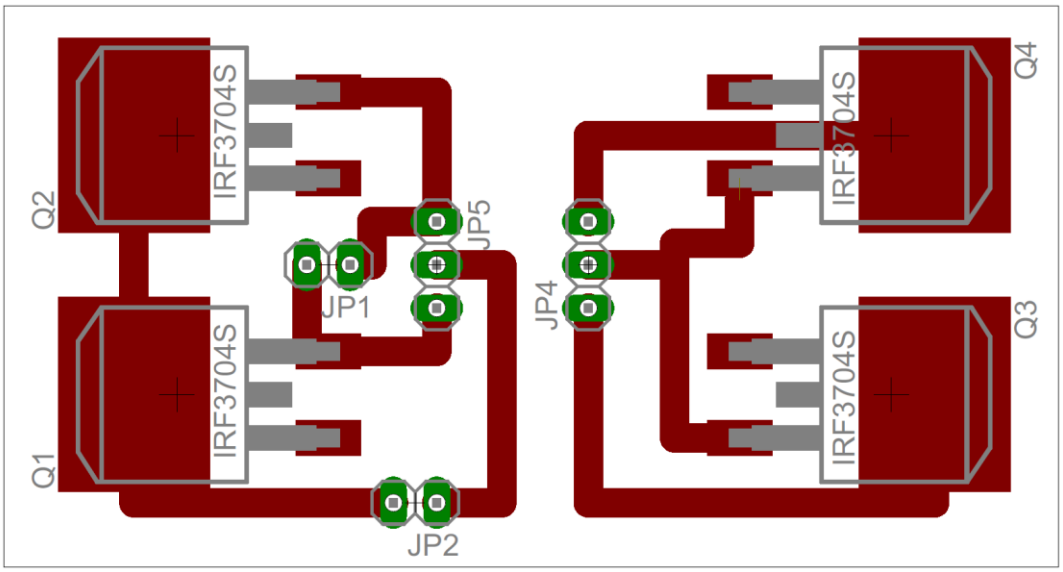



**Figure 4-12 PCB 3 (3 Dimensional Layout) artwork**

The above artwork was developed using EAGLE CAD.

### 4.5.7 PCB4 – Physically Balanced Layout

Figure 4-13 represents the artwork for the improved Geometrically Balanced Layout as depicted in section 3.5.2.4.

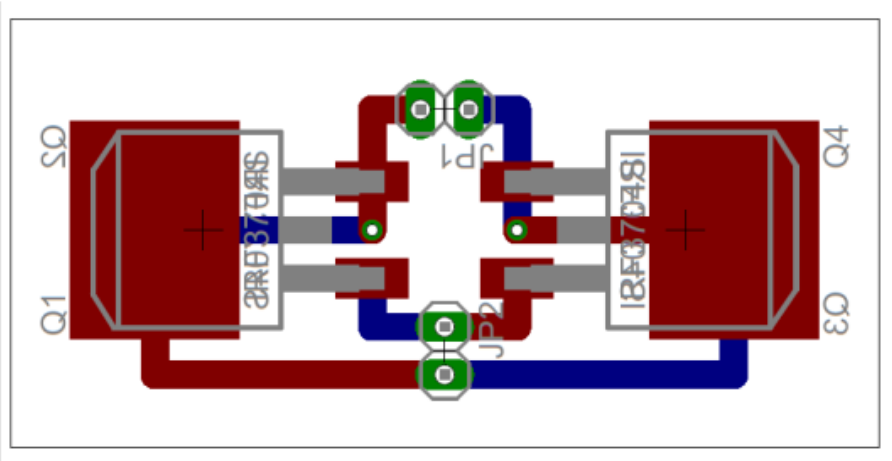



**Figure 4-13 PCB 4 Geometrically Balanced PCB artwork**

As can be seen in Figure 4-13 the circuit is geometrically symmetrical about a vertical mirror line. Both the Component and Copper planes are void of copper pours.

MOSFET's Q1 and Q2 form a phase arm, which are positioned back-to-back and similarly Q3 and Q4 are in the same arrangement. The arrangement of the switches in such a manner allows the circuit to become geometrically and physically symmetrical.

The implementation of the artwork in Figure 4-13 is illustrated in a photograph in Figure 4-21 and Figure 4-22.

## 4.6 IMPLEMENTATION (REALISATION)

The following section documents the prototypes of the schematics within Section 4.5 into populated PCB's

### *4.6.1 MOSFET Driver Boards*

#### *4.6.1.1 Optically Isolated MOSFET Driver Boards*

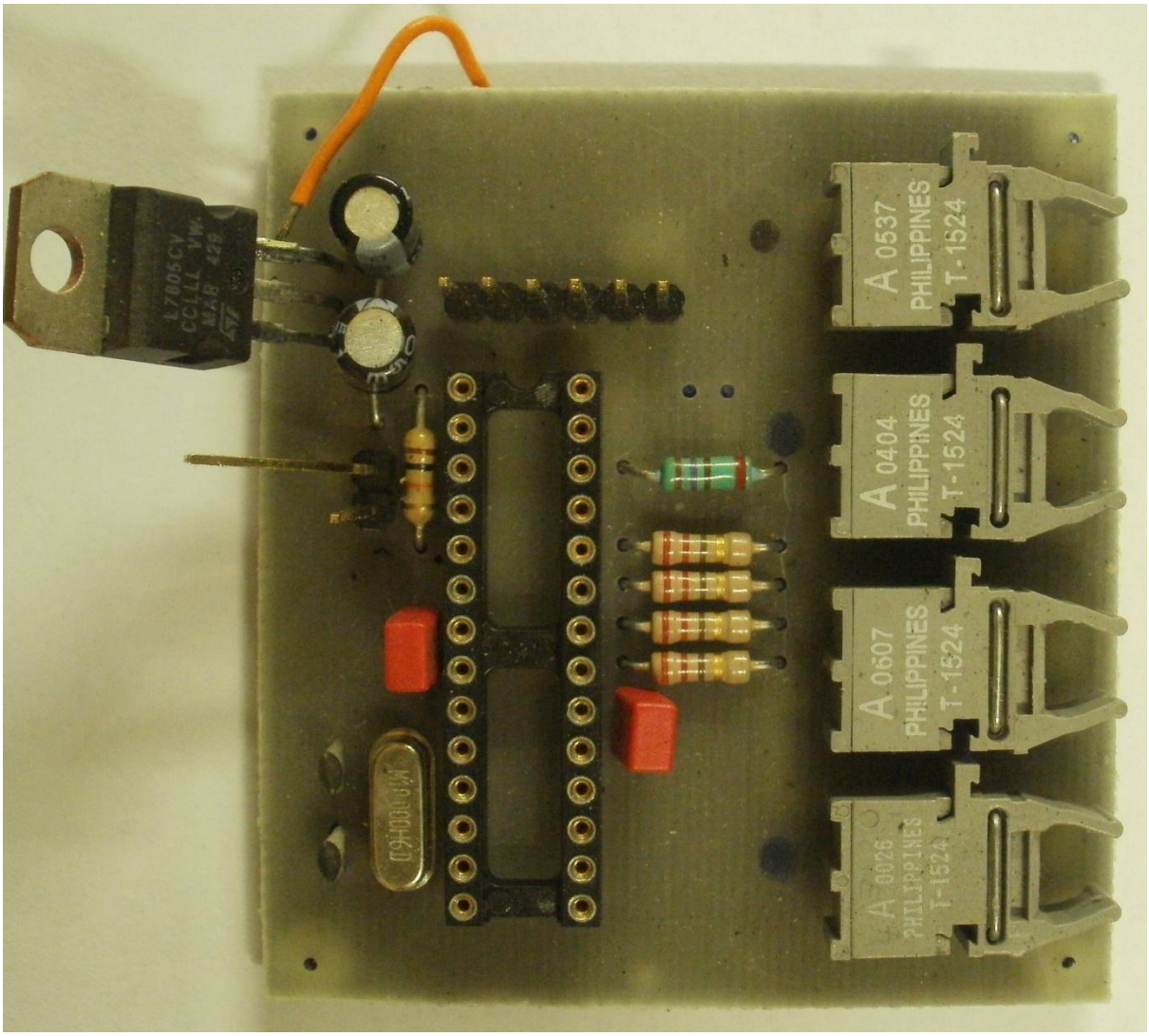



**Figure 4-14 Optical Signal PCB**

Figure 4-14 shows the implementation of the Optical Signal board and Figure 4-15 that of the TLP250 Driver PCB. Both were constructed using a Photolithography process as the artwork was developed in KICAD which was not compatible with the CNC software. The through-holes were drilled by hand using a Dremmel. Population and soldering were done by hand.

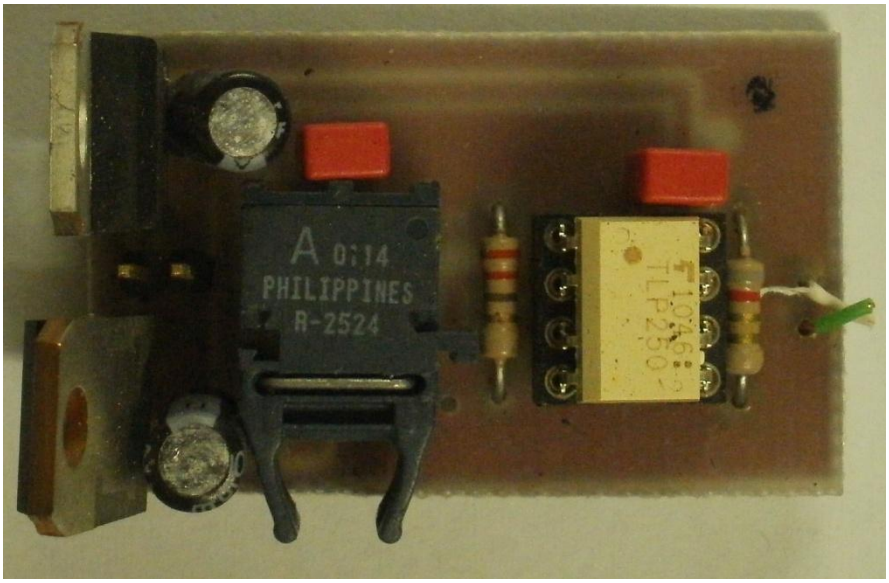



**Figure 4-15 TLP250 Driver PCB**

### *4.6.1.2 Non-Isolated MOSFET Driver Board*

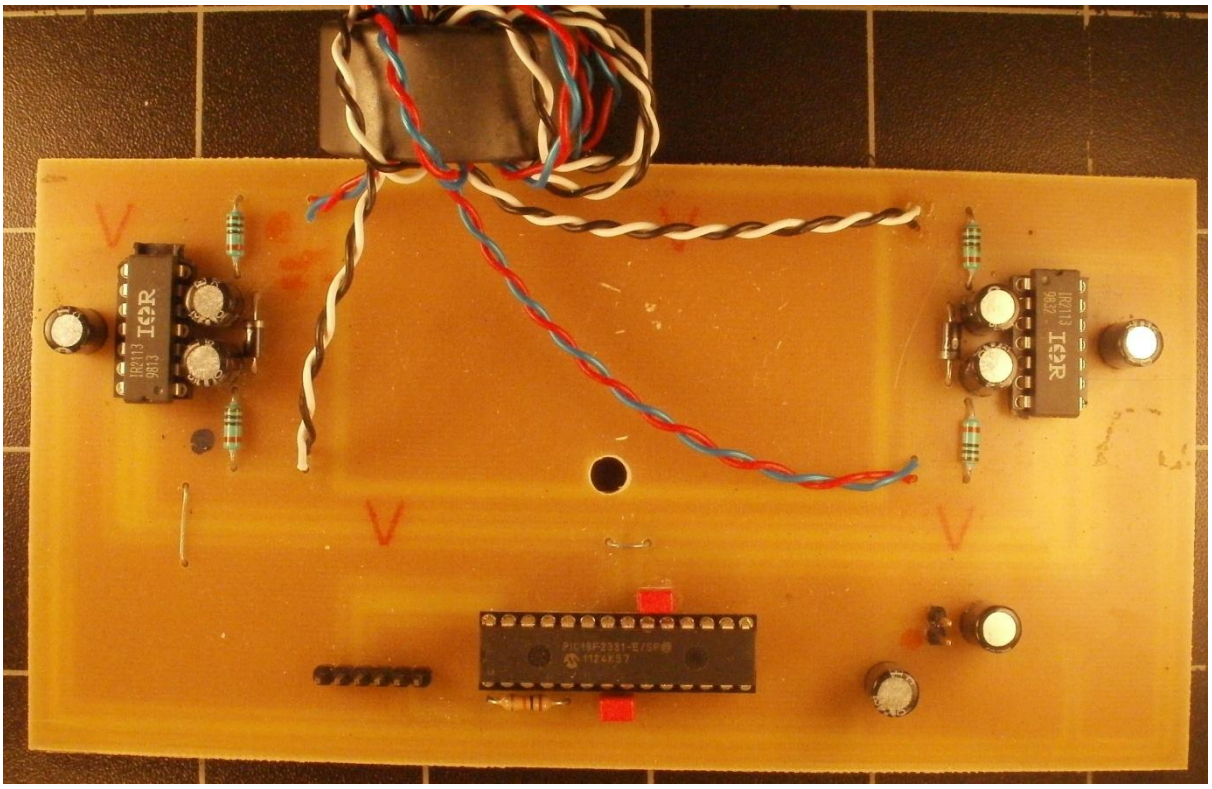



**Figure 4-16 IR2113 MOSFET Driver PCB**

Figure 4-16 shows the implementation of the IR2113 Driver board. The board was constructed from single sided blank PCB and due to the artwork developed within EAGLE CAD and the use of PCB-GCODE, the PCB was milled and corresponding through-holes drilled by a CNC machine. The component population and soldering was done by hand.

The corresponding driving leads (twisted-pairs) are evident within Figure 4-16, including a Common Mode choke to help prevent any EMI contamination from the MOSFET driver circuitry into the DUT's.

### *4.6.2 Devices Under Test*

Figure 4-18 through Figure 4-22 shows the implementation of the DUT prototypes (Circuit 1 through 4). As the artwork was developed within EAGLE CAD (similarly to the IR2113 Driver board), through PCB-G-CODE the PCB's were manufactured on the CNC machine through milling and drilling.

All DUT's were hand populated and soldered.

#### *4.6.2.1 PCB 1*

Figure 4-17 illustrates the Baseline PCB constructed on Veroboard. As is visible within the figure, no particular regard to layout or MOSFET positioning was considered.

The MOSFETS used were IRF540N through hole components.

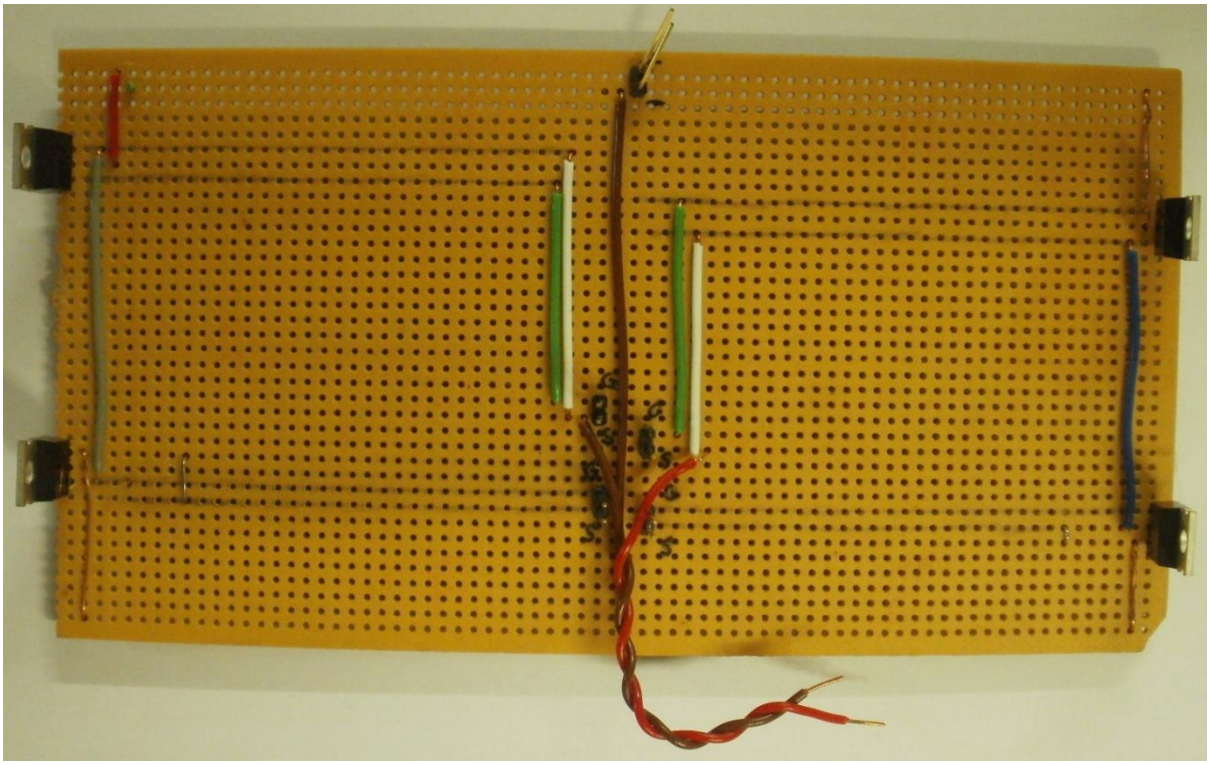


**Figure 4-17 Device Under Test 1 Veroboard (Baseline)**

### *4.6.2.2 PCB 2*

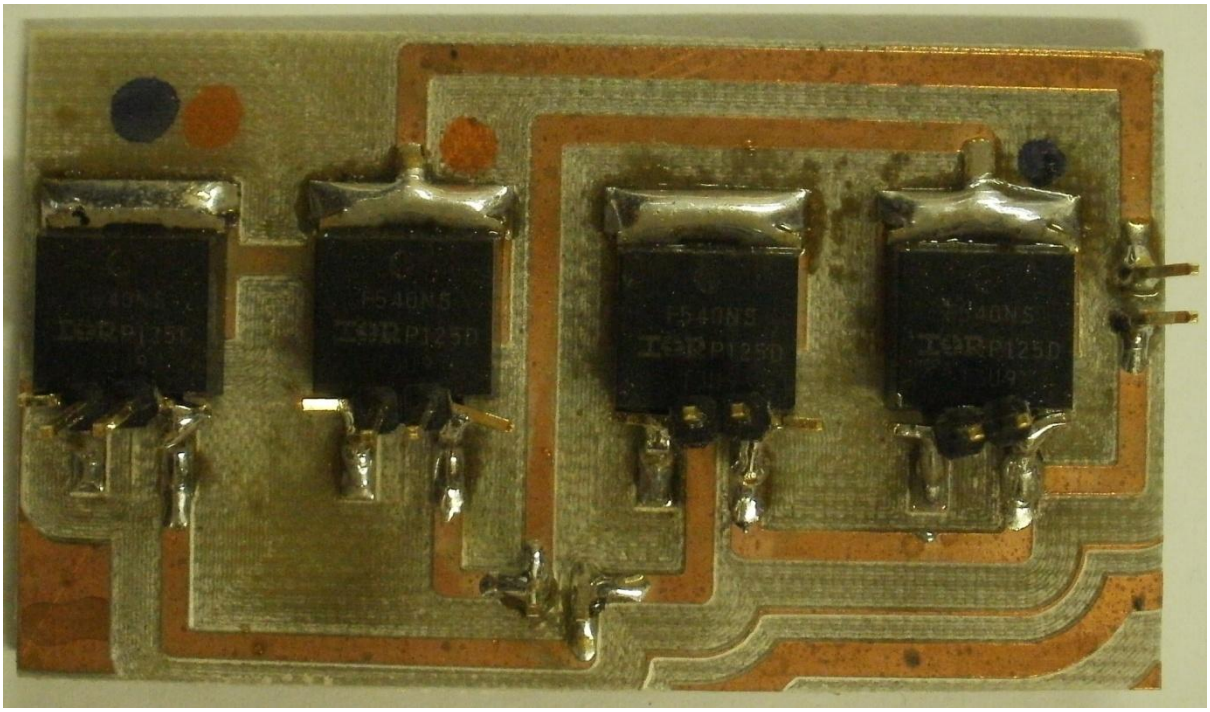


**Figure 4-18 Device Under Test 2 PCB (Second Baseline)**

Figure 4-18 illustrates the completed Second Baseline (PCB 2) PCB. The MOSFET's used were IRF540N MOSFETS. Visible are the header pins used to interface the gate drive signals to the MOSFETs including supply and load interfaces.

### *4.6.2.3 PCB 3*

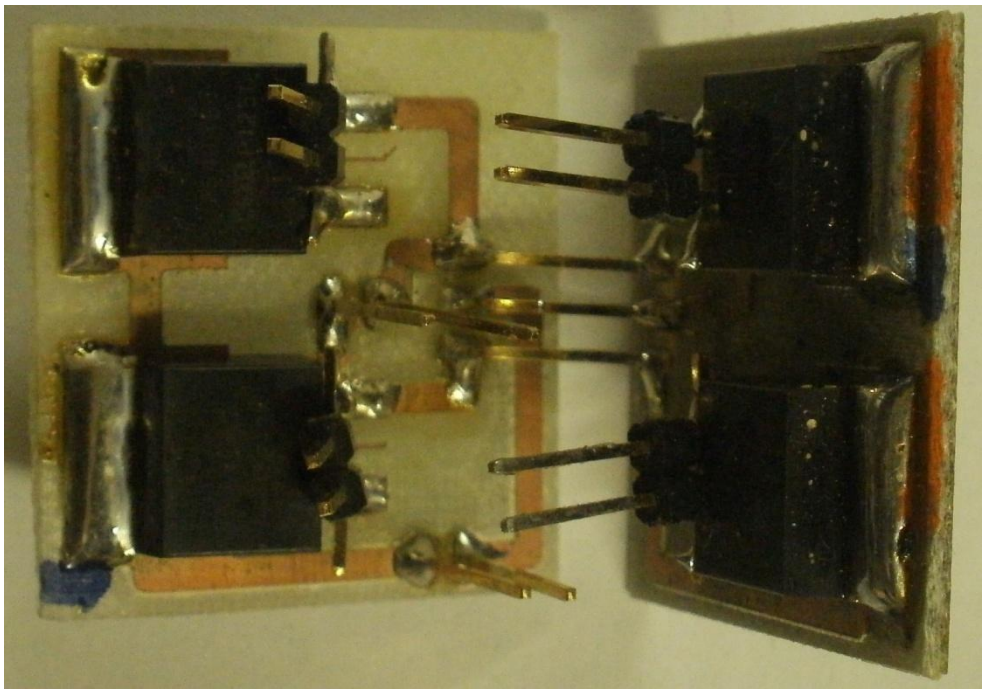


**Figure 4-19 Device Under Test 3 PCB (3 Dimensional)**

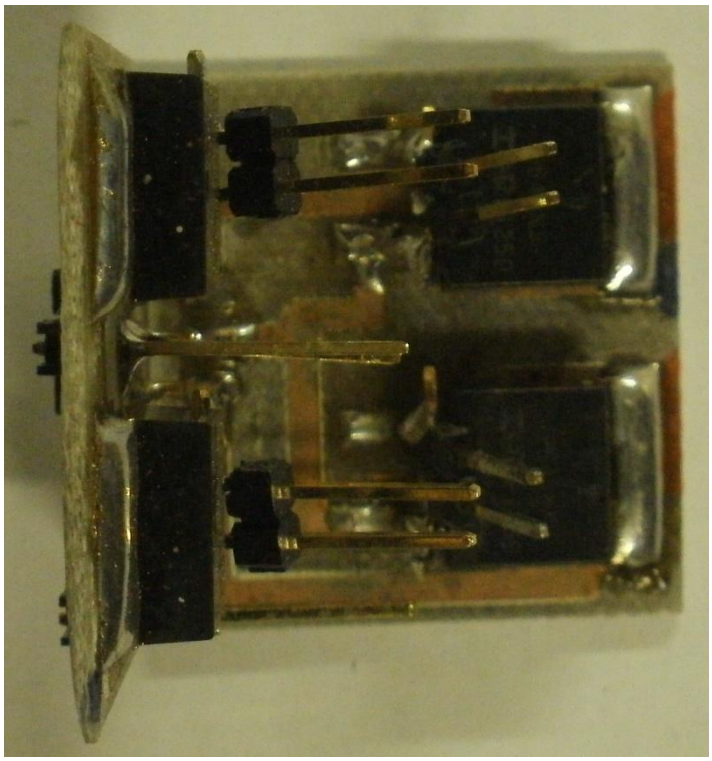


**Figure 4-20 Device Under Test 3 PCB (3 Dimensional – Alternate View)**

Figure 4-19 and Figure 4-20 illustrate the implementation of the 3-Dimensional DUT, showing the perpendicular construction of the DUT with the interfacing header pins. As with the baseline DUT, IRF540N MOSFET's were used.

#### *4.6.2.4 PCB 4*

Figure 4-21 and Figure 4-22 illustrate the implementation of the Geometrically Symmetrical DUT.

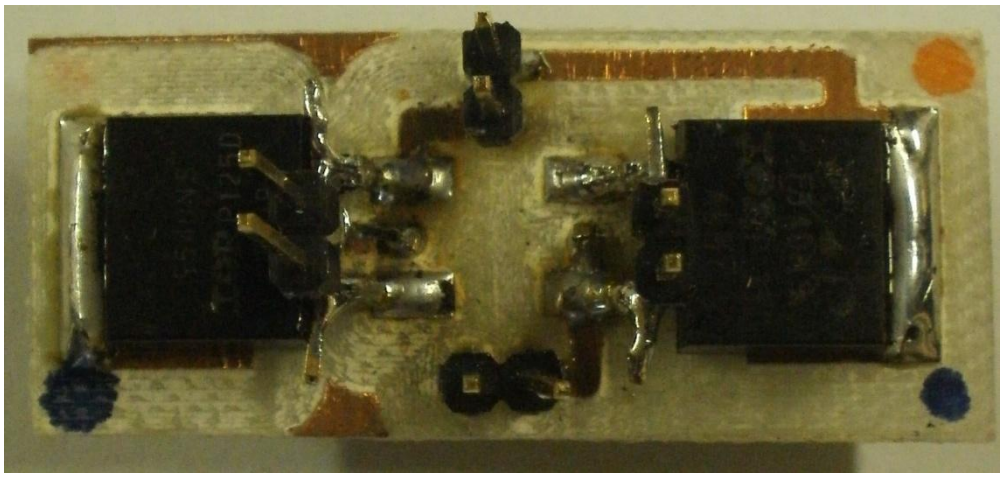


**Figure 4-21 Top view of Device Under Test 4 PCB (Geometrically Symmetrical)**

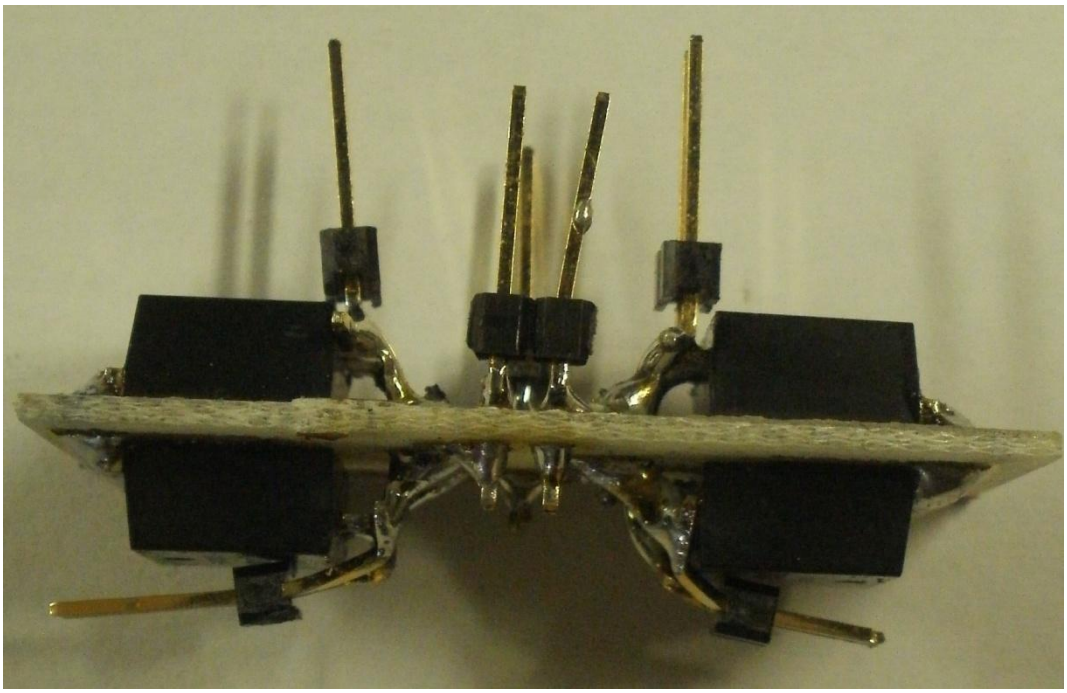


**Figure 4-22 Side view of Device Under Test 4 PCB (Geometrically Symmetrical – Rotated View)**

Similar to the Geometrically Symmetrical DUT, the gate drive signal interfacing was implemented through header pins, including the supply and load interfaces. IRF540N MOSFET's were again used.

The coloured dots seen within the figures were used as identification markers as the board is symmetrical and also used to maintain orientation and repeatability.

An important factor to realise is that during the implementation of a Geometrically Symmetrical converter, it may be impossible to achieve perfect Geometric Symmetry due to the physical construction of the semiconductor devices. The semiconductor devices are typically not symmetrical in their construction and packaging, hence limit the ability to design and construct a perfectly Geometrical Symmetrical layout and circuit. However the implementation presented for a Geometrically Symmetrical circuit with standard package semiconductor devices achieves an adequately symmetrical layout.

## 4.7 CONCLUSION

Chapter 4 presents the design and implementation of the four required prototype H-bridge circuits as stipulated within Chapter 3 to demonstrate differing EMI mitigating techniques. The rationale behind the development of a MOSFET Driver board and the separation of the MOSFET Drivers from the H-Bridge circuit has been discussed. Differing MOSFET Driver setups were developed upon which the solution using the IR2113 MOSFET Drivers were chosen due to their robustness and ease of use. The rationale behind reducing the entire circuit to a H-Bridge only has been presented. The schematics and PCB artwork of each board including the MOSFET Driver board have been illustrated, the physical implementations of which are also illustrated.

# 5 EXPERIMENTAL SETUP

## 5.1 INTRODUCTION

The following section firstly entails the equipment and appropriate setup structure used within the experimental setup and secondly the tests performed and the details of each individual test required.

The experiments outlined in section 5.3 aim to test the effect that physical layout of the PCB's implemented in section 4.6.2 have on both CM and DM EMI measurements. In addition to investigating the physical layout properties only, other test variables are introduced as to gain further insight into the workings of CM and DM EMI and to develop a baseline.

Each individual test was developed to isolate a specific factor and hence multiple tests were developed and executed.

The first experiment outlines the DM EMI from the DUT's with zero load and zero elevation from the copper plane of the test setup.

Similarly the second experiment is to obtain the CM EMI of each DUT with zero load and zero elevation.

The third and fourth experiments are to obtain DM and CM EMI results for the DUT's with varying load present but with zero elevation from the copper plane.

The fifth and sixth are to obtain DM and CM EMI results with zero load but with a specified elevation from the copper plane.

The last experiments, seventh and eighth, are to obtain DM and CM results for the DUT's when there is a specified elevation and a specified load as stipulated within the experimental section.

The results and the analysis of the each experiment and the analysis of the obtained results can be found within section 6.

## 5.2 EQUIPMENT SETUP

The equipment setup section covers the equipment used and the appropriate connections of the equipment to obtain the results.

A basic overview of the experimental setup is illustrated in Figure 5-7.

### 5.2.1 Equipment

#### 5.2.1.1 Linear DC Power Supplies

Linear DC Power supplies capable of outputting 12V DC were required. Linear supplies were used over Switch-mode Power Supplies (SMPS) as they exhibit substantially lower EMI output levels.

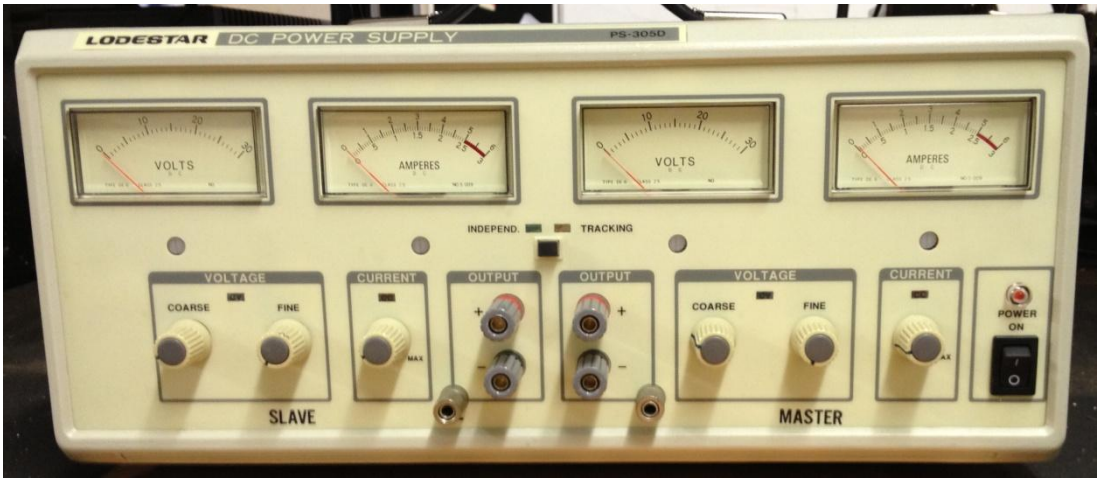



**Figure 5-1 Linear DC Power Supply**

#### 5.2.1.2 EMI Filter

An EMI filter was implemented between the DC supply and the LISN as to mitigate any EMI emanating from the supply should there be any emanation.


**Figure 5-2 EMI Filter**

### 5.2.1.3 Chokes

CM chokes were used within the experimental setup to help avoid any EMI from entering the DUT's as to avoid EMI contamination from other sources.

### 5.2.1.4 LISN

A Line Impedance Stabilisation Network as discussed in section 2.4.2.1 is required to provide a standardised noise impedance for the DUT's as to quantify and compare the EMI generated. Appendix C contains further details on the LISN used.

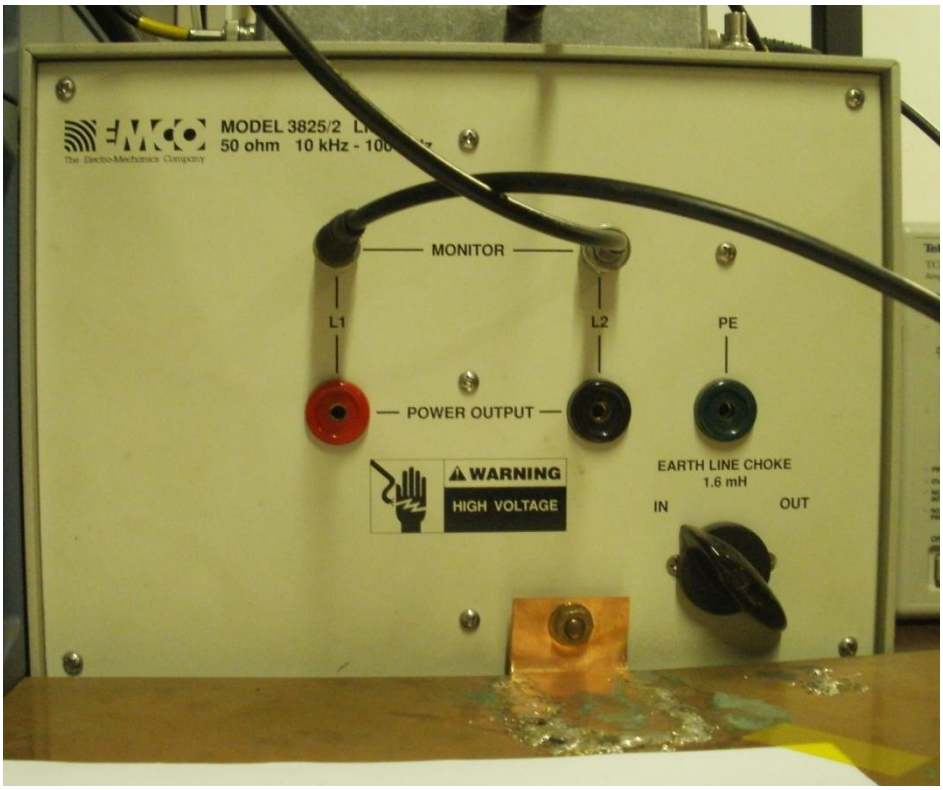



**Figure 5-3 Line Impedance Stabilisation Network (LISN)**

### 5.2.1.5 Ground Plane (Copper Plane)

A flat copper section used as a coupling plane and return path for the EMI between the DUT and the LISN. The Copper plane is connected to the Earth terminal on the front of the LISN. A copper plane was used as to fulfil the requirements of the CISPR test for conducted EMI. The copper plane can be seen to be connected to the LISN in Figure 5-3.

### 5.2.1.6 CM + DM Splitter

A device which connects to both monitor ports of the LISN and the output connected to either an oscilloscope or spectrum analyser. The CM + DM splitter through selection switches takes the combination of CM + DM EMI and splits them into either CM or DM as desired.

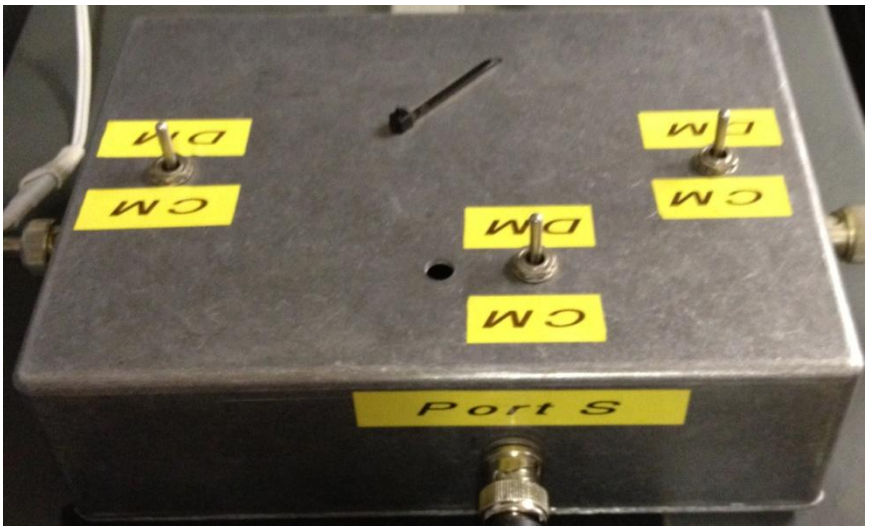



**Figure 5-4 CM + DM Splitter**

### *5.2.1.7 Spectrum Analyser*

The spectrum analyser was used to measure the EMI generated by the DUT's. The spectrum analyser used was a Rohde & Schwarz FSH3 of which details can be found in Appendix C. The spectrum analyser is capable of measuring from a frequency of 100 kHz and hence 100 kHz was set as the start frequency. The stop frequency was set to 60 MHz as to capture the 150 kHz to 30 MHz requirement of the conducted EMI spectrum. A window of 10 kHz was used.

The output of the CM + DM splitter was connected to the spectrum analyser.

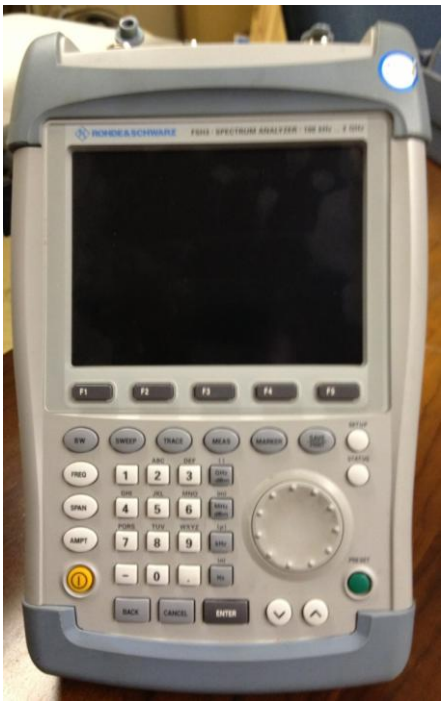


**Figure 5-5 Spectrum Analyser**

#### 5.2.1.8 Oscilloscope

A Tektronix Oscilloscope was used to do measurements in the time domain. The oscilloscope was only used for debug, verification and faultfinding purposes rather than capturing results.

#### 5.2.1.9 EMI Current Probe

An EMI Current Probe capable of measuring in the *dBμA* range was used to measure and verify the workings of the CM + DM splitter.

#### 5.2.1.10 Load

A set of wire-wound resistors mounted on a heat-sink with sufficient cable to place the load an appreciable distance from the test setup. The combination of 3.3Ω and 8Ω resistors were used.

### 5.2.2 Equipment Setup Overview

Figure 5-6 below illustrates the experimental setup and Figure 5-7 the experimental overview illustrating connections between equipment so as to achieve the experimental setup.

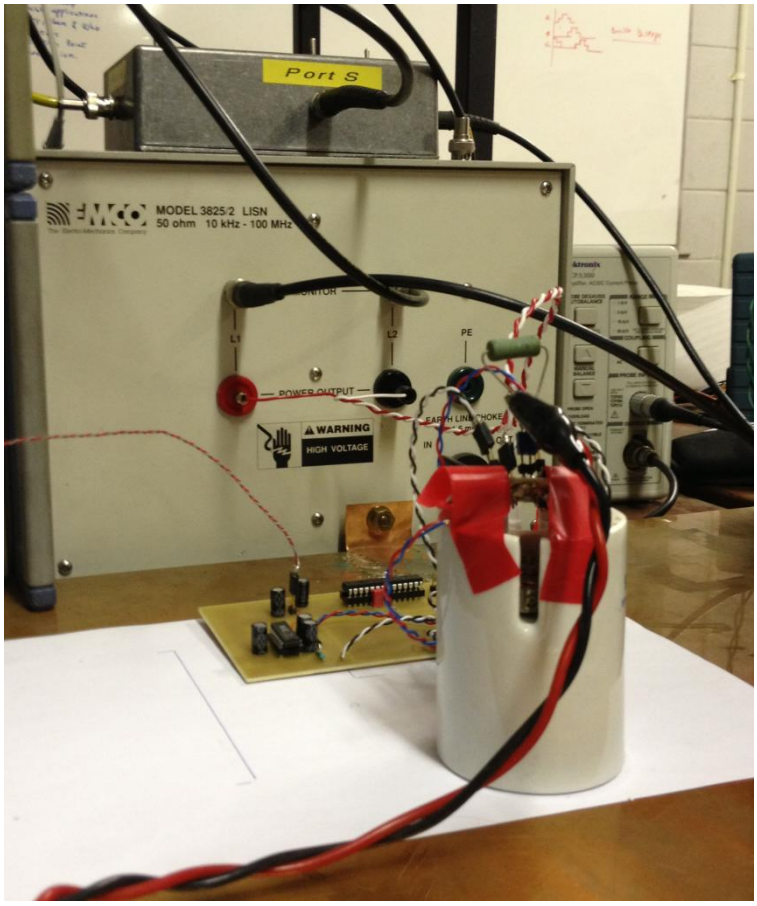



**Figure 5-6 Experimental Setup**

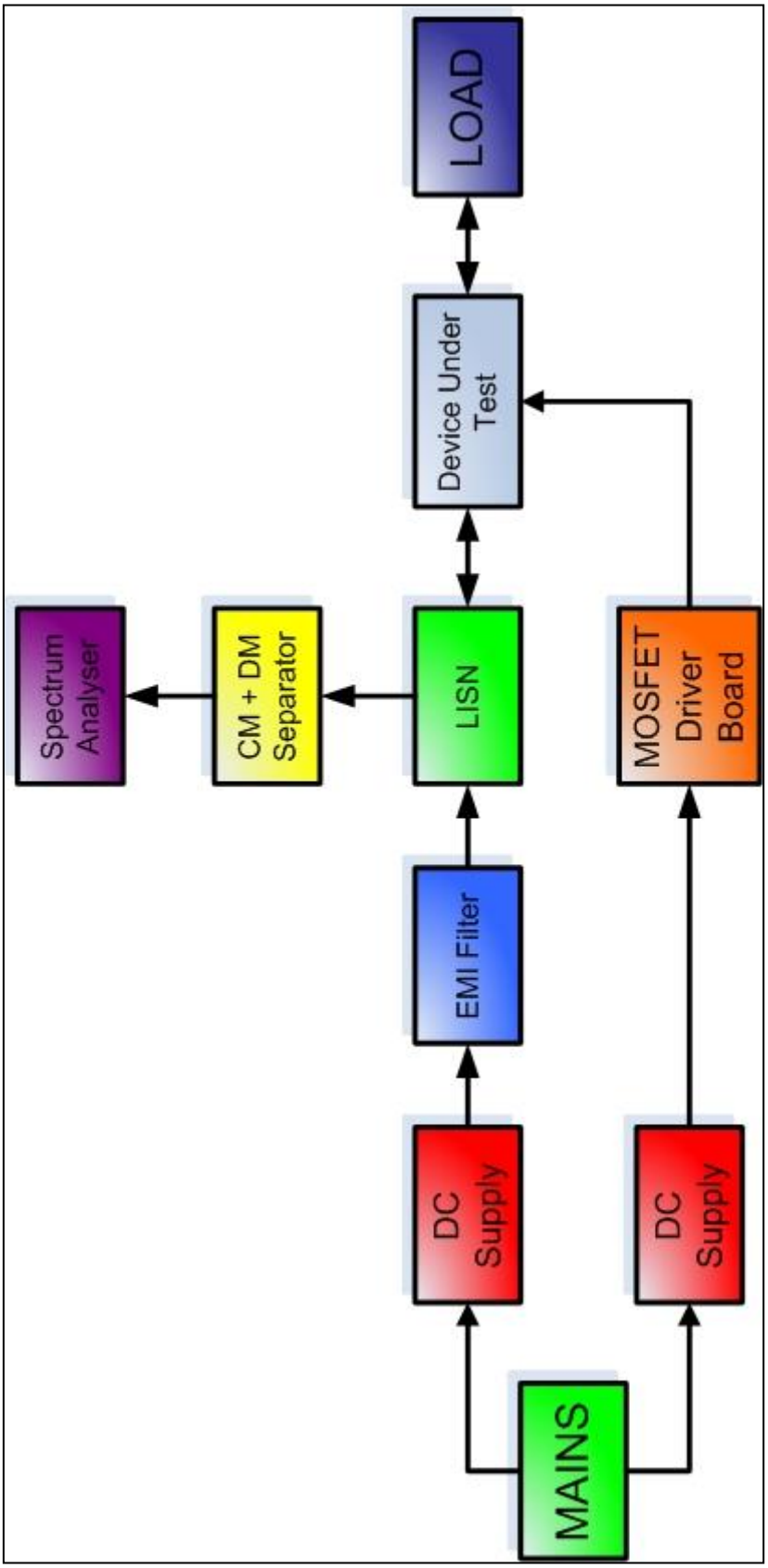



**Figure 5-7 Experiment Overview**

## 5.3 EXPERIMENTAL OVERVIEW

The following section outlines the tests carried out in order to determine the amount of EMI generated by the DUT's. Each test is performed on all the DUT's and changes a single variable only in order to evaluate the performance of each DUT with respect to the changed variable.

As per the General Design Specifications in section 4.2, the following specification apply:

- $V_{IN}$ = 12V
- $I_{MAX}$ = 5A
- $V_{OUT}$ = 12V
- $f$ = 20kHz
- $P_{MAX}$ = 60W

Suitable load resistors to adjust output power were chosen as 8Ω and 3.3Ω, which would yield 18W and 43.6W of output power respectively with $V_{IN}$=12V.

### *5.3.1 Test 1: No Load with Zero Elevation, DM Measurement*

- No Load Connected
- Vertical Elevation: 0mm
- CM +DM Splitter Mode: DM

### *5.3.2 Test 2: No Load with Zero Elevation, CM Measurement*

- No Load Connected
- Vertical Elevation: 0mm
- CM +DM Splitter Mode: CM

### *5.3.3 Test 3: Loaded with Zero Elevation, DM Measurement*

- 8Ω, 3.3Ω Connected
- Vertical Elevation: 0mm
- CM +DM Splitter Mode: DM

### *5.3.4 Test 4: Loaded with Zero Elevation, CM Measurement*

- 8Ω, 3.3Ω Connected
- Vertical Elevation: 0mm
- CM +DM Splitter Mode: CM

### *5.3.5 Test 5: No Load with Elevation, DM Measurement*

- No Load Connected
- Vertical Elevation: 200mm
- CM +DM Splitter Mode: DM

### *5.3.6 Test 6: No Load with Elevation, CM Measurement*

- No Load Connected
- Vertical Elevation: 200mm
- CM +DM Splitter Mode: CM

### *5.3.7 Test 7: Loaded with Elevation, DM Measurement*

- 8Ω, 3.3Ω Connected
- Vertical Elevation: 200mm
- CM +DM Splitter Mode: DM

### *5.3.8 Test 8: Loaded with Elevation, CM Measurement*

- 8Ω, 3.3Ω Connected
- Vertical Elevation: 200mm
- CM +DM Splitter Mode: CM

## 5.4 CONCLUSION

The relevant equipment and the setup thereof has been discussed in order to provide an experimental setup such as to obtain EMI results and provide insight into the relative performance of the different boards to be tested in Chapter 4. The appropriate tests including the stipulated voltage and power levels have been presented. The results of the tests carried out within Chapter 5 are presented within Chapter 6.

# 6 RESULTS AND ANALYSIS

The results presented in this chapter were obtained by performing the experiments outlined in 5.3.

The results are not necessarily documented in the order the tests were conducted as to provide a comparison between individual DUT performance results and comparative DUT's performance results. Each DUT's results are presented and compared individually before comparative analysis between all the DUT boards are presented.

When comparing the results within the following section, note should be taken to the measurement scale and the significance thereof. A difference of 3dB on the logarithmic scale is significant due to a 3dB difference equating to either halving or doubling the measured power as a 3dB decrease or 3dB increase respectively.

Within the results section, the effects of changing height above the ground-plane and the resulting change in parasitic components should be visible as a decrease in spectral content of the CM EMI results throughout section 6. Other phenomena observable include the DM to CM conversion where a large amount of DM or a change in the DM spectrum should be present or prevalent in the CM spectrum for individual results. Additionally, the large layout or changes in circuit layout should present significantly differing EMI results.

EMI measurements are notoriously difficult [3] [17] with a multitude of external unintentional variables affecting the measured results. Any measurement made in conjunction with the EMI measurements, (switching waveforms) causes the EMI measurements to be grossly incorrect as the introduction of other measuring equipment often provides an alternative pathway for the EMI to couple through, often providing incorrect or inconsistent measurements. In the case of the addition of a differential voltage probe (connected to the oscilloscope) to measure the switching waveform to verify proper converter operation, differing power levels resulted in no change to the EMI spectrum, indicating the differential voltage probe influenced the measurement setup significantly. Therefore a consistent measurement setup with only the essential equipment and measuring tools connected and within the vicinity of the measurements should be adhered to in order to achieve meaningful EMI measurement results.

Within section 6, when referring to the circuit or Device Under Test (DUT), the term *flat* indicates the DUT is placed directly on the ground-plane with zero elevation (but insulated from the copper plane). When the term *elevated* is used, it refers to the DUT being raised by 200mm. When the DUT is referred to as being *unloaded*, it indicates zero impedance is connected to the output of the converter or DUT. When referred to as *loaded*, it implies either of the specified impedances in section 5.3 are connected to the output of the DUT.

## 6.1 PCB1 (VEROBOARD) RESULTS

Section 6.1 covers the results and discussion thereof solely of the first device under test, (PCB1). The section covers comparative DM and CM results including loaded and unloaded.

### *6.1.1 DM Results*

In Figure 6-1 the Differential Mode results are presented whereby the DUT is firmly mounted to the copper plane with a varying load connected.

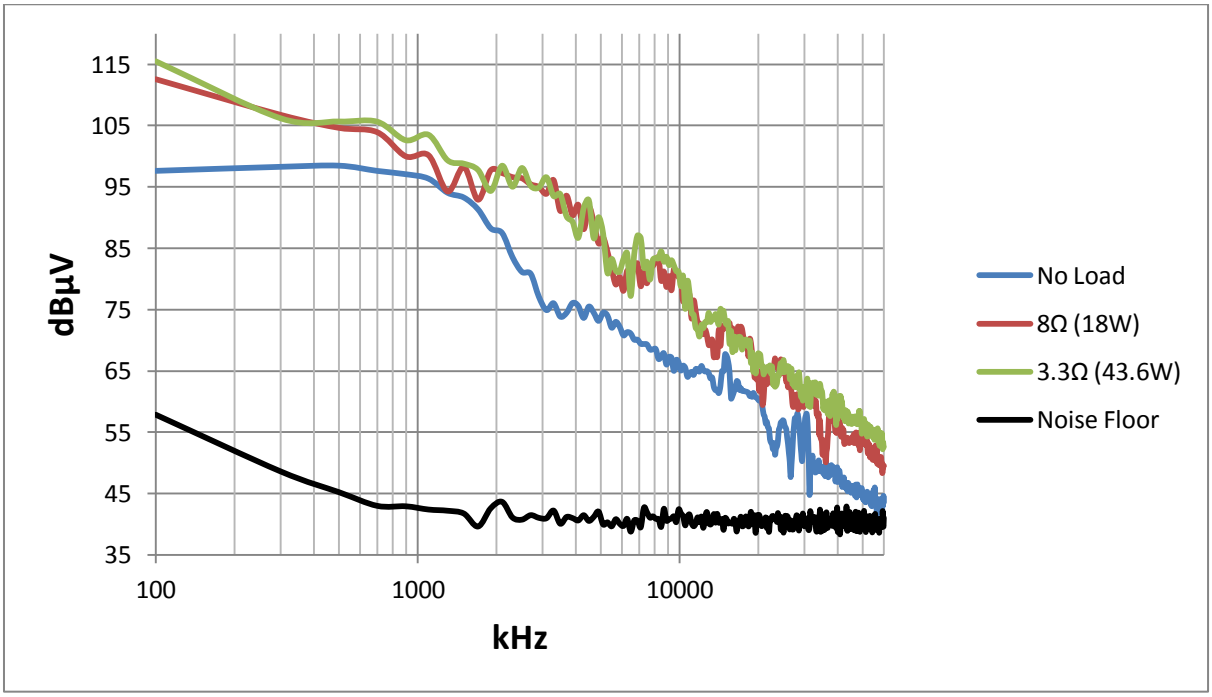



**Figure 6-1 PCB1 Zero Elevation DM Results**

In Figure 6-1, the black trace represents the Noise Floor, and the blue trace the no-load result. During the no-load result, the DUT and MOSFET Driver board are functional but absent of impedance on the output of the converter and hence zero power transfer through the DUT.

The red trace represents a 18W load and the green trace a 43.6W load. The higher load is more than double the lesser load as to investigate whether a significant increase in EMI will be evident from higher power levels.

Evident from the no-load (blue) trace in Figure 6-1 there is an appreciable amount of DM EMI present even in the absence of output impedance on the converter. The nett power transfer is zero with output impedance absent. By definition, the converter operating current is responsible for the generation of DM EMI, however the current drawn from the supply is zero due to lack of output impedance implying other mechanisms or pathways for DM EMI to propagate do exist.

The appreciable amount of DM EMI present under the no-load conditions presents a situation whereby the sole operation of MOSFET driving in absence of power transfer

through a converter gives rise to a significant amount of DM EMI, whereby in theory under no-load conditions DM EMI should not be present or should be insignificant.

The mechanism by which DM EMI is generated by MOSFET Driver operation and MOSFET switching solely is left for discussion in section 6.7.

From Figure 6-1, when operating under loaded conditions there is an increase in DM EMI present over the no-load and Noise Floor which is to be expected: during converter operation switching action of voltage occurs due to the operating function of the converter hence causing current to flow. The resulting current flow generates DM EMI. The difference in DM EMI between the varied power outputs is insignificant implying a doubling of the output power has almost no impact on DM EMI noise generated in the presented case. A marginal increase of DM EMI however is to be expected as an increase in power translates to an increased current magnitude for the same voltage, whereby an increased current magnitude for the same switching frequency generates greater DM EMI. [4]

Figure 6-2 presents the results for the first DUT (VeroBoard) as in the case of Figure 6-1 with the difference being the DUT elevated by 200mm from the ground-plane firmly mounted in place on an isolating piece of material (ceramic). The XY location remained unchanged.

As in Figure 6-1, the no-load DM EMI is significant and remains practically identical up to a frequency of about 10 MHz. From 10 MHz to 60 MHz a slight variation is present.

The waveforms representing the loaded results (red and green trace) in Figure 6-2 are very similar in intensity to the waveforms in Figure 6-1. No major changes in intensity are expected as the currents drawn should be similar as the change in height above the copper ground-plane has little to no effect on the DM circuit of the converter with reference to coupling and parasitic components. However a shift in the waveform between the red and green trace in Figure 6-2 is present. With the change in height of the DUT, a change in the relative position of the cables within the setup inevitably changes which is unavoidable. The change in cable positioning in three-dimensional space results in a physical change in the circuit setup which may lead to a change in other factors such as mutual inductance and other coupling mechanisms (capacitive and inductive). A change in height between cables and a ground-plane results in a change in mutual inductance [14] [18] [19] and hence may affect the total circuit, which may lead to a change in a resonant point within the circuit.

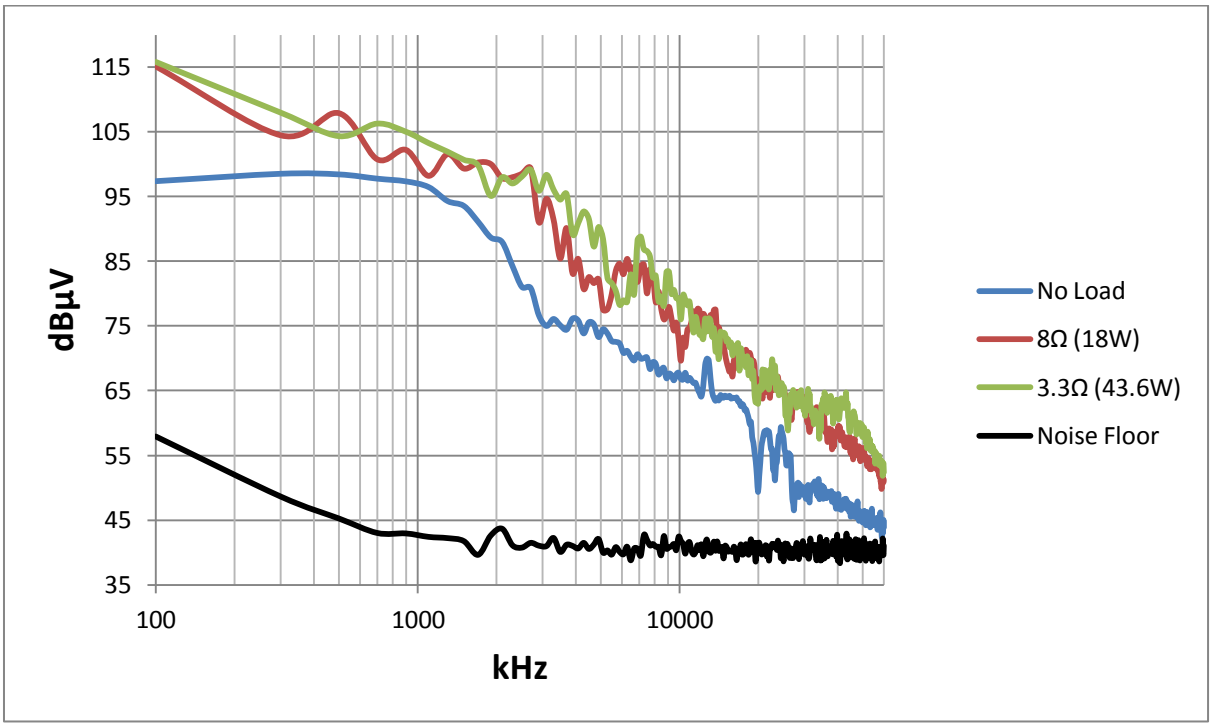



**Figure 6-2 PCB1 200mm Elevation DM Results**

Hence increasing the height of the DUT above a coupling (ground) plane has little impact on the magnitude of DM EMI. However a shift towards the right of the spectrum but may necessarily facilitate in keeping within EMI specifications, resulting from a change in coupling.

### *6.1.2 CM Results*

The PCB 1 CM EMI results for the Flat (non-elevated) and Elevated (200mm elevation) cases are presented in Figure 6-3 and Figure 6-4 respectively.

Due to there being a significant portion of DM EMI present under all load conditions for the DM results for Board 1 as in Figure 6-1 and Figure 6-2, there is the expectation for CM EMI to be present at significant levels even under the no-load case due to converter operation. The conversion of DM EMI to CM EMI should be present and the effects of height above the ground-plane should produce differing results as one of the major methods of CM EMI generation mechanism is capacitive coupling. The elevation above the ground-plane with reference to circuit CM EMI levels should also be indicative within the following results.

For the no-load instances, both Figure 6-3 and Figure 6-4 present a relatively lower level of CM EMI in comparison to the DM EMI situation but surprisingly elevation has little effect other than a shift in the spectrum and a decrease in the case of the elevated result below 300 kHz.

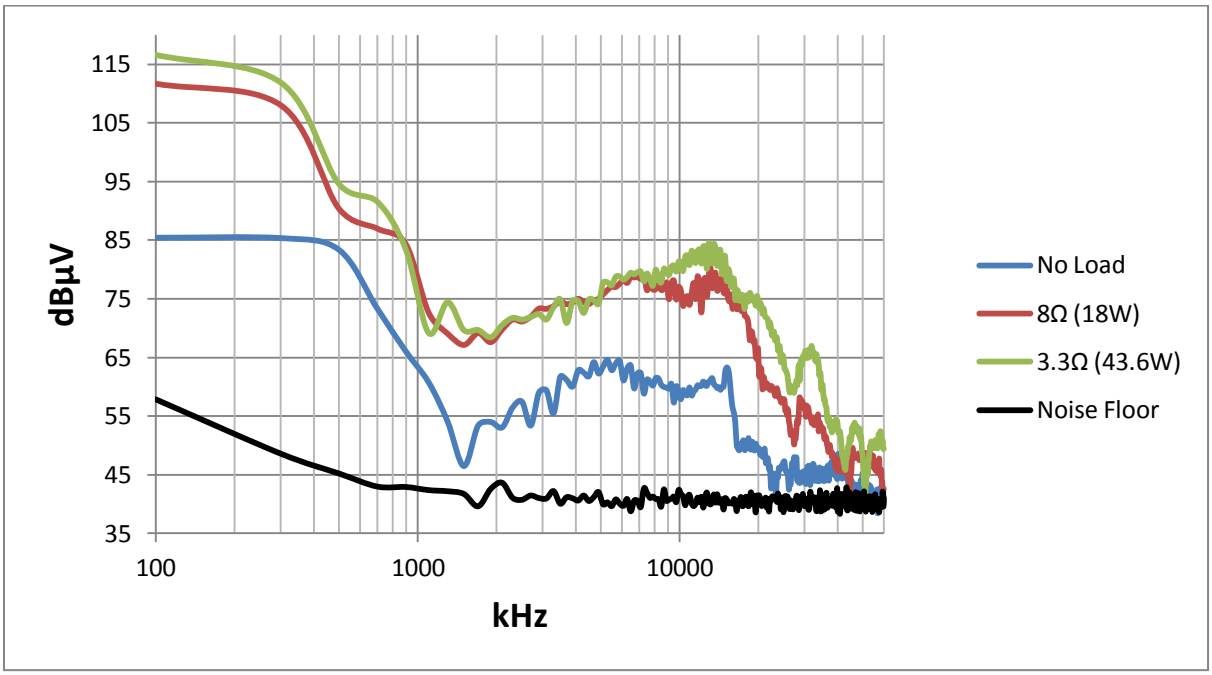



**Figure 6-3 PCB1 Zero Elevation CM Results**

For the instance of the 18W load (red trace) in Figure 6-3 and Figure 6-4, there is once again very little appreciable difference between the elevated and non-elevated CM EMI results other than a slight reduction in the elevated case which is expected due to a reduction in capacitive coupling due to elevation above the ground-plane. A slightly higher result between the 43.6W and 18W load is present which is to be expected as the higher power levels generate larger amounts of DM EMI which in turn results in larger CM EMI through conversion [1] [2] [4] as discussed in section 3.

However there is a major difference between the 18W and 43.6W load levels (red and green trace respectively) in the elevated setup. In addition there is also a significant difference between the 43.6W load (green trace) results for the elevated (Figure 6-4) and non-elevated (Figure 6-3) case. The increase of CM EMI in the 43.6W case with the increase in distance from the ground-plane presents a contradictory result as typically an increase in elevation from the ground-plane results in a decrease in CM EMI due to a reduction in capacitive coupling.

From 400 kHz to roughly 10 MHz is where the significant difference in CM EMI magnitude is present. As discussed previously, the change in elevation between the DUT and the ground-plane changes the amount of coupling experienced by the circuit (parallel plate distances related to capacitance). The change is evident as resonance or ringing is present in the outline between 400 kHz to roughly 10 MHz. The presence of such ringing in the 43.6W case indicates a significant change to the circuit operation over the 18W case during elevation.

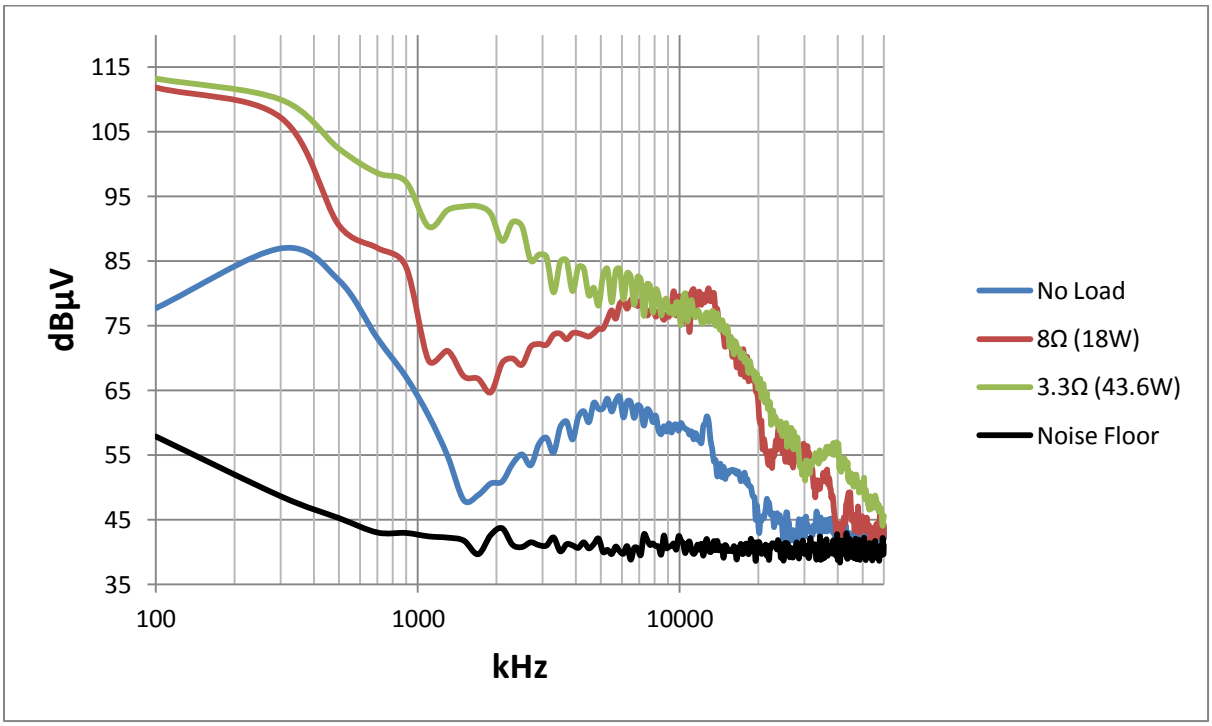



**Figure 6-4 PCB1 200mm Elevation CM Results**

A possible contributing explanation is a change in the coupled inductance (possibly mutual inductance) of a circuit which causes a shift in the spectrum in the DM and often a decrease in DM but in turn causes an increase in CM [4]. The mechanism by which the CM EMI increases is due to the increased transients caused during semiconductor switching and additional inductance present. Additional inductance and the same operational current generate higher transients and these transients (voltage spikes and ringing) find their way through capacitive means to ground. The increased capacitive current hence equates to increased CM EMI.

The increase in inductance as mentioned above does however not explain the substantial increase in CM EMI during the elevated case of the 43.6W load. Other contributing factors such as a change in mutual inductance between the DUT and the ground-plane and the change leading to a resonant point may be the major contributing factor but is however indeterminate and cannot be justified as the definitive resulting factor.

## 6.2 PCB2 (BASELINE) RESULTS

The following section covers the measurements and discussion for the Baseline Board as illustrated in Figure 4-18.

### *6.2.1 DM Results*

Figure 6-5 and Figure 6-6 represent the DM EMI results for the baseline board in the Flat and Elevated (200mm) positions respectively.

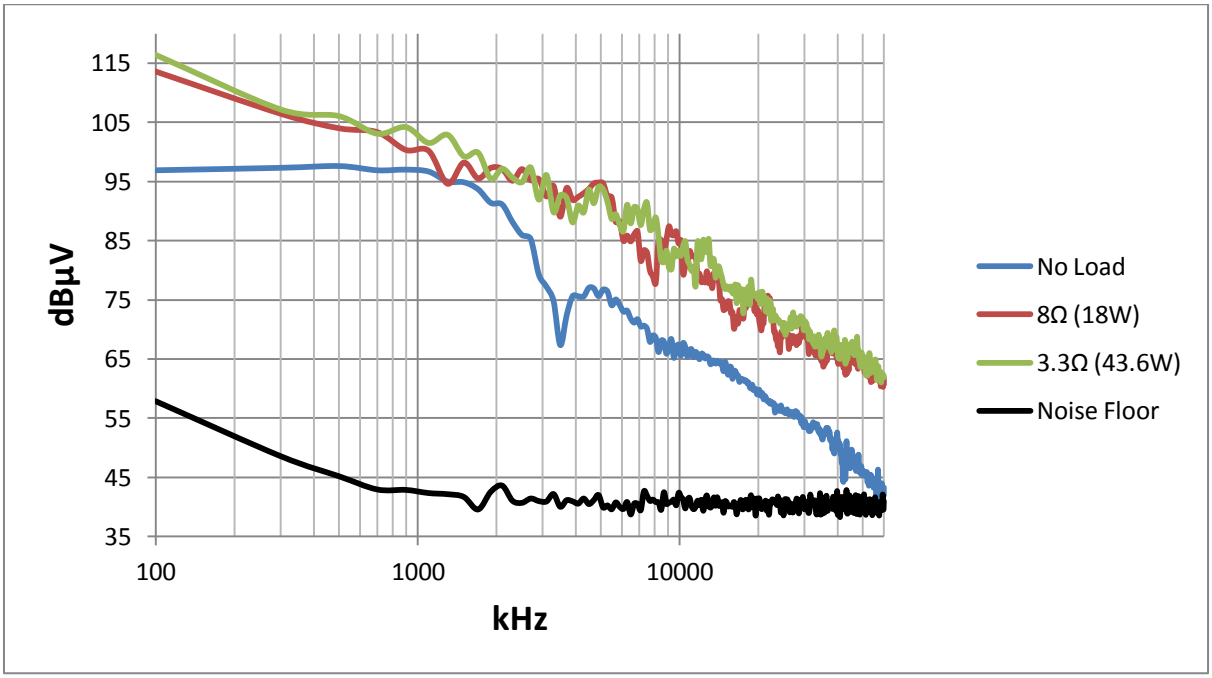



**Figure 6-5 PCB2 Zero Elevation DM Results**

As in 6.1.1, the black trace represents the Noise Floor which remained relatively unchanged throughout the experimentation. The blue trace represents the no-load result, the red and green trace being the 18W and 43.6W case respectively.

Figure 6-5 illustrates as in section 6.1.1 a significant amount of no-load DM EMI, again representing a significant finding in itself due to MOSFET Driver operation as in discussions mentioned earlier. The 18W and 43.6W load spectrums are very similar in nature but worse than for the no-load condition which is to be expected as the converter is in a loaded operational state. The difference between the 18W and 43.6W spectrums with zero elevation are only slight in this DM EMI case.

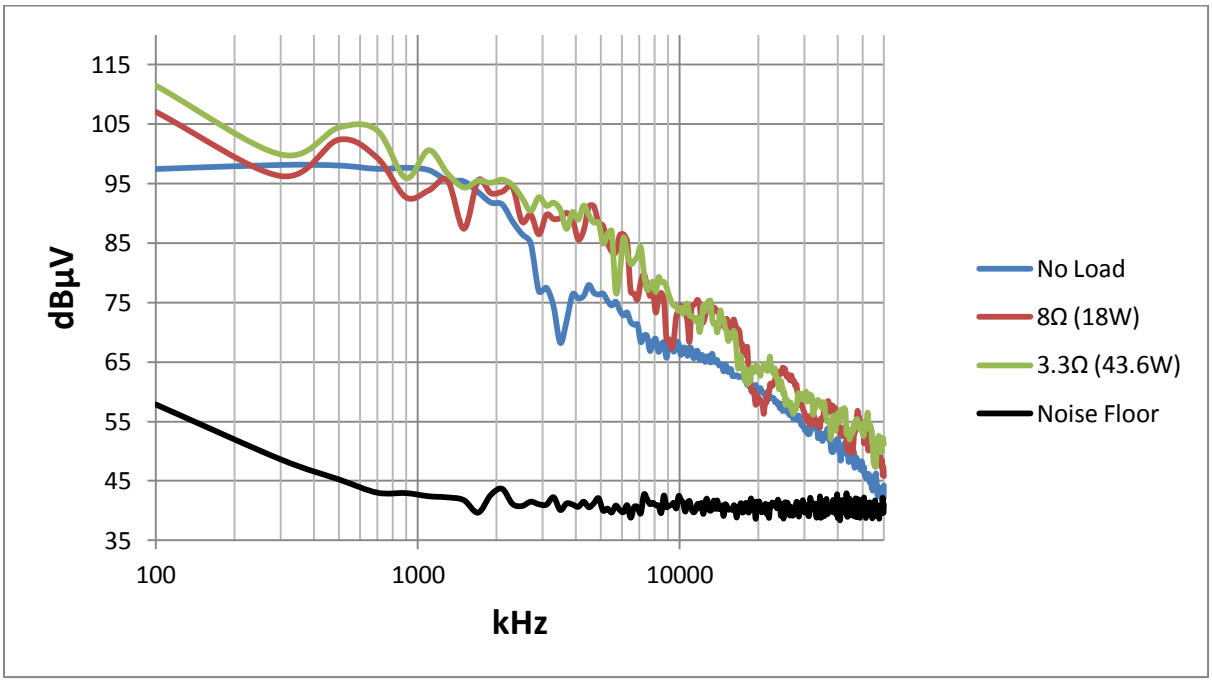



**Figure 6-6 PCB2 200mm Elevation DM Results**

Comparing the no-load spectrum of the Flat and Elevated case in Figure 6-5 and Figure 6-6, there is visibly little or no difference which is expected as zero power flows through the device. Upon loading the DUT, the DM levels increase which is to be expected.

In the instance of the Elevated case and visible in Figure 6-6, below 2MHz there is a visible difference between the 18W and 43.6W results (greater than 3dB). In addition to a variation between the loaded spectrum, the average outline of the said spectrum has decreased to a point where, beyond 10 MHz the loaded and unloaded spectrums essentially meet and at certain instances the loaded spectrum drop below the magnitude of the unloaded spectrum which is not the case in Figure 6-5.

The effect of elevation in the case of DM for Board 2 presents a marginal change if any. As discussed earlier, elevation causes a physical change about the conductors and their physical orientation possibly leading to a change in mutual inductance between the wires and the ground-plane, which may be the factors contributing to a slight variation in DM noise levels.

### *6.2.2 CM Results*

The Common Mode results for the Baseline DUT (PCB 2) are presented in Figure 6-7 and Figure 6-8.

Under no-load conditions in both the elevated and non-elevated case represented by the blue trace, CM EMI is present as was previously observed in 6.1.2 which is speculated to be the resulting effects of MOSFET driver operation. The difference between the elevated and non-elevated spectrums are very slight and hence a change in elevation has little to no effect on MOSFET Driver operation solely.

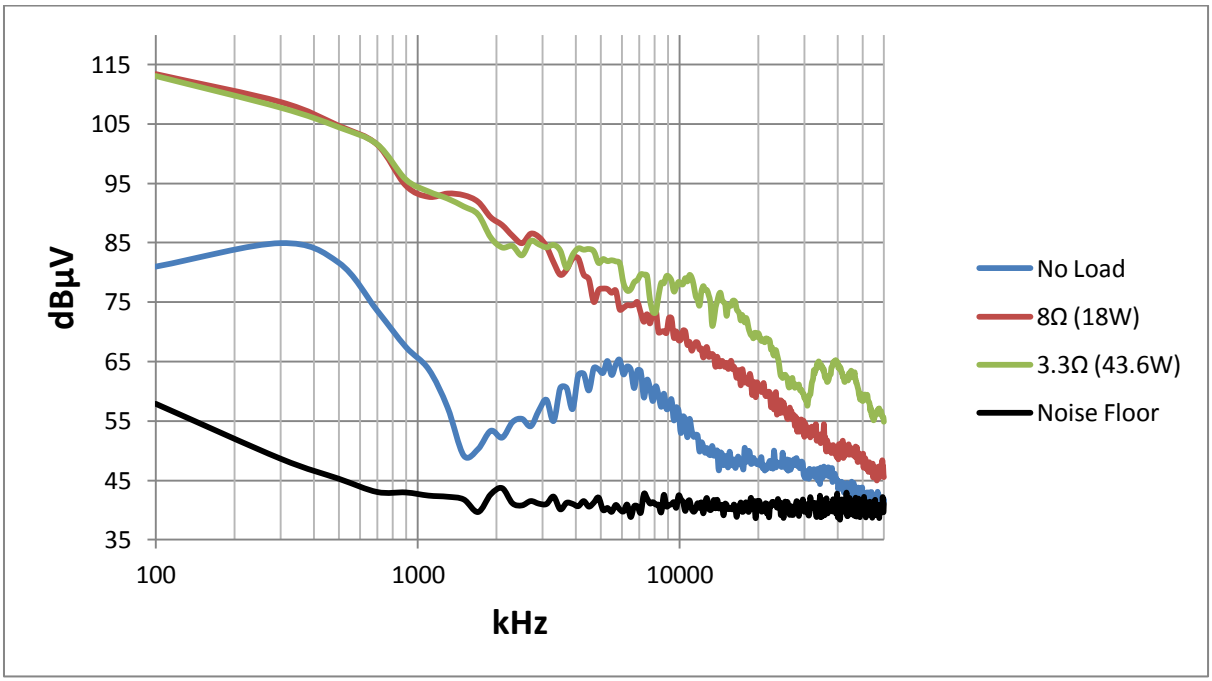



**Figure 6-7 PCB2 Zero Elevation CM Results**

In comparing the loaded waveforms (red and green trace) in Figure 6-7, from approximately 4MHz onwards there is a definite increase in CM EMI present between the respective loads with the greater load (increased power) exhibiting larger EMI magnitudes.

The larger EMI magnitude for the larger load is to be expected as under operating conditions, larger fundamental currents are drawn through the converter which tends to create larger transients and voltage spikes. These flow through parasitic capacitive coupling to the ground-plane, allows larger CM currents to flow and in turn produces a larger CM EMI content.

In the case where the DUT is elevated from the ground-plane in Figure 6-8, the No Load noise outline remains relatively unchanged. However there is a significant difference between the loaded spectrums in both the difference between the elevated and non-elevated instance and between the load levels in the elevated case.

Both the red and green trace in Figure 6-8 exhibit very similar noise outline results where if slightly scrutinised, the higher load actually presents a slightly lower noise outline. Comparing the general outlines of both loads in the elevated case to the non-elevated case, there is a significant decrease in CM EMI content of the 43.6W load. There is also a general decrease of about 3dB across the spectrum.

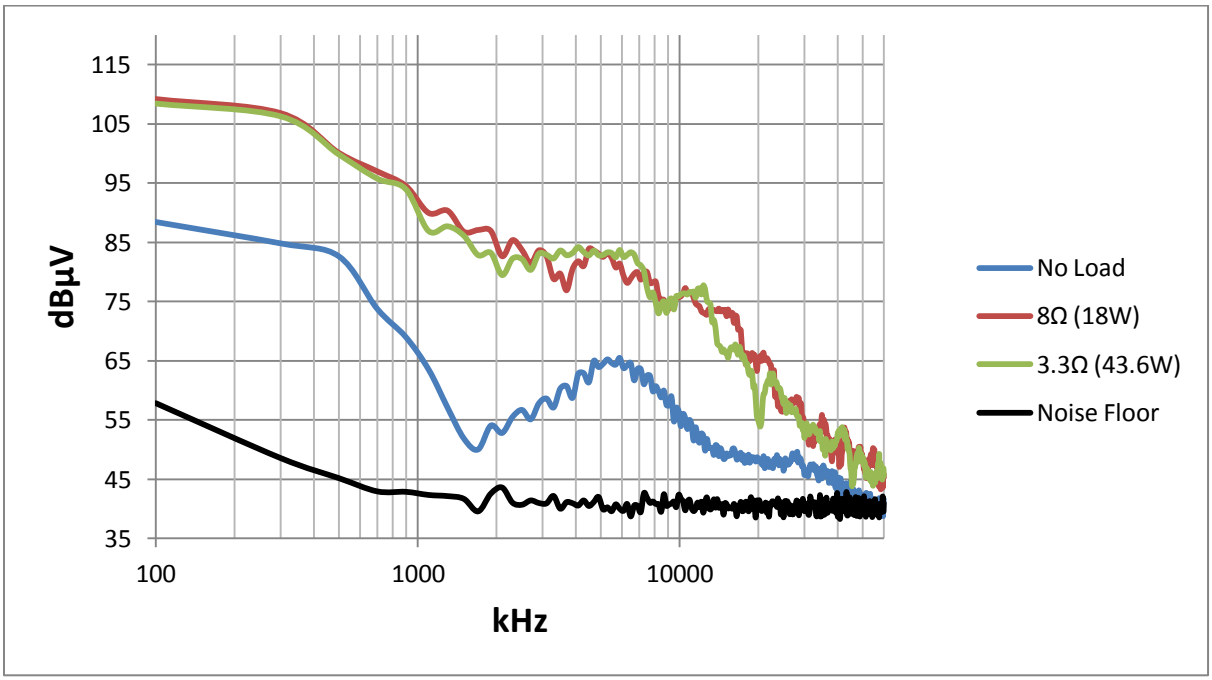



**Figure 6-8 PCB2 200mm Elevation CM Results**

The changes exhibited in the CM noise results illustrate clearly the effect of reduced capacitive coupling to the ground-plane and the effect distance has on the CM EMI. As the distance between the ground-plane is increased, the amount of parasitic capacitance used to couple CM currents is increased resulting in a decrease in CM EMI.

In the case where the DUT is placed on the ground-plane, the parasitic capacitive components become dominant as there is a large difference in CM EMI between the two load levels as seen in Figure 6-7. When the distance between the DUT and the ground-plane is increased, the value of parasitic capacitance is decreased substantially and hence the coupling to the ground-plane decreased subsequently which in turn helps prevent CM currents coupling to the ground-plane, allowing other forms of parasitic components within the circuit to become dominant. The general drop in CM EMI levels of both load levels between the elevated and non-elevated case further illustrates the reduction in the parasitic capacitive coupling effect caused by elevation.

## 6.3 PCB3 (3 DIMENSIONAL) RESULTS

The results of the DUT designed in a 3-dimensional manner as illustrated in Figure 4-19 and Figure 4-20 are presented in section 6.3.

### *6.3.1 DM Results*

The DM EMI results for the 3-dimensional DUT are presented in Figure 6-9 and Figure 6-10.

As presented in sections 6.1 and 6.2, where the blue trace represents the no-load operation of the converter, the DM EMI levels are present at a significant level in absence of converter output impedance. The presence again indicates the significance of MOSFET Driver operation. In the case of the 3-Dimensional DUT, the surface presented to the ground-plane is proportionally smaller in comparison to Boards 1 and 2.

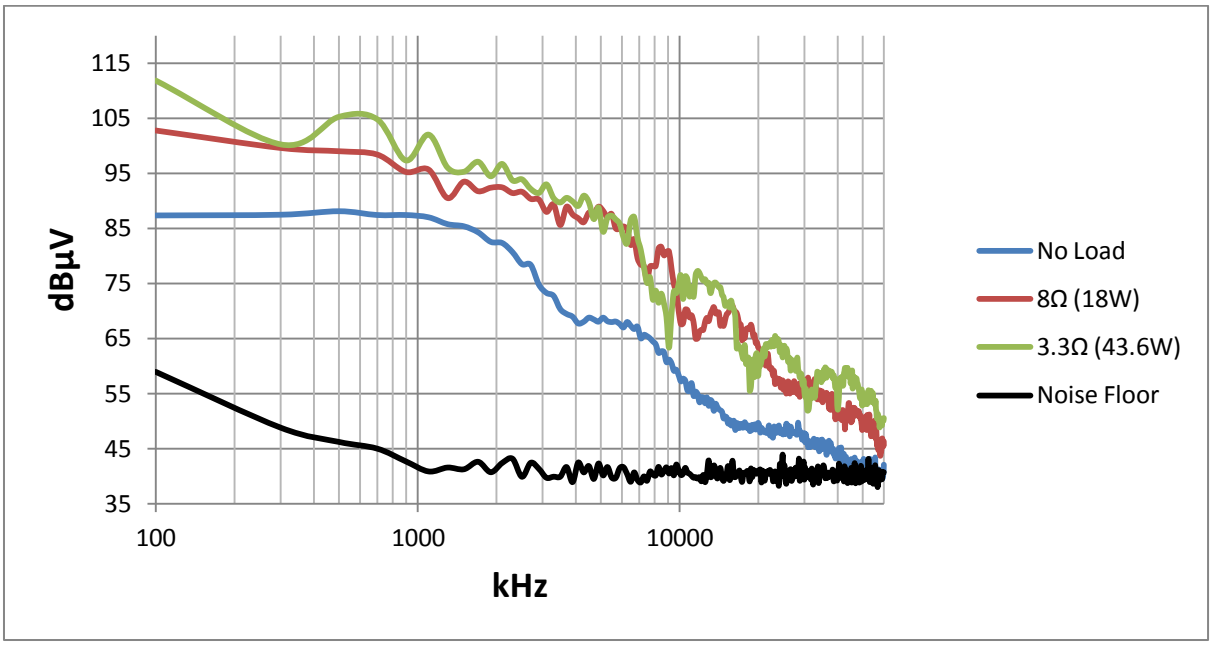



**Figure 6-9 PCB3 Zero Elevation DM Results**

In Figure 6-9 where the elevation above the ground-plane in zero, there is little difference between the results for the 18W and 43.6W load conditions other than a slight increase in noise at frequencies below 4 MHz in the 43.6W loading case. In contrast to the 18W load, the 43.6W load starts to exhibit a fundamental outline of resonance starting just before 10 MHz with an approximate frequency of 1 MHz.

When the DUT is raised from the ground-plane, the results in Figure 6-10 were obtained. The no-load outline presents no appreciable difference whereas there is a notable difference between the loaded instances. The slightly elevated noise levels in the 43.6W measurements below 4 MHz are now reduced to a similar level of the 18W result with the exception of a few peaks over the red trace.

The significantly reduced size of the physical implementation of the 3-Dimensional Board results in similar noise levels for the varied loaded conditions, even when raised significantly above the ground-plane. The reduced physical footprint results in smaller loops and hence less self or loop inductance aiding in the reduction of DM EMI hence the cause for minimal difference between the loaded instances.

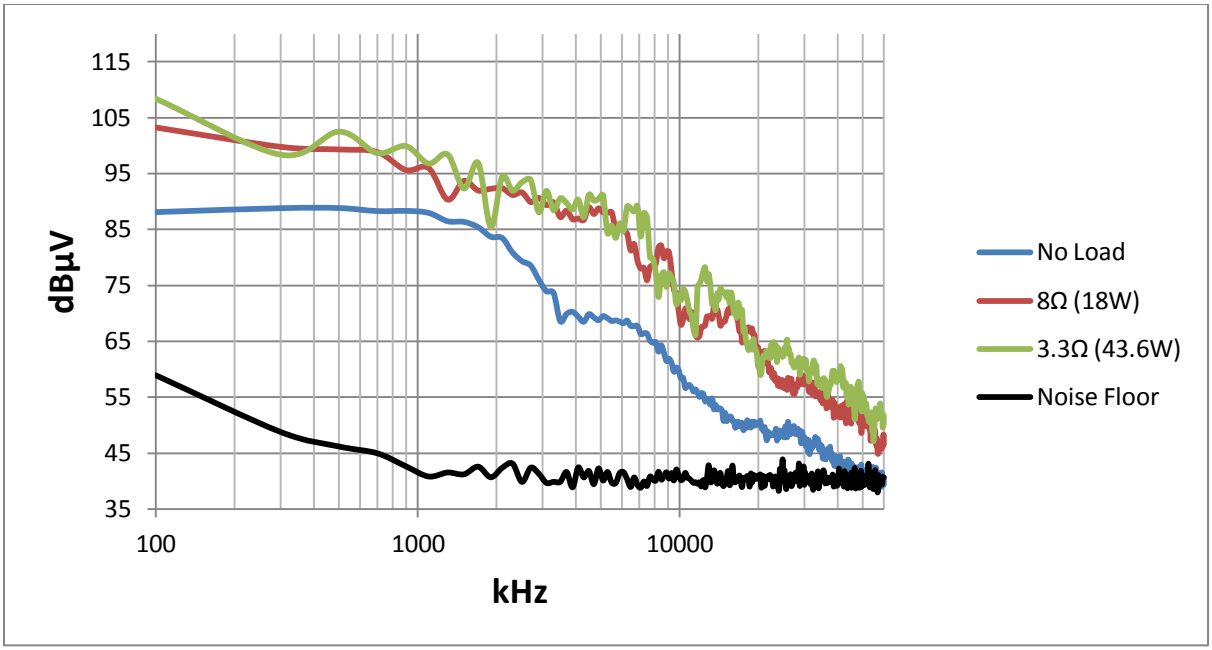



**Figure 6-10 PCB3 200mm Elevation DM Results**

### *6.3.2 CM Results*

The Common-Mode results for the 3-Dimensional DUTs are presented in both Figure 6-11 and Figure 6-12.

Once again during no-load operation of the converter, an appreciable amount of CM EMI is present. The amount of no-load noise differing between the elevated and non-elevated case is once again minimal. The presence of CM in the no-load instance indicates the conversion of DM to CM EMI [2].

The loaded results in the non-elevated case in Figure 6-11 are very similar to the DM results and follow the same trend with the exception of the higher load of 43.6W (green trace) generating less CM EMI from approximately 20 MHz onwards. The increased power throughput leads to increased currents which in the likelihood of the case of the 3-Dimensional board, reaches a resonant point around the 20 MHz point which aids in reducing the EMI generated.

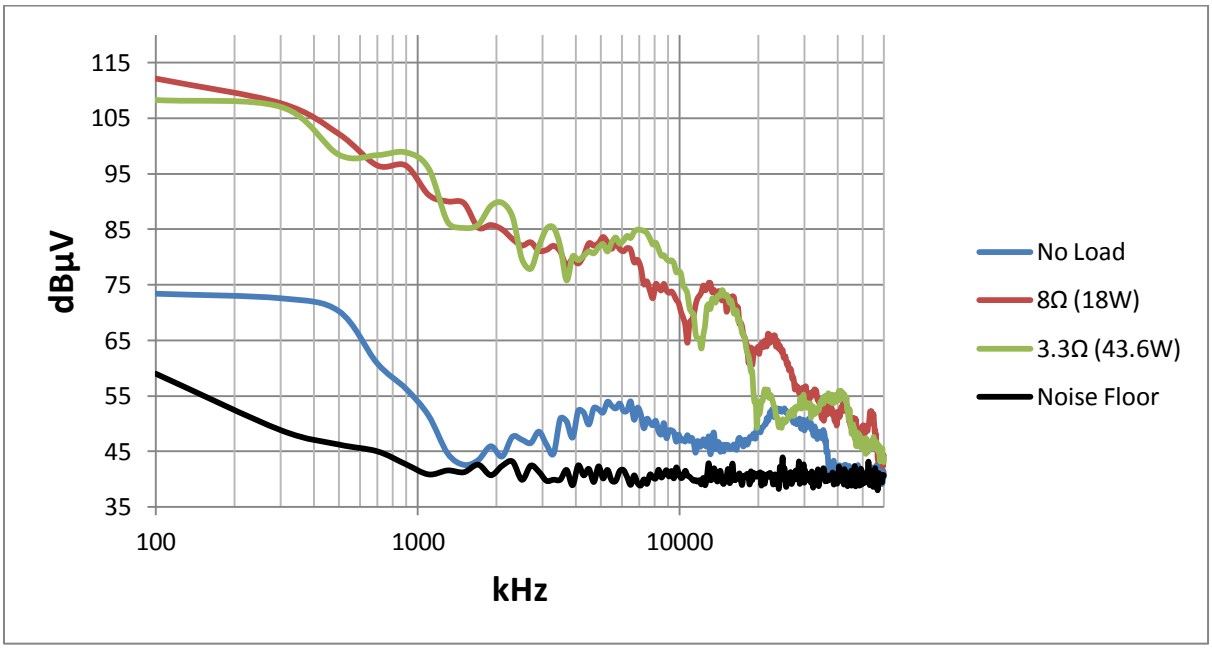



**Figure 6-11 PCB3 Zero Elevation CM Results**

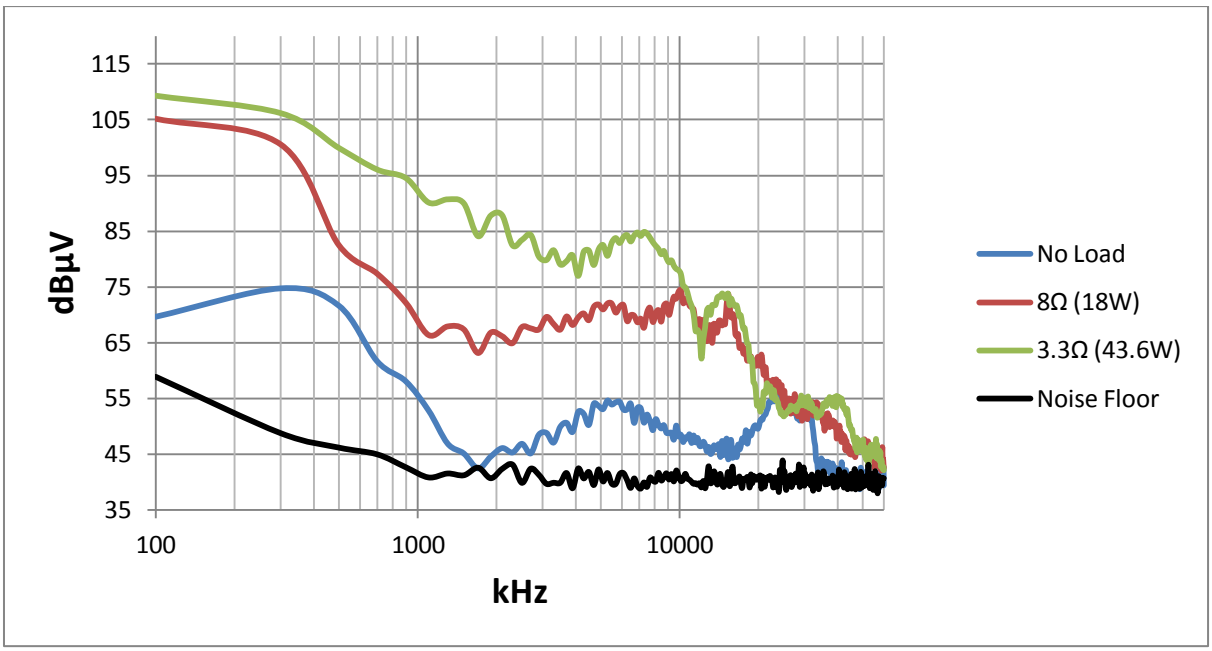



**Figure 6-12 PCB3 200mm Elevation CM Results**

When the board is elevated from the ground-plane in Figure 6-12, the effect of raising the DUT is evident in the 18W load case (red trace) as there is a considerable reduction in CM EMI present below the 10 MHz point. The reduction of noise can be contributed to an increase in the parasitic capacitance between the board and the ground-plane. In addition to the change in the 18W load spectrum, there is very little change in the spectrum of the 43.6W load scenarios between both the elevated and non-elevated case.

The reduction of CM EMI in the case of the 18W load with the change of elevation is to be expected. The lack of change of CM EMI in the 43.6W case is contradictory as the CM EMI spectrum is expected to decrease as a function of elevation from the ground-plane. The lack of decrease in CM EMI during elevation indicates a coupling mechanism is present which is dominant over the coupling of parasitic capacitance between the board and the ground-plane. The mutual-inductance changes as elevation between the ground-plane and the board is increased and may be the factor contributing to the lack of reduction in CM EMI for the 43.6W case.

The presence of a copper pour on the "Component" side of the PCB is likely to give rise to the effects in addition to half the semiconductor switches being perpendicular to the ground-plane. The copper pour should aid in capacitive coupling to the ground-plane and hence a significant reduction in CM EMI should be illustrated with elevation from the ground-plane which is evident in the 18W case, but counter intuitively did not occur in the 43.6W case.

## 6.4 PCB4 (GEOMETRICALLY SYMMETRICAL) RESULTS

The results for the Geometrically Symmetrical DUT (PCB 4) as illustrated in Figure 4-21 and Figure 4-22 are presented in section 6.4.

### *6.4.1 DM Results*

The Differential Mode results for the Geometrically Symmetrical DUT are presented in Figure 6-13 and Figure 6-14.

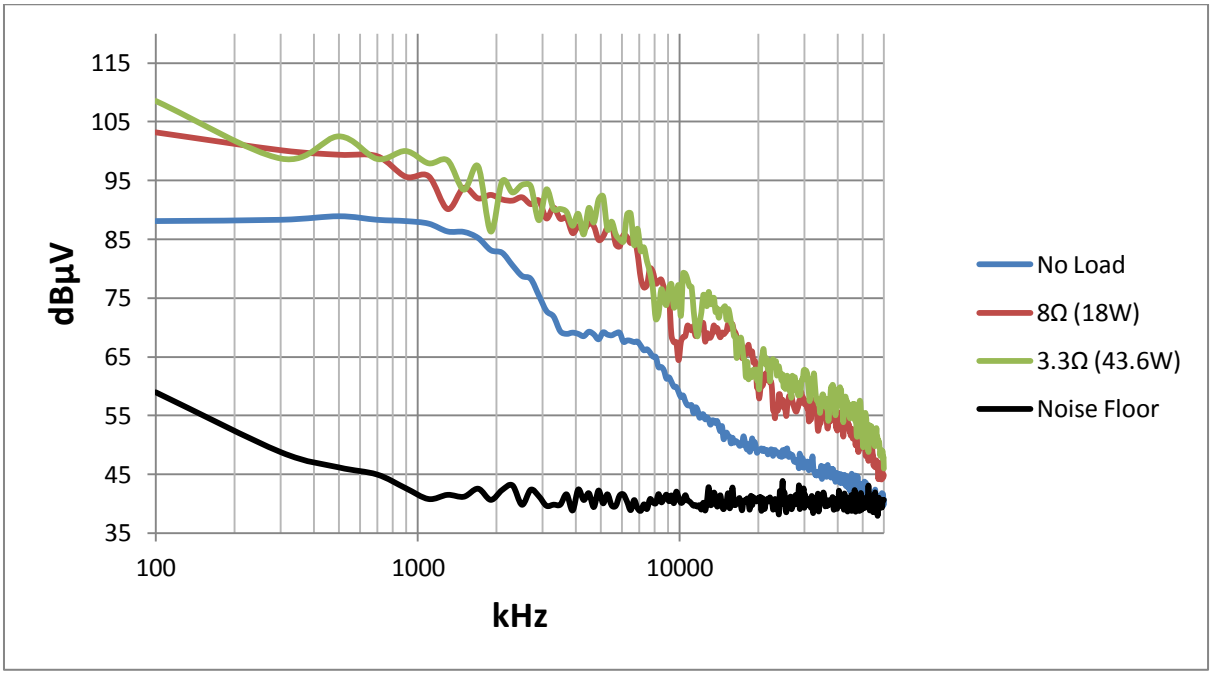



**Figure 6-13 PCB4 Zero Elevation DM Results**

As in the previous sections, the theme of DM EMI present under no-load (blue trace) conditions is evident. In the case of both flat and elevated tests a significant amount of DM EMI is present which is an indication of MOSFET Drive operation as discussed in section 6.7.

Comparing the 18W (red trace) and 43.6W (green trace) load waveforms in the flat case in Figure 6-13, there is no appreciable difference other than a marginal increase in the waveforms, indicating the increased power levels exhibiting little effect which is to be expected under normal conditions. The marginal increase in DM EMI can be expected due to increased currents as per the normal operating conditions of the converter. A slight upward shift can be observed indicating an effect of the relationship between current magnitude and loop inductance within the circuit, which can lead to resonance amongst other phenomena.

Analysis between the waveforms of the elevated case in Figure 6-14 presents very similar results indicating the Geometric Symmetry of the circuit has little effect on DM EMI when elevated from the ground-plane.

The similarity of results during elevated tests indicates Geometric Symmetry and not only the absence of copper pours or planes on the PCB's and semiconductor orientation is responsible for DM EMI generation mechanisms.

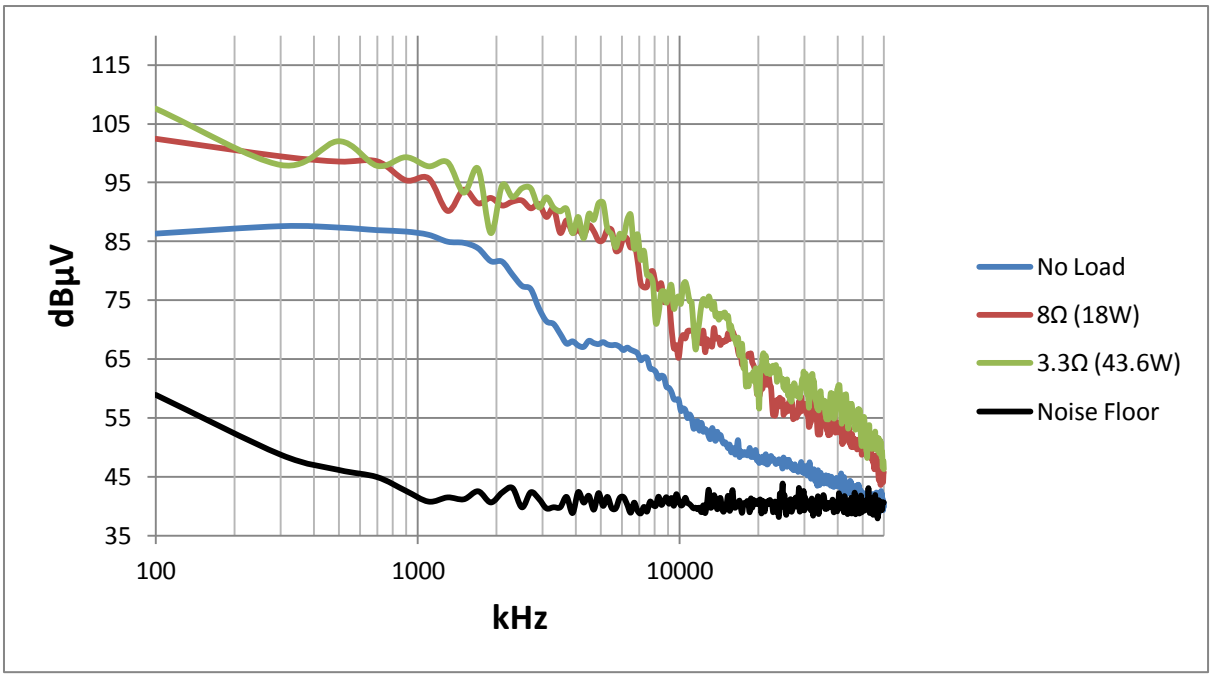



**Figure 6-14 PCB4 200mm Elevation DM Results**

### *6.4.2 CM Results*

The Common-Mode results for the Geometrically Symmetrical DUT are presented for the flat and elevated cases in Figure 6-15 and Figure 6-16 respectively.

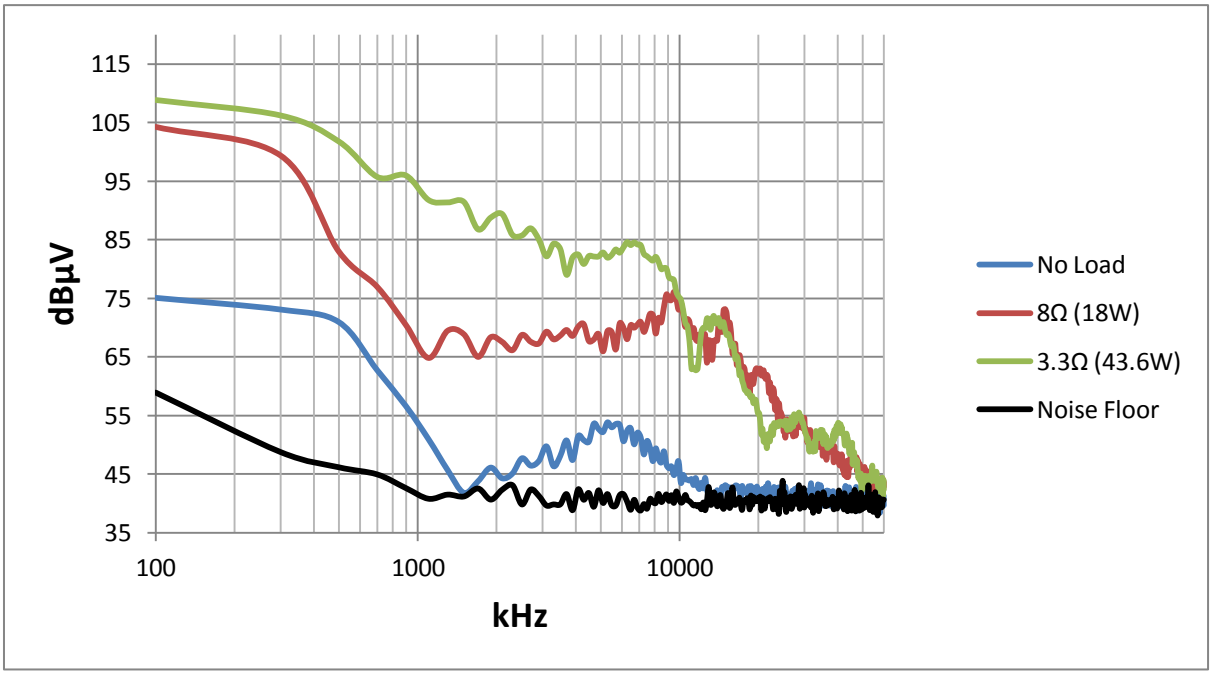



**Figure 6-15 PCB4 Zero Elevation CM Results**

As is the trend within the previous sections, an amount of CM EMI is present during the no-load operating condition of the DUT, implying MOSFET Driver operation presents significant CM EMI generation as discussed in section 6.7.

Comparing the loaded results in Figure 6-15, a CM EMI spectrum of orders of magnitude larger is present up to the 10 MHz mark for the 43.6W load (green trace). A higher noise spectrum is expected as under operating conditions of the converter, larger currents are drawn and hence due to mechanisms discussed in section 2 (such as larger *di/dt*'s) a larger CM EMI content is presented.

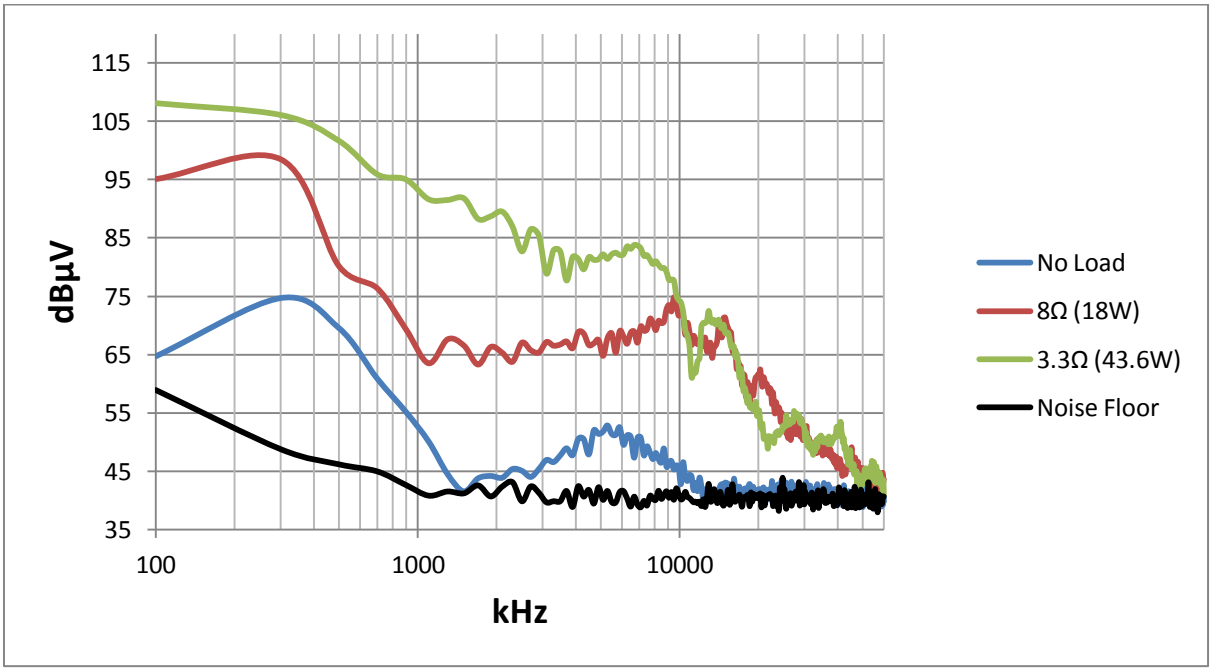



**Figure 6-16 PCB4 200mm Elevation CM Results**

Analysis of the elevated results in Figure 6-16 presents nearly identical results to the flat results in Figure 6-15 and hence the effects of elevation above a ground-plane on the Geometrically Symmetrical Board have little effect.

The absence of a significant change in results between the flat and elevated case indicates the parasitic capacitive coupling normally associated with CM EMI is minimal and distance from a ground-plane has very little effect on the Geometrically Symmetrical Board, indicating Common-Mode currents are more likely to circulate within the circuit or Board than to couple through an alternative source to a victim. The containment of Common-Mode currents within a circuit prevents the currents propagating elsewhere and prevents increased emissions levels.

The absence of a copper pour on any layers and the semiconductor placement are unique to the Geometrically Symmetrical Board. The identical path lengths may also contribute to the reduced CM EMI levels.

## 6.5 PCB1 vs. PCB2 vs. PCB3 vs. PCB4 DM Results

The following section in contrast to the previous subsections is a comparative study of the results of the DUT's against each other in the Differential Mode in order to ascertain the performance of each DUT relative to each other. The direct comparison enables the design of each DUT to be benchmarked against each other to determine the relative performance of each design and the improvements achieved.

### *6.5.1 No Load with Zero Elevation*

The no-load comparisons for the flat experimental results are presented within Figure 6-17 for the Differential Mode measurements.

The first important point to notice in Figure 6-17 is during the no-load operating condition of all the DUT's when zero operational current and hence zero power flows through the converters, there is a significant amount of DM EMI present as previously discovered. The amount of DM EMI can once again be considered significant as the no-load levels exceed EMI Emissions standards (Section 2.4.4) which needs to be complied with even under full load conditions. As discussed in section 6.1, MOSFET Driver operation significantly adds to DM emissions levels.

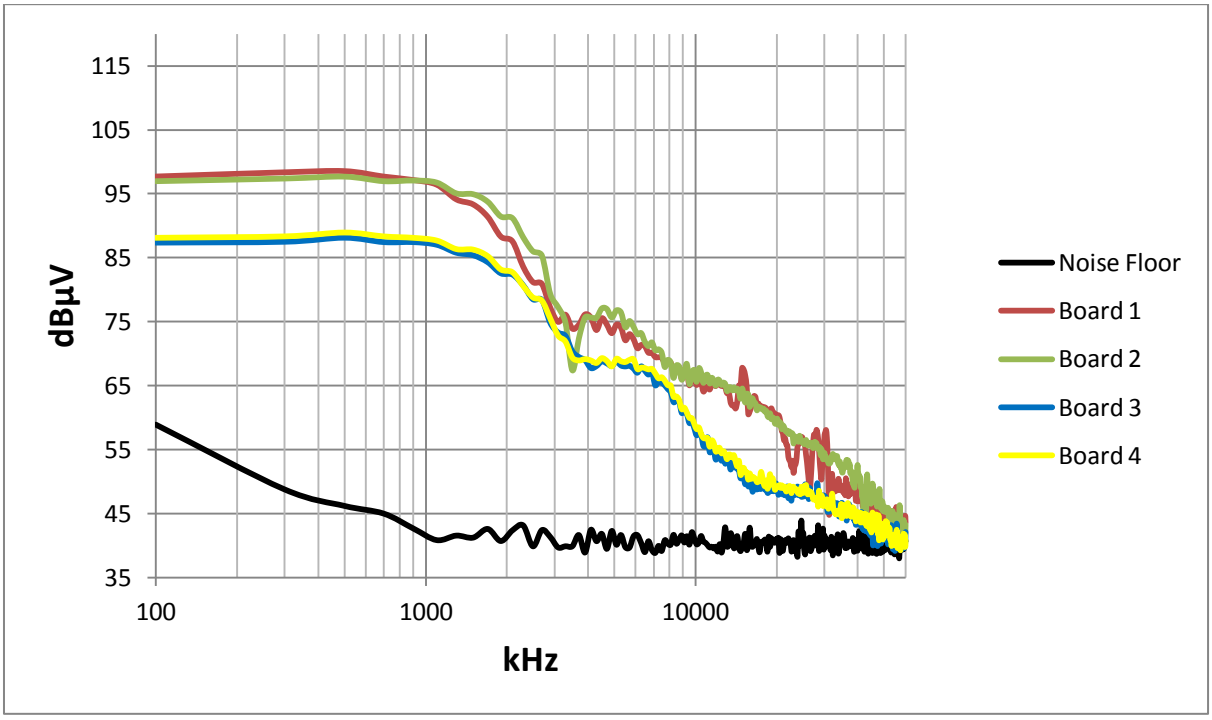



**Figure 6-17 Comparitive No Load Zero Elevation DM Results**

The second noticeable point being the large difference in emission levels between the performance of Board 1 and 2 in comparison to Board 3 and 4, where Board 1 and 2 have similar outlines and similarly Board 3 and 4, despite differing physical layouts.

Points to note about the results in Figure 6-17 when considering Board 1 and 2 are on both these boards the semiconductor devices are on the top side of the PCB or also known as the

Component side. However Board 1 and 2 differ greatly in the physical layout size as Board 1 is orders of magnitude larger in $cm^2$. The significantly larger surface area of Board 1 has little effect on increasing DM EMI in the flat and unloaded case. Hence the physical surface area of the PCB's has little effect on DM EMI during the non-loaded case as represented in Figure 6-17, indicating MOSFET Driving noise is mainly contained within the circuit.

The similarities common to both Board 3 and 4 over the previous two Boards are the physical orientations of the semiconductor devices. In the case of Board 3, the semiconductors are placed in two different planes. The first being two devices on the horizontal and the remaining two devices in the vertical plane. Board 4 has all semiconductor devices in the horizontal plane but are physically situated on opposing layers (Copper and Component side) on the PCB.

Board 1 and Board 3 having copper pours or in the case of Board 1 a "virtual" copper pour as discussed previously, has had no visible effect on the DM EMI spectrum.

From the results presented within Figure 6-17 a noticeable trend is evident, being MOSFET Driver operation only contributes significantly to DM EMI noise in the instance of an unloaded converter. In conjunction with large amounts of DM EMI solely generated from MOSFET Driver operation, the physical layout geometry and properties of a converter aid in either the propagation or mitigation of DM EMI as is evident from the differing amounts of DM EMI generated from the different Boards. The physical placement of semiconductor devices in either perpendicular planes or opposite sides of the converter appears to aid in the mitigation of DM EMI generated through MOSFET Driving. Physical layout area was found to have insignificant impacts in addition to copper pours on EMI mitigation.

### *6.5.2 No Load with 200mm Elevation*

The results for the DUT's when elevated by 200mm from the ground-plane in the unloaded instance are presented in Figure 6-18.

When comparing the results of Figure 6-18 to the flat case as in Figure 6-17, there is very little difference in the results when elevation is the changed variable in the DM EMI measurements.

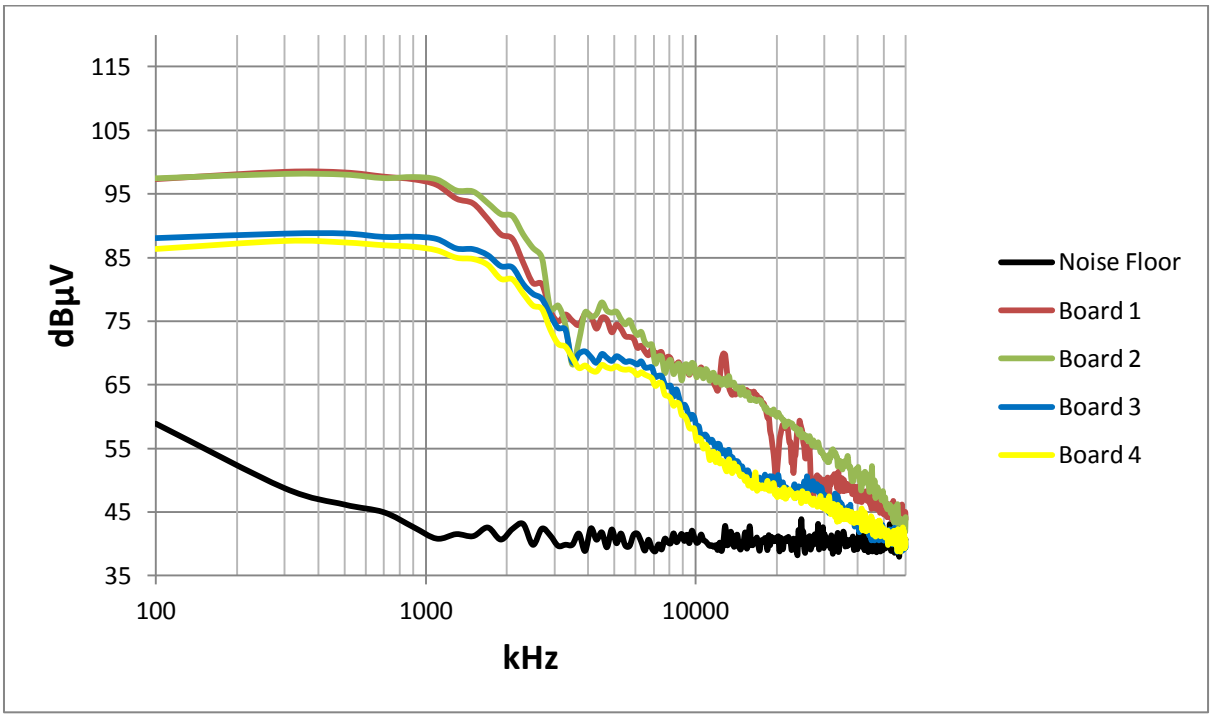



**Figure 6-18 Comparitive No Load 200mm Elevation DM Results**

The only minor differences being a slight shift in the spectrum of Board 1's peaks below 10.5 MHz. Board 1 is the only DUT with an appreciable surface area and the effects of coupling are most evident in the case of Board 1. The shift in the spectrum for Board 1 may arise from a possible change in mutual inductance arising from elevation [14]. An increased amount of inductance may contribute to a shift in the DM EMI spectrum as presented in [4]. A marginal decrease in DM EMI for all Boards is evident, however this is relatively insignificant.

The presence of an appreciable amount of DM EMI when the DUT's are not loaded indicates again the significance of MOSFET Driver operation. The increased height above the ground-plane has little to no effect on MOSFET Driver DM EMI and hence indicates the DM EMI generated through gate driving is mainly contained within the converters and does not use a coupling mechanism through the ground-plane.

### *6.5.3 Loaded with Zero Elevation*

To demonstrate the comparison of the loaded results for the DM EMI of the DUTs at zero elevation, Figure 6-19 only comprises of the 43.6W load cases for Board 1 through 4 as the higher loading presents the most significant worst case DM results for each Board.

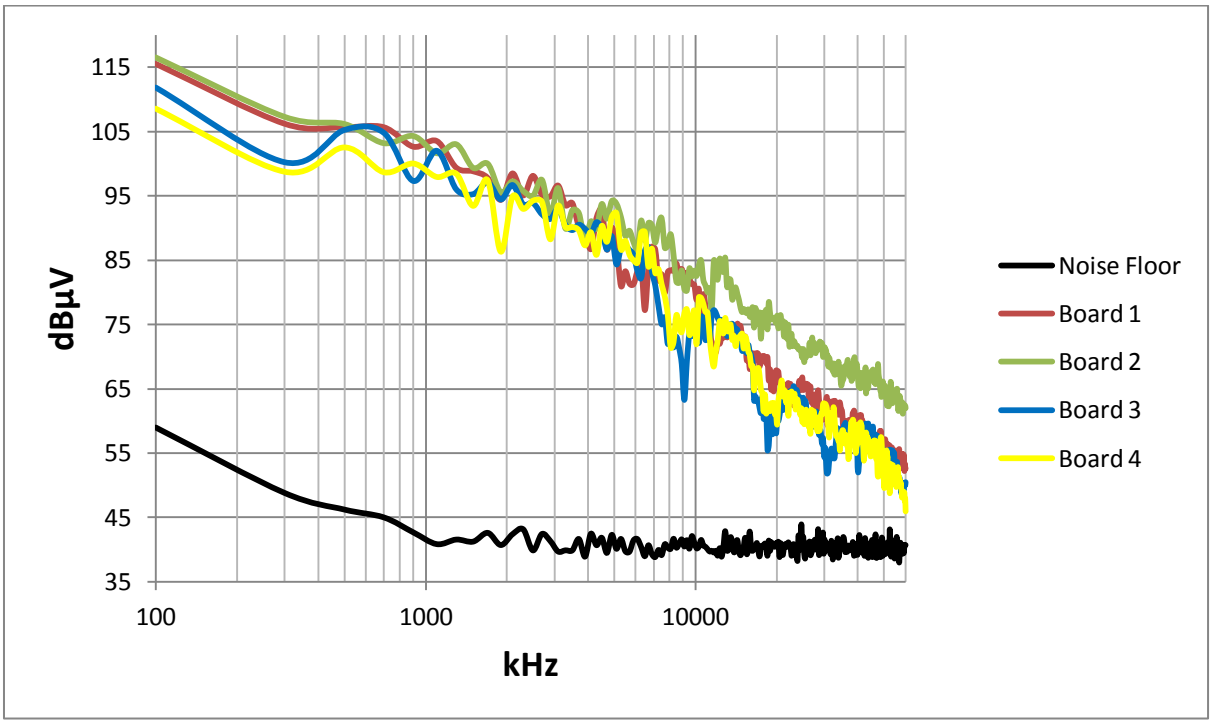



**Figure 6-19 Comparitive Loaded Zero Elevation DM Results**

In Figure 6-19 (similar to the individual results), an increase in power throughput due to current flow in the DUT's causes a general increase in DM EMI. The increase in DM EMI is to be expected as the fundamental operation of the converters by definition generate differential currents and hence DM EMI.

In comparison to Figure 6-17, during loaded operation there is a significant increase in DM EMI, between 10 and 20dB throughout all the results. All the DUT's present a similar noise outline with Board 4 producing a marginally better result throughout the spectrum due to the lowest levels below the 2 MHz mark. The orientation of semiconductor devices on Board 4 seems to aid in the mitigation of the MOSFET Driver operation (Section 6.7) and hence aids in the reduction of levels overall.

Board 2 is the worst performing board with increased noise levels from approximately 6 MHz onwards in the worst case of about 10dB's towards the end of the spectrum. The result of Board 2's performance can firstly be attributed to being the worst performing in mitigation of MOSFET Driver operation as is visible in Figure 6-17 which adds to the overall emissions level. Board 2 is the only board where the semiconductor devices are all on the same plane and are orientated with their heat-sinking surfaces (Drain Pad) parallel to the ground-plane. The semiconductor devices being orientated with their heat-sinking surfaces parallel with the plane and hence the ground-plane provides Board 2 with the greatest parasitic or capacitive coupling.

The large layout and hence large track loops (self inductance) of Board 1 in turn aids the mitigation of DM EMI as an increase in loop inductance or series inductance reduces DM EMI [4].

### 6.5.4 Loaded with 200mm Elevation

As in section 6.5.3, for the loaded results of the DUT's in the elevated case, the 43.6W results were compared only as the higher power levels represent the worst case results for comparison of the Boards.

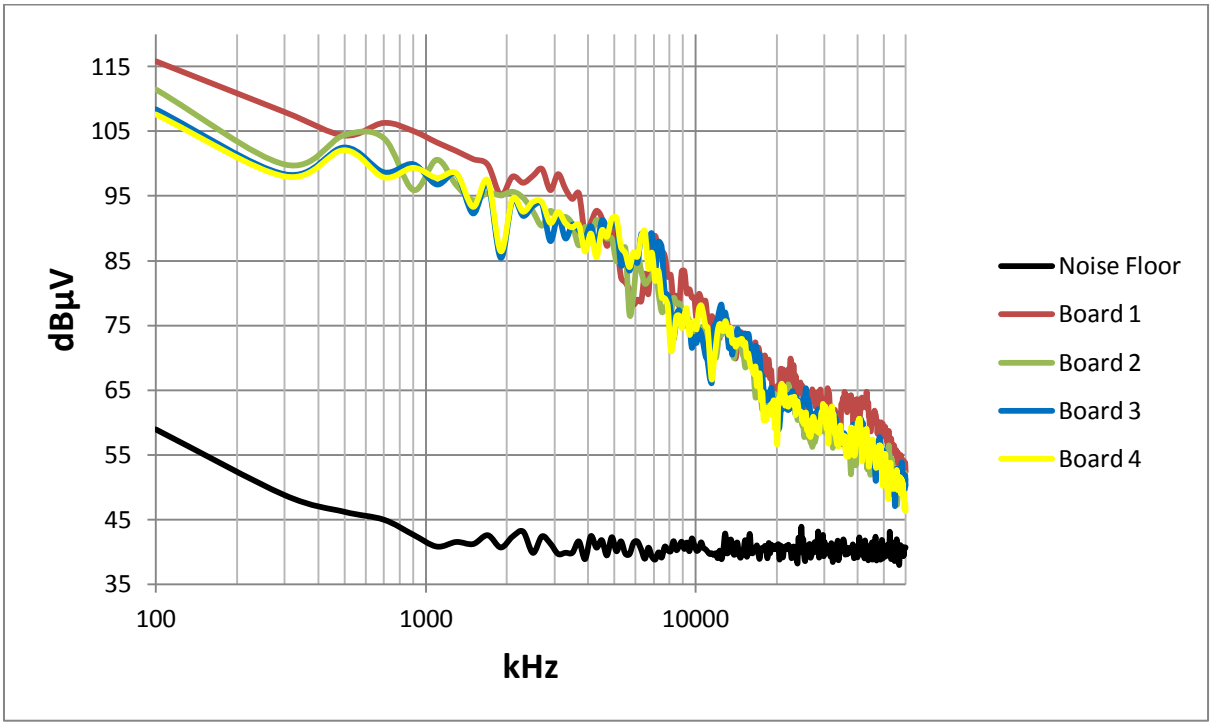



**Figure 6-20 Comparitive Loaded 200mm Elevation DM Results**

As found previously within sections 6.1.1, 6.2.1, 6.3.1 and 6.4.1 the increased elevation above the ground-plane has minimal impact on the DM EMI levels when a DUT is placed under load. The minimal impact on DM EMI with elevation is to be expected as DM currents are primarily associated with current flow within a circuit and not currents flowing out via other parasitic means.

The only significant results are the performance of Board 1 and Board 2, where Board 1 exhibits a slightly higher noise level over the other Boards. Board 2's noise levels have dropped significantly and are in line with the results of Board 3 and 4. The slight change in DM EMI levels mentioned during circuit elevation indicates however there are mechanisms present which affect DM EMI through elevation.

The relatively high emission levels of Board 1 (or the minimal reduction in EMI with elevation) over the other Boards indicates a relationship between physical board size and height between the ground-plane, as Board 1 exhibits the least reduction in DM EMI when elevated. The physically large loops within the circuit remain dominant in the contribution to self inductance and hence when raised from the ground-plane, the possible change in mutual inductance is non-dominant in its effects.

Board 2 however exhibits an appreciable decrease in DM EMI when raised above the ground-plane, in the order of 10dB's from 6 MHz onwards when compared to Figure 6-19. The decrease in DM EMI due to elevation implies orientation of semiconductor devices on their PCB's in relation to ground-planes contributes significantly to the generation mechanisms of DM EMI. In contrast to the other Boards, Board 2 is the only board with all semiconductor devices with their heat-sink (or PAD) surfaces parallel to the ground-plane with double the heat-sink (PAD) surface area in an identical orientation to any other Board. The increased surface area appears to provide a means to couple to the ground-plane. When elevated the coupling appears to reduce and hence DM EMI levels reduce.

## 6.6 PCB1 vs. PCB2 vs. PCB3 vs. PCB4 CM Results

The Common-Mode results comparisons are presented within section 6.6. As in section 6.5, the no-load results are presented for the various DUT's and only the 43.6W load case for each board presented as to illustrate the worst case loaded scenario only. The effects of elevation from the ground-plane are illustrated within the elevation results.

### *6.6.1 No Load with Zero Elevation*

The Common-Mode results for Board 1 through 4 are presented here for the case where the DUT's are flush mounted (flat) to the ground-plane with no load present on the output of the converter. The MOSFET Driver circuit is functional in all cases (excluding the Noise Floor measurements) and the results of which are illustrated in Figure 6-21.

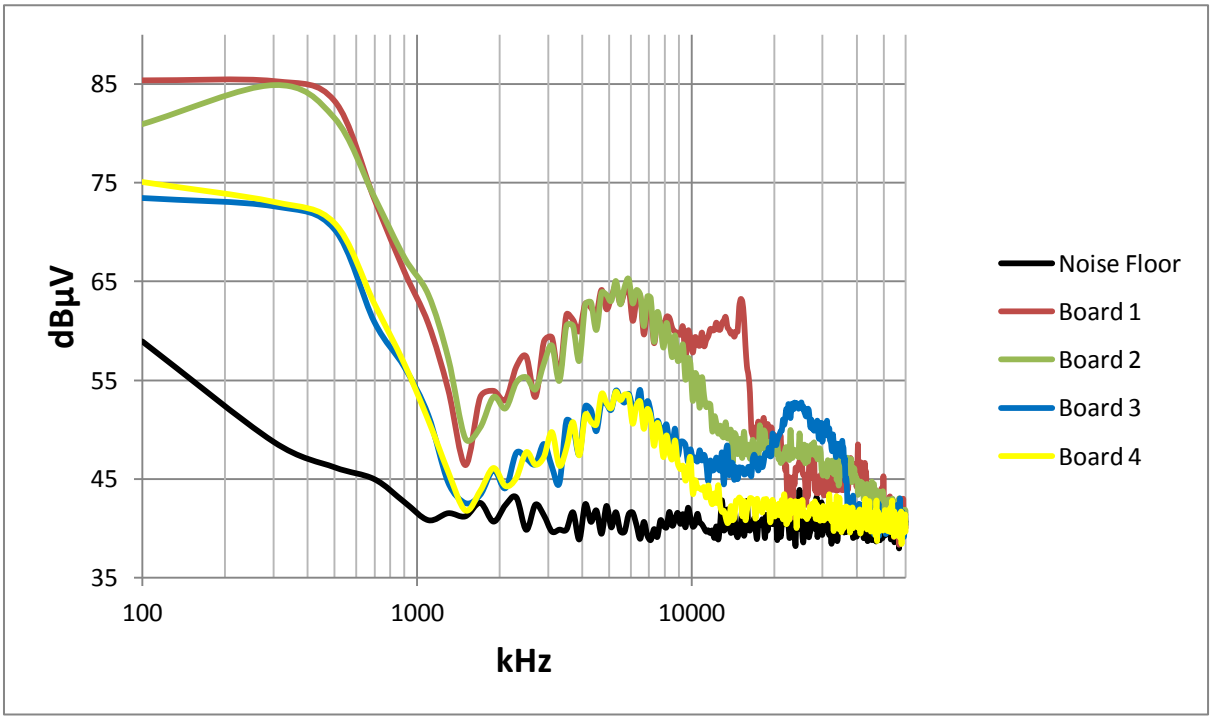



**Figure 6-21 Comparitive No Load Zero Elevation CM Results**

In Figure 6-21, there is a significant amount of CM EMI present during the no-load operation of all the DUT's. The presence of such a large amount of CM EMI under the no-load conditions of the converters is extremely significant as is in the case presented for the DM results in section 6.5.

In addition to the presence of a large CM content for all the Boards, there are two sets of trends. Firstly Board 1 and 2 have a similar spectrum outline up until 10 MHz where in the region between 10 to 20 MHz, Board 1 exhibits a resonant point producing a large peak. Secondly, Boards 3 and 4 present a similar spectral outline up to about 10 MHz as is evident with the case of Boards 1 and 2, where similarly the spectral outline of Board 3 increases substantially before decreasing. Boards 3 and 4 however present significantly lower spectral outlines over Boards 1 and 2, with Board 4 presenting the lowest amount of content beyond

10 MHz and hence the best result. The performance of the Boards relative to each other is similar to the DM results.

A few trends are evident from Figure 6-21. Firstly being Board 1 and 2 with their similar spectrum outlines. As mentioned previously, these boards in contrast to Boards 3 and 4 have all their semiconductor devices on the same plane. The orientation and placement of the semiconductor devices on the same plane presents a larger "PAD" area to the ground-plane. In CM EMI, the larger surface area presented increases capacitive coupling and hence increases the parasitic components between the semiconductor devices and the ground-plane. Larger parasitic components allow for larger CM currents to flow and hence increases the CM content.

The second trend being similar to the first, where both Boards 3 and 4 have their semiconductor devices orientated and positioned differently such as they are either in an adjacent plane or opposing side of the PCB. In contrast to the first trend, the CM EMI content is reduced due to reduced coupling as a result of orientation. Capacitive coupling is reduced as the effective surface area presented parallel to the ground-plane is reduced. In the case of Board 3, half the semiconductor devices are positioned in a horizontal position as to present an extremely small surface area to the ground-plane through the semiconductor PAD. In the case of Board 4, the Geometric Symmetry with the PAD's of the semiconductors overlapping each other, the effects of coupling have been reduced.

The third trend includes Board 1 and 3 where both experience a sudden increase in CM EMI content above 10 MHz. Common to both Boards are the effective copper pours of the DUTs, where Board 1 effectively has a large conductive area due to the remaining "strips" or tracks of the Veroboard which are unused which behaves like a copper pour. Board 3 by design was implemented with a copper pour. These effective areas present a larger conductive coupling plane to the Common-Mode currents which then couple easier to the ground-plane. The increased capacitive coupling in Boards 1 and 3 hence increases the Common-Mode EMI spectrum generated from these Boards which is evident in Figure 6-21.

Board 4, with the combination of both the absence of a copper pour and the orientation of the semiconductor devices relative to the board aid in the mitigating mechanisms and hence produces the least CM EMI resulting in Board 4 performing the best for the no-load, flat case.

### *6.6.2 No Load with 200mm Elevation*

The results for the comparison of Board 1 through 4 during the elevated, unloaded case for the Common–Mode results are presented in Figure 6-23. MOSFET Driving during the test cases was in operation.

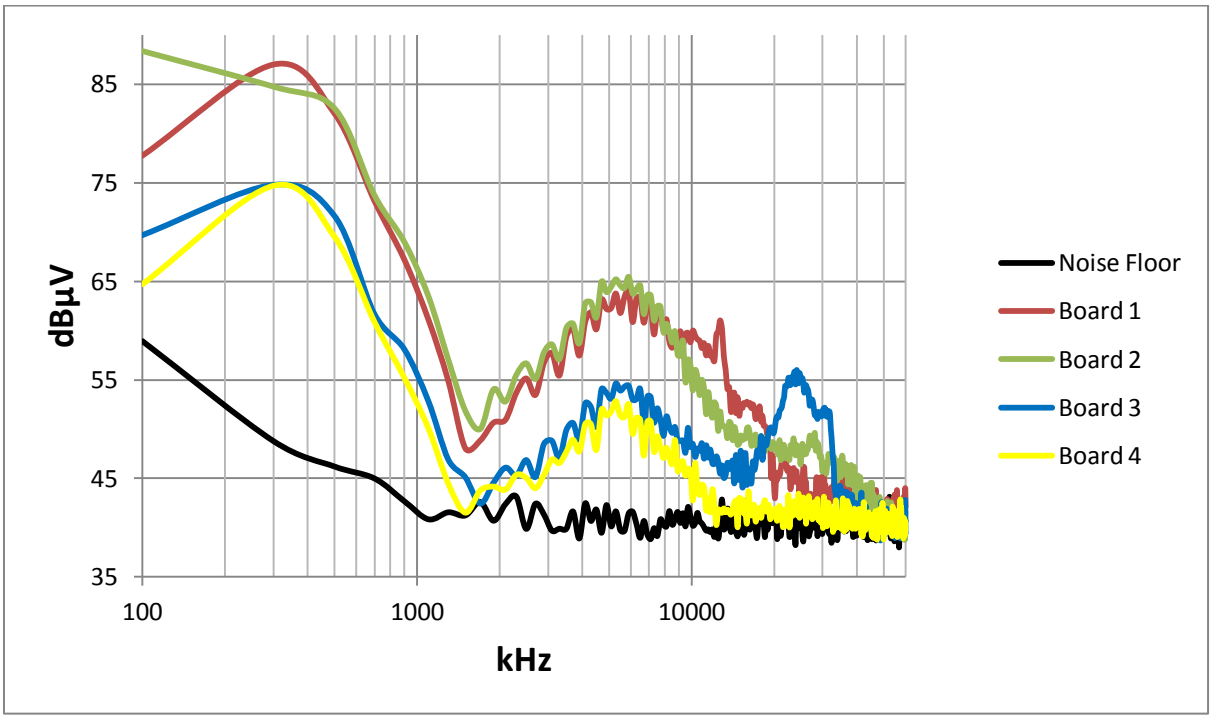



**Figure 6-22 Comparitive No Load 200mm Elevation CM Results**

Two major points are noticeable from Figure 6-22. Firstly, counter intuitively is the increased noise levels of Board 3 (blue trace) at approximately 25 MHz, (about 8dB's) and secondly the decrease in emissions from Board 1 (red trace) in the region of 10-20 MHz with respect to the results in Figure 6-21.

Firstly in Board 3, the evident shift in spectrum in DM between 10-20 MHz (shift left) during elevation and the increase in CM about the same point. The increase in elevation changes a coupling mechanism in the DM and hence through DM to CM conversion, (and presumably resonance) an increase in CM is present around the 10-20 MHz region. Secondly, in Board 1 an increase in height causes decreased capacitive coupling and hence less CM EMI noise is present. The significantly larger decrease in noise levels of Board 1 relative to the other Boards is expected due to the relatively large surface area and coupling surface of the DUT. The increase in height above the ground-plane illustrates an increase in parasitic capacitive coupling for the case of Board 1 and demonstrates the theory associated with CM EMI and coupling to a ground-plane effectively.

In addition to the major points highlighted, the general spectrum outlined by the waveforms in Figure 6-22 have changed very little (except below 300 kHz) indicating the noise generated by the MOSFET Driver circuit is mainly contained within the circuit.

An important trend is highlighted throughout sections 6.5.1, 6.5.2, 6.6.1, 6.6.2, where MOSFET Driver operation is significant and changes in the unloaded case are related to DUT operation and MOSFET Driving noise susceptibility.

### 6.6.3 Loaded with Zero Elevation

The comparative CM EMI results for Boards 1 through 4 are presented in Figure 6-23 during the loaded operation of the DUT's with no elevation (flat).

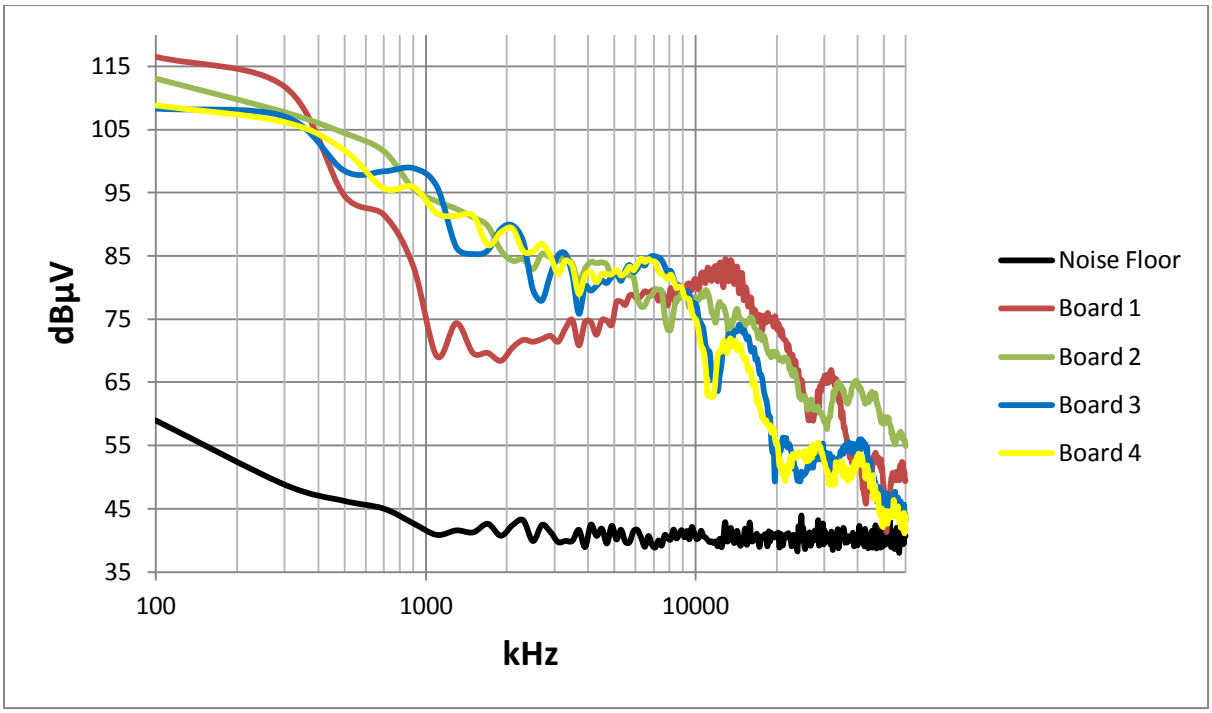



**Figure 6-23 Comparitive Loaded Zero Elevation CM Results**

The introduction of load to the DUT's increases the amount of CM EMI generated significantly below 6 MHz. The significant increase is inherent to the functional operations of the converter due to functional current draw (DM) and the subsequent conversion of DM to CM [2].

Between 400 kHz and 9 MHz, Board 1 (red trace) exhibits a significantly reduced amount of CM EMI during loaded operation, where beyond 9 MHz performance decreases (increased emissions). The lower levels of CM EMI presented for Board 1 below 9 MHz can be attributed to the larger loop or self inductance (DM to CM conversion) due to the appreciably larger circuit of Board 1 in contrast to the other Boards. The performance however above 9 MHz is negated by the dominating capacitive coupling due to an effective larger surface area.

Similarly as with Board 1, the effects of capacitive coupling in Board 2 are evident from 10 MHz onwards where the performance is worse than Boards 3 and 4. The capacitive coupling in the case of Board 2 is due to an effective semiconductor PAD area (four times) presented to the ground-plane which is larger than any of the other Boards.

The performance of Boards 3 and 4 present similar outlines here in the loaded case, where it is difficult to determine whether either performs better. The relatively better results for Board 3 and 4 above 10 MHz can however be attributed to factors which have been mentioned previously and include: semiconductor orientation and placement relative to

planes and PCB sides, effective copper pour areas, physical track lengths and associated loop or self inductance.

### *6.6.4 Loaded with 200mm Elevation*

The results presented within Figure 6-24 demonstrate the performance of Boards 1 through 4 during the loaded, elevated case.

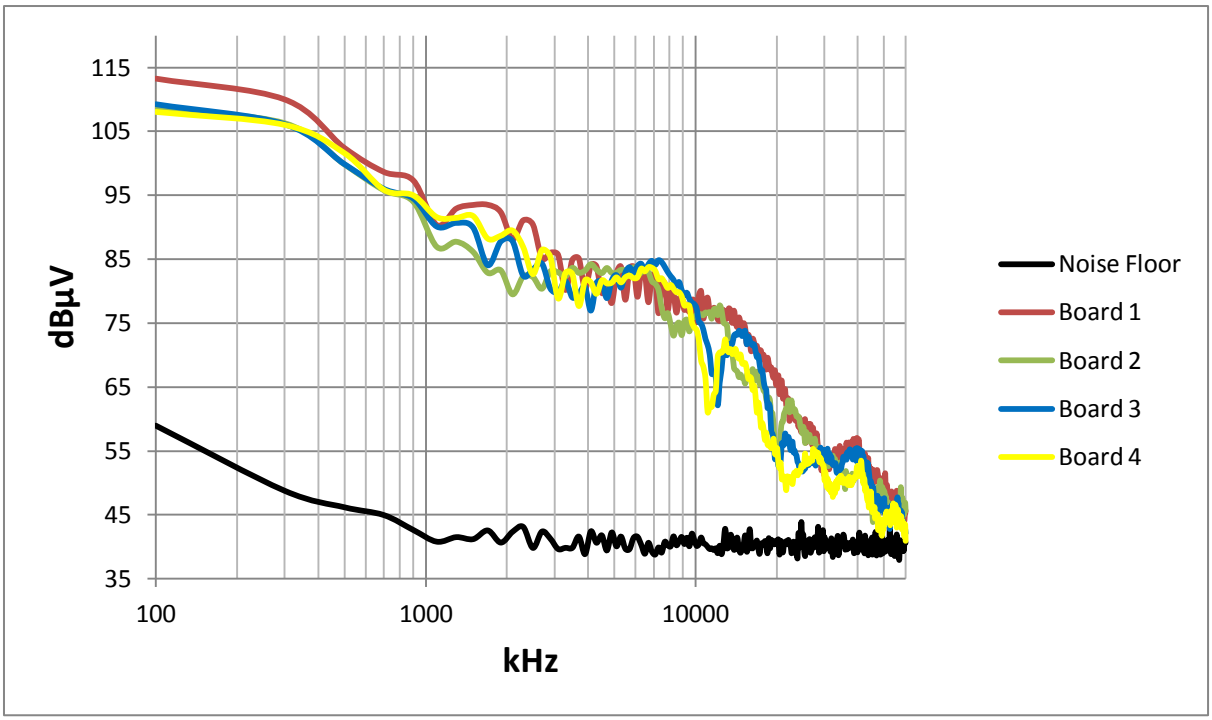



**Figure 6-24 Comparitive Loaded 200mm Elevation CM Results**

In comparison to Figure 6-23, there are two significant changes notable. Firstly being the change in the outline of the spectrum of Board 1 (red trace) and secondly the change in Board 2's spectrum. The average result being a decrease in the spectral outline.

Two dominating phenomena occur in the elevation of Board 1 from the ground-plane. Firstly the decrease of capacitive coupling with the ground-plane as is evident in the decrease of the spectrum above 9 MHz in the red trace. Secondly the increase in spectral content of Board 1 in the 400 kHz to 9 MHz region, due to the speculated change in mutual inductance as discussed previously or other coupling mechanisms in the DM and incidentally the DM to CM conversion process thereof.

Board 2 exhibits a decrease in CM EMI from 9 MHz onwards such that the performance is similar to Boards 3 and 4. The decrease is due to a reduction in parasitic capacitive coupling resulting from the elevation from the ground-plane resulting from the largest collective semiconductor PAD area of all the Boards. Changes in capacitive coupling (decrease in parasitic components) change the pathways CM currents can flow and hence lead to a decrease in spectral content.

In Figure 6-24, for frequencies over 10 MHz Board 4 performs the best, with notable margins in certain instances but only marginally over Board 3.

Factors which enable the relatively better performance of Board 4 are due to:

- Physical board size (reduction of physical path lengths)
- Lack of copper pours (removes additional capacitive coupling pathways)
- Semiconductor orientation (presentation of semiconductor PAD's to ground)
- Semiconductor side placement (relation to PCB sides)

## 6.7 MOSFET DRIVER NOISE

Figure 6-25 illustrates a typical connection between an IR2113 MOSFET Driver and a high and low side MOSFET. Visible within Figure 6-25 and Figure 6-26 are the diode and bootstrap capacitor used to generate a floating supply. The capacitor (between $V_B$ and $V_S$ in Figure 6-25) during operation is applied or disconnected to the high-side MOSFET to achieve isolated drive.

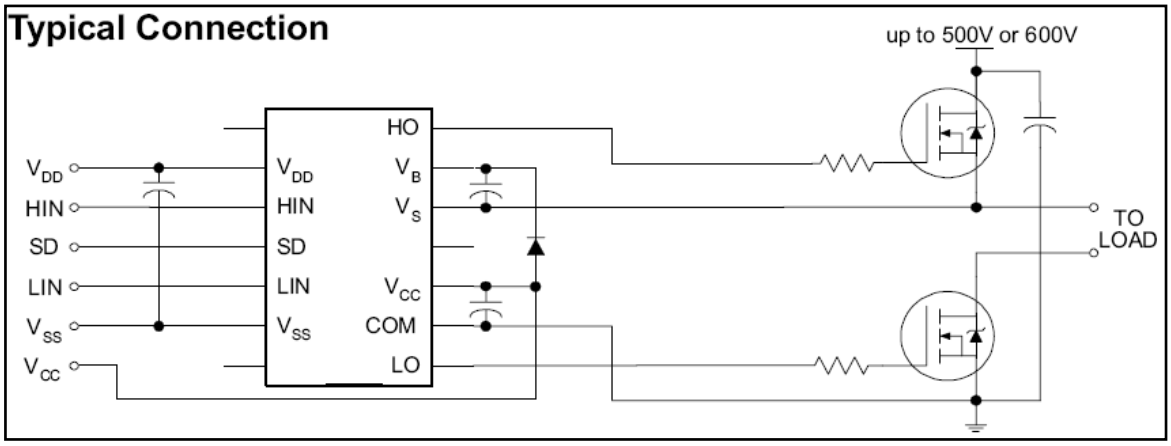



**Figure 6-25 Typical IR2113 Configuration [20]**

During operation of the low-side MOSFET, the current flows in the manner depicted in Figure 6-26 to charge the bootstrap capacitor. During operation of the low side MOSFET in Figure 6-26, current flows through the bootstrap diode and resistor then through the bootstrap capacitor and finally completes the circuit through to ground via the low side MOSFET. Hence current flows through the low side MOSFET during MOSFET Driver operation only. This current can then conduct via the present parasitic capacitive components to form CM currents and hence CM EMI.

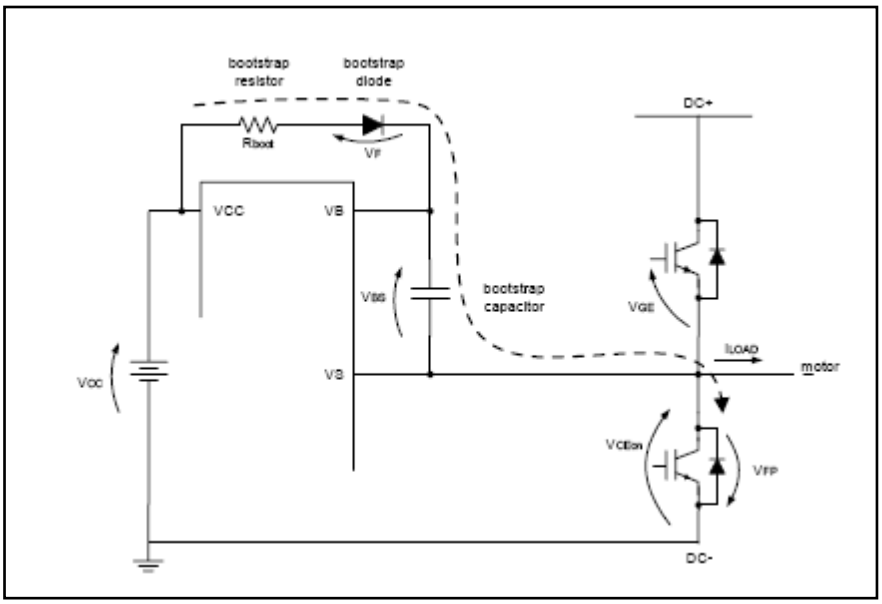



**Figure 6-26 IR2113 Bootstrap Current Path [21]**

The process depicted above in Figure 6-26 is believed to be the root generation mechanism of both DM and CM EMI during the unloaded phases of each DUT. Taking into cognisance the parasitic components of a MOSFET as depicted in Figure 6-27 and the process of bootstrap charging in Figure 6-26, with further research the root mechanisms of MOSFET Driving may be determinable.

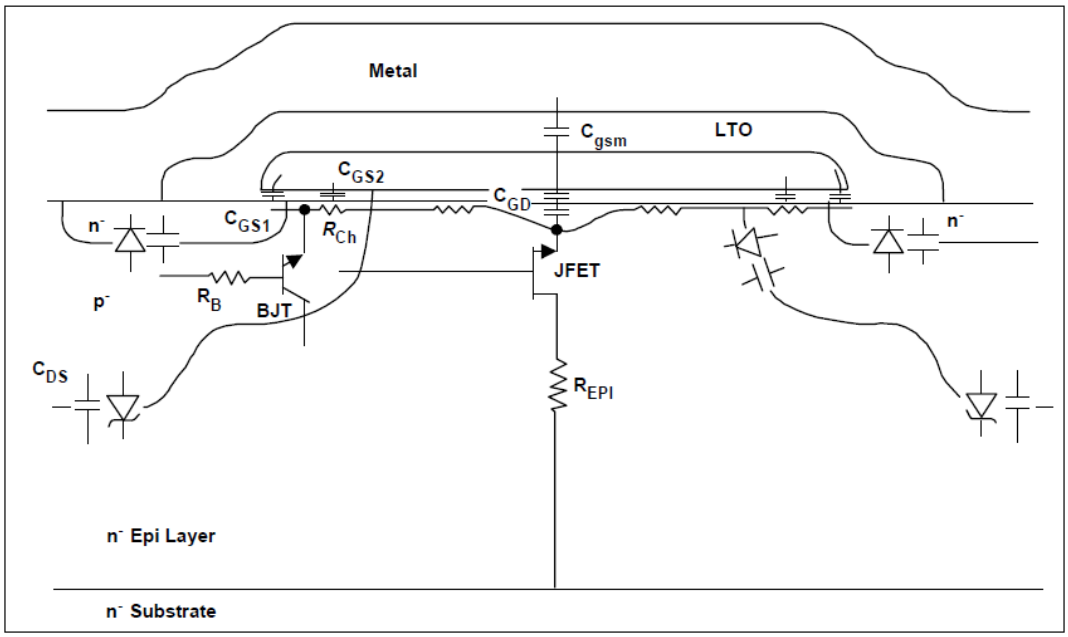



**Figure 6-27 MOSFET Parasitic Components [22]**

## 6.8 CONCLUSION

The results and analysis of the experimental results based on the experimental setup in Chapter 5 for the Boards in Chapter 4 have been presented here within Chapter 6. The differing Boards presented varying EMI results due to their differing circuit layouts and features.

The relatively larger surface and circuit area of Board 1 presented varying results showing the effects of capacitive coupling and large path-lengths, creating large self inductance. Board 2 being relatively smaller showed marginally better results over Board 1. Board 2 demonstrated the effects of EMI caused by presenting all semiconductor PAD's to the ground-plane causing an increase in capacitive coupling. Board 3 presented better results over Board 2. The parallel to the ground-plane orientation of the semiconductors on Board 3 attributed to the relatively better performance over Board 1 and 2. Board 4 presented the best CM results. The relatively better results are attributed to a lack of a copper pour and semiconductor placement. The Geometric Symmetry and associated effects have been discussed pertaining to Board 4's performance as discussed in Section 6.6.4.

An important note during the experimentation process is for the construction of the different DUT's, identical MOSFETS from the same batch were used for Boards 2 through 4. Board 1 used the same part number but in a differing physical package. Despite using identical MOSFETs from the same batch, the semiconductor devices are never absolutely identical in both their rise/fall times and on-state losses. Therefore any difference in the semiconductor switches leads to a mismatch in rise/fall times in phase-pairs and skew may arise which may lead to significant amounts of EMI [23]. As no semiconductors can ever be identically matched in rise/fall times, some amount of EMI is to be expected from mismatch.

To further enhance the experimentation process, the exact semiconductor device used for switch 1 through 4 in the converter could be swapped out to each board such as to maintain the use of the exact semiconductor devices within each Board's test to further enhance the measurement of each Board's performance. In addition to using the same devices for each Board, the rise/fall time of each semiconductor device could be characterised and then tuned through the changing of gate drive resistance in order to achieve near identical rise and fall times, as a variation in rise/fall times results in a change in EMI [4] [23]. The tuning of the rise/fall time for each semiconductor device would further reduce variables within the experiment and hence improve accuracy of the measurements.

# 7 CONCLUSION AND FUTURE WORK

## 7.1 CONCLUSION

The investigation into Electromagnetic Interference and the generation mechanisms of the interference were observed throughout the dissertation. Various circuits and different tests were developed and implemented in order to test the different generation mechanisms of EMI. The following major themes were observed:

- Effective Loop Inductance (Self Inductance)
- Capacitive coupling to the ground-plane
- Distance between ground-plane and converter
- Copper pours areas
- DM to CM conversion process
- MOSFET Driver Operation
- Semiconductor orientation and PCB side placement
- Geometric Symmetry
- Possible Mutual Inductance (in DM)

The presence of a large amount of self inductance through large intentional loops implemented in the first DUT (Board 1) presented expected results. The intentional increase in inductance resulted in a decrease in the magnitude of the operational currents *di/dt* and hence lowered the amount of DM EMI generated. The operational current is said to be choked. The increase in self inductance however has a negating effect on CM EMI as the inductance increases, the voltage transients' increase and these transients then conduct through capacitive means to ground forming larger Common-Mode currents and hence increasing CM EMI. Hence as was observed with Board 1, increased self inductance increases CM EMI whilst reducing DM EMI as in [4].

An additional major generation mechanism of EMI, predominantly in CM EMI was observed and verified. The mechanism being capacitive coupling in the form of parasitic components within semiconductor devices and the copper pour areas within a PCB which couple capacitively to ground. A good example being Board 1 with a large effective capacitive coupling area (remaining strips), which produces large amounts of CM EMI due to coupling to the ground-plane. A second example being Board 2 where the increase in elevation from the ground-plane reduces the amount of CM EMI demonstrating a reduction in capacitive coupling.

Another phenomenon observed was the process of conversion of DM to CM. Board 1 again presented a good example where the DM to CM conversion is visible. The shift in the spectrum of Board 1 during variance is also visible within the CM spectrum indicating a conversion process is evident. The presence of CM EMI during the unloaded cases also confirms the DM to CM conversion process.

A major discovery as highlighted specifically in section 6.1.1 and 6.1.2 and throughout section 6 is the generation of both DM and CM EMI (through conversion) in a converter

when the converter is unloaded and no operational current flows through the converter, but the semiconductor devices still receives gate drive signals. The process of MOSFET Driving hence generates significant amounts of EMI which therefore adds to the EMI spectrum of the converter. The presence of EMI from the MOSFET Drivers is especially significant in the no-load operating point of a converter or in low power converters. The importance thereof needs further investigation and the generation mechanisms need identification. The possible generation mechanisms of which are briefly discussed within section 6.7.

A further discovery observed on EMI levels was the effect semiconductor device placement relative to horizontal or vertical planes and circuit board side placement. The placement of the sum of all the devices on a single plane presented results where the EMI increased due to an effectively larger semiconductor PAD area as discussed in section 6.6.1. The placement of half the semiconductor devices in differing planes or sides as with Boards 3 and 4 showed significantly less EMI predominantly in CM EMI.

The Geometric Symmetry of Board 4 with reference to Figure 4-21 presents a situation where during half-cycle operation as in Figure 3-12, only two semiconductor devices are conducting and hence current only flows through two of the four devices. The implementation of Board 4 as in Figure 4-21 presents a situation where during either the positive half-cycle or negative half-cycle of the converter, current only flows on either the Component or Copper side of the PCB respectively. In turn the Drain PAD of the semiconductors only on the Component side or only the Copper side are conducting PAD's. From an EMI perspective (CM especially) the presence of the PAD's of the semiconductor devices on the non-conducting side may present a coupling surface for the PAD's of the conductive devices. The proposition is such that the CM couples from the conducting semiconductor device to the non-conducting semiconductor device and hence forces the CM currents to circulate within the circuit, which prevents the currents from propagating outwards and increasing EMI.

In addition, Geometric symmetry reduces EMI due to requiring operational currents to flow in an identical path and hence travel identical path-lengths for both positive and negative half-cycles, in hope of creating identical EMI waveforms for both the positive and negative half-cycles. In reference to antenna theory, when creating stacked dipoles to achieve larger gain antennas known as phased arrays [24], the path-length of the conductors to each dipole must be identical in length as to achieve identical phase from each element and achieve maximum power output. The effects of transmission lines therefore with respect to antenna theory are applicable to Geometric Symmetry such as the reduction of reflected power leads to greater throughput. In Geometric Symmetry, these such effects may lead to a reduction of EMI. Similarly in [23], mismatch or skew is a large contributor to CM EMI and hence a Geometrically Balanced layout removes the imbalance due to path-length variations between semiconductor devices. The identical path-lengths allow the signal or power to reach the semiconductors in an identical amount of time (transmission line effects are evident) reducing mismatch or skew as the path distances are identical. The operational currents are therefore relatively unaltered in their rise and fall times due to path length differences and hence semiconductor rise and fall time mismatch becomes the main skew or mismatch contributor.

An additional factor affecting general EMI levels is the distance between the converter and a ground-plane which in the case of a product is normally the chassis of the product. Cognisance of the effects of distance between the chassis and converter should be considered during the design phase of a product as the knowledge of the effects aid in the reduction on EMI, predominantly CM EMI.

In conclusion, Board 4's relatively better performance in both CM and DM is of the direct result of:

1. Absence of copper pour areas
2. Low self inductance through physically small H-bridge circuit size
3. Semiconductor orientation and placement
4. Geometric Symmetry

The points noted above are responsible for the relatively better performance of Board 4 in contrast to the other Boards. However identifiable the generation mechanisms of EMI are, in most cases too many mechanisms operate concurrently which can obscure the exact generation mechanism.

Due to the multiple variables present and the often abstract generation mechanisms of EMI, it is often the lack of identification or knowledge of the major generation mechanisms which results in Engineers labelling EMI as a *"Dark Art"*.

## 7.2 FUTURE WORK

The following section highlights various avenues which require further investigation either on the work presented or additional discovered phenomena during the study.

### *7.2.1 Investigate MOSFET Driver Noise*

The presence of both DM and CM EMI throughout the results during the unloaded tests of the DUT's presents a significant result due to the large presence of EMI. The continued investigation into determining the root generation mechanisms of MOSFET Driving and EMI generation would significantly contribute to the understanding of EMI generation mechanisms. The amount of EMI generated through MOSFET Driving significantly added to EMI levels and therefore needs to be considered during converter design and implementation phases. The possible generation mechanisms of MOSFET Driving have been discussed within section 6.7 which requires further investigation and verification.

### *7.2.2 Development of a Schematically Balanced Boost Converter*

The schematic structure of a boost converter does not present an easily schematically balanced structure. No such reference to a Schematically Balanced boost converter was presented in [9].

Presented below in Figure 7-1 is a possible implementation of the Schematic Balance of a boost converter circuit with which further investigation is required to determine whether the balance produces mitigated EMI results.

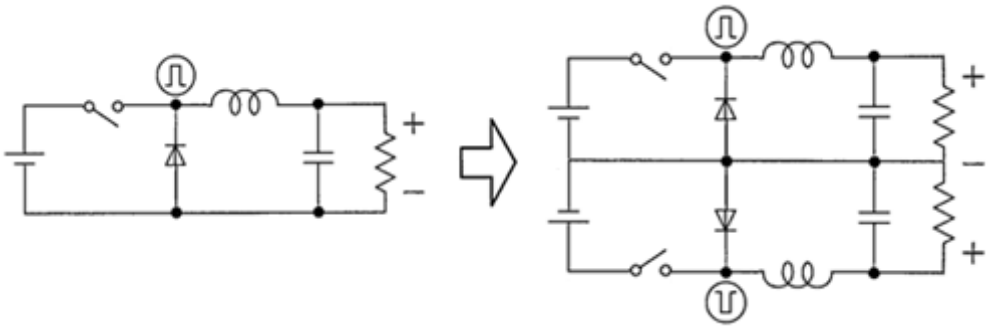


**Figure 7-1 Unbalanced to Balanced Boost Converter**

### *7.2.3 Geometrically Balancing an Unnaturally Schematically Balanced Circuit*

The experimental work presented throughout the dissertation was conducted on a naturally schematically balanced circuit which lead itself to Geometric Symmetry.

Further investigations are warranted firstly into Schematically Balancing other circuit topologies (i.e. a boost converter) as Schematic Balance aids in the design process and EMI mitigation. Secondly determining whether Geometrically Balancing the said circuit achieves Geometric Symmetry produces significantly better EMI results.

### *7.2.4 Root Cause of Geometric Symmetry Reducing EMI Generation Mechanisms*

An extensive and detailed analysis of the root mechanisms as to why Geometric Symmetry produces significantly better EMI results over other counterparts, as the work required to determine the root mechanisms falls beyond the scope of the dissertation.

A hypothesis relating to identical path-lengths and transmission line theory has been put forward regarding the mitigation of EMI from Geometrically Balanced converters in addition to other effects, which requires extensive research and testing in order to identify the exact mechanisms of generation.

### *7.2.5 Mutual Inductance*

An investigation pertaining to the possible effects of mutual inductance on firstly DM EMI as experienced within the experimental section. A conclusive investigation into the mechanisms involved and the effects on DM would benefit in the understanding of additional EMI generation mechanisms, which in turn aids the design process especially when a converter is placed within a metal enclosure.

The second effect which requires investigation is the possible effect mutual inductance has between the power wires and the MOSFET Driving signal wires. An investigation into whether the change in height during the experimentation caused a change in mutual inductance between the said cables and therefore a change in coupling between the devices involved and hence the EMI measured.

# 8 APPENDICES

## 8.1 APPENDIX A

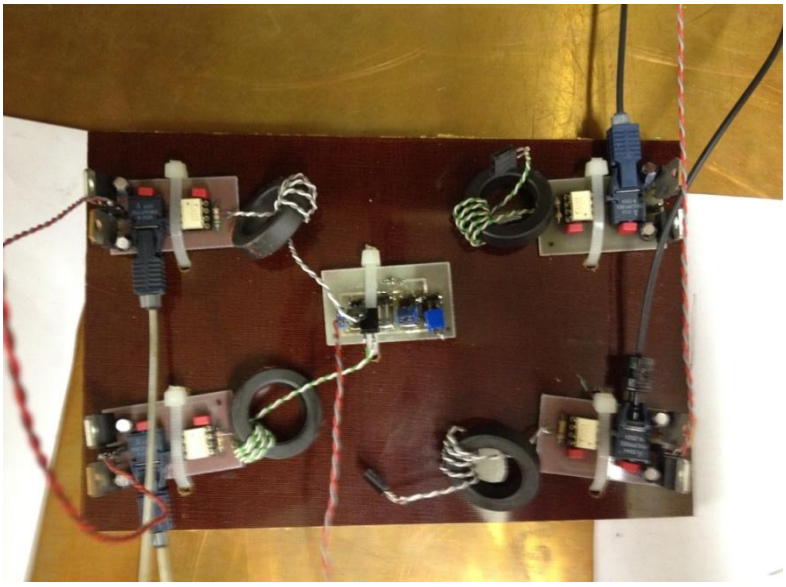


**Figure 8-1 TLP250 MOSFET Driver Experimental Setup**

## 8.2 APPENDIX B

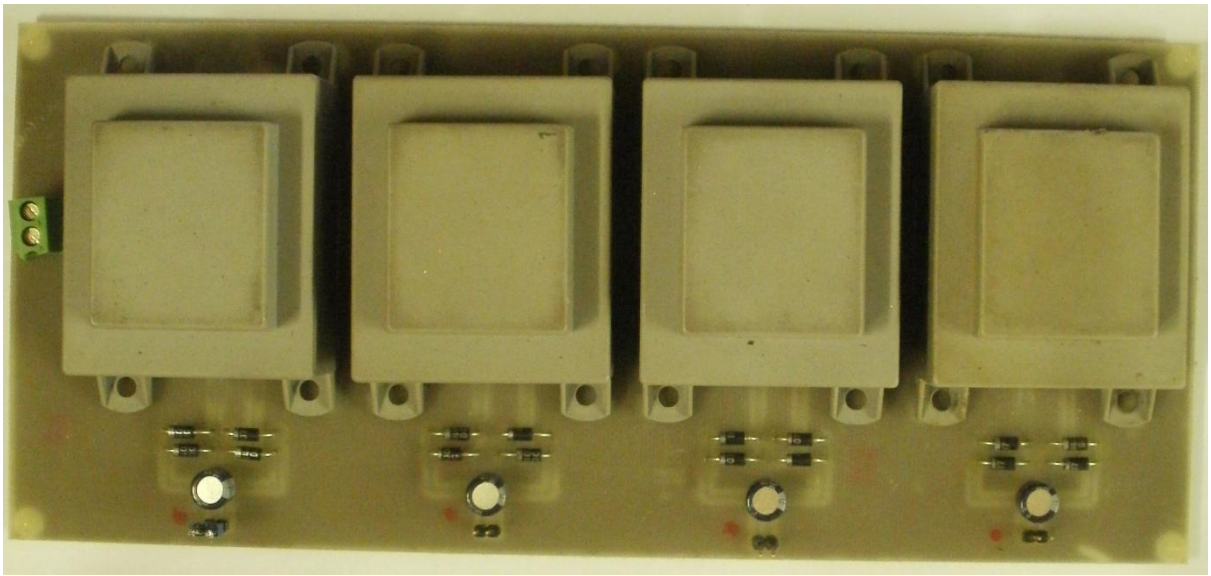


**Figure 8-2 4 Isolated Power Supplies**

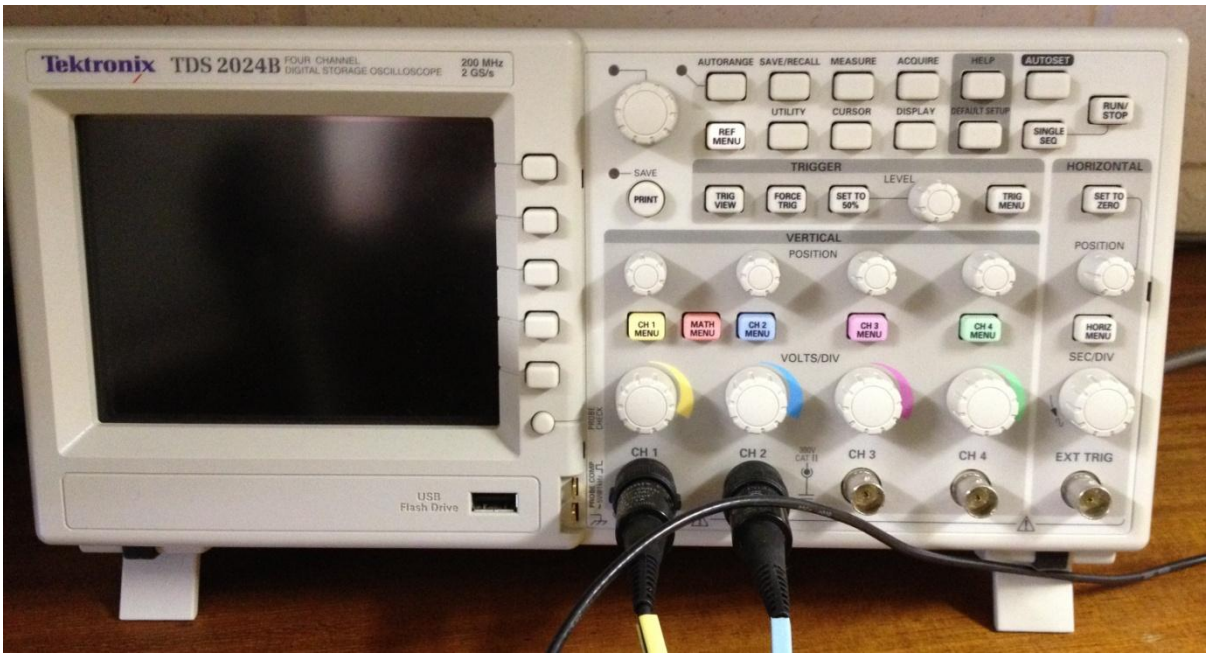


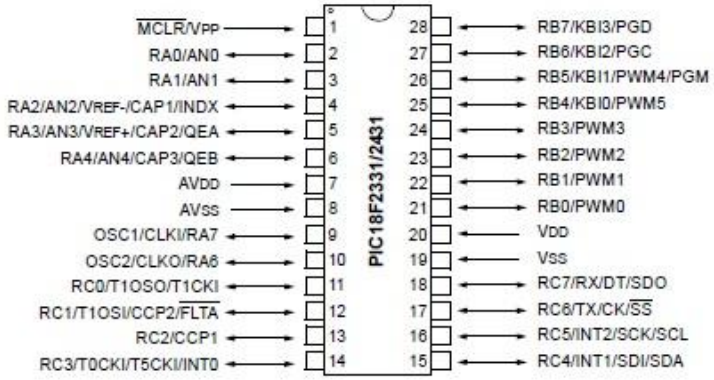

**Figure 8-3 Tektronix TDS 2024B Oscilloscope**

## 8.3 APPENDIX C

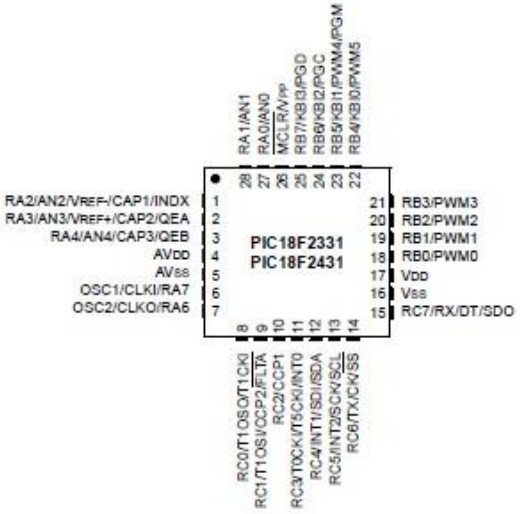
# PIC18F2331/2431/4331/4431

### Pin Diagrams

**28-Pin SPDIP, SOIC**




**28-Pin QFN(1)**




**Note 1:** For the QFN package, it is recommended that the bottom pad be connected to Vss.

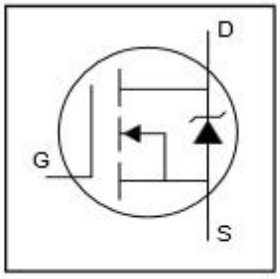
International
IOR Rectifier

PD - 91341B

# IRF540N

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated




$V_{DSS}$ = 100V

$R_{DS(on)}$ = 44mΩ

$I_D$ = 33A

## Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

TO-220AB

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 33 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 23 | |
| $I_{DM}$ | Pulsed Drain Current ① | 110 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 130 | W |
| | Linear Derating Factor | 0.87 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $I_{AR}$ | Avalanche Current① | 16 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | 13 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 7.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |
| | Mounting torque, 6-32 or M3 srew | 10 lbf•in (1.1N•m) | |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | — | 1.15 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 62 | |

# IRF540N

International
IOR Rectifier

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.12 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 44 | mΩ | $V_{GS}$ = 10V, $I_D$ = 16A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $g_{fs}$ | Forward Transconductance | 21 | — | — | S | $V_{DS}$ = 50V, $I_D$ = 16A④ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 25 | µA | $V_{DS}$ = 100V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 80V, $V_{GS}$ = 0V, $T_J$ = 150°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | — | — | 71 | nC | $I_D$ = 16A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 14 | | $V_{DS}$ = 80V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 21 | | $V_{GS}$ = 10V, See Fig. 6 and 13 |
| $t_{d(on)}$ | Turn-On Delay Time | — | 11 | — | ns | $V_{DD}$ = 50V |
| $t_r$ | Rise Time | — | 35 | — | | $I_D$ = 16A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 39 | — | | $R_G$ = 5.1Ω |
| $t_f$ | Fall Time | — | 35 | — | | $V_{GS}$ = 10V, See Fig. 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | |
| $C_{iss}$ | Input Capacitance | — | 1960 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 250 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 40 | — | | $f$ = 1.0MHz, See Fig. 5 |
| $E_{AS}$ | Single Pulse Avalanche Energy② | — | 700⑤ | 185⑥ | mJ | $I_{AS}$ = 16A, L = 1.5mH |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 33 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode)① | — | — | 110 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.2 | V | $T_J$ = 25°C, $I_S$ = 16A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 115 | 170 | ns | $T_J$ = 25°C, $I_F$ = 16A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 505 | 760 | nC | di/dt = 100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J$ = 25°C, L =1.5mH $R_G$ = 25Ω, $I_{AS}$ = 16A. (See Figure 12)

③ $I_{SD}$ ≤ 16A, di/dt ≤ 340A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to $T_J$ = 175°C .

International
IOR Rectifier

Data Sheet No. PD60147 rev.U

# IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

## HIGH AND LOW SIDE DRIVER

### Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

### Product Summary

| | |
|---|---|
| $V_{OFFSET}$ (IR2110) | 500V max. |
| (IR2113) | 600V max. |
| $I_O$+/- | 2A / 2A |
| $V_{OUT}$ | 10 - 20V |
| $t_{on/off}$ (typ.) | 120 & 94 ns |
| Delay Matching (IR2110) | 10 ns max. |
| (IR2113) | 20ns max. |

### Packages

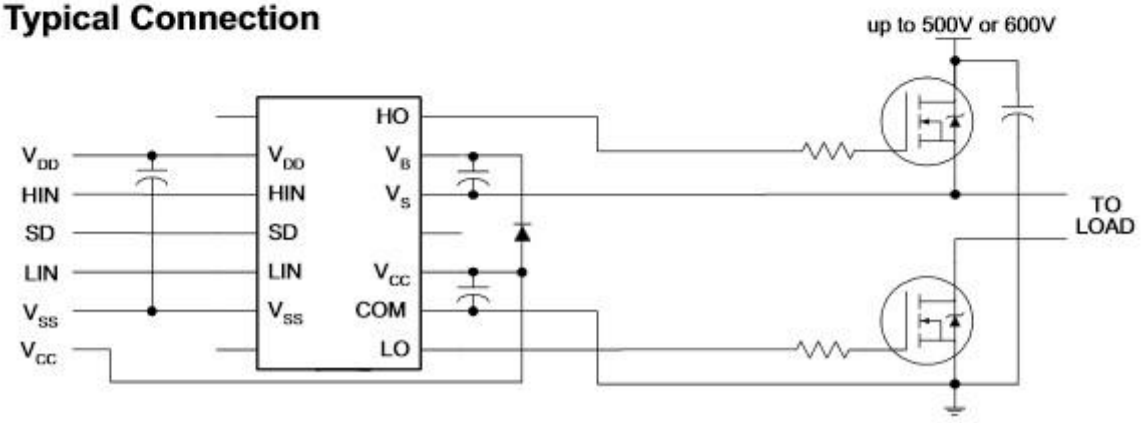
14-Lead PDIP
IR2110/IR2113

16-Lead SOIC
IR2110S/IR2113S

### Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

### Typical Connection




(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

**TOSHIBA** TLP250

TOSHIBA Photocoupler GaAlAs Ired & Photo−IC

# TLP250

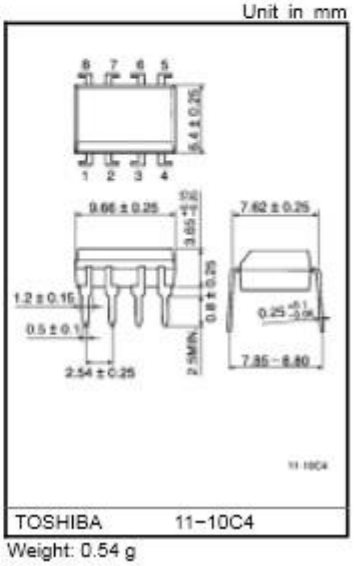
Transistor Inverter
Inverter For Air Conditionor
IGBT Gate Drive
Power MOS FET Gate Drive

The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
This unit is 8−lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: $I_F$=5mA(max.)
- Supply current ($I_{CC}$): 11mA(max.)
- Supply voltage ($V_{CC}$): 10−35V
- Output current ($I_O$): ±1.5A (max.)
- Switching time ($t_{pLH}/t_{pHL}$): 1.5μs(max.)
- Isolation voltage: 2500$V_{rms}$(min.)
- UL recognized: UL1577, file No.E67349
- Option (D4) type
  VDE approved: DIN VDE0884/06.92,certificate No.76823
  Maximum operating insulation voltage: 630$V_{PK}$
  Highest permissible over voltage: 4000$V_{PK}$

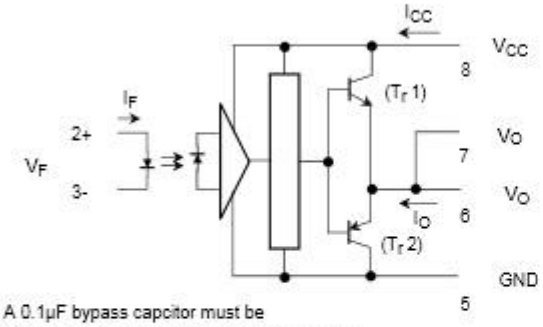
  **(Note) When a VDE0884 approved type is needed, please designate the "option (D4)"**
- Creepage distance: 6.4mm(min.)
  Clearance: 6.4mm(min.)

Unit in mm



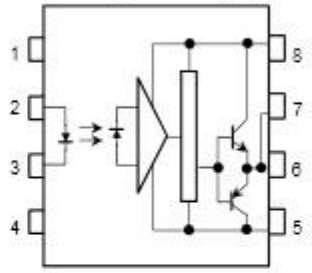

TOSHIBA 11−10C4
Weight: 0.54 g

## Schmatic




A 0.1μF bypass capcitor must be connected between pin 8 and 5 (See Note 5).

## Pin Configuration (top view)




1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : $V_O$ (Output)
7 : $V_O$
8 : $V_{CC}$

## Truth Table

| | | Tr1 | Tr2 |
|---|---|---|---|
| Input LED | On | On | Off |
| | Off | Off | On |

# HFBR-0501 Series
## Versatile Link
## The Versatile Fiber Optic Connection

AVAGO TECHNOLOGIES

## Data Sheet

### Description

The Versatile Link series is a complete family of fiber optic link components for applications requiring a low cost solution. The HFBR-0501 series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The optical link design is simplified by the logic compatible receivers and complete specifications for each component. The key optical and electrical parameters of links configured with the HFBR-0501 family are fully guaranteed from 0° to 70° C.

A wide variety of package configurations and connectors provide the designer with numerous mechanical solutions to meet application requirements. The transmitter and receiver components have been designed for use in high volume/low cost assembly processes such as auto insertion and wave soldering.

Transmitters incorporate a 660 nm LED. Receivers include a monolithic DC coupled, digital IC receiver with open collector Schottky output transistor. An internal pullup resistor is available for use in the HFBR-25X1/2/4 receivers. A shield has been integrated into the receiver IC to provide additional, localized noise immunity.

Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all connector interface losses. Therefore, optical calculations for common link applications are simplified.

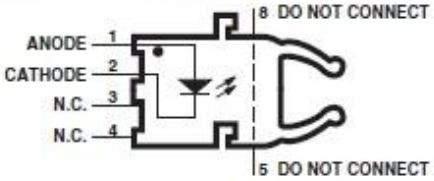
### Features

- Low cost fiber optic components
- Enhanced digital links DC -5 MBd
- Extended distance links up to 120 m at 40 kBd
- Low current link: 6 mA peak supply current
- Horizontal and vertical mounting
- Interlocking feature
- High noise immunity
- Easy connectoring Simplex, Duplex, and Latching connectors
- Flame retardant
- Transmitters incorporate a 660 nm Red LED for easy visibility
- Compatible with standard TTL circuitry

### Applications

- Reduction of lightning/voltage transient susceptibility
- Motor controller triggering
- Data communications and local area networks
- Electromagnetic Compatibility (EMC) for regulated systems: FCC, VDE, CSA, etc.
- Tempest-secure data processing equipment
- Isolation in test and measurement instruments
- Error free signalling for industrial and manufacturing equipment
- Automotive communications and control networks
- Noise immune communication in audio and video equipment

## HFBR-15X3 Transmitter




| Pin # | Function |
|---|---|
| 1 | Anode |
| 2 | Cathode |
| 3 | Open |
| 4 | Open |
| 5 | Do not connect |
| 8 | Do not connect |

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

### Absolute Maximum Ratings

| Parameter | | Symbol | Min. | Max. | Units | Reference |
|---|---|---|---|---|---|---|
| Storage Temperature | | $T_S$ | -40 | +85 | °C | |
| Operating Temperature | | $T_A$ | -40 | +85 | °C | Note 1 |
| Lead Soldering Cycle | Temp. | | | 260 | °C | |
| | Time | | | 10 | sec | |
| Forward Input Current | | $I_{FPK}$ | | 1000 | mA | Note 2, 3 |
| | | $I_{Fdc}$ | | 80 | | |
| Reverse Input Voltage | | $V_{BR}$ | | 5 | V | |

Notes:
1. 1.6 mm below seating plane.
2. Recommended operating range between 10 and 750 mA.
3. 1 µs pulse, 20 µs period.

*All HFBR-15XX LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your local Avago sales representative for more information.*

### Transmitter Electrical/Optical Characteristics 0° C to +70° C unless otherwise specified.

For forward voltage and output power vs. drive current graphs.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions | Ref. |
|---|---|---|---|---|---|---|---|
| Transmitter Output Optical Power | $P_T$ | -11.2<br>-13.6<br>-35.5 | | -5.1<br>-4.5 | dBm | $I_{Fdc}$ = 60 mA, 25° C<br>$I_{Fdc}$ = 60 mA<br>$I_{Fdc}$ = 2 mA, 0-70° C | Notes 3, 4<br>Fig. 9, 10 |
| Output Optical Power Temperature Coefficient | $\Delta P_T/\Delta T$ | | -0.85 | | %/°C | | |
| Peak Emission Wavelength | $\lambda_{PK}$ | | 660 | | nm | | |
| Forward Voltage | $V_F$ | 1.45 | 1.67 | 2.02 | V | $I_{Fdc}$ = 60 mA | |
| Forward Voltage Temperature Coefficient | $\Delta V_F/\Delta T$ | | -1.37 | | mV/°C | | Fig. 18 |
| Effective Diameter | D | | 1 | | mm | | |
| Numerical Aperture | NA | | 0.5 | | | | |
| Reverse Input Breakdown Voltage | $V_{BR}$ | 5.0 | 11.0 | | V | $I_{Fdc}$ = 10 µA, $T_A$ = 25° C | |
| Diode Capacitance | $C_O$ | | 86 | | pF | $V_F$ = 0, f = MHz | |
| Rise Time | $t_r$ | | 80 | | ns | 10% to 90%, $I_F$ = 60 mA | Note 1 |
| Fall Time | $t_f$ | | 40 | | ns | | |

Notes:
1. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 Ω load. A wide bandwidth optical to electrical waveform analyzer, terminated to a 50 Ω input of a wide bandwidth oscilloscope, is used for this response time measurement.

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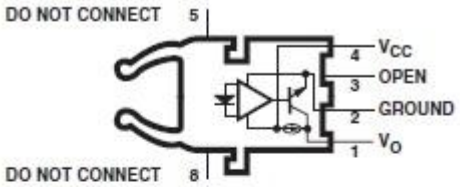
## HFBR-25X3 Receiver




| Pin # | Function |
|---|---|
| 1 | $V_O$ |
| 2 | Ground |
| 3 | Open |
| 4 | $V_{CC}$ |
| 5 | Do not connect |
| 8 | Do not connect |

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

### Absolute Maximum Ratings

| Parameter | | Symbol | Min. | Max. | Units | Reference |
|---|---|---|---|---|---|---|
| Storage Temperature | | $T_S$ | -40 | +85 | °C | |
| Operating Temperature | | $T_A$ | -40 | +85 | °C | |
| Lead Soldering Cycle | Temp. | | | 260 | °C | Note 1 |
| | Time | | | 10 | sec | |
| Supply Voltage | | $V_{CC}$ | -0.5 | 7 | V | Note 2 |
| Average Output Collector Current | | $I_O$ | -1 | 5 | mA | |
| Output Collector Power Dissipation | | $P_{OD}$ | | 25 | mW | |
| Output Voltage | | $V_O$ | -0.5 | 7 | V | |

Notes:
1. 1.6 mm below seating plane.
2. It is essential that a bypass capacitor 0.01 µF be connected from pin 2 to pin 3 of the receiver.

### Receiver Electrical/Optical Characteristics 0° C to 70° C, 4.5 V ≤ $V_{CC}$ ≤ 5.5 V unless otherwise specified

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions | Ref. |
|---|---|---|---|---|---|---|---|
| Input Optical Power Level Logic 0 | $P_{R(L)}$ | -39 | | -13.7 | dBm | $V_O = V_{OL}$, $I_{OL}$ = 3.2 mA | Notes 1, 2, 3 |
| | | -39 | | -13.3 | | $V_O = V_{OL}$, $I_{OH}$ = 8 mA, 25° C | |
| Input Optical Power Level Logic 1 | $P_{R(H)}$ | | | -53 | dBm | $V_{OH}$ = 5.5 V $I_{OH}$ = ≤ 40 µA | Note 3 |
| High Level Output Voltage | $V_{OH}$ | 2.4 | | | V | $V_O$ = -40 µA, $P_R$ = 0 µW | |
| Low Level Output Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 3.2 mA, $P_R = P_{R(L)MIN}$ | Note 4 |
| High Level Supply Current | $I_{CCH}$ | | 1.2 | 1.9 | mA | $V_{CC}$ = 5.5 V, $P_R$ = 0 µW | |
| Low Level Supply Current | $I_{CCL}$ | | 2.9 | 3.7 | mA | $V_{CC}$ = 5.5 V $P_R = P_{RL\ (MIN)}$ | Note 4 |
| Effective Diameter | D | | 1 | | mm | | |
| Numerical Aperture | NA | | 0.5 | | | | |

Notes:
1. Measured at the end of the fiber optic cable with large area detector.
2. Optical flux, P (dBm) = 10 Log P(µW)/1000 µW.
3. Because of the very high sensitivity of the HFBR-25X3, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
4. Including current in 3.3 k pull-up resistor.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**



AVAGO TECHNOLOGIES

EMCO™ **800-253-3761** Phone **512-835-4729** Fax

# LISN / PLISN

Models 3625/2, 3725/2M, 3810/2, 3816/2, 3825/2, 3850/2, 3925/2, 3701

FYI

The Model 3810/2 series of Line Impedance Stabilization Networks have been certified by the Canadian Standards Association to be in compliance with CAN/CSA-22.2 No 1010.1-92 (Safety Requirements for Electrical Equipment for Measurement, Control and Laboratory Use). This certification states that the Model 3810/2 series complies with the applicable requirements of the NFPA National Electric Code.

Model 3810/2 LISN

CSA MODEL 3810/2 APPROVED

**Key Features**

- **One Piece, Multi-Line Design for Convenience**
- **Wide Frequency for Broad Measurement**
- **Coils Matched to Application**
- **Insulated Plugs for Safer Power Connections**
- **RF Shielding to Minimize Intrusion**
- **Individually Calibrated**

**EMCO Line Impedance Stabilization Networks (LISNs) and Power Line Impedance Stabilization Networks (PLISNs)** are multi-line low pass filter networks used for conducted emissions measurement. LISNs and PLISNs isolate an electrically powered EUT from the external power source, stabilize line impedance (for repeatable measurements), and provide a 50-ohm RF connection to measure EMI voltage generated by the EUT. When line currents drawn by the EUT are too great for a LISN, EMCO's Model 3701 Line Probe can be used for EMI voltage measurements.

STANDARD CONFIGURATION

- LISN assembly
- 50 Ω external load (three each on Model 3960/4)
- AC line cord adapters (Model 3925/2 and 3960/4 only)
- Superior® pin plug connectors (6)excluding Models 3810, & 3816
- Individually calibrated per ANSI C63.4. Actual factors and a signed Certificate of Calibration Conformance included in manual.

INDIVIDUALLY CALIBRATED

2 YEAR WARRANTY

QUALITY ASSURANCE

**Operational Features**

| MODEL | MANUALLY SWITCHED EARTH LINE CHOKE | EARTH LINE CHOKE | ARTIFICIAL HAND | HIGH PASS FILTER | MANUALLY SWITCHED TEST PORTS | REMOTE SWITCHED TEST PORTS |
|---|---|---|---|---|---|---|
| 3810/2 | Yes | Yes | Yes | No | Yes | No |
| 3816/2 | Yes | Yes | Yes | Yes | Yes | Yes |



E-mail: info@emctest.com World Wide Web: http://www.emctest.com

**800-253-3761** Phone **512-835-4729** Fax

## Physical Specifications

| MODEL | WIDTH | DEPTH | HEIGHT | WEIGHT |
|---|---|---|---|---|
| 3625/2• | 27.9 cm<br>11.0 in | 27.9 cm<br>11.0 in | 16.5 cm<br>6.5 in | 5.4 kg<br>12.0 lb |
| 3725/2M• | 22.2 cm<br>8.7 in | 38.1 cm<br>15.0 in | 15.2 cm<br>6.0 in | 4.9 kg<br>10.7 lb |
| 3810/2 | 22.2 cm<br>8.7 in | 38.1 cm<br>15.0 in | 15.2 cm<br>6.0 in | 4.9 kg<br>10.7 lb |
| 3816/2 | 22.2 cm<br>8.7 in | 38.1 cm<br>15.0 in | 15.2 cm<br>6.0 in | 4.9 kg<br>10.7 lb |
| 3825/2 | 27.9 cm<br>11.0 in | 38.1 cm<br>15.0 in | 21.2 cm<br>8.3 in | 10.4 kg<br>23.0 lb |
| 3850/2• | 51.4 cm<br>20.2 in | 57.1 cm<br>22.5 in | 34.9 cm<br>13.7 in | 20.4 kg<br>45.0 lb |
| 3925/2• | 51.4 cm<br>20.2 in | 47.0 cm<br>18.5 in | 23.5 cm<br>9.2 in | 27.3 kg<br>60.0 lb |
| 3701 | N/A | 21.6 cm<br>8.5 in | N/A | 164.4 g<br>6.0 oz |

TECH tip

LISN's can be used as a coupling device for power line susceptibility testing above 450 kHz. To do this, connect an RF generator to the RF output port and inject the desired voltage (1Vrms for IEC 1000-4-6) onto the power line. Your EUT should be connected to the LISN as it normally is for emissions testing. Monitor your EUT for indications of abnormal operation indicating susceptibility failure. While this set up isn't appropriate for compliance testing, it will help identify a severe problem.

## Electrical Specifications

| MODEL | POWER OUT CONNECTOR | POWER IN CONNECTOR | LINES PLUS GROUND | FREQUENCY RANGE | POWER SOURCE FREQUENCY | MAXIMUM CURRENT | MAXIMUM VOLTAGE | NETWORK INDUCTANCE IMPEDANCE |
|---|---|---|---|---|---|---|---|---|
| 3625/2• | Superior® Plug | Superior® Plug | 2 | 100 kHz – 65 MHz | DC – 400 Hz | 25 A | 400 VAC Line – Line<br>220 VAC Line to Ground | 5 µH, 50 Ω |
| 3725/2M• | Insulated Binding Posts | Binding Posts | 2 | 10 kHz – 100 MHz | DC – 400 Hz | 25 A | 220 VAC Line to Ground | 50 µH, 50 Ω |
| 3810/2 | NEMA<br>SCHUKO<br>British | IEC Power inlet<br>with customer<br>specified cordset | 2<br>2<br>2 | 9 kHz – 30 MHz<br>9 kHz – 30 MHz<br>9 kHz – 30 MHz | 60 Hz<br>50 Hz<br>50 Hz | 10 A<br>10 A<br>10 A | 125 VAC Line to Ground<br>250 VAC Line to Ground<br>250 VAC Line to Ground | 50 µH/250 µH, 50 Ω<br>50 µH/250 µH, 50 Ω<br>50 µH/250 µH, 50 Ω |
| 3816/2 | NEMA<br>SCHUKO<br>British | Integral cord<br>with customer<br>specified cordset | 2<br>2<br>2 | 9 kHz – 30 MHz<br>9 kHz – 30 MHz<br>9 kHz – 30 MHz | 60 Hz<br>50 Hz<br>50 Hz | 15 A<br>16 A<br>16 A | 125 VAC Line to Ground<br>250 VAC Line to Ground<br>250 VAC Line to Ground | 50 µH/250 µH, 50 Ω<br>50 µH/250 µH, 50 Ω<br>50 µH/250 µH, 50 Ω |
| 3825/2 | Superior® Plug | Superior® Plug | 2 | 9 kHz – 100 MHz | DC – 60 Hz | 25 A | 400 VAC Line – Line<br>220 VAC Line to Ground | 50/250 µH, 50 Ω |
| 3850/2• | Superior® Plug | Superior® Plug | 2 | 9 kHz – 100 MHz | DC – 60 Hz | 50 A | 400 VAC Line – Line<br>220 VAC Line to Ground | 50/250 µH, 50 Ω |
| 3925/2• | Type N female<br>AC Adapter | Superior® Plug | 2 | 5 kHz –1000MHz | DC – 60 Hz | 20 A | 400 VAC Line – Line<br>220 VAC Line to Ground | 50 Ω |
| 3701 | N/A | Clip Lead | N/A | 10 kHz – 30 MHz | | | 400 VAC Line – Line | N/A |

• Specialty Item. Call EMCO for lead time and pricing.

# Specifications

Specifications are valid under the following conditions: 15 minutes warm-up time at ambient temperature, specified environmental conditions met and calibration cycle adhered to. Data without tolerances: typical values. Data designated as "nominal": design parameters, i.e. not tested.

| Specification | Condition | R&S FSH3 | R&S FSH6 | R&S FSH18 |
|---|---|---|---|---|
| Frequency | | | | |
| Frequency range | | 100 kHz to 3 GHz | 100 kHz to 6 GHz | 10 MHz to 18 GHz |
| Reference frequency | | | | |
| Aging | | 1 ppm/year | | |
| Temperature drift | 0 °C to 30 °C<br>30 °C to 50 °C | 2 ppm<br>in addition 2 ppm/10°C | | |
| Frequency counter | | | | |
| Resolution | | 1 Hz | | |
| Frequency span | | 0 Hz, 100 Hz to 3 GHz | 0 Hz, 100 Hz to 6 GHz | 0 Hz, 100 Hz to 18 GHz |
| | 1145.5850.13 | 0 Hz, 1 kHz to 3 GHz | - | - |
| **Spectral purity**<br>SSB phase noise | f = 500 MHz, 20 to 30 °C | | | |
| 30 kHz from carrier | | <-85 dBc/(1 Hz) | | <-85 dBc/(1 Hz) |
| 100 kHz from carrier | | < -100 dBc/(1 Hz) | | < -90 dBc/(1 Hz) |
| 1 MHz from carrier | | < -120 dBc/1 Hz) | | < -100 dBc/(1 Hz) |
| Sweep time | span = 0 Hz | 1 ms to 100 s | | |
| | span > 0 Hz | 20 ms to 1000 s, min. 20 ms/600 MHz | | |
| Bandwidths | | | | |
| Resolution bandwidths (-3 dB) | 1145.5850.13 | 1, 3, 10, 30,100, 200, 300 kHz, 1 MHz | | |
| | 1145.5850.03, .23,<br>1145.5850.06, .26, .18 | In addition 100, 300 Hz | | |
| Tolerance | ≤ 300 kHz | ± 5 %, nominal | | |
| | 1 MHz | ± 10 %, nominal | | |

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