Evaluation and Implementation of Cyclic Permutation Coding for Power Line Communications

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***Abstract*—Noise and attenuation, in the form of frequency disturbance, impulsive noise, additive white Gaussian noise (AWGN) and frequency selective fading, are the major setbacks in power line communications (PLC). In order to effectively combat this challenge, we thus report the development and implementation of a specially coded M-ary differential phase shift keying modulation scheme on narrowband PLC channel. The coding aspect involves the concatenation of conventional Reed Solomon (RS) code with cyclic permutation coding (CPC), resulting in what is termed RS-CPC scheme. The CPC employed in this work maps the output bits of a binary RS code onto non-binary CPC symbols, in a cyclic manner, with a view to improving the distance between two different sets of mapped symbols. For implementation over 230 V AC power line, software defined radio hardware, called the universal software radio peripherals (USRPs), were used, together with narrowband coupling circuits, to couple the signal to and receive it from the power line. Both by simulation and implementation, our scheme outperforms the conventional Reed Solomon-convolutional coding (RS-CC) specified in the G3-PLC standard. An added advantage is that our scheme is easier to implement.**

***Keywords*—Channel coding; Cyclic Permutation Coding; DPSK modulation; G3-PLC; Power Line Communications; PRIME; Software Defined Radio; USRP**

I. Introduction

Low voltage power line is gaining considerable attention as an alternative means of communication, especially for home networking, Internet access, electric vehicle-to-charging stations, smart metering and data distribution. PLC in homes may be cost effective in terms of implementation, because, it makes use of the already existing power network. However, PLC channels are plagued with various kinds of signal attenuation and noise in forms of addtive white Gaussian noise (AWGN), frequency selective fading, narrowband interference (NBI), and impulsive noise (IN), which make it very unstable and hostile to information transmission [1], [2]. AWGN exists over the entire frequency region in the spectrum. It features as a result of random processes such as the flow of charges and thermal vibrations. These phenomenon are normal for any material whose temperature is above absolute zero. NBI arises, when there are interferences emanating from the connected equipments, whose operating frequencies are in the same range as the PLC system. It appears in a narrow portion of the operating spectrum, with time dependent amplitudes above the AWGN floor level [3]. IN has a flat broadband power spectral density, which can result into a multiple of large envelopes [4]–[5]. It sometimes affects multiple frequency components of the transmitted data, at a particular duration.

Orthogonal frequency division multiplexing (OFDM) is the future of PLC, because it is able to combat most of these kinds of noise. The two PLC narrowband standards (i.e. G3-PLC and PRIME) have suggested M-ary differential phase shift keying (MDPSK) as a component of OFDM in their specifications [6], [7]. As such, this work has chosen to implement and evaluate MDPSK, but equipped with RS-CPC coding scheme, so as to contribute to the developments of the two standards.

Although, MDPSK has been implemented on PLC, as reported in [8], but it was in the MHz range. More so, there is no report on its combination with CPC, as far as we know. A recent report on the use of a QPSK-OFDM scheme in combating NBI, is contained in [4] and [9], where RS code is concatenated with non-cyclic permutation coding (PC). Their scheme is seen to have close performance with the conventional RS-CC-OFDM scheme, with the advantage of less complexity. However, the scheme is still at simulation level. Differential modulation schemes (like DQPSK) have been practically demonstrated to be superior in almost all PLC channels [7]. Wetz *et al*. [10] have as well demonstrated the strength of differential modulation, by simulation, in their OFDM-MFSK scheme. The work presented here entails the development and practical implementation of RS-CPC-DQPSK scheme on a low voltage (230 V AC) PLC channel, using USRP, a general purpose software defined radio (SDR) based hardware from Ettus Research. With SDR, communication engineers have the opportunity of configuring the hardware to suit their applications and channel requirements. Here, all the signal processing, which include filtering, modulation, amplification, etc., are done with a compatible software (e.g., GNU Radio, Labview or MATLAB-Simulink Target), while the hardware handles only the digital and analogue conversions, together with some form of interpolation and decimation.

Our contribution in this research is therefore to present the development and implementation of an RS-CPC-DQSK scheme, over PLC channel- the first implementation of its kind, to the best of our knowledge. This implies that our work is not only simulation based, as most work is, but its practical implementation is also presented. The simulation and practical implementation carried out shows how PLC noise and

disturbances can be substantially mitigated, using the proposed scheme. It is worth knowing that the proposed scheme is of a low coding rate, as will be discovered later. However, such a scheme finds application in wide area applications such as the low speed communications used for command and control in the smart grid (SG), where reliability, security, safety, and operational efficiency are of key importance [11], [12]. The essence of command and control in SG is usually for load management and automatic meter reading applications. Since these applications can operate at several thousand bits per seconds, which is in the low speed range, narrowband PLC can be used to accomplish their purposes [13]. In order to ensure fair performance comparisons, coding rate compensations were enforced on all the conventional schemes that were compared with the proposed scheme.

In Section II, we describe channel coding schemes, with emphasis laid on PC. More so, the error correcting capability of PC is discussed therein, with a detailed analysis of how a CPC can outperform an ordinary PC. Section III is dedicated to the description of the proposed RS-CPC-DQPSK scheme, including the encoding and decoding procedures, with much emphasis laid on the CPC algorithms. The experimental setup of the work done is detailed in Section IV. We then present some simulation and practical results in Section V and a concluding note in Section VI.

II. Channel Coding Schemes

Channel coding is a process of signal transformation to improve its performance when plagued with channel impairments like noise, jamming and fading [14]. This is usually referred to as forward error correction (FEC). As explained in [2], mapping or coding can be considered as mathematical manipulation that can be applied to digital information, since it is made up of streams of zeroes (0) and ones (1), all put together to form a digital word. This mathematical manipulation therefore helps to improve the reliability of the system. There are various types of coding schemes, with different complexities and capabilities. Examples include CC, PC and RS codes. RS codes are known to perform well in the presence of burst noise, which may stay for some appreciable duration of bits in the communication channel [14], especially the power line. More than one type of coding scheme can be concatenated to achieve better performance (as done in our work).

Since PC is the channel coding of interest in this study, emphasis shall be laid on it, while detailed studies into other coding schemes such as RS and CC can be found in [1], [14] and [15].

A. Permutation coding

As presented in [16], a PC can be defined in three different ways as either

- an ordered arrangement of a subset of objects, r taken from a parent set, M:

$$^{M}P_r = \frac{M!}{(M-r)!}, \tag{1}$$

- an arrangement of every element in a finite sequence, or
- a bijection of a finite or infinite set to itself. For example, mapping the upper symbols to the bottom symbols in the matrix given by:

$$\left\{ \begin{array}{cccccccc} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 5 & 7 & 6 & 1 & 4 & 2 & 8 & 3 \end{array} \right\}. \tag{2}$$

In the context of this work, a PC is the representation of binary data in non-binary sequence of codewords, each containing M symbols, with each symbol appearing only once in a codeword. Permutation block coding and permutation arrays have been known for some time, as reported in [17] and [18]. However, constructing a long block permutation code poses a difficult computational challenge, and most especially, there is no general decoding algorithm for such codes. As such, permutation trellis coding (PTC) was introduced in [19], in order to solve this challenge. In PTC, PC is used as an inner coding, while a base CC is used as an outer coding. A typical PTC mapping is what is depicted as follows:

$$\left\{ \begin{array}{cccc} 00 & 01 & 10 & 11 \\ \downarrow & \downarrow & \downarrow & \downarrow \\ 0123 & 1230 & 2301 & 3012 \end{array} \right\} \tag{3}$$

Here, two convolutional bits, are mapped onto 4 permutation symbols. The permutation arrangement is made cyclic, hence the term cyclic permutation coding (CPC). This kind of mapping ensures that the distance between two sets of initial/base codewords is increased. The benefit of this arrangement shall be discussed in Section II-B.

Ever since Vinck [20] proposed the use of PC for PLC purposes, it has never seen the light of implementation. We have, therefore, achieved that in this particular study. In our implementation, we employ a binary RS code as an outer coding, while CPC is the inner coding. As such, we have a concatenated RS-CPC system.

B. Error correcting capability of permutation coding

Various reports have been given concerning the capability of permutation coding in correcting PLC channel associated errors, such as IN, NBI and background noise [1], [5], [19], [21], [22]. Hamming distance relationship between PC sequences is one major criteria for evaluating the capability of a PC in handling noise. The larger the Hamming distance, the stronger the code is, in terms of error correction. As reported in [23], all the possible Hamming distances in a PC scheme contribute to its performance. For instance, according to (3), the only possible Hamming distance is 4, which appears 12 times in the distance relationship among the codewords. This means distances 1, 2 and 3 have no contribution. With this, we can respectively compute the probability of these distances as:

$$P_1 = P_2 = P_3 = 0/12 \quad \text{and} \quad P_4 = 12/12, \tag{4}$$

where P_h is the probability of distance h. Note that distances between each codeword and itself are not considered. Since P_4 has the largest share of the distance probability, the CPC's error correcting capability tends to rely mostly on distance 4.

We use the RS-PC-OFDM scheme reported in [4], [9] as the basis for evaluating the better performance of our scheme,

over the conventional RS-CC-DQPSK scheme specified in the G3-PLC standard. This scheme was demonstrated, by simulations, to have relatively similar patterns of behaviour as the conventional RS-CC-OFDM scheme [4], under various channel conditions. The PC codewords used in the RS-PC-OFDM scheme is shown in (5) [9].

$$\left\{ \begin{array}{cccccc} 1234 & 1423 & 1342 & 1111 & 2143 & 2314 \\ 2431 & 2222 & 3124 & 3412 & 3241 & 3333 \\ 4132 & 4213 & 4321 & 4444 & & \end{array} \right\} \quad (5)$$

Using the same notion of the distance relationship, this PC has distances 3 and 4, which appear 192 times and 48 times, respectively, with distances 1 and 2 having no contribution. With this, the distance probabilities are respectively given by:

$$P_1' = P_2' = 0/240, P_3' = 192/240 \text{ and } P_4' = 48/240. \quad (6)$$

Here, the PC's strength relies on distance 3, since P_3' has the largest share of the distance probability. Hence, from these analyses, CPC will theoretically perform better than the ordinary PC used in [4] and [9]. We can therefore infer that RS-CPC-DQPSK scheme has better performance than the conventional RS-CC-DQPSK scheme, because RS-PC-OFDM has been previously demonstrated to have a similar behaviour as that of RS-CC-OFDM [4], [9]. This shall be validated later in our simulation results.

Another yardstick for defining the capability of PCs in handling PLC noise, is the parameter termed, d_{min}, which is defined as the minimum Hamming distance between any pair of code sequences in a codebook. As stated in [1], a number of symbol errors that are $d_{\text{min}} - 1$, can be detected by a PTC system. In the CPC sequence employed in our scheme, $d_{\text{min}} = 4$, while for the ordinary PC in [4] and [9], $d_{\text{min}} = 3$. This means that the CPC is capable of detecting 3 symbol errors, while the PC can detect only 2.

III. The RS-CPC-DQPSK transceiver system

A complete RS-CPC-DQPSK transceiver system used for this work is illustrated in Fig. 1. A non-binary DQPSK modulator is employed as the modulation scheme. Our main focus is on the RS-CPC encoder and decoder segments, which are briefly explained in Sections III-A and III-B respectively. Indepth studies on MDPSK modulation and demodulation schemes can be accessed in [24] and [25].

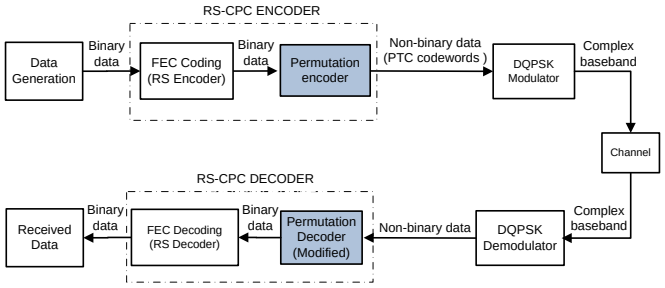

Fig. 1. A complete RS-CPC-DQPSK transceiver. The upper section of the figure represents the transmitter section, while the lower section is the receiver section

A. The RS-CPC encoder

The encoder section comprises of (32, 24) RS code and CPC encoders. This RS code is considered in order to match the error correcting capability of the (247, 255) RS code specified in the G3-PLC standard [6]. The information bit is mapped onto N number of RS bits, which are latter mapped onto PC symbols, using the following CPC algorithm:

Cyclic symbol mapping algorithm:

1) Bits grouping: Group the RS coded bits into sets of n, where n is the number of bits to be mapped onto 1 CPC codeword, with length M. In this case, $n = 2$ and $M = 4$.
2) Binary to decimal conversion: Convert each set of n bits into its corresponding decimal values, and denote it as D_i, where $i = \{1, 2, \ldots, N/n\}$.
3) Codeword selection: From the CPC codebook, select a codeword, whose index corresponds to $D_i + 1$. For this particular study, the CPC codebook used is the set of lower CPC symbols presented in (3).

At this stage, all the CPC symbols in each codeword need to be arranged into a column vector, so they can be mapped onto constellation, symbol by symbol. In this particular study, the constellation mapping is done using the DQPSK modulator.

Example 1: Let us assume we want to map the following RS bits onto the CPC symbols represented in (3):

$$\text{RS} = (1\ 1\ 0\ 1\ 1\ 0\ 1\ 0) \quad (7)$$

From (7), the bits are respectively grouped into 1 1, 0 1, 1 0, and 1 0, according to Step 1 above. Their corresponding decimal equivalents are given by $(D_1, D_2, D_3, D_4,)$ = $(3, 2, 1, 1,)$, according to Step 2 above. According to Step 3, $D_i + 1$ gives $(4, 3, 2, 2)$. Using these indices in the CPC codebook provided in (3), the encoded symbols are therefore given as $(3012, 2301, 1230, 1230)$. Before passing through the communication channel, these set of symbols are merged as (3 0 1 2 2 3 0 1 1 2 3 0 1 2 3 0), arranged into a coulumn vector and passed into the DQPSK modulator for constellation mapping.

B. The RS-CPC decoder

The strength of CPC-DQPSK lies in the codeword assembly process of the receiver. This is because, for every codeword misrepresented, a corresponding loss of 2 bits in the base RS bits is the implication, since 2 RS bits are mapped onto a CPC codeword. As such, a very good algorithm is needed for assembling the CPC codewords. A robust modified demodulator algorithm for PTC was reported in [19], but the algorithm is applicable to MFSK scheme. In that scheme, the generation of $M \times M$ binary matrices at the demodulator's output was suggested, to recover each transmitted PTC codeword, by comparing the binary equivalent of the expected codewords with each received binary matrix. Here, M, otherwise called the codeword length, is the number of symbols per codeword. However, in reality, this approach may appear a bit complex to implement, and latency might be a challenge, in case there is a long train of codewords to decode.

For ease of implementation of our scheme, we directly modulate the non-binary CPC symbols onto their complex basebands. At the receiving end, based on the DPSK algorithm, the non-binary CPC symbols are retrieved from the complex baseband, all still in a single column form. In order to recover the transmitted N RS bits, the following CPC decoding algorithm is employed:

Cyclic symbol demapping algorithm:

1) Symbols grouping: Arrange the received symbols, composed of N rows, into M columns, with each row representing a prospective CPC codeword. As such, we have N/M rows of prospective codewords, denoted as x_i, where $i = \{1, 2, \ldots, N/n\}$.
2) Metric computation: Compute the distance, d_k between x_i and every possible codeword kept in the memory of the receiver, where $k = \{1, 2, \ldots, |C|\}$, with $|C|$ being the cardinality of the CPC.
3) Codeword declaration: The codeword with the lowest distance, d_k, to x_i is selected as the detected codeword.
4) Confusion error declaration: If more than one lowest d_k exists, declare a confusion error, and make a random guess between the codewords having the same lowest d_k.

After the codeword declaration, the corresponding RS bits to the decoded codeword can be obtained, following a reverse procedure of the *Cyclic symbol mapping algorithm* presented above. The lower shaded box in Fig. 1 performs this decoding algorithm. The resulting RS bits are then processed by the FEC decoder (i.e., RS decoder) to obtain the original encoded message. The same CPC algorithms just described are also applicable to the ordinary PC scheme, the only difference being the codewords involved.

Example 2: With the continuation of *Example 1*, let us assume the received DQPSK symbols at the receiver have been demodulated and arranged into N/M rows of prospective CPC codewords x_i, according to Step 1 of the demapping algorithm above. Due to channel corruption, we assume the following prospective codewords have been assembled and they are to be decoded using the CPC codewords of (3):

$$\begin{aligned} x_1 &= (3\ 0\ 0\ 2), \quad x_2 = (2\ 3\ 0\ 1), \\ x_3 &= (1\ 2\ 3\ 0) \quad \text{and} \quad x_4 = (1\ 2\ 0\ 1) \end{aligned} \tag{8}$$

From (3), the codeword, $(3\ 0\ 1\ 2)$ has the lowest d_k to x_1, according to Step 2 and 3 of the demapping algorithm. In x_1, symbol 0 features in location 3, as a symbol error. However, due to the cyclic nature of the codewords, which produces a $d_{\min}$ of 4, the inserted symbol has no effect on selecting the correct codeword. The correct codewords for x_2 and x_3 remain the same as $(2\ 3\ 0\ 1)$ and $(1\ 2\ 3\ 0)$, without errors. In the case of x_4, two codewords, which are $(1\ 2\ 3\ 0)$ and $(2\ 3\ 0\ 1)$, have the same lowest d_k to it. In this regard, a confusion error is declared, and a random guess between the two competing codewords is to be made, according Step 4 of the demapping algorithm.

IV. The Implementation Setup

A similar experimental setup employed in [26] was employed in this work as well. However, this study is based on the implementation of RS-CPC-DQPSK scheme, while the one done in [26] is mainly on channel modelling. The schematic of the experimental setup is depicted in Fig. 2, while Fig. 3 shows the photograph of the setup. The topology contains 4 load points. The entire topology was powered by an isolated 230 V AC uninterrupted power supply (UPS). Another dedicated UPS (not added in the figure for clarity's sake) was used to power the two USRPs, to prevent interference with the channel setup. The USRP hardware at the left hand side of the topology was configured as the transmitter (Tx), whose radio frequency (RF) output port is connected to a PLC coupling circuit (bandpass filter), and the receiving USRP (Rx) sits at the right hand side of the topology. The coupling circuits used are the capacitive types, made of thick cores, and have the capability of supporting communication in the frequency range of 40 kHz to 309 kHz.

Since SDR technology provides the opportunity of performing most of the signal processing in the software domain, our coding and modulation schemes were performed in the software domain. As such, a number of coding schemes could be compared in practical sense (as done in the comparison aspect of this work), since the software can easily be modified.

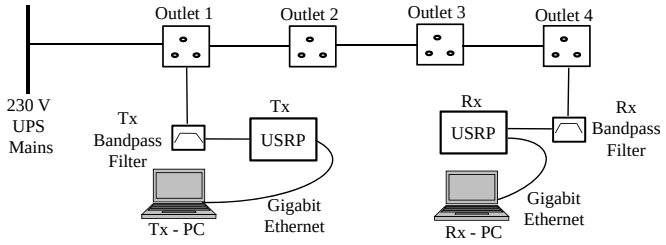

Fig. 2. The schematic of the experimental setup

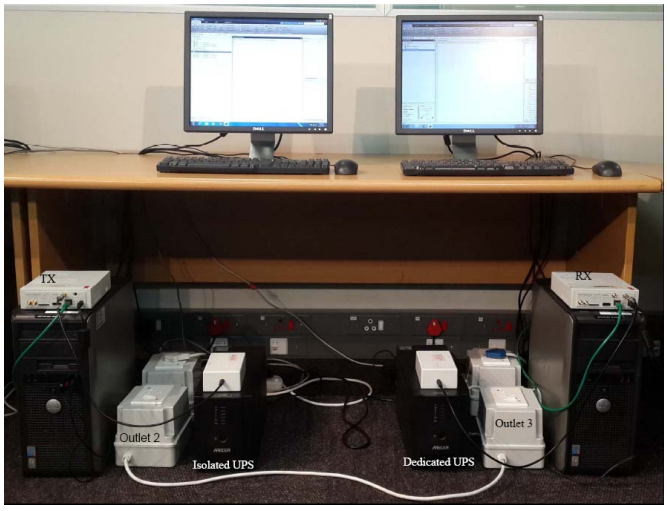

Fig. 3. The photograph of the experimental setup

A. Input data description

The simulation input data is a 5376 random bit sequence generated by the "*randi*" Matlab function. For the practical aspect, the same software and hardware configurations employed in [26] were also used in this work, except for the

TABLE I. SOFTWARE CONFIGURATION

Items/Parameters	Configurations/Values
USRP FPGA & Firmware rev.	003.002.003
Centre frequency	145 kHz
Sampling frequency	0.2 MHz
Decimation and	5e8
Interpolation factors	
USRP daughterboards	LFTX & LFRX
	(0 - 30 MHz)
Host-based Software Version	Matlab R2012b

centre frequency, which is now 145 kHz. For the purpose of emphasis, some of the important parameters have been repeated in Table I. For easy comparison, picture streaming was employed, and the achieved QoS was used as a yardstick for the performances of the various schemes compared. The transmitted picture is a PNG image, with the inscription "TRELLIS PERMUTATION", as shown in Fig. 4.

Fig. 4. The transmitted image

V. RESULTS

Three different coding schemes have been compared in this work. The first scheme is our proposed RS-CPC-DQPSK scheme. The second one is the scheme proposed by G3-PLC, which is RS-CC-DQPSK. The third one is similar to the one considered in [4] and [9], with $d_{\text{min}} = 3$, but in this regard, it is RS-PC-DQPSK. Here, 4 RS bits are mapped onto 4 PC symbols. The PC word sequence for this consists of 16 possible combinations, with some repetitive symbols, as described in [9]. The effective ratio of the coding rates of all the three schemes considered is 1:2:2 (from the first to the third scheme), and these have been put into consideration in the E_b/N_o computations (for the simulation work). This is to ensure fair comparisons. For practical aspect, the transmit gain needs to be manipulated, in order to achieve the rate compensation. However, the transmitting daughterboard has a non-tunable transmit gain, which makes it difficult for the compensation. A work around this, was to manipulate the transmitted signal's strength at the signal processing section, inside the software domain, so as to enforce the coding rate compensation. A spectrum analyzer was used to ascertain the manipulated transmit gain, by directly tapping the signal at the USRP receiver's RF input port and coupling it unto the analyzer's input port. With this, the signal level could be monitored after the gain was varied in the software domain.

A. Simulation results

The transceiver model introduced in Fig.1 was simulated, using a AWGN (additive white Gaussian noise) channel to represent the transmission channel, and a combined IN with AWGN is later considered in the simulation. Since our main focus is on the implementation of the proposed scheme, other cases of PLC channel associated noise are not reported here. We have used a simple IN model in our channel condition. Here, a parameter designated as P is used to define the likelihood of IN occurring in the transmitted frame. Wherever IN occurs, its strength is made higher than the normal AWGN strength. This same concept is what was used in [4] for defining an NBI model in the frequency domain. Three instances of this likelihood/probability (i.e., $P = 2.5\%$, $P = 6.5\%$ and $P = 12.5\%$) are used in evaluating the various coding schemes compared in this study. In-depth understanding of this modeling can be accessed in [4].

Fig. 5 shows the result of the simulated RS-CPC-DQPSK, RS-CC-DQPSK and RS-PC-DQPSK schemes, considering only an AWGN channel. The RS-CC-DQPSK scheme's performance outperforms those of the other two PCs in RS-CPC-DQPSK and RS-PC-DQPSK at $E_b/N_o > 7$. The two schemes with PC have equal and better performances than RS-CC-DQPSK below this E_b/N_o value, before RS-PC-DQPSK starts outperforming our scheme. This is because coding rates have to be compensated for. Hence, our RS-CPC-DQPSK scheme, which has the lowest rate, cannot perform better when only AWGN channel is considered, because it is only a pure random distribution. However, as regards PLC channels, the expected channel condition in reality is more severe than an ordinary AWGN channel. As such, we have extended the simulation to include IN in the channel.

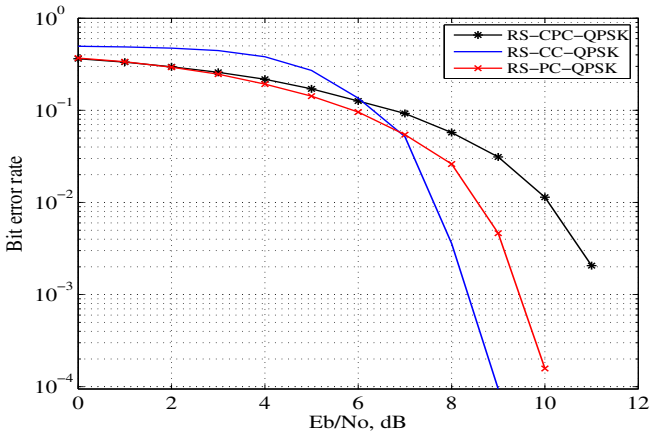

Fig. 5. Bit error rate curve for RS-CPC-DQPSK, RS-CC-DQPSK and RS-PC-DQPSK schemes, in the presence of AWGN

Fig. 6 is the result of the simulation, in the presence of both AWGN and IN. At IN probability, $P = 2.5\%$, all the three schemes have averagely similar performances, but RS-CC-DQPSK can no longer withstand the IN noise floor at $E_b/N_o > 11$. However, the strength of RS-CPC-DQPSK becomes glaring at probabilities above 2.5%. The implication of these findings is that, the more a communication channel gets affected by IN, as in the case of PLC, the use of a CPC as an inner coding scheme is reliable. More so, for implementation purposes, our RS-CPC-DQPSK scheme should be preferred, because, its encoding and decoding algorithms are simpler, owing to the fact that there are only 4 possible codeword sequences involved, while those of RS-PC-DQPSK are 16 possible sequences. The more the number of codewords, the more complex the decoding algorithm becomes.

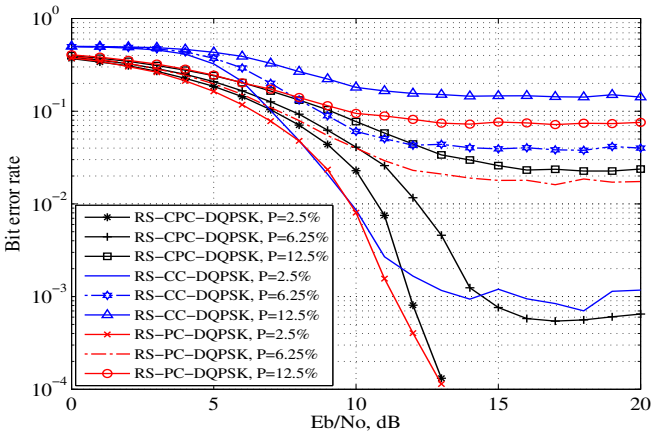

Fig. 6. Bit error rate curve for RS-CPC-DQPSK, RS-CC-DQPSK and RS-PC-DQPSK schemes, in the presence of AWGN and IN

B. Experimental results

For practical analysis, the topology presented in Fig. 2 was used to transmit the image shown in Fig. 4, under two case studies. For case 1, no load was connected in-between the Tx and Rx. For case 2, additional computers were powered through outlets 2 and 4 on the topology, with a flickering incandescent light bulb (100 W) powered through outlet 3. With this, we are able to simulate some form of instability in the channel's state. A typical channel modelling of a topology, such as used in this work, was included in the work reported in [26]. Therein, USRP kits were used for noise measurements so as to obtain data which were further used in a Fritchman model for studying the nature of the noise types associated with PLC channel.

The results of the comparisons made between the three schemes considered, for case 1 are displayed in Fig. 7 to 9. From these figures, the RS-CPC-DQPSK and RS-PC-DQPSK schemes have relatively similar QoS. There is no pronounced difference between the two received images and the transmitted one. The RS-CC-DQPSK has a little bit of errors in it. For case 2, our RS-CPC-DQPSK turned out having the best performance, followed by the RS-PC-DQPSK, as shown in Fig. 10 to 12. One major concern in our scheme is slower transmission speed, in case a huge amount of data is to be transmitted. This is because, it is of lower rate, as compared to the other two schemes.

Fig. 7. The received image using RS-CPC-DQPSK scheme in case 1

Fig. 8. The received image using RS-PC-DQPSK scheme in case 1

VI. Conclusion

A special RS-CPC coding scheme that improves the performance of the OFDM component (i.e., MDPSK), specified in the G3-PLC and PRIME standards, has been presented, together with its encoding and decoding algorithms. This was evaluated both at simulation and implentation levels, using USRP to transmit and receive data packets on a 230 V AC power line channel. The CPC encoder maps the output of an RS encoder onto PC symbols in a cyclic sequence. The modulation process involves direct modulation of the non-binary PC symbols, prior to transmission through the communication channel. Reverse procedures are followed to recover the modulated PC symbols at the receiving end. Comparisons with a conventional RS-CC-DQPSK and another RS-PC-DQPSK scheme, both at simulation and practical levels, prove our RS-CPC-DQPSK scheme to be more robust in most of the instances considered. Since our focus is mainly on the evaluation and implementation of the CPC scheme, a simple decoding algorithm has been considered. An improved work may be done on its decoding algorithm to further improve its performance. It is also worth knowing that the quality of the PLC coupling circuits also have some influence on the performance of the PLC systems in general.

Fig. 9. The received image using RS-CC-DQPSK scheme in case 1

Fig. 10. The received image using RS-CPC-DQPSK scheme in case 2

Fig. 11. The received image using RS-PC-DQPSK scheme in case 2

Fig. 12. The received image using RS-CC-DQPSK scheme in case 2

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