Analysis of bias stress on thin-film transistors obtained by Hot-Wire Chemical Vapour Deposition

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Abstract

The stability under gate bias stress of unpassivated thin-film transistors was studied by measuring the transfer and output characteristics at different temperatures. The active layer of the devices consisted on nano-crystalline silicon deposited at 125ºC by Hot-Wire Chemical Vapour Deposition. The dependence of the sub-threshold activation energy on gate bias for different gate bias stress is quite different from that reported for hydrogenated amorphous silicon. This behaviour has been related to the charge trapped in the active layer of the thin-film transistor.

Keywords: TFT, nano-crystalline silicon, HWCVD, Stability.

1. Introduction

Hot-Wire Chemical Vapour Deposition (HWCVD) is one of the most promising techniques to obtain hydrogenated amorphous silicon (a-Si:H) and hydrogenated nanocrystalline silicon (nc-Si:H) at low substrate temperatures (<300ºC) over large areas and high deposition rates (>1nm/s)[1-3].
Hydrogenated nanocrystalline silicon obtained by HWCVD is composed of small silicon crystallites, with an average grain size of a few nanometers embedded in an amorphous silicon matrix. As a result, nc-Si:H properties lay between those of a-Si:H and polysilicon (with grain sizes of few micrometers).
Hydrogenated amorphous silicon thin-film transistors (TFT) are widely used in liquid crystal displays and matrix image sensors. However a-Si:H TFTs present electrical instability, mainly consisting of a threshold voltage (V_t) shift, when a gate voltage is applied for a prolonged period of time. Two mechanisms contribute to threshold voltage instability: charge trapping in the gate insulator and defect creation in the band-gap of a-Si:H [4].
In this paper, the stability of TFTs with nc-Si:H active layers deposited at 125ºC by HWCVD is studied. The stability was investigated by examining the gate transfer characteristics and the dependence of the subthreshold current activation energy on gate bias for as-deposited samples and after negative and positive bias stress.

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2. Experimental

Nano-crystalline TFT's were deposited by HWCVD by using an ultra-high-vacuum multichamber set-up described elsewhere [5]. Processing gases [silane-hydrogen mixture (4/76 sccm)] were catalytically dissociated by a tungsten wire heated at 1700ºC. Substrate temperature was around 125ºC (measured by a thermocouple attached to the heater) and the process pressure was 1×10^{-2} mbar. Under these conditions the deposition rate was 0.6 nm/s. Thin-film transistors used in this work are inverted staggered structures without top passivation layer. A thermally oxidised n-type (100) silicon wafer with a resistivity of 1-10 Ω·cm was used as substrate. Thicknesses were 250 nm for the active layer and 250 nm for the silicon dioxide. An n^+-doped layer (50 nm) between the drain and source contacts and the intrinsic layer was also deposited by HWCVD.
Finally a chromium layer was thermally evaporated and the metallic contacts (drain and source) were delimited by photolithographic techniques. The channel width was 137 μm and the length 55 μm, giving an aspect ratio for the device (i.e. W/L) of 2.5. Details on the fabrication process have been reported in a previous work [6].
Different TFTs were electrically characterised by measuring the transfer and output characteristics. We also studied the dependence of the subthreshold current activation energies ($E_{ACT} = E_C - E_F$) on gate bias. After the initial characterisation of the samples, stressing processes at different gate voltages (□40, □20 and +40 V) were performed at room temperature (298 K) for 1000 s. All the measurements were performed under dark conditions by using a Hewlett□Packard HP4145B semiconductor parameter analyser and a temperature controlled chuck.

3. Results and discussion.

The output and transfer characteristics of the transistors as deposited and after positive and negative gate bias stress are shown in Fig. 1a. From the output characteristics I_{DS} vs. V_{DS} it can be seen that there is not a current crowding and as a consequence we conclude that the influence of the source and drain contact resistance is not important in our devices. The absence of the Kink effect (a rapid rise of I_{DS} at high V_{DS}) indicates that the electron injection at the contacts is very small. The transfer characteristics in saturation regime were measured to determine the threshold voltage and the field effect mobility of the transistors. A threshold voltage of 6.9 V and field effect mobility of 0.3 $cm^2/V\cdot s$ were obtained. After gate bias stress, a positive shift of threshold voltage ($\Delta V_t \approx +1$ V) for positive gate bias stress and a negative shift ($\Delta V_t \approx -1$ V) for negative gate bias stress were obtained.
The application of a gate voltage in field effect structures shifts the Fermi level inside the gap. This displacement allows us to study the electronic properties of the material. The rate at which EF moves towards the conduction band (in n-channel devices) depends on the density of states located in the band gap and on the distribution of tail states close to the conduction band. For small values of V_{GS} the Fermi level is located in deep states. Increasing V_{GS} shifts the Fermi level to the conduction band, and the tail band states become important. Besides, for high positive V_{GS} applied an influence of the amorphous phase in the nucleation region of the crystallites could not be discarded.
It has been reported (experimentally as well as through simulation results) [7,8] that for hydrogenated amorphous silicon, the application of a negative gate bias create additional states in the upper half part of the bandgap. This additional peak on the density of states leads to a reduction

of the slope of $E_{ACT}(V_{GS})$ for V_{GS}<10 V, indicating the presence of defect states created by degradation.
In Fig. 2 the dependence of E_{ACT} on V_{GS} for TFTs before and after bias stress degradation is shown. For the as-deposited sample we observe that the Fermi level moves from around midgap (E_{ACT} =0.45 eV for V_{GS}=0 V) to the conduction band, remaining nearly constant at approximately 0.15 eV, where the Fermi level is pinned by the band tail states.

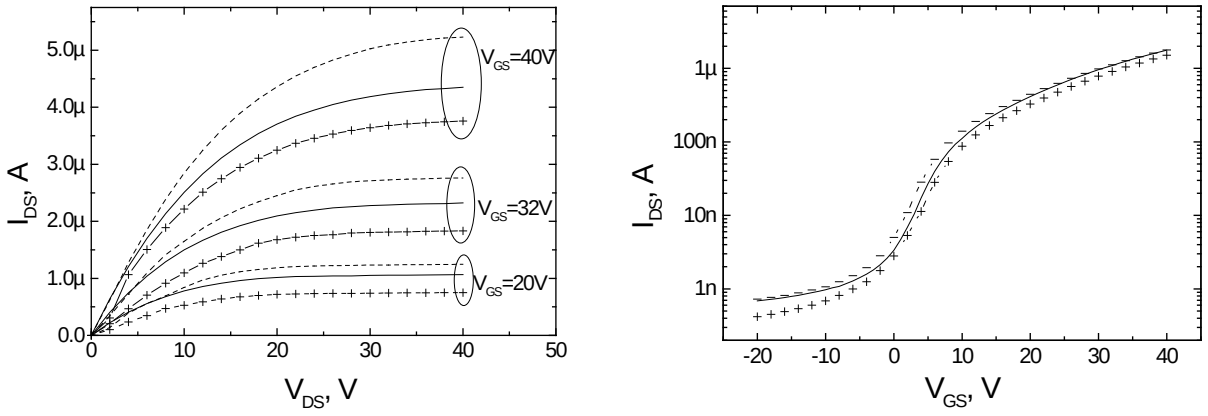

Fig. 1. Output and transfer characteristics of nano-crystalline TFT measured as-deposited (solid lines) and after different gate bias stress: V_{GS} = +40 V (- symbols), V_{GS} = -40 V (+ symbols).

In Fig. 2 it is observed that the application of positive (negative) bias stress to the gate leads to a positive (negative) displacement of the [$E_{ACT}(V_{GS})$] characteristics. The shift obtained after the application of negative gate bias stress is in opposite direction to the one observed for a-Si:H TFTs after a similar degradation process [8].

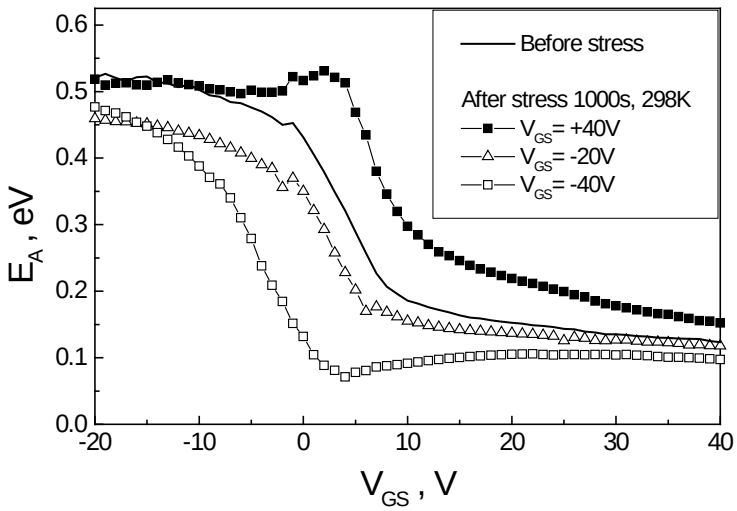

Fig.2. Dependence of the activation energy (E_{ACT} = E_C - E_F) of the sub-threshold transfer characteristics for TFT stressed at different gate biases.

We believe that the application of positive/negative bias stress to the gate causes redistributions in the trapped charge of the active layer in the TFT. Negative stress, for example, depletes the trapped charge between EF and the conduction band, causing the Fermi level to be slightly shifted towards the conduction band. Therefore, the application of small values of V_{GS} easily shifts the E_F to the conduction band, remaining fixed by the band-tail states. This charge trapped could be related to the impurities (oxygen, copper,...) incorporated in the layer during the deposition process [9].
The transistors were measured again 50 h after the stressing process. They showed the same characteristics as before the stressing process including threshold voltage and activation energy, these results also seem to confirm that charge trapping could be the main mechanism involved by the application of gate bias stress.

4. Conclusions

In this work we have presented the results of stress treatment of TFT's with nano-crystalline active layer fabricated at low temperature (125ºC) by HWCVD process. The results indicate that changes in the electrical characteristics of the device could be due to temporarily trapped charge in the material. In our future work detailed analysis of the interface states in the transistors by capacitance measurements will be performed.

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