

## Nonlinear Parasitic Capacitance Modelling of High Voltage Power MOSFETs in Partial SOI Process - DTU Orbit (09/11/2017)

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State-of-the-art power converter topologies such as resonant converters are either designed with or affected by the parasitic capacitances of the power switches. However, the power switches are conventionally characterized in terms of switching time and/or gate charge with little insight into the nonlinearities of the parasitic capacitances. This paper proposes a modeling method that can be utilized to systematically analyze the nonlinear parasitic capacitances. The existing ways of characterizing the off-state capacitance can be extended by the proposed circuit model that covers all the related states: off-state, sub-threshold region, and on-state in the linear region. A high voltage power MOSFET is designed in a partial Silicon on Insulator (SOI) process, with the bulk as a separate terminal. 3D plots and contour plots of the capacitances versus bias voltages for the transistor summarize the nonlinearities of the parasitic capacitances. The equivalent circuits in different states and the evaluation equations are provided.

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