Three-Port dc-dc Conversion in Light-to-Light Systems

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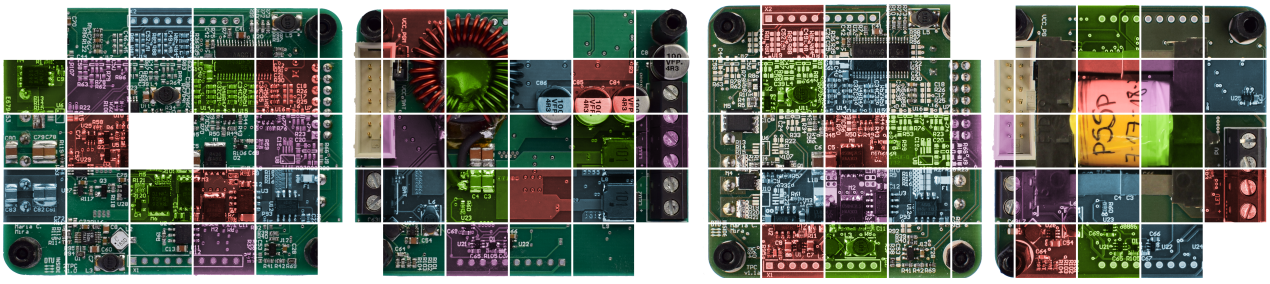

DTU Electrical Engineering
Department of Electrical Engineering

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To my grandmother
Carmen

Preface

This dissertation is submitted in partial fulfillment of the requirements for obtaining the Ph.D. degree at Technical University of Denmark. The research has been carried out at the Electronics Group, Department of Electrical Engineering, from December 2012 to February 2016 under the supervision of Prof. Michael A. E. Andersen and Assoc. Prof. Arnold Knott.

This Ph.D. project has been founded by the Danish Energy Technology Development and Demonstration Programme (EUDP- Energiteknologisk Udvikling og Demonstration), project number 64011-0323 "The PV LED Engine - new generation of intelligent solar powered LED lighting", and has been developed in collaboration with the Department of Photonics Engineering at Risø and industry partners: Out-Sider A/S, AKJ Inventions ApS. and Modelmager Morten Lyhne.

A research visit of 3 months was carried out at Colorado Power Electronics Center (CoPEC) at Colorado University (CU), led by Profs. Dragan Maksimović and Robert Erikson.

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- My childhood best friend, Mari Carmen Martínez, for her friendship and support throughout the years.
- My beloved parents for their unconditional love and encouragement. My family in-law for their love and support.
- Last but not least, my deepest gratitude, to the love of my life, Juan Carlos, for his endless encouragement, confidence, patience and support. My colleague, my friend and my love; half of my life we have been together, and the best is yet to come.

Abstract

Renewable energies, like solar or wind, provide unlimited, clean and free energy that helps reducing (CO_2) emissions, which alleviates global warming and greenhouse effects. Moreover, the ability to produce off-grid electricity allows local electric power generation. However, the main disadvantage of renewable sources is that they are strongly dependent on the weather conditions, and, therefore, intermittent and unpredictable. For this reason they need to be combined with other power sources, or energy storage elements, in order to ensure reliable and constant power to the load.

Solar energy is one of the major renewable energies because the Sun is a vast, inexhaustible and clean resource. Photovoltaic cells transform sunlight into electrical energy and the generated power is proportional to the amount of solar irradiation.

Light-emitting diodes (LEDs) present higher luminous efficiency and lifetime than conventional light sources based on heated filaments (incandescent and halogen) and gas discharge (fluorescent, sodium, etc). The rapid development of this technology makes it possible to replace the conventional technologies towards high brightness LED lighting systems.

The combination of these technologies—solar cells, energy storage elements and LEDs—in a stand-alone solar powered LED system, can provide light where otherwise it would be cumbersome; in rural areas, where cabling can be challenging and expensive, and also in the urban environment, where the cost of digging and construction is very expensive.

Solar powered systems are particularly challenging in locations far from the equator, where the solar resource is scarce, especially during winter, since the amount of solar irradiation is small and the length of the day is short. Therefore, these systems need to be optimized by maximizing the energy conversion efficiency under low irradiation conditions.

This work is part of a Ph.D. research project to study the feasibility of implementing three-port converter (TPC) topologies in solar powered LED, light-to-light (LtL) systems. After the introduction in Chapter 1, an overview of the state-of-the art of solar cells, LED technology and energy storage elements, as well as a review of TPC topologies is given in Chapter 2. Following, the study of a low-power ($10 - 50$ W) stand-alone PV-LED system with aim on high efficiency energy conversion is presented in Chapter 3. The implemented power stage is based on component reutilization and is optimized at low irradiation conditions, achieving a peak efficiency of 98.9%. A discussion on the magnetic component design, semiconductor evaluation based on switching energy measurement and study of the loss distribution is presented. Scalability and implementation of multiple LED outputs on the proposed topology are discussed and demonstrated on a second prototype. A TPC for grid-tied light-to-light applications ($100 - 1000$ W) is studied in Chapter 4. Analysis, modeling and power flow regulation with two control variables are discussed in this section. The dynamic modeling and measurements prove that completely decoupled power flow regulation can be achieved. Finally, the conclusion and future work are presented in Chapter 5. Other research topics—not directly related with the project objectives—are shown in Chapter 6.

Dansk Resumé

Vedvarende energi fra sol eller vind giver ubegrænset ren energi der hjælper med at reducere (CO_2) og lindre den globale opvarmning samt drivhuseffekten. Ydermere muliggør evnen til at producere elektricitet fra vedvarende energikilder uafhængigt af elnettet en lokal el-produktion. Den største ulempe ved vedvarende energikilder er deres store afhængighed af vejrforholdene, hvilket gør dem uregelmæssige og uforudsigelige. Af den grund skal de kombineres med andre strømkilder eller energilagrende elementer, for at sikre en pålidelig og konstant levering af strøm til belastningen.

Solenergi er en af de store vedvarende energikilder, fordi Solen er en stor, uudtømmelig og ren ressource. Solceller omdanner sollys til elektrisk energi og den genererede strøm er proportional med mængden af solens stråler.

Lysdioder (LED) har højere lysstyrke og levetid end konventionelle lyskilder som er baseret på glødetråd (glødepærer og halogenpærer) og gas (neon, natrium, osv.). Den hurtige udvikling af denne teknologi gør det muligt at erstatte de konventionelle teknologier med LED baserede lyssystemer.

Kombinationen af teknologier som solceller, energilagrende elementer og LED lysdioder i et selvstændigt soldrevet LED system kan give lys, hvor det ellers ville være besværligt. Dette gælder f.eks. i landdistrikterne, hvor kabler kan være udfordrende og dyre men også i bymiljøet, hvor installationsomkostningerne kan være høje.

Soldrevne systemer er særligt udfordrende på steder langt fra ækvator, hvor solens ressourcer især om vinteren er sparsomme, da mængden af solbelysning er begrænset, og dagene er korte. Disse systemer skal derfor optimeres ved at maksimere effektiviteten af energikonverteringen under forhold med lav solbelysning.

Dette arbejde er en del af et Ph.D. forskningsprojekt der undersøger muligheden for at implementere tre-port strømforsynings-topologier (TPC) i soldrevne LED, lys-til-lys (LtL) systemer. Først gives en oversigt over state-of-the-art solceller, LED-teknologi og energiopbevarende elementer samt en gennemgang af TPC topologier. Herefter følger en undersøgelsen af et energibesparende ($10-50$ W) separat PV-LED-system med sigte på højeffektiv energikonvertering. Det implementerede effekttrin er baseret på funktionel komponent genbrug og er optimeret til forhold med lav solbelysning. Resultatet er en høj maks. effektivitet på 98.9%. En diskussion af det magnetiske komponentdesign, måling af skriftetab og undersøgelse af tabsfordelingen præsenteres. Skalerbarhed og implementering af flere LED udgange på den foreslåede topologi diskuteres og demonstreres med en yderligere prototype. En TPC for en lys-til-lys applikation der er tilsluttet el-nettet ($100-1000$ W) er beskrevet i kapitel 4. Analyse, modellering og regulering af strømveje med 2 kontrolvariabler bliver diskuteret i en undersektion. Den dynamiske modellering og målinger viser at fuldstændig afkoblet regulering af strømvejen kan opnås. Endeligt præsenteres en konklusion og et bud på videre arbejde i kapitel 5. Andre forskningsemner som ikke er direkte relateret til projektets målsætninger er også inkluderet i dette afsnit.

Contents

List of Abbreviations

ADC	Analog-to-Digital Converter
AM	Air Mass
BIBC	Bidirectional Interleaved Boost Converter
BMS	Battery Management System
CCM	Continuous Conduction Mode
CCT	Correlated Color Temperature
CRI	Color Rendering Index
CSF	Component Stress Factor
DCM	Discontinuous Conduction Mode
DI	Dual Input
DIC	Dual Input Converter
DIDO	Dual Input Dual Output
DO	Dual Output
DOC	Digitally Controlled Oscillator
DOC	Dual Output Converter
DUT	Device Under Test
EDLC	Electric Double-Layer Capacitor
ELP	Economic Low Profile
EMC	Electromagnetic Compatibility
ETD	Economic Transformer Design
FB	Full Bridge
FPC	Four-Port Converter
HB	Half Bridge
LED	Light-Emitting Diode
Li-Ion	Lithium-Ion
Li-Po	Lithium-Polymer
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking

NaS	Sodium-Sulfur
Ni-Cd	Nickel-Cadmium
Ni-MH	Nickel-Metal Hydride
Pb-Acid	Lead-Acid
PCB	Printed Circuit Board
PSFB	Phase-Shift Full Bridge
PV	Photovoltaic
PWM	Pulse-Width Modulation
SISO	Single Input Single Output
SMD	Surface Mount Device
SMPS	Switched Mode Power Supply
SOC	State-of-Charge
STC	Standard Test Conditions
TPC	Three-Port Converter
VNA	Vector Network Analyzer
VRB	Vanadium Redox
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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1

Introduction

1.1 Background and Motivation

Renewable energy sources have become an important part of the energy production because of global warming awareness and fossil fuel resources depletion. Due to the requirement of high efficient energy conversion, switched-mode power supplies (SMPS) play a key role in the integration of renewable energy systems [1]. Solar energy is one of the fastest growing renewable energy sources, mainly because the Sun is an abundant source of energy and is unlimited, clean and free. The main advantages of the renewable energies are the transformation of energy with zero carbon dioxide (CO_2) emissions and the ability of producing off-grid electricity. However, the main disadvantage is that they are intermittent and unpredictable in nature, and need to be combined with other power sources, or energy storage elements, to be able to deliver reliable and constant power to the load. Combining the renewable source with the energy storage element turns the assembly into a stand-alone system, which is very useful to power up systems not only at remote locations, where cabling is challenging and expensive, but also in the urban environment, where digging and construction is very expensive.

Light-emitting diode (LED) technology provides higher luminous efficiency and lifetime than any conventional light sources. The combination of solar cells, energy storage and LEDs in a stand-alone photovoltaic (PV) LED system provides efficient "light-to-light" (LtL) conversion.

Stand-alone solar powered lighting systems in northern latitudes are challenging due to the intrinsic limitations of the geographic location. PV cells convert the sunlight into electricity, and the generated power depends on the amount of solar irradiation, which strongly depends on the location and the weather conditions. This is particularly a drawback in locations far from the equator, especially during winter, where the length of the day is short and the amount of solar irradiation is very small. In these conditions, the lighting fixture needs to be active during long periods of time, which might require over-dimensioning of the energy storage element and the PV panel to be able to provide energy to the load during the long winter days. On the contrary, during summer time, the days are very long, with only a few hours of night. In this context, when applied to high-power light-to-light systems ($100 - 1000$ W), a grid-tied implementation can provide the assembly with a safe and an active mode, i.e., it can supply energy to the

lighting if there was no sunlight to charge the battery during winter time and supply the surplus of energy to the grid during the summer period.

Three-Port converter (TPC) topologies, combining a renewable energy source and an energy storage element to a common load, have attracted research interest in order to reduce the conversion stages and power processing, compared to the conventional interconnection solutions.

1.2 Project Objectives

This dissertation presents a study of dc-dc conversion and multiport systems in light-to-light applications. Special research interest has been addressed to low-power stand-alone solar LED systems. The main project objectives can be summarized as follows:

- To investigate the feasibility of integrating TPC topologies in light-to-light systems, while achieving high efficiency due to reduced power processing stages, and identify challenges in the controllability of the different power flows with two control variables.
- To design and implement a high efficiency scalable low-power ($10 - 50$ W) dc-dc converter for stand-alone PV-LED systems, with special focus on achieving high efficiency conversion under low irradiation conditions.

1.3 Dissertation Scope

The scope of this Ph.D. dissertation is to summarize and present a coherent overview of the work carried out as part of a Ph.D. project from December 2012 to February 2016. The obtained results during this research period have been published in the form of peer reviewed conference and journal papers, as well as a patent application. These represent an important part of this Ph.D. dissertation and have been included in the Appendices at the end of this document.

1.4 Dissertation Structure

Figure 1.1 shows the dissertation structure, which consists of six chapters. Following the introduction, Chapter 2 provides an overview of the state-of-the-art of photovoltaic cells, LED lighting technology, energy storage elements and TPC topologies. The third chapter presents the study of a low-power stand-alone LtL system, with aim on high efficiency energy conversion. Different magnetic structure designs are discussed, in terms of leakage inductance and parasitic capacitances. A semiconductor evaluation based on switching energy measurement is performed and a study of the converter loss distribution is presented. Scalability and implementation of multiple LED outputs on the proposed topology are discussed in the last section. A TPC for high power ($100 - 1000$ W) grid-tied light-to-light systems is presented in Chapter 4. The analysis, modeling and power flow regulation with two control variables is discussed. The conclusion and future work are presented in Chapter 5. Other research topics, not directly related with the main project objectives, are shown in Chapter 6.

1.4 Dissertation Structure

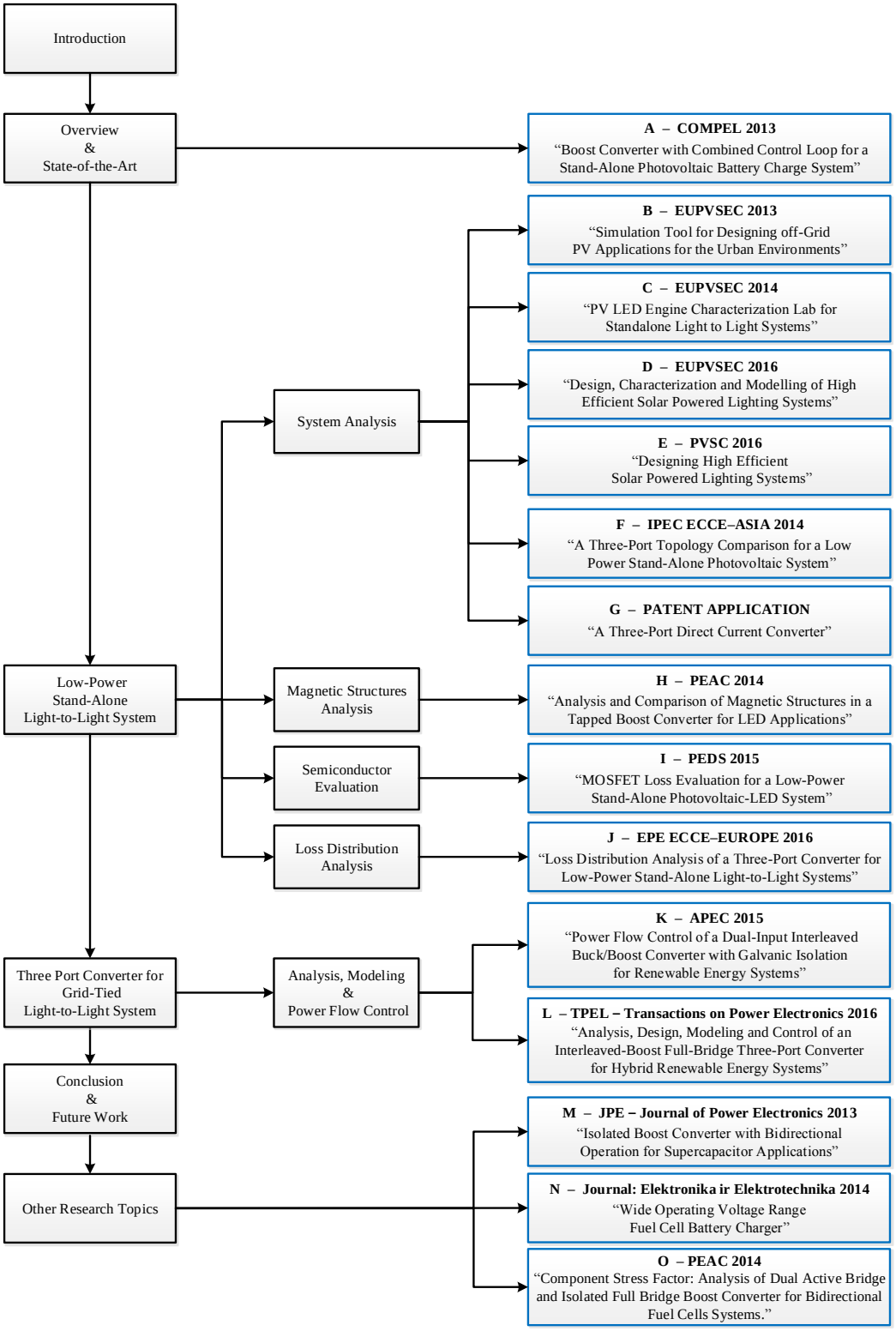


Figure 1.1: Dissertation structure.

2

Overview and State-of-the-Art

2.1 Photovoltaic cells

The photovoltaic effect relates how an electric current is induced in a material due to exposure to light. Notable events in the history of photovoltaics are discussed in [2]. The photovoltaic effect was discovered by E. Becquerel in 1839, who observed a small amount of electric current in liquid electrolytes when exposed to light. In 1883, C. Fritts constructed the first solid-state solar cell using Selenium (Se) film. Nevertheless, it was in 1954 at Bell Labs, when researchers discovered by accident that a *pn* junction diode generated a voltage when the lights of the room were on. It was then where the modern era of photovoltaics started. Figure 2.1 shows the best research-cell efficiencies from 1975 to the present, given by the National Renewable Energy Laboratory (NREL)[3].

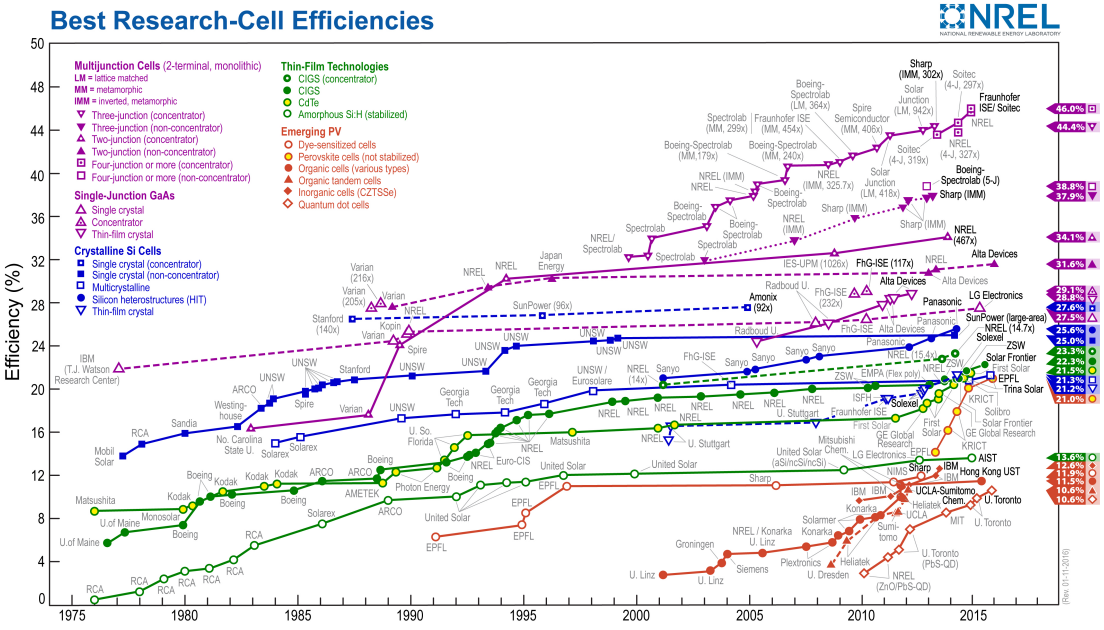


Figure 2.1: Best research-cell efficiencies [3].

The predominant material used for manufacturing solar cells is crystalline Silicon (c-Si). First of all, because Si is one of the most abundant element on the Earth's crust and, second, because Si technology is very mature due to the research on semiconductor technology. Depending on the arrangement and structure of the Si crystals, c-Si technology is divided in two categories, mono crystalline and polycristalline. Monocrystalline Si present higher efficiency than polycristalline Si cells, 18% - 25% and 13% - 20% [4], [5] , respectively, but its production is more expensive. Thin film PV cells are cheaper to produce, however, their efficiency decreases to 6% - 10%. The latest research on multijunction cells reaches efficiencies up to 40%, however, this technology is still very expensive and mainly used in space applications. Therefore, crystallyne Si is nowadays the dominant photovoltaic technology.

A solar cell is basically a *pn* junction that generates a current under the effect of solar irradiation. The basic model of a solar cell is a light dependent current source, representing the photogenerated current, and an anti parallel diode. The single-diode four-parameter model, shown in Figure 2.2a, includes the series resistance (R_s), which accounts for the effects of internal resistances and metal contacts due to interconnections [6]. The five-parameter model, shown in Figure 2.2b, includes the shunt resistance (R_{sh}), which accounts for losses due to the leakage currents across the *pn* junction [7]. Equation (2.1) presents the transcendent equation, which defines the behavior of a solar cell using the five-parameter model [8].

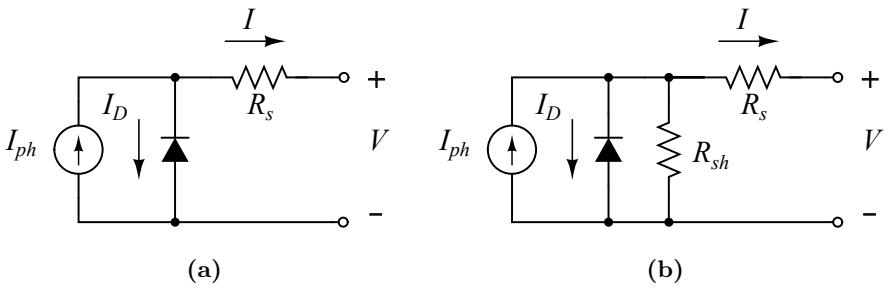


Figure 2.2: Single-diode (a) four-parameter model (b) five-parameter model.

$$I = I_{ph} - \underbrace{I_o \cdot \left(e^{\frac{V+I\cdot R_s}{V_t}} - 1\right)}_{I_D} - \frac{V + IR_s}{R_{sh}}$$
$$V_t = \frac{AkT}{q} \tag{2.1}$$

where:

I_{ph}: photogenerated current (A).
I_o: dark saturation current (diode leakage current density in the absence of light) (A).
R_s: series resistance (Ω).
R_{sh}: shunt resistance (Ω).
V_t: cell's equivalent thermal voltage (V).
A: diode ideality factor (between 1 and 2).
k: Boltzmann's constant ($1.380 \cdot 10^{-23}$ J/K).
q: charge of an electron ($1.602 \cdot 10^{-19}$ C).

T: pn junction temperature (K).

Taking the shunt resistance into consideration considerably increases the complexity of the calculations, requiring iterative methods to determine the model parameters [9]. The four-parameter model approach is considered a good compromise and it is used in this work for simulation of the PV characteristic curves [10].

Figure 2.3 shows the non-linear I–V and P–V characteristic curves of a PV panel. There are several distinctive points, named short circuit current, I_{sc}, open circuit voltage, V_{oc}, maximum power point, MPP, and current and voltage at the maximum power point, I_{mp} and V_{mp}, respectively. As it can be observed, the PV current and voltage are strongly coupled to each other, and when the current is maximum, the voltage is zero and vice versa. The point where the panel delivers its maximum power is located at the knee of the curve. Moreover, it can be observed that for values of voltage below V_{mp} the photovoltaic panel behaves as a current source, whereas for $V > V_{mp}$ it performs as a voltage source. The PV panel characteristic parameters are given by the manufacturers at standard test conditions (STC), which defines the irradiance (G), temperature (T) and air mass (AM) conditions. STC are defined as $G = 1000$ W/m^2, $T = 25$°C and $AM = 1.5$, where AM represents the sunlight path length ratio to the shortest possible path length.

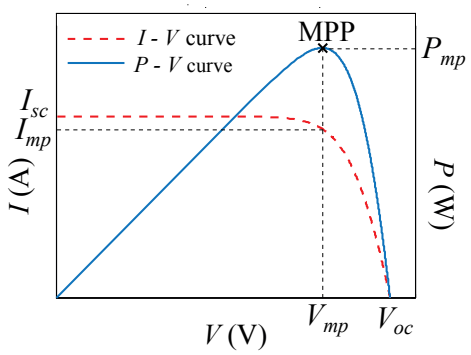


Figure 2.3: I–V and P–V characteristic curves of a PV panel.

The output current and voltage of the photovoltaic panel are strongly dependent on the weather conditions. On the one hand, the output current has a linear dependence with the photogenerated current and, therefore, varies strongly with changes of irradiation, as it can be observed in Figure 2.4a and 2.4b. However, due to the logarithmic dependence of the voltage with the photogenerated current, the PV voltage remains almost constant with irradiation changes. On the other hand, the PV voltage presents variations with temperature changes, whereas the current is slightly affected, as shown in Figure 2.5a and 2.5b. Nevertheless, temperature has slow dynamics compared to irradiation variations, i.e. cloudy atmospheric conditions. For regulation purposes, the control variable should be constant, or change slowly within a certain range. For this reason, voltage control of the photovoltaic panel is preferred over current regulation [11], [12], [13], since fast irradiation changes will result in less MPP deviation in the voltage control loop solution than in the current loop implementation.

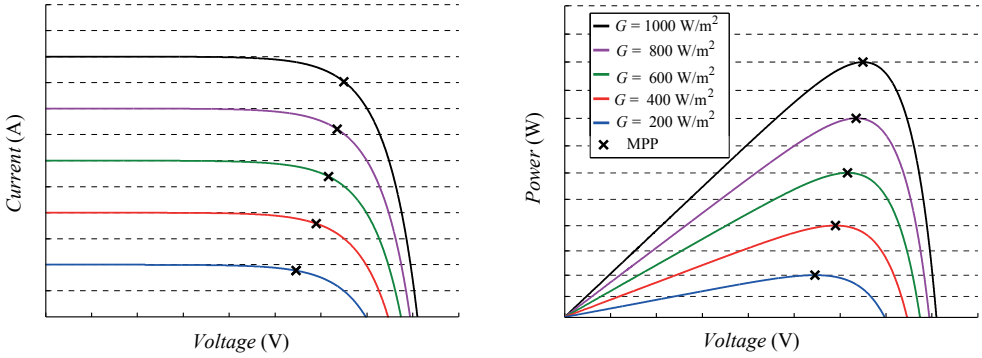


Figure 2.4: PV characteristic curves under irradiance variations ($T = 25°C$) (a) I–V. (b) P–V.

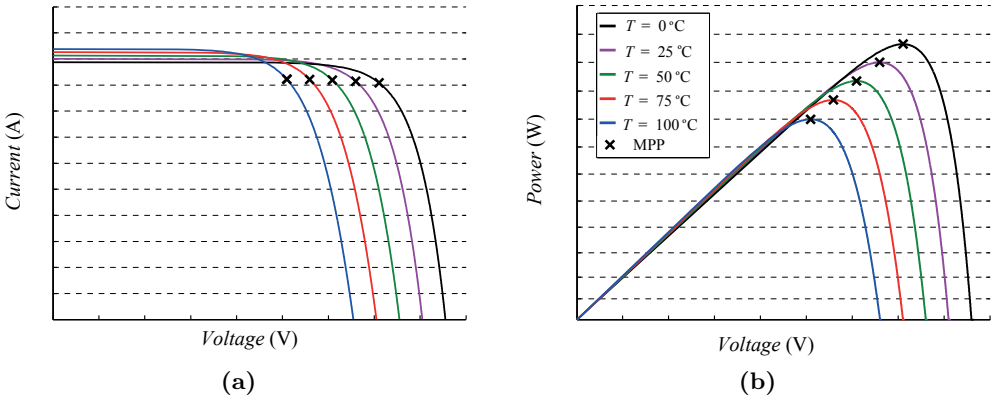
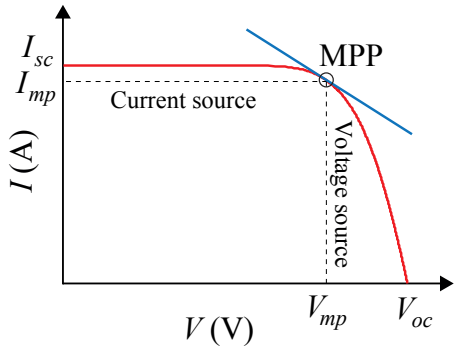


Figure 2.5: PV characteristic curves under temperature variations ($G = 1000$ W/m^2) (a) I–V. (b) P–V.



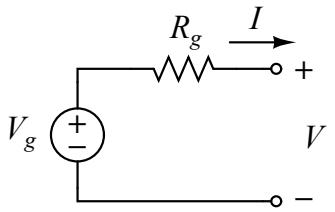
$$I = I_{ph} - I_o \cdot \left(e^{\frac{V+I\cdot R_s}{V_t}} - 1\right) \qquad (2.2)$$

Figure 2.6: Non-linear I–V curve and linear model at the MPP.

In order to ensure stability of the SMPS regulation loop, a linear model of the photovoltaic panel is necessary, which allows to include the input source as a part of the converter. This model can be obtained by using the derivative of the I–V curve (2.2) at the linearization point [12], [14], as shown in (2.3). The linear model is described by the tangent line to the I–V curve at this point (2.4). Figure 2.7 shows the linear equivalent circuit of the PV panel, which is modeled as a voltage source, V_g, with a series resistance, R_g.

$$g = \frac{dI}{dV}\Big|_{\substack{V_{mp}\\ I_{mp}}} = \frac{-I_o}{V_t} \cdot e^{\frac{V_{mp}+I_{mp}\cdot R_s}{V_t}} \tag{2.3}$$

$$I = (-g \cdot V_{mp} + I_{mp}) + g \cdot V \tag{2.4}$$



$$V_g = V_{mp} - \frac{I_{mp}}{g} \tag{2.5}$$

$$R_g = -\frac{1}{g} \tag{2.6}$$

Figure 2.7: Equivalent linearized PV panel.

The PV panel can also be linearized at the current and voltage source regions, and the control loop designed accordingly to fulfill stability margins when PV panel operates in the voltage or current source regions, which will ensure stability of the SMPS regulation loop under all operating conditions. This is shown in Appendix A [13], where a combined control loop for stand-alone PV battery systems is proposed, and the PV panel is linearized at the three operating points—MPP, voltage and current source regions—in order to design the regulation loop to ensure stable operation of the converter under all the PV operating conditions.

2.1.1 Maximum Power Point Tracking (MPPT) Algorithms

Due to the nonlinear characteristic of the PV cells and its low conversion efficiency, it is important to keep the photovoltaic panel operation at its maximum power point, MPP. Therefore, maximum power point tracking algorithms (MPPT) have been a trend research topic in academia and industry. Many MPPT algorithms have been proposed in the literature [15–22]. However, due to their low computational charge, good performance and simple implementation, the most commonly used are perturb & obserb (P&O) and incremental conductance (INC) algorithms, and constant voltage (CV) and constant current (CI) methods.

The most simple methods are the constant voltage (CV) and constant current (CI), also called fractional open-circuit voltage and fractional short-circuit current, respectively. These techniques consist on measuring the PV open circuit voltage or short circuit current and fixing the MPP to a percentage of the measured values [18], [23, 24]. The advantages of these methods are that they require minimal computational power and—unlike the P&O and INC—do not present oscillations around the operating point due to perturbation. However, the disadvantage is that the MPP is not always a fixed percentage of the open circuit voltage or short-circuit current, some energy is lost during the measurements and their performance is poor under fast irradiation changing conditions.

The P&O and INC algorithms are also called “hill-climbing” methods because they are based on finding the “top of the hill” of the P–V characteristic curve, from the sampled PV current and voltage. The basic operation of the P&O algorithm is to periodically

perturb the PV panel voltage and compare the actual and the previous sample of the PV power to determine the direction of the perturbation (increment or decrement). The advantage of this method is the low computational requirement, however, the main disadvantage is the presence of steady state oscillations around the MPP. In order to overcome this limitation, an adaptive perturbation step size and perturbation frequency can be used, which can increase the time response of the algorithm and reduce the ripple around the MPP [25–28].

Similarly, the INC method compares the incremental and the instantaneous conductances of the PV panel in order to decide the direction of the perturbation [29]. The INC method requires higher computational charge than the P&O algorithm however, theoretically, INC is able to determine when the MPP has been found and stop the perturbation, avoiding steady state oscillations around the MPP. Practically, the exact MPP is hardly found and a small marginal error has to be allowed [6],[29], which can be reduced applying variable step size techniques [30, 31].

Both P&O and INC algorithms present the disadvantage of wrong perturbation direction under fast changing irradiation conditions [6], [29], [32]. Very fast irradiation changes of 550 W/m^2 per second were reported in a 20 min period measurement [32]. However, based in a year measurement with 1 Hz sampling rate, realistic variations of irradiation changes were defined in [33], as shown in Table 2.1. If the step of the irradiation change is bigger than the change in power due to the perturbation, the algorithm perturbs in the wrong direction because it assumes that the change in power is an effect of its own action. An improvement of the P&O algorithm presented in [34, 35] proposes an extra measurement of the PV power without any perturbation, in order to determine if the change in power is due to the perturbation or due to an irradiation change.

Effects of partial shading on the PV characteristic curve have been studied in the literature [36–38]. Both P&O and INC algorithms are based on heuristic search, meaning that they only evaluate if the current state is better than the previous one. Therefore, these methods fail finding the MPP when there is local maxima in the P–V characteristic curve due to partial shading conditions. In order to track the global MPP in partial shading conditions [39], improvements to the existing algorithms [40, 41] based on sweeps on the PV I–V curve have been proposed, which allow locating the panel global MPP. In large systems, distributed PV configurations [42, 43] are usually preferred to maximize the system efficiency.

P&O and INC conductance methods perform better at high irradiance levels than at low irradiation conditions due to a reduced slope in the characteristic P–V curve. However, constant methods do not perform as good as hill-climbing algorithms at high irradiation levels, but give better performance at low irradiation conditions. Therefore, the combination of methods is an interesting solution to get good MPPT performance at both high and low irradiance levels [44–46].

The performance of the MPPT methods based on heuristic search, and the speed of the sweeps under partial shading conditions, are directly influenced by the converter regulation loop, i.e. the frequency and the step size of the perturbation will be determined by the settling time of the converter regulation loop. Hence, the importance of maximizing the loop bandwidth and ensuring stability under all operating conditions by using the PV linearized model.

Table 2.1: Categories of irradiance variations

Time scale	Largest realistic variation (W/m^2)
Very fast (within 1 s)	27
Fast (within 5 s)	103
Slow (within 30 s)	441

2.2 LED Lighting Technology

Solid-state lighting (SSL) systems are gradually replacing conventional lighting technologies, like incandescent and fluorescent lamps, due to higher luminous efficacy (lm/W) and lifetime [47]. Important parameters related to the quality of the illumination are correlated color temperature (CCT) and color rendering index (CRI). CCT is a specification of the color appearance, measured in Kelvin, used to describe the color tone of the emitted light compared to the apparent color of a blackbody radiator at a given temperature. CCT ratings below 3200 K are considered warm sources, whereas above 4000 K are considered cool. Temperatures in between are considered neutral. CRI is a numerical scale from 0 to 100 that indicates the ability of the light source to reproduce the object color compared to a reference light source with the same color temperature. Figure 2.8 [48] show the luminous efficiency, lifetime and CRI for different lighting technologies. Light-emitting diode (LED) provide higher efficiency and lifetime than any discharge lamp technology, with excellent color quality and CRI values close to the incandescent lamps. Moreover, LEDs provide easier dimming control than discharge lamps, which makes them the perfect replacement in street lighting applications.

Figure 2.9 [47] shows the efficacy values achieved by white LEDs as well as projections of future efficacies according to OIDA (Optoelectronics Industry Development Association) [49], DOE (U.S. Department of Energy) [50–52] and [53]. However, these targets are by far surpassed, as in 2013 Cree set the performance record with 276 lm/W, and

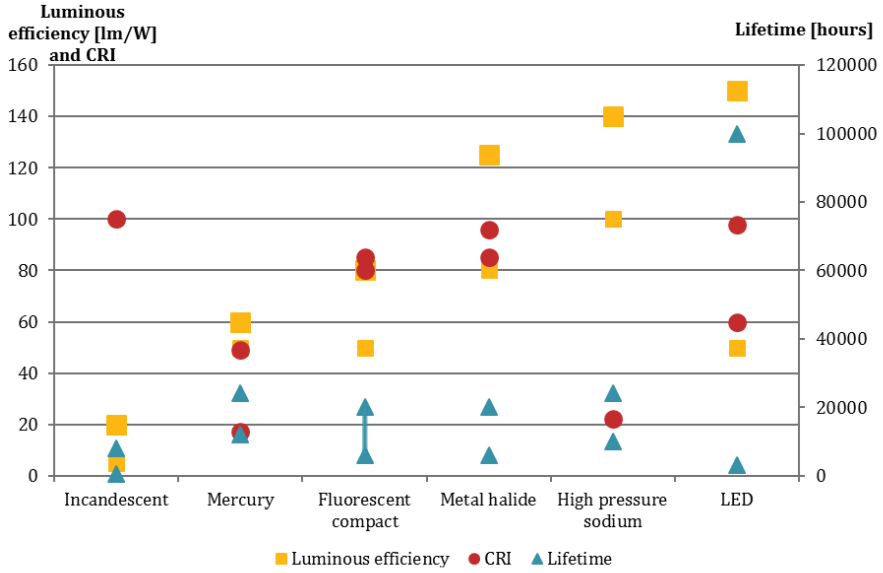


Figure 2.8: Efficiency, lifetime and CRI for different lighting technologies [48].

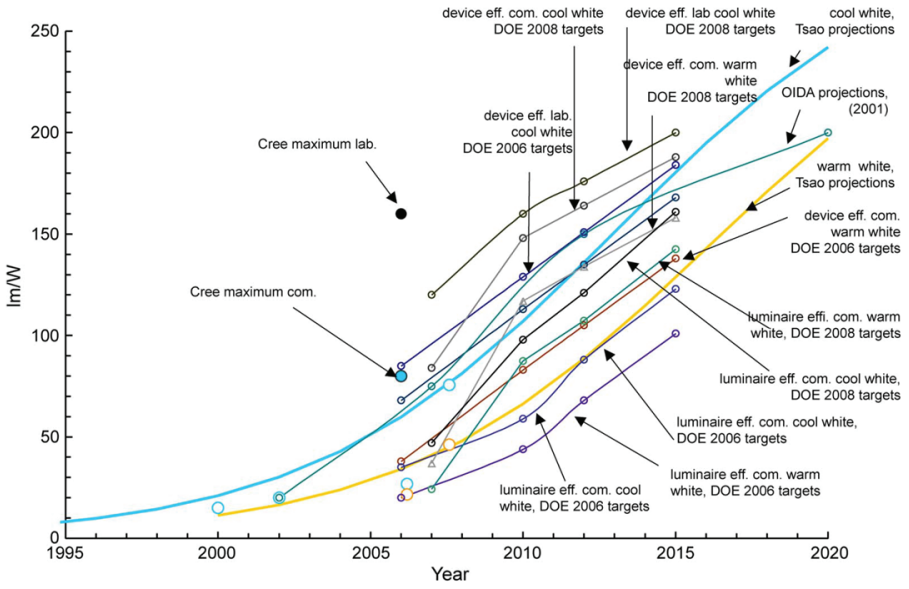


Figure 2.9: Laboratory and commercial efficacy projections for cold and warm white LEDs [47], [49–53].

in 2014 it achieved 303 lm/W in laboratory measurements [54, 55]. Typical commercial LED efficacies are around 90 to 130 lm/W depending on the CCT [56].

The LED I-V characteristic curve is defined by the diode Shockley equation (2.7), and exhibits a non-linear relationship between voltage and current analogue to a solar cell under no illumination, as shown in Figure 2.10a.

$$I_{fw} = I_s \cdot \left(e^{\frac{V_{fw}}{V_t}} - 1 \right) \tag{2.7}$$

where:

I_{fw}: diode forward current.
I_s: saturation current.
V_{fw}: diode forward voltage.
V_t: thermal voltage.

The diode characteristic I–V curve can be linearized around the operating point and modeled as an ideal voltage source with a series resistance as shown in Figure 2.10b. The value of the equivalent voltage source, V_{D0}, is given by the intersection of the tangent line to the I–V curve dc operating point with the voltage axis, and the dynamic resistance is calculated as (2.8).

$$R_{dyn} = \frac{\Delta V}{\Delta I} \tag{2.8}$$

Current control schemes are generally recommended in LED applications [57–60], since controlling the voltage will not ensure constant luminous intensity and the maximum current rating of the device can be exceed, compromising the reliability. First, the output luminous flux presents an almost linear relation with the current device compared to the non-linear characteristic between voltage and current. Second, according to the manufacturer's datasheet, the devices' forward voltage drop as a function of the

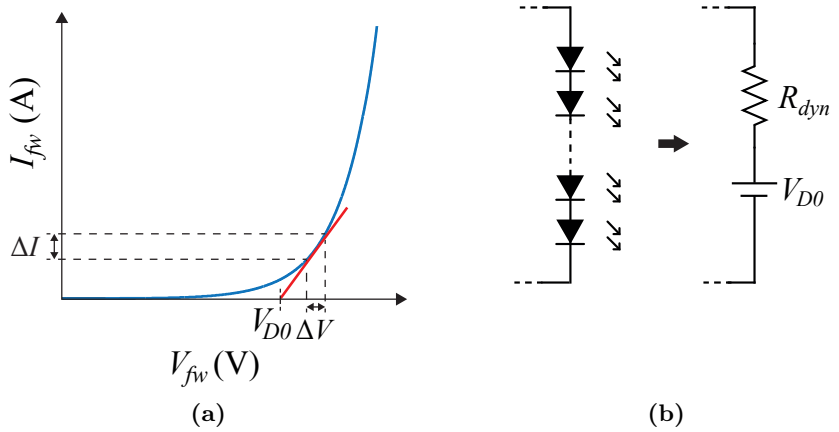


Figure 2.10: (a) LED characteristic I-V curve. (b) Equivalent linearized model.

current can present tolerances up to 20%, making the luminosity control even more challenging. Last but not least, as all *pn* junction devices, LEDs exhibit a negative temperature coefficient, therefore, controlling the voltage can cause the failure of the device due to thermal runaway.

The dimming regulation of the LED current can be performed by using a pulse-width modulated (PWM) or constant current (CI) methods [61]. In the PWM regulation method, the LED luminosity is controlled by directly applying a PWM and adjusting the modulation width. The constant current (CI) or current regulation method (CR) consist of adjusting the LED dc current level to regulate the luminosity output. Constant current regulation method presents a larger variation of the LED chromacity vs. the current level than PWM regulated LED drivers [61, 62], however, PWM techniques require 200 Hz minimum operating frequency to avoid health related issues due to flickering of the light source [63–65].

In order to provide sufficient output illumination single LEDs are combined into arrays to form LED lamps. Series connection is preferred in order to avoid mismatch in the current of parallel connected devices [66, 67]. Due to the phenomenon known as efficiency droop, where LED efficacy decays at high current values and high junction temperatures, in order to achieve high luminous efficiency, LED strings are typically driven at a low current level, which increases the number of required LEDs for the same luminous output.

2.3 Energy Storage Elements

Energy storage elements are often combined with renewable energy sources, like solar or wind, due to their intermittent and unpredictable availability. Different electrochemical energy storage elements are available depending on the application requirements. A review of the different technologies is provided in [68]. The main characteristics according to this review, are summarized in Table 2.2. Lead acid (Pb-Acid) batteries are a mature technology and is usually adopted in low cost implementations, where energy density is not one of the main requirements. Their ruggedness make them the first choice for starting of combustion and explosion engines in automotive applications.

Nickel Cadmiun (Ni-Cd) provide higher power and energy density than Pb-Acid batteries and replaced them in high performance applications; however, in the recent years, they have been replaced by Nickel-metal hydride (Ni-MH) batteries, which offer higher cycle life, higher energy and power density, and lower toxicity. Lithium Ion (Li-Ion) and Lithium Polymer (Li-Po) are the preferred choice in portable applications due to their large energy and power densities and good cycle life, however, they are expensive due to limited lithium resources. Finally, Elechtrochemical double-layer capacitors (EDLC), also known as supercapacitors, act similarly to conventional capacitors, providing low energy density, but a very large power density that, together with a large cycle life and efficiency, makes them the best choice in applications with high dynamics, like regenerative braking in electric vehicles.

Li-Ion solutions provide high energy density and present the optimal choice in portable and stand-alone applications. However, this technology requires from advanced battery management system (BMS), in order to avoid irreversible damage due to overcharge or over-discharge of the battery pack [69–71]. Depending on the battery state-of-charge (SOC), several charge stages need to be implemented as discussed in [72, 73], where current control (CI) is implemented during the first two stages, and voltage regulation (CV) in the last two. The battery SOC determination makes it possible to maximize the utilization of the storage element, while avoiding permanent damage due to overcharge/over-discharge. Additionally, SOC determination provides information to the end user about the remaining operating time in portable applications. A review of existing methods for determination of the SOC and their suitability depending on the field of application is discussed in [74]. The most common method is the Coulomb counter, where the charge flow to the energy storage element is measured to estimate the SOC based on an initial known SOC value. However, this method presents an issue, since not all the energy measured is stored in the element. This is due to the fact that energy losses occur in the element during the charge and discharge stages and they need to be accounted for in order to accurately predict the SOC variations. The second method, is the open circuit V_{oc} measurement method, which makes it possible to determine the element SOC based on the terminal voltage under zero current conditions. This type of measurement is not always viable since, in order to accurately measure V_{oc}, the energy storage element needs an inactivity period. Other common methods are based on impedance or internal resistance measurements; however, their practical

Table 2.2: Characteristics of Most Used Electrochemical Energy Storage Elements

Type	Efficiency $\eta(\%)$	Energy Density (Wh/Kg)	Power Density (W/Kg)	Cycle Life (cycles)	Self Discharge
Pb-Acid	$70-80$	$20-35$	25	$200-2000$	Low
Ni-Cd	$60-90$	$40-60$	$140-180$	$500-2000$	Low
Ni-MH	$50-80$	$60-80$	220	<3000	High
Li-Ion	$70-85$	$100-200$	360	$500-2000$	Med
Li-Po	70	200	$250-1000$	>1200	Med
NaS	70	120	120	2000	-
VRB	80	25	$80-150$	>16000	Negligible
EDLC	95	<50	4000	>50000	Very High

implementation is difficult due to temperature dependence, and measurement complexity due to small variations with SOC, respectively. Electrical circuits with linearized models [75–77], and other methods like neural networks and Kalman filters, provide accurate estimations in large dynamics applications like electric vehicles. However, due to its simplicity and accuracy, if enough recalibration points are given, the Coulomb count method with error compensation is the most common method. The V_{oc} measurement method is often combined with other methods to provide recalibration points.

2.4 Three-Port Converter Topologies

Multiple port converter topologies address the issue of interconnecting several energy sources with a single structure [78], aiming to reduce the conversion stages and increase the system power density and efficiency. Based on this principle, these topologies have attracted research interest in academia and industry; especially, three-port converter (TPC) topologies combining a renewable energy source and an energy storage element. The conventional approach to combine two input sources to a common load is the series-connection of individual converters [79, 80], as shown in Figure 2.11. Figures 2.12a and 2.12b show the integration of multiple input sources as two individual converters parallel-connected at the input or at the output [81–83]. These topologies provide a simple solution, but present the disadvantage of multiple conversion stages, which can act in detriment of the efficiency.

Multi-port topologies can be mainly classified into non-isolated and isolated topologies. The key characteristic of the isolated topologies is the shared output stage [84, 85], which reduces the number of components, increasing the power density. Within this category, fully isolation between all three ports, or partial isolation between two of the ports can be distinguished. Many fully isolated topologies are based on half bridge (HB) [86–88] and full bridge (FB) [89–96] switching cells, coupled through a multi-winding transformer. In order to decouple the inputs and control the power flow, they present

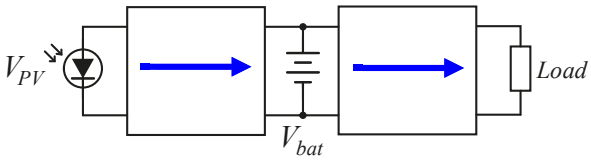


Figure 2.11: Series-connection of individual converters.

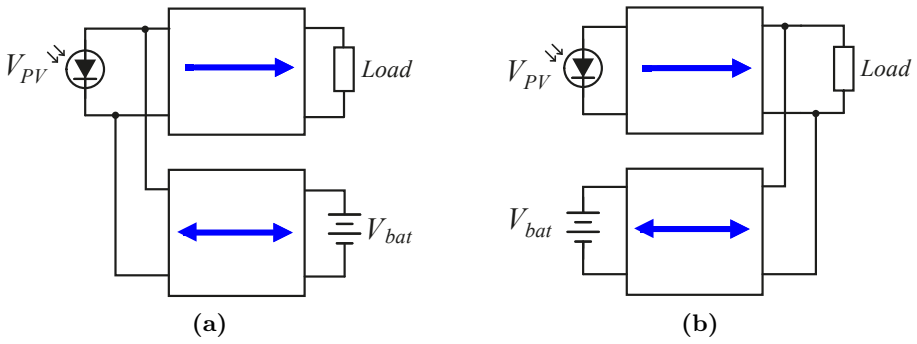


Figure 2.12: Integration of multiple sources (a) parallel input. (b) parallel output.

solutions based on phase-shift [86, 88–96] or phase-shift and duty cycle operation [87].

Partially isolated topologies usually present no isolation between the two input sources and include an isolation transformer to interface with the output load. This configuration is common in applications where an energy storage element is required, and therefore, a bidirectional converter is integrated [97].

Figure 2.13 illustrates a TPC topology to interface a renewable energy source, a bidirectional port and a load in a single structure. Different power flows can take place in the system depending on the availability of the renewable energy source and the load demand. The converter will operate in dual input (DI) mode when the load demand is higher than the available power from the renewable energy source ($P_{PV} < P_{Load}$), and the battery delivers the extra energy, as shown in Figure 2.14a. The converter will operate in dual output (DO) mode when the available power of the renewable energy source is higher than the load demand ($P_{PV} > P_{Load}$), and the battery has to store the excess energy, as illustrated in Figure 2.14b. Single-input single-output (SISO) conversion can also take place among the three conversion paths.

As in the fully isolated topologies, many of the proposed TPC are based on HB [98–102] and FB [103–107] switching cells. In order to obtain the bidirectional port, the FB bridge switching cell is reutilized to implement an interleaved buck-boost converter providing a bidirectional port for the energy storage [103, 104, 106, 107]. Integration of an LLC resonant tank on the FB-interleaved-buck-boost configuration is discussed in [108] and extended to a TPC topology in [109, 110]. A systematic method for deriving multiport topologies based on the integration of FB and bidirectional converters is proposed in [97]. The method is extended and applied to a buck-boost four-port converter, including two PV sources and an energy storage element. Reutilization of the transformer's magnetizing inductance as a power interface between the non isolated ports is presented in [101, 102] and [105], for HB and FB configurations, respectively, which offer high integration and low component number. A TPC based on an im-

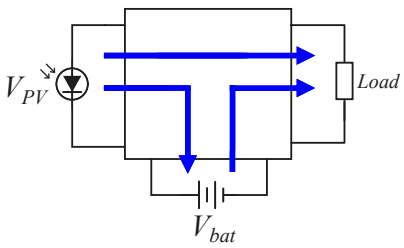


Figure 2.13: Integration of multiple sources in a single structure.

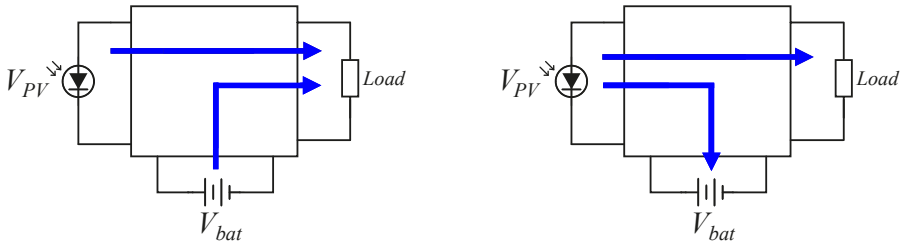


Figure 2.14: (a) Dual input (DI) mode. (b) Dual output (DO) mode.

proved flyback-forward topology discussed in [111], reutilizes the leakage inductance of two coupled inductors to transfer power to the output port. However, in this solutions the power delivering capability from the battery port to the output load is limited due to the flyback operation. In order to regulate two of the converter ports, duty cycle and phase-shift control schemes are adopted [103, 104, 106, 107, 111], where the duty cycle of the primary switches is used to regulate the power flow of the two independent sources, and the phase-shift between the switching legs to control the power flow to the output port. In order to reduce the current ripple at the input ports, regulation from the secondary side is proposed in [112], at the expense of two extra active switches at the rectifier side.

Depending on the application, isolation may not be required; non-isolated topologies offer lower component number than isolated topologies, which makes them more suitable for low power stand-alone applications. Non-isolated TPC configurations are based on the basic buck, boost and buck-boost converters. The work presented in [113–115] derives TPC structures by adding a switch-diode pair to reconfigure the power flow in a two converter DO structure. A family of single inductor TPC and its dynamical modeling and control are presented in [116] and [117], respectively. This approach is based on inserting a switch/diode/energy storage element cell in the switching node of conventional SISO topologies. An interesting solution for deriving non-isolated TPC from dual-input (DIC) and dual-output converters (DOC), based on component sharing and the combination of power flows with similar characteristics, is discussed in [118, 119] and applied in [120]. This method starts by reducing the traditional con-

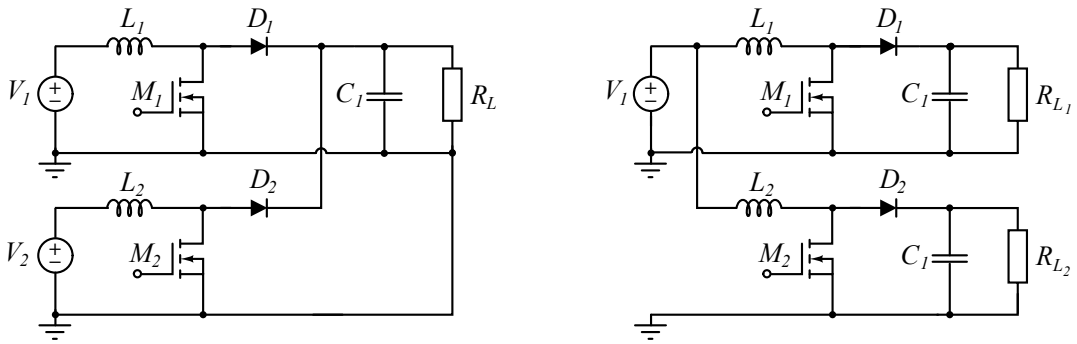


Figure 2.15: Individual converters configuration [118] (a) Dual input (DIC) converters. (b) Dual output (DOC) converters.

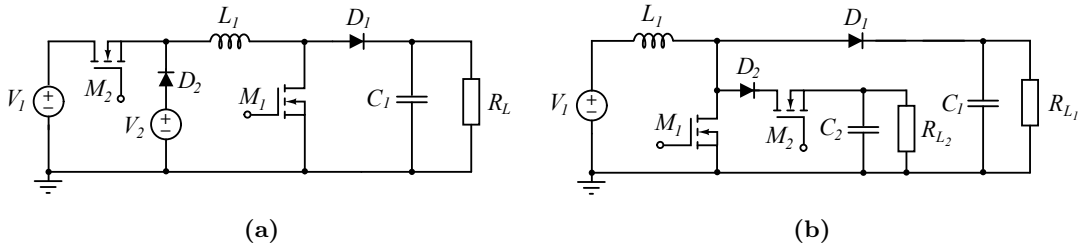


Figure 2.16: Combined converters configuration [118] (a) Dual input (DI) mode. (b) Dual output (DO) mode.

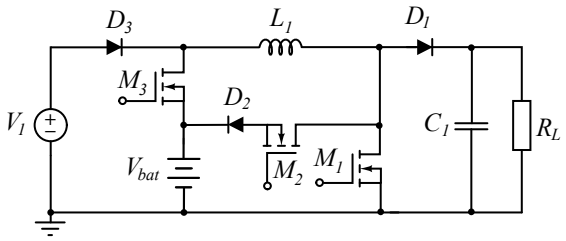


Figure 2.17: Integration of DIC and DOC in a single inductor TPC structure [118].

figurations formed by separate DIC and DOC, as shown in Figure 2.15a and Figure 2.15b [118], into a reduced structure with a single magnetic component, whose charge and discharge subintervals are shared between the input sources or the output loads [118], as illustrated in Figure 2.16a and Figure 2.16b , respectively. By further combining these type of solutions, it is possible to generate a TPC topology with a single magnetic component [118], as shown in Figure 2.17 .

3

Low-Power Stand-Alone Light-to-Light System

3.1 System analysis

The integration of solar cells, energy storage elements and LEDs in a stand-alone solar powered lighting system, combines the advantages of clean off-grid electricity and high efficiency autonomous light-to-light (LtL) conversion. Stand-alone solar powered LED systems have attracted research interest in the last decades [80, 121–124], especially street lighting applications [125–129].

The system under analysis is a low-power stand-alone PV-LED structure for street lighting applications. In locations far from the equator, solar powered systems are challenging due to the intrinsic limitations of the geographic location, as illustrated in Figure 3.1 [130], where the low irradiation levels during winter in a northern latitude can be observed. In order to maximize the solar resource, the aim is to achieve high efficiency energy conversion at low irradiation conditions. In order to develop a simulation tool for correct dimensioning of the system, a characterization of the different elements under field test conditions is presented in Appendices B [131] and C [132]. Appendices

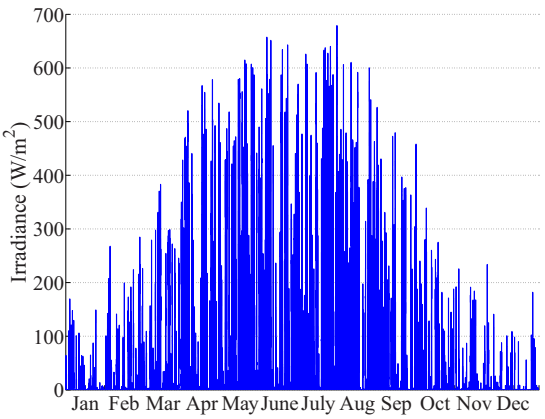


Figure 3.1: Annual solar irradiation pattern in a northern latitude [130].

D and E discuss about the challenges of designing high efficient solar powered LED systems.

In the low-power system under study, in order to maximize the energy conversion at low power levels, it is important to reduce switching, gate and any other source of idle losses. Moreover, due to the low voltage operation of the system, it is interesting to avoid any voltage drop, and therefore, the use of diodes in the power flow path. As discussed in Section 2.4, the conventional approach to interconnect the three components—PV panel, battery and LEDs—is to implement a cascade configuration [80, 121–127]. Although this solution present the disadvantage of series-connected conversion stages, it provides easier implementation of the control loops—MPPT, BMS and CI—than TPC topologies, since the control variables are completely decoupled. On the other hand, non isolated TPC topologies require extra switches and diodes to provide controllability and to configure the power flow path. Moreover, in many cases, there are switches that are not referenced to ground [118, 119], which increases complexity and losses in the drive circuitry.

The LtL structure under analysis is composed of two parallel-connected monocrystalline PV panels, a Li-ion battery and 8 series-connected high bright white LEDs. The specifications of the low-power LtL system are presented in Table 3.1.

Appendix F [133] presents a comparison of TPC topologies for a low-power stand-alone PV system based on components stress factor (CSF) analysis. CSF analysis [134–136] provides an estimation of the stress distribution in the semiconductors, magnetic components and capacitors of the converter. It is calculated with the maximum voltage across the devices and the *rms* current, and scaled to the processed power. The contribution of each component to the CSF is determined using a weighting factor, which represents the distribution of the resources among the components. This numerical method is correlated to the converter conduction losses and can give an estimation of the converter efficiency. A series-connected solution and two TPC configurations are evaluated. The comparison is performed with the generated power of the irradiation pattern of a day at the input, and two different LED patterns at the output, one intended for street lighting and the other for street signalling. The different LED patterns produce different overlaps between the PV and LED power flows, which varies the converter DI, DO and SISO modes' period. According to the results, the cascaded solution

Table 3.1: Stand-alone LtL System Specifications

P_{PV-max}	10.92 W
V_{mp}	6.5 V
I_{mp}	1.68 A
V_{oc}	8.10 V
I_{sc}	1.86 A
V_{bat}	3.6 V
Battery capacity	4.5 Ah
$P_{LED-max}$	26.4 W
LED V_{fw}	8 x (2.6 to 3.3) V
LED $I_{fw_{max}}$	1000 mA

provides the lowest CSF, even for the LED pattern that requires more DI operation. This is due to the fact that TPC need extra switching elements, which has a negative impact on the resources' weight distribution, even though the cascade solution need to process the PV power twice. From this analysis is clear that the cascade solution will achieve better performance than TPC topologies as the power flow from the PV panel to the LED is reduced. Therefore, it is interesting to investigate the weight of this power flow in the application under study.

The threshold value to turn-on/off the LED lighting fixture, is determined by the minimum ambient light level established by street lighting regulations [137–139]. According to [137], the required maximum street lighting illuminance in Denmark corresponds to LE1 class—intersections in motorized roads— with a recommended value of 45 lux. Taking into account that the solar irradiation constant is equal to 1350 W/m^2, and the photometric illuminance of the Sun is equal to $1.2 \cdot 10^5$ lux [140], in order to ensure the specified minimum amount of illuminance, the LED fixture needs to be turned-on when the solar irradiance level is equal to 0.5 W/m^2, which corresponds to a PV panel output power of 1.3 mW. This determines that, in this specific application, DI mode operation will never occur, since the power obtained from the PV panel at these irradiation conditions is extremely low for the size of the system.

As no direct sunlight conversion is required, the system allows for the sequential separation of the energy power flows from the PV to the battery, and from the battery to the LED lighting. Hence, the conventional solution of two cascaded converters can be combined into a single structure with shared components [128, 129], as shown in Figure 3.2. Magnetic components play an important role on the converter size, price and weight. The proposed solution is a combination of two converters, where the magnetic component is shared between the two operation modes by reconfiguring the power flow path, depending on the availability of the energy source.

In order to drive the LED lamp from the battery port, a high step-up converter topology is required. The use of tapped-inductors avoids extreme duty cycles and high current stress in the components, which reduces switching and conduction losses. Figure 3.3 shows the schematic of the implemented stand-alone LtL system. Switches M_4 and M_5 are utilized to reconfigure the power flow path depending on the availability of the renewable energy. Therefore, these switches do not contribute to the converter switching losses, which makes it possible to select a device with a large die size to minimize the extra inserted conduction losses. When the renewable source is available, the circuit operates as a synchronous buck converter from the PV panel to the battery, as shown in Figure 3.4a. In this power flow, M_4 is off, M_5 is fully on, and M_1 and M_2 are the main switch and the synchronous rectifier, respectively. During the night time,

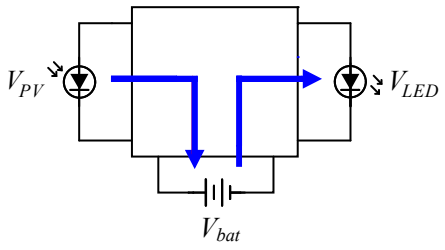


Figure 3.2: Stand-Alone PV-LED LtL system.

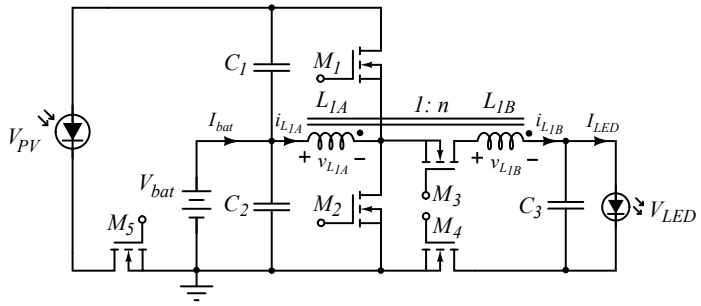


Figure 3.3: Schematic of low-power stand-alone LtL system.

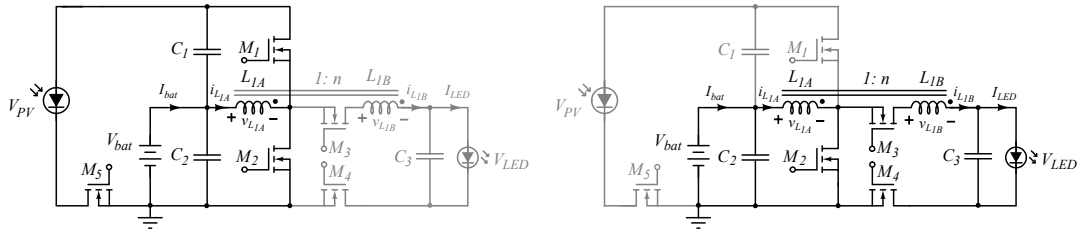


Figure 3.4: Schematic of low-power stand-alone LtL system (a) PV panel to battery port power flow: buck mode (b) battery port to LED lamp power flow: tapped boost mode.

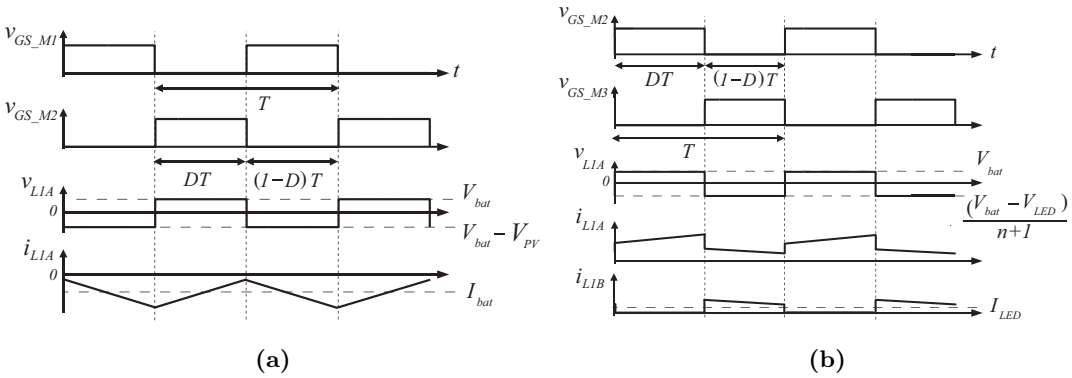


Figure 3.5: LtL system operating waveforms (a) PV panel to battery port power flow: buck mode (b) battery port to LED lamp power flow: tapped boost mode.

the structure is configured as a synchronous tapped boost converter from the battery to the LED port, as illustrated in Figure 3.4b, reutilizing M_2 and winding L_{1A}. In this power flow, M_5 is off, M_4 is fully on, and M_2 and M_3 are the main switch and synchronous rectifier, respectively.

Figure 3.5a and Figure 3.5b shows the converter operating waveforms in buck and tapped boost modes, which correspond to the power flow from the PV to the battery and from the battery to the LED port, respectively.

The proposed solution to interconnect the PV panel, the energy storage and the LED lighting makes the power stage of each power flow path to feature low number of compo-

nents and synchronous rectification, which allows for high efficiency energy conversion in both operation modes. The technology is part of a patent application, included in Appendix G.

The power flow from the PV panel to the battery (buck mode) is designed for a maximum power of $P_{PV-max} = 10.9$ W. The power from the battery to the LED driver (tapped boost mode) is designed for a maximum power of $P_{LED-max} = 26.4$ W, as presented in Table 3.1. Inductor L_{1A} is the power interface in the PV panel to the battery power flow (buck mode), and reutilized as the coupled inductors magnetic structure (L_{1A}, L_{1B}) in the battery to LED power flow (tapped boost mode). The design of the magnetic component is determined by the specifications of the LED driver. This stage is designed to be able to drive the LED lamp at the maximum drive current allowed by the LED specifications.

3.2 Tapped Boost Magnetic Structures Analysis

An experimental analysis of different tapped-inductor magnetic structures in terms of leakage inductance and parasitic capacitances is discussed in this section, which is extended in Appendix H [141]. Planar magnetic components can achieve low leakage inductance by applying extensive interleaving techniques [142], however, heavy winding interleaving causes high parasitic capacitances [143, 144]. These parasitic components will have a negative effect on the converter efficiency.

The evaluated magnetic components are a planar structure ELP32/6/20 with full interleaving winding arrangement, and three wire-wound ETD29/16/10 with different winding arrangements—full, partial and no interleaving—as shown in Figure 3.6. The selected cores use soft ferrite material N87 from Epcos [145]. To perform a fair comparison, structures with similar core and copper volume are selected ($V_{e-ELP} = 5350$ mm^3, $V_{e-ETD} = 5390$ mm^3, $V_{cu-ELP} = 1523$ mm^3 and $V_{cu-ETD} = 1551$ mm^3). The number of turns (N_{L1A}/N_{L1B}) are selected to produce approximately the same core loss in both structures. The PCB windings are implemented using 270 µm copper thickness in 8 layers with a full interleaving technique (PSPSPSPS, where P and S stands for primary and secondary windings, respectively). The ETD structure, with a copper thickness of $d = 0.7$ mm, present different winding arrangements (PSPS, PSSP and PPSS) implemented in a U-type winding scheme, which helps reducing the leakage inductance, however, increases the parasitic capacitances compared to the Z-type winding [146]. The characteristic parameters of the implemented structures are measured with an impedance analyzer Agilent 4294A, as shown in Table 3.2. Full interleaving techniques

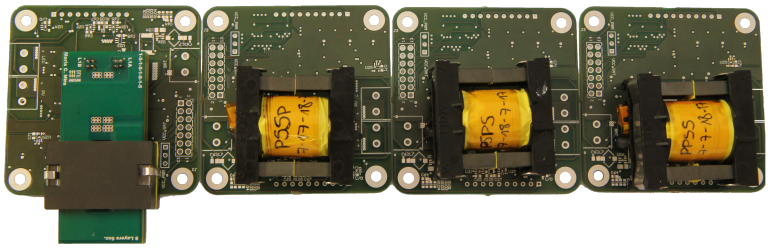


Figure 3.6: Magnetic structures arrangement ELP32/6/20 (left) and 3 wire-wound structures ETD29/16/10 with different winding arrangements.

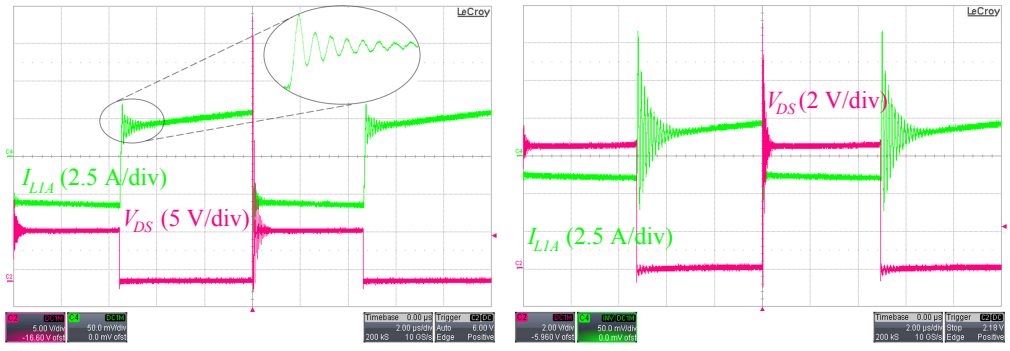
Table 3.2: Characteristic Parameters of the Implemented Magnetic Structures @ 20 kHz

Core Type - N_{L1A}/N_{L1B} (winding arrangement)	L_{1A} [µH]	L_{lk} [nH]	$C_p + C_s n^2$ [nF]	$C_{pri-sec}$ [nF]
ETD29 - 7/35 (PSPS)	18.64	87.20	0.50	0.19
ETD29 - 7/35 (PSSP)	19.48	97.44	1.04	0.15
ETD29 - 7/35 (PPSS)	18.70	199.20	0.73	0.07
ELP32 - 4/20 2 PCB parallel (PSPSPSPS)	18.56	18.40	4.95	2.78

considerably reduces the leakage inductance, as it can be observed in the wire-wound structures with and without interleaving, where a reduction of 56.2% can be achieved in the full interleaving arrangement compared to the non interleaved. The lowest leakage inductance value is achieved with the planar magnetic structure, however, this structure present the highest primary (C_p) and primary to secondary ($C_{pri-sec}$) parasitic capacitances.

The effect of the leakage inductance and parasitic capacitances can be observed in the operating waveforms of the tapped boost stage. Figure 3.7a and Figure 3.7b show the inductor current (i_{L1A}) and drain to source voltage of switch M_2 for the wire-wound structure with no interleaving and the planar magnetics with full interleaving arrangement, respectively. The stored energy in the leakage inductance can be observed in the spike of the drain to source voltage of M_2 at turn-off. The effect of the magnetic component parasitic capacitances can be observed at the turn-on event of MOSFET M_2. At this event, a change in the energy stored in the parasitic capacitances will produce the same amount of energy loss in the MOSFET's channel and circuit parasitic resistances.

Figure 3.8 shows the efficiency measurements of the tapped boost power stage, measured with 6 $^1/_2$ digit multimeters Agilent 34410A. Note that this measurement is performed with a different battery than the specified in Table 3.1 ($V_{bat} = 3.2$ V). The primary to secondary interwinding capacitance is subjected to high voltage stress in the topology. This effect is observed in the planar magnetics efficiency measurement, which penalizes



(a) **(b)**

Figure 3.7: Tapped boost stage operating waveforms. Time scale: 2 µs/div. (a) ETD wire-wound structure with no interleaving (b) Planar magnetics with full interleaving winding arrangement.

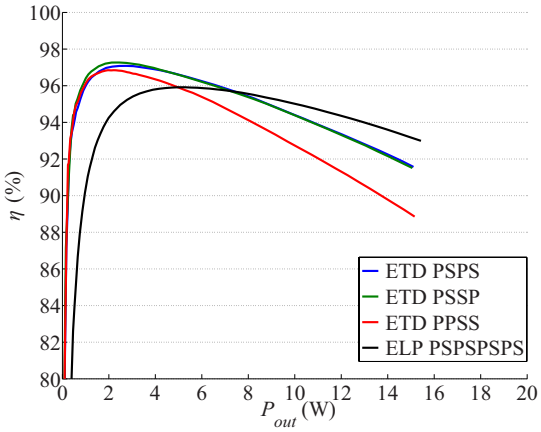


Figure 3.8: Efficiency measurement of the tapped boost stage for different magnetic structures and winding arrangements.

the efficiency at low output power levels. However, the reduced parasitic inductance of the planar structure makes this implementation outperform the wire-wound structures at high power levels. The different winding arrangements of the wire-wound structure perform similarly at low power levels, but the high leakage inductance of the non interleaved arrangement, penalizes the efficiency at higher power levels. In the LtL system under study, the preferred magnetic component is the ETD wire-wound structure with partial interleaving arrangement (PSSP). This solution gives the best performance at low power levels, due to the reduced interwinding capacitance, while offering a good compromise in terms of leakage inductance for the efficiency at high power levels.

3.3 Semiconductor Evaluation

At low power levels, the semiconductor gate and capacitive switching losses are one of the main loss contribution. These losses are difficult to calculate since they depend on the input and output MOSFET capacitances, C_{iss} and C_{oss}, which are highly nonlinear. Analytical models to calculate switching loss have been proposed [147], however, a measurement of the device energy loss at the exact operating conditions can be significantly more accurate [148]. In this section, an evaluation of low voltage Si MOSFETs based on dynamic characterization is discussed; further details are presented in Appendix I [149]. This characterization helps to develop an accurate semiconductor loss breakdown, which can be used for component selection and optimization of the system under different irradiance patterns and LED illumination profiles.

The evaluated MOSFETs are selected based on the required blocking voltage in each power flow configuration. In the PV to battery power flow (buck mode), the switches must withstand a maximum voltage determined by the PV open circuit voltage (V_{oc}). In the battery to LED power flow (tapped boost mode), the main switch blocking voltage is set by $((n \cdot V_{bat} + V_{LED})/(n+1))$ and $(n \cdot V_{bat} + V_{LED})$ for the synchronous rectifier, where n is the coupled inductors transformation ratio. The selected devices are 25 V for MOSFETs M_1 and M_2, and 60 V for MOSFET M_3. The characteristic parameters of the devices under test (DUT) are presented in Table 3.3. In order to investigate the effect of the parasitic components of the magnetic structures in the switching losses, the evaluation is performed with the wire-wound structure with no interleaving and

Table 3.3: Characteristic Parameters of the Devices Under Test

	V_{DS}	R_{DS} @ V_{GS} = 4.5 V	Q_G @ V_{GS} = 5 V	C_{oss}
IRFH4213	25 V	1.9 mΩ	30 nC @ V_{DS} = 13 V, I_D = 50 A	1250 pF @ V_{DS} =6.5 V
BSC050NE2LS	25 V	5 mΩ	5.5 nC @ V_{DS} = 12 V, I_D = 30 A	450 pF @ V_{DS} = 6.5 V
FDM5362L	60 V	74 mΩ	8.7 nC @ V_{DS} =36 V, I_D =17.6 A	68 pF @ V_{DS} = 45 V
Si7120DN	60 V	28 mΩ	16 nC @ V_{DS} = 10 V, I_D =10 A	136 pF @ V_{DS} =45 V

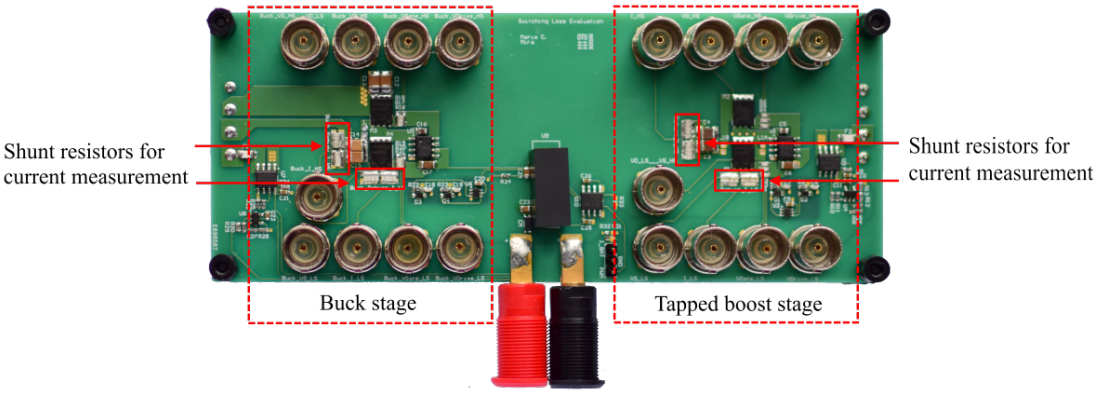


Figure 3.9: Switching loss evaluation board.

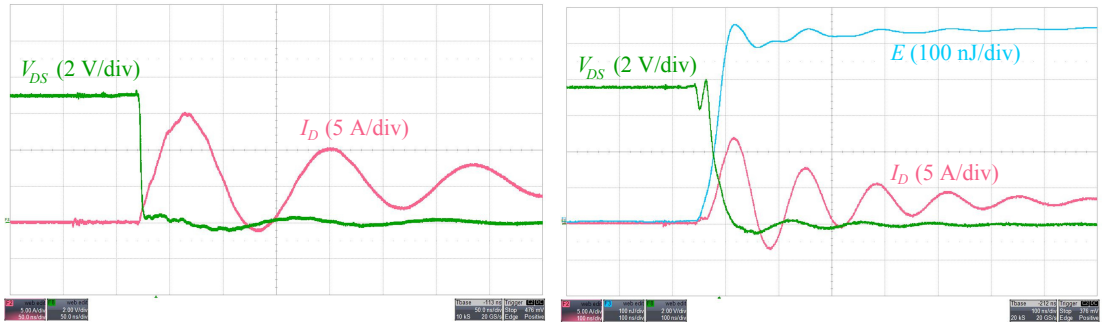
the planar magnetics with full interleaving arrangement, which represent the extreme conditions in terms of leakage inductance and parasitic capacitances, respectively.

The switching loss evaluation board is shown in Figure 3.9, which consists of two power stages, buck and tapped boost, corresponding to the PV to battery and battery to LED power flow paths, respectively. The prototype is designed using 4 layer printed circuit board (PCB) to minimize the areas of the high ac current paths. The current measurement is performed with a high bandwidth low intrusive method, as presented in [150–152]. The method is based on flat current shunt resistors and a pick-up wire strategically placed to minimize the inductive coupling into the measurement loop.

3.3.1 Battery to LED Power Flow

The power flow from the battery to the LED port corresponds to the LtL system operating in tapped boost mode. The tapped boost stage is evaluated with the pair BSC050-FDM5362 and IRFH4213-Si7120, for the planar magnetics and the wire-wound structures. The characterization is performed with the LED lamp as a load, since due to the characteristic I–V LED curve, the output voltage will increase with the output power.

Using the characterization data, an evaluation of the devices is performed by calculating the switching and conduction losses. The switching loss is calculated based on the



(a) (b)

Figure 3.10: Tapped boost stage measured turn-on event with planar magnetics (a) BSC050-Si7120 devices. Time scale: 50 ns/div. (b) IRFH4213-Si7120 devices. Time scale: 100 ns/div.

measured energy, for a switching frequency of $f_{sw} = 100$ kHz, as (3.1). The conduction losses are calculated with the root mean square (rms) current value and the devices' on-resistance, as (3.2). The gate drive loss energy is measured in the characterization setup and calculated as 9.2 mW and 26.6 mW for the BSC050-FDM5362 and IRFH4213-Si7120 combination, respectively.

$$P_{sw} = f_{sw} \cdot (E_{turn-on} + E_{turn-off} + E_{gate}) \tag{3.1}$$

$$P_{cond} = {I_{rms}}^2 \cdot R_{DS-on} \tag{3.2}$$

Figure 3.10a and Figure 3.10b show the turn-on event of the tapped boost stage with the planar magnetics and the pair BSC050-Si7120 and IRFH4213-Si7120, respectively. As it can be observed, the increased switching speed of the BSC050 devices compared to the IRFH4213, results in zero-current switching (ZCS) conditions at the turn-on event. In the wire-wound structure, the increased leakage inductance delays the current transition resulting in ZCS conditions for all the evaluated devices. However, it is important to notice that, even there is ZCS conditions in this switching event, the energy stored in the parasitic capacitance of the magnetic structure, will resonate with the component leakage inductance until is dissipated in the circuit as resistive loss. The ZCS operation, removes these losses from the semiconductor, but does not improve the overall efficiency.

Figure 3.11a and Figure 3.11b shows the semiconductor evaluation of the tapped boost stage with the planar magnetics and the wire-wound structure, respectively. The efficiency loss (η_{loss}) represents the component power loss contribution to the converter efficiency loss, which can be calculated by normalizing the power loss to the converter output power as (3.3).

$$\eta_{loss} = \frac{P_{loss}}{P_{out}} \cdot 100 \quad [\%] \tag{3.3}$$

As it can be observed from comparing the switching energy loss at low power levels, the large parasitic capacitances of the coupled inductors in the planar magnetic structure, penalizes the efficiency loss at low power levels. The effect becomes worse with the IRFH4213-Si7120 pair, due to the reduced switching speed of the devices. The effect of the parasitic capacitances with the BSC050-FDM5362 are not visible on the semiconductor loss due to the ZCS conditions. However, the losses during the charge process

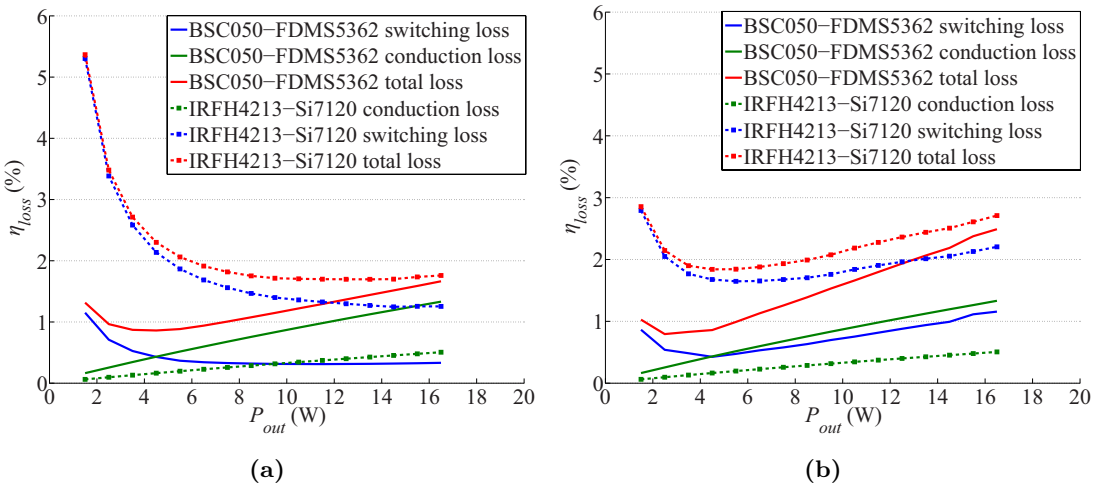


Figure 3.11: Tapped boost stage semiconductor calculated efficiency loss based on measured switching energy (a) planar magnetic coupled inductors (b) wire-wound structure.

will be dissipated in the circuit parasitic resistances. The large leakage inductance of the wire-wound structure has a negative effect on the turn-off losses and causes the switching loss to increase at high power levels. The pair BSC050-FDM5362 offer better performance than the IRFH4213-Si7120 combination over the evaluated power range. Moreover, they achieve almost 2% efficiency improvement at low power levels with the wire-wound coupled inductors, which makes them more suitable for the evaluated application.

3.3.2 PV to Battery Power Flow

The power flow from the PV to the battery port corresponds to the LtL system operating in buck mode. The buck stage characterization is performed with a pair of the 25 V devices IRFH4213 and BSC050, as the main switch and the synchronous rectifier. The voltage at the input port is considered fixed at $V_{in} = 6.5$ V, which is the voltage of the PV panel at the *MPP* @ 1000 W/m^2 and $T = 25$°C. The voltage at the battery port will vary depending on the load current and the SOC. In order to maintain a stable voltage to perform the measurements, a custom build electronic load is designed and implemented. The details are presented in Appendix I.

The gate drive loss energy is measured in the characterization and calculated as 26 mW and 6.6 mW for the IRFH4213 and the BSC050, respectively. This loss represent an important contribution to the total loss and cannot be neglected in a low-power system.

Figure 3.12 shows a comparison of the semiconductor efficiency loss as a function of the power in the buck stage with a pair of IRFH4213 and BSC050 devices. As it can be observed, the IRFH4213 pair presents 3 times more switching losses than the BSC050 at low power levels, which corresponds to a larger gate charge and output capacitance. The BSC050 presents higher on-resistance and, therefore, higher conduction losses than the IRFH4213. However, the BSC050 presents lower total semiconductor loss for the whole power range, due to a reduced switching loss. The IRFH4213 switching losses dominate over the conduction losses at all power levels, which indicates that the device's

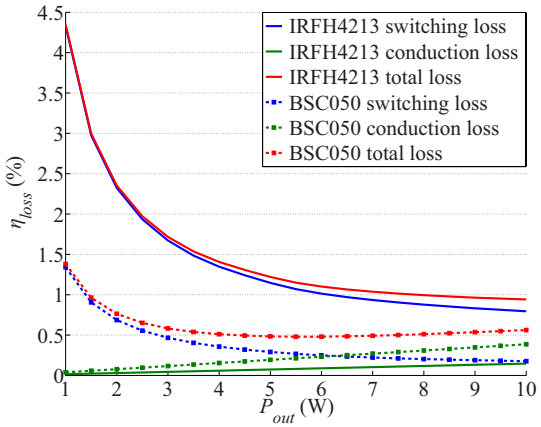


Figure 3.12: Buck stage calculated efficiency loss (based on measured switching energy) for IRFH4213 and BSC050 devices.

die size is too large for this application. The device selection is based on Q_G and R_{DS} trade-off, with special interest in achieving reduced gate and capacitive loss, however, due to the limited selection of devices for low-power applications, the BSC050 still presents a large die size for the application under study.

3.4 Prototype Implementation

In this section the implementation of the low-power stand-alone LtL prototype is discussed. Figure 3.13 shows the schematic of the LtL prototype. The different regulation loops of the power stage are implemented digitally by means of a mixed-signal microcontroller MSP430F5172, which claims ultra-low power consumption of 224 µA/MHz. The MSP430 can operate with a clock frequency up to 25 MHz, provides high-resolution PWM—3.9 ns tick resolution with a digitally controlled oscillator (DCO)—and 10 bit analog-to-digital conversion (ADC) modules. This solution provides easy implementation of the MPPT algorithm and gives flexibility to implement different management system configurations.

Voltages of the PV panel and the battery are monitored. The current of the battery is measured with a Hall effect current sensor (ACS711) with bidirectional operation. The battery current measurement is used for the MPPT algorithm and in the regulation loops of both power flow paths. After the conditioning, the signals are low-pass filtered ($f_c = 10$ kHz) to avoid noise at the MSP430 ADC inputs. A P&O MPPT algorithm is implemented in the MPS430. The MPPT is performed at the battery port, therefore, the tracking algorithm observes the converter output power, maximizing the efficiency of the complete system—PV panel and power stage—instead of the PV panel. A closed loop control to regulate the PV panel voltage is preferred over the direct duty cycle technique [14]. The closed loop controller determines the properties of the system response—settling time, overshoot, etc—and can be designed in accordance with the step and frequency parameters of the MPPT algorithm. As discussed in Section 2.1, voltage regulation of the PV panel is preferred over current control, since the input voltage presents small variation with irradiation changes.

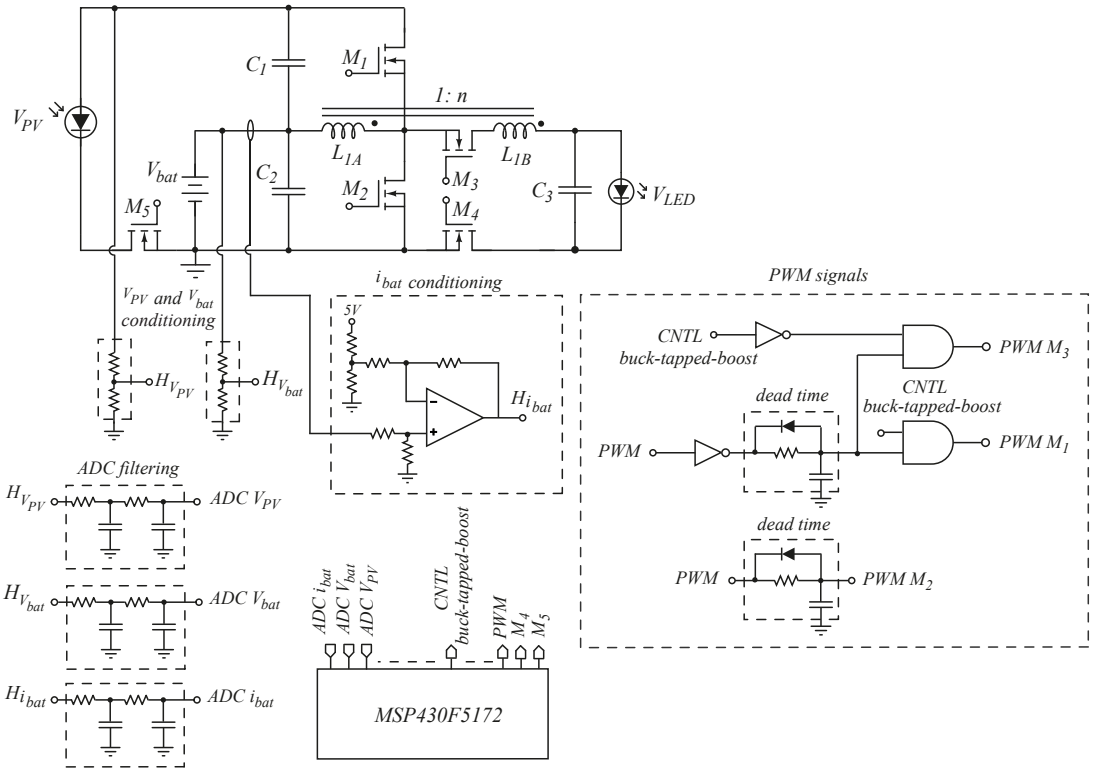


Figure 3.13: Low-power stand-alone LtL schematic.

It is noteworthy to observe that regulating the converter output current will result in erratic operation of the controller when working with the MPPT algorithm. This can be observed in the following way. Assuming that the *MPP* has been reached, when the MPPT algorithm perturbs by increasing the battery current reference, the PV output power will decrease, decreasing the battery current and making the current controller to further increase its ouput until it saturates and the PV panel reaches short circuit conditions.

The different converter plant transfer functions are calculated using state-space modeling [153]. Several regulation loops are implemented on the PV to battery power flow: duty cycle-to-input voltage ($G_{v_{PV}d}$) for the PV panel regulation loop, duty cycle-to-output voltage ($G_{v_{bat}d}$) and duty cycle-to-inductor current ($G_{i_{L1A}d}$) for CV and CI of the BMS on the battery side. In the tapped boost stage, LED constant current regulation (CI) is performed by controlling the inductor current ($G_{i_{L1A}d}$). This method is preferred over PWM dimming regulation due to lower control loop bandwidth requirement and, consequently, lower microcontroller computational demand. It is noteworthy that, due to the discontinuity of the tapped boost inductor current, the transfer function is derived using the magnetic flux in the core [154], which provides a continuous state-space variable for the mathematical modeling. Analog controllers are designed for each of the converter plant transfer functions and moved to the z-domain using Tustin's transformation [155]. The digital controller transfer functions, represented by a ratio of polinomials in z-domain, are implemented in the MSP430.

Figure 3.14 shows the top and bottom sides of the PCB implementation and Table 3.4 presents the main components of the LtL prototype.

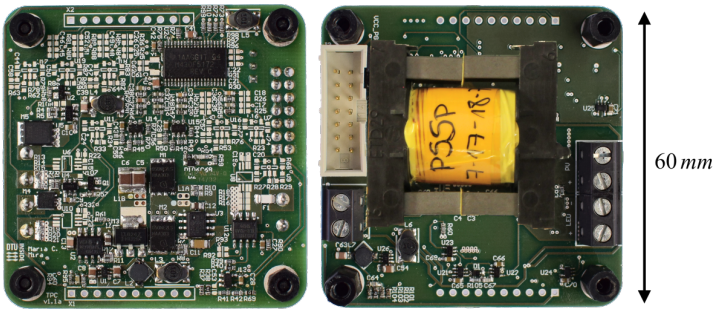


Figure 3.14: Low-power stand-alone LtL prototype.

Table 3.4: Power Stage LtL Sytem Components.

gate driver	MCP14700
M_1, M_2	BSC050NE2LS
M_3	AUIRL024Z
M_4	BSZ105N04NS
M_5	IRFH4213
C_1, C_2	2 x 47 µF 10 V X7R MLLC
C_3	2 x 10 µF 10 V X7R MLLC
core type	ETD29/16/10
L_{1A}	19.5 µH
N_{L1A}/N_{L1B}	7/35 (PSSP)
n	5

3.5 Loss Distribution Analysis

In this section a loss distribution analysis of the main components—coupled inductors, MOSFETs and capacitors—of the LtL power stage is discussed. Further details are presented in Appendix J. The main components of the LtL system are specified in Table 3.4.

3.5.1 Battery to LED Power Flow

The power flow from the battery to the LED lamp in tapped boost operation mode is investigated. As discussed in Section 3.1, the magnetic component is determined by the specifications of the LED driver. The power stage is designed to drive the LEDs at the maximum current, however, the LED lamp will be mostly driven at low power levels, which achieves higher luminous efficiency. Therefore, the coupled inductors structure is optimized for operation at low power range. As discussed in Section 3.2, the wire-wound coupled inductors with partial interleaving winding arrangement is the selected magnetic structure, since it gives the best performance at low power levels. The inductor winding losses consist of dc and ac resistive losses. The dc conduction losses are calculated with the dc current and the dc resistance (3.4). The value of the coupled inductors dc resistance is measured with an impedance analyzer as 3.5 mΩ and 81.2 mΩ for the charge and discharge subintervals, respectively. The ac conduction

losses are calculated with the rms value of the inductor current ac component and the ac resistance (3.5). The ac resistance is measured as proposed in [156], where the core loss is measured using the resonant method in [157] and separated from the winding loss measurement value. The ac resistance, measured at the converter switching frequency (f_{sw} = 100 kHz), is 47.6 mΩ for the charge and 1.27 Ω for discharge subinterval. The core losses are calculated using Modified Steinmetz Equation [158], as shown in (3.6).

$$P_{dc_{cond}} = {I_{dc}}^2 \cdot R_{dc} \tag{3.4}$$

$$P_{ac_{cond}} = {I_{rms}}^2 \cdot R_{ac} \tag{3.5}$$

$$P_{MSE} = K \cdot {f_{eq}}^{(\alpha-1)} \cdot {B_{pk}}^{\beta} \cdot f_{sw} \quad [\mathrm{kW/m^3}]$$

$$f_{eq} = \frac{2}{\Delta B^2 \cdot \pi^2} \cdot \int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{3.6}$$

$$\Delta B = \frac{V_{bat}}{N \cdot A_e} DT$$

where K, α and β are the Steinmetz coefficients, f_{sw} is the switching frequency, B_{pk} is the peak ac flux density, ΔB is the peak to peak ac flux density, N is the number of turns and A_e is the effective area of the magnetic core.

The semiconductor losses are calculated as switching (3.1) and conduction losses (3.2), as discussed in Section 3.3. The selected tapped boost stage synchronous rectifier (M_3) presents better Q_G and R_{DS} than the DUT evaluated in Section 3.3 (V_{DS} = 55 V, R_{DS} = 16 mΩ @ V_{GS} = 5 V, Q_G = 7 nC @ V_{GS} = 5 V and C_{oss} = 50 pF @ V_{DS} = 45 V). A measurement of the switching energy loss with the wire-wound partial interleaving structure is performed. As discussed in Section 3.3, due to the ZCS conditions at the turn-on event, the energy losses due to the magnetic component parasitic capacitances are not visible in the semiconductor switching loss measurement. The capacitive loss can be calculated with (3.7) and (3.8), using the measured values of the stray capacitances shown in Table 3.2, Section 3.2.

$$E_{C_p} = \frac{1}{2} \cdot C_p \cdot \left({V_{bat}}^2 + \left(\frac{V_{bat} - V_{LED}}{n+1}\right)^2\right) \tag{3.7}$$

$$E_{C_{pri-sec}} = \frac{1}{2} \cdot C_{pri-sec} \cdot (nV_{bat} + V_{LED})^2 \tag{3.8}$$

Figure 3.15a and Figure 3.15b show the calculated efficiency loss of the magnetic component and the semiconductors in the tapped boost stage, respectively. The inductor losses are divided into winding ac and dc conduction losses, core and capacitive loss. The semiconductor losses consist of gate, switching and conduction losses. At low power levels, the capacitive loss, both on the inductor and in the semiconductors, and the magnetic component core loss are predominant. However, at higher power levels the windings ac conduction loss becomes predominant. This figure can be improved using litz wire to reduce proximity effect if high efficiency at high power levels is required.

The mathematical loss distribution analysis is verified by experimental efficiency measurements. Figure 3.16 shows the calculated and measured efficiency of the tapped-boost operation mode. The measurements are performed only on the power stage and

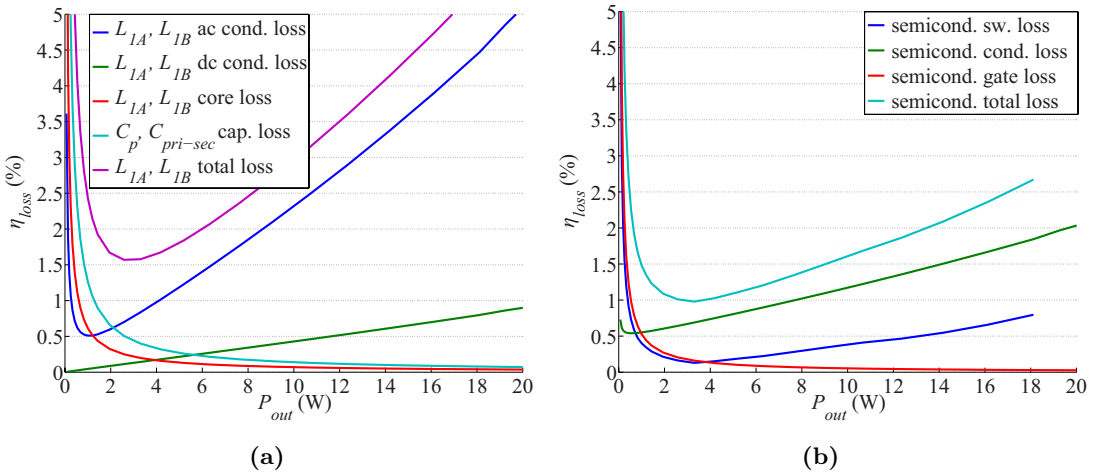


Figure 3.15: Tapped boost stage calculated efficiency loss (a) coupled inductors L_{1A}, L_{1B} (b) semiconductors M_2, M_3.

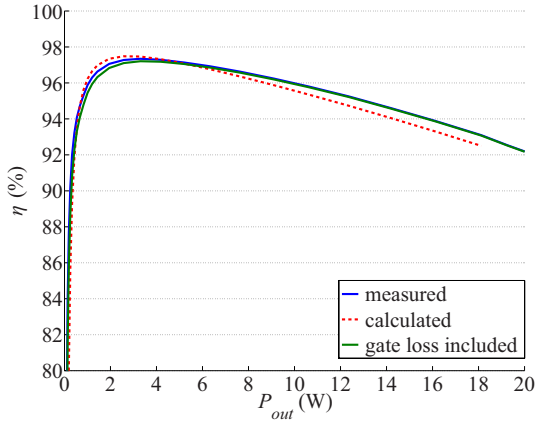


Figure 3.16: Measured and calculated efficiency curves of the tapped boost stage.

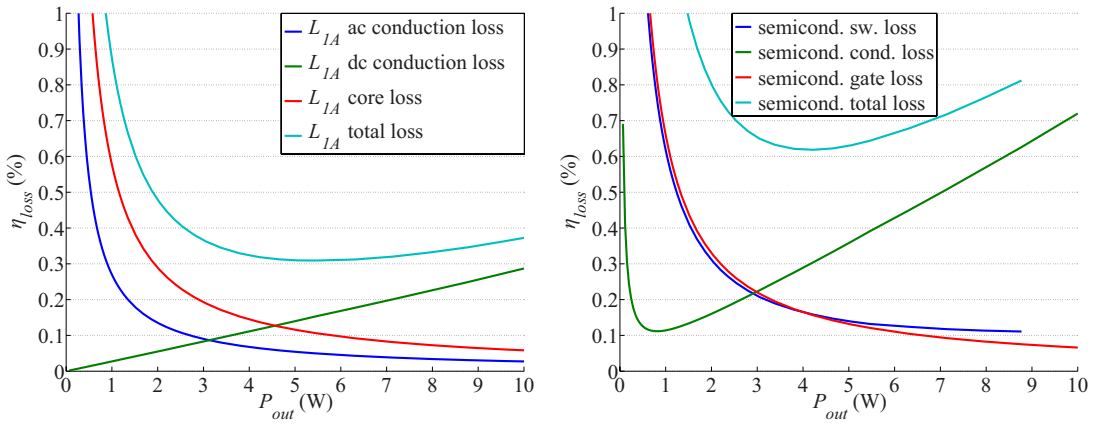
do not include the gate drive loss. The input and output ceramic capacitors are included in the calculation, although they have a low impact on the converter efficiency. As it can be observed the mathematical model presents very good match with the experimental measurements. The efficiency including the gate drive losses (P_{loss} = 4.7 mW) is presented as well in Figure 3.16. The high step-up tapped boost stage including the gate drive losses achieves a peak efficiency of 97.2% @ 3.2 W. The battery to LED power flow demonstrates an efficiency higher than 96% for an output power range from 1.2 W to 9.7 W.

3.5.2 PV to Battery Power Flow

The power flow from the PV panel to the battery in buck operation mode is investigated. The magnetic component reutilization is the key point of the proposed LtL structure. The parasitic capacitances of the coupled inductors structure are reflected and affect the switching loss in buck operation mode. The selected low parasitic capacitance coupled inductors implementation helps reducing the capacitive switching losses in the PV to battery power flow. The characterization of the semiconductors of the buck stage is

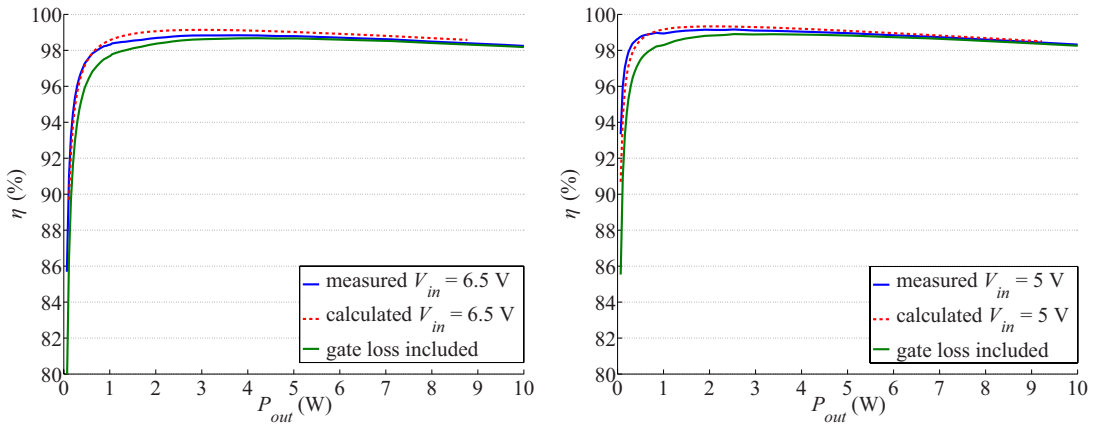
performed at two input voltages V_{in} = 6.5 V, V_{in} = 5 V, which corresponds to the output voltage of the PV panel at irradiance levels of 1000 W/m^2 and 100 W/m^2 @ T = 25°C, respectively. Figure 3.17a and Figure 3.17b presents the calculated efficiency loss of the inductor and semiconductors of the buck stage at V_{in} = 6.5 V. As it can be observed the inductor core loss and the semiconductor capacitive loss are predominant at low power level. The semiconductors gate and switching loss, and the magnetic component core loss, each contribute with 1% efficiency loss @ 1 W output power. At high power levels, the predominant contribution to the converter efficiency loss is caused by the semiconductor conduction loss. Further efficiency improvement at low power levels can be achieved by selecting devices with smaller die size, however, there is a limited selection of power devices for this voltage and power range.

The mathematical loss distribution analysis is compared to experimental measurements. Figure 3.18a and Figure 3.18b present the calculated and measured efficiency of the buck stage for V_{in} = 6.5 V and V_{in} = 5 V input voltages, respectively. The measurement



(a) **(b)**

Figure 3.17: Buck stage calculated efficiency loss @ V_{in} = 6.5 V(a) inductor L_{1A} (b) semiconductors M_1, M_2



(a) **(b)**

Figure 3.18: Measured and calculated efficiency curves of the buck stage. (a) V_{in} = 6.5 V (b) V_{in} = 5 V.

is performed on the power stage and do not include gate drive loss. As it can be observed, the mathematical loss distribution analysis shows very good match with the experimental efficiency measurements. The buck power stage efficiency including the measured gate drive loss (6.6 mW) is presented as well in Figure 3.18a and Figure 3.18b. As it can be observed, the gate drive loss presents a large contribution at low power levels. At V_{in} = 6.5 V, corresponding to the voltage of the PV panel at high irradiation level, higher than 98% efficiency is achieved for a power range from 1.3 W to full power. A peak efficiency of 98.7% @ 4 W output power is achieved. At low irradiation level, V_{in} = 5 V, the efficiency is higher than 98% in the range of 0.7 W to full output power. The peak efficiency of this power flow is 98.9% @ 3.4 W. The experimental results fulfill the target operation of maximizing the solar resource by achieving high energy efficiency conversion at low irradiation conditions.

The proposed LtL solution features low number of components and effective reutilization of the magnetic structure. The high efficiency conversion achieved in both power flow operation modes proves the reutilization of the primary winding of the coupled inductors LED driver, in a high efficient converter stage from the PV panel to the battery port.

3.6 Control Circuitry Loss Analysis

Power consumption of the control circuitry in low-power stand-alone systems have a big effect on the overall system efficiency and autonomy. The idle circuitry losses in this type of systems have to be minimized by careful selection of the components and by applying low-power modes depending on the operating conditions of the system. Although this project did not focus on optimizing the control circuitry idle losses, this section presents an overview of the implemented control circuitry loss and the effect on the overall system efficiency. Moreover, several ideas are proposed to minimize the main control circuitry losses.

The contribution from each component to the idle consumption losses is measured by isolating the different components in the control circuitry. These losses are divided as: step-down and step-up monolithic regulators (P_{loss} = 1 mW), MSP430 microcontroller (P_{loss} = 15 mW), gate drivers including the MOSFET gate loss (P_{loss} = 14 mW) and Hall effect current sensor (P_{loss} = 19 mW), which combined correspond to a total idle loss of P_{loss} = 49 mW. The contribution of the control circuitry losses to the overall system efficiency is presented in Figure 3.19a and Figure 3.19b for the battery to LED (tapped boost mode) and PV to battery (buck mode) power flows, respectively.

The current sensor introduces a large part of the idle losses, which can be minimized by using a resistive current shunt solution. This modification was considered during the prototype design stage. The implemented PCB can accommodate MAX9928 bidirectional current-sense amplifiers with low supply current (22 µA). This solution can reduce this idle loss with a small penalty for the converter efficiency at high power levels due to the inserted shunt resistor value ($R_{shunt} \simeq 10$ mΩ).

The implemented microcontroller claims a current consumption of 224 µA/MHz [159]. This measurement does not specify the voltage test conditions, however, it is reasonable to assume that this value corresponds to the minimum operating core voltage conditions (V_{cc} = 1.8 V). In this prototype, the microcontroller is configured with a clock

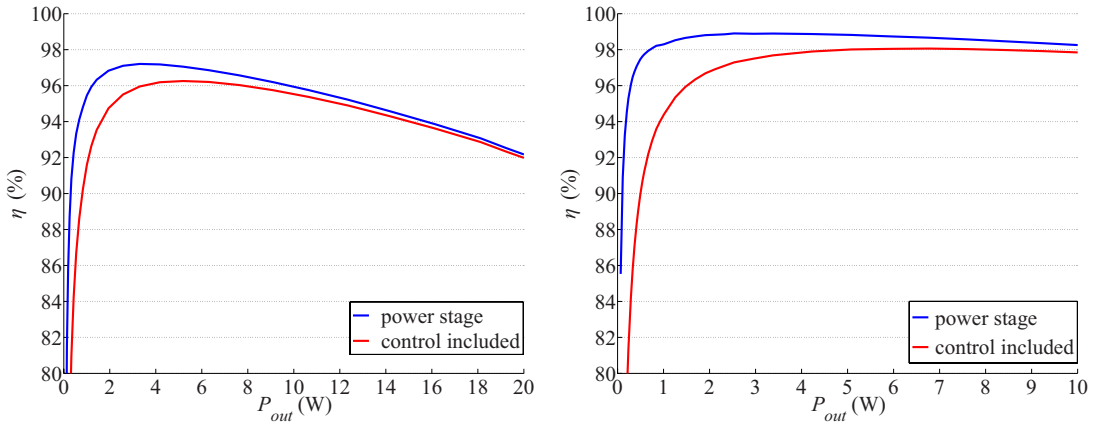


Figure 3.19: Measured efficiency curves with and without control circuitry losses. (a) tapped boost power stage (b) buck power stage @ $V_{in} = 5$ V.

frequency of $f_{core} = 10$ MHz @ $V_{cc} = 3.3$ V, which produces a power loss of $P_{loss} = 15$ mW. According to [160], the microcontroller can operate @ $f_{core} = 10$ MHz with the minimum core voltage ($V_{cc} = 1.8$ V) and 224 µA/MHz current consumption, resulting in $P_{loss} = 7.5$ mW. However, in the performed experiments a minimum $V_{cc} = 2.5$ V was required for stable operation at the selected frequency. During buck operation mode, the control loop regulates the PV voltage with the reference given by the MPPT algorithm. Increased core frequency operation, increases the number of instructions per second, which reduces propagation delay times and improves control loop transient response, improving the MPPT performance. As discussed in Section 2.1.1, at high irradiation level, a heuristic algorithm is preferred, however, at low irradiation conditions, constant voltage or constant current methods give better performance with lower computational requirement than hill-climbing methods. In these conditions, the microcontroller frequency operation can be reduced, which increases the overall system efficiency at low power levels. On the other hand, when the converter is configured as a tapped boost to regulate the battery to LED power flow in constant current (CI) dimming mode, the speed of the regulation loop is not a critical parameter, due to the battery and LED slow dynamics. Under these operating conditions it is also possible to reduce the microcontroller operating frequency, decreasing the power consumption.

3.7 Scalability

When scaling the system to a higher LED power level, some design consideration need to be addressed. As discussed in Section 2.2, series-connection of LEDs is preferred to avoid current mismatches of parallel connected strings. The required step-up conversion ratio of the SMPS is determined by the voltage of the battery ports and the number of LEDs connected in series. In order to increase the number of series-connected LEDs, a high transformation ratio of the tapped-inductor configuration will be necessary, which will increase the magnetic component and semiconductors current stress and affect the efficiency negatively. The series-connected LEDs can be divided into strings and connected in parallel, however, the current unbalance will reduce the luminous flux and,

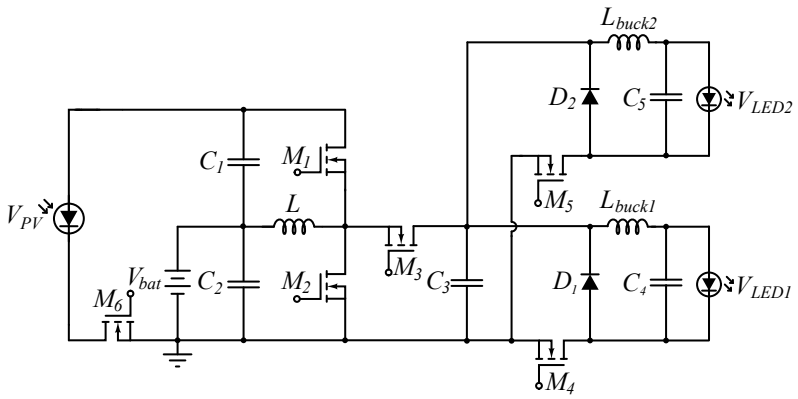


Figure 3.20: Schematic of scaled stand-alone LtL system with two LED outputs.

therefore, the system efficiency. The proposed solution to scale the LtL system provides two regulated LED strings, while achieving high reutilization of the power stage. Figure 3.20 shows the schematic of the LtL system. The structure is based on the same switching cell as the previous LtL system—M_1, M_2 and M_3—in boost configuration and two output LED strings. In order to achieve independent LED dimming regulation, while reutilizing the power stage, two small buck post-regulators are implemented at each of the LEDs output strings. If the buck cell switches, M_4 or M_5, are not regulating, i.e. only control the power flow path, the buck post-regulator acts just as an extra LC filter added to the LED output. In order to achieve high efficiency conversion, while providing independent dimming regulation, the key idea is to regulate one of the LED strings by controlling the boost stage duty cycle. In this way, the switch of one of the buck post-regulator stages is always on, while the other regulates the second string with a voltage slightly smaller than the other string. Due to the characteristic LED I–V curve, small voltage variations will result in large luminosity changes, therefore, the duty cycle of the regulating switch can be kept at high values. Hence, the small buck post-regulators can achieve very high efficiency, since the MOSFET is conducting most of the time, which minimizes the current stress, inductor ripple and core losses in this stage. In this way, independent string current regulation can be achieved with little effect on the LED driver efficiency, while reutilizing the main power stage switching cell.

A prototype with the specifications presented in Table 3.5 is designed and assembled. Figure 3.21 shows the top and bottom sides of PCB board implementation.

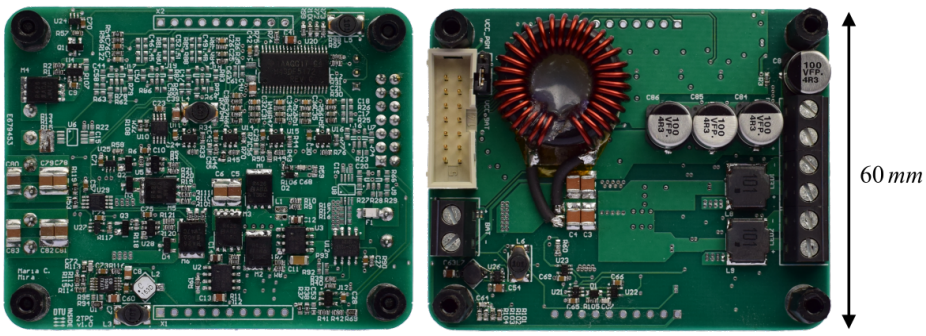
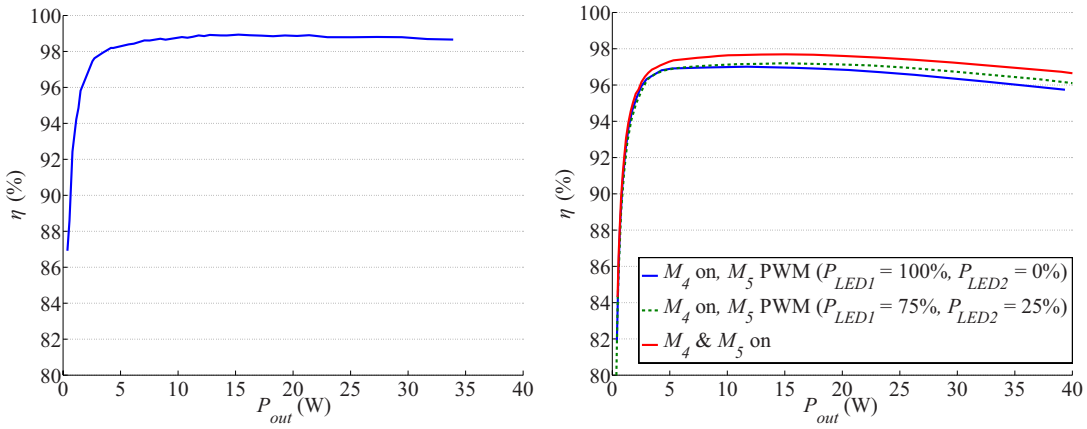


Figure 3.21: Prototype of the scaled stand-alone LtL system with two LED outputs.

Table 3.5: Specifications of the scaled stand-alone LtL system

P_{PV-max}	57.6 W
V_{mp}	19.4 V
I_{mp}	2.9 A
V_{oc}	23.94 V
I_{sc}	3.17 A
V_{bat}	11.1 V
Battery capacity	5.2 Ah
$P_{LED1,2-max}$	26.4 W
LED V_{fw}	9 x (2.6 to 3.3) V
LED $I_{fw_{max}}$	1000 mA

Figure 3.22a and 3.22b shows the measured efficiency curves from the PV panel to the battery and from the battery to the LED strings, respectively. The measurements are performed on the power stage and do not include gate drive and control circuitry losses. The buck operation mode achieves higher than 98% efficiency from $P_{out} = 3.5$ W with a peak efficiency 98.9% @ $P_{out} = 15$ W. The boost stage efficiency with two LED strings is measured in order to analyze the effects of the post-regulators on the system efficiency. The red trace shows the measured efficiency with both M_4 and M_5 switches fully on. The converter achieves an efficiency higher than 96% in the power range $P_{out} = 2.5$ to 40 W with a peak efficiency of 97.6% @ $P_{out} = 15$ W. Green and blue traces show the converter efficiency with M_4 fully on and M_5 performing PWM regulation on the second LED string, corresponding to 75/25% and 100/0% power distribution, respectively. As it can be observed, the extra switching and core losses from the post-regulation buck stage have a minimal effect on the overall system efficiency with only 0.5% loss @ $P_{out} = 1$ W. As the power level increases, the efficiency drops as the power distribution moves from the two LED outputs to a single one, due



(a) **(b)**

Figure 3.22: Efficiency of the scaled LtL system with two LED outputs (a) PV to battery power flow (b) LED driver power flow for different buck post-regulator configurations.

to the increased dc conduction loss on L_{buck1} and M_4 components, which are part of the buck post-regulation stage that is fully on. The achieved system efficiency with only one of the LED strings operating is higher than 96% in the power range $P_{out} = 2.7$ to 35 W. The efficiency measurements shows that this configuration allow reutilizing the components of the power stage, while achieving independent regulation of the LED strings without having a big penalty in the converter efficiency. The large duty cycle operation of the buck post-regulating stages reduces the current stress and makes it possible to select small semiconductor devices, which do not have a big impact on the overall system switching losses, without drastically increasing the conduction loss at high power levels. It is important to observe, that the implemented prototype uses a powder core as the main shared inductor between the buck and boost stages. A ferrite core implementation would further increase the system efficiency at low power levels [161], however the powder core implementation was preferred due to the soft saturation properties during the circuit debugging stage.

4

Three-Port Converter for Grid-Tied Light-to-Light System

4.1 System analysis

In large solar powered LtL applications ($100-1000$ W), it might be necessary to supply the system with a grid connection in order to provide the structure with an active and a safe mode. This is especially interesting in locations far from the equator, where the length of the day between summer and winter present large variations and might need over-dimensioning of the energy storage element and the PV panel. During summer time, the length of the day is large, with only a few hours or dark. In this case, the structure can work in active mode and the extra energy can be sent to the utility grid. During winter time, the length of the night considerably increases, worsened by the low sun irradiation levels during daytime. In this case, a grid connection can provide the system with a safe mode, which ensures LED lighting in extreme conditions.

Figure 4.1a presents a block diagram of the analyzed grid-tied LtL system. A TPC interconnects the renewable source and the energy storage element with a grid-tied

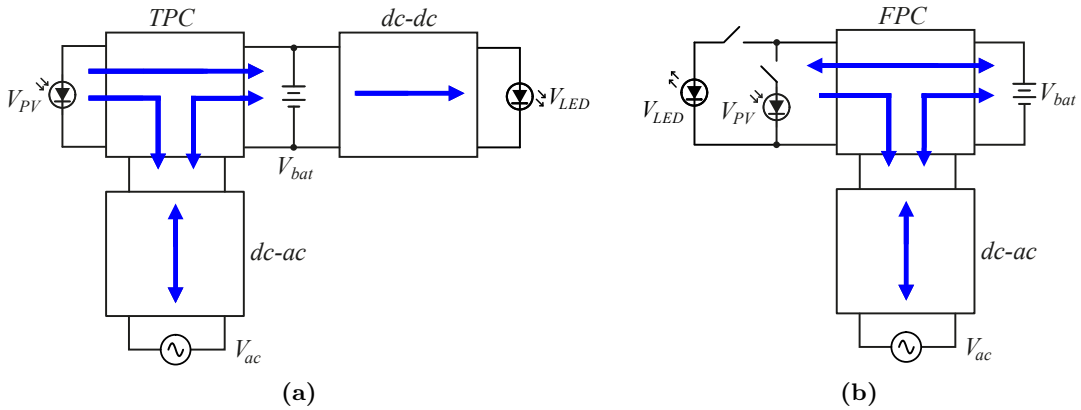


Figure 4.1: (a) Grid-tied TPC LtL system block diagram. (b) Grid-tied FPC LtL system block diagram.

dc-ac inverter. The LED lighting fixture is connected to the battery port through a separate dc-dc converter. However, as discussed in Section 3.1, in street lighting applications, since no overlap between the LED and PV power flows exist, it is possible to reconfigure the PV port and reutilize one of the power flows of the TPC topology creating a four-port converter (FPC) system, as shown in Figure 4.1b. This chapter discusses the analysis, modeling and control of the TPC structure in Figure 4.1a. Details of the operation and mathematical models are presented in Appendices K [107] and L. Unidirectional power flow from the battery to the dc-ac converter is analyzed. Further research for bidirectional operation of the proposed TPC topology needs to be carried out.

4.2 Circuit Description and Operation Principles

The studied TPC topology is based on the integration of a FB switching cell and a bidirectional converter [97, 104], combined with a high frequency transformer, an ac inductor as the power interface between the primary and the secondary ports, and a bridge rectifier. Figure 4.2 shows the schematic of the proposed TPC topology, where the renewable energy source is connected to the input port V_1, the energy storage element to the bidirectional port V_2, and the output port interfaces with a dc-ac inverter connected to the grid. The power flow between the two independent inputs (V_1 and V_2) is controlled by the switches' duty cycle (D), and the power transferred to the output port is regulated by the phase-shift angle(Φ) between the two interleaved switching cells. Figure 4.3a and Figure 4.3b show the equivalent circuits during the six time intervals and the converter operating waveforms, respectively. Depending on the duty cycle and its relationship with the phase-shift angle, three different operation modes can exist, based on the shape of the ac inductor current, which can be classified as completely demagnetized, partial demagnetized and fully magnetized. Completely demagnetized operation is the preferred mode since the output port voltage only depends on the phase-shift value, as shown in (4.1), for $\Phi < \min[D,\ (1-D)]$. Therefore, in completely demagnetized operation mode, the energy transferred to the output does not depend on the converter duty cycle.

$$V_o = \frac{n \cdot V_2}{k} \cdot \Phi(-\Phi + \sqrt{\Phi^2 + 2k}) \qquad k = \frac{2L_{ac}}{R_L T} \tag{4.1}$$

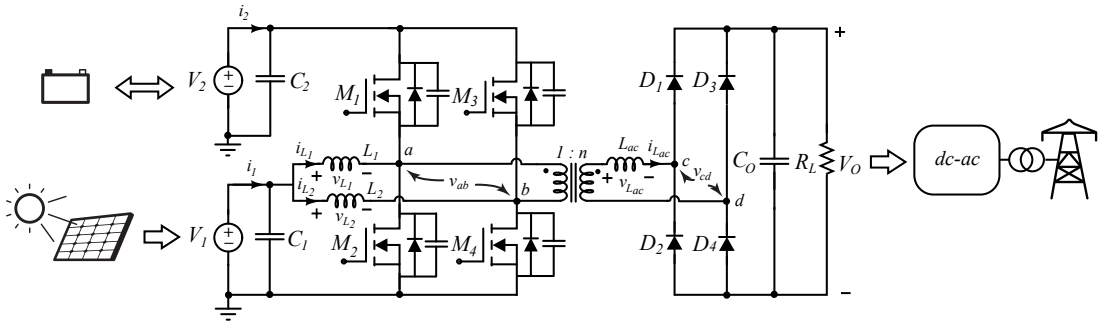


Figure 4.2: Schematic of the proposed TPC topology.

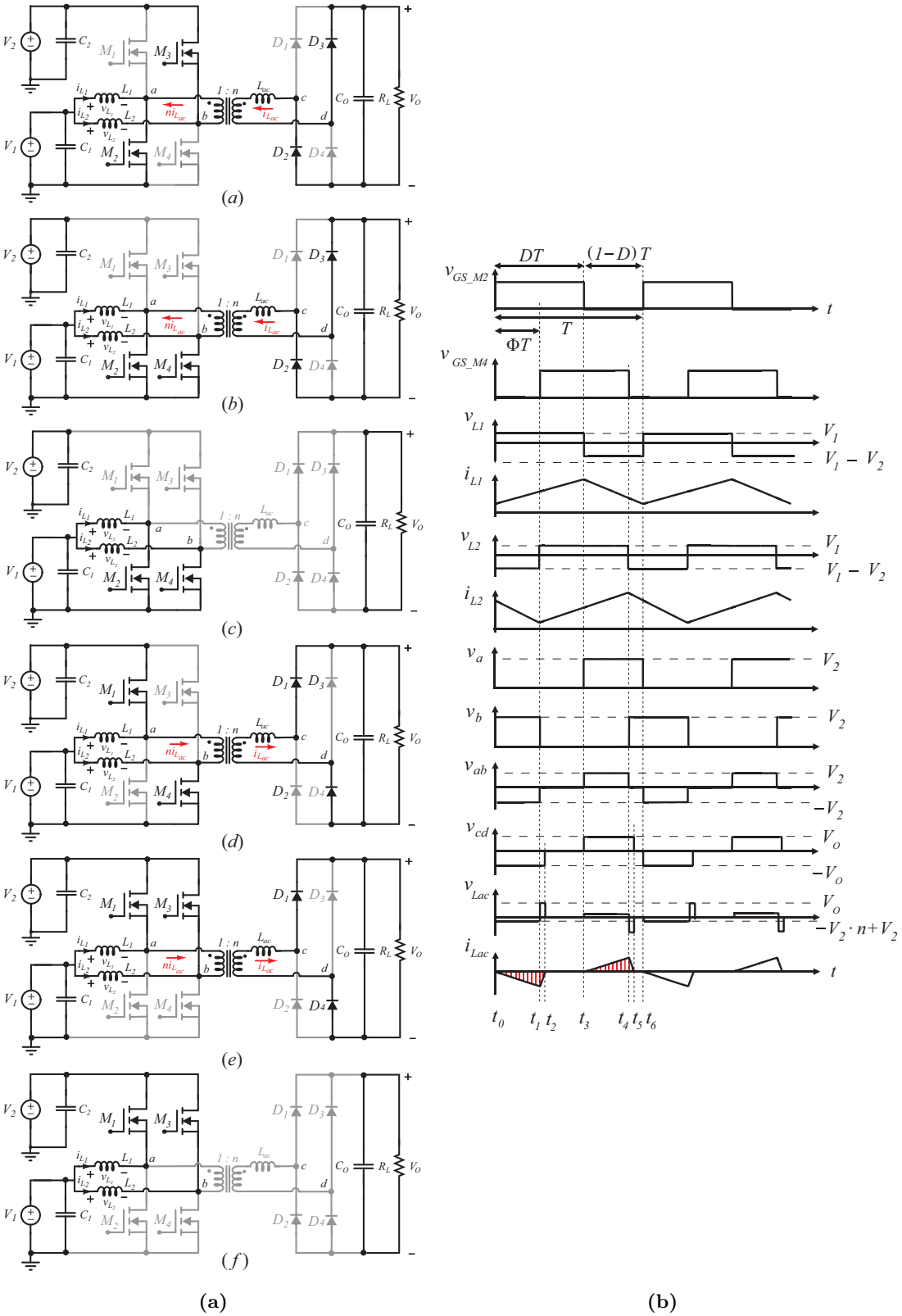


Figure 4.3: (a) Equivalent circuits for completely demagnetized ac inductor current (b) Key operating waveforms.

When the converter enters any of the other operation modes—partial demagnetized and fully magnetized—the converter output voltage is no longer solely controlled by the phase-shift angle, and becomes dependent on the duty cycle variable, as shown in (4.2) for the fully magnetized operation mode.

$$V_o = nV_2 \cdot (-2k + \sqrt{4D(1-D) - 4\Phi(1-\Phi) + 4k^2 - 1}) \tag{4.2}$$

Completely demagnetized operation mode makes it possible to design a control strategy with totally uncoupled control variables. Therefore, the proposed TPC offers independent controllability by using duty cycle and phase-shift as control variables, and reutilizes the primary switches to regulate the two power flows. This fact makes this TPC topology a very interesting solution for renewable energy applications, where an energy storage element is required, since full reutilization of the primary switches is achieved without having a negative impact on the controllability of the converter.

The TPC topology can achieve soft-switching operation of the MOSFETs and the output rectifier. On the one hand, the primary side switches M_1 and M_3 can inherently achieve ZVS conditions, as they operate as synchronous rectifier switches of the interleaved boost stage. Moreover, switch M_4 on the lagging interleaved stage, can achieve ZVS depending on the instantaneous current values i_{L_2} and $i_{L_{ac}}$ at t_1. On the other hand, as it can be observed in the key operating waveforms, the output bridge rectifier always changes its conduction stage when the ac inductor current reaches zero. Therefore, due to the use of an ac inductor, the secondary side diodes always turn-off under ZCS conditions, avoiding reverse recovery losses.

4.3 Modeling and Power Flow Control

An experimental prototype of the proposed TPC is designed and assembled, as shown in Figure 4.4, which is constructed with a fast prototyping technique. The specifications and the main components of the prototype implementation are presented in Table 4.1.

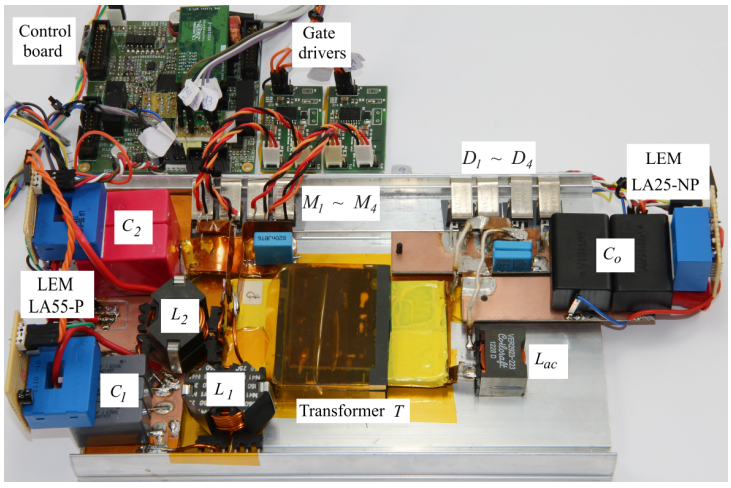


Figure 4.4: Experimental prototype of the grid-tied TPC LtL system.

Table 4.1: Grid-tied TPC Specifications and Components

Input Voltages	$V_1 = 25 - 60$ V , $V_{2_{max}} = 120$ V
Output Voltage	$V_o = 300 - 380$ V
Maximum output power	$P_{o_{max}} = 1000$ W
$M_1 \sim M_4$	IRFB4115 (150 V/104 A)
$D_1 \sim D_4$	HFA08TB60 (600 V/8 A)
Transformer T	4:16, ELP64/10/50 Ferrite N87
Inductors L_1 and L_2	155 µH N41 gapped core RM12
Inductors L_{ac}	28 µH Coilcraft VER2923-223
Capacitor C_1	2 x 10 µH 160 V WIMA MKP4
Capacitor C_2	3 x 22 µH 63 V AV MKT
Capacitor C_o	2 x 10 µH 700 V VISHAY MKP
Switching frequency	$f_{sw} = 60$ kHz
Digital controller	TMS320F28035 DSP

The relation between the system dynamics and the two control variables is investigated by performing state-space modeling. As it can be observed from the key operating waveforms, the ac inductor charge and discharge depends on the converter input voltage V_2 and the converter output voltage V_o, which means that the power transferred to the output is performed from the converter input port V_2. Therefore, the proposed TPC topology can be dynamically modelled as two individual converters: a bidirectional interleaved boost converter (BIBC), which balances the power flow withing the two input sources, and a phase-shift full bridge converter (PSFB), which delivers power to the load through the ac inductor. The high integration of the two structures in a TPC results in a topology with lower number of components and higher power density than multiple converter systems.

The PSFB and the BIBC control and line-to-output transfer functions are derived. The audio susceptibility, or line-to-output transfer function, relates how variations at the input port will affect the output as a function of the frequency. In the PSFB converter, the phase-shift-to-output voltage ($G_{v_o\Phi}$) and the audio susceptibility from V_2 to V_o ($G_{v_o v_2}$) transfer functions are obtained. In the BIBC, the duty cycle-to-inductor current ($G_{i_L d}$) and the audio susceptibility from V_1 to V_2 ($G_{v_2 v_1}$) transfer functions are derived. Last, in order to examine the interaction between the two power flows within the proposed TPC topology, the audio susceptibility from V_1 to V_o ($G_{v_o v_1}$) is analyzed.

The PSFB converter operating in completely demagnetized operation mode can be modelled using the traditional approach to analyze discontinuous conduction mode (DCM) operation [162], since the inductor current becomes zero for a portion of the switching period. When the PSFB converter enters in fully magnetized operation mode, the dynamic equation of the output capacitor needs to be expressed in terms of conservation of charge [163, 164] in order to take into account the correct charge applied to the output capacitor and accurately describe the dynamics involved in the rectified inductor current. State-space modeling of the BIBC operating in continuous conduction mode (CCM) is also carried out. The ports of the BIBC are modelled as an ideal voltage source with a series resistance, in order to account for the dynamic resistance of the renewable energy source and the energy storage element.

The small-signal mathematical models are verified by simulations and experimental measurements [165] performed with a vector network analyzer (VNA) Omicron Lab Bode100. Figure 4.5a and 4.5b shows the calculated and measured transfer functions of the PSFB and BIBC, phase-shift-to-output voltage ($G_{v_o\Phi}$) and duty cycle-to-inductor current (G_{i_Ld}), respectively. The calculation and measurements of the BIBC are perfomed with a resistive load instead of with an electronic load configured in CV mode. Measuring any transfer function with an electronic load is not recommended since the control circuit of the electronic load can interfere with the converter under test. As it can be observed, the mathematical model shows good match with the experimental measurements.

Figure 4.6 presents the calculated and measured audio susceptibility transfer function of the PSFB ($G_{v_ov_2}$) and the BIBC ($G_{v_2v_1}$), as well as the integration of the two converters as a TPC topology ($G_{v_ov_1}$). The line-to-output transfer function demonstrates that the converter output regulation is not directly affected by the perturbations on the converter input port V_1 or the converter duty cycle. Therefore, from a control point of view, the proposed TPC effectively behaves as two separate converters to regulate the two power

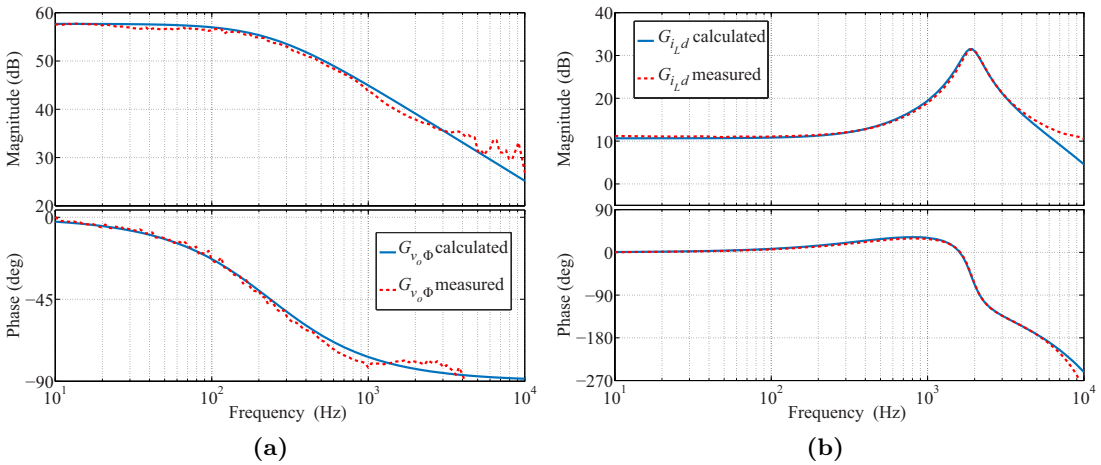


Figure 4.5: Calculated and measured transfer functions (a) PSFB phase-shift-to-output voltage ($G_{v_o\Phi}$) (b) BIBC duty cycle-to-inductor current (G_{i_Ld}).

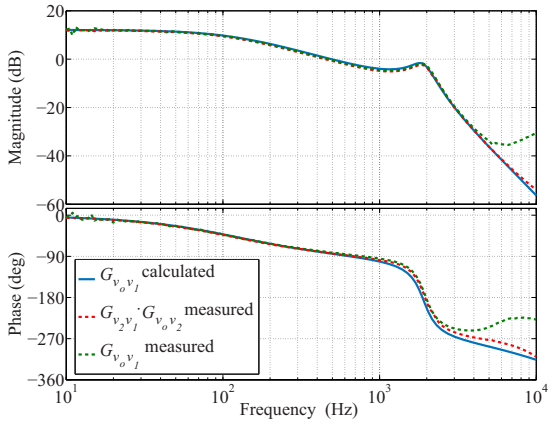


Figure 4.6: Calculated and measured TPC audio susceptibility transfer function ($G_{v_ov_1}$).

flows.

Based on the converter dynamic modeling, the power flow control is designed and the converter is tested under various operation modes, i.e. DI, DO and SISO. The performance of the energy management system and the control loops is verified by different experimental measurements. The measurement is performed with a dc power supply connected in parallel to an electronic load at the bidirectional port. The electronic load is configured in CV mode in order to simulate the behaviour of a battery.

The converter operating conditions are $V_1 = 50$ V, $V_2 = 100$ V and $V_o = 370$ V. Figure 4.7 (a) to (e) shows the transitions between different operating modes due to variations on the available power at the renewable energy port, while the load demand remains constant ($P_o = 250$ W). The input currents of both of the converter input ports, I_1 and I_2, as well as the load current, I_o, and the output voltage, V_o, waveforms are presented. Depending on the available power at the renewable energy port, the converter operating mode changes between DI, DO, SISO V_1 and SISO V_2 modes, as illustrated in Table 4.2. As it can be observed from the different transitions in Figure 4.7, variations of the power at the renewable energy port does not affect the voltage regulation at the output port, since the duty cycle control variable does not have an effect on the output voltage regulation when the converter operates in completely demagnetized mode.

In the same way, the transitions between different operating modes due to variations of the output port load demand are tested. Figure 4.8 (a) to (f) shows the transitions between different operating modes due to variations on the output power, while the power at the renewable energy port remains constant ($P_1 = 250$ W). Depending on the load demand, the converter operating mode changes between SISO, DI and DO modes, as presented in Table 4.3. As it can be observed from the different load steps in Figure

Table 4.2: Power at the ports for transitions between operating modes under constant output load

	SISO V_1	SISO V_2	DI	DO
P_1 [W]	250	0	125	375
P_2 [W]	0	250	125	−125
P_o [W]	250	250	250	250

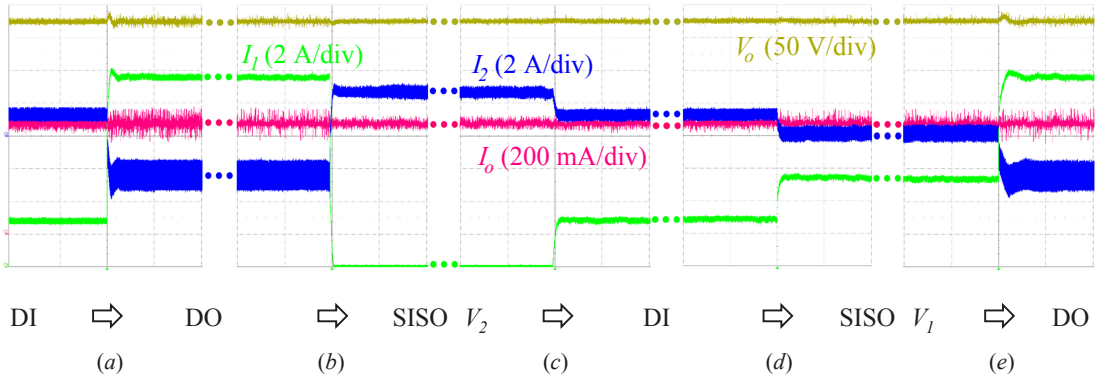


Figure 4.7: Transition between different operating modes due to variations of the available power at the renewable energy port. Time scale: 20 ms/div.

Table 4.3: Power at the ports for transitions between operating modes under constant power at the renewable energy source

	SISO V_1	DI	DO
P_1 [W]	250	250	250
P_2 [W]	0	125	−125
P_o [W]	250	375	125

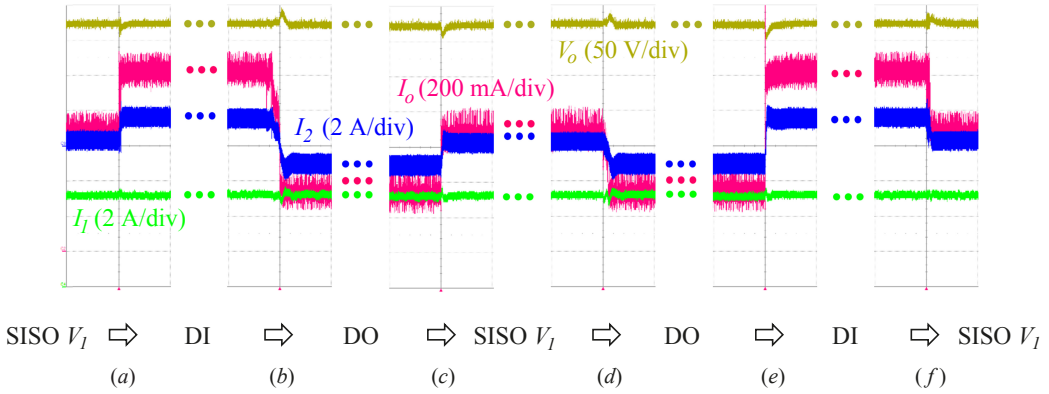


Figure 4.8: Transition between different operating modes due to variations of the output port load demand. Time scale: 20 ms/div.

4.8, variations of the output power does not affect the current at the renewable energy port (I_1), since the phase-shift control loop is decoupled from the duty cycle regulation that controls the power flow from the renewable energy source. Therefore, the power at the renewable energy port can be fully controlled, while the voltage at the output port is regulated, and the energy storage will compensate for the load dynamics.

Last, the efficiency of the TPC topology operating in different modes is investigated. Figure 4.9a and Figure 4.9b show the measured efficiency curves of the proposed TPC

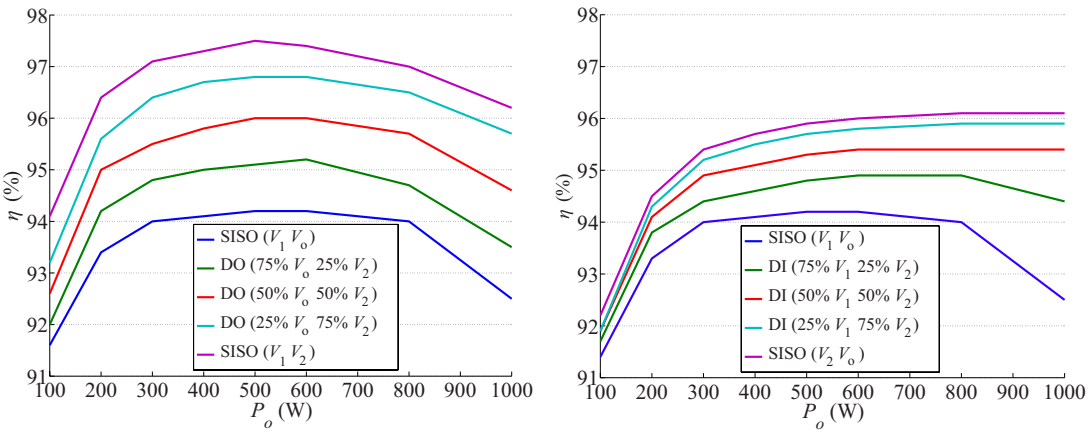


Figure 4.9: Measured TPC efficiency curves @ $V_1 = 50$ V, $V_2 = 100$ V $V_o = 370$ V (a) DO and SISO operation (b) DI and SISO operation.

topology operating in DI, DO and SISO modes. As it can be observed, when the converter operates in DO mode, the efficiency increases as the power flow moves from the output port (SISO V_1V_o) towards the bidirectional port (SISO V_1V_2). This is due to the fact that the energy is processed only by the non-isolated interleaved boost converter, instead of being boosted to V_2 and transferred through the transformer to the output port V_o. A peak efficiency of 97.5% is achieved in SISO V_1V_2, whereas the maximum efficiency achieved in SISO V_1V_o is 94.2%. The same behaviour is observed when the converter operates in DI mode and the operation changes from SISO V_1V_o to SISO V_2V_o. In this case, SISO V_2V_o shows higher efficiency than SISO V_1V_o due to the energy being processed once through the phase-shift isolated stage, instead of being boosted from V_1 to V_2 and then transferred to the output through the isolated stage. The maximum efficiency in SISO V_2V_o is 96.1%.

5

Conclusion and Future Work

Solar powered systems —combining a PV panel, an energy storage and an LED lamp— in locations far from the equator are challenging due to the intrinsic limitations of the geographic location, especially in low-power systems. In order to maximize the solar resource, the main goal is to achieve high energy efficiency conversion at low sun irradiation levels.

This work is based on the study of dc-dc conversion and multiport topologies in light-to-light LtL applications. The feasibility of the integration of TPC topologies in LtL systems is analyzed. Selecting the most suitable topology for an specific application is the key of achieving high efficiency energy conversion.

TPC topologies claim high efficiency and power density due to reduced conversion stages. Reutilization of components is the key in TPC structures. In order to achieve high efficiency, low number of components and low current stress on the components is desired. Non isolated TPC topologies require extra switches and diodes to provide controllability and to configure the power flow path. In some TPC topologies the charge and discharge subintervals of the magnetic component are shared between the input sources or the output loads, which increases current stress in the components. In other TPC topologies, the power is processed through an intermediate stage before is sent to the output port, which traduces in multiple conversion stages within the TPC.

Depending on the application DI and DO modes might not be necessary, requiring only single conversion between two of the stages. This is the case of street lighting systems, since no direct sunlight to LED energy conversion is required. The sequential separation of the power flow paths allows the conventional solution of two cascaded converters to be combined in a single structure with shared components. Magnetic components play an important role on the converter size, price and weight. A LtL solution is proposed, which features low number of components and effective reutilization of the magnetic structure. The high efficiency conversion achieved in both power flow operating modes proves the reutilization of the primary winding of the coupled inductors LED driver, in a high efficient converter stage from the PV panel to the battery port.

The main research areas and conclusions from this work can be summarized as:

- A low-power (10 W) LtL system with high peak efficiency (98.9%) of the PV to battery power flow (buck mode) at low irradiation conditions is demonstrated.

The high step-up battery to LED lamp power flow (tapped boost mode) achieves a peak efficiency of 97.2%.

  - Capacitive losses are the predominant source of loss at low power levels. Low capacitive implementation of the magnetic component is the key of reutilizing the component in different power flow paths.
  - Careful selection of the semiconductor devices in terms of capacitive losses—low gate charge (Q_G) and output capacitance (C_{oss})—is required for high efficiency at low power levels.

- Scalability and multiple LED strings of the low-power LtL system is demonstrated in a second prototype (50 W). The proposed solution to scale the power of the LED stage provides independent regulation of the individual strings, while reutilizing the main switching cell of the power stage. The power stage achieves a peak efficiency of 98.9% in the PV panel to the battery power flow (buck mode) and 97.6% in the battery to LED power flow (boost mode).

- A high power TPC (1000 W) for a grid-tied LtL system based on the integration of a FB switching cell and a bidirectional converter is investigated. Analysis and dynamic modeling of the TPC demonstrates decoupled control variables of the two power flows, while working in completely demagnetized operation mode. Experimental results demonstrate effective control of the power flow among the three ports.

5.1 Future Work

Further research needs to be carried out in different areas:

- Control circuitry losses. The Hall effect current sensor introduces a large part of the idle losses. A current measurement solution based on resistive current shunt can help to reduce the system idle losses improving the efficiency at low power levels. This solution and the effect on the converter efficiency due to increased conduction loss needs to be further investigated.

- The microcontroller unit and its operating conditions need to be fine tuned to further reduce the control circuitry idle losses depending on the system operating mode.

- A Coulomb counter combined with V_{oc} battery measurements needs to be implemented to obtain accurate estimations of the battery SOC, helping increase the element lifetime. A combined constant method/hill-climbing MPPT algorithm has to be implemented to increase the MPPT accuracy at low irradiation conditions, while decreasing the system idle losses at low power levels.

- Implementation of a mixed analog-digital control of the system needs to be considered as a way of improving the control loops regulation speed, while removing power processing requirements from the microcontroller unit.

- Study of the feasibility of using wide bandgap semiconductors in the power stage of the LtL system.

- To bring the design of the demonstrator to a commercial product, several aspects in different areas should be investigated:
  - Operation under different environmental conditions (temperature, humidity, etc).
  - Electromagnetic compatibility (EMC) compliance.
  - Different design considerations need to be re-evatluated taking production cost into account.
- Bidirectional operation of the analyzed TPC topology for grid-tied applications has to be investigated by including synchronous rectification on the converter secondary side.

6

Other Research Topics

This chapter presents the work carried out during the Ph.D. project that is not related to the project objectives.

6.1 Isolated Boost Converter with Bidirectional Operation for Supercapacitor Applications

An isolated bidirectional boost converter for regenerative braking applications is presented in Appendix M [166]. State-space modeling and control are analyzed, and a safe start-up converter strategy is investigated. The results show the bidirectional operation of the converter with batteries at both of the ports. A supercapacitor charge event under constant power operation is achieved with a second prototype.

6.2 Wide Operating Voltage Range Fuel Cell Battery Charger

A fuel cell battery charger based on primary parallel isolated boost converter (PPIBC) topology is presented in Appendix N [167]. An extended operation mode is analyzed, which is intended for applications with wide variations in the converter output voltage due to large current load demands.

6.3 Component Stress Factor: Analysis of Dual Active Bridge and Isolated Full Bridge Boost Converter for Bidirectional Fuel Cells Systems

An analysis, based on component stress factor (CSF) of dual active bridge and isolated full bridge boost converter is presented in Appendix O [168]. A comparison of the application of the two topologies in a grid-tied bidirectional fuel system is carried out. The performed CSF analysis compares the two solutions in a wide operating range determined by the fuel cell operating conditions.

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List of Publications

Appendix A

- **"Boost Converter with Combined Control Loop for a Stand-Alone Photovoltaic Battery Charge System"**

  2013 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2013).

Appendix B

- **"Simulation Tool for Designing off-Grid PV Applications for the Urban Environments"**

  28^{th} *European Photovoltaic Energy Conference and Exhibition (EUPVSEC 2013).*

Appendix C

- **"PV LED Engine Characterization Lab for Standalone Light to Light Systems"**

  29^{th} *European Photovoltaic Energy Conference and Exhibition (EUPVSEC 2014).*

Appendix D

- **"Design, Characterization and Modelling of High Efficient Solar Powered Lighting Systems"**

  32^{nd} *European Photovoltaic Energy Conference and Exhibition (EUPVSEC 2016).*

Appendix E

- **"Designing High Efficient Solar Powered Lighting Systems"**

  43^{rd} *IEEE Photovoltaic Specialist Conference (PVSC 2016).*

Appendix F

- **"A Three-Port Topology Comparison for a Low Power Stand-Alone Photovoltaic System"**

  2014 IEEE International Power Electronics Conference (IPEC 2014 ECCE–ASIA).

Appendix G

- **"A Three-Port Direct Current Converter"**

  Patent Application – DTU-95727/P3806EP00.

Appendix H

- **"Analysis and Comparison of Magnetic Structures in a Tapped Boost Converter for LED Applications"**

  2014 IEEE Power Electronics and Applications Conference (PEAC 2014).

Appendix I

- **"MOSFET Loss Evaluation for a Low-Power Stand-Alone Photovoltaic-LED System"**

  2015 IEEE Power Electronics and Drive Systems (PEDS 2015).

Appendix J

- **"Loss Distribution Analysis of a Three-Port Converter for Low-Power Stand-Alone Light-to-Light Systems"**

  2016 IEEE European Power Electronics and Drives (EPE 2016 ECCE–EUROPE).

Appendix K

- **"Power Flow Control of a Dual-Input Interleaved Buck/Boost Converter with Galvanic Isolation for Renewable Energy Systems"**

  2015 IEEE Applied Power Electronics Conference (APEC 2015).

Appendix L

- **"Analysis, Design, Modeling and Control of an Interleaved-Boost Full-Bridge Three-Port Converter for Hybrid Renewable Energy systems"**

  IEEE Transactions on Power Electronics (TPEL). ISSN: 0885-8993. DOI: 10.1109/TPEL.2016.2549015.

Appendix M

- **"Isolated Boost Converter with Bidirectional Operation for Supercapacitor Applications"**

  Journal of Power Electronics (JPE) Vol. 13, No. 4, 2013, pp. 507-505.

Appendix N

- **"Wide Operating Voltage Range Fuel Cell Battery Charger"**

  Elektronika IR Elektrotechnika, Vol. 20, No. 5, 2014, p. 97-103.

Appendix O

- **"Component Stress Factor: Analysis of Dual Active Bridge and Isolated Full Bridge Boost Converter for Bidirectional Fuel Cells Systems"**

  2014 IEEE Power Electronics and Applications Conference (PEAC 2014).

A

Boost Converter with Combined Control Loop for a Stand-Alone Photovoltaic Battery Charge System

2013 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL2013)

Boost Converter with Combined Control Loop for a Stand-Alone Photovoltaic Battery Charge System

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***Abstract*— The converter control scheme plays an important role in the performance of maximum power point tracking (MPPT) algorithms. In this paper, an input voltage control with double loop for a stand-alone photovoltaic system is designed and tested. The inner current control loop with high crossover frequency avoids perturbations in the load being propagated to the photovoltaic panel and thus deviating the operating point. Linearization of the photovoltaic panel and converter state-space modeling is performed. In order to achieve stable operation under all operating conditions, the photovoltaic panel is linearized at the maximum power point (MPP) and at the voltage and current source regions. A settling time under 1 ms is obtained which allows fast MPP tracking implementation.**

Index Terms: Photovoltaic, battery, MPPT, averaged small-signal modeling, linearized PV panel.

I. INTRODUCTION

Renewable energies have become more important in the last decades due to the fact that fossil fuel reserves are being depleted together with the awareness of global warming and climate change. In the last years, solar energy has become one of the fastest growing technologies mainly because the Sun is the most abundant source of energy currently available and is unlimited, clean and free.

Solar cells combined with a storage element in a stand-alone system can be used as a self-sustained power source for all kind of electrical powered applications. An off grid system eliminates the cost of cables, which is very interesting for powering up systems at remote locations, where cabling is challenging and expensive. Moreover, it is also relevant in urban areas where, digging, construction, reconstruction, etc. is extremely costly.

A photovoltaic cell is basically a p-n junction that generates current under the effect of solar irradiation [1]. Due to its non-linear behavior, a maximum power point tracking (MPPT) algorithm that continuously tracks the maximum instantaneous power is required. The importance of the maximum power point seeking relies on the low energy-conversion efficiency of photovoltaic panels. Many MPPT algorithms have been developed [2], [3] and several publications can be found in the literature presenting improvements on the classical algorithms [4], [5], [6]; however, less attention has been given to the converter control technique. Nevertheless, the performance of the MPPT will depend on the ability of the converter to regulate the operating point of the photovoltaic panel, which is determined by the control strategy [7]. Both voltage and current of the photovoltaic panel are usually taken as the control variable in order to regulate the converter operating point. Ideally, the control variable should be constant or present small variations over time. However, output current and voltage of the photovoltaic panel are time variant with changes of irradiation and temperature. The output current of a photovoltaic panel shows a linear dependence with the photogenerated current and, therefore, varies strongly with changes of irradiation. On the contrary, due to the logarithmic dependence of the voltage with the photogenerated current, the PV voltage does not present such a strong variation with irradiation changes. However, the output voltage varies with temperature changes, while the current is less affected. Regardless, temperature has slow dynamics compared to irradiation variations (e.g. due to cloudy atmospheric conditions). The aforementioned arguments make PV voltage regulation preferred over current regulation [8].

This paper presents a control scheme based in a double control loop, where the output voltage of the PV panel is controlled by the mean value of the inductor current. Fig. 1 shows the case study where a boost converter is connected to a photovoltaic panel at the input and a battery at the output.

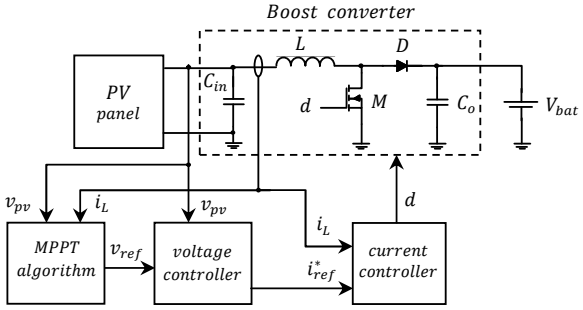

Figure 1. Block diagram of the system with the proposed control strategy

The inner current loop controls the inductor current and the outer voltage loop controls the converter input voltage by setting the mean value of the inductor current. This configuration allows decoupling the PV panel operating conditions from perturbations at the load. In this case, the converter is loaded with batteries and the output voltage can be considered constant. However, if a grid connected battery charger or inverter is inserted in the system, perturbations with the grid frequency can propagate to the PV panel side altering the operating point. The inner current loop with higher crossover frequency than the outer voltage loop will present a higher error reduction at this frequency, avoiding propagation of these perturbations to the PV panel side.

II. PV PANEL AND CONVERTER MODELING

A. Photovoltaic panel modeling

Photovoltaic devices present a non-linear I-V characteristic. Fig. 2 shows the single diode equivalent model of a solar cell neglecting the shunt resistance. Equation (1) describes the output current of a photovoltaic cell, where I_{ph} represents the photogenerated current (directly proportional to the Sun irradiation), I_o is the diode's dark saturation current, $V_t = AkT/q$ is the thermal voltage, A is the diode ideality factor, k is Boltzmann's constant ($1.380 \cdot 10^{-23} JK^{-1}$), $T\,[K]$ is the p-n junction temperature and q is the electron charge ($1.602 \cdot 10^{-19} C$). Fig. 3 shows the I-V curve of a PV panel where the maximum power point is located at the knee of the curve given by the points V_{mp} and I_{mp}. For $V_{pv} < V_{mp}$, the PV panel operates as a current source while for $V_{pv} > V_{mp}$ the panel acts as a voltage source [9]. In order to include the input source as a part of the converter, a linearized model of the photovoltaic panel is required.

$$I = I_{ph} - I_o\left(e^{\frac{V+I\cdot R_S}{V_t}} - 1\right) \tag{1}$$

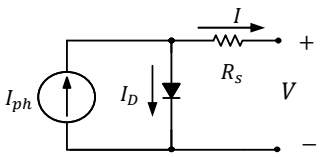

Figure 2. Single diode with series resistance equivalent model

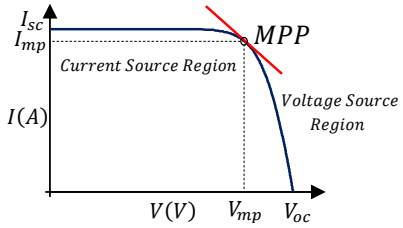

Figure 3. $I-$V characteristic of a PV panel

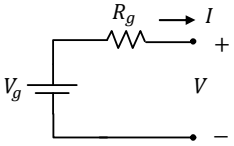

Figure 4. Equivalent linearized model of a PV panel

Based in [9] the PV panel can be linearized by using the derivative of the non-linear curve (1) at the linearization point, as shown in (2). The linear model is described by the tangent line to the I-V curve at this point (3).

$$g = \left.\frac{dI}{dV}\right|_{\substack{V=V_{mp}\\ I=I_{mp}}} = -\frac{I_O}{V_t}\cdot e^{\left(\frac{V_{mp}+I_{mp}\cdot R_S}{V_t}\right)} \tag{2}$$

$$I = \left(-g\cdot V_{mp} + I_{mp}\right) + g\cdot V \tag{3}$$

Fig. 4 shows the linear equivalent circuit of the photovoltaic panel. It is represented by an equivalent voltage source (4) and a series resistance (5), obtained by particularizing (3) at $I = 0$ and $V = 0$, respectively.

$$V_g = V_{mp} - \frac{I_{mp}}{g} \tag{4}$$

$$R_g = -\frac{1}{g} \tag{5}$$

The model is valid at the linearization point and it is a good aproximation for obtatining a small signal model of the photovoltaic panel. It is desired to always operate at the maximum point; however, it is possible that the PV panel changes its operation point to the current or voltage source region. The dynamic behavior of the overall system, photovoltaic panel and power stage, will strongly depend on the operating point of the panel. In order to design the control loop and ensure stability of the converter under all the operating conditions, the PV panel is also linearized at the current and voltage source regions by using (2) and (3).

B. Boost converter modeling

In this section state-space average modeling [10] of boost converter is performed. The model includes parasitic resistances of the reactive elements, the MOSFET's on resistance and the diode forward voltage drop. Since the converter acts as a battery charge system, the load is modeled as an ideal voltage source in series with the battery dynamic resistance. In order to obtain a linear model, the converter is taken as an equivalent circuit for the charging and discharging states. Each switching state is expressed in terms of state space equations, (6) and (7). Note that the output equation (7) is not used since the controlled variables, inductor current (inner control loop) and input voltage (outer control loop), are state variables.

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t) \tag{6}$$

$$y(t) = Cx(t) + Du(t) \tag{7}$$

Fig. 5 and Fig. 6 show the equivalent linear circuits during the charging and discharging states. The equivalent resistance, r_{eq}, is the series combination of the inductor parasitic resistance and the MOSFET's on resistance, $r_{eq} = r_L + r_M$.

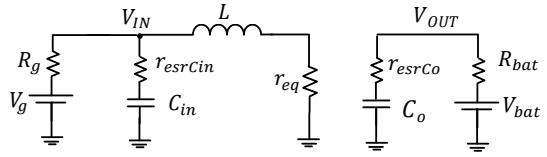

Figure 5. Equivalent boost converter during the charging state

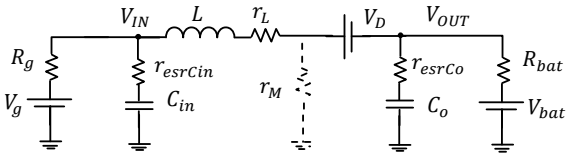

Figure 6. Equivalent linear circuit during the discharging state

The dynamic equations corresponding to the charging state are obtained by evaluating the derivatives of the inductor and the input and output capacitor of Fig. 5 as shown in (8), (9) and (10).

$$\frac{di_L(t)}{dt} = \frac{V_{IN}(t) - i_L(t) \cdot r_{eq}}{L} \tag{8}$$

$$\frac{dv_{C_{in}}(t)}{dt} = \frac{V_{IN}(t) - v_{C_{in}}(t)}{C_{in} \cdot r_{resrCin}} \tag{9}$$

$$\frac{dv_{C_O}(t)}{dt} = \frac{V_{OUT}(t) - v_{C_O}(t)}{C_O \cdot r_{esrCo}} \tag{10}$$

Rewriting the dynamic equations (8), (9) and (10) in state-space form as (11) results in (12), shown at the bottom of the page.

$$\frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \tag{11}$$

The dynamic equations during the discharging state are found by evaluating the derivatives of the state variables of Fig. 6 as given in (13), (14) and (15).

$$\frac{di_L(t)}{dt} = \frac{V_{IN}(t) - i_L(t) \cdot r_L - V_D - V_{OUT}(t)}{L} \tag{13}$$

$$\frac{dv_{C_{in}}(t)}{dt} = \frac{V_{IN}(t) - v_{C_{in}}(t)}{C_{in} \cdot r_{esrCin}} \tag{14}$$

$$\frac{dv_{C_O}(t)}{dt} = \frac{V_{OUT}(t) - v_{C_O}(t)}{C_O \cdot r_{esrCo}} \tag{15}$$

Expressions of V_{IN} and V_{OUT} for each subinterval can be found by applying Kirchhoff's laws on the corresponding equivalent linear circuit.

Expressing (13), (14) and (15) in the matrix form given in (16) results in (17), shown at the bottom of the page.

$$\frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) \tag{16}$$

The state and input matrixes are averaged over a period by multiplying the state and input matrixes by the two switched intervals' duty cycle.

$$A = A_1 \cdot d + A_2 \cdot (1 - d) \tag{18}$$

$$B = B_1 \cdot d + B_2 \cdot (1 - d) \tag{19}$$

After averaging, the system is perturbed around a quiescent operating point $(X + \hat{x},\ D + \hat{d},\ U + \hat{u})$ where $X \gg \hat{x}$, and linearized by neglecting the second order terms. Applying the Laplace transform and separating the dc and ac part of the linearized model, the steady-state operating point (20) and the dynamic or small-signal model (21) are obtained.

$$X = -A^{-1} \cdot B \cdot U \tag{20}$$

$$\dot{\hat{x}} = A \cdot \hat{x} + B \cdot \hat{u} + [(A_1 - A_2)X + (B_1 - B_2) \cdot U] \cdot \hat{d} \tag{21}$$

The control transfer functions are defined for small variations of the input matrix $(\hat{u})$ equal to zero. The solution of the state variable is given by (22).

$$\hat{x} = (sI - A)^{-1} \cdot [(A_1 - A_2)X + (B_1 - B_2)U] \cdot \hat{d} \tag{22}$$

The duty cycle-to-inductor current transfer function (23) is used in the inner control loop and relates the small variations of the inductor current and the control variable d.

$$G_{id}(s) = \left.\frac{\hat{\imath}_L(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0} \tag{23}$$

In the outer control loop the controlled variable is the input voltage while the control variable is the inductor current. The transfer function from inductor current to input voltage is given by (24).

$$G_{vi}(s) = \frac{G_{vd}(s)}{G_{id}(s)} = \frac{\left.\frac{\hat{v}_{Cin}(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0}}{\left.\frac{\hat{\imath}_L(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0}} = \frac{\hat{v}_{Cin}(s)}{\hat{\imath}_L(s)} \tag{24}$$

In order to validate the calculated transfer functions, the mathematical model obtained by state-space modeling is plotted using MATLAB and compared with LTspice simulations. The photovoltaic panel specifications are presented in Table I. Table II shows the equivalent voltage and resistance of the linearized panel for the three different areas of the I-V curve –MPP, voltage and current source regions.

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_{in}}(t) \\ v_{C_O}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\cdot\left(r_{eq} + \frac{R_g \cdot r_{esrCin}}{R_g + r_{esrCin}}\right) & \frac{R_g}{L\cdot(R_g + r_{esrCin})} & 0 \\ -\frac{R_g}{C_{in}\cdot(R_g + r_{esrCin})} & -\frac{1}{C_{in}\cdot(R_g + r_{esrCin})} & 0 \\ 0 & 0 & -\frac{1}{C_O\cdot(R_{bat} + r_{esrCo})} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_{in}}(t) \\ v_{C_O}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrCin}}{L\cdot(R_g + r_{esrCin})} & 0 & 0 \\ \frac{1}{C_{in}\cdot(R_g + r_{esrCin})} & 0 & 0 \\ 0 & \frac{1}{C_O\cdot(R_{bat} + r_{esrCo})} & 0 \end{bmatrix} \cdot \begin{bmatrix} V_g \\ V_{bat} \\ V_D \end{bmatrix} \tag{12}$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_{in}}(t) \\ v_{C_O}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\cdot\left(r_L + \frac{R_{bat} \cdot r_{esrCo}}{R_{bat} + r_{esrCo}} + \frac{R_g \cdot r_{esrCin}}{R_g + r_{esrCin}}\right) & \frac{R_g}{L\cdot(R_g + r_{esrCin})} & -\frac{R_{bat}}{L\cdot(R_{bat} + r_{esrCin})} \\ -\frac{R_g}{C_{in}\cdot(R_g + r_{esrCin})} & -\frac{1}{C_{in}\cdot(R_g + r_{esrCin})} & 0 \\ \frac{R_{bat}}{C_O\cdot(R_{bat} + r_{esrCo})} & 0 & -\frac{1}{C_O\cdot(R_{bat} + r_{esrCo})} \end{bmatrix} \cdot \begin{bmatrix} i_L(t) \\ v_{C_{in}}(t) \\ v_{C_O}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrCin}}{L\cdot(R_g + r_{esrCin})} & -\frac{r_{esrCo}}{L\cdot(R_{bat} + r_{esrCo})} & -\frac{1}{L} \\ \frac{1}{C_{in}\cdot(R_g + r_{esrCin})} & 0 & 0 \\ 0 & \frac{1}{C_O\cdot(R_{bat} + r_{esrCo})} & 0 \end{bmatrix} \cdot \begin{bmatrix} V_g \\ V_{bat} \\ V_D \end{bmatrix} \tag{17}$$

TABLE I
PV PANEL SPECIFICATIONS @ STC

P_{max}	104.4 W
V_{mp}	18 V
I_{mp}	5.8 A
V_{oc}	22.1 V
I_{sc}	6.3 A

TABLE II
LINEARIZED PV EQUIVALENT VOLTAGE AND RESISTANCE

	V_g	R_g
MPP	35.78 V	3.07 Ω
Voltage Source Region	22.1 V	0.306 Ω
Current Source Region	796.9 V	124.7 Ω

TABLE III
PARAMETERS OF THE CONVERTER

Battery Voltage V_{bat}	28 V
Inductor L	48.15 µH
Capacitor C_{in}	40 µH
Capacitor C_O	40 µH
MOSFET	IPP039N04L
Diode	DSB10I45PM
Switching frequency	100 kHz

TABLE IV
CONVERTER PARASITIC RESISTANCES

r_L	8.9 mΩ
r_M	3.9 mΩ
r_{esrCin}	3 mΩ
r_{esrCo}	3 mΩ
R_{bat}	10 mΩ

The simulations are performed using the parameters of the converter shown in Table III and the parasitic resistances of Table IV, for the PV panel linearized at the MPP. Fig. 7 and Fig. 8 show the gain and phase plots of the converter duty cycle-to-inductor current transfer function (G_{id}) and the inductor current-to-input voltage transfer function (G_{vi}). It can be observed that the calculated transfer functions obtained by state-space modeling show very good match with the simulations. The duty cycle-to-inductor current transfer function is a second order system formed by the inductor and the input capacitor. However, a zero formed by the equivalent input resistance R_g and the input capacitor makes the system to behave as a first order system. On the other hand, the inductor current-to-input voltage transfer function is a first order system with a pole formed by the input capacitor and the equivalent input resistance R_g. Note that this transfer function presents a $-180°$ phase shift.

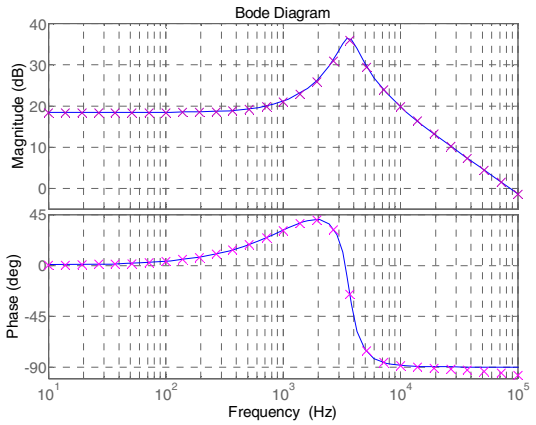

Figure 7. Duty cycle-to-inductor current (G_{id}) transfer function calculated (blue line) and simulated (crosses)

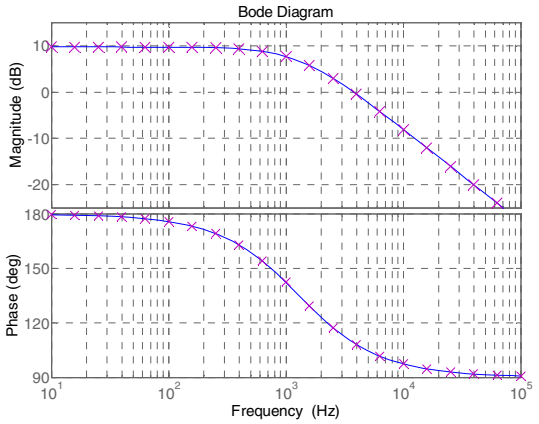

Figure 8. Inductor current-to-input voltage (G_{vi}) transfer function calculated (blue line) and simulated (crosses)

III. CONTROL LOOP DESIGN

The proposed control scheme is a double loop control [7] where the output voltage of the photovoltaic panel, v_{pv}, is controlled by the mean value of the inductor current, i_L. Fig. 9 shows the simplified block diagram of the control strategy where C_v represents the voltage compensation, G_{i_cl} the closed loop transfer function of the inner current control loop, G_{vi} the converter inductor current-to-input voltage transfer function and H_v the input voltage measurement gain. Fig. 10 shows the block diagram of the inner current control loop ($G_{i,cl}$) where C_i denotes the current compensation, PWM the pulse-width modulator, G_{id} the converter duty cycle-to-inductor current transfer function and $Diff.Amp.$ and $Current\ Sensor$ the current measurement gain.

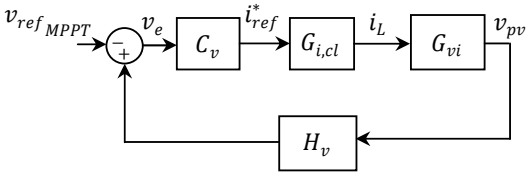

Figure 9. Simplified block diagram of the control scheme

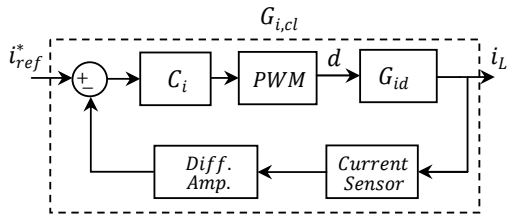

Figure 10. Inner current control loop block diagram

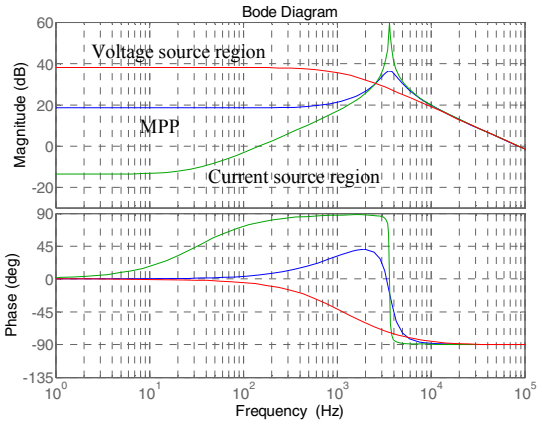

Figure 11. Duty cycle-to-inductor current transfer function (G_{id}) for different operating point of the PV panel

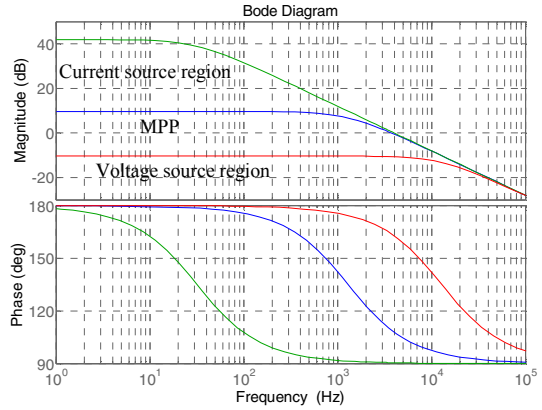

Figure 12. Inductor current-to-input voltage transfer function (G_{vi}) for different operating point of the PV panel

Fig. 11 shows the duty cycle-to-inductor current transfer function for the three different operating points defined in Table II. Blue line corresponds to the transfer function when the PV panel operates at the maximum power point; green line when it operates in the current source region and red line in the voltage source region. In the current source region, where the equivalent input resistance R_g is high, the zero formed by R_g and the input capacitor moves to a lower frequency and the quality factor of the second order system formed by L, C_{in} and R_g increases. Moreover, the dc gain, inversely proportional to the input resistance R_g, is below zero dB meaning that the PV panel behaves as a current source and the controlability of the inductor current is poor. In the voltage source area the dc gain increases due to the decrease in the equivalent input resistor. The poles, that were a pair of complex poles at the resonant frequency, split and the system shows an overdamped response. Fig. 12 shows the inductor current-to-input voltage transfer function for the three different operating points of the PV panel. The plant is a first order system with a pole formed by the input capacitor and the equivalent input resistance R_g. In the voltage source region where the equivalent resistance is low, the pole appears at high frequency and it moves to lower frequencies as the resistance increases. The dc gain, directly proportional to the input equivalent resistance, is low at the voltage source region and it increases as the operating point moves towards the current source region. In the voltage source region, where the PV panel behaves as an ideal voltage source, the low dc gain indicates that variations in the inductor current have small effect in the panel output voltage.

Fig. 13 shows the power stage and the control loop circuitry with defined blocks for the current and voltage loops. Table V shows the designed component values.

The design process starts by designing the inner current control loop (Fig. 10). The current sensor used is a Hall effect sensor from Allegro MicroSystems with a peak current of ± 12.5 A and sensibility of 56 mV/A. A differential amplifier is used to remove the offset introduced by the current sensor and to adapt the signal level of the measured current. The dc gain introduced by the differential amplifier is given by (29).

$$G_{Diff\ Amp} = \left(1 + \frac{R_4}{R_3}\right) \cdot \frac{R_6}{(R_5 + R_6)} \tag{29}$$

The current loop compensation (30) is formed by an integrator and a zero placed at the resonant frequency of the plant transfer function (G_{id}).

$$C_i = \frac{1}{R_7 C_1} \cdot \frac{1}{s} \cdot (1 + R_8 C_1 s) \tag{30}$$

The current loop gain is determined by (31), where $1/Vm$ is the PWM gain and Vm the modulator triangular peak value.

$$T_i = C_i \cdot \frac{1}{Vm} \cdot G_{id} \cdot G_{DiffAmp} \cdot G_{CS} \tag{31}$$

Fig. 14 shows the current loop gain for the three different points of the PV curve. The loop is closed at 5.56 kHz for the MPP point and the current source region. The phase margin is 66° and 57° respectively. In the voltage source region the crossover frequency decreases down to 4 kHz with a phase margin of 62°.

The inner current closed loop transfer function $G_{i,cl}$, (32), is required for the design of the outer voltage loop. Note that the current-error amplifier transfer function (C_i) differs depending if it is obtained from the input (negative leg) or the reference (positive leg) with a " +1" term.

$$G_{i,cl} = \frac{(1 + C_i) \cdot \frac{1}{Vm} \cdot G_{id}}{1 + C_i \cdot \frac{1}{Vm} \cdot G_{id} \cdot G_{Diffamp} \cdot G_{CS}} \tag{32}$$

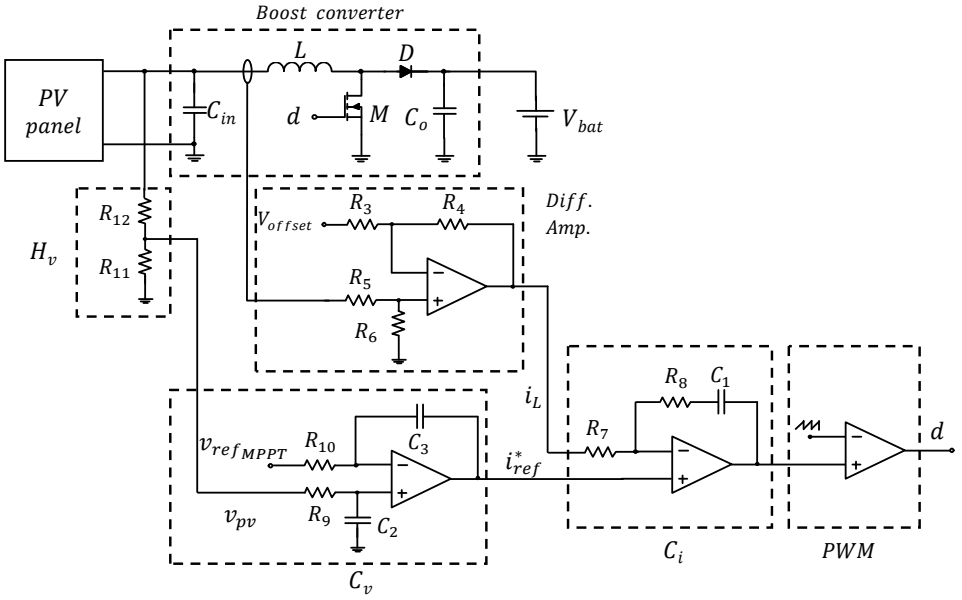

Figure 13. Boost converter and combined control loop circuitry schematic

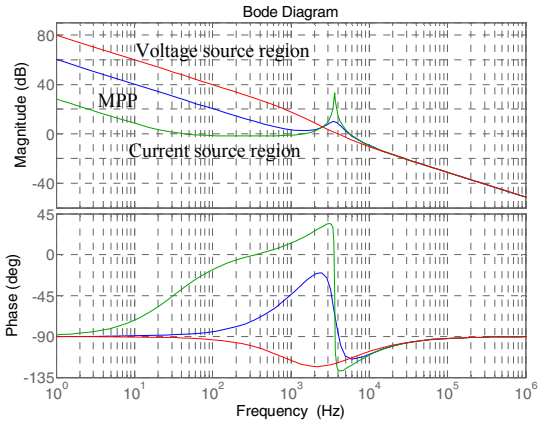

Figure 14. Current loop gain for different operating points of the PV panel

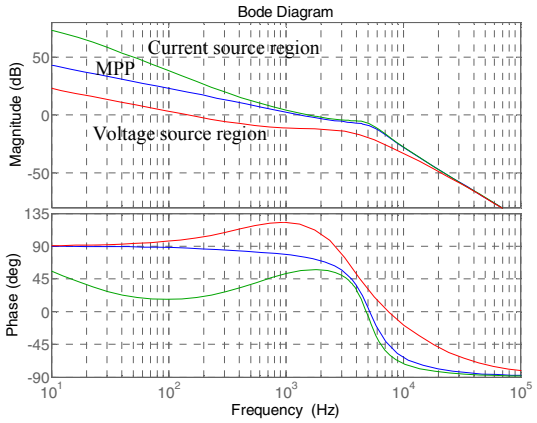

Figure 15. Voltage loop gain for different operating points of the PV panel

The voltage loop compensation (33) is designed to behave as an ideal integrator. This is achieved by inserting a pole $(R_9,\ C_2)$ at the same frequency as the zero formed by R_{10}, C_3.

$$C_v = \frac{1}{R_{10}C_3} \cdot \frac{1}{s} \cdot \frac{(1 + R_{10}C_3 s)}{(1 + R_9 C_2 s)} \tag{33}$$

A voltage divider is used for the voltage conditioning gain (H_v) to adapt the signal level of the PV output voltage to the error amplifier. The voltage loop gain is given by (34).

$$T_v = C_v \cdot G_{i,cl} \cdot G_{vi} \cdot H_v \tag{34}$$

Fig. 15 shows the voltage loop gain for different operating points of the PV panel. When the system operates at the maximum point the crossover frequency is 1.33 kHz with a phase margin of 76°. In the current source region the crossover frequency is around 1.55 kHz with a phase margin of 57°. In the voltage source region the crossover frequency goes down to 145 Hz and the phase margin is 99°.

TABLE V
LIST OF CONTROL CIRCUITRY COMPONENTS

R_{11}	1.8 kΩ
R_{12}	10 kΩ
R_3, R_7	100 kΩ
R_4	910 kΩ
R_5	51 kΩ
R_6	470 kΩ
R_8	19 kΩ
R_9, R_{10}	47 kΩ
C_1, C_2, C_3	2.2 nF
Operational amplifiers	$TSV632$
Current sensor	$ACS710$
PWM controller	$TL494$

Fig. 16 shows the calculated and simulated closed loop transfer function at the MPP. Fig. 17 presents the step response at the MPP calculated by using MATLAB.

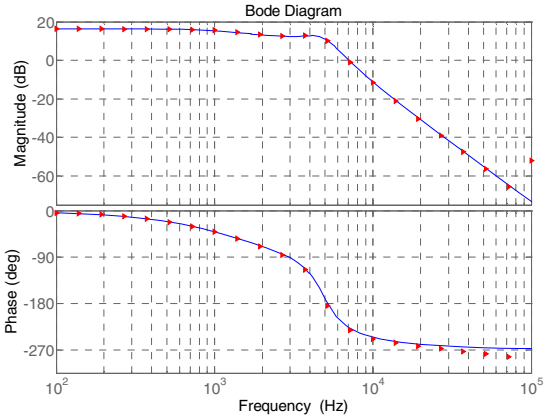

Figure 16. Closed loop transfer function in MATLAB (blue line) and LTspice (red dots) for the PV panel linearized at the MPP

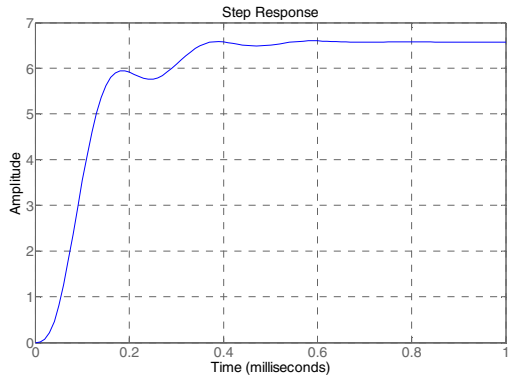

Figure 17. Calculated input voltage step response to a 1 V reference change for the PV panel linearized at the MPP

The calculated closed loop transfer function (35) shows very close match with the simulation. The system presents a bandwidth of 1.9 kHz and a settling time of 0.5 ms (2% criterion).

$$G_{v,cl} = \frac{(1 - C_v) \cdot G_{i,cl} \cdot G_{iv}}{1 - C_v \cdot G_{i_{cl}} \cdot G_{iv} \cdot H_v} \tag{35}$$

IV. EXPERIMENTAL RESULTS

A 104,4 W boost converter is constructed using a fast prototyping technique. The inductor is designed by using a planar magnetic core, size E32/6/20 with plate in material 3F3 from Ferroxcube. Fig. 18 shows a view of the converter prototype. Fig. 19 shows the converter steady-state operating waveforms for $V_{in} = 18$ V, $I_{in} = 5.8$ A and $V_{out} = 28$ V.

The efficiency of the power stage is measured by using a power analyzer PPA5530 from N4L. The measurement is done in open loop at $V_{in} = 18$ V, $I_{in} = 5.8$ A and $V_{out} = 30$ V. The measured converter efficiency @ $P_{out} = 101{,}6$ W is 97.3 % $\pm$ 0.2 % (without accounting the losses due to the control circuitry and MOSFET gate drive).

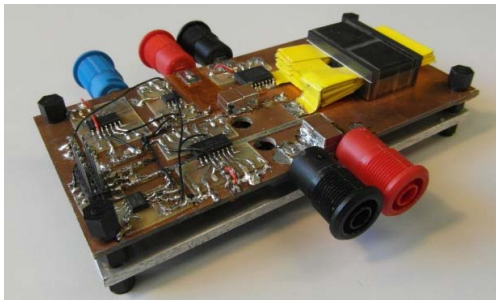

Figure 18. Boost converter with combined control loop prototype

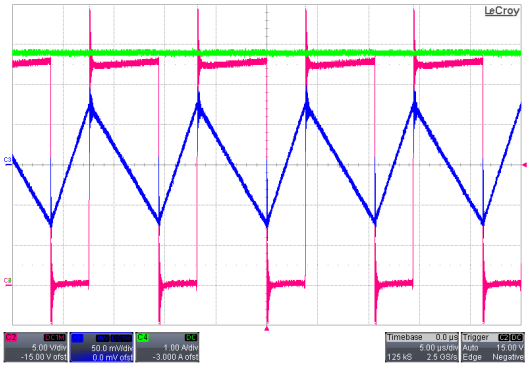

Figure 19. Converter steady-state operating waveforms. Drain to source MOSFET (red, 5V/div), input current (green, 1A/div) and inductor ripple (blue, 500mA/div). Time scale 5us/div

In order to verify the control loop design, a measurement of the loop gain is performed by using a frequency response analyzer N4L PSM1735. In order to simulate the operating conditions of the photovoltaic panel at the maximum power point, the measurements are executed by using a voltage source (V_g) with a series resistance (R_g). This set up allows to linearize the I-V PV panel curve around the MPP. The converter operating conditions during the measurement are: $V_g = 38.02$ V, $R_g = 3.43\ \Omega$, $V_{bat} = 28.35$ V and $I_{in} = 5.8$ A. Fig. 20 shows the measured loop gain transfer function (red line) and the calculated transfer function (blue line). It can be observed that the calculated crossover frequency (1.33 kHz) matches perfectly with the measurement.

Hill-climbing MPPT algorithms continuously perturb the reference, causing the PV voltage to fluctuate even if the irradiance and temperature are constant. The time between perturbations should be long enough so that the converter reaches steady-state operation. The tracking performance of the control loop is tested (Fig. 21) by perturbing the reference signal every 2.5 ms. The amplitude of the perturbation is selected to be 160 mV, which corresponds to 1 V step change in the PV panel. Note that the small slopes observed in the signals are a result of the measurement being performed with ac coupling in all the oscilloscope channels.

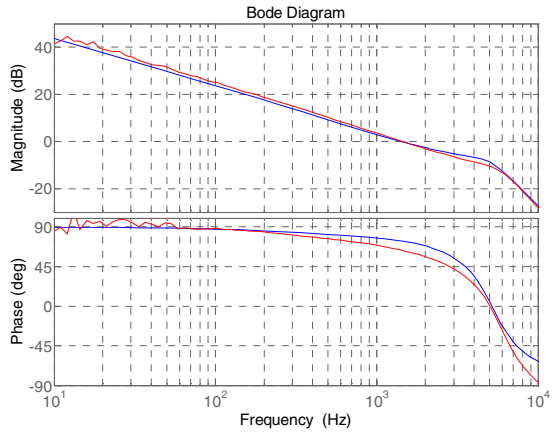

Figure 20. Voltage loop gain transfer function measured (red) and calculated (blue)

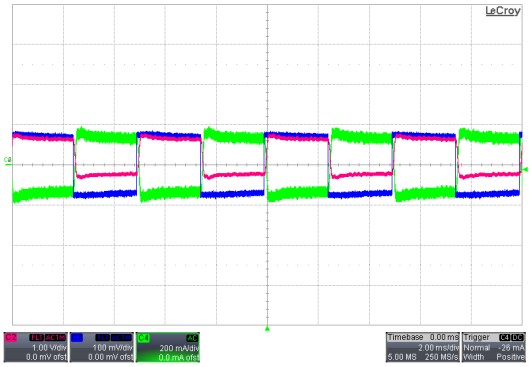

Figure 21. Voltage loop reference tracking. Reference signal (blue line, 100mV/div), input current (green line, 200mV/div) and input voltage (red line, 1V/div). Time scale 2ms/div

The converter stabilizes around 0.6 ms, as shown in Fig. 21. Compared with the control scheme presented in [11], where the converter operating point is perturbed every 25 ms, this fast time response brings several benefits to the MPPT capabilities of the converter. First, the amplitude of the perturbation can be adjusted to achieve fast tracking during fast changing irradiation conditions, while maintaining a small error in steady-state conditions. Second, under partial shading conditions, the fast tracking capabilities will allow to perform very fast sweeps over the whole PV panel *I-V* curve to determine the position of the maximum power point. In this way, the amount of wasted energy during the sweep is minimized.

V. CONCLUSION

A boost converter with input voltage control for photovoltaic applications is designed and tested. The PV output voltage is selected to be the control variable because it presents small variations with changes in irradiation. In order to obtain a fast dynamic response of the converter, a double control loop is implemented. The system controls the input voltage of the converter by regulating the mean value of the inductor current. By including the inner current loop with higher crossover frequency, the overall system presents a faster response. This helps to avoid propagating load perturbations to the photovoltaic panel side. The mathematical model obtained by average state-space modeling shows a very close match to the measured loop gain transfer function. The converter control scheme plays an important role in the performance of MPPT algorithms. The designed control loop allows the system to be perturbed every 1 ms, which enhances the converter maximum power point tracking capabilities.

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B

Simulation Tool for Designing off-Grid PV Applications for the Urban Environments

28th European Photovoltaic Energy Conference and Exhibition (EU-PVSEC 2013)

SIMULATION TOOL FOR DESIGNING OFF-GRID PV APPLICATIONS FOR THE URBAN ENVIRONMENTS

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ABSTRACT: A barrier for exploiting use of standalone solar lighting for the urban environment seem to be lack of knowledge and lack of available tools for proper dimensioning. In this work, the first part of the development of powerful dimensioning tool is described and initial measurements are presented.
Keywords: PV urban lighting, Energy systems, standalone, LED lighting, dimensioning

1 INTRODUCTION

Digging down cables for small electrical applications in the urban environment is extremely expensive due to the high labor cost associated with it. Small stand-alone PV applications powered by 0.5-50 Wp can become very attractive since e.g. in Copenhagen in Denmark the cost of digging down cables in the city is about 1000 $ pr. running meter so the cost savings on the cable digging can easily pay for the solar cells and electronics. The requirements to the products from the municipalities are high so if e.g. the products are for lighting purpose the reliability of the product meeting some specified amount of light is very important. The willingness to pay for such high-end stand-alone PV applications is though high but it is essential to be able to evaluate if the product will work in a given environment in both the development and dimension phase of the product and as a credible proof tool towards consumer/buyer/decision makers.

The barrier for exploiting this potential seems to be the lack of knowledge and tools for dimensioning and designing PV applications for the urban environments. The authors investigated the many PV dimensioning tools on the market and found none addressing exactly this issue and in the present project a design and simulation tool for small PV applications for the urban environment is under development.

2 PV-LED ENGINE MODEL

The block diagram below (Figure 1) shows the design of the simulation tool, which essentially is a computer model of a basic PV application, including PV panel, electronics, battery and power consumption.

Inputs to the model are data such as geographical position, orientation, local environment class and specifications about the PV module, control system, battery, etc. Also, a system data bank contributes with meteorological data and components data. Based on these parameters, the model calculates the performance of the PV application in a time resolved manner. The output of the model gives a detailed view on the energy flow in the system so sizing becomes easy.

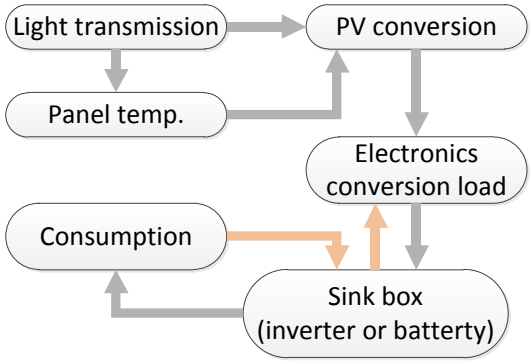


Figure 1: Block diagram of the PV simulation tool.

3 CHARACTERIZATION

To give a first implementation of the model, it is compared with the performance of a number of commercialized available high end park lamp products. These products are put out in the field in different environments and the performance of the PV-panel, electronics, battery and LEDs are logged. Few selected of these are also taken to lab where they have been disassembled and the sub-parts are afterwards characterized in the lab, to give input to the model.

3.1 Position Characterization

The conditions of the field positions are measured using a commercialized available hand-held shade measurement tool for solar site assessments (SunEye 210 Shade Tool, Solmetric). Equipped with fisheye lens camera, compass, GPS and shading identifying image processing software, this tool provides shading patterns, annual sun paths and monthly solar access, etc. Below (Figure 2) a solar access chart of one particularly site is shown.

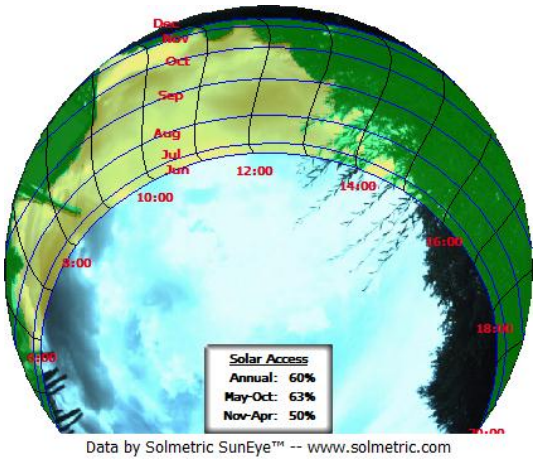


Figure 2: Solar access chart provided by the SunEye tool.

3.2 Parts Characterization

In order to accurately determine the performance of a particular park lamp product, the product is disassembled and each part is characterized in details so the performance can be estimated by interpolation of data points.

A typical park light system consists of a small PV module in the range 0.5-5 Wp, an electronic controller managing the charging of the battery and managing the power flow to the LED, a battery and a LED.
Each of these 4 components is characterized in dedicated labs under different load conditions.

For the PV part IV-curves is recorded under 10-15 different illuminations, all AM 1.5 varying from .05 Sun till 1.2 Sun, and the full IV-curves is put into the simulation since it turns out that far from all charge controllers have maximum power point trackers. The IV curves are plotted in Figure 3 with the current on the left and the sun intensity on the right, which should be read at the left axis intersection – i.e. at the short circuit current.

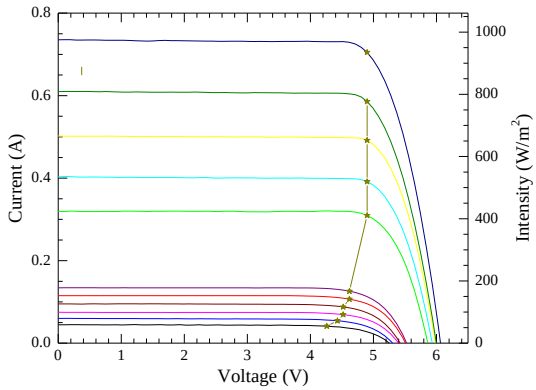


Figure 3: IV-curves.

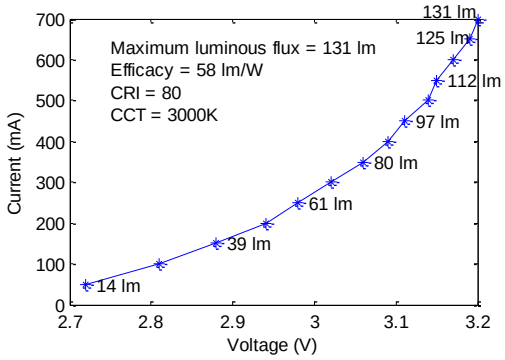
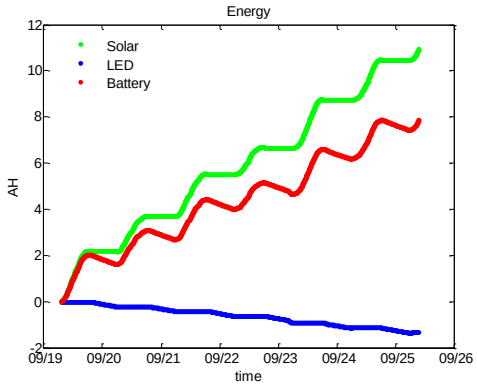


Figure 4: Example of concluded results from a characterization measurement of a LED light source in one of the purchased park lamps.

Included in the work of validating the model is characterizing the different components of the park lamps purchased, as briefly mentioned above. Figure 4 shows some concluded results of one of the park lamps LED light source, after being measured in the lab. Besides the quality of the light, such as Correlated Color Temperature (CCT) and Color Rendering Index (CRI), parameters related to the efficiency of the light source are being measured, such as total luminous flux, efficacy and total radiant flux. All these parameters are possible inputs in the model, which will make it possible to investigate the potential of improvements associated with different available products.

3.3 Field measurement

A few Park lights were put onto to our test side, equipped with data logging in order to determine the energy flow in the system with reference to a pyranometer (Kipp & Zonen SMP3-I) installed nearby. Since typically the PV is voltage controlled, measuring the current in the PV loop requires special attention. Measuring the current by measuring a voltage drop over a resistor, gives an additional voltage drop in the loop and perturbs the control of the PV. Choosing a resistive current measurement, the resistor should be chosen to be as small as possible, however large enough to provide good resolution to the data logger. Therefore a current sensor that senses without introducing a voltage drop in the loop is preferred; however these are expensive for the relevant current range. Another alternative is to improve the resolution by amplifying the voltage over the measurement resistor. For the data logging in this system the current is measured via a very small resistor limiting the resolution on the current measurements. The cumulative energy flow for few selected days is plotted in Figur 5, with the zero being arbitrary. The data is recorded close to fall equinox and therefore it is to be expected that there is energy enough for the night to light the LED, as can be seen as a straight blue line. For this product the size of the battery around 6 AH, however the charge controller seems to continue charging even though the battery is full, and thereby degrading the battery.



Figur 5: Energy gain for a few days in septemeber. The starting point is arbitrary chosen and the battery was not empty.

4 FUTURE WORK

The next step forward in this project is to collect measurements on the electronic controller and the batteries that will enable to simulate the behavior of the chosen park light and later on validate the model by comparing the simulated behavior with the actual measured behavior.

The resolution on the current measurement on the field testing will be improved and generic models that describe system behavior via datasheet information will be developed.

Parallel to the modeling work prototypes of park lights will be demonstrated where both dedicated power electronics, PV and LEDs will be chosen and combined with intelligent dimming control. The total system electronic efficiency is expected to be above 80 %.

5 CONCLUSION

We have demonstrated important building blocks to facilitate a powerful dimensioning tool and partial validated it to existing product. Measurement on existing products shows a lot can be done by upgrading the performance of the electronics.

6 AKNOWLEDGEMENTS

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C

PV LED Engine Characterization Lab for Standalone Light to Light Systems

29th European Photovoltaic Energy Conference and Exhibition (EU-PVSEC 2014)

PVLED ENGINE CHARACTERIZATION LAB FOR STANDALONE LIGHT TO LIGHT SYSTEMS

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Keywords: solar cells, PV applications, characterization, energy systems

ABSTRACT: PV-powered light systems, light to light systems (L2L), offer outdoor lighting where it is elsewhere cumbersome to enable lighting. Application of these systems at high latitudes, where the difference in day length between summer and winter is large and the solar energy is less requires smart dimming functions for reliable lighting. In this work we have build a laboratory to characterize these systems up to 200 WP from "nose to tail" in great details to support improvement of the systems and to make accurate field performance predictions.

1 INTRODUCTION

Light to light systems are typically solar powered stand alone lamps using a LED as light source. Park lights and bollards are examples of L2L systems and these systems offers lighting solutions, for places where lighting is not feasible due to very high cabling costs of e.g. 700 € /m in Copenhagen. At low latitudes dimensioning of such products is relatively easy, since there is plenty of sun and the difference between day length between summer and winter is small. However in locations further away from equator, the difference in day length between summer and winter increases, and the solar potential is less. Therefore construction of reliable lighting with feasible dimensions requires intelligent harvesting and efficient usage of energy becomes crucial[1]. Since high power MPPT-charge regulators are not subjected to any standards e.g.[2] not all charge regulators comply with the manufactures specification[3], and within this work low maximum power point tracking (MPPT)-efficiencies of commercially available regulators are measured, and therefore this work emphasize the importance of full system testing.

In this work we build a laboratory where we can measure all the parts of such light to light systems, and use the data for optimization of products and accurate prediction of field performance.

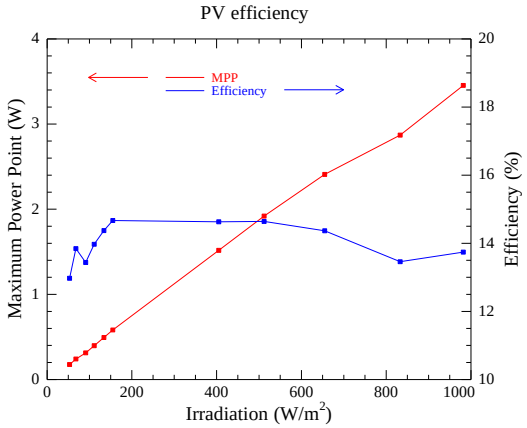
2 THE LAB

The idea behind the lab is to characterize all subparts under the specific loads they experience in the field. Therefore IV curves of the PV panels are measured under different illuminations starting from around 50 W/m^2 to 1000 W/m ^{2}. These measurement are fed in to the Solar Array simulator.

2.1 IV Characterization

A Newport class AAA solar simulator is used for illumination of the panels, and IV-curves from 50 W/m^2 to 1000 W/m^2 are recorded, using a Keithley 2401 SMU for small panels.

An example of such series of measurement is shown in Figure 1.



Figur 1: Measurement of the Solar panel at difernt illumination. An IV-curve is recorded for each measurement point.

2.2 Electronic characterization

We characterize 4 electronics features on the electronic controller board:

- The MPP-tracking efficiency
- The Charge conversion efficiency
- The efficiency of the LED supply
- The standby consumption.

The electronic characterization lab consists of 3 different emulators and a 3 channel power analyzer to measure the powerflow.

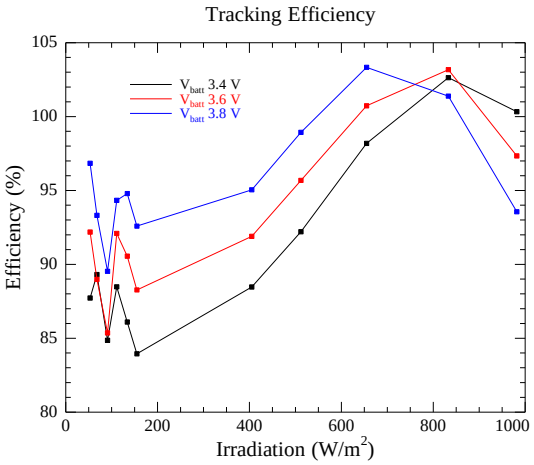
The equipment are:

- Two Agilent B2962 - 2 Channel programmable source measure unit, 30 W pr channel. The channels are floating enabling serial and parallel connection of the channels
- One Agilent Solar Array Simulator E4360A mainframe with a E4361A DC module (0-65 V and 0 8.5 A)
- One Keithley 2651A Highpower Sourcementer (200 W 2000 W pulsed)
- One Tektronix Poweranalyzer PA4000 3CH.

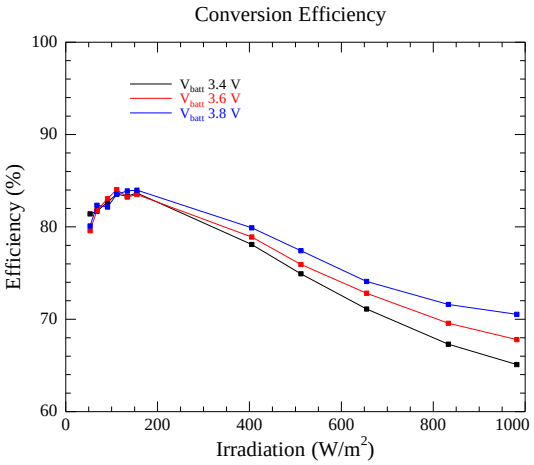
CHARGE EFFICIENCY MEASUREMENTS

The charge part of the characterization is done using either an Agilent E4361A Solar Array Simulator for larger PV modules and for smaller PV modules an Agilent B2962 Source Measure Unit (SMU) as an emulator. The SAS is not very accurate for power levels under 5 - 10 watts. As battery the Keithley 2651A Source meter is used in constant voltage mode, and since charge

currents is typically below 0.2 C the constant voltage emulates the battery fairly well. The devices supports though more advanced battery emulation.
All voltages and currents are measured using a precision power analyzer PA 4000 from Tektronix.
As input to the solar emulators the measured sets of VOC, ISC, VMP and IMP, recorded at different light intensities are used. The set of IV-curve parameters is measured for different relevant battery voltages, and thereby a full mapping of the working ranges is obtained for a specific system. The measurement and data acquisition is automated in Labview.
Based on these measurements the tracking efficiency and the conversion efficiency are obtained and examples are shown in figures 2 and 3.



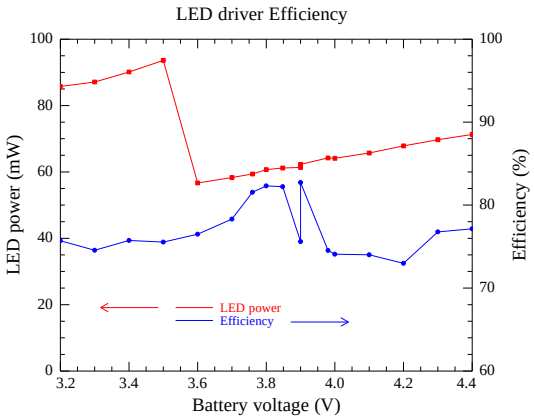
Figur 2: The powerpoint tracking efficiency as a function of irradiation. The efficiencies above 100 %, is explained by the accuracy of the emulator, in this case the Agilelent E436x SAS system.



Figur 3: The conversion efficiency of the charger. This chargers seems to be optimize for low power.

LED DRIVER EFFICIENCY MEASUREMENTS

The LED driver is also tested by letting the Ketihley 2651A emulate a battery in constant voltage mode, vary the battery voltage and using the real LED as sink. The system tested here is simple without a clock and therefor it turns the LED on once the PV Energy is decreased to zero. Therefore for this system a LED output can be stimulated with a constant battery voltage and a solar input for a short while e.g a minute. The LED output is stimulated after the solar input is turned on. However some controllers are time based why it is sometimes hard stimulate a LED output for the controller.



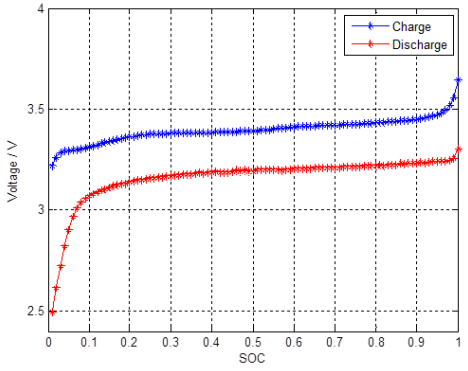
Figur 4: The led drive efficiency and Power. The sudden decrease in powerlevel at 3.5 volts has no explaination, but is a reproducible system behaviour.

STANDBY POWER MEASUREMENTS

The Power analyzer has a special standby mode, where it measures the standby by integrating the power over a period set by the user and then output the average power. With a similar approach as for the LED driver the standby power consumption, can be measured when the LED is disconnected. The measurement in Figur 3 also includes the standby power in the efficiency calculation and therefore this measurement provides sufficient information for a field performance prediction. However, the standby power consumption measurement is a powerful tool to differentiate the converter loss and standby power consumption enabling a more targeted product improvement.

2.3 Battery characterization

Charge and discharge curves are recorded using an ELV ALC 8500 Expert battery tester. This device can charge and discharge the battery at a specified rate, and record the data, and an example of a such measurement is showed in figure 5.

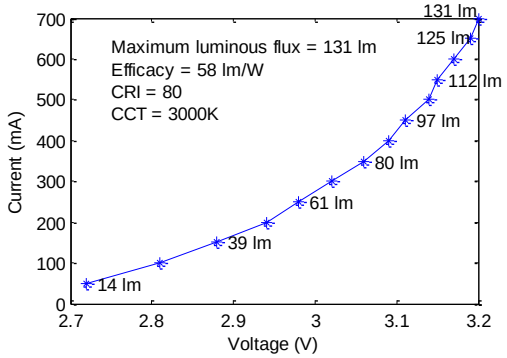


Figur 5: Charge and discharge curve of a NiMH battery.

2.4 Luminaire testing

The Led is characterized at DOLL quality lab[4], where both a gonio photometer (Techno Team, Rigo 801), and

an integrating sphere (Instrument Systems, ISP 1000 and ISP 2000), which are both equipped with a spectrometer (Instrument Systems, CAS 140, 380-1040 nm) and a high quality luxmeter (PRC Krochman, f_1'<1.2).
The Integrating sphere measures the total luminous flux, and the gonio photometer measures the light distribution from a luminaire.
Figur 6 shows an example of a measurement in the integrating sphere, where the luminous flux is measured as a function of voltage and current.



Figur 6: Characterization of an LED

3 FIRST MEASUREMENTS

A measurement on a commercial high end system was done, and the results can be found in figures 1-6. The average conversion efficiency is 78% and the tracking efficiency is 93.5 % giving the controller a total charging efficiency of 72 %, the average battery efficiency is 94 % and further the average LED driver efficiency is 77%. i.e approximately only 53% of the incoming electric power is available for the LED.

4. CONCLUSIONS

These preliminary measurements provide a deep insight in the losses and the behavior of these smaller light to light systems. Further the preliminary measurements indicate that the electronic controller in the L2L systems has the highest potential for improvement.
Future work includes implementing the shown laboratory measurement in the PV LED engine software, and use these data for accurate field prediction.

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D

Design, Characterization and Modelling of High Efficient Solar Powered Lighting Systems

32th European Photovoltaic Energy Conference and Exhibition (EU-PVSEC 2016)

Design, characterization and modelling of high efficient solar powered lighting systems

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EUPVSEC Topic 6.4: PV Applications Without a Centralized Grid

Abstract
This paper discusses some of the major challenges in the development of L2L (Light-2-Light) products. It's the lack of efficient converter electronics, modelling tools for dimensioning and furthermore, characterization facilities to support the successful development of the products. We report the development of 2 Three-Port-Converters respectively for 1-10Wp with a peak efficiency of 99.1% at 1.5 W output power at PV to battery and almost similar characteristics for a 10-50 Wp. Furthermore, a modelling tool for L2L products has been developed and a laboratory for feeding in component data not available in the datasheets to the model is described. A living lab facility is realized to field test prototypes of L2L lighting products in their development state to validate the modelling tool and tweak the parameters in the system for optimized performance the product.

Introduction
The last few year significant progress has been made in research and development of renewable systems. Solar energy is one of the most reliable, daily available and environment friendly renewable energy source, being unlimited, clean and free [1], [2]. Furthermore, due to the ability to generate off-grid electricity, sustainable energy systems have attracted research interest in the last decades [3]. Due to the rapid increasing efficiency of light emitted diodes (LEDs) stand-alone combinations of PV module, battery storage and LED luminaires is becoming more attractive for a variety of lighting applications [4]. The systems operates entirely on DC and is often called Light-to-light (L2L) systems, see Fig. 1. Park lights and bollards are examples of L2L systems and these systems offers lighting solutions, for places where lighting is not feasible due to very high cabling costs of up to e.g. 700 €/m in Copenhagen and up to 2000€/m in Berlin [5]. Some of the major obstacles still remaining for successful L2L systems are 1) lack of efficient conversion electronics for small PV systems, (PV powers of 1-50 Wp) 2) lack of a dimensioning and assessment tool for L2L systems and 3) knowledge centers and laboratory facilities for supporting the complicated process of designing successful L2L products. The latter being an interdisciplinary technical task involving at least knowledge, tools, and test equipment for the technology fields of lighting, photovoltaics and power electronics. A series of Danish research projects has addressed these issues and the results are reported here.

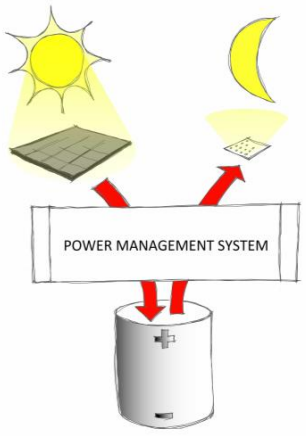

Fig. 1. A principle sketch of a Light-2-Light system.

Electronic Converter
An electronic converter for outdoor light-to-light purposes should be able to work in two modes:

1. In the daytime: Convert energy from the PV panel while maintaining Maximum Power Point Tracking (MPPT) in order to harvest as much energy to the battery from the available solar energy as possible.
2. In the night: Convert stored energy from the battery to the operating point of the LED panel.

Hence this application calls for a Three-Port-Converter (TPC) with two operating modes as sketched in Fig. 2.

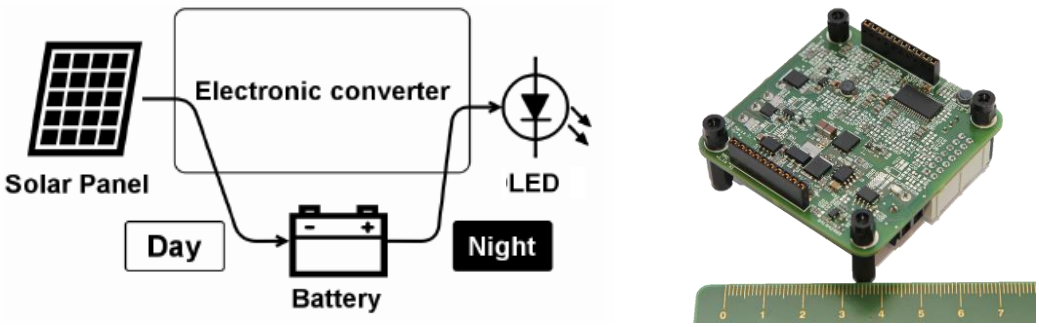

Fig. 2. Working principle of the converter (left) and image of prototype of 1-10 Wp converter (right)

To cover the full range of 1-50 Wp of solar panels with high efficiency, 2 versions of converters was developed. A low range for PV powers 1-10 Wp and a high power range of 10-50 Wp, giving the versatility of choosing solar panels in the whole span. The efficiency curve for the 10 Wp version is shown in Fig. 3. It is sought to achieve the peak conversion efficiency in the lower part of its operating range since L2L products often are placed in areas with a lot of shadows on the solar panels e.g. in parks or in the urban environments, making peak power operation rare.

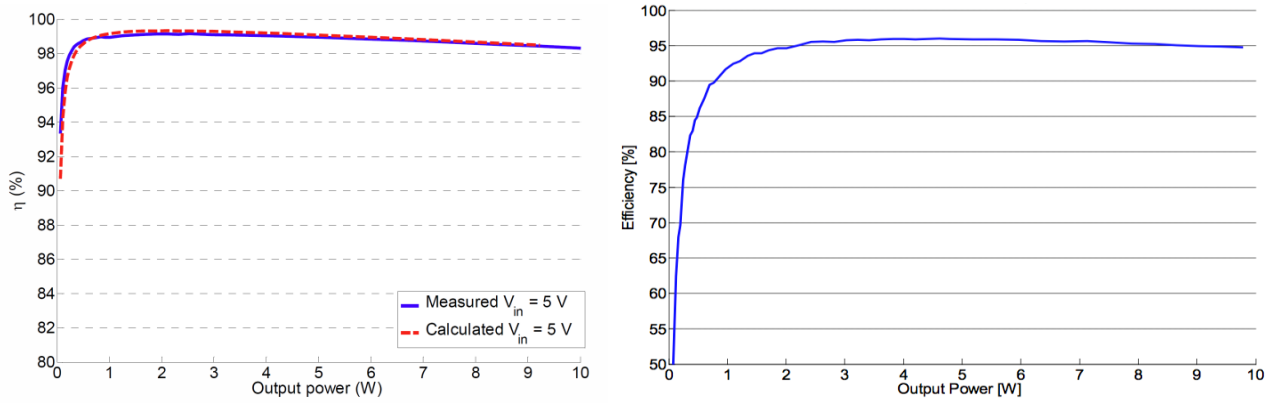

Fig. 3. Efficiency curve of the 10 W converter when harvesting energy from PV panel to the battery (left). It can be seen that the converter excels in having its highest efficiency at the lowest power obtaining >99% from 1.2W to 4W output power. The curve (right) shows the LED driver stage efficiency peaking at 3W output power with 97.3%.

The converters peak efficiency is 99.1 % when operating at 1.5 W. The output power and the LED driver stage present a peak efficiency of 97.3% at 3W output power. The electronics converter work is documented in [6] and [7].

Software for dimensioning and simulation of PV LED applications

The authors have investigated several software tools on the market and none was found suited for the task of dimensioning and simulating performance of solar powered L2L products. A customized tool is therefore developed in MATLAB as a starting point with input from several specialized tools. The block diagram, Fig. 4, shows the design of the simulation tool, which essentially is a computer model of a basic PV application, including PV panel, electronics, battery and power consumption in the form of an LED luminaire. The L2L dimensioning tool differs since it uses highly time resolved weather data in 1-minute resolution. This is important when modelling solar products operating most of its time in the shadows from buildings and other artefacts. The efficiency curve, Fig. 3, of the developed converter is rather flat in the whole irradiation interval from 0-1 sun. The full electronic controller unit, however, consist of both converter and controller with a microcontroller operating in several states, running algorithms, and controlling other external devices as a battery management system, motions sensors etc. The real energy conversion functions are therefore usually far from linear and depend heavily on irradiation level on the PV panel, temperature, battery voltage and other parameters which need to be modelled for precision. The energy flow is basically made up of

1. Energy flow from the sun to the PV panel
2. Energy flow from the panel – through the charger – and into the battery
3. Energy flow from the battery – through the discharger – into the LEDs
4. Stand-by consumption of the electronics controller due the intelligent disposition of the energy for lighting (the lighting scheme) and the loss in its external components (if any).

The datasheets of small solar panels, PV/LED controllers and batteries are rarely having data for this type of modelling to be done.

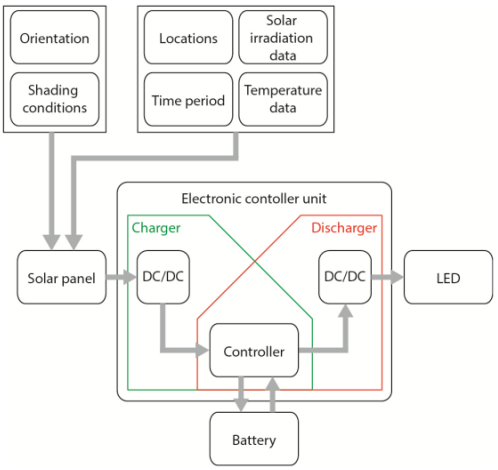

Fig. 4. Block diagram of L2L modelling tool.

Laboratory for characterization of L2L products

A specialized laboratory has been built, to feed the mathematical simulation tool with accurate and sufficient data for modelling of L2L products and support the development of successful solar powered LED products. It is composed of the following facilities

Component characterization

- Solar cell electrical (I, V, Irradiation 0-1 sun AM 1.5)
- Solar panel electrical (I, V, Irradiation 0-1 sun AM 1.5)
- Battery (I, V, Charge, Temp)
- LED electrical and photometrical (I, V, lumens)
- Electronics controller
    - Charging efficiency (Emulation of the PV panel and the battery, allowing mapping of the full operating range for the charger)
    - Discharge efficiency (Vbat, I_{LED}, V_{LED})
- Shade measurement/simulation

Luminaire characterization

- Spectroradiometry
- Photometry
- Goniospectroradiometry
- Goniophotometry

The measurements are tailored to fit into the L2L modelling tool and are more or less automated to characterize the individual components in the many different operating states needed. The luminaire characterization is not part of the model but a part of the process of creating highly efficient high end L2L products. The light rays need to illuminate the desired object nicely without the light being lost in reflectors and diffusers, giving rise to glare or other waste mechanisms. Here good optical engineering can reduce the total amount of light needed, and thus improving the efficiency. The relevant metric is useful lux or useful lumens which can be modelled by use of e.g. DIALux and RELUX which can be used iteratively with the L2L model.

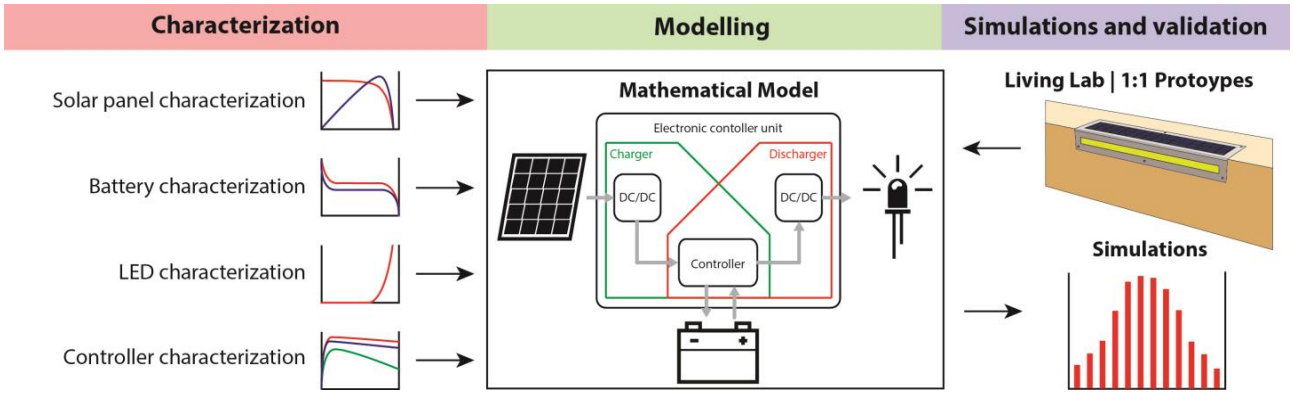

Fig. 5. Diagram of the data feed-back loop for simulation of L2L products and validation of the model.

L2L - Living Lab

A living lab for installation and monitoring the energy flow inside the L2L products is made and will be expanded in the coming years the university campus of the Technical University of Denmark around the building of Department of Photonics Engineering in Roskilde. The modelling tool can thereby be validated against periods with known weather data where data logging has been implemented in the products. The differences between simulated performance of a product and the logged performance is due to inaccuracies in the model and is a valuable tool to optimize it. The validation process will be disclosed later in a publication. Fig. 5. shows the data feed-back loop.

Prototype development of L2L products

Several products have been designed parallel in the process of developing the L2L converter electronics, the L2L simulation tool and L2L laboratory and living lab. The products were developed together with the company, Outsider, who is designing, producing and distributing high-end solar powered lighting product for the urban environments. 2 Products were developed together with Outsider and the Architecture company, Snøhetta, for the King Abdulaziz Centre for World Culture in Dhahran Saudi Arabia, see Fig. 6 (left). below.

Fig. 6. King Abdulaziz Center for World Culture - Rendering Snøhetta/Mir (left). LIGHT-TUBE (right)

One of the products are called LIGHT-TUBE and is inspired by bulrushes swaying gently in the wind, shown Fig. 6 (right). Especially the shade modelling was a special challenge of this product along with temperature modelling of the systems that had to be done to fit the data to the model. The PV is integrated in the base of the product and the LEDs in the end of the metal stick where luminaires is composed of edge-lit accryllic wave guides, sandblasted on the sides.

Conclusion

3 major challenges in the development of L2L products is the lack of efficient converter electronics, modelling tools for dimensioning and furthermore, characterization facilities to support the successful development of the products. Above we report the development of 2 Three-Port-Converters respectively for 1-10Wp and 10-50 Wp PV panels with a peak efficiency of 99.1% at 1.5 W of output power for the 10 Wp version PV to battery conversion state. Furthermore, a modelling tool for L2L products has been described and a laboratory for feeding in component data not available in the datasheets to the model is described. A living lab for field test of L2L product to validate the modelling tool and assisting in the development process of L2L products is also under development.

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E

Designing High Efficient Solar Powered Lighting Systems

43rd IEEE Photovoltaic Specialist Conference (PVSC 2016)

Designing high efficient solar powered lighting systems

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[b] Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby, Denmark
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***Abstract* — Some major challenges in the development of L2L products is the lack of efficient converter electronics, modelling tools for dimensioning and furthermore, characterization facilities to support the successful development of the products. We report the development of 2 Three-Port-Converters respectively for 1-10Wp and 10-50 Wp with a peak efficiency of 97% at 1.8 W of PV power for the 10 Wp version. Furthermore, a modelling tool for L2L products has been developed and a laboratory for feeding in component data not available in the datasheets to the model is described.**

I. Introduction

Due to the rapid increasing efficiency of light emitted diodes (LEDs) stand-alone combinations of PV module, battery storage and LED luminaires is becoming more attractive for a variety of lighting applications [1]. The systems operate entirely on DC and is often called Light-to-light (L2L) systems, see Fig. 1. Park lights and bollards are examples of L2L systems and these systems offers lighting solutions, for places where lighting is not feasible due to very high cabling costs of up to e.g. 700 €/m in Copenhagen and up to 2000€/m in Berlin [2]. Some of the major obstacles still remaining for successful L2L systems are 1) lack of efficient conversion electronics for small PV systems, (PV powers of 1-50 Wp) 2) lack of a dimensioning and assessment tool for L2L systems and 3) knowledge centers and laboratory facilities for supporting the complicated process of designing successful L2L products. The latter being an interdisciplinary technical task involving at least knowledge, tools, and test equipment for the technology fields of lighting, photovoltaics and power electronics. A series of Danish research projects has addressed these issues and the results are reported here.

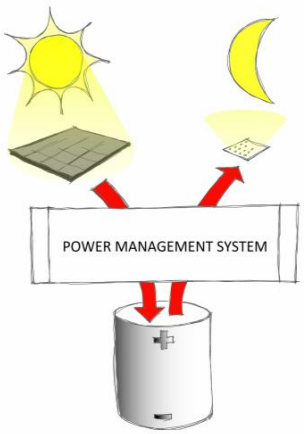


Fig. 1. A principle sketch of a Light-2-Light system.

II. Electronic Converter

An electronic converter for outdoor light-to-light purposes should be able to work in two modes:

1. In the daytime: Convert energy from the PV panel while maintaining Maximum Power Point Tracking (MPPT) in order to harvest as much energy to the battery from the available solar energy as possible.
2. In the night: Convert stored energy from the battery to the operating point of the LED panel.

Hence this application calls for a Three-Port-Converter (TPC) with two operating modes as sketched in Fig. 2.

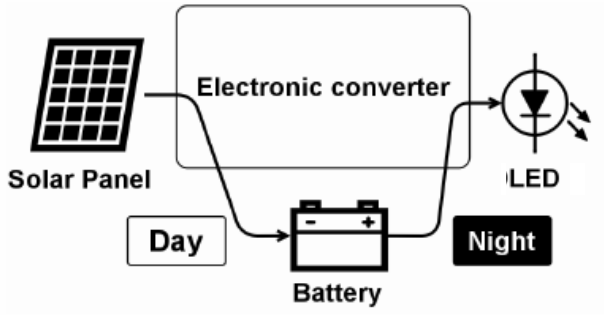


Fig. 2. Working principle of the converter

To cover the full range of 1-50 Wp of solar panels with high efficiency, 2 versions of converters was developed. A low range for PV powers 1-10 Wp and a high power range of 10-50 Wp, giving the versatility of choosing solar panels in the whole span. The efficiency curve for the 10 Wp version is shown in Fig. 3. It is sought to achieve the peak conversion efficiency in the lower part of its operating range since L2L products often are placed in areas with a lot of shadows on the solar panels e.g. in parks or in the urban environments, making peak power operation rare.

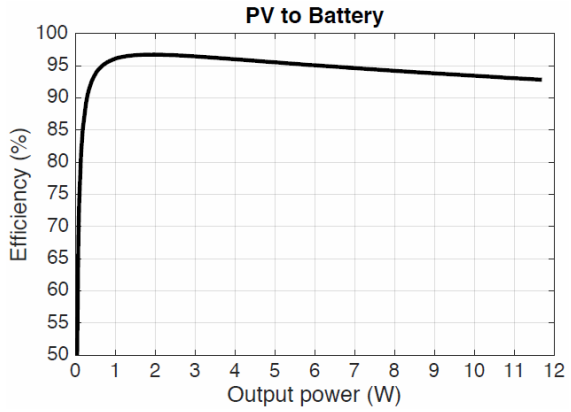
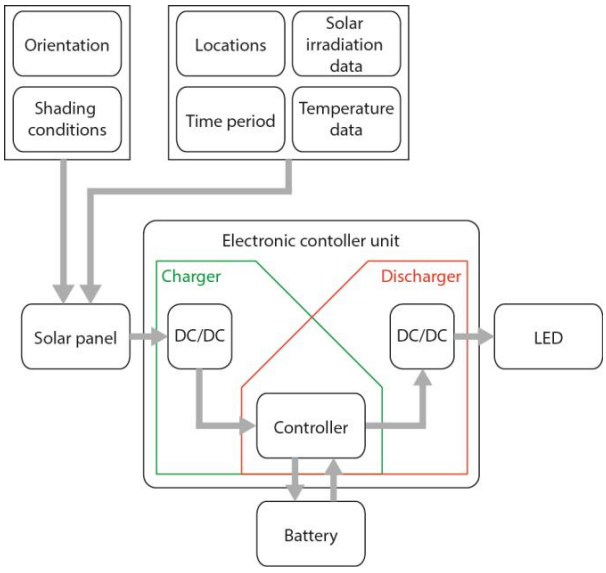


Fig. 3. Efficiency curve of the 10 W converter when harvesting energy from PV panel to the battery. It can be seen that the converter excels in having its highest efficiency at the lowest power obtaining 94 % at 0.5 W and peaking at 97% at 1.8 W.

The converters peak efficiency is 97 % when operating at 1.8 W. The conversion from battery to light is of similar efficiency. The electronics converter work is documented in [3] and [4].

III. Software for Dimensioning and Simulation of PV LED Applications

The authors have investigated several software tools on the market and none was found suited for the task of dimensioning and simulating performance of solar powered L2L products. A customized tool is therefore developed in MATLAB as a starting point with input from several specialized tools.



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IV. Laboratory for Characterization of L2L Products

A specialized laboratory has been built, to feed the mathematical simulation tool with accurate and sufficient data for modelling of L2L products and support the development of successful solar powered LED products. It is composed of the following facilities

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IV. Case

Several products have been designed parallel in the process of developing the L2L converter electronics, the L2L simulation tool and L2L laboratory. The products were developed together with the company, Outsider, who is designing, producing and distributing high-end solar powered lighting product for the urban environments. 2 Products were developed together with Outsider and the Architecture company, Snøhetta, for the King Abdulaziz Centre for World Culture in Dhahran Saudi Arabia, see Fig. 5. below.

Fig. 5. King Abdulaziz Center for World Culture - Rendering Snøhetta/Mir.

One of the products are called LIGHT-TUBE and is inspired by bulrushes swaying gently in the wind, shown Fig. 6. Especially the shade modelling was a special challenge of this product along with temperature modelling of the systems that had to be done to fit the data to the model. The PV is integrated in the base of the product and the LEDs in the end of the metal stick where luminaires is composed of edge-lit accryllic wave guides sandblasted on the sides.

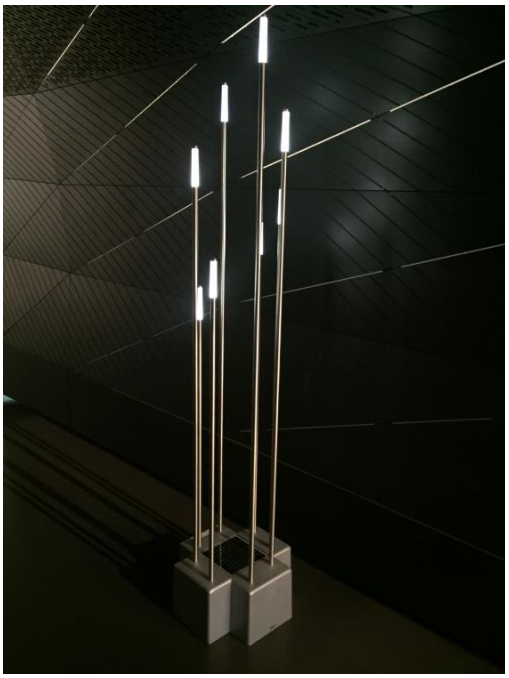

Fig. 6. LIGHT-TUBE

VI. Summary

3 major challenges in the development of L2L products is the lack of efficient converter electronics, modelling tools for dimensioning and furthermore, characterization facilities to support the successful development of the products. Above we report the development of 2 Three-Port-Converters respectively for 1-10Wp and 10-50 Wp PV panels with a peak efficiency of 97% at 1.8 W of PV power for the 10 Wp version. Furthermore, a modelling tool for L2L products has been descriped and a laboratory for feeding in component data not available in the datasheets to the model is proposed.

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F

A Three-Port Topology Comparison for a Low Power Stand-Alone Photovoltaic System

2014 IEEE International Power Electronics Conference (IPEC 2014 ECCE–ASIA)

A Three-Port Topology Comparison for a Low Power Stand-Alone Photovoltaic System

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***Abstract*—Three-port converter (TPC) topologies for renewable energy systems aim to provide higher efficiency and power density than conventional cascaded structures. This work proposes an analytical comparison of different TPC topologies for a photovoltaic LED lamp stand-alone system. A comparison using component stress factor (CSF) is performed, which gives a quantitative measure of the performance of the converter. The candidate topologies are compared to each other according to a defined LED lighting strategy and a solar irradiation profile.**

Keywords— Photovoltaic, three port converter, stand-alone, component stress factor.

I. INTRODUCTION

Due to fossil fuel reserves depletion together with climate concerns, in the last decades renewable energies have become an important part of energy production. Switched-mode power supplies (SMPS) play an important role in the integration of renewable energies due to the requirement of high efficiency conversion.

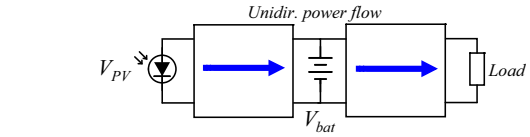
Solar energy is one of the fastest growing renewable energy sources mainly because sunlight is the most abundant source of energy and is unlimited, clean and free. The major advantage of renewable energy sources, like solar or wind, is the transformation of energy with zero carbon dioxide (CO_2) emissions. However, the main drawback is that the energy source is intermittent in nature since it strongly depends on the weather conditions. In order to overcome this limitation, multiple energy sources are combined to provide a constant power source.

Multi-input converters (MIC) topologies address the issue of interconnecting several energy sources with a single power converter [1]. The common characteristic of MIC is the shared output stage, so the number of components is reduced and the power density is increased. Some MIC make use of magnetic coupling (multiple transformer windings) and present solutions based on flux additivity [2], [3], phase-shifted operation [4], distributed transformers [5] or a four quadrant magnetic structure [6] which allows the two input power stages to deliver power simultaneously. Feasible and unfeasible non-isolated MIC topologies are presented in [7] and a systematic approach to synthesize MIC based on the concept of pulsating voltage source cell (PVSC) and pulsating current source cell (PCSC) is proposed in [8] and [9].

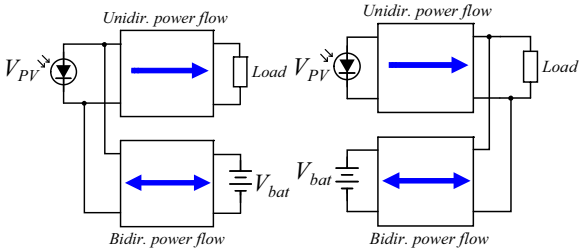
When a storage element is included in a MIC, a stand-alone system is formed. A stand-alone structure is very interesting for powering up systems at remote locations, where cabling is challenging and expensive. It is also of interest in urban areas where not only the cost of cabling but also digging and construction is extremely costly.

The aim of this work is to analyze TPC topologies suitable for low power stand-alone photovoltaic systems and to compare them to conventional cascaded converters. In this type of application, a bidirectional port with a storage element is necessary. The battery will store the excess energy in light or no load conditions and provide energy in case of no input power.

The conventional approach to implement multi-input power systems is to interconnect the elements using different cascaded power converters [10] [11], or parallel [12] as shown in Fig. 1. However, the main disadvantage is the low efficiency of the system due to the power processed in multiple conversion stages. The proposed solution is to implement a multiport converter, which can interface with renewable energies, storage elements and loads simultaneously, as the TPC shown in Fig. 2. Authors claim that the advantage of this method is higher efficiency due to reduced conversion stages and compact packaging [13], [14], [15], [16].



a) Cascade connection



b) Parallel input c) Parallel output

Fig. 1 Conventional integration method of a multi-input port stand-alone photovoltaic system

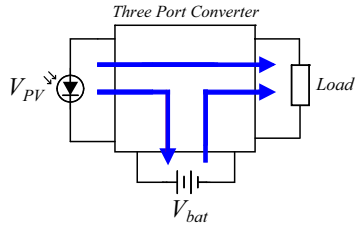


Fig. 2 Three-port stand-alone photovoltaic system

Three different power flows can take place in the system depending on the solar energy and load consumption. The converter will operate in dual input (DI) mode when the load power is higher than the available PV power, so the battery has to deliver the extra required energy. The converter will operate in dual output (DO) mode when the PV power is higher than the load power and the battery has to store the excess energy. During night time, the system will operate in single input single output (SISO) mode delivering power from the battery to the LEDs.

II. System Specifications

The stand-alone system under analysis is a photovoltaic LED lamp system with a lithium battery for energy storage. The photovoltaic panel is composed of two paralleled connected monocristaline panels with the specifications shown in Table I. Fig. 3 shows the I-V curve of the PV panel. The maximum power point (MPP) is located at the knee of the curve given by the points V_{mp} and I_{mp}. Equation (1) describes the output current of a photovoltaic cell. The integrated battery is a $LiFePO_4$ (lithium iron phosphate) battery GWL Power WINA with a nominal voltage of $3.2\,V$ and a capacity of $15\,Ah$. The LED lamp is composed of eight series-connected Cree XLamp XP-E with a maximum current of $1\,A$ and a forward voltage drop of $[2.6-3.3]\,V$. Fig 4 shows the LED lamp I-V curve extracted from the component datasheet.

$$I = I_{ph} - I_o\left(e^{\frac{V+I\cdot R_s}{V_t}} - 1\right) \qquad (1)$$

I_{ph}: photogenerated current (A)
I_o: diode's dark saturation current (A)
R_s: series resistance (Ω)
V_t: cell's equivalent thermal voltage. $V_t = AkT/q$ (V)
A: diode ideality factor
k: Boltzmann's constant ($1.380 \cdot 10^{-23}\mathrm{JK}^{-1}$)
q: charge of an electron ($1.602 \cdot 10^{-19}C$)
T: p-n junction temperature (K)

TABLE I
PV Panel Specifications @ STC

P_{mp}	8.32 W
V_{mp}	5.4 V
I_{mp}	1.54 A
V_{oc}	6.48 V
I_{sc}	1.65 A

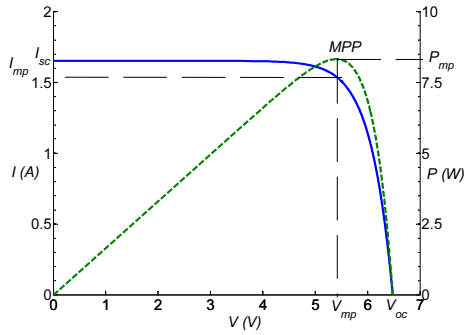


Fig. 3 I-V and P-V characteristic curve of the photovoltaic panel, continuous blue and dotted green line, respectively

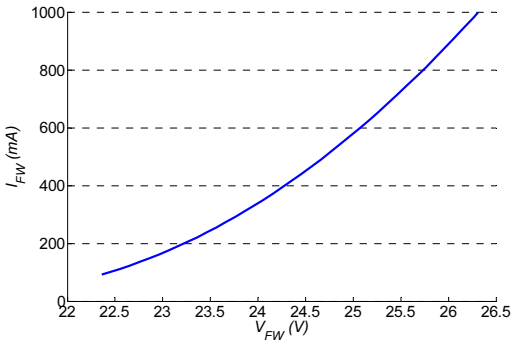


Fig. 4 LED lamp I-V curve (8 series connected LED Cree XLamp XP-E)

III. Topology Selection

TPC topologies are based on reduced energy processing and shared components to achieve a high efficiency and power density. However, it is often required to add extra switches to provide controllability and/or diodes to configure the power flow path. Therefore, TPC topologies usually need a high number of semiconductors [13], [16], [17].

The conventional cascaded structure chosen as the reference design is a buck and a tapped boost converter connected in series as shown in Fig. 5. In order to drive the LED port, a high step-up ratio is needed from both inputs – battery and PV source. The tapped boost converter provides the required step-up ratio with low amount of components. This topology is selected because it achieves high transformation ratio and makes good use of the coupled inductors, since both windings are active during the discharge. Fig. 6 shows the operating waveforms of the tapped boost converter. The dc voltage transfer functions are obtained from the inductor volt-second balance as shown in (2) for the buck converter and (3) and (4) for to the tapped boost topology.

$$V_{bat} = V_{PV} D_1 \qquad (2)$$

$$V_{bat} \cdot D_2 T + \left(\frac{V_{bat} - V_{LED}}{n+1}\right) \cdot (1 - D_2) T = 0 \qquad (3)$$

$$V_{LED} = V_{bat}\left(1 + \frac{(n+1)\cdot D_2}{(1-D_2)}\right) \qquad (4)$$

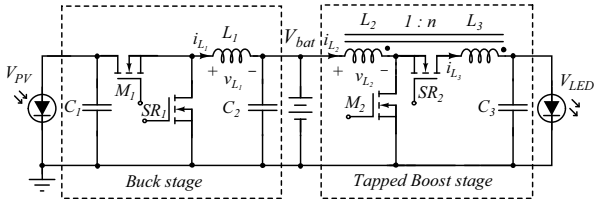


Fig. 5 Conventional cascaded solution. Buck and tapped boost converters series-connected .

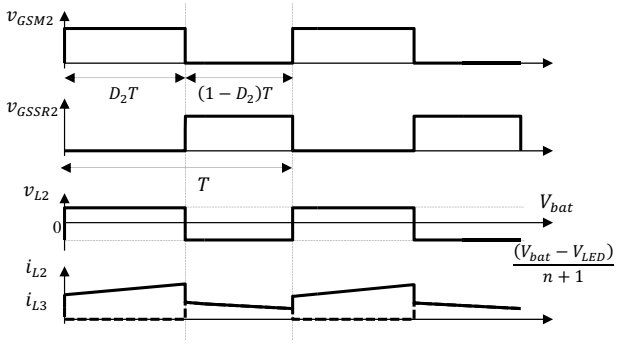


Fig. 6 Tapped boost converter operating waveforms. From top to bottom: Gate source voltage of switches M_2 and SR_2, inductor L_2 voltage and inductor L_2 and L_3 current, continuous and dotted line, respectively

The TPC structures considered have been selected according to the number of components. In order to avoid voltage drops in the power flow path, diodes have been replaced with MOSFETs. However, this solution makes it difficult to drive these components since they are usually not referenced to ground. Moreover, in some topologies these MOSFETs need to be active during the whole period. This complicates the drive circuitry even more since gate drive transformers cannot be used.

Two TPC topologies are analyzed. The first is a non-isolated TPC (NI-TPC). NI-TPC topologies can be derived from dual input converters (DIC) or dual output converters (DOC) as proposed in [16]. The key idea of deriving TPC topologies based on DIC or DOC is to combine power flows with similar characteristics. In a DIC, both the source and the battery can deliver power to the load. For the given specifications, both power flows need to boost the voltage and therefore, can be combined. Hence, a DIC is formed by combining two power flows with similar characteristics. An additional power flow to interconnect the main source and the battery is needed. A buck converter is added to cover the third power flow and therefore a TPC is derived from a DIC topology [16], [14].

The NI-TPC synthesized by combining DI and SISO converters is shown in Fig. 7. This structure is similar to the cascaded conventional buck and tapped boost solution found in SISO mode. In DO mode, it performs like two separate converters. Switch M_3 is always active and switch M_4 is always off. Therefore, there are two direct paths: from PV-LED and PV-battery with a tapped boost and a buck converter respectively.

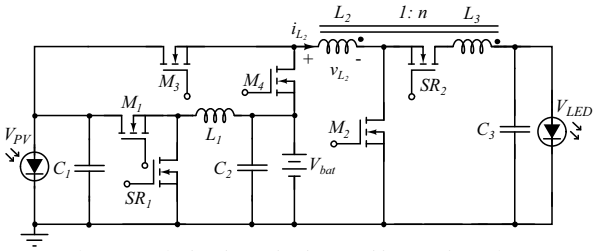


Fig. 7 Non-isolated TPC buck-tapped boost schematic

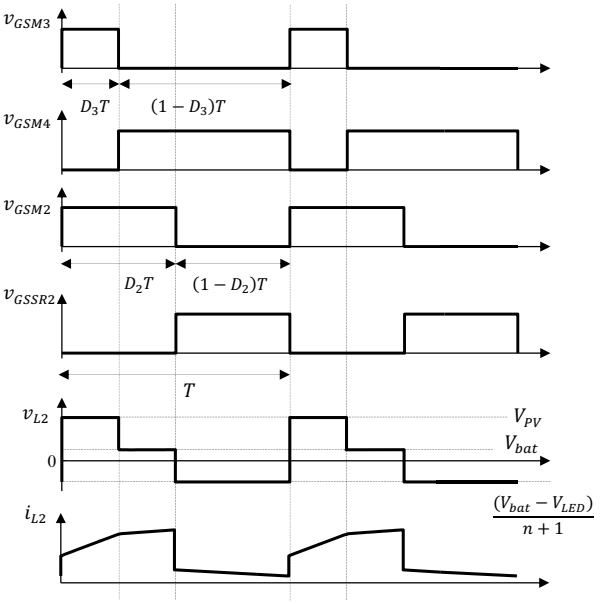


Fig. 8 Non-isolated TPC buck and tapped boost operating waveforms in DI mode. From top to bottom: Gate source voltage of switches M_3, M_4, and M_2, SR_2, inductor L_2 voltage and inductor L_2 current

In DI mode, both the PV panel and the battery are providing energy to the load. The NI-TPC behaves as a single tapped boost converter. The inductor charge time is adjusted with switches M_3 and M_4, which control the power flow from each of the power sources. The NI-TPC operating waveforms in DI mode are shown in Fig. 8. The dc voltage transfer function in DI mode can be calculated by applying the volt-second balance on the inductor L_2 as shown in (5) and (6).

$$V_{PV}D_3 + V_{bat}(D_2 - D_3) + \frac{V_{bat} - V_{LED}}{n+1}(1 - D_2) = 0 \qquad (5)$$

$$V_{LED} = \frac{(n+1)V_{PV}D_3 + V_{bat}\big(n(D_2 - D_3) + (1 - D_3)\big)}{(1 - D_2)} \qquad (6)$$

The second topology considered is a half-bridge three-port converter (HB-TPC) [15] [18] as shown in Fig. 9. The full-bridge version (FB-TPC) has also been proposed in literature [19]. However, in this application the HB-TPC is selected because it has a lower number of components. The half-bridge transformer allows for an isolated output port while providing step up/down transformation. In this topology, the magnetizing inductance of the transformer is used as the inductor of the buck converter linking the PV panel with the battery. The HB-TPC operating waveforms in DI mode are shown in Fig. 10.

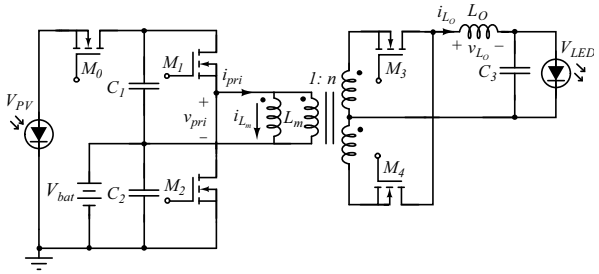


Fig. 9 Half-bridge three-port converter HB-TPC

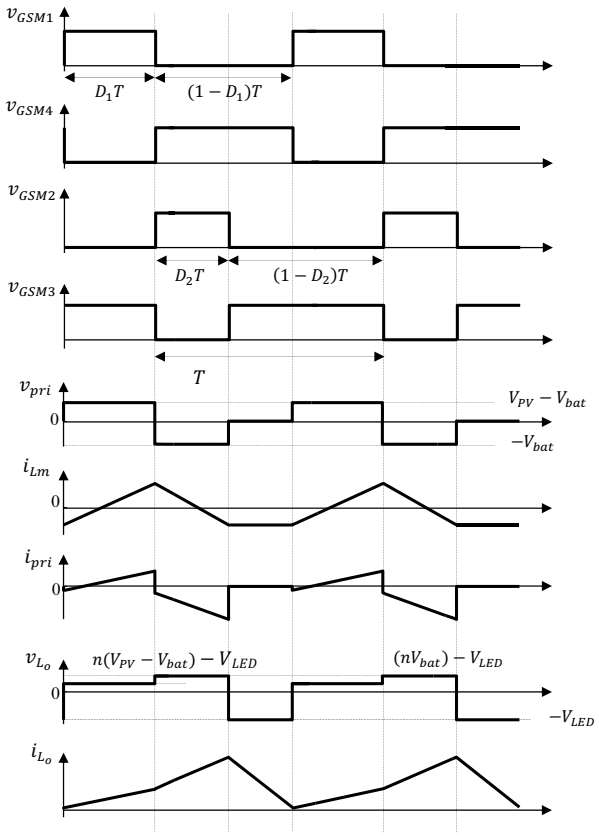


Fig. 10 HB-TPC converter operating waveforms in DI mode. From top to bottom: Gate source voltage of switches M_1, M_4, M_2 and M_3, transformer primary voltage v_{pri}, magnetizing inductor current i_{Lm}, transformer primary current i_{pri}, output inductor voltage v_{L_o} and output inductor current i_{L_o}

Switch M_0 is used to prevent reverse current from flowing to the PV panel and it is active when there is power flow from the PV panel. Switches M_1 and M_4 are driven in complementary mode, like M_2 and M_3. During M_1 conduction time, switch M_3 is also active and the energy from the PV panel is transferred to both the battery and the output port. When switch M_2 is active, rectifier M_3 is also active and the energy from the battery is moved to the output. When the rectifier switches M_3 and M_4 are on, the primary winding is clamped to zero and both the magnetizing and the output inductor are freewheeling.

Two PWM signals are necessary to control the power flow from both the inputs – PV panel and battery – to the load. The dc voltage transfer functions to regulate the power flow form the PV to the battery and from the battery to the LED are obtained by applying the volt-second balance on the transformer magnetizing inductor and output inductor as presented in (7) and (8).

$$V_{bat} = \frac{V_{PV} D_1}{D_1 + D_2} \tag{7}$$

$$V_{LED} = n[D_1(V_{PV} - V_{bat}) + D_2 V_{bat}] = 2nD_2 V_{bat} \tag{8}$$

In DO mode, the converter operating waveforms are the same as in DI mode except that the average value of the primary and the magnetizing inductance current is positive.

In SISO battery-to-load mode, the converter operates in a forward flyback mode. Switches M_1 and M_2 are driven in complementary mode and M_3 and M_4 are the synchronous rectifiers. When M_2 and M_4 are active, the converter operates in a forward mode. When M_1 and M_3 are on, the converter operates in a flyback mode in order to demagnetize the primary winding. The dc voltage transfer function for this operating mode is shown in (9).

$$V_{LED} = V_{bat} \cdot 2n(1 - D) \tag{9}$$

The main disadvantage of this topology is that under low power conditions at the LED port, there will be a long period where the magnetizing current (or buck inductor current) will be circulating through the transformer secondary windings and synchronous rectifiers, reducing the efficiency of the converter significantly. Moreover, in order to operate in SISO mode from the PV panel to the battery, an extra switch in the return path of the transformer's secondary windings needs to be added so the primary side can be operated as a buck converter.

From the three topologies presented, the conventional cascade solution has the lowest number of semiconductors, followed by the HB-TPC. The topology with highest number of semiconductors is the NI-TPC.

IV. Component Stress Factor Analysis

To perform a topology comparison, a component stress factor (CSF) is performed [20]. This analysis provides an estimation of the converter stress distribution in the different components. The motivation for using CSF is that it gives a quantitative measure of converter performance. A similar approach called component load factor (CLF) was introduced in [21] and used by [22] to compare single-stage and two-stage PFC solutions. The difference between CLF and CSF is how the individual and total component factors are calculated. In the CSF analysis, in order to make a fair comparison, the same amount of silicon, magnetic winding area and capacitor volume for the components in all the candidate topologies is required. The distribution of resources between the different elements is done according to the specific weighting factor assigned to each component.

Three different CSFs are calculated: semiconductor component stress factor (SCSF), winding component stress factor (WCSF) and capacitor component stress factor (CCSF). The stress in a component will depend on the maximum applied voltage and the maximum current.

CSF gives an estimation of the converter's efficiency because it can be correlated to the conduction losses. In a MOSFET the conduction losses are given by the rms current and the MOSFET's on resistance. SCSF is calculated according to the MOSFET's squared maximum voltage and the rms current as shown in (10). Moreover, it is scaled to the processed power, which normalizes the CSF and makes it a dimensionless quantity. WCSF is calculated according to (11). The maximum voltage is defined by (12), which is calculated as the average voltage applied to the inductor winding over a period. CCSF is calculated using the peak voltage of the capacitor and the rms current as shown in (13).

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{{V_{DS}}^2 \cdot {I_{rms}}^2}{P^2} \quad (10)$$

$$WCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{{V_{max}}^2 \cdot {I_{rms}}^2}{P^2} \quad (11)$$

$$V_{max} = \sum_i D_i \cdot |V_i| \quad (12)$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{{V_{pk}}^2 \cdot {I_{rms}}^2}{P^2} \quad (13)$$

From (10) to (13) $\frac{\sum_j W_j}{W_i}$ is the weighting factor, which is applied to every component. $\sum_j W_j$ is the sum of the individual weights for the components of the same type in the circuit and W_i is the weight assigned to component i. The weighting factor represents the amount of resources given to a component. In the first CSF iteration, the same component weight is usually given for all the components. Once the components with higher CSF are identified, the weighting factor can be adjusted by giving higher amount of resources to that specific component in order to achieve lower CSF.

After calculating a CSF for each component, the sum of component factors of the same type is performed as shown in (14), (15) and (16).

$$SCSF = \sum_{Semiconductors} SCSF_i \quad (14)$$

$$WCSF = \sum_{Windings} WCSF_i \quad (15)$$

$$CCSF = \sum_{Capacitors} CCSF_i \quad (16)$$

The CSF gives a numerical comparison between components within power converter topologies. This quantitative measure is related to the performance of the converter since component stress can be translated into cost, size and efficiency.

To simplify the calculations, it is assumed that the power losses are neglected ($P_{in} = P_{out}$). It is also assumed that inductors are infinitely large, meaning that the current ripple is null.

A MATLAB program is developed in order to calculate the CSF of the selected topologies for the different operating modes: DI, DO, SISO from the PV panel to the battery and SISO from the battery to the LED port. The calculated rms currents and voltages have been verified with closed loop control simulations in a SPICE-based software.

The CSF is calculated with the same component weight for all the components inside each of the topologies. The resources to be assigned are selected as one unit ($\sum_j W_j = 1$) and distributed equally between the components of the same type.

In order to observe how the stress on the semiconductors moves depending on the power flow, the PV panel is swept from minimum to maximum power. The output power in the LED port is kept at a constant $2.5\,W$. The selected number of turns of the coupled inductors for the cascade solution and the NI-TPC is $n = 5$, which is the value that gives the lower SCSF in SISO mode. The transformer turn ratio in the HB-TPC is chosen as $1:11$, which is the minimum value required to operate in SISO mode from the battery to the LED. Fig. 11 shows the semiconductor CSF of each of the candidate topologies operating in DI and DO mode. From 0 to 2.5 W the converters operate in DI mode. In this mode, the LED power is higher than the available PV power, so the battery is providing the extra energy. When the PV power is higher than the LED power, the converters operate in DO mode and the energy surplus is stored in the battery. It should be noticed that the CSF is normalized to the processed power. Hence, operating in DI mode the power processed is the output power. On the other hand, when operating in DO mode the total power processed corresponds to the converter input power. It can be observed that for the cascaded solution and the NI-TPC, the higher stress appears on the tapped boost components. Specifically the synchronous rectifier SR_2 has to withstand a large voltage stress. Comparing the cascaded solution to the NI-TPC, it can be seen that the NI-TPC SCSF is degraded due to the increased number of MOSFETs and the fact that the turn ratio of the coupled inductors must be selected according to the stress on both PV-to-LED and battery-to-LED power flows.

When the cascaded converters operate in DI mode, it can be seen that the CSF increases as the power increases since the power must be processed twice. However, even when the power is processed twice, the SCSF is smaller than in the NI-TPC solution. It is interesting to note that

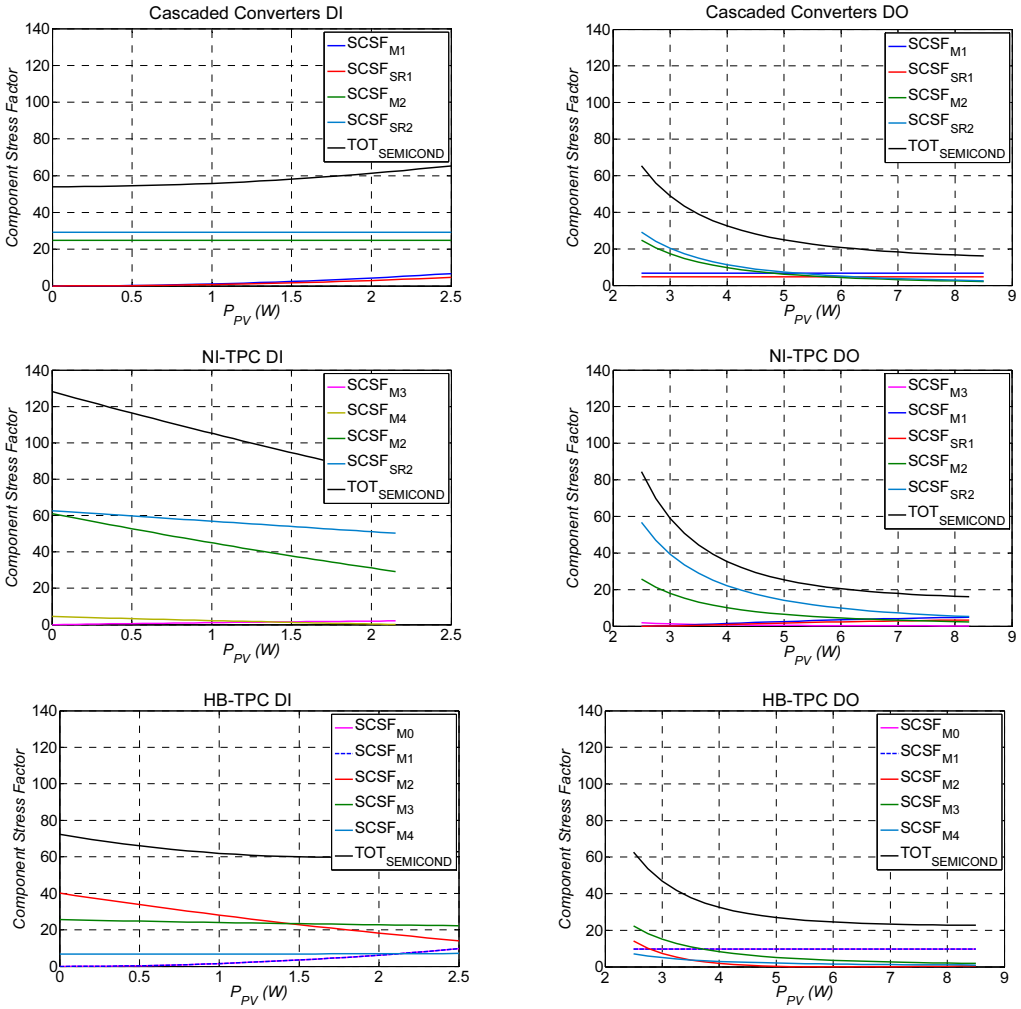


Fig. 11 Semiconductors CSF of the converters operating in DI mode (left column) and DO mode (right column)

for the NI-TPC operating in DI mode, the PV panel can never deliver the full power directly to the LED since the discharge of the inductor is always done through the battery power flow. In the HB-TPC structure, the higher stress in DI mode appears in the switch M_2 and synchronous rectifier M_3. This stress is reduced as the power flow from the panel to the LED increases and moves to the switch M_1 and synchronous rectifier M_4. For all the topologies operating in DO mode, the SCSF decreases as the power flow from the panel to the battery increases since all this power flow is processed by the buck structure.

Depending on the converter operating conditions, LED lighting strategy and the amount of available solar irradiance, the power flows in the system will vary together with the operating voltages, duty cycles and consequently, current and voltage stresses. In such a system, it is important to perform a comparison between the considered topologies for all the possible conditions. This can be done by analyzing the CSF based on real field solar irradiance measurements that will provide a pattern of the PV panel operating voltage and available power. An irradiance measurement performed over a day [23] is taken as a reference. From the irradiance value, the maximum available power can be obtained using (1). Two different LED lighting patterns are defined in order to compare the CSF analysis for different applications. Fig. 12 shows the maximum available power from the PV panel together with two LED illumination patterns for a period of 24 hours.

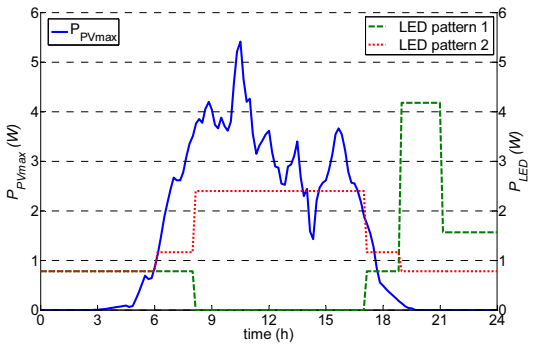


Fig. 12 Maximum PV panel power (blue), LED pattern 1 (green) and LED pattern 2 (red) for a 24 hours period

The two illumination patterns are defined in order to compare the selected topologies under different operating conditions. The LED pattern 1 (green line) can be used for an application where no light is necessary during the day, like in a garden lighting system. The LED pattern 2 (red line) is defined for an application where the LED power is mostly used during the day, like in a signaling light. In the LED pattern 1, the converter works mostly in SISO PV-to-battery during the day and in SISO battery-to-LED during the night, except for short periods where it operates in DI and DO mode. In the LED pattern 2 the converters never operate in SISO PV-to-battery and work in DI and DO modes.

The CSF at each operating condition is weighted in respect to the maximum processed power and averaged over the whole operating period in order to extract a CSF value that directly relates to the amount of energy lost during the evaluated time. Table II and Table III show the calculated CSF for the cascaded solution and the analyzed TPC topologies for the two lighting pattern. The turn ratio of the tapped boost converter in both the cascaded and the NI-TPC solution is selected to obtain the lowest total CSF. The transformation ratio of the HB-TPC is the minimum value in order to operate in SISO battery-to-LED mode, which also gives the lowest SCSF.

According to the results, it can be seen that the cascaded solution provides the lowest CSF, even when taking into account that the PV power is processed twice. This is due to the fact that the TPC topologies need extra switching elements to control the power flows, which has a negative impact on the amount of available resources for the design of the converter. Further analysis can be carried out by adjusting the different component weights to find an optimal solution for each of the analyzed topologies.

When an irradiance measurement performed over a year (Fig. 13) is used, a different CSF weighting factor can be calculated depending on whether the converter has to be optimized for minimum annual energy loss or for maximum efficiency under low irradiance conditions.

TABLE II
CSF – LED PATTERN 1

$Topology$	$SCSF$	$WCSF$	$CCSF$
$Cascaded \quad (n = 5)$	10.92	1.76	0.98
$NI - TPC \quad (n = 5)$	17.05	1.64	0.84
$HB - TPC \quad (n = 11)$	18.25	3.51	1.17

TABLE III
CSF – LED PATTERN 2

$Topology$	$SCSF$	$WCSF$	$CCSF$
$Cascaded \quad (n = 5)$	14.11	2.27	1.66
$NI - TPC \quad (n = 3)$	16.75	1.55	0.82
$HB - TPC \quad (n = 11)$	18.99	2.63	0.80

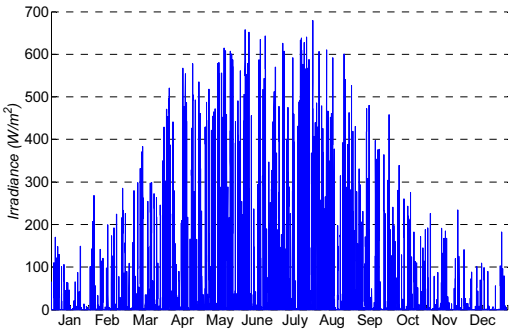


Fig. 13. Annual solar irradiation pattern

V. CONCLUSION

This paper presents a comparison of TPC topologies for a low power PV-battery-LED stand-alone system. The comparison is performed using CSF analysis based on a solar irradiance pattern measurement and a defined LED lighting strategy. The proposed method allows performing a direct comparison of different topologies for a specific application. Two different suitable TPC topologies are compared to a conventional cascaded solution. This is done to evaluate whether having a third power flow improves the system efficiency by reducing the amount of times the power is processed. The results of the CSF analysis employed shows that the cascaded structure provides the best results under the considered lightning patterns. Observing the results of the SCSF , for the first LED lighting pattern considered, the cascaded topology presents a improvement of 35.9% over the NI-TPC topology and a 40.16% over the HB-TPC topology. For the second LED pattern considered, the improvement of the cascaded topology is lower: 15.7% and 25.7% over the NI-TPC and HB-TPC, respectively.

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G

A Three-Port Direct Current Converter

Patent Application – DTU-95727/P3806EP00

A three-port direct current converter

Field of invention

The invention relates to a three-port direct current converter, operating in two mutually exclusive power flow configurations, sharing a magnetic component.

Background of invention

Solar energy is one of the fastest growing renewable energy sources mainly because sunlight is the most abundant source of energy and is unlimited, clean and free. The major advantage of solar energy is the transformation of energy with zero carbon dioxide (CO2) emissions. However, the main drawback is that the energy source is intermittent in nature since it strongly depends on the weather conditions. In order to overcome this limitation, energy storage elements are often required in order to provide a constant power source.

Multi-input converters (MIC) topologies address the issue of interconnecting several energy sources with a single power converter. The conventional approach to implement multi-input power systems is to interconnect the elements using different series or parallel connected power converters. However, the disadvantages are low power density and efficiency due to multiple conversions stages. The solution is to implement a multiport converter, which can interface with renewable energy sources, storage elements and loads.

Recently introduced three-port converter (TPC) topologies are based on reduced energy processing and shared components and claim to achieve high efficiency and power density. TPCs can be said to have fewer conversion stages and generally higher efficiency compared to solutions employing several independent two-port converters. However, in TPCs it is required to add extra switches to provide controllability and/or diodes to configure the power flow paths. TPC topologies need a high number of semiconductors.

Fig. 1 shows the concept of a conventional three-port converter. The three-port converter has an input voltage port, a battery port, and a load, to which power is delivered.

Summary of invention

The present disclosure relates to a topology for a three-port direct current converter, in which a single magnetic component is shared by a primary side circuit and a secondary side circuit, by having the three-port direct current converter configured to operate in two mutually exclusive power flow configurations. Therefore, the invention relates to a three-port direct current converter comprising: at least one input direct current source; at least one storage battery; a primary side circuit; a secondary side circuit; a single magnetic component shared by the primary side circuit and the secondary side circuit, wherein the primary side circuit comprises a connection between the at least one input direct current source and the at least one storage battery, the primary side circuit configured for operating as a buck converter, wherein the secondary side circuit comprises a connection between the at least one storage battery and at least one load, the secondary side configured for operating as a boost converter, and wherein the three-port direct current converter is configured to operate in two mutually exclusive power flow configurations.

The inventor has realized that in particular in street light applications, wherein the input power source is solar energy, there is room for optimization of the conventional three-port converter topologies. When there is daylight, there is no need for the street light to be active, and therefore the three-port converter can operate as a buck converter, wherein the power input charges the battery. The street light becomes active when there is no daylight, and in this power configuration the three-port converter operates as a boost converter, driving the load. These two modes can share a number of components. Compared to a conventional three-port converter, this means that there is no direct power flow from the power input to the load. In the converter proposed in the present invention, the single magnetic component may regulate a first output voltage of the primary side circuit in the first power flow configuration, and regulate a second output voltage of the secondary side circuit in the second power flow configuration. The three-port converter operating with a single magnetic component can be seen as a significant benefit compared to conventional three-port converters since magnetic components play an important role for the size, price and weight of the converter.

A further aspect of the presently disclosed invention relates to the three-port direct current converter configured to operate without diodes. The inventor has realized that if the three-port direct current converter operates with actively controlled switching

elements, such as MOSFETs, configured to control power flows of three-port direct current converter, further advantages can be obtained. This technique is referred to as synchronous rectification or active rectification and reduces power drops in the power flow paths. The drawback of this technique is that typically extra gate control signals are needed for controlling the MOSFETs. In one embodiment of the present inventions all the switches are active switches in order to reduce voltage drops in the power flow path, where M5 and M4 are power flow path configuration switches, M2 acts as synchronous rectifier in buck mode and M3 operates as synchronous rectifier in boost/tapped boost mode. By combining the topology of the present invention, in which a single magnetic component is shared by a primary side circuit and a secondary side circuit, and synchronous rectification, a further optimized converter can be obtained, in which one MOSFET M_2 is shared between the primary side circuit and the secondary side circuit. Furthermore, with the proposed converter two of the MOSFETs are simple to drive since they only operate in two configurations (on/off) depending on which of the two mutually exclusive power flow configurations that is active. In summary this means that in one embodiment of the present invention, there are five MOSFETs, wherein one (M_2) is shared between the primary side circuit and the secondary side circuit, and wherein two of the other MOSFETs do not have to be dynamically driven (on/off depending on power flow configuration). Fig. 3 shows this embodiment.

Description of drawings

The invention will in the following be described in greater detail with reference to the accompanying drawings. The drawings are exemplary and are intended to illustrate some of the features of the presently disclosed three-port direct current converter, and are not to be construed as limiting to the presently disclosed invention.

Fig. 1 shows a conventional three-port converter having an input power source, a battery and a load.

Fig. 2 is a conceptual drawing of a three-port converter according to the present invention having an input power source, a battery and a load, wherein the three-port direct current converter is configured to operate in two mutually exclusive power flow configurations.

Fig. 3a shows an embodiment of a three-port converter according to the present invention, wherein a single magnetic component (L) is shared by the primary side circuit and the secondary side circuit.

Fig. 3b shows the three-port converter in fig. 3a, wherein the primary side circuit, configured for operating as a buck converter, is highlighted.

Fig. 3c shows the three-port converter in fig. 3a, wherein the secondary side circuit, configured for operating as a boost converter, is highlighted.

Fig. 4a shows an embodiment of a three-port converter according to the present invention, wherein a magnetic component (L_{1A}) is shared by the primary side circuit and the secondary side circuit. In this embodiment there is a second optional magnetic component (L_{1B}) serially coupled to the first inductor to perform a voltage step-up of the second output voltage.

Fig. 4b shows the three-port converter in fig. 4a, wherein the primary side circuit, configured for operating as a buck converter, is highlighted.

Fig. 4c shows the three-port converter in fig. 4a, wherein the secondary side circuit, configured for operating as a tapped boost converter, is highlighted. In this embodiment there is a second optional magnetic component (L_{1B}) serially coupled to the first inductor to perform a voltage step-up of the second output voltage.

Fig. 5 shows a three-port converter according to the present invention operating as a buck converter.

Fig. 6 shows a three-port converter according to the present invention operating as a boost converter.

Fig. 7 shows a three-port converter according to the present invention operating as a tapped-boost converter.

Detailed description of the invention

The present disclosure relates to a topology for a three-port direct current converter, in which a single magnetic component is shared by a primary side circuit and a secondary side circuit, by having the three-port direct current converter configured to operate in two mutually exclusive power flow configurations. Therefore, the invention relates to a three-port direct current converter comprising: at least one input direct current source; at least one storage battery; a primary side circuit; a secondary side circuit; a single magnetic component shared by the primary side circuit and the secondary side circuit, wherein the primary side circuit comprises a connection between the at least one input direct current source and the at least one storage battery, the primary side circuit configured for operating as a buck converter, wherein the secondary side circuit comprises a connection between the at least one storage battery and at least one load, the secondary side configured for operating as a boost converter, and wherein the

three-port direct current converter is configured to operate in two mutually exclusive power flow configurations.

The proposed topology is a combination of two converters in a single magnetic component multi-port converter with at least one power input, at least one power output and at least one bidirectional power port. The proposed converter is based on the concept of shared components in order to increase the power density. Magnetic components play an important role in power density, weight and price. The topology uses a single magnetic component (L), which is shared between two mutually exclusive operating modes. The three-port direct current converter may operate as a buck converter charging the at least one storage battery in a first power flow configuration, and operate as a boost converter driving the at least one load in a second power flow configuration. The two mutually exclusive operating modes are 1) the circuit operating as a buck converter, wherein the input direct current source charges the at least one storage battery, and 2) the circuit operates as a boost converter, wherein the storage battery powers the at least one load. The possibility to share one single magnetic component can be seen as a result of realizing that if there is no direct power flow from the power input to the load, two mutually exclusive power flow configuration can be achieved, and by designing the voltage regulating parts, including a magnetic portion, a design can be achieved in which a single magnetic component can be shared between the two circuits (first and secondary). The inventor has realized that such a designed is suitable for light-to-light solutions, i.e. wherein the input power source is solar energy and the power output is a light, for example a street light. In principle, when there is daylight there is no need for the street light, and when there is no daylight it is not possible to charge the storage battery. These two cases may translate into the two mutually exclusive power flow configurations, and therefore the presently disclosed invention may be suitable for light-to-light solutions. Compared to a convention three-port converter, the presently disclosed invention can be seen as significant benefit since it is capable of operating with one single magnetic component. This is beneficial for the size, price and weight of the converter.

In one embodiment of the present invention the magnetic component is a first inductor. The conceptual model of a buck converter is best understood in terms of the relation between current and voltage of the inductor. Beginning with the switch open (in the "off" position), the current in the circuit is 0. When the switch is first closed, the current will begin to increase, and the inductor (L in the fig. 3b example) will produce an

opposing voltage across its terminals in response to the changing current. This voltage drop counteracts the voltage of the source and therefore reduces the net voltage across the load. For the present invention this means that the role of the magnetic component can be seen as regulating a first output voltage of the primary side circuit in the first power flow configuration. The first output voltage corresponds to the voltage of the at least one storage battery. The first output voltage may therefore be regulated to match a predefined voltage range of the at least one storage battery. The primary side circuit can also be said to operate as a voltage step down and current step up converter in a first power flow configuration.

The conceptual model of a boost converter can also be understood in terms of the relation between current and voltage of an inductor. In a boost converter, the output voltage is higher than the input voltage. In a boost converter, there is one state in which the current flows through the load and the inductor stores some energy by generating a magnetic field. In a second state, a switch is typically opened which increases the impedance, reduces the current, and, as a consequence, causes a higher voltage to charge the capacitor (C3 in the fig. 3c example). When the switch is then closed the capacitor is able to provide the voltage and energy to the load. For the present invention this means that the role of the magnetic component can be seen as regulating a second output voltage of the secondary side circuit in the second power flow configuration. Optionally, the magnetic component can be said to regulating a second output voltage by using an additional capacitor. The second output voltage may therefore be regulated to match a predefined voltage range of the at least one load.

A further aspect of the presently disclosed invention relates to the secondary side circuit optionally comprising a second inductor serially coupled to the first inductor, wherein the first and second inductors are configured to perform a voltage step-up of the second output voltage. In this mode the topology operates as a tapped-boost converter, which provides high step-up ratio from the battery port. An example of such a topology can be found in fig. 4a-c, wherein the component L_{1B} is the second inductor. If the specification at the load of the secondary side circuit requires high step-up voltage; the output voltage can then be adjusted with the turns ratio between the two inductors, depending on the required output voltage.

In one embodiment, the at least one input direct current source comprises a photovoltaic panel. As stated above that the present invention is suitable for light-to-

light solutions, i.e. wherein the input power source is solar energy. Therefore, in one embodiment the at least one input direct current source comprises a photovoltaic panel (solar panel). In principle, the topology also works for any other direct input source. Also relating to light-to-light solutions, one embodiment of the invention relates to the at least one load comprises at least one light source, including any electronically powered light sources, such as light-emitting diodes.

When designing a three-port converter, weather conditions, battery performance and load requirements have to be taken into consideration. In the example of a light-to-light solution the following factors are examples of factors that have to be taken into account: For how long will the battery have to power the light (i.e. how many dark hours during a 24 hour day)? What are the weather (sun) conditions? What is the input power during a day worst case? How much power does the load require? How much energy can the battery store? The presently proposed topology is power efficient and therefore eases the design choices in these respects. However, to further improve the system, the inventor has realized that by having a dimmable light source, the requirements on the rest of the system can be reduced. For example, if it has been a cloudy day and the battery has not been fully charged, the light source can be adjusted to use less power and thereby reduce the power consumption for the following night. In one embodiment direct current converter is configured to dim the light-emitting diode according to a state of charge requirement of the at least one storage battery. A further aspect of the present invention relates to the secondary side circuit comprising parallel-connected loads. A further aspect of the present invention relates to the fact that the secondary side circuit may comprise multiple loads. The proposed solution is power efficient and if several loads can be powered by the same storage battery, further efficiency can be achieved. In a further embodiment the multiple loads may be regulated independently. Since the power of the battery is limited it may be useful to implement a solution wherein the loads are regulated such that the optimal use of the resources is achieved with respect to the needs of the different loads.

A further aspect of the presently disclosed invention relates to the three-port direct current converter being configured to operate without diodes. Synchronous rectification, or active rectification, is a technique for improving the efficiency of rectification by replacing diodes with actively controlled switches such as transistors. In low voltage converters, the voltage drop of a diode has an adverse effect on efficiency. Replacing a diode with an actively controlled switching element such as a MOSFET is

the heart of synchronous rectification. MOSFETs have a constant very low resistance when conducting. The voltage drop across the transistor is then much lower, meaning a reduction in power loss and a gain in efficiency. The drawback of this technique is that typically extra gate control signals are needed for controlling the MOSFETs. In one embodiment of the present inventions all the switches are active switches in order to reduce voltage drops in the power flow path, where M5 and M4 are power flow path configuration switches, M2 acts as synchronous rectifier in buck mode and M3 operates as synchronous rectifier in boost/tapped boost mode.By combining the topology of the present invention, in which a single magnetic component is shared by a primary side circuit and a secondary side circuit, and synchronous rectification, a further optimized topology can be obtained, in which one MOSFET M_2 is shared between the primary side circuit and the secondary side circuit. Therefore, a MOSFET M_2 may be shared between the primary side circuit and the secondary side circuit, which also means that it is shared between the two power flow configurations. Figure 3a shows the topology, wherein the primary side circuit and a secondary side circuit share an inductor L and a MOSFET M_2. Figs. 3b and 3c show the circuit being used as a buck converter and a boost converter respectively. This means that both a magnetic component, such as L, and a MOSFET, such as M_2, may be shared between the primary side circuit and a secondary side circuit according to the present invention, wherein L is the only magnetic component of the three-port direct current converter (unless the secondary side circuit is configured to operate as a tapped-boost converter, which means that a second inductor is serially coupled to the first inductor). As previously stated, the shared magnetic component regulates a first output voltage of the primary side circuit in the first power flow configuration, and regulates a second output voltage of the secondary side circuit in the second power flow configuration. In this embodiment M_2 actively controls the current and voltage of the inductor in both power flow configurations.

A further effect of the proposed topology is that the MOSFETs are simpler to drive compared to a conventional three-port converter. As stated, MOSFET M_2 may be shared between the primary side circuit and the secondary side circuit. In one embodiment there are four other MOSFETs M_1, M_3, M_4 and M_5, of which only two (M_1 and M_3) have to be dynamically driven by pulse-width modulators since M_4 and M_5 only have two states (on/off) and never change state in a power flow configuration. Fig. 3 shows this embodiment. During the time the solar energy is not available, MOSFET M_5 is turned off and M_4 is active, so the battery port powers the LED output as shown in

Fig. 3c. When the renewable energy source is available, MOSFET M_5 is active and M_4 is turned off so the converter processes the energy from the photovoltaic panel to the battery side as shown in Fig. 3b. Therefore, M_4 and M_5 do not require pulse-width modulators.

In one embodiment of the present invention, the three-port direct current converter comprises a MOSFET M_1 configured to control the current and voltage of the at least one single magnetic component. The single magnetic component in this embodiment is preferably the inductor L. As previously stated, the shared magnetic component regulates a first output voltage of the primary side circuit in the first power flow configuration. In this embodiment M_1 actively controls the current and voltage of the inductor in the first power flow configuration. In another (or within the same) embodiment, the secondary side circuit comprising a MOSFET M_3 between the first inductor and the at least one load. If the converter is configured to operate as a tapped-boost converter, i.e. having a second inductor serially coupled to the first inductor as showed in fig. 4a, the MOSFET M_3 may be placed between the first inductor L_{1A} and the second inductor L_{1B}. As previously stated, the shared magnetic component regulates a second output voltage of the second side circuit in the second power flow configuration. In this embodiment M_3 actively controls the current and voltage of the inductor in the second power flow configuration.

A further embodiment of the present invention relates to a system, such as a street light, or a path light, or a guiding light, or a garden light or decorative light comprising the three-port direct current converter described above. These are applications that would benefit from a stand-alone off-grid system according to the present invention. Such a system provides flexibility in terms of positioning of the system and eliminates the cost of cables etc. The presently disclosed three-port converter offers improved power density, weight and price in comparison to convention three-port converters. Street light in this context shall be interpreted broadly and includes any kind of street light or lighting, also for indoor purposes or lights placed e.g. directly on the ground, e.g. to light pavements or buildings. Path lights are used to light paths or guide roads or paths in e.g. gardens, parks and urban environment. The system may also be integrated into urban furniture, such as benches, bike racks and the like. The system may also serve as light decoration, and can also be used for indication purposes, for example to indicate security or emergency equipment, such as rescue ladders or emergency doors. Other examples of applications are as indications of runways for

airplanes or mounted on buoys in the sea for orientation purposes. The three-port converter according to the present invention is not limited to lighting applications. The at least one load in the secondary side circuit could be any electrical component that consumes electric power, and the current source in the primary side circuit could be any direct current source.

Examples

Fig. 1 shows a conventional three-port converter having an input power source 1, a battery 3 and a load 2. The design of the three-port converter is complex and requires a large number of electrical components. In the conventional three-port converter there is a direct power flow 4 from the power input to the load.

Fig. 2 is a conceptual drawing of a three-port converter according to the present invention having an input power source 1, a battery 3 and a light-emitting diode 5, which constitutes the load, wherein the three-port direct current converter is configured to operate in two mutually exclusive power flow configurations. This design corresponds to an electrical circuit having a primary side circuit comprising a connection between the at least one input direct current source and the at least one storage battery, the primary side circuit configured for operating as a buck converter, and having a secondary side circuit comprising a connection between the at least one storage battery and at least one load, the secondary side configured for operating as a boost converter, and wherein the three-port direct current converter is configured to operate in two mutually exclusive power flow configuration. A single magnetic component is shared by the primary side circuit and the secondary side circuit. A consequence of the proposed topology is that there is no direct power flow from the power input to the load.

Fig. 3a shows an embodiment of a three-port converter according to the present invention, wherein a single magnetic component (L) is shared by the primary side circuit and the secondary side circuit. In this embodiment there is MOSFET M_5 with one side connected to ground (node n_1). On the other side of M_5 seen from the ground, there is a photovoltaic input power source V_{PV} connected serially to M_5, wherein there is a node n_2 on the other side of V_{PV}. Also connected to n1 are: the battery V_{bat}, a capacitor C_2, wherein the sides of V_{bat} and C_2 (fronting away from the ground) are joined in a node 3. Also connected to n_1 are a MOSFET M_2, defining a node n_4 on the

opposite side of M_2 compared to the ground, and a MOSFET M_4, defining a node n_5 on the opposite side of M_4 compared to the ground. Furthermore there is a capacitor C_1 between n_2 and n_3, an inductor L between n_3 and n_4, and a MOSFET M_1 between n_2 and n_4. There is also a MOSFET M_3 with one end connected to n_4 and one end defining a node n_6. A capacitor C_3 and a light-emitting diode V_{LED} are connected in parallel between nodes n_5 and n_6.

Fig. 3b shows the three-port converter in fig. 3a, wherein the primary side circuit, configured for operating as a buck converter, is highlighted. The components from fig. 3a that are active in this configuration are V_{PV}, M_5, $V_{ba}t$, C_1, M_1, L, M_2 and C_2.

Fig. 3c shows the three-port converter in fig. 3a, wherein the secondary side circuit, configured for operating as a boost converter, is highlighted. The components from fig. 3a that are active in this configuration are V_{LED}, C_3, M_3, M_4, L, M_2 and C_2. Thus, the component that are active both in the primary side circuit and the the secondary side circuit are: L, M_2 and C_2.

Fig. 4a shows an embodiment of a three-port converter according to the present invention, wherein a single magnetic component (L_{1A}) is shared by the primary side circuit and the secondary side circuit. The principle is the same as in fig. 3, but in this embodiment there is a second optional magnetic component (L_{1B}) serially coupled to the first inductor through a node n7 to perform a voltage step-up of the second output voltage. In this embodiment M3 is locate between the nodes n4 and n7, and the second optional magnetic component (L_{1B}) is located between nodes n7 and n6.

Fig. 4b shows the three-port converter in fig. 4a, wherein the primary side circuit, configured for operating as a buck converter, is highlighted.

Fig. 4c shows the three-port converter in fig. 4a, wherein the secondary side circuit, configured for operating as a tapped boost converter, is highlighted. In this embodiment there is a second optional magnetic component (L_{1B}) serially coupled to the first inductor to perform a voltage step-up of the second output voltage.

Fig. 5 shows a three-port converter according to the present invention operating as a buck converter, with ideal operating waveforms. Switch M_5 is constanly on and switch M_4 is constantly off. From top to bottom: Gate-to-source voltage V_{GS} of switches M_1 and

M_2, respectively, drain-to-source voltage V_{DS} of switch M_2, current through switches M_1 and M_2, I_{M1} and I_{M2}, respectively, inductor voltage V_L and inductor current I_L.

Fig. 6 shows a three-port converter according to the present invention operating as a boost converter, with ideal operating waveforms. Switch M_4 is constanly on and switch M_5 is constantly off. From top to bottom: Gate-to-source voltage V_{GS} of switches M_2 and M_3, respectively, drain-to-source voltage V_{DS} of switch M_2, current through switches M_2 and M_3, I_{M2} and I_{M3} respectively, inductor voltage V_L and inductor current I_L.

Fig. 7 shows a three-port converter according to the present invention operating as a tapped-boost converter, with ideal operating waveforms. Switch M_4 is constanly on and switch M_5 is constantly off. From top to bottom: Gate-to-source voltage V_{GS} of switches M_2 and M_3, respectively, drain-to-source voltage V_{DS} of switch M_2, current through switches M_2 and M_3, I_{M2} and I_{M3} respectively, inductor L_{1A} voltage V_{L1A} and current I_{L1A} and inductor L_{1B} voltage V_{L1B} and current I_{L1B}.

Further details of the invention

1. A three-port direct current converter comprising:
   - at least one input direct current source;
   - at least one storage battery;
   - a primary side circuit;
   - a secondary side circuit;
   - a single magnetic component shared by the primary side circuit and the secondary side circuit,

   wherein the primary side circuit comprises a connection between the at least one input direct current source and the at least one storage battery, the primary side circuit configured for operating as a buck converter,
   wherein the secondary side circuit comprises a connection between the at least one storage battery and at least one load, the secondary side configured for operating as a boost converter,
   and wherein the three-port direct current converter is configured to operate in two mutually exclusive power flow configurations.

2. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter operates as a buck converter

charging the at least one storage battery in a first power flow configuration, and the three-port direct current converter operates as a boost converter driving the at least one load in a second power flow configuration.

3. The three-port direct current converter according to any of the preceding claims, wherein the magnetic component regulates a first output voltage of the primary side circuit in the first power flow configuration, and wherein the magnetic component regulates a second output voltage of the secondary side circuit in the second power flow configuration.

4. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter operates as a voltage step down and current step up converter in a first power flow configuration.

5. The three-port direct current converter according to any of the preceding claims, wherein the first output voltage is regulated to match a predefined voltage range of the at least one storage battery.

6. The three-port direct current converter according to any of the preceding claims, wherein the second output voltage is regulated to match a predefined voltage range of the at least one load.

7. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter is configured to operate without a direct power flow from the at least one input direct current source to the at least one load.

8. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter is configured to operate with one single magnetic component.

9. The three-port direct current converter according to any of the preceding claims, wherein the single magnetic component is the only magnetic component of the three-port direct current converter.

10. The three-port direct current converter according to any of the preceding claims, wherein the magnetic component is a first inductor.

11. The three-port direct current converter according to any of the preceding claims, the secondary side circuit comprising a second inductor serially coupled to the first inductor, wherein the first and second inductors are configured to perform a voltage step-up of the second output voltage.

12. The three-port direct current converter according to claim 7, wherein said secondary side is configured to operate as a tapped boost converter.

13. The three-port direct current converter according to any of the preceding claims, wherein the at least one input direct current source comprises a photovoltaic panel.

14. The three-port direct current converter according to any of the preceding claims, wherein the at least one load comprises a light-emitting diode.

15. The three-port direct current converter according to claim 8, wherein the three-port direct current converter is configured to dim the light-emitting diode according to a state of charge requirement of the at least one storage battery.

16. The three-port direct current converter according to any of the preceding claims, wherein the secondary side circuit comprises parallel-connected loads.

17. The three-port direct current converter according to any of the preceding claims, wherein the secondary side circuit comprises multiple loads.

18. The three-port direct current converter according to claim **Fejl! Henvisningskilde ikke fundet.**, wherein the loads are regulated independently.

19. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter is configured to operate without diodes.

20. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter comprises actively controlled switching elements configured to control power flows of three-port direct current converter.

21. The three-port direct current converter according to claim 9, wherein the actively controlled switching elements are metal–oxide–semiconductor field-effect transistors (MOSFETs).

22. The three-port direct current converter according to any of claims 9-9, wherein a MOSFET M_2 is shared between the primary side circuit and the secondary side circuit.

23. The three-port direct current converter according to any of the preceding claims, the secondary side circuit comprising a MOSFET M_3 between the first inductor and the at least one load.

24. The three-port direct current converter according to any of claims 9-11, the three-port direct current converter comprising a MOSFET M_5 configured to enable and disable the first power flow configuration, such that when M_5 is turned on energy is processed from the at least one input direct current source to the at least one storage battery.

25. The three-port direct current converter according to any of claims 9-12, the three-port direct current converter comprising a MOSFET M_4 configured to enable and disable the second power flow configuration, such that when M_4 is turned on the at least one storage battery powers the at least one load.

26. The three-port direct current converter according to any of claims 9-12, the three-port direct current converter comprising a MOSFET M_1 configured to control the current and voltage of the at least one single magnetic component.

27. The three-port direct current converter according to any of claims 9-13, wherein M_1, M_2 and M_3 are driven by pulse-width modulated signals, and M_4 and M_5 are

driven by enable/disable signals that do not vary within the power flow configurations.

28. A system, such as a street light, or a path light, or a guiding light, or a garden light or decorative light, comprising the three-port direct current converter according to any of claims 1-14.

Claims

1. A three-port direct current converter comprising:
   - at least one input direct current source;
   - at least one storage battery;
   - a primary side circuit;
   - a secondary side circuit;
   - a single magnetic component shared by the primary side circuit and the secondary side circuit,

   wherein the primary side circuit comprises a connection between the at least one input direct current source and the at least one storage battery, the primary side circuit configured for operating as a buck converter,
   wherein the secondary side circuit comprises a connection between the at least one storage battery and at least one load, the secondary side configured for operating as a boost converter,
   and wherein the three-port direct current converter is configured to operate in two mutually exclusive power flow configurations.

2. The three-port direct current converter according to any of the preceding claims, wherein the magnetic component regulates a first output voltage of the primary side circuit in the first power flow configuration, and wherein the magnetic component regulates a second output voltage of the secondary side circuit in the second power flow configuration.

3. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter operates as a voltage step down and current step up converter in a first power flow configuration.

4. The three-port direct current converter according to any of the preceding claims, wherein the second output voltage is regulated to match a predefined voltage range of the at least one load.

5. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter is configured to operate without a direct power flow from the at least one input direct current source to the at least one load.

6. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter is configured to operate with one single magnetic component, and wherein the magnetic component is a first inductor.

7. The three-port direct current converter according to any of the preceding claims, the secondary side circuit comprising a second inductor serially coupled to the first inductor, wherein the first and second inductors are configured to perform a voltage step-up of the second output voltage.

8. The three-port direct current converter according to any of the preceding claims, wherein the at least one input direct current source comprises a photovoltaic panel, and the at least one load comprises a light-emitting diode.

9. The three-port direct current converter according to any of the preceding claims, wherein the three-port direct current converter comprises actively controlled switching elements configured to control power flows of three-port direct current converter, and wherein the actively controlled switching elements are metal-oxide-semiconductor field-effect transistors (MOSFETs).

10. The three-port direct current converter according to claim 9, wherein a MOSFET M_2 is shared between the primary side circuit and the secondary side circuit.

11. The three-port direct current converter according to any of the preceding claims, the secondary side circuit comprising a MOSFET M_3 between the first inductor and the at least one load.

12. The three-port direct current converter according to any of claims 9-11, the three-port direct current converter comprising a MOSFET M_5 configured to enable and disable the first power flow configuration, such that when M_5 is turned on energy is processed from the at least one input direct current source to the at least one storage battery, the three-port direct current converter further comprising a MOSFET M_4 configured to enable and disable the second power

flow configuration, such that when M_4 is turned on the at least one storage battery powers the at least one load.

13. The three-port direct current converter according to any of claims 9-12, the three-port direct current converter comprising a MOSFET M_1 configured to control the current and voltage of the at least one single magnetic component.

14. The three-port direct current converter according to any of claims 9-13, wherein M_1, M_2 and M_3 are driven by pulse-width modulated signals, and M_4 and M_5 are driven by enable/disable signals that do not vary within the power flow configurations.

15. A system, such as a street light, or a path light, or a guiding light, or a garden light or decorative light, comprising the three-port direct current converter according to any of claims 1-14.

Abstract

The present disclosure relates to a three-port direct current converter comprising: at least one input direct current source; at least one storage battery; a primary side circuit; a secondary side circuit; a single magnetic component (L) shared by the primary side circuit and the secondary side circuit, wherein the primary side circuit comprises a connection between the at least one input direct current source and the at least one storage battery, the primary side circuit configured for operating as a buck converter, wherein the secondary side circuit comprises a connection between the at least one storage battery and at least one load, the secondary side configured for operating as a boost converter, and wherein the three-port direct current converter is configured to operate in two mutually exclusive power flow configurations.

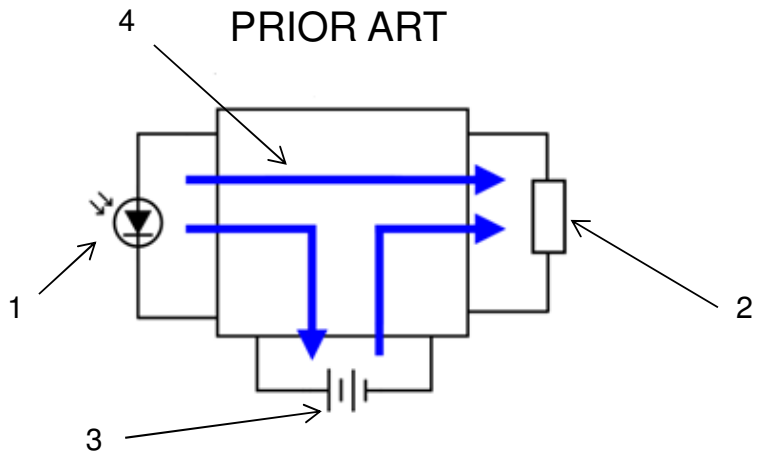

Fig. 1

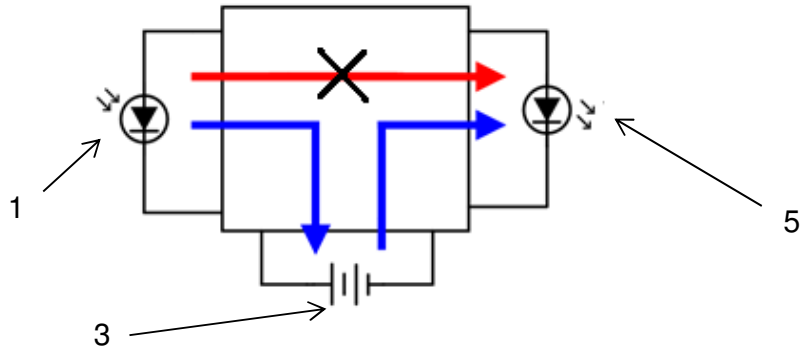

Fig. 2

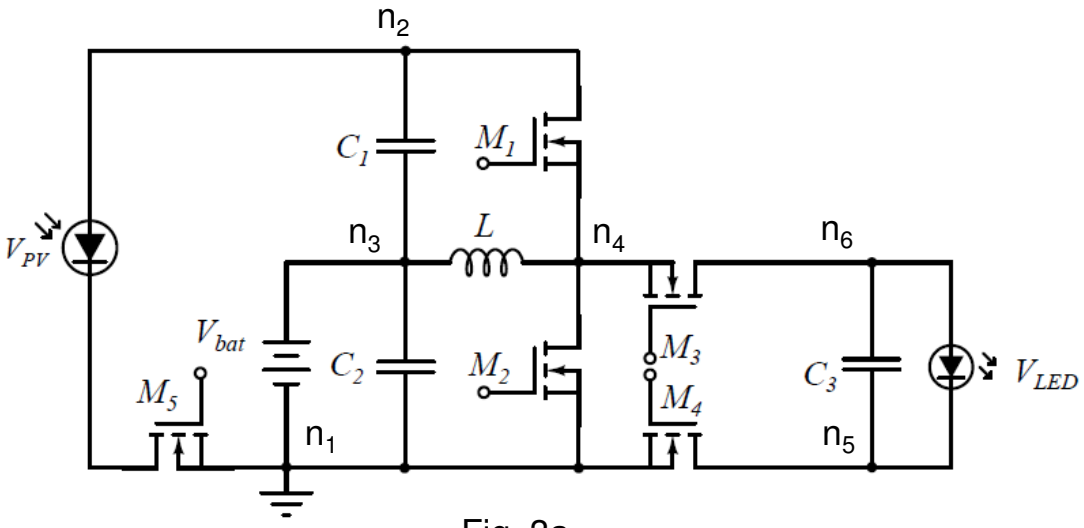

Fig. 3a

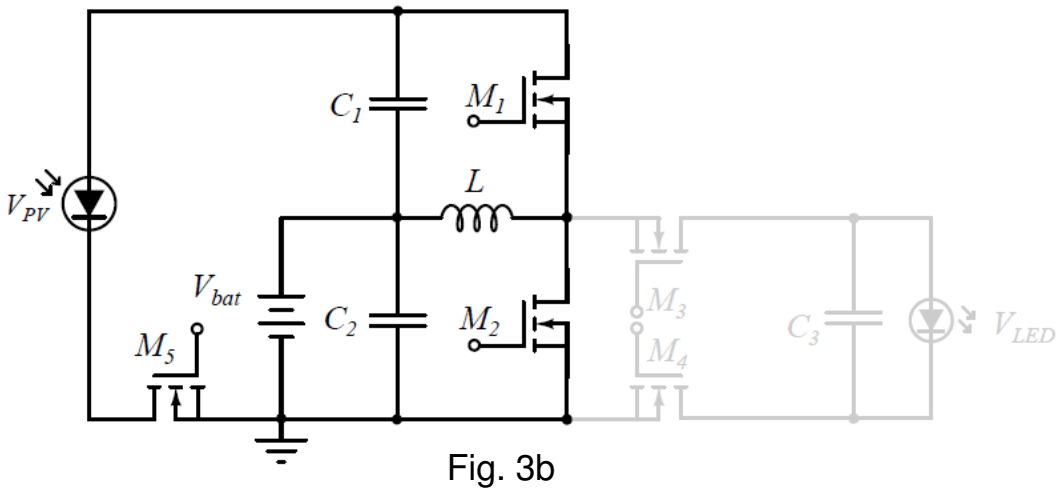

Fig. 3b

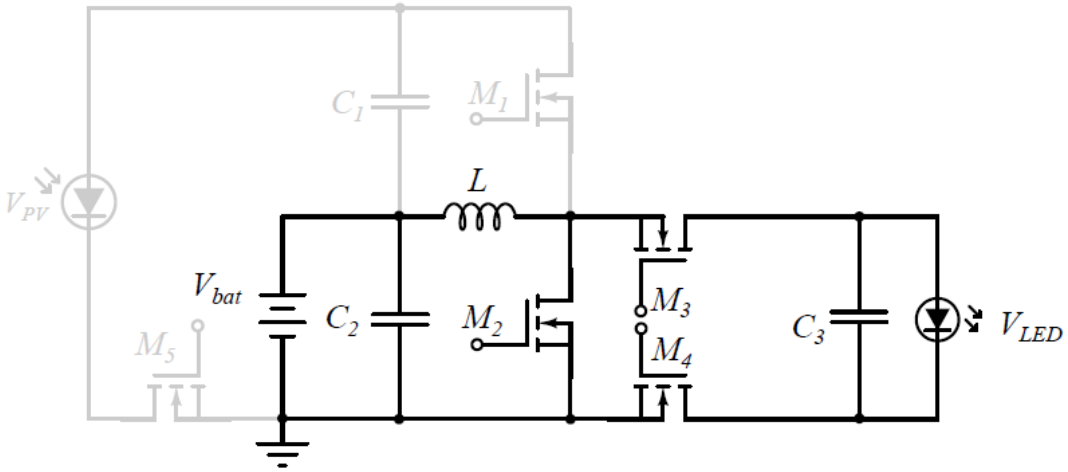

Fig. 3c

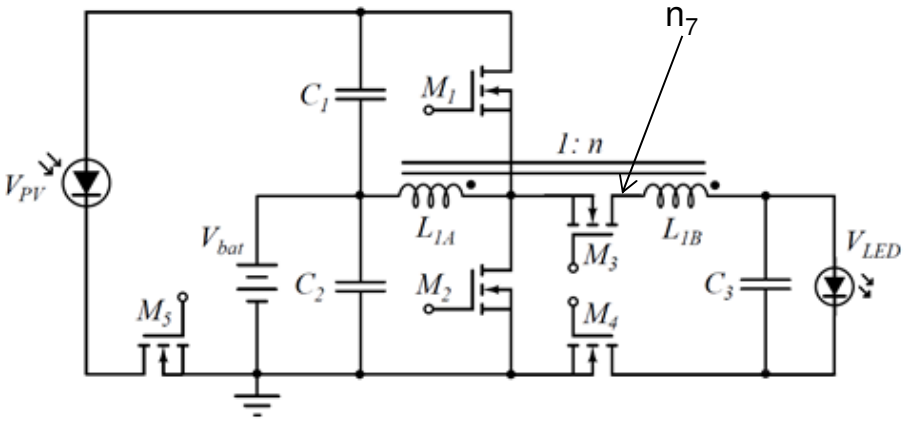

Fig. 4a

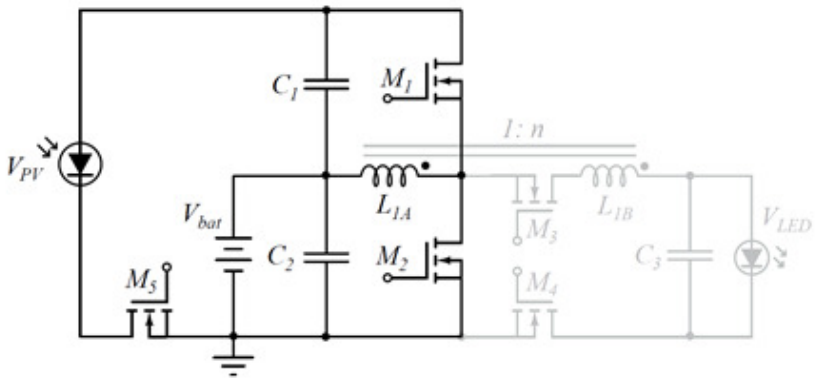

Fig. 4b

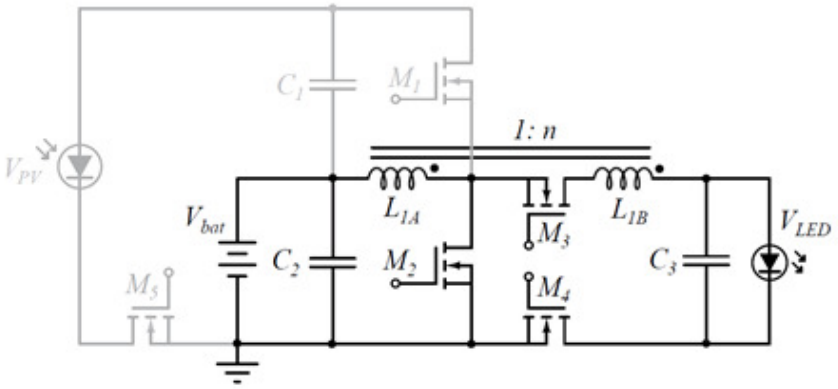

Fig. 4c

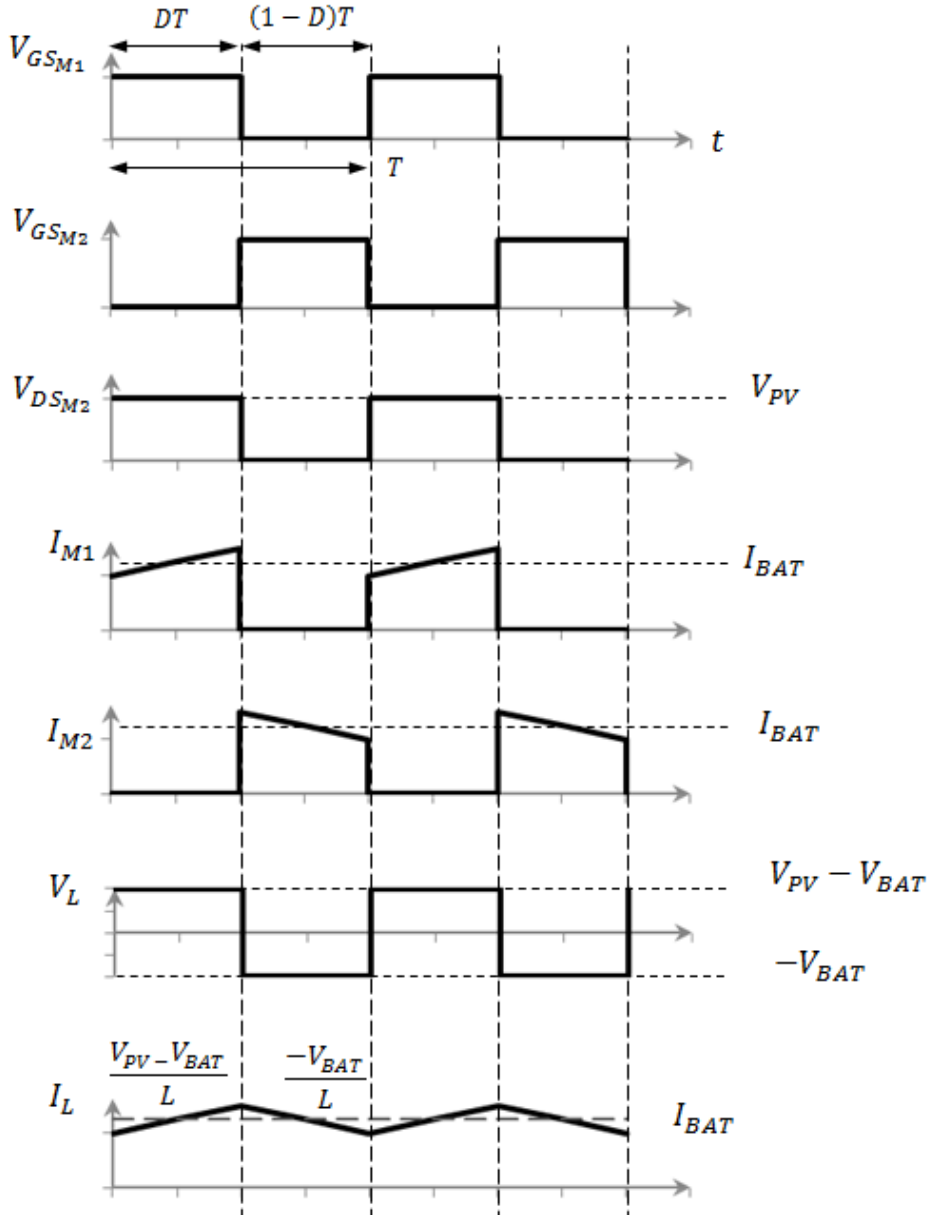
DT
(1 − D)T
$V_{GS_{M1}}$
t
T
$V_{GS_{M2}}$
$V_{DS_{M2}}$
V_{PV}
I_{M1}
I_{BAT}
I_{M2}
I_{BAT}
V_L
$V_{PV} - V_{BAT}$
$-V_{BAT}$
$\frac{V_{PV}-V_{BAT}}{L}$
$\frac{-V_{BAT}}{L}$
I_L
I_{BAT}

Fig. 5

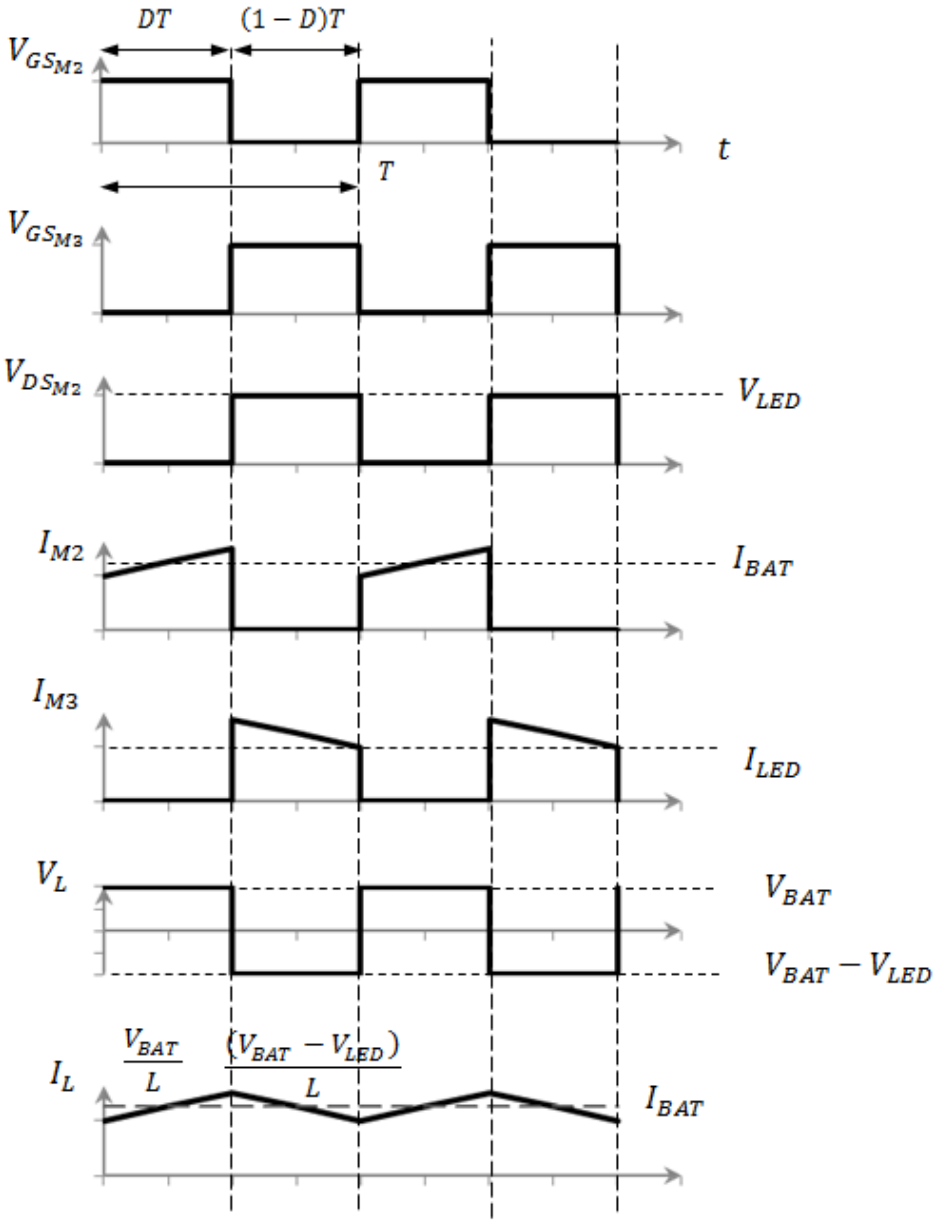
DT
(1 − D)T
$V_{GS_{M2}}$
t
T
$V_{GS_{M3}}$
$V_{DS_{M2}}$
V_{LED}
I_{M2}
I_{BAT}
I_{M3}
I_{LED}
V_L
V_{BAT}
$V_{BAT} - V_{LED}$
I_L
$\frac{V_{BAT}}{L}$
$\frac{(V_{BAT} - V_{LED})}{L}$
I_{BAT}

Fig. 6

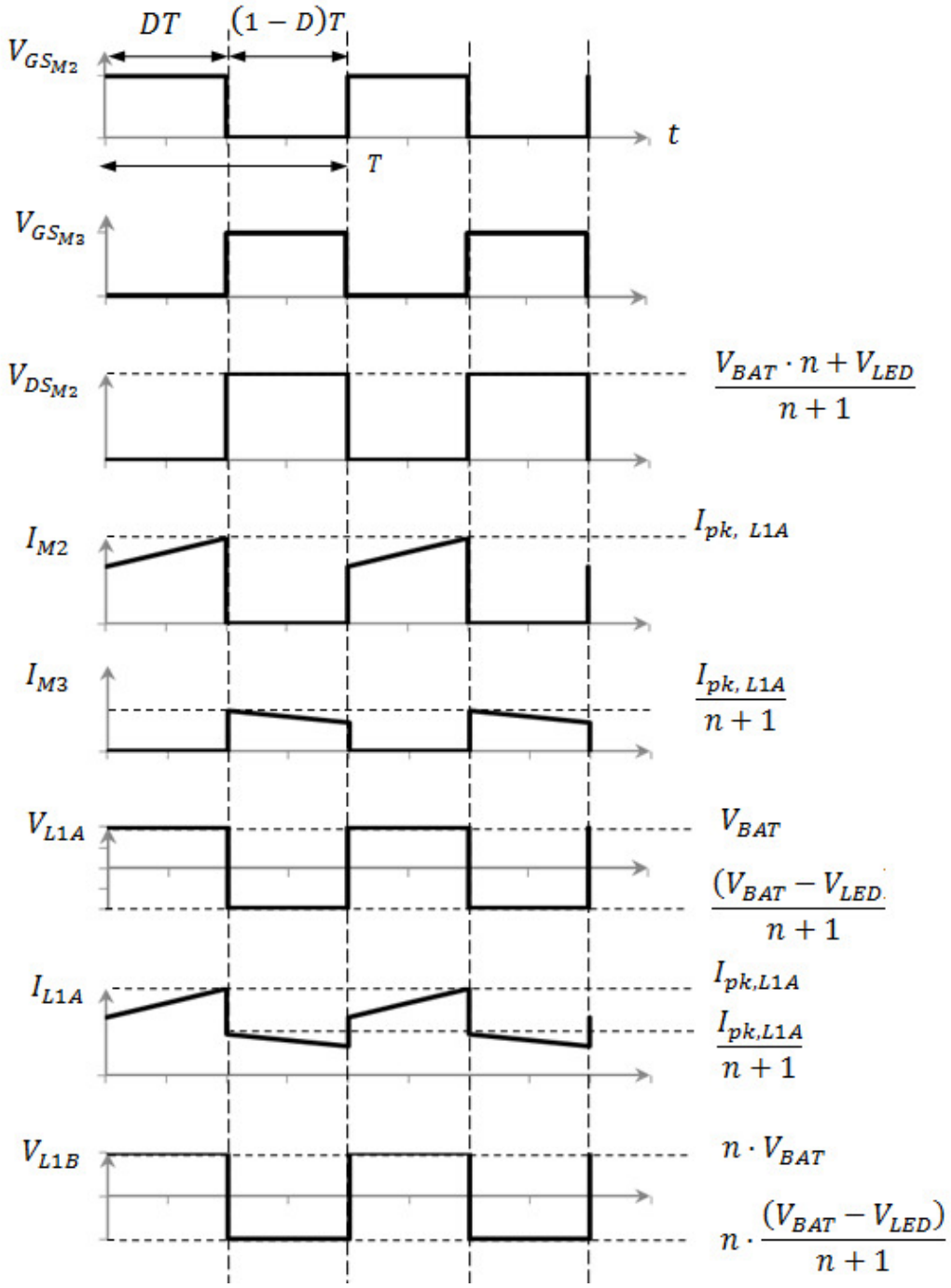
DT
(1 − D)T
$V_{GS_{M2}}$
t
T
$V_{GS_{M3}}$
$V_{DS_{M2}}$
$\frac{V_{BAT} \cdot n + V_{LED}}{n+1}$
I_{M2}
$I_{pk,\ L1A}$
I_{M3}
$\frac{I_{pk,\ L1A}}{n+1}$
V_{L1A}
V_{BAT}
$\frac{(V_{BAT} - V_{LED})}{n+1}$
I_{L1A}
$I_{pk,L1A}$
$\frac{I_{pk,L1A}}{n+1}$
V_{L1B}
$n \cdot V_{BAT}$
$n \cdot \frac{(V_{BAT} - V_{LED})}{n+1}$

Fig. 7

H

Analysis and Comparison of Magnetic Structures in a Tapped Boost Converter for LED Applications

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Analysis and Comparison of Magnetic Structures in a Tapped Boost Converter for LED Applications

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***Abstract*— This paper presents an analysis and comparison of magnetics structures in a tapped boost converter for LED applications. The magnetic structure is a coupled inductor which is analyzed in a conventional wire-wound core as well as in a planar structure for different interleaving winding arrangements. The analysis is performed in terms of leakage inductance, winding capacitance and winding loss. Efficiency measurements are performed to verify the effect on the converter performance.**

Keywords*— High step-up, stand-alone, LED lighting, tapped-inductor, leakage inductance, stray capacitance.

I. INTRODUCTION

Modern switched-mode power supplies (SMPS) nowadays, are dominated by a trend to achieve both high efficiency and high power density. In order to increase the converters power density, the energy storage requirement plays an important role. One option to reduce the size of the energy storage elements is to increase the converter switching frequency using soft-switching techniques [1], however in hard switched PWM converters the increment in the switching frequency is penalized in the form of increased converter switching losses. This work focusses on evaluating different magnetic structures for a LED lightning application in order to maximize the converter efficiency.

On the one hand, planar magnetics components provide lower profile than conventional wire-wound structures. Moreover, planar magnetic technology provides good thermal characteristics since they present higher surface area, which make them more efficient to conduct heat. Furthermore, lower leakage inductance than conventional structures can be achieved because of improved magnetic coupling and extensive interleaving [2], [3]. All these characteristics make planar magnetics a good candidate for effectively increasing the system power density and efficiency. Moreover, printed circuit boards (PCB) windings offer easier manufacturability and better repeatability than conventional wire-wound magnetic components. On the other hand, planar magnetics present the disadvantage of increased inter-layer capacitance and limited number of turns by the manufacturing process.

The stored energy in the leakage inductance of the magnetic component causes undesirable overvoltage spikes on the drain of the main switch at turn off, which leads to increased switching losses. On the other hand, applications with high voltage stress will suffer from large stray capacitances in the magnetic structure, which can lead to undesirable resonating current spikes and consequently large capacitive switching losses. In this work an analysis and comparison of magnetics structures in a tapped boost converter for LED applications is performed. The aim is to compare different winding arrangements in a conventional wire-wound structure in terms of leakage inductance, winding capacitance and winding loss. The results are compared to the possible advantages attained by using planar magnetics instead of conventional wire-wound structures. The magnetic component is a coupled inductor, which is analyzed in a conventional wire-wound core ETD for full interleaving, partial interleaving and no interleaving and compared to a planar structure ELP with full interleaving winding arrangement.

II. SYSTEM ANALYSIS AND SPECIFICATIONS

The application under analysis is a stand-alone photovoltaic LED lamp system with a lithium battery for energy storage. The photovoltaic panel is formed by two parallel-connected monocrystalline panels. The integrated battery is a LiFePO4 (lithium iron phosphate) battery from GWL Power with a nominal voltage of 3.2 V and a capacity of 15 Ah. The LED lamp is composed of eight series-connected Cree XLamp XP-E. Fig. 1 shows the LED lamp I-V curve extracted from the component datasheet and Table I presents the specifications of the PV-LED system.

Three port converter topologies (TPC) for renewable energy systems [3] have been recently introduced. These topologies claim to provide higher efficiency and power density than conventional cascaded structures [4] due to reduced conversion stages. However, it is required to add extra switches to provide controllability and/or diodes to configure the power flow path. Therefore, TPC topologies need a high number of semiconductors, which directly influences the system efficiency and power density. Figure 2 shows the block diagram of the TPC structure and the conventional cascade converters in a light to light (LtL) system. In this work the conventional cascaded structure is preferred since it features lower number of components and easier implementation of the control scheme of the maximum power point tracking (MPPT) and battery management system (BMS) than TPC topologies.

TABLE I
PV-LED SYSTEM SPECIFICATIONS

P_{PV_mp}	$10.92\ W$
V_{mp}	$6.50\ V$
I_{mp}	$1.68\ A$
V_{oc}	$8.10\ V$
I_{sc}	$1.86\ A$
$V_{bat-nom}$	$3.2\ V$
R_{bat}	$\leq 9\ m\Omega$
LED	$8\ x\ [2.6 - 3.3]\ V_{fw}$

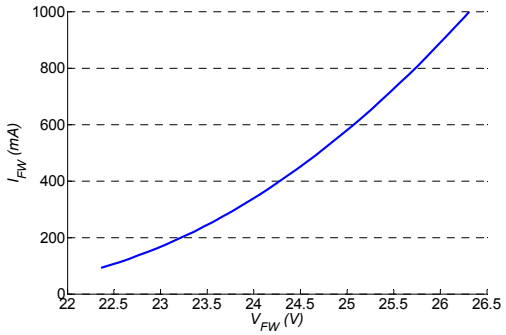

Fig. 1 LED lamp $I - V$ curve (8 series-connected LED Cree XLamp XP-E)

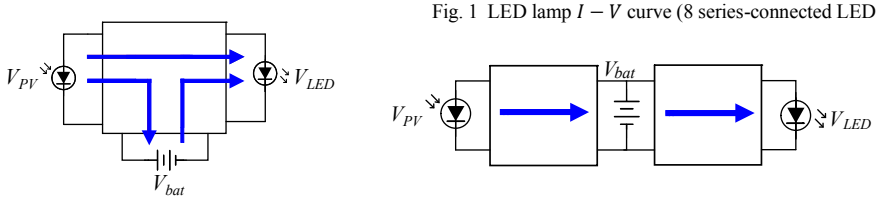

Fig. 2 Light to Light (LtL) three port converter TPC (left) and cascaded solution (right)

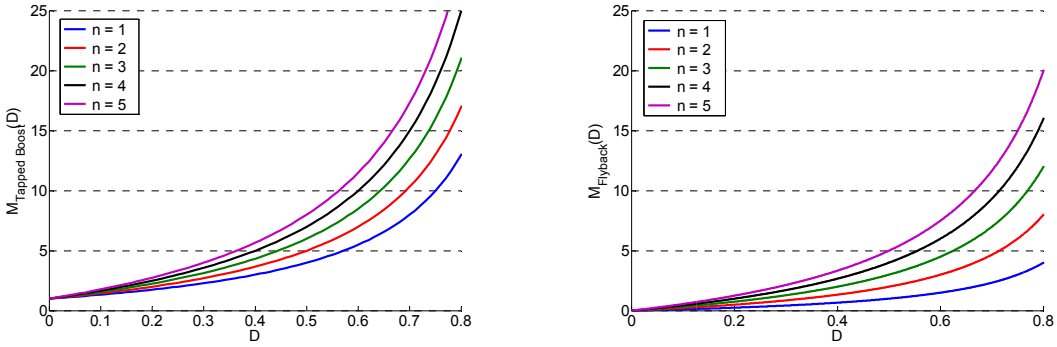

Fig. 3 Tapped boost topology (left) and flyback converter (right) input to output voltage gain

The topology selected for the LtL system is a buck converter from the photovoltaic panel to the battery and a tapped boost converter from the battery to the LED port connected in series. In order to drive the LED light from the battery port, a high voltage conversion ratio is needed. The use of tapped inductors provides high step-up ratio, which makes it possible to avoid extreme duty cycles and high current stress in the components reducing switching and conduction losses [5], [7]. The tapped boost converter achieves high transformation ratio with low amount of components and present higher voltage gain than the flyback topology as shown in Fig. 3. Fig. 4 (a) shows the buck and tapped boost converters series-connected and (b) shows the operating waveforms of the tapped boost converter. During the first subinterval switch M_2 is active and inductor L_2 is charging with a rate determined by the battery voltage and the inductor value. When switch M_2 is turned off, the synchronous rectifier SR_2 turns on and the energy is transferred to the load through the series combination of the inductors L_2 and L_3. The dc voltage transfer function of the tapped boost is obtained from the inductor volt-second balance as shown in (1) and (2).

$$V_{bat} \cdot D_2 T + \left(\frac{V_{bat} - V_{LED}}{n+1}\right) \cdot (1 - D_2)T = 0 \qquad (1)$$

$$V_{LED} = V_{bat}\left(\frac{1 + nD_2}{1 - D_2}\right) \qquad (2)$$

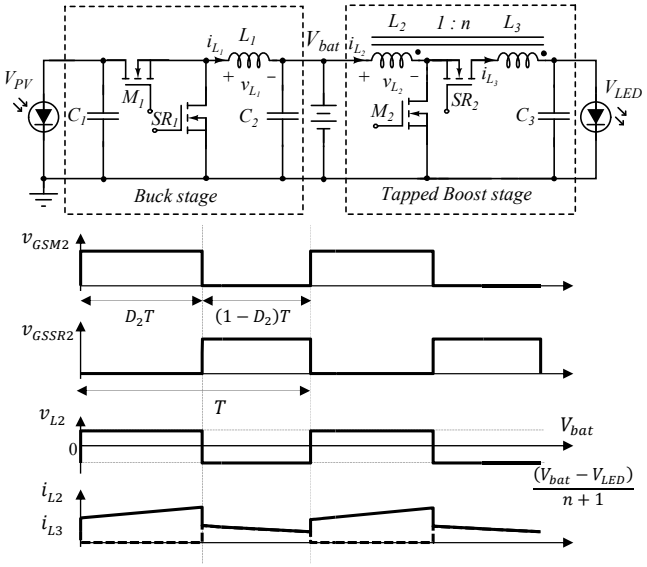

Fig. 4 a) LtL Buck and tapped boost converters series-connected. b) Tapped boost converter operating waveforms: gate to source voltage of switches M_2 and SR_2, inductor L_2 voltage and inductor L_2 and L_3 current, continuous and dotted line.

III. Leakage Inductance, AC Resistance and Stray Capacitance

The different magnetic structures are evaluated taking into account the leakage inductance between the coupled inductors, the parasitic capacitance and the ac resistance. All these components will have a negative effect on the converter efficiency and need to be carefully evaluated.

The leakage inductance is produced by the fact that the flux linkage between two windings is never complete. According to [8] the leakage inductance can be calculated from the energy stored in the magnetic field of the leakage flux. The stored energy in each layer can be found integrating across the cross sectional area of the layer as given by (3). By using (4) the energy stored in the magnetic field can be calculated as in (5).

$$E = \frac{1}{2} \cdot \int B \cdot H \cdot dV = \frac{1}{2} \cdot L_{lk} \cdot {I_p}^2 \tag{3}$$

$$B = \mu_0 \cdot H \tag{4}$$

$$E = \frac{\mu_0}{2} \cdot \int_0^h H^2 \cdot l_w \cdot b_w \cdot dx \tag{5}$$

Where μ_0 is the vacuum permeability, B is the magnetic flux density, H is the magnetic field strength, I_p is the peak current in the winding, l_w is the mean length turn, b_w is the width of the layer and h is the thickness of the layer. The magnetic field strength is equal to the total current passing through the interior of the total flux path as given by (6).

$$H = \frac{I}{l_m} \tag{6}$$

Where l_m is the magnetic path length. If interleaving is used in the structure, the effective magnetic field strength in each of the layer can be considerably reduced. Planar magnetics can help to reduce the component leakage inductance because they make possible to apply extensive interleaving.

On the other hand, the conduction losses due to the winding resistance dramatically increases with frequency due to eddy currents losses (skin and proximity effect). The dc resistance can be calculated according to (7).

$$R_{dc} = \rho \cdot \frac{N \cdot l_w}{b_w \cdot h} \tag{7}$$

Where N is the number of turns and ρ the resistivity of copper at room temperature. The value of ac resistance can be obtained by using Dowell's equation [9] as shown in (8). Dowell curves give the relation between ac and dc resistance for different layers as shown Fig. 5. The value of ac resistance will depend on the m value for each layer, where m can be calculated as the ratio of magneto motive forces (MMFs) to ampere-turns of the actual layer as shown in (9).

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2}\left[\frac{sinh\ \xi + sin\ \xi}{cosh\ \xi - cos\ \xi} + (2m-1)^2 \frac{sinh\,\xi - sin\ \xi}{cosh\ \xi + cos\ \xi}\right] \tag{8}$$

$$m = \frac{F(h)}{F(h) - F(0)} \tag{9}$$

Where $\xi = h\ /\ \delta$ is the ratio between the copper thickness and the skin depth given by $\delta = \sqrt{\rho/\pi\mu_0 f}$.

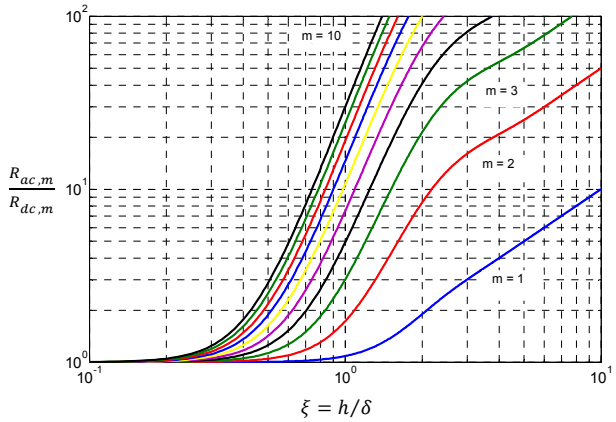

Fig. 5 Dowell's curves. Ratio of ac to dc winding resistance as a function of the conductor thickness and skin depth and number of layers

The value of the inter-winding and intra-winding capacitances can be calculated according to [10] as shown in (10). The electro static energy stored in the capacitance is given by (11).

$$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d} \tag{10}$$

$$E = \frac{1}{2} \cdot C \cdot V^2 \tag{11}$$

Where ε_0 is the vacuum permittivity, ε_r is the relative permittivity of the dielectric material, A and d are the capacitor plates area and distance respectively and V is the total voltage across the winding.

To perform a fair comparison structures with similar core volume are selected. The wire-wound structure core is an ETD29/16/10 with an effective volume of $V_e = 5350\ mm^3$ and the planar structure is an ELP32/6/20 with an effective volume of $V_e = 5390\ mm^3$ both in material N87 from EPCOS. The inductance value and number of turns in each magnetic structure are selected to produce approximately the same core losses. The core losses are calculated using Modified Steinmetz Equation (MSE) according to [11] as shown in (12), (13) and (14). The calculated core losses are 5.6 mW for the ELP and 4.5 mW for the ETD structure, with 4 and 7 turns respectively and a transformation ratio 1:5.

$$P_{MSE} = K \cdot {f_{eq}}^{\alpha-1} \cdot \left(B_{pk}\right)^{\beta} \cdot f \quad (mW/cm^3) \tag{12}$$

$$f_{eq} = \frac{2}{\Delta B^2 \cdot \pi^2} \cdot \int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{13}$$

$$\Delta B = \frac{V_{bat}}{N \cdot A_e}\, D_2\, T \tag{14}$$

Where K, α and β are the Steinmetz coefficients, f is the frequency, B_{pk} is the peak ac flux density, ΔB is the peak to peak ac flux density and A_e is the effective area of the core.

The PCB windings are implemented using 270 μm copper thickness in 8 layers using full interleaving technique (PSPSPSPS). Two PCB stacks are connected in parallel which helps to reduce the dc resistance. The copper thickness of the wire-wound structures ($d = 0.70\ mm$) is selected to have approximately the same copper volume than the planar magnetics PCB windings.

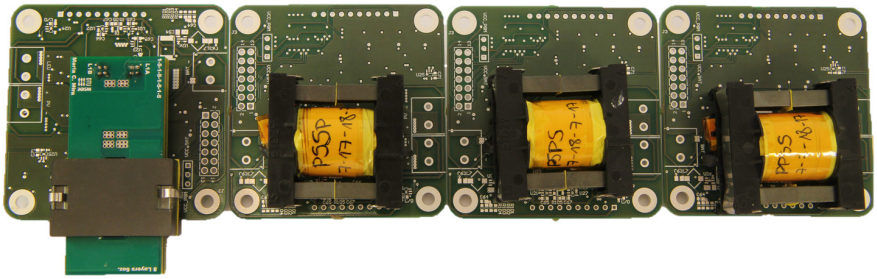

Fig. 6 Coupled inductors in planar magnetics ELP32/6/20 (left) and wire-wound structure ETD29/16/10 core (right) for different winding arrangements

TABLE II
COUPLED INDUCTORS MEASURED PARAMETERS @ 20 KHZ

$\boldsymbol{Core\ Type - n_{pri}/n_{sec}\ (Winding\ arrangement)}$	$\boldsymbol{L_2\ (\mu H)}$	$\boldsymbol{L_{lk}\ (nH)}$	$\boldsymbol{C_p\ (nF)}$	$\boldsymbol{C_{pri-sec}\ (nF)}$
$\boldsymbol{ETD29\ -\ 7/35\ (PSPS)}$	18.64	87.20	0.50	0.19
$\boldsymbol{ETD29\ -\ 7/35\ (PSSP)}$	19.48	97.44	1.04	0.15
$\boldsymbol{ETD29\ -\ 7/35\ (PPSS)}$	18.7	199.20	0.73	0.07
$\boldsymbol{ELP\ 32\ -\ 4/20\ -\ 2\ PCB\ parallel\ (PSPSPSPS)}$	18.56	18.40	4.95	2.78

In order to use the full window width of the ETD structure each of the primary layers is formed by 3 windings in parallel. The copper volume is calculated as $V_{cu} = 1523\ mm^3$ for the ELP structure and $V_{cu} = 1551\ mm^3$ for the ETD core. The implemented winding scheme is U-type, which helps to decrease the distance between windings in order to reduce the structure leakage inductance. However, this arrangement will produce higher capacitive loss than the Z-type winding [12].

Fig. 6 shows the implemented coupled inductors in planar magnetics ELP and conventional ETD wire-wound for different winding configurations. Full interleaving (PSPS), partial interleaving (PSSP), and no interleaving (PPSS) winding arrangements are implemented to compare the effects of the leakage inductance, winding capacitance and winding loss. Table II shows the measured coupled inductor parameters using an Agilent 4294A impedance analyzer. The values are referred to the primary side. The leakage inductance is measured at the secondary side to minimize the error in the measurement. Fig. 7 shows the parasitic capacitances of the tapped-inductor structure. Full interleaving techniques helps reducing the leakage inductance. By interleaving primary and secondary layers the MMF is reduced since each layer effectively operates with $m = 1$. The lowest leakage inductance is achieved with the ELP full interleaving structure. The highest value is given by the ETD core with no interleaving arrangement. On the other hand, the planar magnetics present the highest primary and primary to secondary capacitances, C_p and $C_{pri-sec}$.

Fig. 8 and Fig. 9 show the measured value of the winding resistance as a function of the frequency for the charge and discharge intervals. The measurements are performed with core, therefore they include core and fringing flux loss. The ac resistance cannot be directly extracted from this measurement, however since the couple inductors have been designed to have approximately the same core loss, the measurement allows for a direct comparison of the resistance value of the different structures. The planar structure shows very low dc resistance in both charge and discharge intervals.

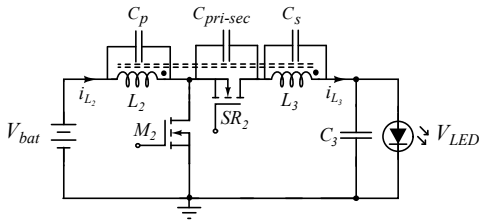

Fig. 7 Tapped-inductor structure stray capacitances

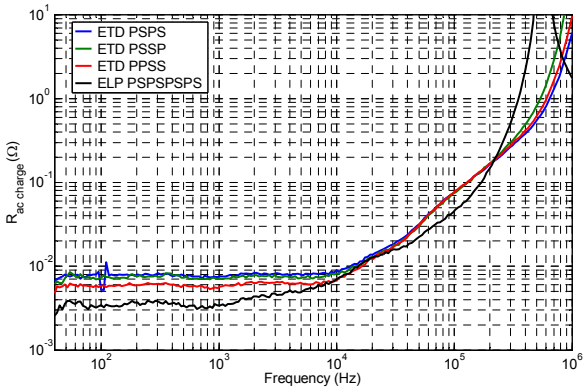

Fig. 8 Coupled inductors measured resistance during the charge interval

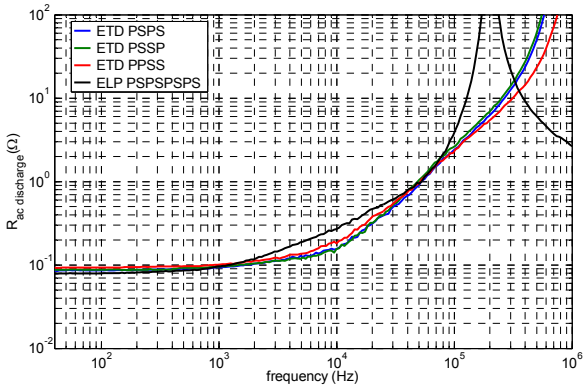

Fig. 9 Coupled inductors measured resistance during the discharge interval

The ELP structure resonance frequency is placed at 500 and 200 kHz for the charge and discharge subintervals respectively. This makes it difficult to compare their ac resistance. However, it is possible to observe that the planar structure at 100 kHz presents the lower charge resistance. On the other hand, the discharge resistance is similar in all the implemented structures.

IV. Experimental Results

Fig. 10 shows the implemented prototype, where the magnetic components are placed at the bottom side of the board. The converter operating frequency is 100 kHz. The power stage is controlled by a 16 bit low power consumption microcontroller from Texas Instruments MSP430F5172. Fig 11 shows the converter operating waveforms with the wire-wound coupled inductors and no interleaving winding arrangement (PPSS). Fig. 12 shows the converter operating waveforms with the planar magnetics structure and full interleaving winding arrangement (PSPSPSPS). The effect of the leakage inductance can be observed in the drain to source voltage of the switch M_2. The energy stored in the leakage inductance resonates with the semiconductor and inductor parasitic capacitances, until it is damped as joule loss in the circuit or until the MOSFET enters into avalanche mode. Moreover, the magnetic component parasitic capacitances can be observed at the switch M_2 turn on event. At this event, a change in the energy stored in the parasitic capacitances will generate the same amount of joule energy loss in the MOSFET channel and circuit parasitic resistances.

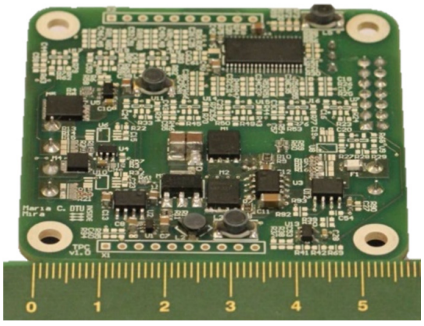

Fig. 10 Tapped boost converter prototype

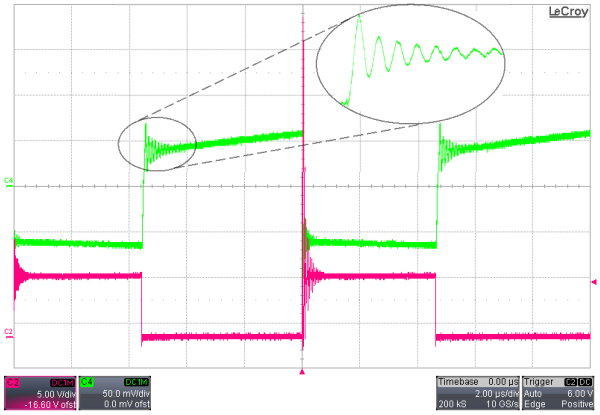

Fig. 11 Tapped boost converter operating waveforms with ETD wire-wound structure and no interleaving winding arrangement (PPSS). Red trace: switch M_2 drain to source voltage (5V/div). Green trace: inductor current (2.5A/div) measured with a Rogowski coil (20mV/A, 125x). Time scale 2µs/div.

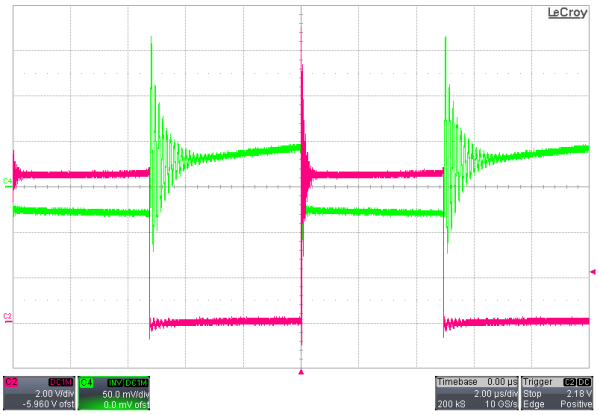

Fig. 12 Tapped boost converter operating waveforms with ELP planar magnetics structure and full interleaving winding arrangement (PSPSPSPS). Red trace: switch M_2 drain to source voltage (2V/div). Green trace: inductor current (2.5A/div) measured with a Rogowski coil (20mV/A, 125x). Time scale 2µs/div.

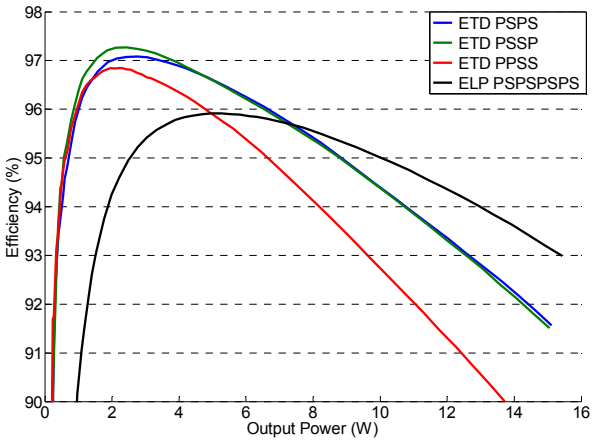

Fig. 13 Tapped boost converter efficiency measurements for different magnetic structures and winding arrangements

Fig. 13 shows the tapped boost converter efficiency measurements for the different structures and winding arrangements. The measurement is performed with 6.5 digit precision multimeters Agilent 34410A and it only includes the power stage losses. From the efficiency measurements the effects of the different parasitics on the converter performance can be observed. The ETD structures with lower stray capacitance than the planar structure present lower capacitive loss. This effect can be observed in the efficiency curves at low power levels where capacitive losses are predominant. After the efficiency peak and as the power level increases the effect of the winding losses and leakage inductance become predominant. The ETD structure with no interleaving presents the lowest efficiency at high power levels since it presents the highest leakage inductance. The ETD structures with full and partial interleaving present similar parasitics values and efficiency curves. The highest efficiency is achieved with the ETD structure with partial interleaving technique (PSSP). Is only at high power levels where the lower ELP leakage inductance gives an efficiency improvement. Due to the high step-up voltage in this application, the inter-winding capacitance $C_{pri-sec}$ is subjected to high voltage stress. The large inter-winding capacitance in the ELP structure causes a large efficiency degradation at low power levels compared to the ETD structures.

In order to evaluate how the capacitive loss affect the total efficiency, the energy loss can be calculated applying (11) and using the stray capacitance measurements from Table II as shown in (15) and (16).

$$E_{C_{pri}} = \frac{1}{2} \cdot C_{pri} \cdot \left({V_{bat}}^2 + \left(\frac{V_{LED} - nV_{bat}}{n+1} \right)^2 \right) \quad (15)$$

$$E_{C_{pri-sec}} = \frac{1}{2} \cdot C_{pri-sec} \cdot (V_{LED} + nV_{bat})^2 \quad (16)$$

However, the measured primary to secondary capacitance $C_{pri-sec}$ corresponds to the capacitance between windings with both of the windings shorted. In the real circuit only the capacitance between the winding turns placed closer to the MOSFET and the synchronous rectifier switching nodes will store most of the inter-winding parasitic capacitance energy. In order to take this into account, the value of this parasitic component is calculated from the self-resonance frequency of the inductor current at the MOSFET turn on event. The calculated inter-winding capacitance values are $520.09\ pF$ and $65.97\ pF$ for the ELP and ETD structures, respectively.

Fig. 14 shows the calculated capacitive power loss of the tapped boost converter working with the planar ELP structure (full interleaving) and with the wire-wound ETD structure (no interleaving). The capacitive loss due to the primary capacitance (C_{pri}) is plotted in blue and black lines for the ELP and ETD structures, respectively. The primary to secondary capacitive loss ($C_{pri-sec}$) is shown in green and red lines for the planar and the wire-wound structures, respectively. It can be observed that the losses due to the primary stray capacitance are very small compared to the loss due to the inter-winding capacitance. This is due to the high voltage stress in this parasitic component. The planar magnetics present high stray capacitance losses, which deteriorate the converter performance at low power levels. At $2\ W$ output power, the inter-winding capacitive loss of the ELP structure corresponds to 30 % of the total converter loss. The wire-wound ETD structure at $2\ W$ output power represents 7 % of the total power loss. As the power level increases, the contribution of the capacitive loss decreases and the major source of loss comes from the ac resistance and the leakage inductance.

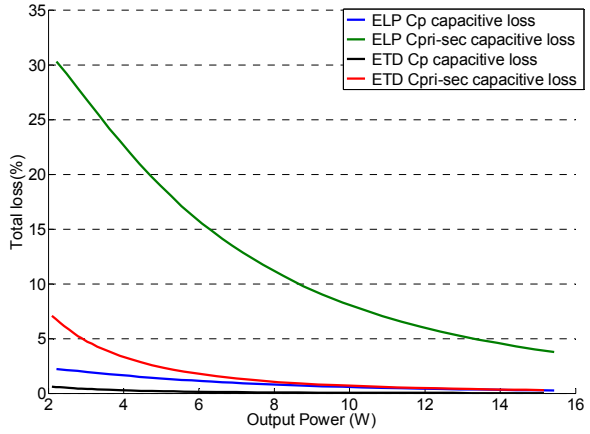

Fig. 14 Calculated capacitive loss of the tapped boost converter with the ELP structure (full interleaving) and with the wire-wound ETD structure (no interleaving)

V. Conclusions

This work presents an experimental evaluation and comparison of conventional wire-wound structures and planar magnetics with PCB windings for a high step-up ratio tapped boost converter. The converter application is a stand-alone LED lighting and the magnetic structure evaluation is performed with the aim of maximizing the converter efficiency. Different winding arrangements are evaluated in terms of leakage inductance, winding resistance and stray capacitances. Efficiency measurements show the influence of the different parasitics on the converter performance. The experimental results shows that the planar structure is only a valid candidate for optimizing the converter at high output power levels where leakage inductance is the predominant cause of loss. However, at low power levels the conventional ETD wire-wound structures are preferred compared to the planar solution due to the smaller parasitic capacitances. Moreover, conventional wire-wound structures make it possible to apply Z-type winding technique to further reduce stray capacitances.

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I

MOSFET Loss Evaluation for a Low-Power Stand-Alone Photovoltaic-LED System

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MOSFET Loss Evaluation for a Low-Power Stand-Alone Photovoltaic-LED System

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***Abstract*- This paper presents a performance evaluation and comparison of state-of-the-art low voltage Si MOSFETs for a stand-alone photovoltaic-LED Light to Light (LtL) system. The complete system is formed by two cascaded converters that will be optimized for a determined solar irradiation and LED illumination profiles. The comparison is performed based on dynamic characterization and evaluation of the devices energy loss at different current levels.**

Keywords— Renewable energy, photovoltaic, stand-alone, LED lighting, switching loss.

I. INTRODUCTION

Renewable energies have become an important part of energy production. Switched-mode power supplies (SMPS) play an important role in the integration of renewable energies due to the requirement of high efficiency conversion. One of the main advantages of renewable energies is the transformation of energy with zero carbon dioxide (CO2) emissions. Moreover, the ability of producing electricity off the grid allows to power up systems at remote locations, where cabling can be challenging and expensive. However, the main disadvantage is that the energy source is intermittent in nature since it strongly depends on the weather conditions. This is especially a drawback for solar energy in northern latitudes where the level of solar irradiation during winter is very low. Moreover, the solar resource in locations far away from the equator is characterized by large annual variations. The length of night and day are very different during the year, consequently, the major part of the solar radiation is received during summer, while there is very little radiation available during winter time as it can be observed in Fig. 1, which shows the annual solar irradiance pattern in a northern latitude [1].

Depending on the converter operating conditions, LED lighting strategy and the amount of available solar irradiance, the operating voltages, duty cycles and consequently current and voltage stresses in the system will vary. In such a system, it is important to investigate the performance of the different components under all the possible conditions. Therefore, it is possible to optimize the system to overcome the limitations due to the geographic location. On the one hand, in locations close to the equator where it is usual to have high irradiance levels all year long, conduction loss will dominate the performance of the system and switching loss will not be as significant. On the other hand, in northern latitudes −especially during winter time− it is important to overcome the low solar radiation by maximizing the system efficiency at low power levels. In this case switching losses will be the predominant source of loss. Switching loss can be difficult to calculate [2] since the result heavily depends on the circuit parasitic inductances and MOSFET input and output capacitances, C_{iss} and C_{oss}, which are highly nonlinear. Instead a measurement of the energy loss is significantly more accurate, since the device performance can be measured at the exact operating conditions. The aim of this paper is to perform a MOSFET loss evaluation for a low-power stand-alone photovoltaic LED system, which will be used in further work to optimize the system for a set of irradiance conditions and LED illumination patterns.

II. SYSTEM ANALYSIS AND SPECIFICATIONS

The investigation of the switching loss will be carried out on a low-power stand-alone photovoltaic LED system for street lightning applications. The system is composed by two parallel-connected monocrystalline panels at the input, a lithium-ion battery for energy storage and eight series-connected Cree XLamp XP-E LED at the output port. Fig. 2 shows the I-V and P-V characteristic curves of photovoltaic panel for different irradiation levels (G). As it can be observed, the output current of a photovoltaic panel varies strongly with changes of irradiation. Fig. 3 shows the LED lamp I-V curve extracted from the component datasheet. Table I presents the specifications of the photovoltaic LED system.

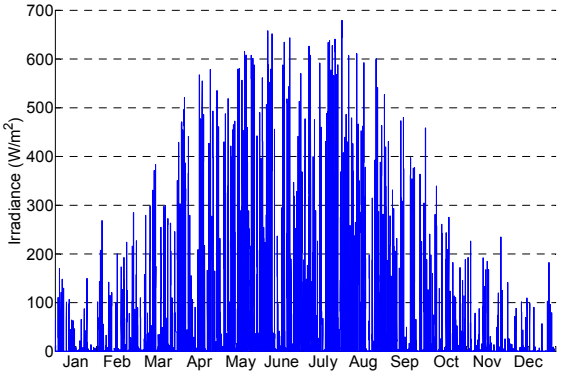


Fig. 1. Annual solar irradiance pattern in a northern latitude

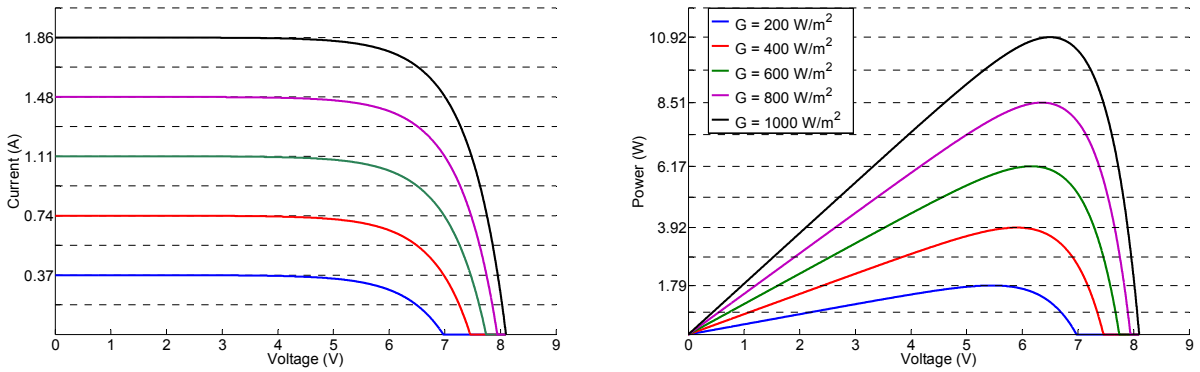


Fig. 2. Photovoltaic I-V (left) and P-V (right) curve characteristic for different irradiation levels (G).

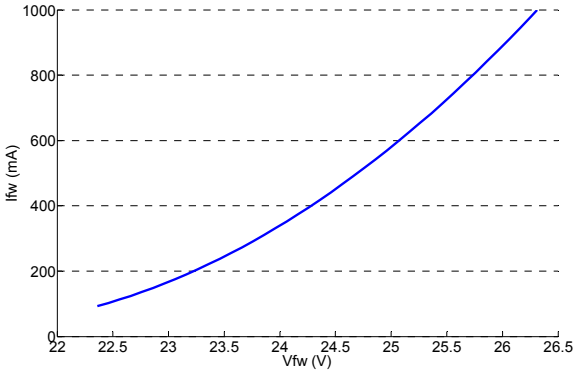


Fig. 3. LED lamp I-V curve (8 series-connected LED).

TABLE I
PV-LED SYSTEM SPECIFICATIONS

P_{PV-max}	10.92 W
V_{mp}	6.5 V
I_{mp}	1.68 A
V_{oc}	8.10 V
I_{sc}	1.86 A
V_{bat}	3.6 V
$Capacity_{bat}$	4.5 Ah
LED	8 x (2.6 − 3.3) V_{fw}

The configuration selected for the Light to Light (LtL) system is a cascaded combination of a buck converter from the photovoltaic panel to the battery and a tapped boost converter from the battery to the LED port, as shown in Fig. 4. An alternative solution to the cascaded configuration is the use of three-port converter topologies (TPC) [3], [4], [5]. Authors claim lower component number, higher efficiency and power density in TPC topologies than in combined separate converters [6], [7]. Nevertheless, many TPC topologies need extra switches and diodes in order to configure the power flow path and to provide controllability [8]. In some topologies, there are switches that are not referenced to ground and need to be active the whole period, which complicates the drive circuitry. In the low-power system under investigation, where the voltages of the photovoltaic panel –especially at low irradiance levels– and the battery are low it is important to avoid any voltage drop, and therefore the use of diodes in the power flow path. A comparison of TPC topologies for low-power stand-alone applications [9] based on component stress factor (CSF) analysis [10], showed that the combination of individual converters provides the best solution, even given the fact that the power from the photovoltaic panel is processed twice in some of the power flows. Therefore, in this application the cascaded structure is preferred because it features low number of components and easy implementation of synchronous rectification in both of the conversion stages. In order to drive the LED port, a high step-up ratio is required. The tapped boost converter is the selected topology because it achieves higher transformation ratio than the flyback topology and presents low number of components. The use of tapped inductors provides the necessary high step-up ratio, which makes it possible to avoid extreme duty cycles and high current stress in the components, reducing switching and conduction losses.

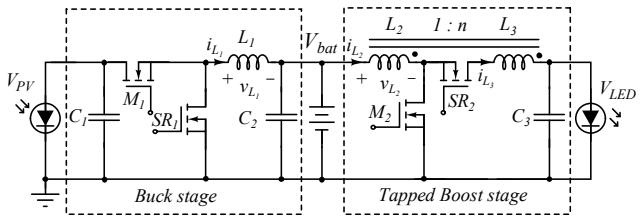


Fig. 4. Light to Light (LtL) system. Buck and tapped boost converters series-connected schematic.

The voltage at the battery port will vary as a function of the load current and battery state of charge (SOC). In order to maintain a stable voltage to perform the measurements, an electronic load configured in constant voltage (CV) mode can be used. However, due to the low voltage and power requirements of the application, a custom build electronic load is used in this work. The schematic circuit and the constructed prototype are shown in Fig. 5 and Fig. 6, respectively. The components used in the prototype are listed in Table II.

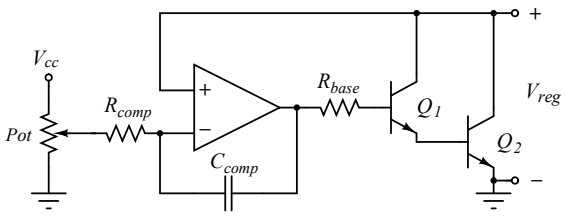


Fig. 5. Schematic circuit of the designed electronic load.

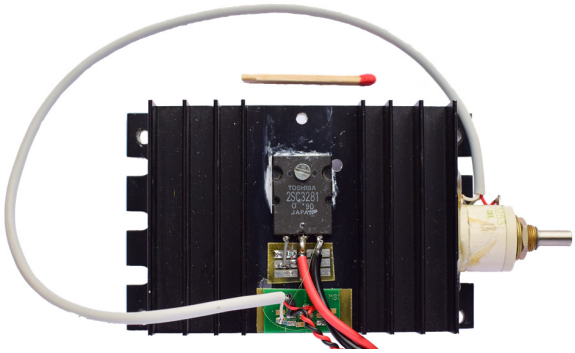


Fig 6. Prototype of the designed electronic load.

TABLE II
ELECTRONIC LOAD COMPONENTS

Q_1	MMBT2222L
Q_2	2SC3281
$op.amp$	MAX4470
R_{base}	470 Ω
R_{comp}	90.1 $k\Omega$
C_{comp}	100 nF
Pot	10 $k\Omega$

The design is based on bipolar junction transistors (BJT) in Darlington configuration in order to achieve high forward current gain. An operational amplifier controls the base current of the BJT pair according to the desired regulated voltage on the collector of the transistors. Therefore, this circuit is used as the load in the buck converter stage (PV panel to battery) in order to keep a regulated voltage during the measurements over the different current values. For the same reason, in the tapped boost converter stage, a power supply with kelvin connection is used at the input port. The kelvin connection is used to regulate the voltage at the converter terminals to achieve a constant voltage over the different current levels. Regarding the load of the tapped boost stage, the 8 series-connected LEDs are used at the output port.

III. SWITCHING LOSS EVALUATION

The switching loss of the LtL system will be evaluated in a buck converter (PV panel to battery) and a tapped boost converter (battery to LED lamp) stages. On the one hand, the switching losses on the buck stage will be measured at different inductor current levels. On the other hand, the switching losses on the tapped boost stage will be investigated for different leakage inductances and stray capacitances of the magnetic component. Both prototypes are implemented using a four layer printed circuit board (PCB) to minimize the areas of the high ac current paths. Moreover, a high bandwidth low intrusive current measurement method as presented in [11], [12], [13], [14] has been used. This current measurement method consists of a parallel combination of resistors with a pick-up wire, which is strategically placed in order to minimize the inductive coupling into the current measurement loop. Fig. 7 shows the implemented prototype with integrated flat current shunt resistors. The current measurement is performed in the main switch as well as in the synchronous rectifier device in both of the stages. The buck converter shunt resistance is composed of 8 parallel-connected 0603 resistors of 500 $m\Omega$ (R_{shunt} = 62.5 $m\Omega$) for both current paths. The tapped boost converter shunt resistors are mounted in the same way, with a total resistance of 67.5 $m\Omega$ and 100 $m\Omega$ for the main switch and the synchronous rectifier, respectively. Since under low solar irradiation conditions the gate losses are also critical, the devices gate loss in both stages are also evaluated. The gate resistance of the main switch and the synchronous rectifier for both of the stages is $R_g = 10\,\Omega$. The MOSFETs gates are driven with a dual input synchronous driver MCP14700 from Microchip with an output voltage of 5 V. The prototype is designed to accommodate two Power-SO8 devices on each stage. The devices are selected with a low threshold value in order to be fully active at the selected driver voltage. Table III shows the characteristic parameters of the devices under test.

The magnetic components in both of the stages are placed at the bottom side of the board. The inductor value of the buck converter is $L = 33\ \mu H$ and is measured with an impedance analyzer Agilent 4294A. The stray capacitance is obtained from the resonance frequency of the impedance curve $C_p = 2\ pF$. The tapped boost stage switching losses are investigated for the coupled inductors structures shown in Fig. 8. The wire-wound structure core is an ETD29/16/10 and the planar magnetics is an ELP32/6/20, both in material N87 from EPCOS. The inductance value is $L = 18.7\ \mu H$ and $L = 18.56\ \mu H$ for the wire-wound and planar magnetics structure, respectively, with a transformation ratio of 1:5.

TABLE III
CHARACTERISTIC PARAMETERS OF THE DEVICES UNDER TEST

	V_{DS}	$R_{DS(on)}$ @ $V_{GS} = 4.5\ V$	Q_G @ $V_{GS} = 5\ V$	C_{oss}
IRFH4213	25 V	1.9 $m\Omega$	30 nC @ $V_{DS} = 13\ V, I_D = 50\ A$	1250 pF @ $V_{DS} = 6.5\ V$
BSC050NE2LS	25 V	5 $m\Omega$	5.5 nC @ $V_{DS} = 12\ V, I_D = 30\ A$	450 pF @ $V_{DS} = 6.5\ V$
FDMS5362L	60 V	74 $m\Omega$	8.7 nC @ $V_{DS} = 36\ V, I_D = 17.6\ A$	68 pF @ $V_{DS} = 45\ V$
Si7120DN	60 V	28 $m\Omega$	16 nC @ $V_{DS} = 10\ V, I_D = 10\ A$	136 pF @ $V_{DS} = 45\ V$

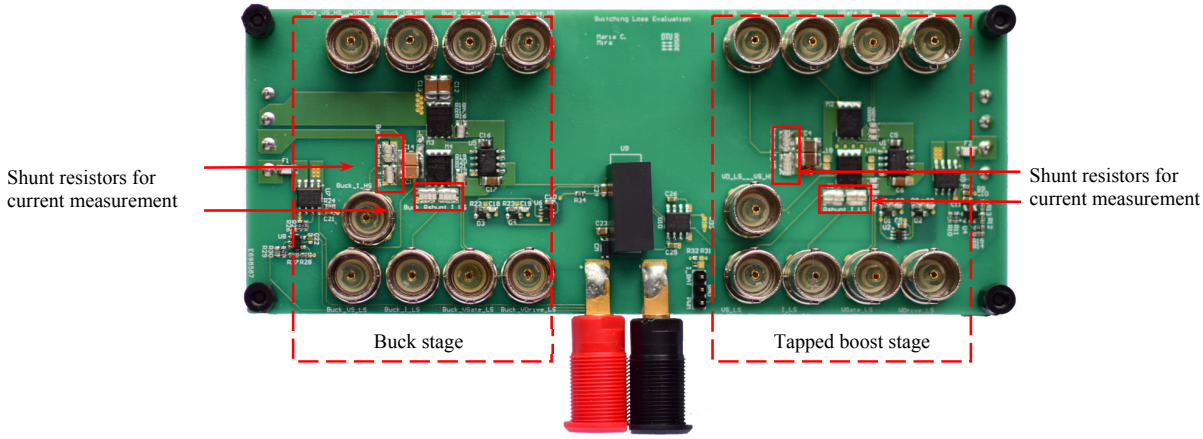


Fig. 7. Buck and tapped boost converter prototypes used to evaluate the switching loss.

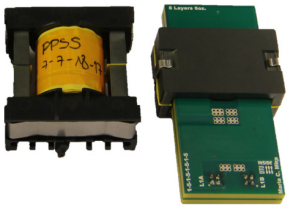
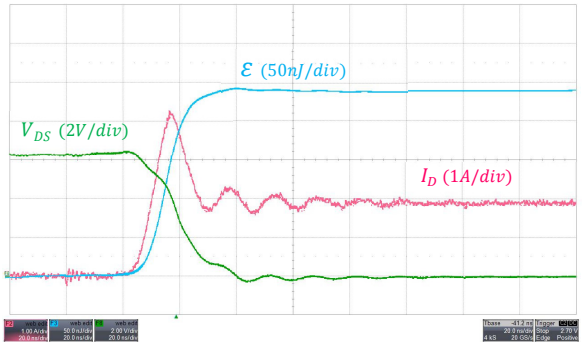


Fig 8. Coupled inductors structures of the tapped boost stage.

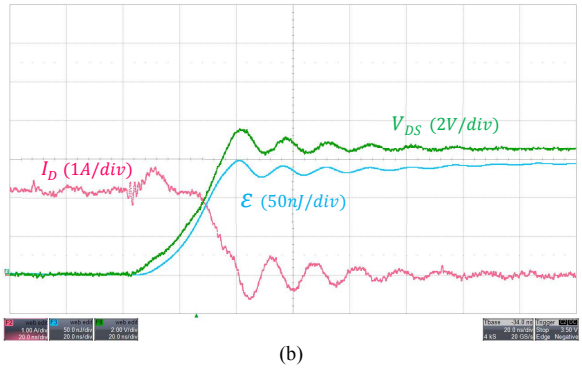
Different coupled inductor structures and interleaving techniques in a tapped boost converter for LED applications were analyzed in [15]. On the one hand, the ETD wire-wound magnetic structure without interleaving (PPSS) presents very low parasitic capacitance ($C_p = 0.73\ nF$) but very high leakage inductance ($L_{lk} = 199.20\ nH$). On the contrary, the planar magnetic structure with full interleaving technique presents very low leakage inductance ($L_{lk} = 18.40\ nH$) but very high stray capacitance $C_p = 4.95\ nF$.

The buck converter stage will be evaluated with the 25 V devices (IRFH4213 and BSC050) for both switches. The input voltage is considered constant ($V_{mp} = 6.5\ V$) since the output voltage of the photovoltaic panel presents small variations with irradiation changes. The tapped boost stage characterization will be performed with the 25V devices as the main switch and the 60 V devices (FDMS5362 and Si7210) as the synchronous rectifier.

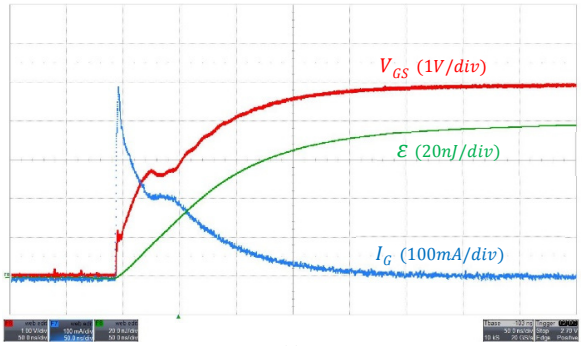
Fig. 9 show the measured switching waveforms of the buck stage with IRF4213 devices. Fig. 9 (a) shows the turn-on event drain-to-source voltage and drain current together with the energy loss. In the same way, Fig. 9 (b) shows the turn-off event of the main switch. Fig. 9 (c) presents the waveforms of the gate-to-source voltage of the synchronous rectifier switch together with the current through the gate resistors and the energy loss. The gate current is obtained from the differential voltage across the gate resistors. The energy measured is half of the total energy loss since the other half is dissipated in the resistive part of the drive circuitry. Fig. 10 presents the measured switching energy at the turn-on and turn-off events together with the energy loss of the main switch and synchronous rectifier gates for different current levels.



(a)



(b)



(c)

Fig. 9. Buck stage measured switching waveforms: turn-on and turn-off event, (a) and (b), respectively, on the main switch IRFH4213. Drain-to-source voltage (green), drain current (light red) and energy loss (light blue). Time scale 20 ns/div. Synchronous rectifier IRFH4213 gate activation (c). Gate-to-source voltage (red), current through the gate resistors (blue) and energy loss (green). Time scale 50 ns/div.

In the same way, the switching energy measurement is performed on the buck stage with BSC050NE2LS devices. Fig. 11 presents the measured switching energy at different current levels. It can be observed that for both of the characterized pair of devices, the gate energy loss is an important part of the total losses, and consequently it cannot be omitted for a low-power application. Fig. 12 shows a comparison of the semiconductor efficiency loss as a function of the available power in the photovoltaic panel for both of the evaluated devices. The switching loss is calculated based on the measured energy loss for a switching frequency of $f_{sw} = 100\,kHz$. The conduction loss is calculated from the semiconductor rms current value. For simplification, both calculations are perfomed assuming zero ripple in the inductor current. As it can be observed, the pair of BSC050NE2LS devices present the lowest semiconductor loss for the whole power range, due to a reduced switching loss. The evaluated IRFH4213 devices possess too large die size area for this application, since the switching losses are predominant over the conduction losses at all the power levels.

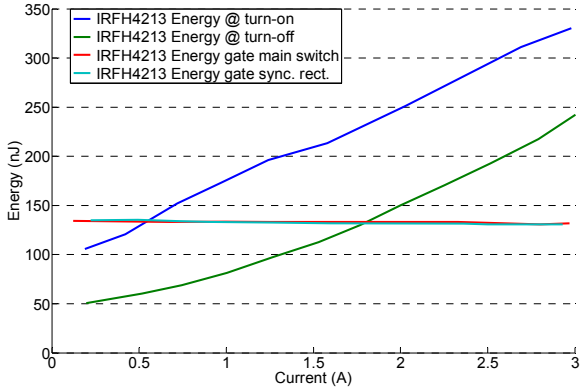


Fig. 10. Buck stage measured energy at different current levels with a pair of IRFH4213 devices.

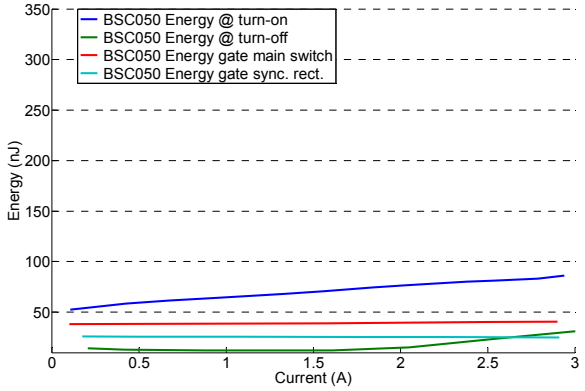


Fig. 11. Buck stage measured energy at different current levels with a pair of BSC050NE2LS devices.

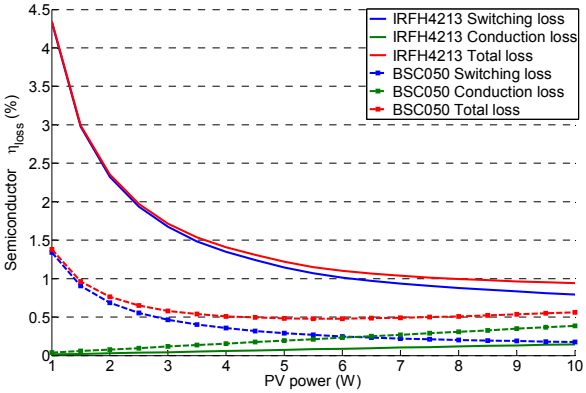


Fig. 12. Buck stage semiconductor efficiency loss for IRFH4213 (continuous line) and BSC050NE2LS (dotted line) devices.

Fig. 13 and Fig. 14 show the energy at the turn-on event for a pair of BSC050NE2LS-Si7120 in the tapped boost stage with the wire-wound and the planar magnetics coupled inductor, respectively. As it can be observed in Fig. 13, due to the large leakage inductance of the wire-wound structure, the turn-on event happens under zero current switching (ZCS) conditions producing zero turn-on switching losses on the semiconductor devices. It is important to observe, that even there is no switching loss on the devices in this event, the charge of the coupled inductor parasitic capacitance is done in a resistive way and the same amount of energy stored in this capacitance will be dissipated in the circuit as resistive losses. Fig. 14 shows the same event with the planar magnetics structure. It can be observed that in this case there is much more energy involved in the charge of the magnetic component parasitic capacitance (5A/div compare to 1A/div in the wire-wound structure). Moreover, in this case there is some overlapping between the drain-to-source voltage and the current (the switch current is equal to 2A before the drain voltage drops down). This is due to the fact that the reduced leakage inductance does not delay the current enough to produce ZCS conditions at the MOSFET turn-on.

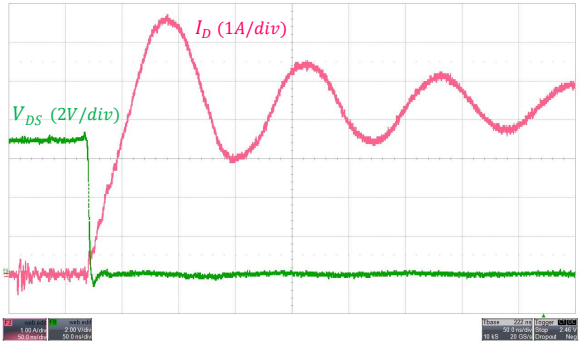


Fig. 13. Turn-on event on the tapped boost stage with ETD wire-wound coupled inductors and BSC050NE2LS-Si7120 devices. Drain-to-source voltage (green) and drain current (light red). Time scale 50 ns/div.

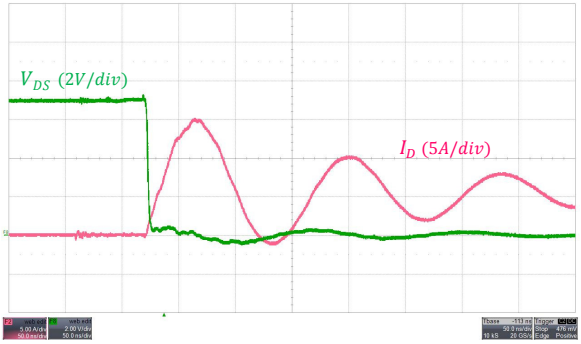


Fig. 14. Turn-on event on the tapped boost stage with planar magnetics coupled inductors and BSC050NE2LS-Si7120 devices. Drain-to-source voltage (green) and drain current (light red). Time scale 50 ns/div.

Fig. 15 shows the turn-on event with the planar magnetic structure and the IRFH4213-Si7120 combination. As it can be observed, the lower switching speed of these devices increases the amount of energy dissipated due to the charge of the parasitic capacitance in the inductors.

Fig. 16 and Fig. 17 presents the measured switching energy on the tapped boost stage with the planar magnetic structure and the wire-wound coupled inductors, respectively, for two combination of devices. Fig. 18 and Fig. 19 show the calculated semiconductor loss as a function of the converter output power or LED power for the planar magnetics and the wire-wound structure, respectively.

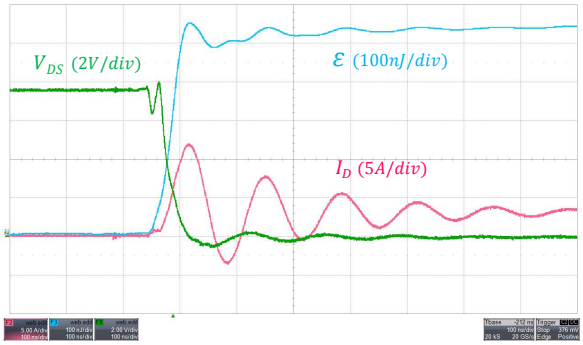


Fig. 15. Turn-on event on the tapped boost stage with planar magnetics and IRFH4213-Si7120 devices. Drain-to-source voltage (green) drain current (light red) and energy (light blue). Time scale 100 ns/div.

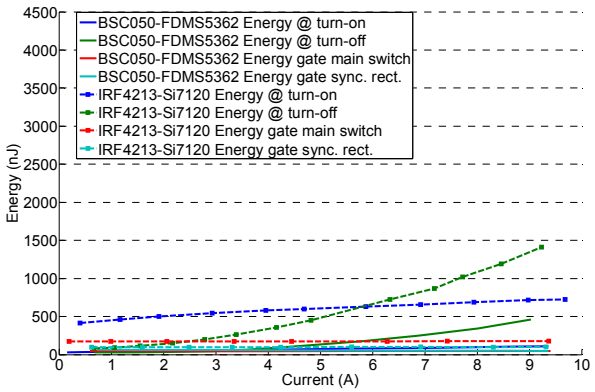


Fig 16. Measured energy at different current levels on the tapped boost stage with planar magnetic coupled inductors.

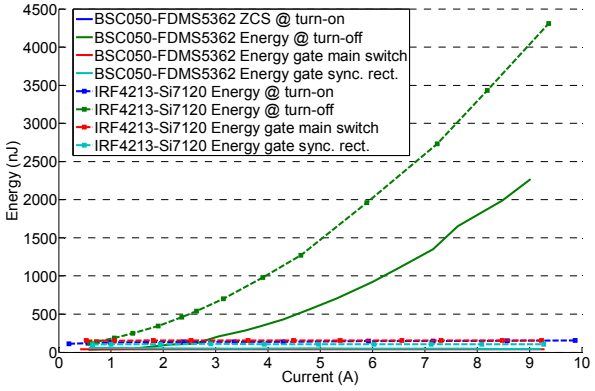


Fig. 17. Measured energy at different current levels on the tapped boost stage with wire-wound coupled inductors.

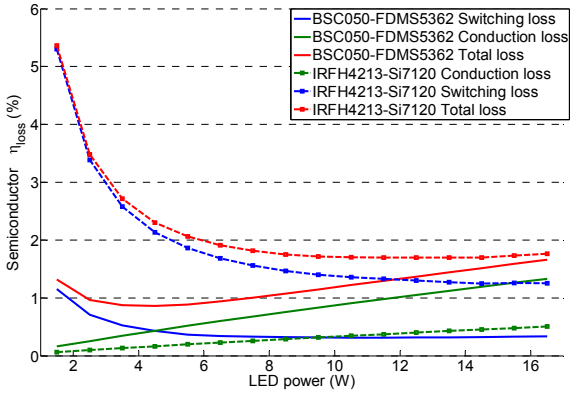


Fig. 18. Semiconductor efficiency loss of the tapped boost stage with planar magnetics coupled inductors.

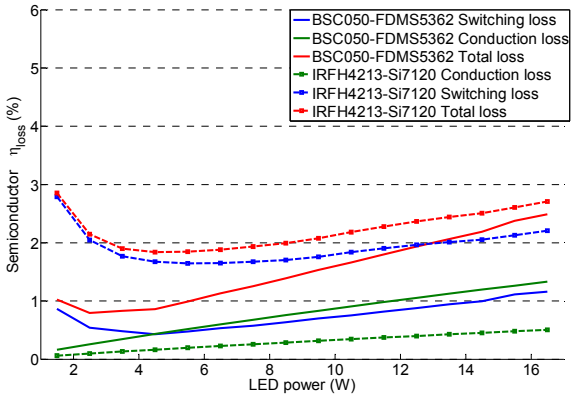


Fig. 19. Semiconductor efficiency loss of the tapped boost stage with wire-wound coupled inductors.

As it can be observed from Fig. 16 and Fig. 18, the high stray capacitance of the planar structure has a negative effect on the semiconductor switching loss at low power levels. This phenomenon is aggravated on the IRFH4213-Si7120 combination due to the reduced switching speed of the devices. However, in the BSC050-FDMS5362 pair, this parasitic capacitance energy will not dramatically affect the semiconductor turn-on loss, but will create energy loss on the circuit parasitic resistances during the charge process, moving the stress to other parts of the circuit. On the other hand, as it can be observed from Fig. 17 and Fig. 19, the increased leakage inductance of the wire-wound structure has a negative effect on the turn-off losses degrading in almost 1% the semiconductor loss at high power levels. Therefore, in this specific application the BSC050-FDMS5362 pair is preferred over the IRFH4213-Si7120 combination because it offers lower total semiconductor loss all the way up to 16 W of output power level, with a 2% improvement in the wire-wound case at 1 W output power level.

IV. Conclusion

This paper presents a MOSFET switching loss evaluation for a low-power stand-alone photovoltaic-LED (LtL) system. The evaluation is performed on a buck stage from the photovoltaic panel to the battery and a tapped boost stage from the battery to the LED output port. The switching energy of several

combination of devices, together with the gate loss energy of the main switch and the synchronous rectifier are measured. Based on the energy measurement, a semiconductor efficiency loss is calculated for both of the analyzed power stages.

In the buck stage the energy measurement shows that the gate energy loss is a significant part of the total losses, especially at low power levels. In the case of the IRFH4213 device, the gate loss of both switches at 1 W corresponds to 2.6% of the total power loss. Therefore, for a low-power application it is important to select a MOSFET with a small total gate charge. The calculated semiconductor efficiency loss of the buck stage presented in Fig. 12 shows an improvement of 3% on the total semiconductor loss at the lowest power level by using the devices with the lower gate charge (BSC050NE2LS). Moreover, this combination performs better over the whole power range of the converter because the reduction in conduction losses of the IRFH4213 is not visible at the evaluated power levels.

The tapped boost stage switching losses are investigated for two coupled inductor structures, with very different leakage inductances and parasitic capacitances. The effect of the high stray capacitance of the planar structure has a negative influence on the turn-on losses, especially at low power levels. However, not all the energy loss from the charge of this capacitance is visible at the MOSFET turn-on event. This is due to the fact that the parasitic inductances produce a delay in the current at turn-on, creating ZCS turn-on conditions depending on the switching speed of the device. This phenomenon can be observed by comparing Fig. 18 and Fig. 19. As it can be seen, the planar magnetics structure produces an increase of the semiconductor switching loss in the IRFH4213-Si7120 combination, but not in the BSC050-FDMS5362 pair. It is importance to notice that even if the parasitic capacitance has not a negative impact in the semiconductor switching loss (because of the ZCS conditions at turn-on), this parasitic capacitance will produce joule losses in different parts of the circuit. On the other hand, the high leakage inductance of the wire-wound magnetic component presents a significant impact on semiconductor turn-off losses. In the application under analysis the LED lighting strategy will operate most of the time at low power levels. In this case, the wire-wound structure with the BSC050-FDMS5362 pair is preferred over the planar structure and the IRFH4213-Si7120 combination, since it offers the best performance due to reduced magnetic and semiconductors parasitic capacitances.

The performed experimental work allows to create an accurate semiconductor loss breakdown, which can be used to perform an optimization for achieving minimum energy loss under a specific irradiance and LED illumination profiles. Therefore, this analysis allows for component selection and optimization of the PV-LED system for different geographic locations.

ACKNOWLEDGEMENT

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Loss Distribution Analysis of a Three-Port Converter for Low-Power Stand-Alone Light-to-Light Systems

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Loss Distribution Analysis of a Three-Port Converter for Low-Power Stand-Alone Light-to-Light Systems

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Keywords

≪Three-Port Converter (TPC)≫, ≪photovoltaic (PV)≫, ≪light-emitting diode (LED)≫, ≪stand-alone≫, ≪high efficiency≫.

Abstract

In locations far from the equator achieving high conversion efficiency in low-power solar systems is challenging due to low solar irradiance levels. This paper presents a high efficiency three-port converter (TPC) for light-to-light (LtL) applications where no direct solar conversion is required. The separation of the power flows allows to replace the conventional solution of two cascaded converters into a single structure with shared components. A loss distribution analysis of the proposed structure is performed, which shows very good match with the experimental results. A prototype of the TPC demonstrates high efficiency in both power flow paths. At low irradiation level, the power flow from the photovoltaic panel to the battery shows a peak efficiency of 99.1% at at 1.5 W output power, and the LED driver stage presents a peak efficiency of 97.3% at 3 W output power.

Introduction

Renewable energy systems play an important role in order to overcome carbon dioxide emissions (CO_2) and fossil fuel resources depletion. Furthermore, due to the ability to generate off-grid electricity, sustainable energy systems have attracted research interest in the last decades [1]. Switched-mode power supplies (SMPS) are a key part of the integration of renewable energy systems due to the importance of high energy conversion [2]. Solar energy is one of the major renewable energy sources because it is unlimited, clean and free. However, because of the intermittent nature of the energy source, solar powered systems need to be combined with an energy storage element. The energy storage turns the assembly into a stand-alone structure, which is very useful to power up systems both at remote locations and in the urban environment, completely eliminating the cost of cabling and construction.

The application under analysis is a light-to-light (LtL) solar powered LED lighting system. Photovoltaic (PV) technology converts the sunlight into electricity, and the generated output power depends on the amount of solar irradiation, which strongly depends on the location and the weather conditions. This is particularly a drawback during winter in northern latitudes, where the length of the day is short and the amount of solar irradiation is very low, as it can be observed in Fig. 1, which shows the annual solar irradiance pattern in a northern latitude [3]. This fact together with the low energy conversion efficiency of PV panels, which is around 18-20% for multicrystalline Silicon (Si) cells [4], makes high efficiency conversion a critical aspect especially in solar powered applications.

Light-emitting diode (LED) technology is gradually replacing conventional lighting systems towards solid-state lighting (SSL) systems due to significantly higher luminous efficacy and longer lifetime [5, 6].

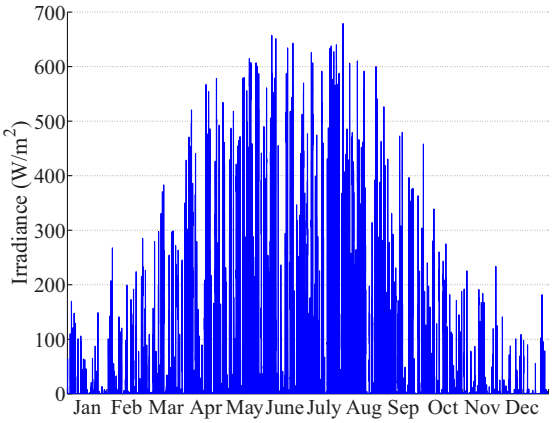


Fig. 1: Annual solar irradiation pattern in a northern latitude [3].

To provide sufficient output illumination single LEDs are combined into arrays to form LED lamps. In high-brightness applications, series connection is usually adopted in order to avoid mismatch in the current of parallel connected LEDs [7, 8, 9] due to devices characteristic *I–V* curve and temperature variation. Moreover, due to the phenomenon known as efficiency droop, where LED efficacy decays at high current values, in order to achieve high luminous efficiency LED strings are typically driven at a low current level, which increases the number of required LEDs for the same luminous output. In low-voltage low-power stand-alone battery applications, these two characteristics makes a high step-up power converter necessary in order to drive a large number of series-connected LEDs.

In locations far from the equator, low-power photovoltaic systems are challenging due to the intrinsic limitations of the geographic location. This paper presents a high efficiency TPC to interconnect with PV panels, energy storage and LEDs for street lightning applications, where no direct solar conversion is required. In order to investigate each component contribution to the total loss, a loss distribution analysis is performed and the theoretical results are compared to the experimental efficiency measurements.

System Specifications

The input port of the LtL system is composed of two PV panels connected in parallel with a maximum power of $P_{mp} = 10.92$ W, $V_{mp} = 6.50$ V, $I_{mp} = 1.68$ A , $V_{oc} = 8.10$ V, $I_{sc} = 1.86$ A. Fig. 2a and Fig. 2b show the characteristic *I–V* and *P–V* curves of the PV panels as a function of the irradiation level (G), where the maximum power point (MPP) is highlighted. The photogenerated current of a PV cell is proportional to the irradiation level and, consequently, the generated output power strongly depends on the irradiation level. As energy storage, a lithium-ion (Li-ion) battery is used at the bidirectional port with a nominal voltage of $V_{bat} = 3.6$ V and 4.5 Ah capacity. At the output port 8 series-connected XP-E high efficiency white LEDs from Cree are used.

In the low-power system under study, it is important to avoid any voltage drop, and therefore the use of diodes in the power flow path. Non-isolated TPC topologies for renewable energy systems have been presented [10, 11, 12, 13, 14]. These type of implementations need additional switches and diodes in order to configure the power flow path among the three ports. Since the application under study is a night street lighting structure, no direct sunlight conversion is required. This allows the sequential separation of the energy flows from the PV source to the battery and from the battery to the LED lighting. As a result, the conventional solution of two cascaded converters [15, 16, 17] can be combined into a single structure with shared components as shown in Fig. 3a. Magnetic components play an important role on the converter size, price and weight. The proposed topology is a combination of two converters, where the magnetic component is shared between the two operation modes by reconfiguring the power flow path depending on the availability of the energy source. Fig. 3b shows the schematic of the proposed stand-alone LtL system and Fig. 4a and Fig. 4b show the circuit configuration for the two energy flows. Switches M_5 and M_4 control the power flow direction depending on the availability of

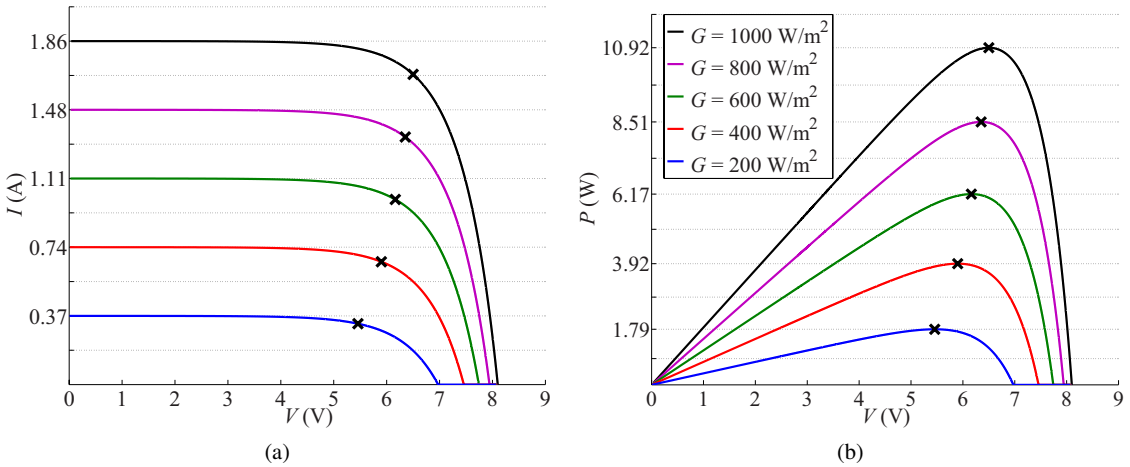


Fig. 2: PV characteristic curves for different irradiations (G) levels @ $T = 25°C$ (a) I–V. (b) P–V.

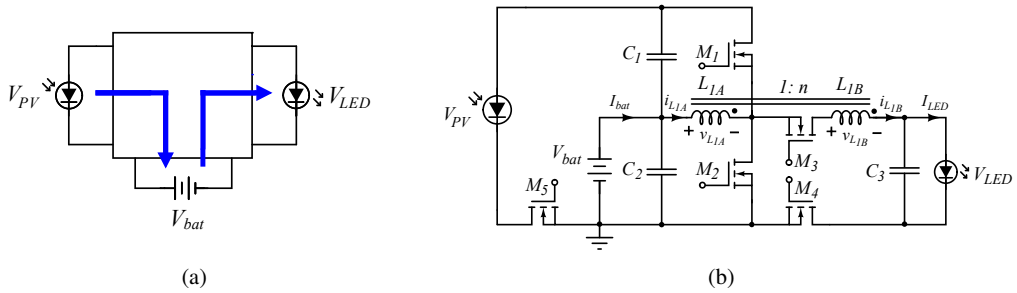


Fig. 3: Low-power stand-alone PV-LED LtL system. (a) block diagram. (b) schematic.

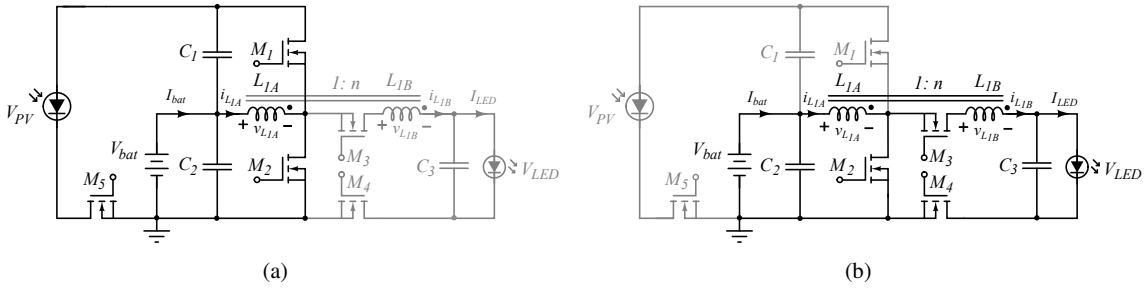


Fig. 4: Schematic of low-power stand-alone LtL system (a) (a) PV panel to battery port power flow: buck mode (b) battery port to LED power flow: tapped boost mode.

the solar energy. When the renewable energy source is available, the system operates as a synchronous buck converter, as shown inFig. 4a. During the night time, the structure is configured as a synchronous tapped boost converter, as shown in Fig. 4b, to provide the high step-up ratio from the battery port to the LED output. The use of the tapped-inductor allows to avoid extreme duty cycles and high current stress in the components, which reduces switching and conduction losses. Fig. 5a and Fig. 5b shows the operating waveforms in buck and tapped boost operation modes, respectively. The proposed solution to interconnect the PV panel, the battery and the LED port makes the power stage to feature low number of components and high efficiency in both operation modes. The switches used to control the power flow path do not contribute to the converters switching losses, which are the predominant source of loss at low power level.

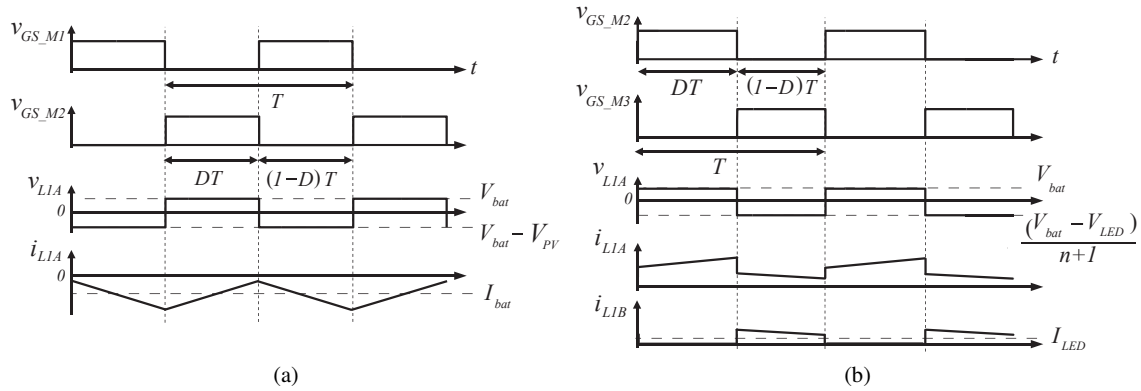


Fig. 5: LtL system operating waveforms (a) PV panel to battery port power flow: buck mode (b) battery port to LED power flow: tapped boost mode.

Loss Distribution Analysis

In this section a loss performance analysis of the power stage of the proposed stand-alone LtL system is performed. The power flow from the battery to the LED (tapped boost mode) is analyzed first. The magnetic component is determined by the specifications of the LED driver stage, which is designed to be able to drive the LED lamp at the maximum current allowed by the LED specifications. However, the LED lamp will be mostly driven at low current level, therefore, the coupled inductors structure will be optimized for operation at low power range. The tapped-inductor is constructed in an ETD29/16/10 core in material N87 from EPCOS, with 7 and 35 turns for L_{1A} and L_{1B}, respectively. Each of the primary layers is formed by 3 windings in parallel. The implemented winding scheme is U-type, which helps to decrease the distance between windings to reduce the leakage inductance. However, this arrangement will produce higher capacitive loss than the Z-type winding. This structure with partial interleaving winding arrangement shows the best efficiency performance at low power levels compared to the same structure with full and no interleaving and a planar magnetics ELP32/6/20 with full interleaving arrangement [18]. The coupled inductor leakage inductance and stray capacitances measured with an impedance analyzer Agilent 4294A are: $L_{lk} = 97.44$ nH, $C_p = 1.04$ nF and $C_{pri-sec} = 0.15$ nF. The inductor winding losses are divided into ac and dc resistive loses. The dc conduction losses are calculated with the squared value of the dc current and the dc resistance as (1). The dc resistance is measured with an impedance analyzer and the value for the charge and discharge intervals is 3.5 mΩ and 81.2 mΩ, respectively. The ac conduction losses are calculated with the squared rms value of the inductor current ac component as (2). The ac resistance is measured by using the method proposed in [19], where the inductor core loss is measured using the resonant method proposed in [20] and separated from the winding loss measurement. The measured ac resistance at the converter switching frequency ($f_{sw} = 100$ kHz) is 47.6 mΩ and 1.27 Ω for the charge and discharge intervals, respectively.

$$P_{dc_{cond}} = {I_{dc}}^2 \cdot R_{dc} \tag{1}$$

$$P_{ac_{cond}} = {I_{rms}}^2 \cdot R_{ac} \tag{2}$$

The core losses are calculated using Modified Steinmetz Equation (MSE) [21] as shown in (3), (4) and (5).

$$P_{MSE} = K \cdot {f_{eq}}^{(\alpha-1)} \cdot {B_{pk}}^{\beta} \cdot f_{sw} \quad [\mathrm{kW/m^3}] \tag{3}$$

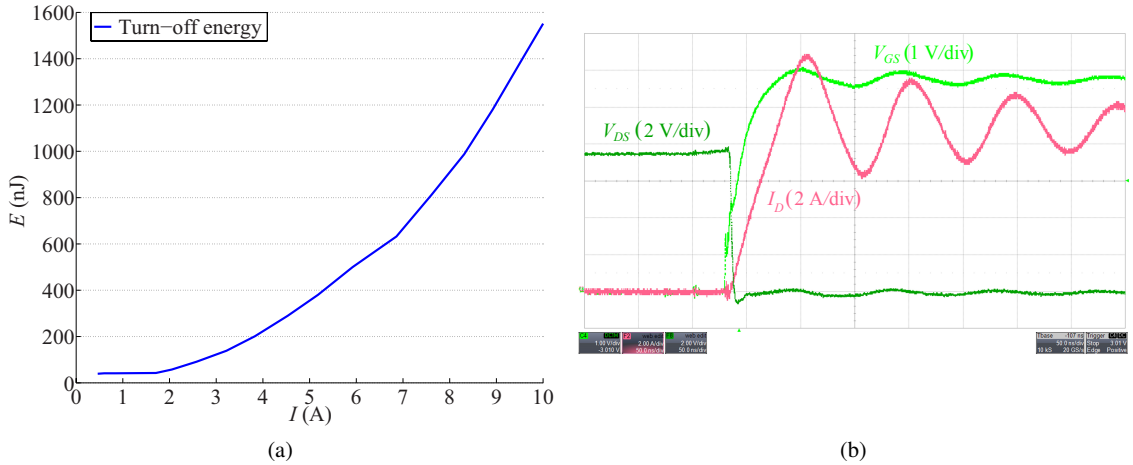
$$f_{eq} = \frac{2}{\Delta B^2 \cdot \pi^2} \cdot \int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{4}$$

$$\Delta B = \frac{V_{bat}}{N \cdot A_e} DT \tag{5}$$

where K, α and β are the Steinmetz coefficients, f_{sw} is the switching frequency, B_{pk} is the peak ac flux density, ΔB is the peak to peak ac flux density, N is the number of turns and A_e is the effective area of the magnetic core.

The MOSFETs selection is performed according to the required blocking voltage in each power flow configuration. In buck mode M_1 and M_2 must withstand a maximum voltage determined by the PV open circuit voltage (V_{oc}). In tapped boost mode, the main switch must block $V_{DS-M2} = (nV_{bat} + V_{LED})/(n+1)$ and the synchronous rectifier must withstand a drain-to-source voltage $V_{DS-M3} = (nV_{bat} + V_{LED})$. In buck operation mode, 25 V devices are selected for M_1 and M_2. This choice also fits the blocking voltage requirement of the shared switch M_2 in tapped boost mode. The selected synchronous rectifier M_3 is a 55 V device. In a low-power system the semiconductor gate and capacitive switching losses have a large effect on the converter efficiency, especially at low power levels. Therefore, a careful selection of the power stage switches in terms of gate charge Q_G and output capacitance C_{oss} must be carried out. Selection of M_1, M_2 and M_3 is performed to achieve high efficiency at low power levels by minimizing capacitive and gate drive losses as presented in [22]. On the other hand, the power flow control devices M_4 and M_5 do not contribute to the switching loss, therefore, the selected devices aim to minimize the conduction loss. The selected MOSFETs of the power stage are: M_1, M_2: BSC050NE2LS, M_3: AUIRL024Z, M_4: BSZ105N04NS and M_5: IRFH4213.

The semiconductor devices can be evaluated by calculating the switching and conduction losses. The conduction losses can be calculated from the devices on-resistance specified in the manufacturer datasheet. However, the switching losses are difficult to calculate due to the circuit parasitic inductances and MOSFET input and output capacitances, C_{iss} and C_{oss}, which are highly nonlinear. A measurement of the energy loss, as presented in [22], provides accurate results because the device performance can be measured at the exact operating conditions. In order to evaluate the converter switching losses, a measurement of the semiconductor energy loss on the battery to LED power flow (tapped boost mode) is performed. Fig. 6a shows the measured switching energy loss at the turn-off event as a function of the inductor current level. Zero turn-on energy loss is obtained in this operation mode due to the leakage inductance of tapped boost structure, which delays the current transition and results in zero current switching (ZCS) turn-on conditions as shown in Fig. 6b. However, the large leakage inductance of the partial interleaving arrangement has a negative impact on the main switch turn-off energy loss at high current levels as it can be observed in Fig. 6a. The semiconductor switching losses are calculated using the obtained



(a) (b)

Fig. 6: Battery to LED power flow (tapped boost) (a) turn-off event measured semiconductor switching energy loss vs. inductor current level. (b) ZCS conditions at turn-on event. Drain-to-source voltage (V_{GS}) (2 V/div), drain current (I_D) (2 A/div) and gate-to-source voltage (V_{GS}) (1 V/div). Time scale 50 ns/div.

characterization data as shown in (6).

$$P_{sw} = f_{sw} \cdot (E_{turn-on} + E_{turn-off} + E_{gate}) \tag{6}$$

where E_{gate} corresponds to the gate drive loss in the main switch M_2 and the synchronous rectifier M_3, which are measured in the characterization setup as 40 nJ and 7 nJ, respectively.

The MOSFETs conduction losses are calculated with the root mean square rms of the current and the device on-resistance as in (7). The MOSFET channel on-resistance is extracted from the manufacturer component datasheet at the selected gate drive voltage value $V_{GS} = 5$ V and at 25°C operating temperature. The extracted values are 5.5 mΩ, 16 mΩ and 50 mΩ for M_2, M_3 and M_4, respectively.

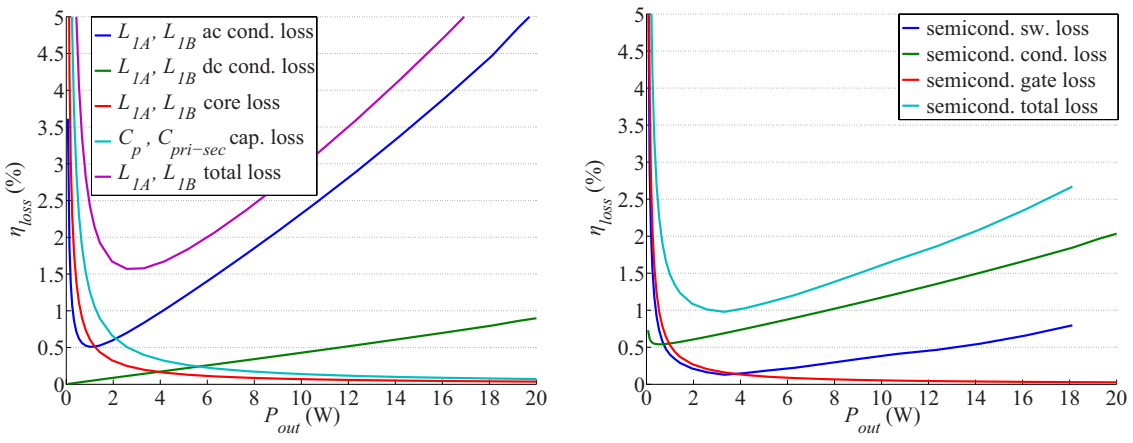
$$P_{cond} = {I_{rms}}^2 \cdot R_{DS-on} \tag{7}$$

Due to the ZCS conditions caused by the coupled inductor leakage inductance, the energy loss in the magnetic component parasitic capacitances is not visible in the semiconductor switching loss characterization. This capacitive loss can be calculated using the measured stray capacitance C_p and $C_{pri-sec}$ as shown in (8) and (9).

$$E_{C_p} = \frac{1}{2} \cdot C_p \cdot \left({V_{bat}}^2 + \left(\frac{V_{bat} - V_{LED}}{n+1} \right)^2 \right) \tag{8}$$

$$E_{C_{pri-sec}} = \frac{1}{2} \cdot C_{pri-sec} \cdot (nV_{bat} + V_{LED})^2 \tag{9}$$

Fig. 7a shows the calculated efficiency loss of the coupled inductor structure as a function of the output power level. The component losses are divided in ac and dc winding loss, core loss and capacitive loss. The magnetic component is optimized to operate at low power level. At it can be observed, at high power level the ac conduction loss is the predominant loss; however, at low power level, core loss and capacitive loss need to be minimized in order to achieve high efficiency operation. Fig. 7b shows the semiconductor losses as a function of the output power. These losses consist of switching, conduction and gate drive losses. As it can be observed, the conduction loss dominates at high power level due to the devices on-resistance. The effect of the coupled inductor leakage inductance can be observed as an increased switching loss at high power level. At low power level, the main loss contribution comes from the capacitive switching and gate loss. Moreover, it is noteworthy that the converter output voltage increases with the output power due to the characteristic LED *I–V* curve, which makes the converter current stress



(a) (b)

Fig. 7: Battery to LED power flow (tapped boost mode) calculated efficiency loss (a) coupled inductors L_{1A}, L_{1B} (b) semiconductors.

to increase faster when the output power increases, further penalizing the conduction losses.

The loss distribution of the PV to battery power flow (buck mode) is next analyzed. Reutilization of the magnetic component is the key point of the proposed PV-LED structure. Inductor L_{1A} is reused in the PV to battery power flow, consequently, all the parasitic capacitances of the coupled inductor structure are reflected and affect the semiconductor switching loss in this operating mode. Therefore, selecting a low parasitic capacitance implementation for the tapped-inductor in the battery to LED power flow reduces the capacitive switching losses in buck mode, which has a positive effect on the converter efficiency at low power level. The same characterization procedure used in the tapped boost is applied to the buck operation mode. The switching energy of the PV to battery power flow is measured at different input voltage levels in order to account for irradiation and temperature variations in the photovoltaic panel.

Fig. 8 shows the measurement of the turn-on and turn-off energy at different input voltages. The turn-off energy loss at zero current level corresponds to the energy stored on the main switch parasitic capacitance, whilst in the turn-on event represents the capacitive loss from the magnetic structure and the synchronous rectifier output capacitance. It can be observed that the switching loss energy increases with the photovoltaic input voltage due to the quadratic dependence of the stored capacitive energy and the converter input voltage. The gate drive energy loss is measured in the characterization setup as 40 nJ

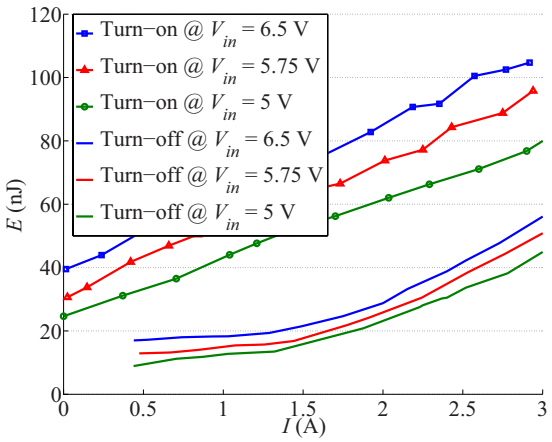
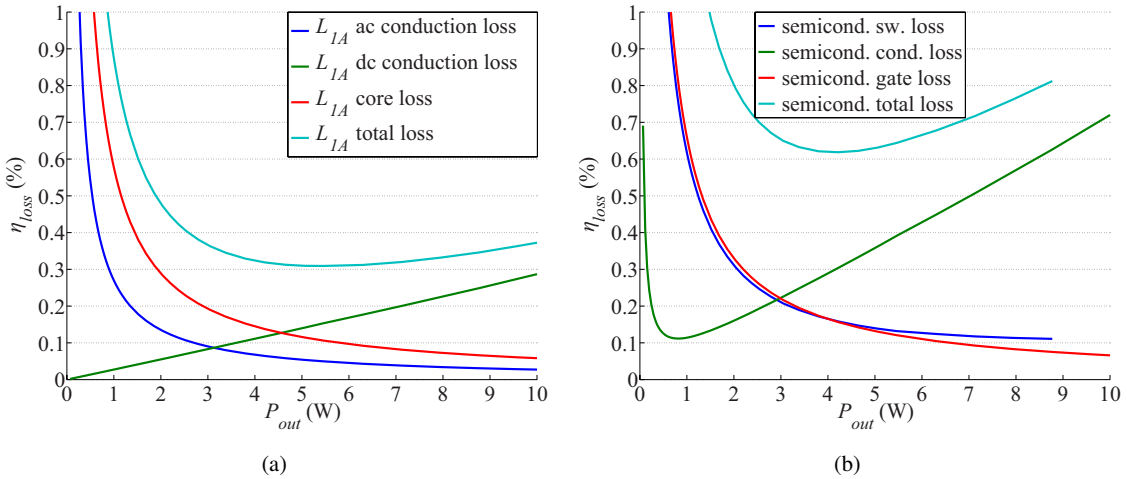


Fig. 8: PV to battery power flow (buck mode) measured semiconductor switching energy loss at different input voltage vs. inductor current levels.



(a) (b)

Fig. 9: PV to battery power flow (buck mode) calculated efficiency loss (a) inductor L_{1A} (b) semiconductors.

and 26 nJ, for the main switch and the synchronous rectifier, respectively. As in the tapped boost mode, the switching loss in buck mode is calculated using (6) and the characterization data from the energy loss measurement. The semiconductor conduction loss is calculated using (7) and the devices on-resistance, which is 5.5 mΩ for M_1 and M_2 and 2.25 mΩ for the power flow control switch M_5. Fig. 9a shows the efficiency loss breakdown for the magnetic component in buck mode. As it can be observed, the core loss produces 1% efficiency loss @ $V_{in} = 6.5$ V and $P_{out} = 1$ W. The core loss could be further reduced by increasing the number of turns without having a big penalty in dc conduction loss at high power levels. However, increasing number of turns will have a negative effect on the magnetic component ac and dc conduction loss in the tapped boost mode. Fig. 9b shows the switching, conduction and gate loss of the LtL system in buck operation mode. It can be observed that the gate and the switching loss have a big effect on the converter efficiency at low power levels, with 1% efficiency loss due to each of them @ $V_{in} = 6.5$ V and $P_{out} = 1$ W. It has to be noticed that the device selection is based on Q_G and R_{DS} trade-off with special interest on achieving reduced gate and capacitive loss. However, due to a limited selection of devices for low-power applications, the selected MOSFETs still possess a large die size for the selected application, resulting in a decreased performance at low power levels.

Experimental results

In order to verify the loss distribution analysis of the proposed low-power TPC a prototype of the LtL system is constructed. Fig. 10 shows the top and bottom sides of the experimental prototype. A low-power mixed-signal microcontroller MSP430F5172 is selected to digitally implement the different control loops on the power stage. The prototype is working with maximum power point tracking (MPPT) on the PV side, constant voltage (CV) and constant current (CI) control on the battery side and dimming regulation at the LED output port. A Hall effect current sensor is used for monitoring the battery port current, which allows implementation of the different control algorithms.

The efficiency is measured with 6 ½ digit multimeters Agilent 34410A. The instruments are connected and synchronized through a computer and set up with long integration time in order to ensure high frequency noise filtering and good repeatability. Efficiency curves are measured for both power flow paths as shown in Fig. 11, Fig. 12a and Fig. 12b. Fig. 11 shows the efficiency measured on the battery to LED power flow (tapped boost mode) together with the calculated efficiency. The measurement is performed only on the power stage and does not include the gate drive and control circuitry losses. The calculated total gate loss on this stage is 4.7 mW. The input and output ceramic capacitor conduction losses are also included in the calculation although they have a low impact on the converter efficiency. As it can be observed, the predicted efficiency shows a good match with the measured efficiency, which validates the performed loss distribution analysis. The low capacitive implementation of the magnetic structure and the selection of the semiconductor devices with low parasitic capacitances make it possible to achieve high efficiency at low power levels. In this case, a high step-up tapped boost stage with more than 97% efficiency for output power levels in the range of 1.5 W to 5.5 W is demonstrated. Fig. 12a presents the calculated and measured converter efficiency for the PV to battery power flow (buck mode) at $V_{in} = 6.5$ V. Equal than before, the input and output capacitor, but not the gate drive losses of the power stage, which are calculated to be 6.6 mW. An efficiency higher than 98% is achieved from 0.7 W

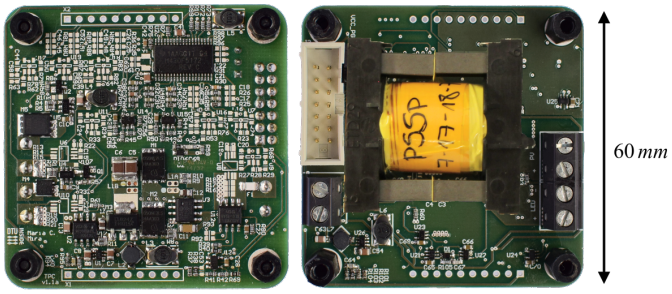


Fig. 10: Low-power stand-alone LtL prototype.

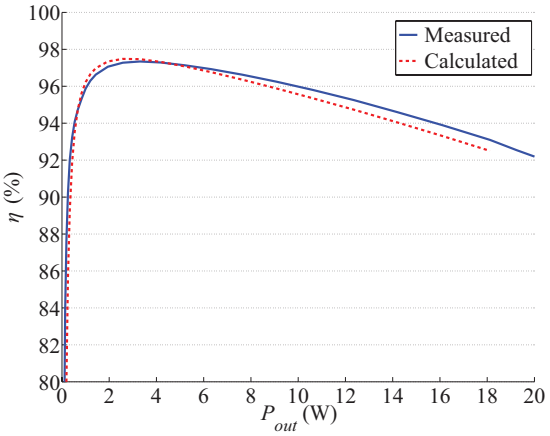
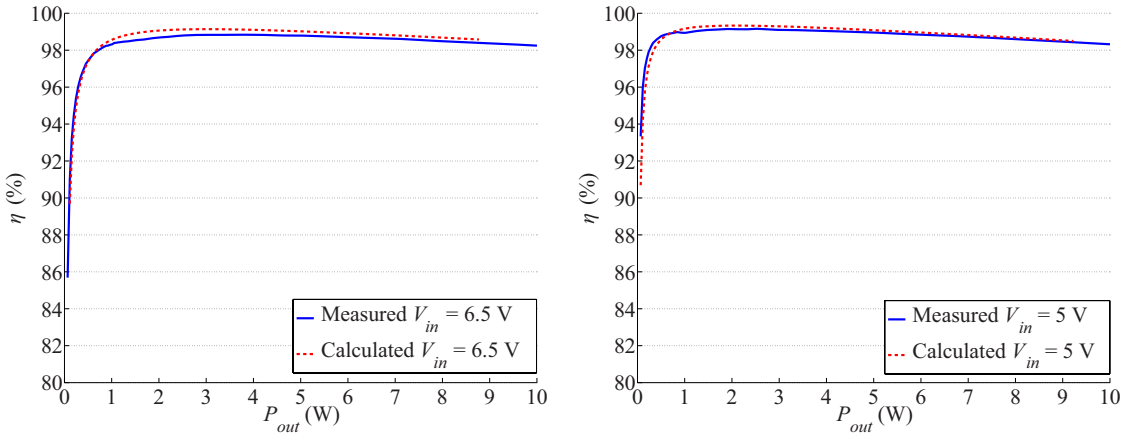


Fig. 11: Measured and calculated efficiency curves of the battery to LED power flow.



(a) (b)

Fig. 12: Measured and calculated efficiency curves of the PV to battery power flow. (a) $V_{in} = 6.5$ V (b) $V_{in} = 5$ V.

to full output power, which proves the reutilization of the primary winding of the low capacitive coupled inductor structure in a high efficient buck converter stage. Moreover, as can be seen in Fig. 12b, the efficiency of this power flow is further increased under low input voltage condition due to the reduced capacitive losses and current stress. As it can be observed, the stage presents an efficiency over 99% from 1.2 W to 4 W output power.

As shown in Fig. 2a and Fig. 2b, low irradiation level on the PV panel corresponds to low voltage operation at the input of the converter. The designed PV to battery stage fulfill the target of high efficiency operation at low irradiation conditions. Moreover, the LED driver stage achieves high efficiency operation at low current drive of the LED lamp. Therefore, the proposed low-power LtL structure achieves high efficiency operation in both power flow paths.

Conclusion

This paper presents a TPC topology for stand-alone low-power PV-LED systems, where no direct solar conversion is required. The key design guidelines of the LtL system are discussed and a detailed loss distribution analysis is performed. A measurement of the semiconductor switching energy loss is carried out, which allows accurate calculation of the converter switching losses. An experimental prototype is constructed and the efficiency measurements show very good match with the loss calculation, which ver-

ifies the performed loss breakdown analysis. In locations far from the Equator, solar powered systems are challenging due to low irradiation, and therefore, low generated power. The proposed solution features low component number and reutilization of the magnetic component whilst achieving high efficiency in both power flow paths. At low input voltage, which corresponds to low irradiation level, the PV to battery power flow shows a peak efficiency of 99.1% at 1.5 W output power. The tapped boost LED driver stage presents a peak efficiency of 97.3% at 3 W output power.

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Power Flow Control of a Dual-Input Interleaved Buck/Boost Converter with Galvanic Isolation for Renewable Energy Systems

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Power Flow Control of a Dual-Input Interleaved Buck/Boost Converter with Galvanic Isolation for Renewable Energy Systems

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***Abstract*— DC microgrids or nanogrids have attracted increasing research interest in recent years. Therefore, as a critical component, dc-dc converters with multiple inputs are required. In this paper, a dual-input interleaved buck/boost converter is proposed and its corresponding power flow control methods are analyzed and designed accordingly. Furthermore, the design guidelines are discussed. Finally, in order to verify the validity of this study, the measurement results are presented.**

Keywords—Dual-input; isolated; interleaved buck/boost; renewable energy systems; energy storage; power flow control.

I. INTRODUCTION

Renewable energy sources have become an important part of energy production. The application of clean and renewable energy sources, such as wind energy, solar energy and hydrogen, in dc microgrids or nanogrids has been a focus in academia and industry [1], [2], [3]. However, due to intermittent feature of wind and solar sources, wind power and photovoltaic (PV) systems need energy storage units to balance electricity generation and consumption within a power system, which has a high wind/solar energy penetration. In order to fulfill various system requirements, many hybrid system configurations and converter topologies have been proposed and investigated as reviewed in [4]. In order to combine several input power sources two approaches are usually adopted: multiple-converter systems and multiple-port systems. On the one hand, multiple-converter systems are formed by connecting the input sources by individual dc-dc converters. This system configuration offers some advantages such as easier implementation of the power management and control scheme. However, it presents the disadvantage of higher number of components and, consequently, low power density and high cost. On the other hand, multiple-port or multiple-input converters (MIC) [5], [6], [7] have recently been introduced and have attracted increased research interest. In these topologies, the common characteristic is the shared output stage by the different input ports, reducing the cost by reducing the number of components, and increasing the system efficiency and power density. However, the control and power management system tend to become more complex. Some of the proposed MIC do not allow bidirectional operation [8], [9], as the input ports are completely decoupled, and therefore they cannot be used in systems requiring of energy storage units.

Systems interconnecting a renewable energy source and an energy storage unit are usually known as dual-input converters or three-port converters (TPC) [10], [11]. In such a system, the mismatch power is handled by the energy storage unit, which will absorb the surplus energy at light load and will supply the energy deficit at heavy load conditions. Therefore, different power flows can take place depending on the power of the renewable energy source and load consumption.

Based on the previous research [12], in this paper, a dual-input interleaved buck/boost converter with galvanic isolation is proposed. The schematic of the circuit topology is presented in Fig. 1. The proposed converter consists of two interleaved bidirectional buck/boost converters, one transformer, an ac inductor and one full-bridge diode rectifier. Switches S_1 and S_2, as well as S_3 and S_4, have complementary gate signals with a deadband. The ac inductor, L_{ac}, is the power interface element between the two inputs and the output port. In order to decouple the two power inputs as well as to effectively regulate the output voltage, a duty cycle plus phase-shift control strategy [13], [14] is adopted. The duty cycle of the primary side switches is used to control the power flow between the two independent sources, i.e. V_{in1} and V_{in2}. The phase-shift angle between the middle points of the interleaved half-bridges is employed to regulate the output voltage accordingly. Compared to the topologies investigated in [13] and [15], for the proposed converter, due to the absence of output inductors, there is neither freewheeling current nor reactive power transferring back and forth to the power input. Therefore, higher conversion efficiency than other investigated solutions can be expected.

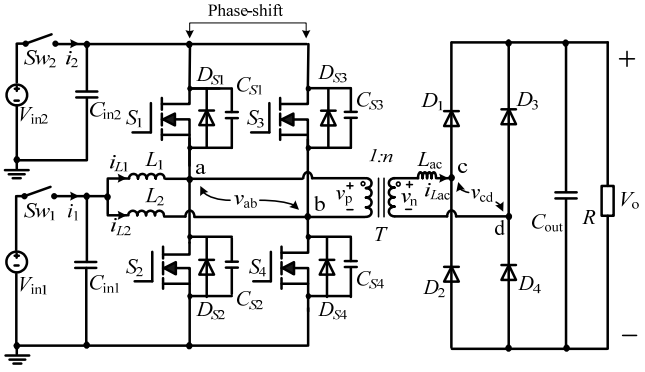

Fig 1. Topology of the interleaved Buck/Boost converter.

II. Power Flow Regulation And Control

Different power flows can occur subject to the input power and load consumption. The converter will operate in dual input (DI) mode when the load power is higher than the available input power, so the battery has to deliver the extra required energy. The converter will operate in dual output (DO) mode when the input power is higher than the load power and the battery has to store the excess energy. The system can also operate in single input single output (SISO) mode, when power transfers between the inputs or from one of the inputs to the output port. According to the control variable and the direction of the power flow, the proposed converter can operate in different modes as explained below.

A. Duty cycle control mode

Power transfers only between the two inputs V_{in1} and V_{in2}, and there is no power delivered to the output. The duty cycle, D, is the control parameter while the phase-shift angle φ is kept at π. In this mode, the voltage relationship of V_{in1} and V_{in2} can be expressed accordingly,

$$V_{in2} = \frac{V_{in1}}{(1-D)} \tag{1}$$

where D is the duty cycle of the low side switches S_2 and S_4.

B. Phase-shift control mode

One input is completely powered off and only the other input supplies power to the load. Based upon the typical operating waveforms, which are depicted in Fig. 2, the output power in this mode can be calculated as,

$$P_o = \frac{2\cdot(2V_{in1}-V_o)\cdot V_{in1}}{f_s\cdot L_{ac}}\cdot\left(\frac{\varphi}{2\pi}\right)^2 \qquad (0<\varphi<\pi) \tag{2}$$

where φ is the phase-shift angle of S_2 and S_4.

C. Duty cycle plus phase-shift control mode

Switches S_{w1} and S_{w2} are turned on and both of the inputs can deliver power to the load. In order to decouple the two inputs effectively as well as regulate the output voltage accurately, both the duty cycle and the phase-shift angle are used as the control variable. Therefore, the power flowing between the inputs and the power delivered to the load are controlled by D and φ, respectively.

The typical operating waveforms are shown in Fig. 3 where $\varphi/2\pi < \min[D, (1-D)]$. The equivalent circuits in each time interval are presented in Fig. 4. During the first subinterval, shown in Fig. 4 (a), switches S_2 and S_3 are conducting and switches S_1 and S_4 are off. The upper point of the transformer, V_a, is zero and the voltage applied to the transformer primary side is negative and determined by the input voltage source V_{in2}. The inductor current i_{Lac} flows to the load through diodes D_2 and D_3. During time interval t_1 to t_2, switch S_3 turns off and S_4 turns on, as shown in Fig. 4 (b). The voltage applied to the transformer is clamped at zero and the inductor current discharges through diodes D_2 and D_3 to the output. The equivalent circuit during time interval t_2 to t_3 is shown in Fig. 4 (c). The voltage on the transformer is still clamped to zero and the energy to the load is supplied by the output capacitor. At time t_3, switch S_2 turns off and switch S_1 turns on. The voltage applied to the transformer is positive and determined by V_{in2}. At the secondary side, the power is transferred to the load through diodes D_1 and D_4. It can be observed that the phase-shift determines the time interval from 0 ~ t_1 and the duty cycle defines the time interval from 0 ~ t_3. The output power can be calculated as shown in (3).

$$P_o = \begin{cases} \dfrac{m(m-1)V_o^2}{L_{ac}f_s}\cdot\left(\dfrac{\varphi}{2\pi}\right)^2, & \dfrac{\varphi}{2\pi} \le \min[D,1-D] \\ \dfrac{m(m-1)V_o^2}{L_{ac}f_s}\cdot D^2, & D<\dfrac{\varphi}{2\pi}<0.5 \\ \dfrac{m(m-1)V_o^2}{L_{ac}f_s}\cdot(1-D)^2, & 1-D<\dfrac{\varphi}{2\pi}<0.5 \end{cases} \tag{3}$$

$$m = \frac{nV_{ab}}{V_{cd}} = \frac{nV_{in1}}{(1-D)V_o} = \frac{nV_{in2}}{V_o} \tag{4}$$

From (3), it can be noticed that the phase-shift angle can only regulate the output power if the condition shown in (5) is satisfied.

$$\frac{\varphi}{2\pi} > 1-D \ \ (D>0.5) \text{ and } \frac{\varphi}{2\pi} > D \ (D<0.5) \tag{5}$$

On the other hand, when the converter is supplied with a constant input voltage and connected to a constant resistive load, changing the phase-shift angle will lead to a variable m. In this condition, the output voltage varies as a function of phase-shift angle and the duty cycle as shown in Fig.5.

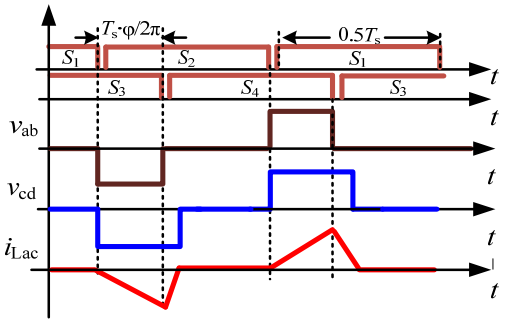

Fig. 2. Operating waveforms in phase-shift control mode.

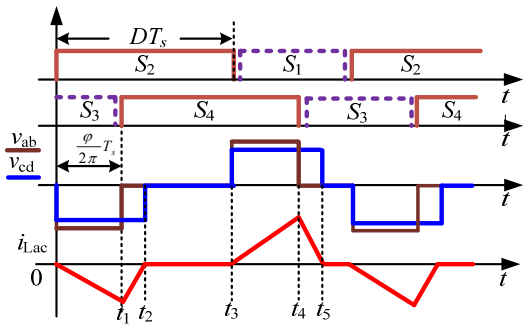

Fig. 3. Operating waveforms in duty cycle plus phase-shift control mode.

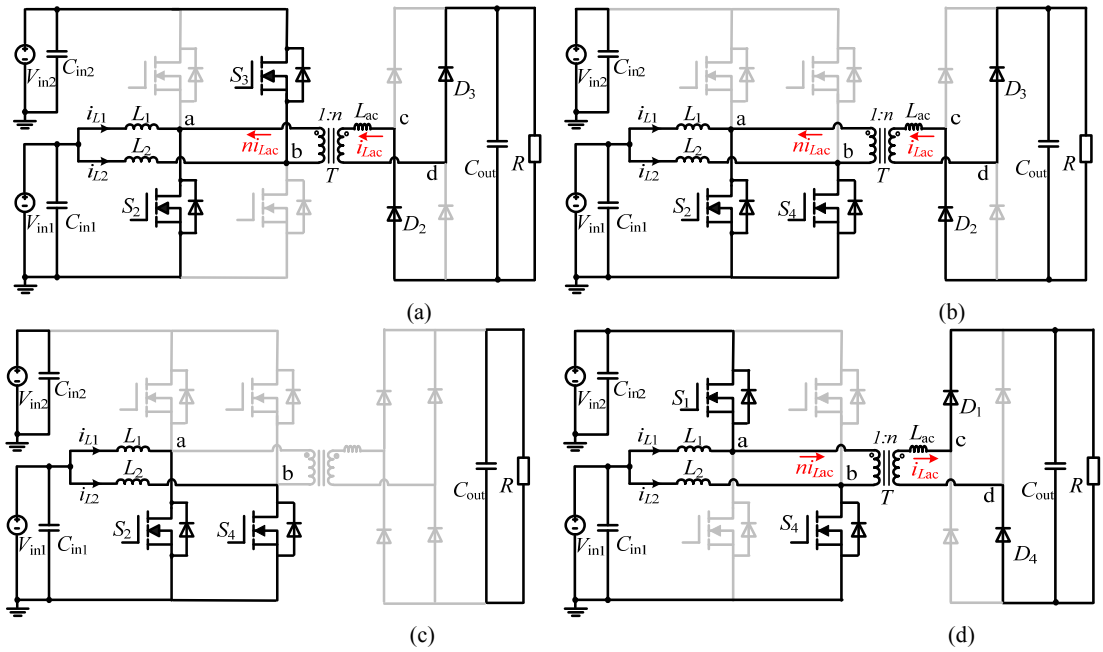

Fig. 4. Equivalent circuits in duty cycle plus phase-shift control mode. (a) Interval [0~t_1], (b) interval [t_1~t_2], (c) interval [t_2~t_3], and (d) interval [t_3~t_4].

III. Design Guidelines

A. No-reactive power operation

In order to achieve the operation without reactive power, which means ac current i_{Lac} and voltage v_{cd} are in phase, the inequality below must be satisfied.

$$\frac{(1-D)^2 \cdot V_o}{nV_{in1}} = \frac{(1-D)\cdot V_o}{nV_{in2}} \geq \frac{\varphi}{2\pi} \tag{6}$$

B. Soft-switching constraints

To ensure operation of zero voltage switching (ZVS) at turn on, current flowing through MOSFETs $S_1 \sim S_4$ must be negative when the corresponding MOSFET is triggered. Therefore, the voltage across the MOSFET is clamped by the forward biased voltage of its body diode. As the waveforms shown in Fig. 3, where $\varphi/2\pi < (1-D)$ and $D > 0.5$, when the input V_{in1} provides power to the load, the MOSFET S_2 in the leading half-bridge cannot operate under ZVS. However, MOSFET S_4 in the lagging half-bridge can achieve ZVS if the constraints depicted in Fig. 6 are satisfied. Due to the operation principle of buck/boost converters, the high side switches S_1 and S_3 can operate under ZVS inherently.

C. Current stress over switches

Due to the absence of output inductors, the MOSFETs always switch off the current at its peak. Consequently, the current stress is relatively high, which leads to high switching losses. On the other hand, when V_{in1} provides power to the load, the current stress has imbalanced distribution among the power MOSFETs.

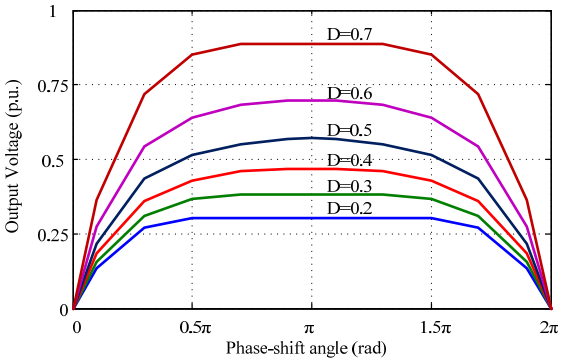

Fig. 5: Output voltage as a function of phase-shift angle with different m and D.

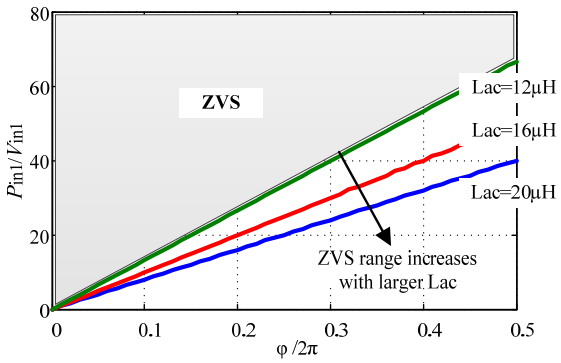

Fig 6. ZVS range with V_{in2} = 100 V and V_o = 380 V.

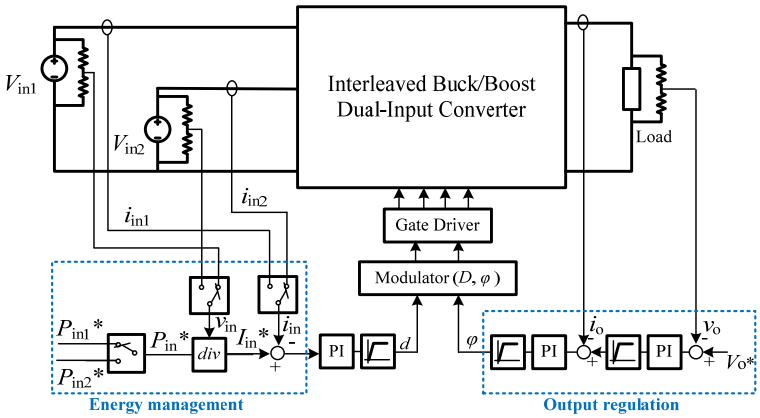

Fig 7. Block diagram of energy/power management and control.

D. Energy / power management and control

In order to control the power among the two inputs and the load, the block diagram of the designed power management and feedback controller is shown in Fig. 7. The output regulation loop is employed to regulate the load voltage by the phase-shift angle φ. Assuming V_{in1} is the renewable energy source such as fuel cell or photovoltaic, its power is controlled by the duty cycle D. The power from the other input V_{in2} as an energy storage unit, for example a battery or a super capacitor bank, can be controlled dependently. The energy management and control scheme can be summarized in the following way. On the one hand, if both of the input sources are available, the multi-terminal switches are set to control the input power of the renewable source, i.e. by a maximum power point tracking (MPPT) algorithm, and the storage unit will compensate for the power difference automatically. On the other hand, if the renewable energy source is not available, i.e. during night time in the case of solar energy, the multi-terminal switches are set to control the power of the energy storage unit. Finally, the state of charge (SOC) of the energy storage can be regulated as well. If the SOC of the energy storage is below its maximum, the multi-terminal switches are set to P_{in2}, V_{in2} and I_{in2} and the storage unit is charged by V_{in1} until it reaches its maximum SOC. At this moment, switch S_{w2} will be turned off and the load will be supported only by the renewable source V_{in1}.

IV. Experimental Results

To verify the theoretical analysis above, an experimental prototype of the dual-input interleaved buck/boost converter has been constructed. The transformer is implemented with planar magnetics as it can be observed from the laboratory prototype shown in Fig. 8. The system specifications and the components used in the prototype are presented in Table 1. MOSFETs $S_1 \sim S_4$ are driven by gate drivers IR2110.The current at the input and output ports are measured with Hall effect current transducers LEM LA55-P, LA25-NP, respectively. The sensed signals are low pass filtered to avoid noise at the inputs of the analog-to-digital converter (A/D). A 32 bit digital signal processor (DSP) TMS320F28035 is used to generate the corresponding PWM gate signals and phase-shift angle. The used control law is an assembly (ASM) function included in the library API for Piccolo B (C2803x). This control law implements a digital controller named 2P2Z optimized for minimal time delay calculation. The A/D converter is triggered when the PWM1A counter register is equal to zero, the sampled value is then given to the 2P2Z controller and the corresponding duty cycle and/or phase-shift values are calculated as a function of the reference, the sampled values and the digital controller parameters.

In order to test bidirectional capability of the input ports, the set-up is configured to simulate the behavior of an energy storage unit, i.e. a super capacitor or battery bank. This is carried out with a power supply parallel-connected with an electronic load configured in constant voltage (CV) mode.

TABLE I
SYSTEM SPECIFICATIONS AND COMPONENTS

Input voltage	V_{in1_max} = 60 V V_{in2_max} =120 V
Maximum output power	P_{out_max} = 1.5 kW
$S_1 \sim S_4$	IRFB4115 (150 V/104 A)
$D_1 \sim D_4$	HFA08TB60 (600 V/8 A)
Transformer T	4:16, ELP64/10/50 Ferrite N87
Inductors L_1 and L_2	55 µH N41 gapped RM12 core
Inductor L_{ac}	20 µH Coilcraft 1228D
Capacitors C_{in1} and C_{in2}	2 × 10 µF 160 V WIMA MKP4 3 × 22 µF 63 V AV MKT
Capacitor C_{out}	2 × 10 µF 700V VISHAY MKP
Switching frequency	60 kHz
Digital controller	TMS320F28035 DSP

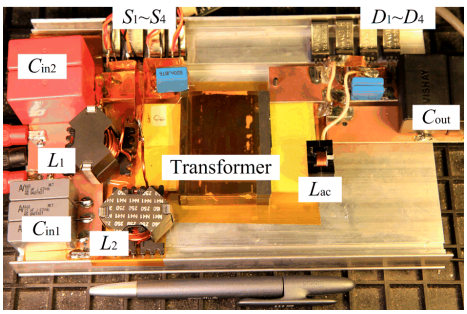

Fig. 8. Experimental laboratory prototype.

Figure. 9 shows experimental waveforms of the voltages V_{ab} and V_{cd} toghether with the ac inductor current. It can be observed that the experimental waveforms can match their theoretical counterparts shown in Fig. 3.

The performance of the implemented energy management system and control loops is verified by different experimental measurements. Fig. 10 to Fig. 15 show the input current of both of the converter input ports, I_{in1} and I_{in2}, in green and blue lines, respectively, as well as the load current, I_o, in red. Fig. 10 shows a step change in the reference of the input current I_{in1} when the converter is operating in SISO mode and it changes to DO mode. At first, the current at the bidirectional port, I_{in2}, is zero and the load is supplied only by the renewable source P_{in1}. An increment in the available power makes the energy storage port to start absorbing the energy surplus, while the power at the output remains constant. Fig. 11 shows a step change in the reference of the input current I_{in1} when the converter is operating in DI mode. As it can be observed, in this mode both of the inputs are delivering power to the output. If a variation in the available power occurs, the power between the inputs is immediately balanced, while the power at the output remains constant. Fig. 12 and Fig. 13 show a load step when the converter operates in DI mode. If the input power of the renewable source is controlled, i.e. by a maximum power point tracking (MPPT) algorithm, and there is a request of energy by the load, the bidirectional port automatically compensates the load energy demand, while the input current of the renewable source is kept constant. In Fig. 12, at first the converter is working in SISO. When there is an energy demand from the load, the energy storage unit starts delivering power to the load, while the power of the renewable source is kept constant. In Fig. 13, the converter is operating in DI mode, so both of the input sources deliver energy to the output. When the energy demand at the load decreases, the power at the storage unit is compensated automatically and the load is supported only by the renewable source in SISO mode. In the same way, a load step is tested when the converter operates in DO mode. In this case, the renewable energy source is delivering power to both the output and the energy storage unit. When an increment or decrement in the energy required at the output occurs, the energy storage unit balances the energy while keeping the power of the renewable source constant. The results are shown in Fig. 14 and Fig. 15, respectively.

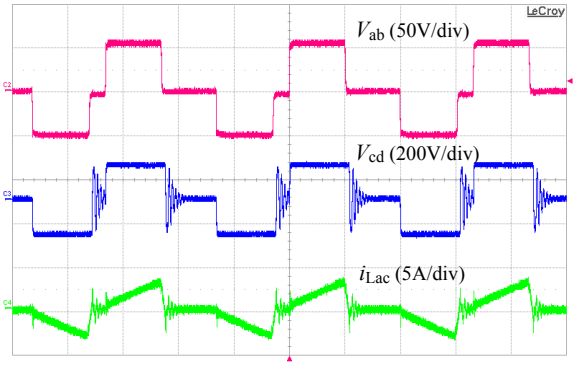

Fig. 9. Experimental waveforms of V_{ab}, V_{cd} and i_{Lac} at duty cycle $D = 0.7$ and phase-shift angle $\varphi = 0.8\pi$. Time scale: 5µs/div.

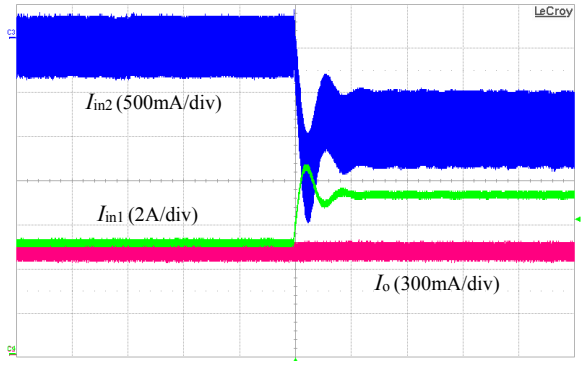

Fig. 10. Step change in the reference of the input current I_{in1} during DO mode operation of the converter. Time scale: 1.6 ms/div.

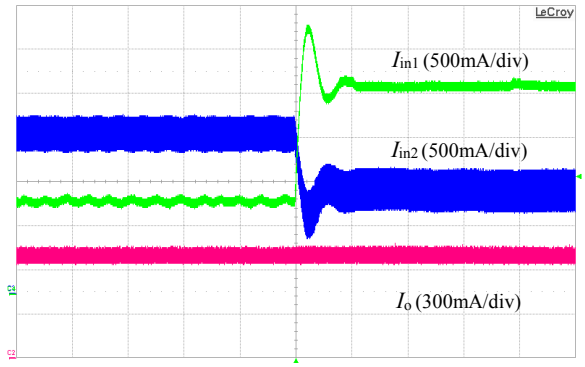

Fig. 11. Step change in the reference of the input current I_{in1} during DI mode operation of the converter. Time scale: 1.6 ms/div.

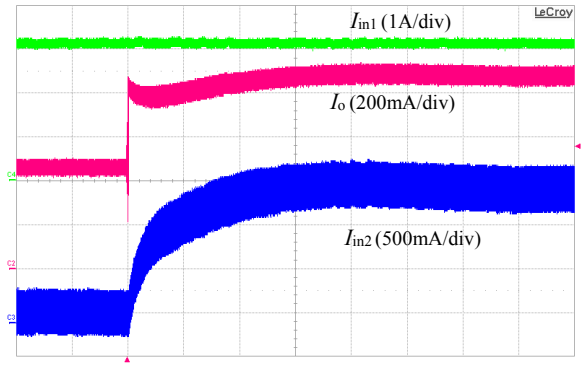

Fig. 12. Load step forcing the converter operation to change from SISO to DI mode. Time scale: 3.2 ms/div.

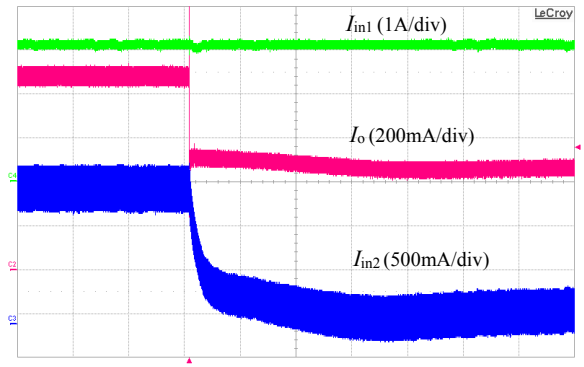

Fig. 13. Load step forcing the converter operation to change from DI mode to SISO. Time scale: 3.2 ms/div.

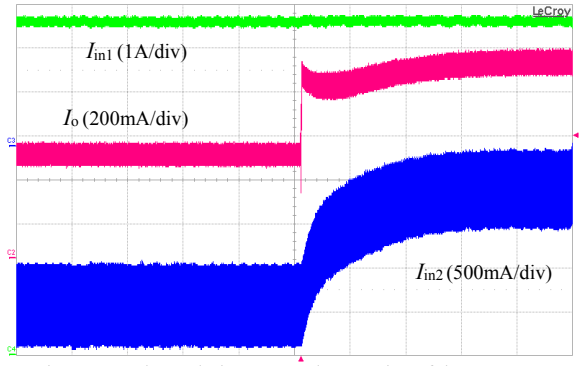

Fig. 14. Load step during DO mode operation of the converter. Time scale: 3.2 ms/div.

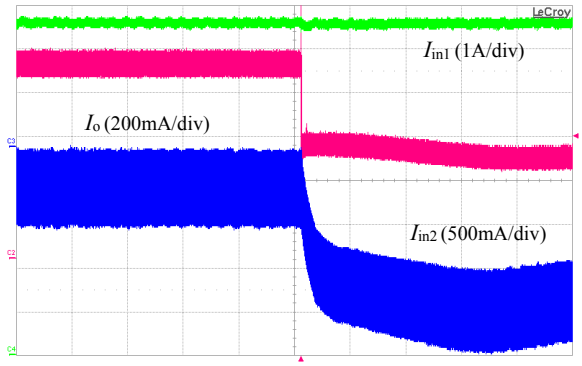

Fig. 15. Load step during DO mode operation of the converter. Time scale: 3.2 ms/div.

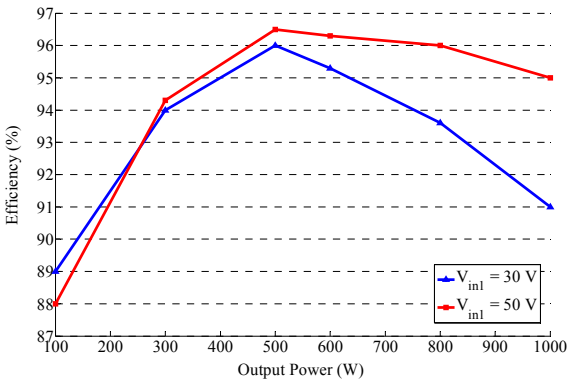

Fig. 16. Laboratoty prototype measured efficiency.

Finally, the measured efficiency curves at input voltage V_{in1} of 30 V and 50 V, respectively are given in Fig. 16. In the worst case scenario (lowest voltage and full power), the converter efficiency reaches over 91%. Compared to other topologies with similar configuration proposed in previous literature, the freewheeling current and ac reactive power are eliminated; therefore, the efficiency is improved.

V. CONCLUSIONS

In this paper, a newly proposed dual-input isolated dc-dc converter based on an interleaved buck/boost circuit is analyzed and designed. The converter shows good characteristics to be used in hybrid renewable energy systems, where an energy storage unit is required. In order to control the power flow between the different ports, duty cycle plus phase-shift control scheme is adopted. The duty cycle is used to control the power flow between the two independent sources, while the phase-shift angle is employed to regulate the output voltage. Different experimental results demonstrate that the proposed energy/power management solution achieves total control of the power flow between the input port and output ports.

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Analysis, Design, Modeling and Control of an Interleaved-Boost Full-Bridge Three-Port Converter for Hybrid Renewable Energy Systems

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Analysis, Design, Modeling and Control of an Interleaved-Boost Full-Bridge Three-Port Converter for Hybrid Renewable Energy Systems

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***Abstract*—This paper presents the design, modeling and control of an isolated dc-dc three-port converter (TPC) based on interleaved-boost full-bridge with pulsewidth modulation (PWM) and phase-shift control for hybrid renewable energy systems. In the proposed topology, the switches are driven by phase-shifted PWM signals, where both phase angle and duty cycle are controlled variables. The power flow between the two inputs is controlled through the duty cycle, whereas the output voltage can be regulated effectively through the phase-shift. The primary side MOSFETs can achieve zero-voltage switching (ZVS) operation without additional circuitry. Additionally, due to the ac output inductor, the secondary side diodes can operate under zero-current switching (ZCS) conditions. In this work, the operation principles of the converter are analyzed and the critical design considerations are discussed. The dynamic behavior of the proposed ac inductor based TPC is investigated by performing state-space modeling. Moreover, the derived mathematical models are validated by simulation and measurements. In order to verify the validity of the theoretical analysis, design and power decoupling control scheme, a prototype is constructed and tested under the various modes, depending on the availability of the renewable energy source and the load consumption. The experimental results show that the two decoupled control variables achieve effective regulation of the power flow among the three ports.**

***Index Terms*—Energy storage, phase-shift and duty cycle control, renewable energy, state-space modeling, three-port converter.**

I. INTRODUCTION

THE application of clean and renewable energy, such as solar, wind and hydrogen, has been a focus in academia and industry over the last decade [1], [2], [3]. Due to the intermittent feature of renewable energy sources, energy storage units are needed in order to balance the electricity generation and consumption within a power system having a high renewable energy penetration. Moreover, multiple energy sources hybridization can distinctly improve various aspects of system performance, such as decreasing cost, isolating energy sources from load fluctuations and enhancing the system dynamics. Hence, hybrid energy conversion systems are well suited for applications in which the average power demand is low whereas the load dynamics are relatively high [4], [5]. As a result, merging the renewable energy source elements together as a hybrid power conversion system, as well as controlling the power flows effectively has become a topic of interest.

In order to fulfill different system requirements, various hybrid system configurations and converter topologies have been proposed and investigated as reviewed in [3]. In applications where galvanic isolation is required, there are basically two categories classified as: multiple-converter conversion and multiple-port conversion. In the multiple-converter configurations, power converters are connected in parallel or in series in order to couple the energy sources and loads. By contrast, multiple-port power conversion systems can have high power density and low cost, due to the fact that some components and circuits in various power ports, such as transformers, rectifiers and output filters, can be shared as a common part along the power conversion path. Therefore, multiple-port converters have been receiving increased attention in recent years [6], [7], [8]. A general solution to obtain an isolated multiple-port converter is to adopt the magnetic coupling method, where various input power sources can be coupled with transformer windings or independent transformers [9], [10], [11]. In this solution, the multiport converter can be constructed from the basic high frequency switching cells, including the half-bridge (HB), full-bridge (FB), boost-half-bridge (BHB) and their combinations, according to the system constraints imposed by the features of the input power sources. Based upon this principle, a number of three-port (TPC) bidirectional dc-dc converters, which can

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fully isolate the various power ports and control the power flows into/out of each port, were reported in [12], [13], [14], [15], [16]. However, a large number of power switches have to be employed in those converters, resulting in increased cost and size. Besides the fully isolated multi-port topologies, partially isolated multiple-input converters, i.e. only some of the input/output ports are fully isolated, have been attracting more attention due to simple structure, less components and easy control. A dual-input dc-dc converter with BHB and FB switching cells was proposed in [17]. Two independent transformers are adopted in order to integrate both voltage-fed and current-fed power sources effectively. By combining a BHB with an LLC resonant tank, a wide-gain unidirectional two-port resonant converter is presented in [18], which can be extended to a TPC by replacing the low voltage dc bus with a voltage source. However, the control scheme to decouple the power flow will be complex due to the characteristics of the LLC circuitry. A systematic method for deriving a TPC with a diode rectifier was studied in [19], where the magnetizing inductance of an isolation transformer is utilized as a power interfacing element between the two non-isolated sources; however, this solution limits the converter's output power capability. A TPC based on an improved flyback-forward topology, with duty cycle and phase-shift control, proposed in [20], makes use of the leakage inductance of two coupled inductors to transfer power to the output port. However, in this solution the power delivering capability from the battery port to the output load is limited due to the flyback operation. Two three-port converter (TPC) topologies were proposed in [21] and [22] by integrating a boost converter into a phase-shift full-bridge buck converter, hence, the two non-isolated input ports, which connect with the renewable energy sources, are isolated from the load. After that, the topologies and their derived structures are investigated and presented in [23], [24], [25], [26]. By adopting the phase-shift with duty cycle control, the decoupled power flow can be controlled effectively among the various ports in a certain operating range. However, due to the employed output dc inductor, all the output rectifier diodes operate under hard switching condition, and suffer from high voltage stress and reverse recovery losses. Moreover, like other phase-shift zero-voltage switching (ZVS) converters, the duty cycle loss issue due to the leakage inductance still occurs. A FB TPC with duty cycle and phase-shift control derived from an interleaved boost-full-bridge (BFB) and a bridgeless boost rectifier is presented in [27]. This topology reduces the input current ripple and current stress of the input ports because of the 180° phase-shift operation of the primary switching legs. The output port regulation is achieved through the phase-shift between the primary and secondary switches. Therefore, two extra active switches in the secondary side are necessary to control the output port power flow, both with high side driver requirements, which increases the circuit complexity. Moreover, the body diode of the secondary MOSFETs operate under hard switched current conditions generating reverse recovery losses.

The goal of this work is to propose, analyze and design a TPC topology for hybrid renewable energy systems. The proposed topology, as illustrated in Fig. 1, is derived from a ZVS HB inductive dc-dc converter with an active clamped circuit [28], [29]. By replacing the clamp capacitor in the ZVS circuit with the second voltage source, an additional input port can be obtained. Compared to the topologies in [21] and [25], the rectifier diodes achieve zero-current switching (ZCS) at turn-off avoiding reverse recovery losses. Additionally, the voltage across the diodes is inherently clamped by the output capacitor C_O, therefore, voltage rings caused by the stray inductance can be eliminated. Furthermore, the secondary freewheeling current is limited due to the absence of a dc output inductor. Moreover, this converter is superior to its LLC counterparts due to lower complexity of the modulation and control. Compared to previous research on TPC topologies, modeling and analysis of dynamic performance with multiple control parameters are seldom reported. The major contribution of this paper is to analyze the relation between the two control variables, phase-shift and duty cycle, and the system dynamics based on the converter small-signal model. The derived mathematical model is verified by simulations as well as experimental measurements. Based on the small-signal model, the power flow control is designed and the converter is tested under various operation modes, i.e. dual input (DI) mode, dual output (DO) mode and single input single output (SISO) mode.

This paper is organized into seven sections: following the introduction in Section I, the topology and operation principle of the proposed converter are presented in Section II. Design considerations and the associated guidelines are given in Section III. The dynamic behavior is investigated in Section IV. The power flow regulation scheme is analyzed in Section. V. The corresponding experimental results from a laboratory prototype are provided and discussed in Section VI. As a final point, the conclusion is presented in Section VII.

II. Circuit Description and Operation Principles

The studied topology in Fig. 1 consists of two input inductors, L_1 and L_2, an ac inductor L_{ac}, four power MOSFETs $M_1 \sim M_4$, and a high frequency transformer with a turn ratio of 1: n. The ac inductor, which is the sum of the leakage inductance and the auxiliary inductance, is the power interface element between primary and secondary sides of the transformer. Switches M_1, M_2 and M_3, M_4 are driven with complementary gate signals with a deadband. V_1 and V_2 represent the input voltages; i_{L1} and i_{L2} are defined as the input inductor currents;

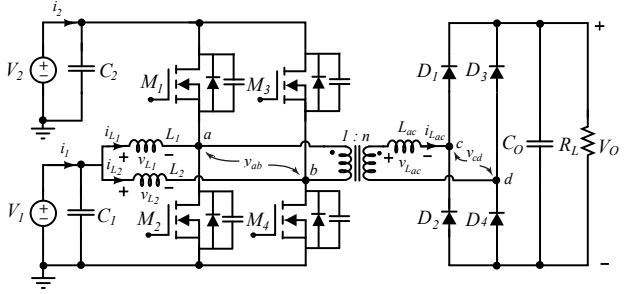


Fig. 1. Topology of the proposed TPC for hybrid renewable energy systems.

v_{ab} is the voltage between the midpoints of the bidirectional interleaved boost switching legs, and i_{Lac} is the current of the secondary side winding. In order to decouple the two inputs, V_1 and V_2, and regulate the output voltage accurately, both the duty cycle and the phase-shift angle are adopted as the control variables simultaneously. The duty cycle of the power switches is used to adjust the power among the two independent sources, and the phase-shift angle between the midpoints of the full bridge is employed to regulate the power flow to the output port.

Through the phase-shift with duty cycle control, and according to the availability of the renewable energy source and the load demand, the proposed converter can operate in various operating modes: in DI mode when the load demand is higher than the available power from the renewable energy source and the energy storage element delivers the extra energy to the load; in DO mode when the input power is higher than the load power demand and the energy storage element balances the power by storing the excess energy; and in SISO mode when power transfers between the two inputs or from one of the inputs to the output port.

For the theoretical analysis it is assumed that inductors L_1, L_2 and capacitors C_1, C_2, and C_O are big enough and the deadband effect is negligible. Due to the operation symmetry, the variation range of the phase-shift angle φ is: $0 < \varphi < \pi$. Depending on the duty cycle and its relationship with the phase-shift angle, there are three operational cases existing, based on the current shape of the ac inductor, which can be classified as completely demagnetized, partially magnetized and fully magnetized.

Fig. 2 and Fig. 3 shows the equivalent circuits during the defined time intervals and the key operating waveforms when the ac inductor current is completely demagnetized in each period. During the first subinterval, i.e. [0 ~ t_1] as shown in Fig. 2 (*a*), M_2 and M_3 are conducing simultaneously, so that L_1 and L_2 are charged and discharged, respectively. The voltage across midpoints *a* and *b* is clamped at $-V_2$, therefore, L_{ac} is charged with ($nV_{ab} - V_{cd}$). The ac inductor current is negative, as denoted in Fig. 2 (*a*), and satisfies

$$I_{Lac_{pk}} = \frac{-nV_2 + V_O}{L_{ac}} \cdot \Phi T \tag{1}$$

where the phase-shift angle normalized to the period is defined as

$$\Phi = \frac{\varphi}{2\pi} \tag{2}$$

During the interval [t_1 ~ t_2] in Fig 2 (*b*), M_4 is triggered at t_1 and L_1 and L_2 are charged. Since in this interval the voltage across the transformer, v_{ab} is clamped at zero, L_{ac} is discharged with a slope determined by the output voltage V_O. Defining β as the interval [t_1 ~ t_2] normalized to the period as in (3), the ac inductor discharge interval Δt can be calculated as shown in (4).

$$\beta = \frac{nV_2 - V_O}{V_O} \cdot \Phi \tag{3}$$

$$\Delta t = t_2 - t_1 = \beta \cdot T \tag{4}$$

When the ac inductor current reaches zero the bridge rectifier diodes stop conducting, which concludes the second subinterval.

During subinterval [t_2 ~ t_3], L_1 and L_2 will continue being charged, as represented in Fig. 2 (*c*), until M_2 is turned-off at t_3. Since the ac inductor current is completely demagnetized during the previous interval, in this state there is no power transferring from the primary side to the output port.

The equivalent circuit during interval [t_3 ~ t_4] is presented in Fig. 2 (*d*). It can be seen that the operation principle is symmetrical to that of [0 ~ t_1], thus

$$I_{Lac}(t_4) = -I_{Lac}(t_1) \tag{5}$$

From the key waveforms shown in Fig. 3, it can be observed the phase-shift value, Φ, should be smaller than the duty cycle (*D*) and the complement of the duty cycle (1 − *D*), as expressed in (6).

$$\Phi < \min\left[D,\ (1-D)\right] \tag{6}$$

Using equations (1) to (4), the output voltage of the converter can be obtained as in (7).

$$V_O = \frac{nV_2}{k} \cdot \Phi\left(-\Phi + \sqrt{\Phi^2 + 2k}\right) \tag{7}$$

where the parameter *k* is a dimensionless magnitude defined by the inductance, the output load and switching frequency as shown in (8).

$$k = \frac{2L_{ac}}{R_L T} \tag{8}$$

The relationship between V_1 and V_2 is obtained as

$$V_2 = \frac{V_1}{(1-D)} \tag{9}$$

It is noteworthy that in this operation mode the energy transferred to the output port does not directly depend on the duty cycle. Therefore, in the completely demagnetized operating mode the power flow from V_1 and V_2 to the output port will be entirely controlled by Φ.

If the inductor current i_{Lac} does not decrease to zero before M_2 is triggered, the ac current is partially magnetized, as shown in Fig. 4 (*a*). The boundary condition between completely demagnetized and partially magnetized inductor current can then be derived as

$$\Delta t + \Phi T \le (1-D)T \tag{10}$$

Substitution of (4) into (10) leads to (11).

$$\Phi \le \frac{(1-D)}{M} \tag{11}$$

where the relation between the input and output ports is defined as

$$M = \frac{nV_{ab}}{V_{cd}} = \frac{nV_1}{(1-D)V_O} = \frac{nV_2}{V_O} \tag{12}$$

In the same way, if the i_{Lac} does not reach zero before M_2 is turned off, the ac current becomes fully magnetized, as shown in Fig. 4 (*b*). As it can be observed from the inductor current shape in the key waveforms shown in Fig. 4, these operation modes, i.e. partial and fully magnetized, allow to transfer higher power to the output than the completely demagnetized counterpart. However, during the time intervals in which the inductor current does not reach zero, [0 ~ t_1] in the partially magnetized mode and [0 ~ t_1] and [t_3 ~ t_4] in the fully

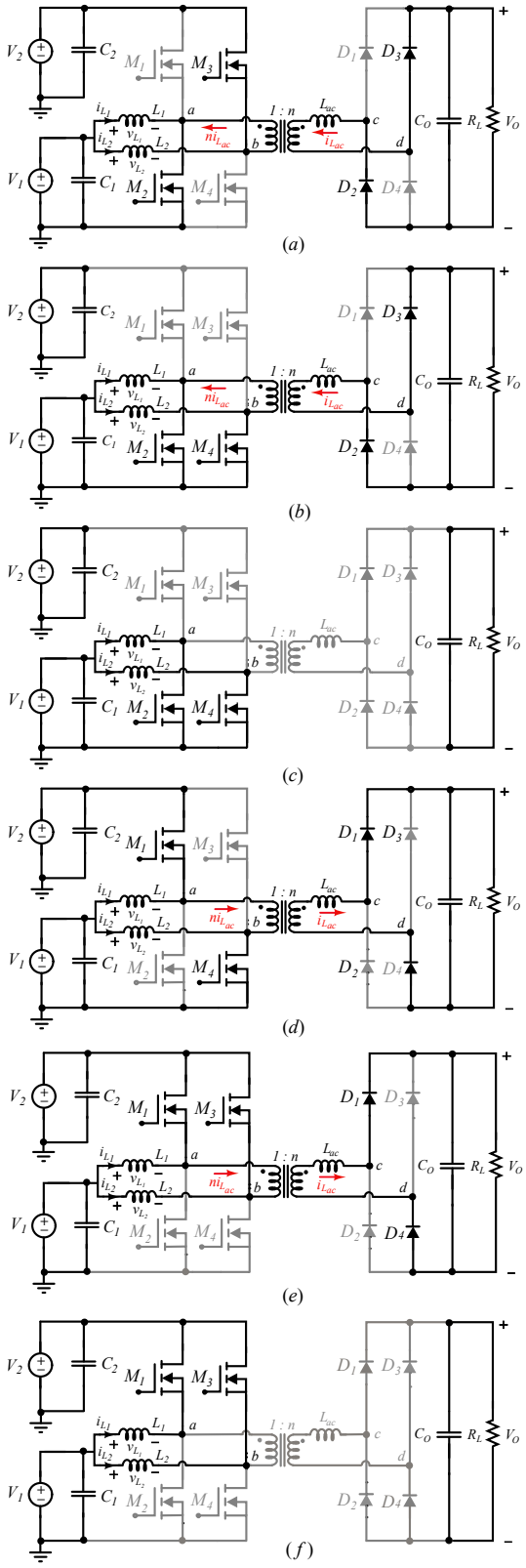


Fig. 2. Equivalent operating circuits for completely demagnetized output inductor current (left): (*a*) time interval [0 ~ t_1], (*b*) time interval [t_1 ~ t_2], (*c*) time interval [t_2 ~ t_3], (*d*) time interval [t_3 ~ t_4], (*e*) time interval [t_4 ~ t_5] and (*f*) time interval [t_5 ~ t_6].

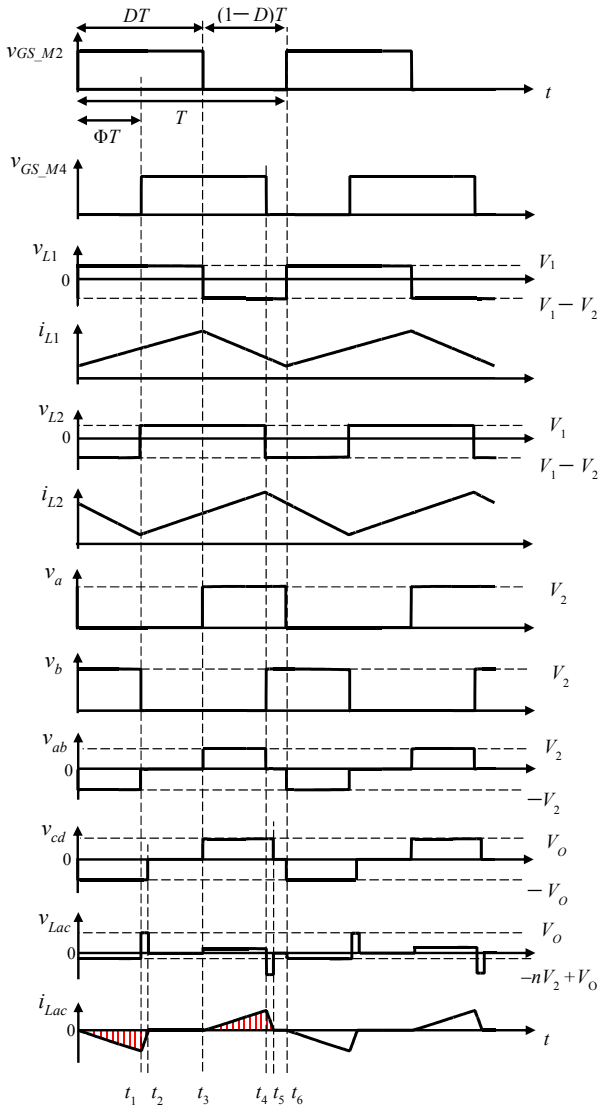


Fig. 3. Completely demagnetized ac inductor current key operating waveforms.

magnetized mode, the same current flowing through the ac inductor is flowing in the primary side and therefore, sent back to the source V_2. Therefore, when the input voltage and the inductor current are not in phase reactive power is generated, which results in higher current stress in the converter primary side and, therefore, higher losses than in the completely demagnetized operating mode.

As performed in the completely demagnetized operation mode, the partially and fully magnetized operation modes can be analyzed by describing the converter operation intervals. By solving the equation relating the average of the rectified inductor current (13) and the load current (V_O/R_L), the output voltage of the converter operating in partially magnetized operation mode can be obtained.

$$I_{Lac_{rec},avg} = \frac{V_O \Phi \left(\Phi (1-D) \left(M^2 - 2M - 1 \right) - \Phi^2 - (1-D)^2 \right)}{L_{ac} f \left(M + 1 \right)^2} \quad (13)$$

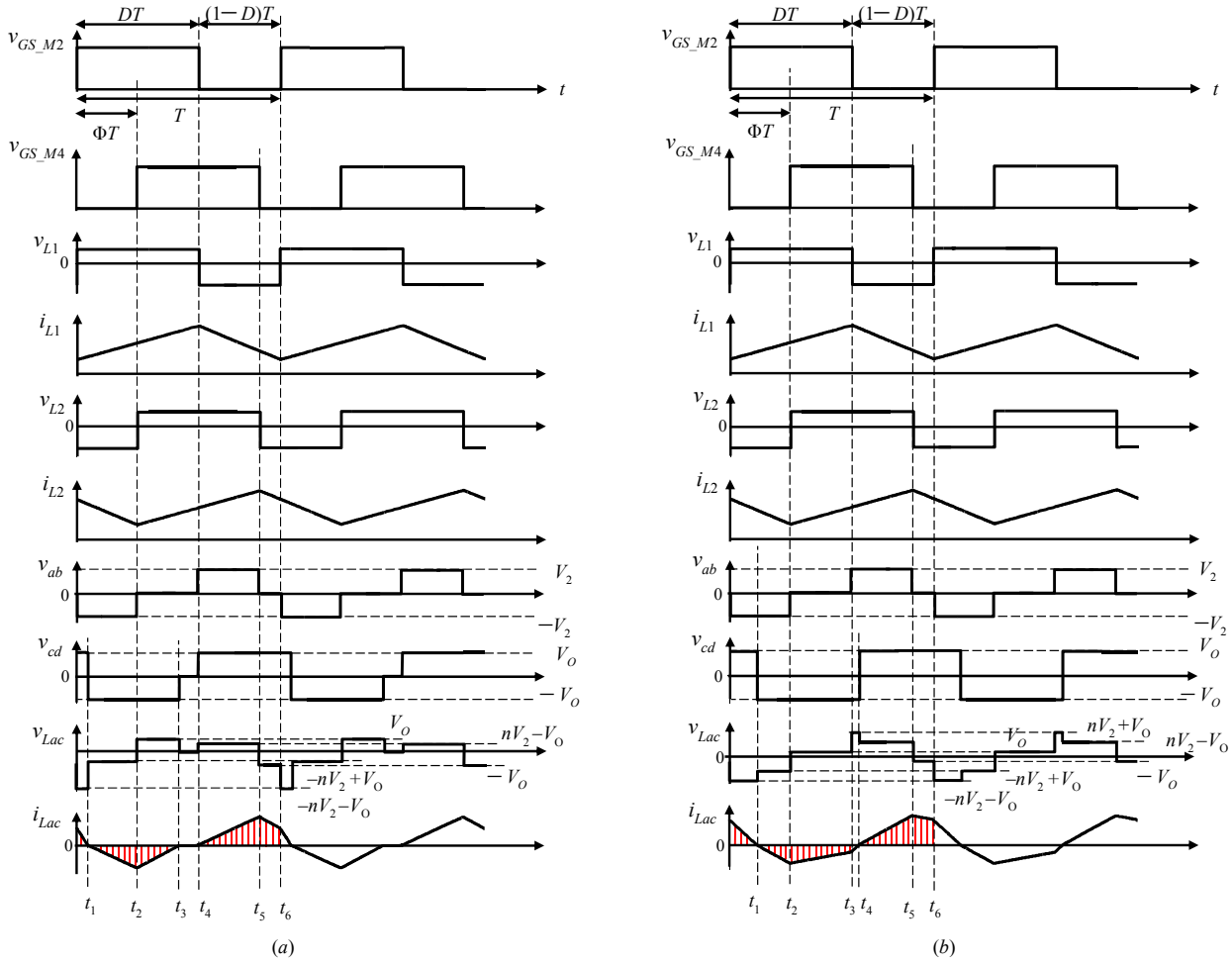


Fig. 4. (*a*) Partially magnetized ac inductor current key operating waveforms. (*b*) Fully magnetized ac inductor current key operating waveforms.

The time intervals corresponding to the fully magnetized operating mode can be calculated according to the waveforms shown in Fig. 4 (*b*), by solving the system of equations formed by the ac inductor volt-second balance and the rectified ac inductor current. By defining the interval [0 ~ t_1] normalized to the period as shown in (14), the time intervals as a function of the phase-shift and the duty cycle parameters can be written as

$$\alpha = \frac{1}{4}\cdot\left(2D+2\Phi+2k-\sqrt{4D(1-D)+4\Phi(1-\Phi)+4k^2-1}\right) \quad (14)$$

$$t_1 = \alpha\cdot T \quad (15)$$

$$t_2 - t_1 = (\Phi-\alpha)\cdot T \quad (16)$$

$$t_3 - t_2 = (D-\Phi)\cdot T \quad (17)$$

$$t_4 - t_3 = \left(\alpha - D + \frac{1}{2}\right)\cdot T \quad (18)$$

$$t_5 - t_4 = \left(\Phi - \alpha + D - \frac{1}{2}\right)\cdot T \quad (19)$$

$$t_6 - t_5 = (1-D-\Phi)\cdot T \quad (20)$$

The output voltage as a function of the phase-shift value and the duty cycle can be calculated by

$$V_O = nV_2\left(-2k+\sqrt{4D(1-D)-4\Phi(1-\Phi)+4k^2-1}\right) \quad (21)$$

Partially and fully magnetized operation allow for higher power transfer for the same inductor value than the completely demagnetized mode. This is due to the increased charge per switching cycle delivered to the output capacitor, which can be observed in the highlighted area of the ac inductor current shown in Fig. 4 (*a*) and (*b*) compared to the completely demagnetized inductor current shown in Fig. 3. However, as discussed before, these operating modes move the current stress from the converter secondary to the primary side due to the generated reactive power, which acts in detriment of the efficiency in step up applications. Moreover, as it can be seen by comparing (7) and (21), when the converter leaves the completely demagnetized mode, the converter output voltage is no longer controlled solely by the phase-shift angle. This characteristic increases the difficulty in the implementation of the dual power flow converter control strategy. Considering all the aforementioned characteristics, completely demagnetized ac inductor current is the preferred operation mode.

III. Design Considerations

In this section, design guidelines about the soft-switching operation and the *rms* current distribution of the primary switches for the completely demagnetized operation mode are discussed.

A. Soft-Switching Constraints

The proposed converter, unlike the conventional phase-shift full-bridge ZVS converter, has a relatively more complicated ZVS performance to analyze due to the input inductor currents i_{L1} and i_{L2}. ZVS can be deduced on the precondition that the anti-parallel diode of the MOSFET must conduct before the MOSFET is triggered. In other words, the main devices are turned-off with a positive current flowing and then the current diverts to the opposite diode, which allows the in-coming MOSFET to be switched-on under zero voltage condition. Therefore, the current flowing through MOSFETs $M_1 \sim M_4$ must be negative when the corresponding MOSFET is triggered. Taking into account the amount of stored energy in the MOSFETs' output capacitance (C_{OSS}), in order to obtain ZVS at turn-on the following relationships must be satisfied

$$\begin{cases} I_{L1,max} - ni_{Lac}(t_3) > I_{min} & \text{for } M_1 \\ I_{L1,min} - ni_{Lac}(t_0) < I_{min} & \text{for } M_2 \\ I_{L2,max} + ni_{Lac}(t_4) > I_{min} & \text{for } M_3 \\ I_{L2,min} + ni_{Lac}(t_1) < I_{min} & \text{for } M_4 \end{cases} \tag{22}$$

where

$$I_{Li,max} = \frac{P_1}{2V_1} + \frac{V_1(1-D)T}{2L_i} \quad (i=1,2) \tag{23}$$

$$I_{Li,min} = \frac{P_1}{2V_1} - \frac{V_1(1-D)T}{2L_i} \quad (i=1,2) \tag{24}$$

$$I_{min} = \sqrt{\frac{(2\cdot C_{OSS})\cdot V_2^2}{L_{ac}}} \tag{25}$$

As the waveforms shown in Fig. 4, where $\Phi < (1-D)$ and $D > 0.5$, when the input V_1 provides power to the load, M_2 in the leading half-bridge cannot operate under ZVS. However, M_4 in the lagging half-bridge can achieve ZVS if the constraints depicted in Fig. 5 are satisfied. As it can be observed in Fig. 5, as the power flow to the output port increases, the turn-on condition of M_4 moves towards the ZVS region due to the increased negative ac inductor peak current. However, increasing the power flow from the input port V_1 to the bidirectional port V_2 has the opposite effect due to an increased $I_{L2,min}$ value. It is important to observe the influence of the input inductor and ac inductor values on the switch ZVS region. Increasing both of the inductor values reduces the ZVS region, since $I_{L2,min}$ increases due to a reduced input inductor ripple current, and $ni_{Lac}(t_1)$ decreases for larger ac inductor values. Regarding the high side switches M_1 and M_3, since they operate as synchronous rectifiers in the interleaved boost stage, both can operate under ZVS inherently, because the reflected ac inductor current, $ni_{Lac}(t_3)$, is equal to zero and $ni_{Lac}(t_4)$ is always positive.

A significant advantage of the proposed TPC topology is that the diodes on the secondary side can operate under ZCS conditions. As it can be observed in Fig. 3 and Fig. 4, the output bridge rectifier always changes its conduction state (edges of the waveform v_{cd}) when the ac inductor current reaches zero for all operating conditions. Therefore, due to the use of an ac inductor, the diodes on the secondary side always turn-off under ZCS conditions, which avoids the reverse recovery losses and makes it possible to use conventional silicon (Si) diodes.

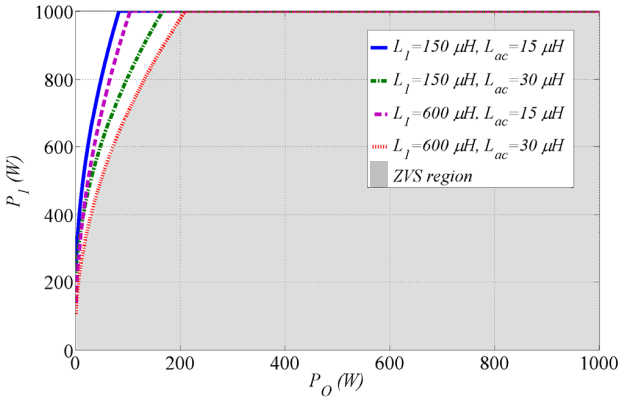


Fig. 5. ZVS range (operating conditions V_1 = 50 V, V_2 = 100 V and V_O = 380 V).

B. Selection of MOSFETs and Diodes

Like all half-bridge boost derived converters, the current distribution in the primary side MOSFETs is unequal. In the proposed converter the analysis on the *rms* current distribution is more complex due to the variable phase-shift angle. If $\varphi = \pi$, the *rms* current of the MOSFETs can be calculated by,

$$I_{M1,rms} = I_{M3,rms} = \sqrt{nI_{Lac,rms}^{\ 2} - I_{L1,rms}^{\ 2}} \tag{26}$$

$$I_{M2,rms} = I_{M4,rms} = \sqrt{nI_{Lac,rms}^{\ 2} + I_{L1,rms}^{\ 2}} \tag{27}$$

According to the operating waveform of i_{Lac} shown in Fig. 3 and (1) – (4), the *rms* value of the ac inductor current can be obtained as

$$I_{Lac,rms} = I_{Lac_{pk}}\sqrt{\frac{2}{3}(\Phi+\beta)} \tag{28}$$

where $I_{Lac_{pk}} = I_{Lac}(t_4) = |I_{Lac}(t_1)|$ is given in (1).

Fig. 6 shows the switches' *rms* current as a function of duty cycle D. It can be found that for $\varphi = \pi$, M_2 and M_4 have the maximum *rms* current (worst case for M_2 and M_4), whereas M_1 and M_3 have the minimum *rms* current. Also, it can be observed that when $\varphi \neq \pi$, the current distribution will be more equal than the case $\varphi = \pi$. This phenomenon must be considered when choosing components and deciding thermal design for the proposed converter.

The current flowing through the diodes on the secondary side is distributed equally, and the average current in each diode can be calculated as

$$I_{D_1,D_4,avg} = I_{D_2,D_3,avg} = \frac{1}{2}\cdot I_{Lac_{pk}}\cdot(\Phi+\beta) \tag{29}$$

According to the operation principle analysis, the voltage stress over the MOSFETs is the maximum voltage of V_2. The voltage stress across the diodes is the maximum output voltage owing to the voltage clamp effect by the output capacitor.

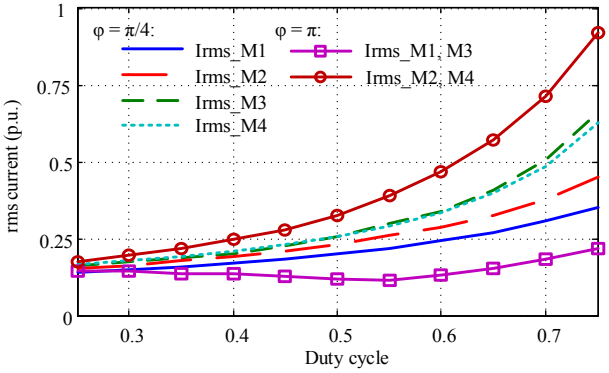


Fig. 6. Switches' *rms* current as a function of duty cycle *D*.

IV. State-Space Modeling

In this section, state-space average modeling of the proposed TPC is presented. This technique to modeling switching dc-dc converters [30], which results in a dynamic linear model in terms of state-space equations, is used in this work. Due to the inherent sampling process of switched-mode converters, averaged models can accurately predict the behavior up to half of the switching frequency [31]. If precise modeling beyond the switching frequency is required, i.e. in self-oscillating control schemes, a discrete-time approach for modeling switched-mode controllers can be used [32].

From the key operating waveforms illustrated in Fig. 3, it can be observed that the ac inductor charge and discharge always depends on the converter input voltage V_2, the converter output voltage V_O and the phase-shift angle, whereas voltages V_1 and V_2 are regulated by the duty cycle. Therefore, the proposed topology can be dynamically modelled as two individual converters: a bidirectional interleaved boost converter, which balances the power flow within the two input sources, and a phase-shift full-bridge converter or single active bridge converter, which delivers the power to the load through the ac inductor. As a result, the proposed converter offers independent controllability by using duty cycle and phase-shift as control variables, and reutilizes the primary side switches to regulate the two power flows. The high integration of the two structures in a TPC results in a topology with lower component number and higher power density than multiple-converter systems. Moreover, as previously discussed, in the completely demagnetized case the energy transferred to the output port does not depend on the converter duty cycle; therefore, the two control variables, phase-shift Φ and duty-cycle D, are completely decoupled. Fig. 7 shows the integration of the bidirectional interleaved boost converter (BIBC) and the phase-shift full-bridge (PSFB) converter as a TPC topology.

As previously discussed, the completely demagnetized operation is the preferred operation mode, however, the converter can enter any of the other operating modes depending on the two input port voltages, the duty-cycle requirement and the output port loading conditions. Therefore, in order to ensure stability of the converter under all possible operating conditions, the dynamic modelling in the fully magnetized mode is also investigated.

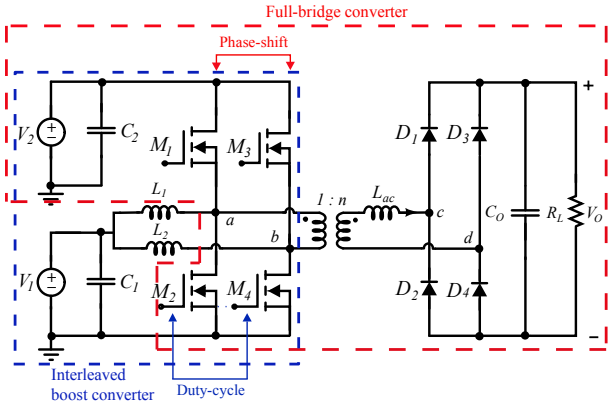


Fig. 7. Integration of the interleaved boost converter and phase-shift full-bridge converter as a TPC.

A. State-Space Modeling of the Phase-Shift Full-Bridge (PSFB) Converter

State-space average modeling of the phase-shift full-bridge (PSFB) converter is performed in this section. First, the completely demagnetized operating mode is analyzed. The rectified ac inductor current and the output capacitor voltage are selected as state-variables, i.e. $x = [i_{L_{ac}}\ v_{C_O}]^T$. Fig. 8 shows the voltage and current across the ac inductor during the different switching states, together with the rectified ac inductor current. The state and input matrices are averaged over a period by multiplying them by the corresponding time interval. As shown in Fig. 3, there are six conduction states; however, since the state-variable is the rectified ac inductor current, the charge and discharge of the ac inductor during time intervals $[0 \sim t_1]$ and $[t_1 \sim t_2]$ is equivalent to time intervals $[t_3 \sim t_4]$ and $[t_4 \sim t_5]$, as shown in Fig. 8. Notice that because two control variables are used, duty cycle and phase-shift, time intervals $[t_2 \sim t_3]$ and $[t_5 \sim t_6]$ are not the same since they are related to D and $(1 - D)$, respectively.

The system is perturbed around a quiescent operating point $(X + \hat{x},\ \Phi + \hat{\Phi},\ \beta + \hat{\beta},\ V_2 + \hat{v}_2)$ where $X \gg \hat{x}$, and linearized by neglecting the second order terms. Separating the dc and ac part of the linearized model, the steady-state operating point (30) and the small-signal model (31) are obtained.

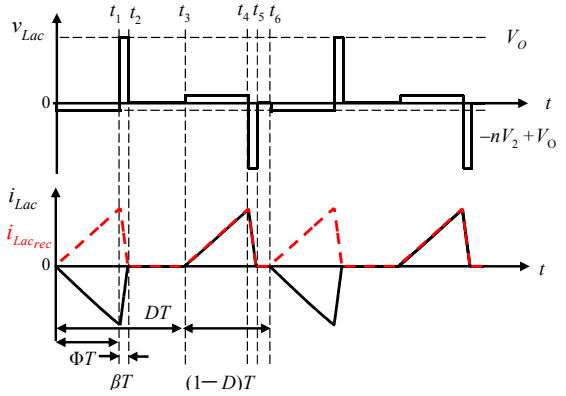


Fig. 8. Voltage and current across the ac inductor L_{ac} (continuous) and rectified ac inductor current (dashed) in completely demagnetized operation mode.

$$X=\begin{bmatrix} I_{Lac} \\ V_{C_O} \end{bmatrix} = -A^{-1}BV_2 = \begin{bmatrix} \dfrac{nV_2\Phi}{2R_L(\Phi+\beta)^2} \\ \dfrac{nV_2\Phi}{\Phi+\beta} \end{bmatrix} \tag{30}$$

$$\dot{\hat{x}} = A\hat{x} + B\hat{v}_2 + \left[\left(2A_4 - 2A_6\right)X + \left(2B_4 - 2B_6\right)V_2\right]\hat{\Phi} + \\ + \left[\left(2A_5 - 2A_6\right)X + \left(2B_5 - 2B_6\right)V_2\right]\hat{\beta}$$

$$\dot{\hat{x}} = \begin{bmatrix} 0 & -\dfrac{2(\Phi+\beta)}{L_{ac}} \\ \dfrac{2(\Phi+\beta)}{C_O} & -\dfrac{1}{C_O R_L} \end{bmatrix}\hat{x} + \begin{bmatrix} \dfrac{2n\Phi}{L_{ac}} \\ 0 \end{bmatrix}\hat{v}_2 + \\ + \begin{bmatrix} \dfrac{2nV_2\alpha}{L_{ac}(\Phi+\beta)} \\ \dfrac{nV_2\Phi}{C_O R_L(\Phi+\beta)^2} \end{bmatrix}\hat{\Phi} + \begin{bmatrix} -\dfrac{2nV_2\Phi}{L_{ac}(\Phi+\beta)} \\ \dfrac{nV_2\Phi}{C_O R_L(\Phi+\beta)^2} \end{bmatrix}\hat{\beta} \tag{31}$$

where the averaged state and input matrices are given by

$$A = 2A_4\Phi + 2A_5\beta + A_6\left(1-(2\Phi+2\beta)\right) \tag{32}$$

$$B = 2B_4\Phi + 2B_5\beta + B_6\left(1-(2\Phi+2\beta)\right) \tag{33}$$

$$A_4 = \begin{bmatrix} 0 & -\dfrac{1}{L_{ac}} \\ \dfrac{1}{C_O} & -\dfrac{1}{R_L C_O} \end{bmatrix} \quad A_5 = \begin{bmatrix} 0 & -\dfrac{1}{L_{ac}} \\ \dfrac{1}{C_O} & -\dfrac{1}{R_L C_O} \end{bmatrix}$$

$$A_6 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{R_L C_O} \end{bmatrix} \tag{34}$$

$$B_4 = \begin{bmatrix} \dfrac{n}{L_{ac}} \\ 0 \end{bmatrix} \qquad B_5 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \qquad B_6 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

The discharge parameter β is defined in (3) and the phase-shift value Φ s given by

$$\Phi = \frac{V_O}{\sqrt{2}}\sqrt{\frac{-k}{nV_2(V_O - nV_2)}} \tag{35}$$

In order to obtain the dynamic model of the converter in the completely demagnetized mode, additional constrains need to be applied. The first constraint comes from the fact that the inductor current becomes zero for a portion of the switching period. Applying the constraint defined in (36) to the ac model presented in (31), leads to (37). As a result, the inductor dynamic equation turns into a static equation, as shown in (38), meaning that the ac inductor current does not behave as a true state-space variable since it losses its dynamic properties [33].

$$\frac{d\hat{i}_{Lac}}{dt} = 0 \tag{36}$$

$$\hat{\beta} = \frac{-(\Phi+\beta)}{V_O}\hat{v}_O + \frac{n\Phi}{V_O}\hat{v}_2 + \frac{nV_2\beta}{V_O(\Phi+\beta)}\hat{\Phi} \tag{37}$$

$$\dot{\hat{x}} = \begin{bmatrix} 0 & 0 \\ \dfrac{2(\Phi+\beta)}{C_O} & -\dfrac{2}{C_O R_L} \end{bmatrix}\hat{x} + \begin{bmatrix} 0 \\ \dfrac{n\Phi}{C_O R_L(\Phi+\beta)} \end{bmatrix}\hat{v}_2 \\ + \begin{bmatrix} 0 \\ \dfrac{nV_2}{C_O R_L(\Phi+\beta)} \end{bmatrix}\hat{\Phi} \tag{38}$$

The second constraint is obtained from the average of the inductor current as shown in (39).

$$i_{Lac} = f\left(v_2,\, v_O, \Phi,\, L_{ac},\, T\right) = \frac{i_{Lac,pk}}{2}\frac{(nV_2 - V_O)\Phi}{R_L k} \tag{39}$$

The perturbation equation is found by taking the partial derivatives of (39) as shown in (40).

$$\hat{i}_{Lac} = \frac{\partial i_{Lac}}{\partial v_O}\hat{v}_O + \frac{\partial i_{Lac}}{\partial v_2}\hat{v}_2 + \frac{\partial i_{Lac}}{\partial \Phi}\hat{\Phi}$$
$$\hat{i}_{Lac} = \frac{\Phi}{R_L k}\hat{v}_O + \frac{n\Phi}{R_L k}\hat{v}_2 + \frac{(nV_2 - V_O)}{R_L k}\hat{\Phi} \tag{40}$$

By applying the perturbation equation (40) to (38), the phase-shift-to-output voltage transfer function in completely demagnetized mode is obtained (41). As previously discussed, in this operating mode the two control variables are decoupled and, therefore, the duty cycle control parameter has no direct effect on the regulation of the output voltage.

$$G_{v_O\Phi}(s) = \left.\frac{\hat{v}_O(s)}{\hat{\Phi}(s)}\right|_{\hat{u}_2(s)=0} = \\ = \frac{nV_2 k + 2(\Phi+\beta)^2(nV_2 - V_O)}{(\Phi+\beta)} \cdot \frac{1}{sR_L C_O k + 2k + 2\Phi(\Phi+\beta)} \tag{41}$$

In the same way, the audio susceptibility or line-to-output transfer function can be calculated as shown in (42).

$$G_{v_O v_2}(s) = \left.\frac{\hat{v}_O(s)}{\hat{v}_2(s)}\right|_{\hat{\Phi}(s)=0} = \\ = \frac{n\Phi k + 2n\Phi(\Phi+\beta)^2}{(\Phi+\beta)} \cdot \frac{1}{sR_L C_O k + 2k + 2\Phi(\Phi+\beta)} \tag{42}$$

In order to ensure stability under all operating conditions, the dynamic behavior of the TPC operating in the fully magnetized mode is also investigated. This operating mode is more complex than the completely demagnetized operation since no symmetry can be applied to the ac inductor waveform, as illustrated in Fig. 9.

As in the completely demagnetized operating mode, in the fully magnetized mode the state-variables are the rectified ac inductor current and the output capacitor voltage. The dynamic equation of the capacitor C_O is expressed in terms of conservation of charge [36], [37] in order to take into account the correct charge applied to the output capacitor and accurately describe the dynamics involved in the rectified inductor current. By using the time intervals defined in (14) – (20) the input and state matrices for the six time intervals can be written as (43).

$$A_1=\begin{bmatrix}0 & -\frac{1}{L_{ac}}\\ 0 & \frac{\alpha T}{2L_{ac}C_O}-\frac{1}{R_LC_O}\end{bmatrix}\quad A_2=\begin{bmatrix}0 & -\frac{1}{L_{ac}}\\ 0 & \frac{(\Phi-\alpha)T}{2L_{ac}C_O}-\frac{1}{R_LC_O}\end{bmatrix}\quad A_3=\begin{bmatrix}0 & -\frac{1}{L_{ac}}\\ 0 & \frac{(D-\Phi)T}{2L_{ac}C_O}+\frac{(\alpha-D+1/2)T}{L_{ac}C_O}-\frac{1}{R_LC_O}\end{bmatrix}$$

$$A_4=\begin{bmatrix}0 & -\frac{1}{L_{ac}}\\ 0 & \frac{(\alpha-D+1/2)T}{2L_{ac}C_O}-\frac{1}{R_LC_O}\end{bmatrix}\quad A_5=\begin{bmatrix}0 & -\frac{1}{L_{ac}}\\ 0 & \frac{(\Phi-\alpha+D-1/2)T}{2L_{ac}C_O}-\frac{1}{R_LC_O}\end{bmatrix}\quad A_6=\begin{bmatrix}0 & -\frac{1}{L_{ac}}\\ 0 & \frac{(1-D-\Phi)T}{2L_{ac}C_O}+\frac{\alpha T}{L_{ac}C_O}-\frac{1}{R_LC_O}\end{bmatrix} \tag{43}$$

$$B_1=\begin{bmatrix}-\frac{n}{L_{ac}}\\ \frac{\alpha nT}{2L_{ac}C_O}\end{bmatrix}\quad B_2=\begin{bmatrix}\frac{n}{L_{ac}}\\ \frac{(\Phi-\alpha)nT}{2L_{ac}C_O}\end{bmatrix}\quad B_3=\begin{bmatrix}0\\ \frac{n(\alpha-D+1/2)T}{2L_{ac}C_O}\end{bmatrix}$$

$$B_4=\begin{bmatrix}-\frac{n}{L_{ac}}\\ \frac{n(\alpha-D+1/2)T}{2L_{ac}C_O}\end{bmatrix}\quad B_5=\begin{bmatrix}\frac{n}{L_{ac}}\\ \frac{(\Phi-\alpha+D-1/2)nT}{2L_{ac}C_O}\end{bmatrix}\quad B_6=\begin{bmatrix}0\\ \frac{\alpha nT}{2L_{ac}C_O}\end{bmatrix}$$

$$A=A_1\alpha+A_2(\Phi-\alpha)+A_3(D-\Phi)+A_4(\alpha-D+1/2)+A_5(\Phi-\alpha+D-1/2)+A_6(1-D-\Phi) \tag{44}$$

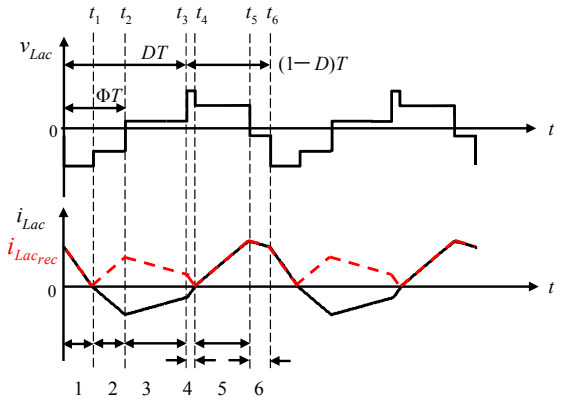
$$B=B_1\alpha+B_2(\Phi-\alpha)+B_3(D-\Phi)+B_4(\alpha-D+1/2)+B_5(\Phi-\alpha+D-1/2)+B_6(1-D-\Phi) \tag{45}$$

The state and input matrices are averaged over a period, by using the time intervals defined in (14) – (20), as shown in (44) and (45).

The system is linearized by using the Jacobian linearization as

$$\dot{\hat{x}}=A_{alt}\hat{x}+B_{alt}\hat{u} \tag{46}$$

where the Jacobian matrices (47) are defined as the derivatives of the inductor and capacitor differential equations at the linearization point (48).



1: αT 2: $(\Phi-\alpha)T$ 3: $(D-\Phi)T$ 4: $(\alpha-D+1/2)T$

5: $(\Phi-\alpha+D-1/2)T$ 6: $(1-D-\Phi)T$

Fig. 9. Voltage and current across the ac inductor L_{ac} (continuous) and rectified ac inductor current (dashed) in fully magnetized operation mode.

$$A_{alt}=\left[\begin{matrix}\frac{\partial f_1}{\partial i_{L_{ac}}} & \frac{\partial f_1}{\partial v_{C_O}}\\ \frac{\partial f_2}{\partial i_{L_{ac}}} & \frac{\partial f_2}{\partial v_{C_O}}\end{matrix}\right]_{\substack{i_{L_{ac}}=I_{L_{ac}}\\ v_{C_O}=V_O}} \tag{47}$$

$$B_{alt}=\left[\begin{matrix}\frac{\partial f_1}{\partial u_2}\\ \frac{\partial f_2}{\partial u_2}\end{matrix}\right]_{u_2=V_2}\qquad E_{alt}=\left[\begin{matrix}\frac{\partial f_1}{\partial \Phi}\\ \frac{\partial f_2}{\partial \Phi}\end{matrix}\right]_{\Phi=\Phi}$$

$$\begin{bmatrix}\frac{di_{L_{ac}}}{dt}\\ \frac{dv_{C_O}}{dt}\end{bmatrix}=\begin{bmatrix}A_{11} & A_{12}\\ A_{21} & A_{22}\end{bmatrix}\begin{bmatrix}i_{L_{ac}}\\ v_{C_O}\end{bmatrix}+\begin{bmatrix}B_1\\ B_2\end{bmatrix}u_2 \tag{48}$$

$$f_1=\frac{di_{L_{ac}}}{dt}=A_{11}i_{L_{ac}}+A_{12}v_{C_O}+B_1u_2$$

$$f_2=\frac{dv_{C_O}}{dt}=A_{21}i_{L_{ac}}+A_{22}v_{C_O}+B_2u_2$$

The state-variable-to-phase-shift transfer function is obtained as

$$G_{x\Phi}(s)=\frac{\hat{x}(s)}{\hat{\Phi}(s)}\bigg|_{\substack{\hat{u}_2(s)=0\\ \hat{d}(s)=0}}=[sI-A_{alt}]^{-1}\cdot E_{alt} \tag{49}$$

In the same way, by using (46) to (49) and calculating the partial derivatives respect to the duty cycle instead of the phase-shift, the duty-cycle-to-output voltage transfer function for the fully magnetized operation mode can be obtained.

B. State-Space Modeling of the Bidirectional Interleaved Boost Converter (BIBC)

In this section, state-space modeling of the BIBC, which operates in continuous conduction mode (CCM), is performed. The circuit diagram of the converter is shown in Fig. 10. The input ports, V_1 and V_2, interface with the renewable energy source and energy storage, respectively. Hence, the primary side of the proposed topology can be seen as an interleaved boost or buck converter depending on the direction of the power flow. In the case of a photovoltaic (PV) panel as the renewable energy source, the control variable will be taken as the converter input voltage, since the PV voltage does not present strong variations with irradiation changes [38]. In the case of a fuel cell, input current control will be selected in order to operate the fuel cell at a constant load level. Moreover, the parameters of the energy storage port can be monitored and the control scheme changed to voltage or current control on the battery depending on its state of charge (SOC).

The state-space modeling of the BIBC is performed with ideal components; nevertheless, both ports V_1 and V_2, are modelled as an ideal voltage source with a series resistance in order to account for the dynamic resistance of the renewable energy source or the energy storage element. The state-space vector is chosen as $x = [i_L \; v_{C_1} \; v_{C_2}]^T$. The converter presents two switching intervals depending on the position of the switches M_2 and M_4. The state, input, output and direct transmission matrices, A, B, C, D, respectively, for each subinterval (50), (51), are averaged over a period by multiplying by each switching interval duty cycle, (52) and expressed in terms of the state-space equation, as shown in (53) and (54).

$$A_1 = \begin{bmatrix} 0 & \frac{1}{L_1}+\frac{1}{L_2} & 0 \\ -\frac{1}{C_1} & -\frac{1}{R_1C_1} & 0 \\ 0 & 0 & -\frac{1}{R_2C_2} \end{bmatrix} \quad B_1 = \begin{bmatrix} 0 & 0 \\ \frac{1}{R_1C_1} & 0 \\ 0 & \frac{1}{R_2C_2} \end{bmatrix} \tag{50}$$

$$C_1 = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \qquad D_1 = \begin{bmatrix} 0 & 0 \end{bmatrix}$$

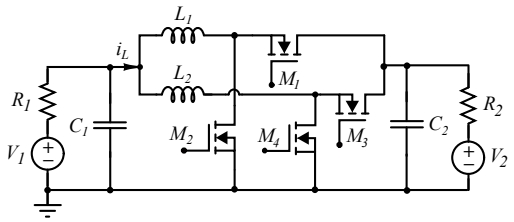


Fig. 10. Bidirectional interleaved boost converter BIBC.

$$A_2 = \begin{bmatrix} 0 & \frac{1}{L_1}+\frac{1}{L_2} & -\frac{1}{L_1}-\frac{1}{L_2} \\ -\frac{1}{C_1} & -\frac{1}{R_1C_1} & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{R_2C_2} \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 & 0 \\ \frac{1}{R_1C_1} & 0 \\ 0 & \frac{1}{R_2C_2} \end{bmatrix} \tag{51}$$

$$C_2 = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \qquad D_2 = \begin{bmatrix} 0 & 0 \end{bmatrix}$$

$$\begin{aligned} A &= A_1D + A_2(1-D) \\ B &= B_1D + B_2(1-D) \\ C &= C_1D + C_2(1-D) \\ D &= D_1D + D_2(1-D) \end{aligned} \tag{52}$$

$$\dot{x} = Ax + Bu \tag{53}$$

$$y = Cx + Du \tag{54}$$

After the perturbation and linearization, the duty-cycle to state-variable (55) and the steady-state (dc) operating point (56) are obtained. From (55), the controllers for voltage and current regulation of the renewable energy and the energy storage port can be designed accordingly.

$$\hat{x} = (sI - A)^{-1} \cdot \left[(A_1 - A_2)X + (B_1 - B_2)U \right] \tag{55}$$

$$X = -A^{-1} \cdot B \cdot U \tag{56}$$

The audio susceptibility transfer function is calculated as (57).

$$G_{v_2v_1}(s) = \left. \frac{\hat{v}_2(s)}{\hat{v}_1(s)} \right|_{\hat{d}(s)=0} = C(sI - A)^{-1} \cdot B \tag{57}$$

In the BIBC, the variation of the phase-shift angle will only affect the input current ripple; therefore, it does not have an effect on the averaged current, and consequently, on the duty-cycle-to-inductor current transfer function.

V. Power Flow Regulation and Control

The block diagram of the designed power management and feedback regulators is shown in Fig. 11. Four different controllers are designed for the energy management of the renewable power system. At the renewable energy port, either voltage or current can be selected to be regulated depending on the type of the selected renewable energy source. At the energy storage port, constant voltage (CV) and constant current (CI) regulators are implemented, and at the output port, voltage regulation is performed. In order to control the power among the two inputs and the load and thereby balance the power between the different energy sources, two control loops are active at any time. The output port regulation loop is employed to regulate the load voltage by the phase-shift angle Φ. On the other hand, assuming V_1 is the renewable energy source such as fuel cells or photovoltaics, the voltage or current is controlled by the duty cycle D. The power from the other input V_2 as an energy storage unit, for example a battery or a super-capacitor, is controlled depending on the power at the renewable energy source and the output load power

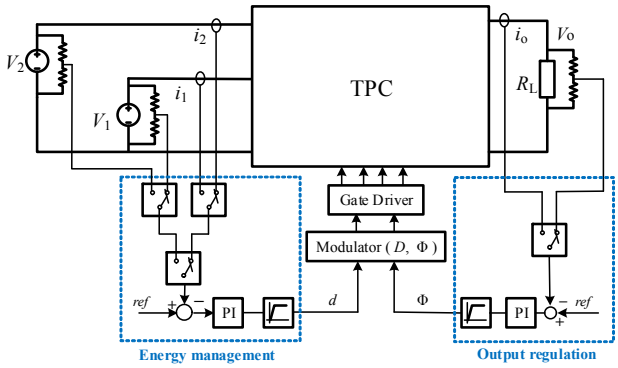


Fig. 11. Block diagram of energy/power management and control.

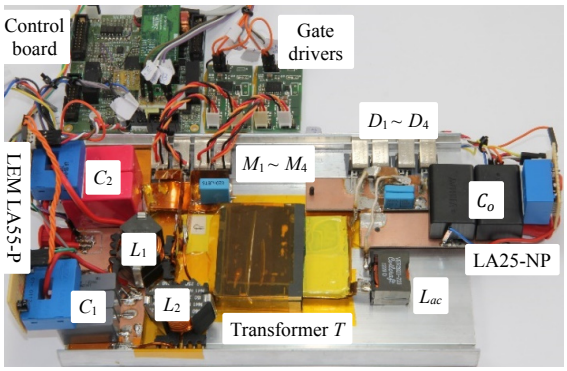


Fig. 12. Experimental prototype of the proposed TPC topology.

demand. Therefore, the energy management and control scheme can be summarized in the following way. The system is always set to control the renewable energy source and in the case of a photovoltaic application, to maximize the power delivered to the system through a maximum power point tracking algorithm (MPPT). If the renewable input power is smaller than the required power at the output port, the storage unit will compensate the power difference automatically. On the other hand, if the input power is bigger than the power required at the load terminal, the energy surplus is used to charge the energy storage element by inverting the power flow direction at this port. The state-of-charge (SOC) of the energy storage element is always being monitored and when it is above or below its recommended values, the system is set to control the bidirectional port by performing CV or CI control, until the energy storage element SOC allows for a change in the operation mode.

VI. Experimental Results

The proposed TPC has been simulated, designed, built and tested to validate the previous theoretical analysis including the derived small-signal models. Fig. 12 shows the experimental prototype of the proposed TPC topology, which is constructed with a fast prototyping technique. The converter is designed to interface with hybrid renewable energy systems, i.e operating a single phase grid-tie or as stand-alone dc microgrid power system. The specifications and the components employed in the construction of the prototype are listed in Table I. The control law is implemented by means of a digital signal processor (DSP) TMS320F28035 to generate the four gate signals with an adjustable duty cycle and phase-shift angle. The currents at the input and output ports are measured with Hall Effect current transducers LEM LA55-P, LA25-NP respectively.

Fig. 13 illustrates the measured waveforms of the PWM signal $v_{GS\text{-}M2}$ and $v_{GS\text{-}M4}$ and the two phase-shifted inductor currents i_{L1} and i_{L2}.

According to the waveforms of ZVS operation shown in Fig. 14, the drain to source voltage $v_{DS\text{-}M3}$ and $v_{DS\text{-}M4}$ have completely decreased to zero before switches M_3 and M_4 are turned-on, and there are no transient voltage spikes and rings across the switches. Therefore, the converter will have close to zero switching losses and low electromagnetic emissions.

TABLE I
System Specifications And Components

Input voltage	$V_1 = 25 - 60$ V $V_{2\,max} = 120$ V
Output voltage	$V_O = 300 \sim 380$ V
Maximum output power	$P_{Omax} = 1000$ W
$M_1 \sim M_4$	IRFB4115 (150 V / 104 A)
$D_1 \sim D_4$	HFA08TB60 (600 V / 8 A)
Transformer T	4:16, ELP64/10/50 Ferrite N87
Inductors L_1 and L_2	155 μH N41 gapped core RM12
Inductor L_{ac}	28 μH Coilcraft VER2923-223
Capacitor C_1	2 × 10 μF 160 V WIMA MKP4
Capacitor C_2	3 × 22 μF 63 V AV MKT
Capacitor C_O	2 × 10 μF 700 V VISHAY MKP
Switching frequency	$f = 60$ kHz
Digital controller	TMS320F28035 DSP

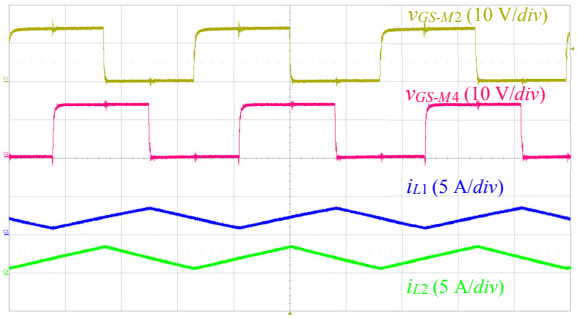


Fig. 13. Experimental results of the phase-shifted gate-source voltage of M_2 and M_4 and the inductor currents i_{L1} and i_{L2} operating in DI mode at $V_1 = 50$ V, $V_2 = 100$ V and $V_O = 370$ V, $P_O = 400$ W, $P_1 = 200$ W, $P_2 = 200$ W. Time scale: 5 $\mu s/div$.

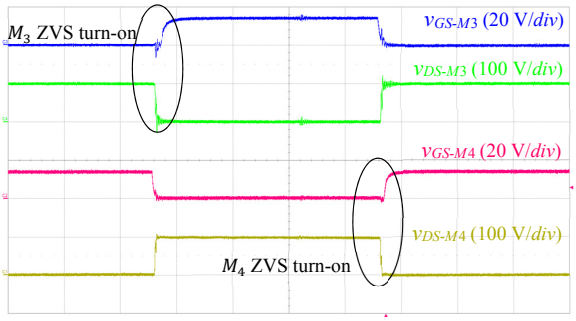
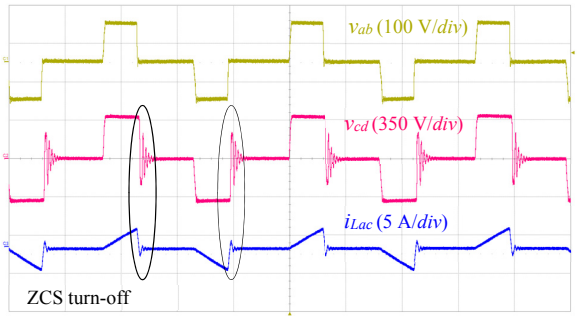
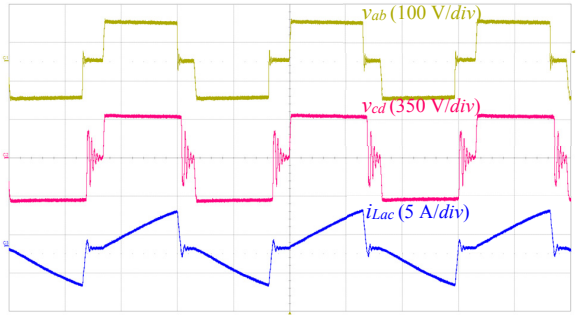


Fig. 14. Experimental results of the gate voltage and drain voltage of M_3 and M_4 at $V_1 = 50$ V, $V_2 = 100$ V and $V_O = 370$ V, $P_1 = 100$ W, $P_2 = 100$ W, $P_O = 200$ W. Time scale: 2 $\mu s/div$.



(*a*)



(*b*)

Fig. 15. Experimental results of the high frequency ac voltages v_{ab}, v_{cd} and inductor current i_{Lac} operating in DI mode at V_1 = 50 V, V_2 = 100 V and V_O = 370 V (*a*) P_O = 200 W, P_1 = 100 W, P_2 = 100 W. (*b*) P_O = 800 W, P_1 = 100 W, P_2 = 700 W. Time scale: 5 *μs/div*.

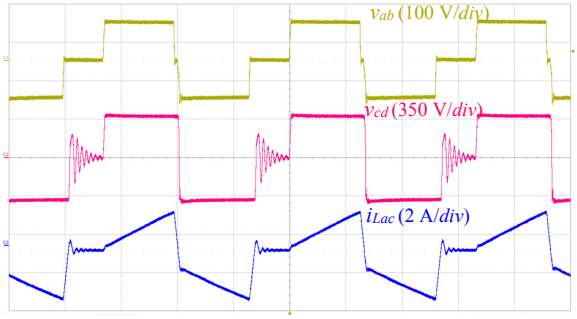


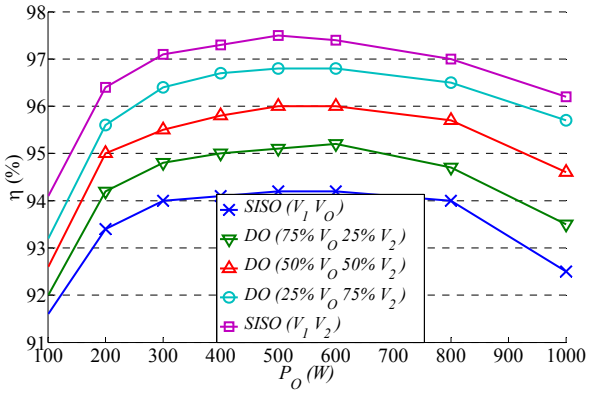
Fig. 16. Experimental waveforms of v_{ab}, v_{cd} and partially magnetized i_{Lac} operating in DI mode at V_1 = 40 V, V_2 = 100 V and V_O = 370 V, P_1 = 100 W, P_2 = 300 W, P_O = 400 W. Time scale: 5 *μs/div*.

Fig. 15 (*a*) and (*b*) shows the measured high frequency ac voltages v_{ab}, v_{cd} and inductor current i_{Lac} of the converter operating in DI mode at different output power levels, respectively. It can be found that by using the capacitor C_2 and high side switches M_1 and M_3 as an active clamp circuit, the voltage transient spike across the current-fed bridge is suppressed.

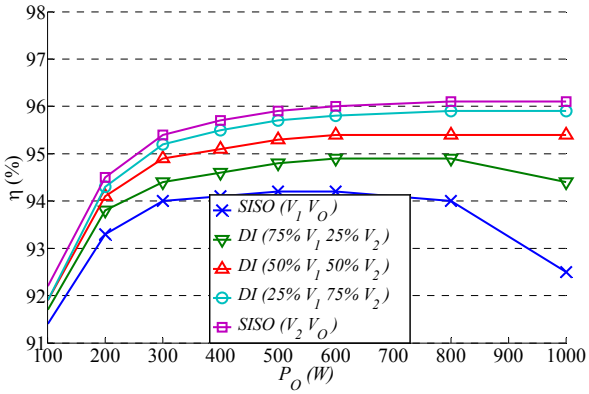
The ZCS operation of the output diodes can be observed in the high frequency ac voltage v_{Lac} and current i_{Lac} shown in Fig. 15. As discussed in section III, due to the use of an ac inductor, the output bridge rectifier always changes its conduction state when the ac inductor current reaches zero, and therefore, the diodes always turn-off under ZCS conditions. A high frequency oscillation in the ac voltage v_{cd} can also be observed in Fig. 15. As in any discontinuous conduction mode (DCM) converter operation, when the inductor current reaches zero, a resonance between the bridge rectifier parasitic capacitance and the ac inductor magnetizing inductance occurs. The energy stored in the diodes' parasitic capacitance will be dissipated in the circuit as resistive losses. This loss, independent of the converter output power, is calculated to be 16 mW, for $V_D = V_O$ = 380 V, according to the junction capacitance value given in the component's datasheet.

As an example, if a larger ac inductor is used (66 μH), the ac inductor current becomes partially magnetized. The experimental waveforms in this operating mode are presented in Fig. 16, where it can be seen that the ac inductor current does not stay at zero level before starting the next charging subinterval, as in the key operating waveform shown in Fig. 4.

Fig. 17 (*a*) and (*b*) shows the measured efficiency curves of the TPC topology operating in DI, DO and SISO modes at V_1 = 50 V, V_2 = 100 V and V_O = 370 V. The efficiency measurement is performed with the converter operating in closed loop with a dc power supply connected in parallel to an electronic load at the bidirectional port. The electronic load is configured in constant voltage (CV) mode to simulate the behavior of a battery. As it can be observed, when the converter operates in DO mode, the efficiency increases as the power flow moves from the output port (SISO V_1V_O) towards the bidirectional port (SISO V_1V_2). This is due to the fact that the energy is processed only by the non-isolated interleaved boost converter instead of being boosted to V_2 and transferred through the transformer to the output port V_O. A peak



(*a*)



(*b*)

Fig. 17. Measured efficiency curves of the converter in DI, DO and SISO modes at V_1 = 50 V, V_2 = 100 V and V_O = 370 V.

efficiency of 97.5% is achieved in SISO V_1V_2, whereas the maximum achieved efficiency in SISO V_1V_O mode is 94.2%. The same behavior is observed when the converter operates in DI mode and the operation changes from SISO V_1V_O to SISO V_2V_O. In this case, SISO V_2V_O shows higher efficiency than SISO V_1V_O due to the energy being processed once through the phase-shift isolated stage instead of being boosted from V_1 to V_2 and then transferred to the output through the isolated stage. The maximum efficiency achieved in SISO V_2V_O mode is 96.1%.

In order to validate the mathematical modeling performed in section IV, the calculated control and input transfer functions are compared to LTspice simulations [34], [35], as well as experimental measurements. The dynamic behavior of the TPC is measured with a vector network analyser (VNA) OmicronLab Bode100. Fig. 18 shows the calculated, simulated and measured phase-shift-to-output voltage transfer function of the PSFB converter operating in completely demagnetized mode under the following conditions: V_2 = 50 V, V_O = 100 V, R_L = 100 Ω, P_O = 100 W, $\Phi = 0.17\pi$. As it can be observed, the mathematical model shows very good match with the simulation and the experimental results.

As in the completely demagnetized mode, in order to validate the mathematical model of the PSFB operating in fully magnetized operation, the circuit is simulated in LTspice and the result is compared to the mathematical model, as shown in Fig. 19. The simulation and the calculation are performed under the following conditions: V_2 = 50 V, V_O = 100 V, R_L = 10 Ω, P_O = 1000 W, $\Phi = 0.74\pi$, D = 0.6. As it can be observed, in the fully magnetized mode, the system behaves as a first order system, since the inductor current dynamics contributes very little to the control-to-output transfer function. This is due to the fact that the inductor current is an ac waveform, which makes the dynamics of this state-variable only visible at high frequencies. The control-to-output transfer function in fully magnetized mode is, therefore similar to the demagnetized operation; however, in this case, the gain is reduced due to the increased output load. As observed in Fig. 19, the proposed mathematical model shows good match with the simulation results. On the other hand, the duty cycle-to-output voltage transfer function gain is several

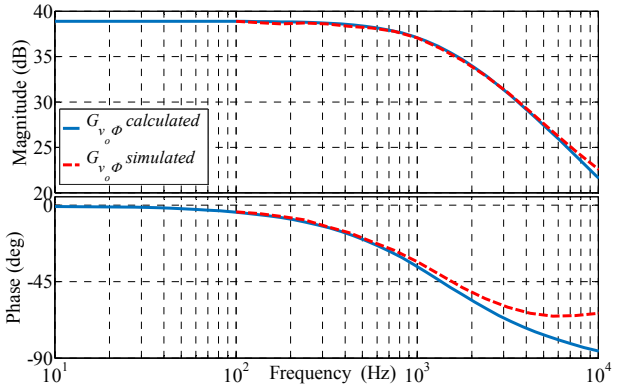


Fig. 19. PSFB fully magnetized ac inductor current phase-shift-to-output voltage ($G_{v_o\Phi}$)) transfer function calculated (continuous line) and measured (dashed line).

orders of magnitude smaller than the phase-shift-to-output voltage transfer function gain. Therefore, the perturbations on the duty cycle due to the regulation of the power flow between V_1 and V_2, will have very small effect on the regulation of the converter output voltage. Since the plant transfer function behaves similarly to the demagnetized mode, and no special consideration need to be taken into account to suppress perturbations due to variations in the converter duty cycle, it can be concluded that entering this mode will not present any stability issues.

Once the validity of the model is verified, a compensation for the PSFB converter operating in completely demagnetized mode is designed. The compensation consists of an integrator and a zero placed at the resonant frequency of the plant transfer function. Fig. 20 shows the PSFB converter calculated and measured loop-gain for the designed controller with a crossover frequency of f_c = 2.29 kHz and phase margin PM = 40°. As it can be observed in Fig. 20, the loop gain measurement presents very close match with the mathematical calculation.

As in the PSFB case, in order to validate the mathematical modeling of the BIBC duty-cycle-to-inductor current transfer measurement is performed with the converter working with a

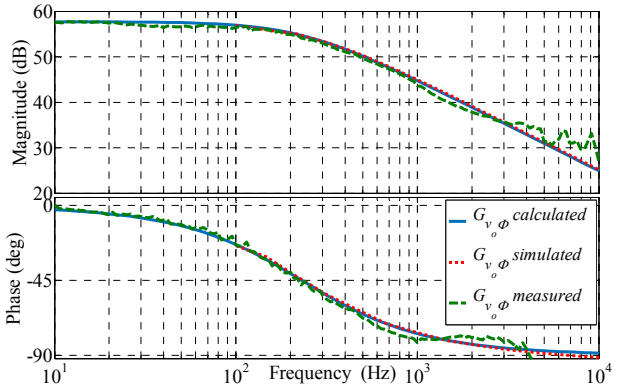


Fig. 18. PSFB completely demagnetized ac inductor current phase-shift-to-output voltage ($G_{v_o\Phi}$) transfer function calculated (continuous line), simulated (dotted line) and measured (dashed line).

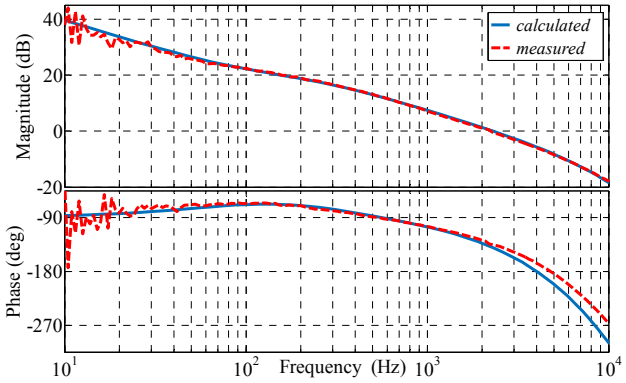


Fig. 20. PSFB completely demagnetized ac inductor current phase-shift-to-output voltage loop-gain transfer function calculated (continuous line) and measured (dashed line).

resistive load instead of with an electronic load configured in CV mode. Measuring any transfer function with an electronic load is not recommended since the control circuit of the electronic load can interfere with the converter under test. Notice that the BIBC plant transfer function differs when is operated with a battery or with a resistive load. This can be observed from the calculated and simulated duty-cycle-to-inductor current transfer function shown in Fig. 21 (*a*) for battery load, and the measured transfer function with a resistive load, shown Fig. 21 (*b*), for the same converter power level. The complex poles appearing at the converter natural resonant frequency in the resistive load case are split in the case of battery loading, which make the battery load case to behave as a first order system. Fig. 21 (*a*) shows the calculated and simulated duty-cycle-to-inductor current transfer function with a battery as a load under the following operating conditions: V_1 = 25 V, R_1 = 150 mΩ, V_2 = 50 V, R_2 = 25 Ω, I_L = 4 A, P_2 = 100 W, D = 0.513. Fig. 21 (*b*) shows the measurement of the BIBC duty-cycle-to-inductor current transfer function with resistive load under the following conditions: V_1 = 25 V, R_1 = 150 mΩ, V_2 = 50 V, R_2 = 100 mΩ, I_L = 4 A, P_2 = 100 W, D = 0.513. As it can be observed from the results presented in Fig. 21, the mathematical model shows very good match with the performed simulation and measurement. A compensation for the BIBC operating with a battery at the bidirectional port V_2 is designed. The compensation consisting of an integrator and a zero is designed and tested; nevertheless, the measurement results are not shown due to the aforementioned reasons.

The audio susceptibilities of the separate converters as well as the combination as a TPC topology are investigated. The audio susceptibility, or line-to-output transfer function, relates how variations at the input port will affect the output as a function of the frequency; hence, the interaction between the two control loops within the proposed topology can be examined. Fig. 22 (*a*) and (*b*) present the calculated and measured audio susceptibility transfer functions of the PSFB converter and the BIBC, respectively, under the conditions: V_1 = 25 V, R_1 = 150 mΩ, V_2 = 50 V, R_2 = 50 Ω, I_L = 2 A, P_2 = 50 W, D = 0.513, where a Picotest J2120 is used to inject up to 50 V input voltage and 5 A input current. As it can be observed the measurements show close match with the proposed model.

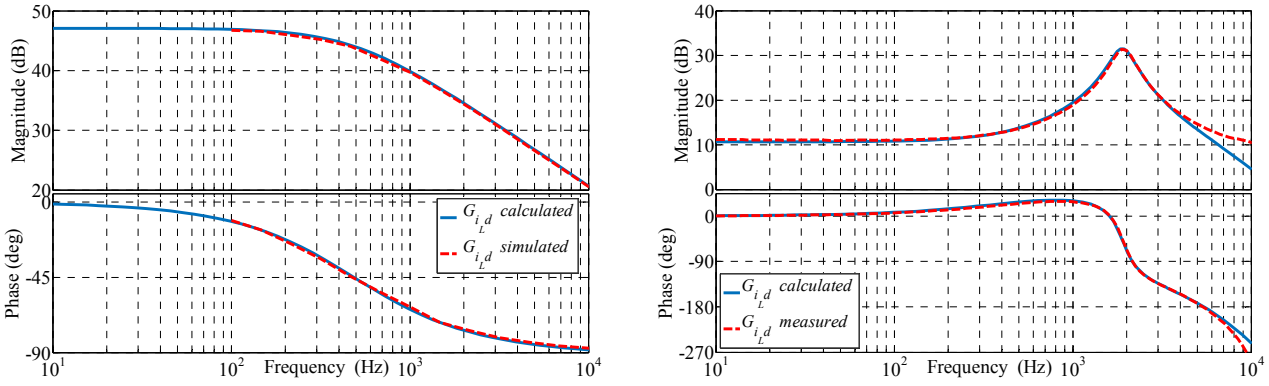


Fig. 21. BIBC duty-cycle-to-inductor current ($G_{i_L d}$) transfer function: (*a*) operated with a battery as a load calculated (continuous line) and simulated (dashed line) and (*b*) operated with a resistive load, calculated (continuous line) and measured (dashed line).

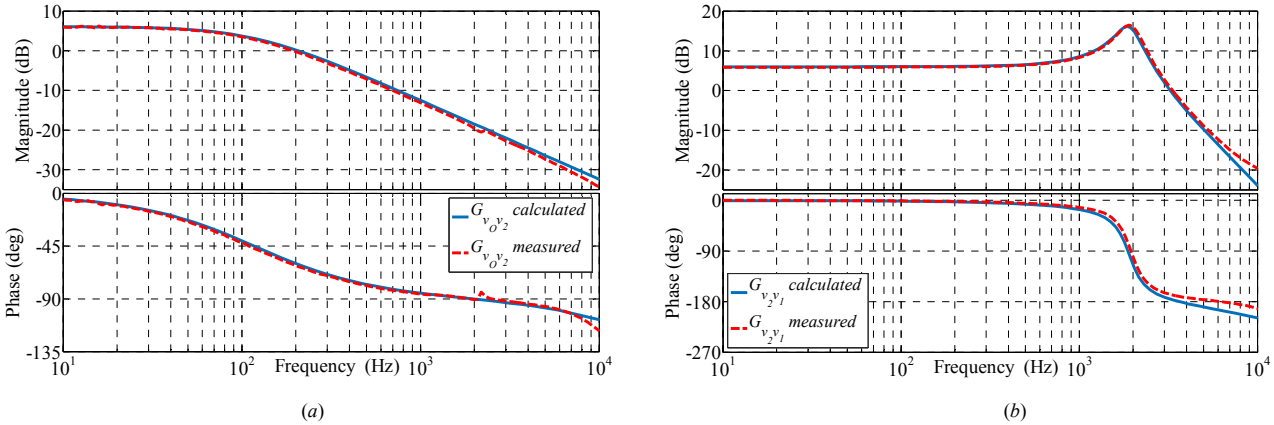


Fig. 22. Calculated (continuous line) and measured (dashed line) audio susceptibility transfer functions: (*a*) PSFB audio susceptibility ($G_{v_O v_2}$), (*b*) BIBC audio susceptibility ($G_{v_2 v_1}$).

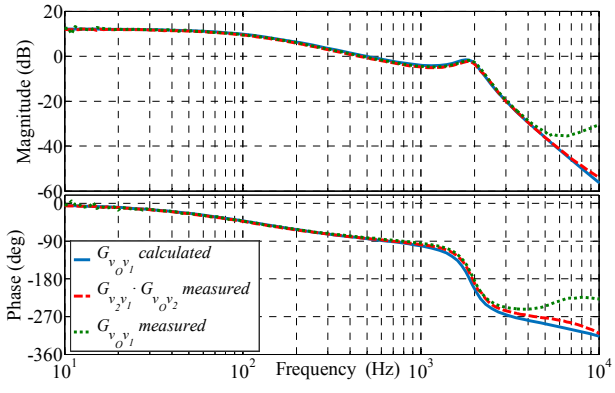


Fig. 23. Calculated (continuous line) and measured (dashed lines) TPC audio susceptibility ($G_{v_o v_1}$) transfer function.

Fig. 23 shows the calculated and measured line-to-output transfer function of the TCP (from the input port V_1 to the output port V_O), measured under the following conditions: V_1 = 25 V, R_1 = 150 mΩ, V_2 = 50 V, R_2 = 50 Ω, I_L = 2 A, P_2 = 50 W, D = 0.513, V_O = 100 V, R_L = 200 Ω, P_O = 50 W, Φ = 0.17π. The calculated transfer function is obtained as the series combination of the individual transfer functions (58).

$$G_{v_o v_1}(s) = G_{v_2 v_1}(s) \cdot G_{v_o v_2}(s) = \left.\frac{\hat{v}_2(s)}{\hat{v}_1(s)}\right|_{\hat{d}(s)=0} \cdot \left.\frac{\hat{v}_o(s)}{\hat{v}_2(s)}\right|_{\hat{\Phi}(s)=0} \quad (58)$$

As it can be observed in Fig. 23, the measurement of the audio susceptibility from the input port V_1 to the output port V_O matches with the calculated transfer function where the system dynamic behavior is modelled as two separate converters. From this measurement, it can be concluded that the converter output voltage V_O is not directly affected by perturbations on the converter input port V_1 or the duty cycle, but by the effect of these on the converter bidirectional port voltage V_2. Therefore, as discussed in the converter modeling section, from a control point of view the proposed TPC effectively behaves as two separate converters to regulate the two power flows.

The performance of the proposed energy management system and control loops is verified by different experimental measurements [39]. Fig. 24 and Fig. 25 show the input currents of both of the converter input ports, I_1 and I_2, as well as the load current, I_O, and the output voltage V_O. The converter is operating at V_1 = 50 V, V_2 = 100 V and V_O = 370 V. Fig. 24 (*a*) to (*e*) shows the transition between different operating modes due to variations of the available power at the renewable energy port, while the load demand remains constant (P_O = 250 W). Depending on the available power at the renewable energy port, the converter operating mode changes between DI mode, DO mode and SISO V_1 as illustrated in Table II. As it can be observed from the transitions shown in Fig. 24, variations of the power at the renewable energy port does not affect the voltage regulation at the output port, since the duty cycle control variable does not have an effect on the output voltage regulation when the converter operates in completely demagnetized mode.

In the same way, the transitions between different operating modes due to variations of the output port load demand are tested. Fig. 25 (*a*) to (*f*) shows the transition between different operating modes due to variations of the output power, while the power at the renewable energy port remains constant (P_1 = 250 W). Depending on the load demand, the converter operating mode changes between SISO V_1, DI mode and DO mode, as presented in Table III. As it can be observed from

TABLE II
POWER AT THE PORTS FOR TRANSITIONS BETWEEN OPERATING MODES UNDER CONSTANT OUTPUT LOAD

	SISO V_1	SISO V_2	DI	DO
$P_1(W)$	250	0	125	375
$P_2(W)$	0	250	125	-125
$P_O(W)$	250	250	250	250

TABLE III
POWER AT THE PORTS FOR TRANSITIONS BETWEEN OPERATING MODES UNDER CONSTANT POWER AT THE RENEWABLE ENERGY SOURCE

	SISO V_1	DI	DO
$P_1(W)$	250	250	250
$P_2(W)$	0	125	-125
$P_O(W)$	250	375	125

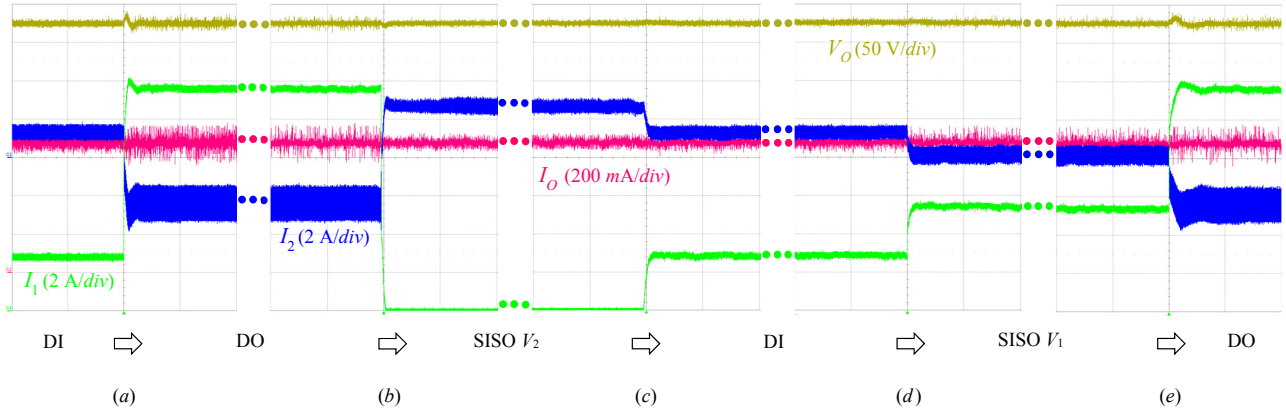


Fig. 24. Transition between different operating modes due to variations of the available power at the renewable energy port. Time scale: 20 *ms/div*.

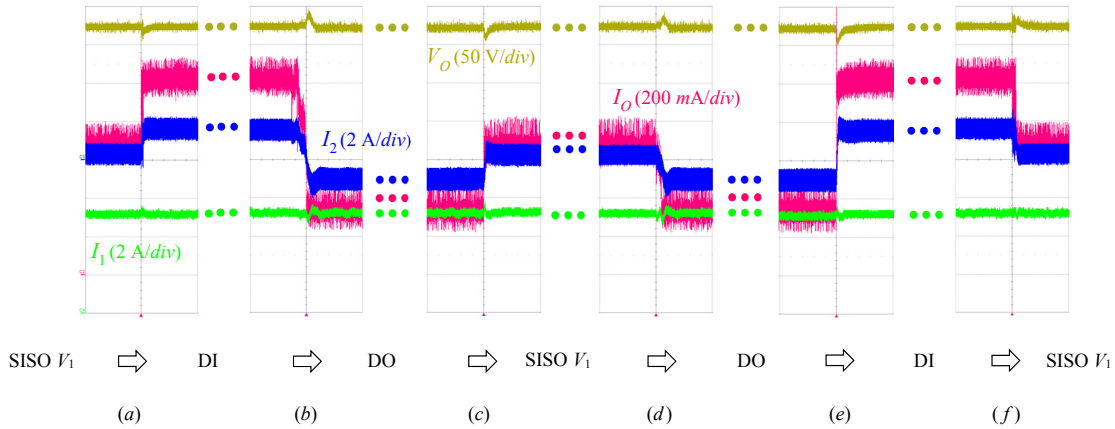


Fig. 25. Transition between different operating modes due to variations of the output port load demand. Time scale: 50 *ms/div*.

the different load steps in Fig. 25, variations of the output power do not affect the current at the renewable energy port, since the phase-shift control loop is decoupled from the duty cycle regulation that controls the power flow from the renewable energy source. Therefore, the power at the renewable energy port can be fully controlled, while the voltage at the output port is regulated, and the energy storage will compensate for the load dynamics. A disturbance in the output voltage V_O in Fig. 24 and in the input current I_1 in Fig. 25 can be observed due to the perturbation in the voltage V_2 at the bidirectional port under heavy load steps. The amplitude and dynamics of this perturbation are determined by the ability of the electronic load connected to the bidirectional port to regulate the voltage under CV operating mode.

VII. Conclusion

In this paper, an isolated soft-switched TPC to interface with hybrid renewable energy systems is presented. Its operating principle and design considerations are discussed and verified by simulation and experimental results. In order to control the power flow between the different ports, a duty cycle and phase-shift control scheme is adopted. The duty cycle is used to control the power flow between the two independent sources, whereas the phase-shift angle is employed to regulate the output voltage. The state-space modeling and control of the proposed TPC operating in completely demagnetized and fully magnetized mode is presented. The mathematical model is validated by simulation as well as experimental measurements of the plant and line-to-output transfer functions. The advantage of the proposed topology is that it can be dynamically modelled as individual converters, which makes it possible to design a control strategy with totally uncoupled control variables. This fact makes this topology a very interesting solution in renewable energy applications where an energy storage element is required, since full reutilization of the converter primary side switches is achieved, without having a negative impact in the controllability of the converter. By selecting the renewable source and the energy storage voltages, V_1 and V_2, to require a duty cycle approximately to 0.5 the phase-shift value range can be fully utilized. Experimental results demonstrate that the proposed energy/power management solution achieves effective control of the power flow among the input, bidirectional and output ports.

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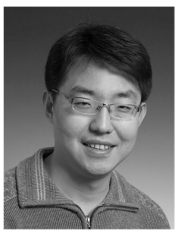

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Isolated Boost Converter with Bidirectional Operation for Supercapacitor Applications

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Isolated Boost Converter with Bidirectional Operation for Supercapacitor Applications

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Abstract

This paper presents an isolated bidirectional dc/dc converter based on primary parallel isolated boost converter (PPIBC). This topology is an efficient solution in low voltage high power applications due to its ability to handle high currents in the low voltage side. In this paper, the converter has been modeled using non-ideal components and operated without any additional circuitry for startup using a digital soft-start procedure. Simulated and measured loop gains have been compared for the validity of the model. On-the-fly current direction change has been achieved with a prototype interconnecting two battery banks. A second prototype has been constructed and tested for supercapacitor operation in constant power charge mode.

Key words: Battery, Bidirectional, Isolated, Modeling, Startup, Supercapacitor

NOMENCLATURE

$R_{D_{Bat}}$	Battery dynamic resistance
$V_{OC_{Bat}}$	Battery open circuit voltage
R_{ESR}	Supercapacitor series resistance
V_{SC}	Supercapacitor voltage
r_L	Inductor parasitic resistance
$r_{M\,P}$	Primary MOSFETs on resistance
r_p	Transformer primary resistance
r_S	Transformer secondary resistance
$r_{M\,S}$	Secondary MOSFETs on resistance
r_{ESR}	Capacitor series resistance

I. INTRODUCTION

Nowadays the depletion of fossil fuels together with the awareness of the climate change is forcing the industry to move towards green energy solutions. The same change is starting to be a reality in transportation industry where hybrid and electric vehicles are presented as an alternative solution to CO2 emission reduction. Extension of the driving range in electric vehicles has become one of the main concerns to make this an attractive technology. Special efforts have been taken to improve the capacity of the energy storage elements and to increase the efficiency of all the parts inside the power drive train. Regenerative brakin g is one of the adopted solutions for increasing the driving range by recovering the kinetic energy of the vehicle during the braking process.

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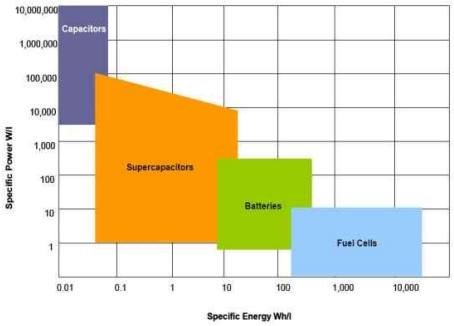

Fig. 1. Ragone chart. Power density vs. energy density for various energy storage systems [1].

Supercapacitors have relatively large power density, as shown in Fig. 1, and are the preferred energy storage elements in regenerative braking applications. The aim of this work is to integrate a supercapacitor bank in a fuel cell powered drive train (Fig. 2) to increase the dynamics and the power density of the system.

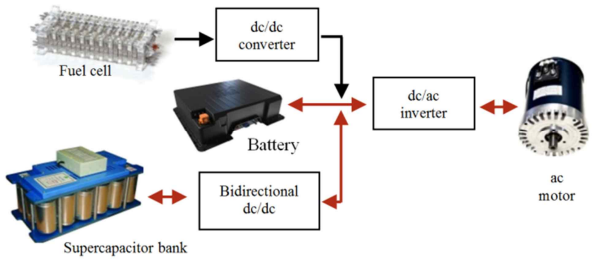

Fig. 2. Supercapacitor and bidirectional converter integration into a fuel cell powered drive train.

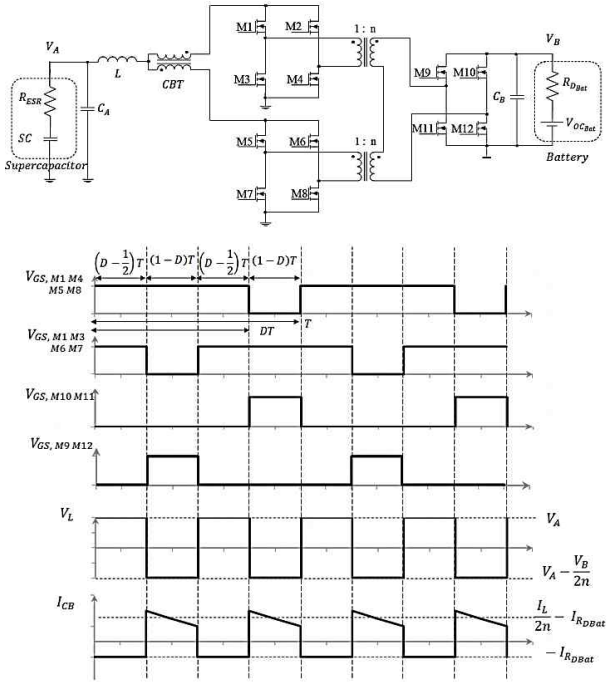

Fig. 3. Converter schematic (up) and boost mode steady state operating waveforms (down).

Different bidirectional dc-dc converter topologies have been proposed and investigated in the literature so far [2]-[7]. PPIBC is an efficient solution for low voltage high current applications [8]-[9]. Due to the transformer series connection on the secondary side, the current on each parallel primary stage is forced to be equal. However, different stray inductances in the current path or mismatches in the gate drive signal can cause the input current of each full bridge deviate from each other. In order to prevent this situation a current balancing transformer (CBT) is inserted to the circuit in series with the input inductor [10]. The CBT, which is implemented as an inverse coupled inductor, shows high impedance between the two parallel primary stages and keeps the branch currents to be equal. The schematic and waveforms of the proposed bidirectional converter are shown in Fig. 3.

In this topology, parallel primary power stages share the same control signals with the same phase switching sequence for the corresponding switches, which allows a simple control, similar to a simple isolated boost converter.

Output rectification unit as well as input and output filters are common to both of the parallel primary stages. The paralleling method splits the critical high ac-current-loop into two smaller loops. Each of the smaller loops only needs to switch half of the input current thereby achieving higher conversion efficiency. Since the two transformers share the same input current and have their secondary windings connected in series, a higher turns-ratio transformer can be replaced by two lower turns-ratio transformers, which allows a simple design and manufacturing of the transformers.

In this paper bidirectional operation of the PPIBC is studied. An accurate dynamic model of the converter has been derived taking into consideration the component non-idealities. Simple supercapacitor and battery models with internal impedances are also included in the model. PPIBC has been reduced to a simple boost converter in order to derive the state space equations.
Gain and phase plots of the compensated loop have been obtained from both the derived model and the experimental setup.

II. CONVERTER MODELING

Due to the large voltage time constant of batteries and supercapacitors, for small signal modeling purposes, these components can be treated as ideal voltage sources with an equivalent series resistance. Dc-dc converters interfacing this kind of energy storage elements need to be designed based on an accurate small signal model. This is due to the fact that the low value of the supercapacitor and battery series resistance makes the current flow in the converter to be very sensitive to duty cycle perturbations [11].

State space average modeling has been used to obtain an accurate model that predicts the dynamics of the system in a precise way. The converter parasitic resistances have been included in the model since they are in the same range with the battery and supercapacitor series resistances. Consequently, not considering these parasitics will have an effect on the dc gain of the plant transfer functions.

Fig. 4 shows the first state of the converter that corresponds to the charging state in boost mode and the discharging state in buck mode. Fig. 5 shows the simplified version of Fig. 4 where the two transformers are combined into an equivalent transformer with a turn ratio of $1:2n$. All the components are reflected to the inductor side and parasitic resistances are combined into an equivalent resistance $(r_{eq\,1})$.

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\cdot\left(r_{eq\,1} + \frac{r_{esrA}\cdot R_{ESR}}{R_{ESR}+r_{esrA}}\right) & \frac{R_{ESR}}{L\cdot(R_{ESR}+r_{esrA})} & 0 \\ -\frac{R_{ESR}}{C_A\cdot(R_{ESR}+r_{esrA})} & -\frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ 0 & 0 & -\frac{1}{C_B\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrA}}{L\cdot(R_{ESR}+r_{esrA})} & 0 \\ \frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ 0 & \frac{1}{2\cdot C_B\cdot n\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} V_{SC} \\ V_{OC_{Bat}} \end{bmatrix} \quad (5)$$

$$V_B(t) = \begin{bmatrix} 0 & 0 & \frac{R_{D_{Bat}}}{R_{D_{Bat}}+r_{esrB}} \end{bmatrix}\cdot\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{r_{esrB}}{2\cdot n\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} V_{SC} \\ V_{OC_{Bat}} \end{bmatrix} \quad (6)$$

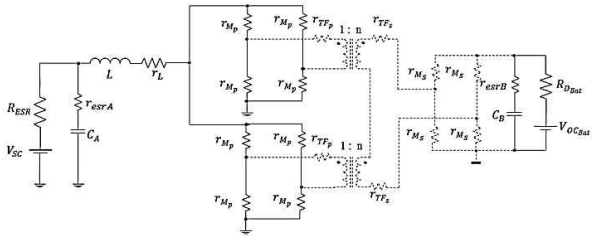

Fig. 4. Converter first state with parasitic resistances.

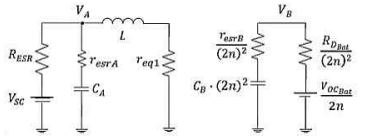

Fig. 5. Simplified equivalent circuit. Converter first state.

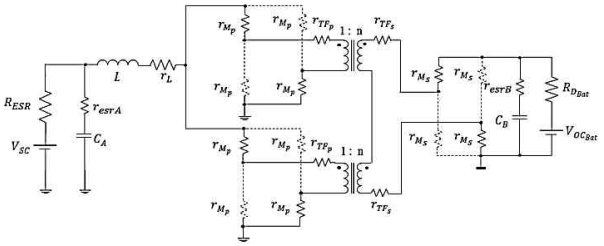

Fig. 6. Converter second state with parasitic resistances.

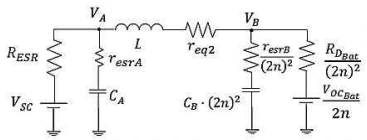

Fig. 7. Simplified equivalent circuit. Converter second state.

Fig. 6 presents the second state of operation corresponding to the discharging state of the boost mode and the charging state of the buck mode. Similar to the previous state the circuit is reduced to a simpler form as shown in Fig. 7.

The equivalent resistances in Fig. 5 and Fig. 7 are given by (1) and (2).

$$r_{eq1} = r_L + r_{MP}/2 \tag{1}$$

$$r_{eq2} = r_L + r_{MP} + \frac{r_P}{2} + \frac{2r_S}{(2n)^2} + \frac{2r_{MS}}{(2n)^2} \tag{2}$$

Based on the simplified circuits for both operating states, the state and output matrixes can be written in the form of (3) and (4) as in (5) and (6) for the first converter state.

$$\frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) \tag{3}$$

$$V_B(t) = q_1 x(t) + k_1 u(t) \tag{4}$$

In the same way, (7) and (8) can be obtained as shown in (9) and (10) for the second converter state.

$$\frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) \tag{7}$$

$$V_B(t) = q_2 x(t) + k_2 u(t) \tag{8}$$

The state, input and output matrixes are obtained by averaging the individual matrixes for each state over a period as shown in (11), (12), (13) and (14).

$$A = A_1 \cdot d + A_2 \cdot (1-d) \tag{11}$$

$$B = B_1 \cdot d + B_2 \cdot (1-d) \tag{12}$$

$$q = q_1 \cdot d + q_2 \cdot (1-d) \tag{13}$$

$$k = k_1 \cdot d + k_2 \cdot (1-d) \tag{14}$$

After perturbing the circuit around a steady state operating point, the first order terms are collected to obtain the linear model as in (15) and (16).

$$\hat{x} = A \cdot \hat{x} + B \cdot \hat{u} + [(A_1 - A_2)X + (B_1 - B_2) \cdot U] \cdot \hat{d} \tag{15}$$

$$\hat{v}_b = q \cdot \hat{x} + k \cdot \hat{u} + [(q_1 - q_2)X + (k_1 - k_2) \cdot U] \cdot \hat{d} \tag{16}$$

The term X corresponds to the steady state solution given in (17).

$$X = -A^{-1} \cdot B \cdot U \tag{17}$$

Finally the small signal expressions of the state variables and the high side output voltage can be obtained by making $\hat{u}$ equal to zero and applying the Laplace transformation to (15) and (16) obtaining (18) and (19) respectively.

$$\hat{x} = (sI - A)^{-1} \cdot [(A_1 - A_2)X + (B_1 - B_2)U] \cdot \hat{d} \tag{18}$$

$$\hat{v}_b = \left[q \cdot (sI - A)^{-1} \cdot [(A_1 - A_2)X + (B_1 - B_2)U]\right] \cdot \left[+[(q_1 - q_2)X + (k_1 - k_2) \cdot U]\right] \cdot \hat{d} \tag{19}$$

The derived equations are valid independent of the power flow direction because the same differential equations govern the circuit for buck and boost operation modes. For this reason a single model is derived for both operating modes. In other words, if we consider the boost operating mode, the inductor charging subinterval is defined as dT which corresponds to discharging subinterval for buck mode defined

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{L}\cdot\left(r_{eq2} + \frac{r_{esrB}\cdot R_{D_{Bat}}}{4\cdot n^2\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} + \frac{r_{esrA}\cdot R_{ESR}}{R_{ESR}+r_{esrA}}\right) & \frac{R_{ESR}}{L\cdot(R_{ESR}+r_{esrA})} & -\frac{R_{D_{Bat}}}{L\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \\ -\frac{R_{ESR}}{C_A\cdot(R_{ESR}+r_{esrA})} & -\frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ \frac{R_{D_{Bat}}}{4\cdot C_B\cdot n^2\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} & 0 & -\frac{1}{C_B\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} \frac{r_{esrA}}{L\cdot(R_{ESR}+r_{esrA})} & -\frac{r_{esrB}}{2\cdot n\cdot L\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \\ \frac{1}{C_A\cdot(R_{ESR}+r_{esrA})} & 0 \\ 0 & \frac{1}{2\cdot n\cdot C_B\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} V_{SC} \\ V_{OC_{BatB}} \end{bmatrix} \tag{9}$$

$$V_B(t) = \begin{bmatrix} \frac{R_{D_{Bat}}\cdot r_{esrB}}{4\cdot n^2\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} & 0 & \frac{R_{D_{Bat}}}{R_{D_{Bat}}+r_{esrB}} \end{bmatrix}\cdot\begin{bmatrix} i_L(t) \\ v_{C_A}(t) \\ v_{C_B}(t) \end{bmatrix} + \begin{bmatrix} 0 & \frac{r_{esrB}}{2\cdot n\cdot\left(R_{D_{Bat}}+r_{esrB}\right)} \end{bmatrix}\cdot\begin{bmatrix} V_{SC} \\ V_{OC_{Bat}} \end{bmatrix} \tag{10}$$

TABLE I

CONVERTER OPERATION MODES

Boost Mode		Buck Mode
d	=	$1-d$
$1-d$	=	d
A_1	=	A_2
A_2	=	A_1
B_1	=	B_2
B_2	=	B_1
A	=	A
B	=	B

as $(1-d)T$. This duality is valid for all the converter dynamic expressions between buck and boost operating modes. Consequently, the final state equations remain the same independent of the power flow direction as shown in Table I.

III. CONTROL STRATEGY

In this application, current control on the battery side is preferred in order to absorb and deliver the necessary current to the inverter during regenerative braking and acceleration events. In this operation mode the supercapacitor is charged and discharged with constant power between the nominal voltage and half the nominal voltage to avoid high current stress on the low voltage side. However, when the supercapacitor voltage is under half of the nominal value due to the effect of leakage currents during long periods of inactivity of the system, the supercapacitor will be charged with constant current by controlling the inductor current.

From the state variable solution (18), the duty cycle-to-inductor current transfer function is obtained. Moreover, the duty cycle-to-high side output current can be obtained by dividing the duty cycle-to-high side voltage transfer function (19) by the battery dynamic resistance as shown in (20).

$$G_{IB}(s) = \frac{\hat{\imath}_B(s)}{\hat{d}(s)}\bigg|_{\hat{u}=0} = \frac{G_{VB}(s)}{R_{dbat}} \tag{20}$$

LTspice IV simulations are performed to validate the derived model by comparing the gain and phase plots. The steady state value of the inductor current is selected to be 100A in both power flow directions. The converter duty cycle is calculated from the dc steady state solution given in (17). The selected parameters for the simulations are presented in Table I.

Fig. 8 and Fig. 9 present the calculated and simulated gain and phase plots of the converter duty cycle-to-inductor current transfer function in boost and buck operation modes respectively. Very close matching between the simulation and the calculated model is achieved. It can be observed that the obtained plant transfer function is very similar for both modes. Only a small difference in the low frequency gain between the two operating modes can be observed. This effect is produced by the voltage drop across the parasitic resistances of the system.

TABLE II

CONVERTER SIMULATION PARAMETERS

L	$5\ \mu H$
r_L	$1\ m\Omega$
I_L	$100\ A$
n	$1/2$
V_{SC}	$30\ V$
R_{ESR}	$10\ m\Omega$
$V_{OC_{Bat}}$	$80\ V$
$R_{D_{Bat}}$	$40\ m\Omega$
$r_{M\,P}$	$10\ m\Omega$
r_p	$5\ m\Omega$
$r_{M\,S}$	$5\ m\Omega$
C_A	$100\ \mu F$
r_{esrA}	$2\ m\Omega$
C_B	$200\ \mu F$
r_{esrB}	$1\ m\Omega$

Fig. 10 and Fig. 11 show the comparison between the calculated and simulated duty cycle-to-high side output current transfer function. Equal than before very close matching between the simulation and the calculation is achieved. In this case, the dynamics of the system depend on the current flow direction because of the presence of a right half plane zero in boost operation mode.

IV. EXPERIMENTAL RESULTS

The first PPIBC prototype is shown in Fig. 12. The converter is controlled by using a 32 bit fixed point DSP.

The two transformers are integrated into the same magnetic core structure. This integrated magnetic component is constructed with four halves of ELP64/10/50 based on N87 core material.

The input inductor is built using four halves of E64/10/50 based on 3F3 material. The windings in both magnetic components are implemented using PCB boards with FR4 material. The inductor current is sensed by a Hall Effect current transducer LAS100-TP. The current measurement is low pass filtered by a differential amplifier to avoid aliasing at the ADC input.

In order to test the bidirectional operation, the prototype is connected to two battery banks at the low and high voltage side. The battery bank on the low voltage side is formed by three series connected AGM batteries Haze HZB-EV12-26

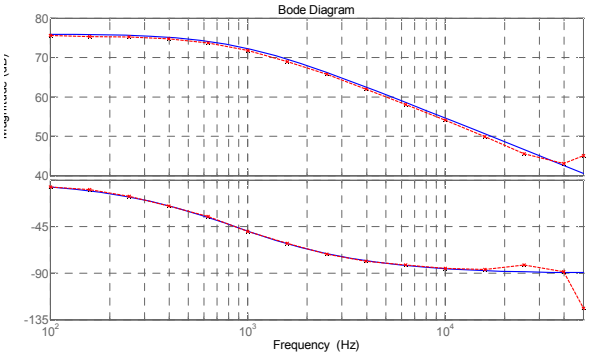

Fig. 8. Duty cycle-to-inductor current boost mode. Calculated (blue) and simulated (red).

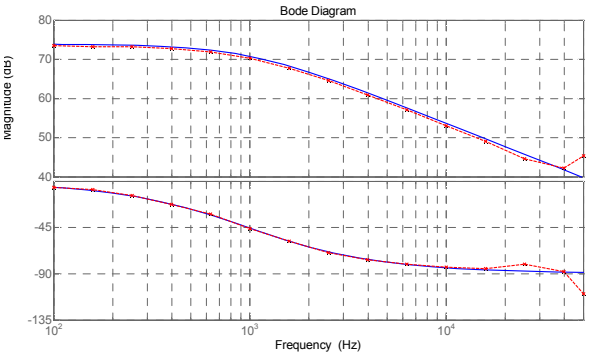

Fig. 9. Duty cycle-to-inductor current buck mode. Calculated (blue) and simulated (red).

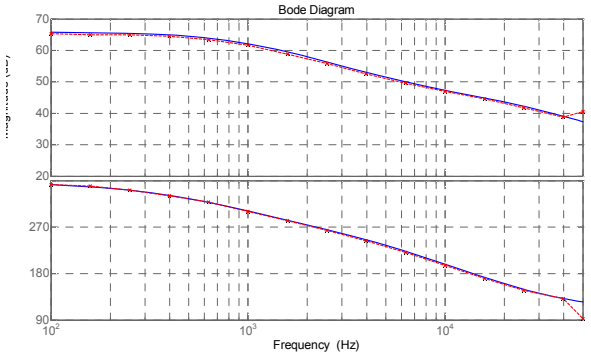

Fig. 10. Duty cycle-to-output current boost mode. Calculated (blue) and simulated (red).

which are rated for 12 volts and 26 Ah. On the high voltage side, the battery bank is composed of four series connected batteries of the same type. In this prototype, the inductor current is the selected control variable.

The battery impedance is measured and the obtained value at 1 kHz is used in the derived dynamic model to match the gain at the desired converter crossover frequency. The converter parameters are shown in Table III and the parasitic resistances are presented in Table IV. The magnetic component parasitic resistances correspond to the measured values at 1 kHz.

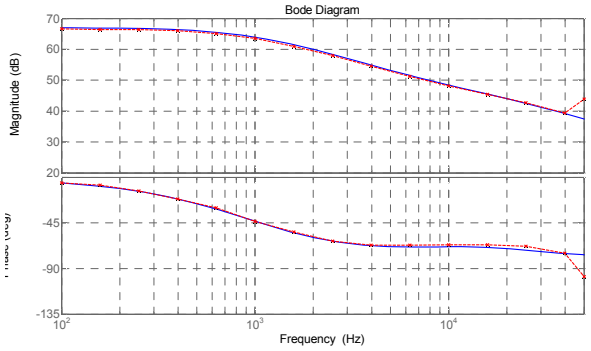

Fig. 11. Duty cycle to-output-current buck mode. Calculated (blue) and simulated (red).

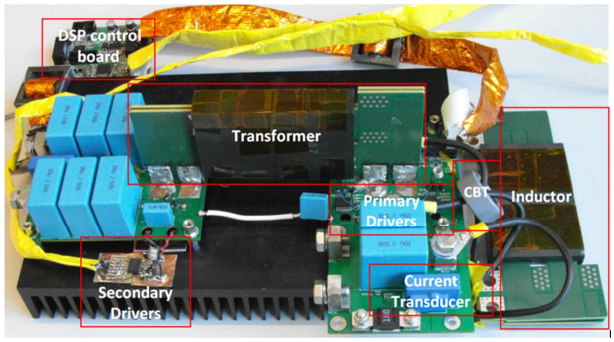

Fig. 12. First PPIBC prototype.

It is important to note that for calculating the dc operating point, the battery terminal voltage will change as a function of the current direction and magnitude as well as the battery state of charge (SOC). As presented in [12], the battery can be modeled as a dependent voltage source in series with the battery dynamic resistance. True understanding of the changes in the terminal voltages is possible through accurate modeling of the battery with capacitance-like effects of the battery internal chemistry, which is beyond the scope of this work.

In this paper the battery terminal voltages are measured at the desired operating conditions as shown in Table V. These values are used in the model to calculate the converter dc operating point.

The converter loop measurements are performed for both operating modes with a dc power supply as the input source to the converter and the corresponding battery bank as the converter load. The power supply output resistance is assumed to be negligible at the frequencies of interest. Moreover, it should to be noticed that the measured battery terminal voltages already include the voltage drop across the battery dynamic resistances.

The converter inductor current control loops are compensated by inserting an integrator and a zero before the lower frequency pole of the plant transfer function. Although

TABLE III

PARAMETERS OF THE CONVERTER

Battery A open circuit Voltage	$36V$
Battery B open circuit Voltage	$48V$
Transformer turn ratio	$1:3$
Inductor	$13.5\ \mu H$
Transformer and inductor core material	Ferrite 3F3
Capacitor A	$40\ \mu H$
Capacitor B	$120\ \mu H$
Switches M1-M8	IPA075N15N3 G
Switches M9-M12	FDH055N15A
Switching frequency	$50\ kHz$
Battery A dynamic resistance	$60\ m\Omega$ @ 1kHz
Battery B dynamic resistance	$80\ m\Omega$ @ 1kHz

TABLE IV

CONVERTER PARASITIC RESISTANCES

r_L	$3.9\ m\Omega$
r_{MP}	$7.5\ m\Omega$
r_p	$3.5\ m\Omega$
r_S	$0.4\ m\Omega$
r_{MS}	$5.9\ m\Omega$
r_{esrA}	$3.15\ m\Omega$
r_{esrB}	$1.1\ m\Omega$

TABLE V

CONVERTER STEADY OPERATING CONDITIONS

Boost Mode	Buck Mode
$V_G = 33.6\ V$	$V_{BatA} = 41\ V$
$V_{BatB} = 56.1\ V$	$V_G = 48\ V$
$I_L = 10\ A$	$I_L = -10\ A$
$d = 0.604$	$d = 0.422$

the converter plant transfer function is the same regardless of the current direction, different controllers have been used for boost and buck operation modes. This is due to the fact that the converter dc operating point is changed due to the battery terminal voltage being dependent on the current direction, which affects the converter transfer function. The compensation gain has been adjusted for a loop crossover frequency of 1 kHz for both operating modes.

Fig. 13 presents a measurement of the converter steady state waveforms. Fig. 14 and Fig. 15 show the calculated and

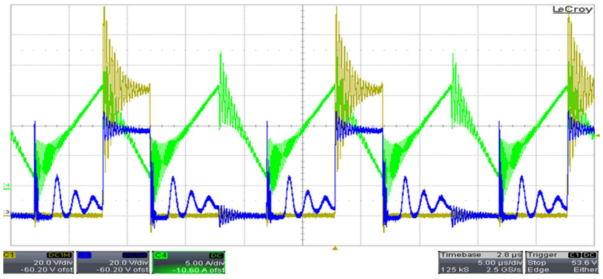

Fig. 13. Inductor current (green, 5A/div) with low voltage side (light brown, 20V/div) and high voltage side (blue, 20V/div) drain to source voltage waveforms during steady state operation. Time scale: 5µs/div.

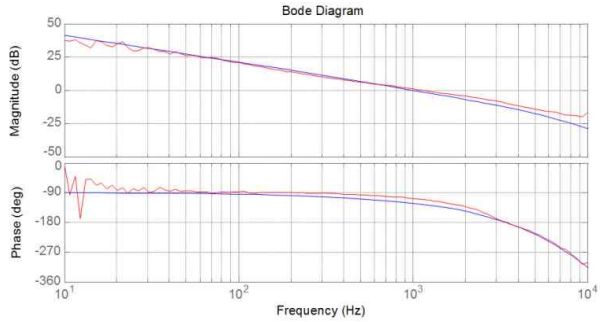

Fig. 14. Calculated (blue trace) and measured (red trace) open loop transfer function boost mode.

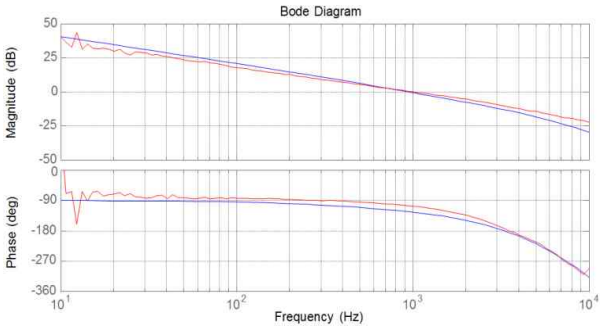

Fig. 15. Calculated (blue trace) and measured (red trace) open loop transfer function buck mode.

measured converter loop gain and phase plots where close matching can be observed. The calculated model includes the controller transfer function implemented inside the DSP with the sampling, calculation and PWM reconstruction delays, as well as the signal conditioning amplifier transfer function.

After designing the controllers for both operation modes, a soft start procedure of the converter needs to be implemented.

The implemented soft start function is able to turn on the converter in both directions without any additional circuitry.

While working with batteries, the duty cycle to inductor current transfer function has a larger gain compared to a pure resistive load for the same power level, meaning that the inductor current is very sensitive to small duty cycle perturbations in case of battery applications [11]. The converter has to be started with minimum duty cycle without

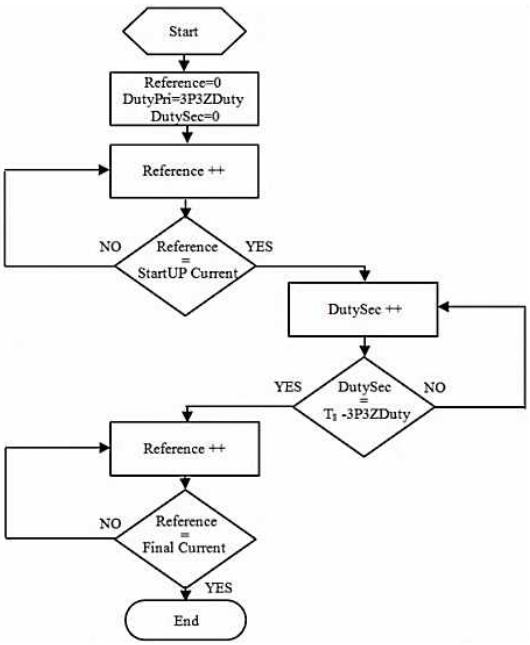

Fig. 16. Converter soft start flow diagram.

using synchronous rectification. Otherwise, starting with minimum duty cycle on one side will correspond to maximum duty cycle to the other side, creating an uncontrolled amount of initial current flow in the incorrect direction during converter startup. To avoid this situation, the converter should first be started by raising the current reference up to a certain startup current level. This current level has to be big enough to ensure CCM operation of the converter; otherwise, if the synchronous rectification is initiated, the duty cycle-to-inductor current transfer function will present a difference in dynamic behavior between DCM and CCM operation, resulting in an uncontrolled current increase until the control loop manages to compensate the error. Once the current trough the inductor has reached the desired level which ensures CCM operation, synchronous rectification can be started. At this point, the duty cycle for the synchronous MOSFETs is increased very slowly from zero to the final value calculated by the control law. This progressive introduction of the synchronous rectification avoids the current level to change again because of the difference in conduction resistance between the MOSFETs and the body diodes (used during normal rectification) that will affect the converter steady state conditions.

Once the synchronous rectification has been introduced, the final step is to increase the reference value up to the desired final current level. This soft start procedure removes unnecessary current and voltage stress from the switches at the start up increasing the converter reliability. The flow diagram of the proposed soft start procedure is presented in Fig. 16.

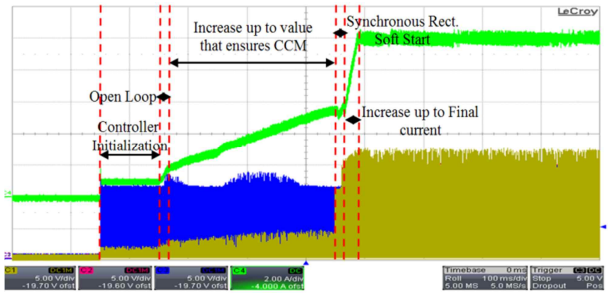

Fig. 17. Converter gradual soft start with two level inductor current reference change (green, 2A/div). Low voltage side MOSFETs gate waveform (blue, 5V/div) and high voltage side MOSFETs gate waveform (light brown, 5V/div.)Time scale: 100ms/div.

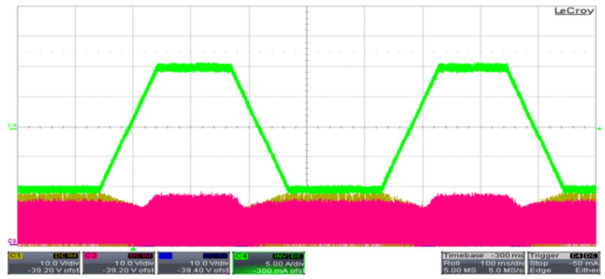

Fig. 18. Inductor current direction change with a defined ramp (5A/div. Time scale: 100ms/div).

Fig. 17 shows the detailed startup sequence where the converter input current on the low voltage side together with the gate waveforms of the MOSFETs can be observed. Fig. 18 shows the bidirectional operation of the converter with average inductor current control. The figure shows four current direction change events where the current change transition time has been adjusted to 100 ms.

After testing the soft start procedure and the bidirectional operation of the converter, a second PPIBC prototype with an input power of 8kW is constructed. This converter is used for testing operation with a supercapacitor module with constant power charge by controlling the high side output current of the converter. The prototype is implemented by using copper foil windings in the magnetic components and interconnections.

The two transformers with $n = 1/2$ are constructed using a stacked structure with four halves of E64/10/50 in 3F3 material. The input inductor is constructed with a Kool Mu core from Magnetics K6527E040. The converter prototype is shown in Fig. 19.

The converter is operated with a supercapacitor module from Maxwell $BM\,OD0130\,P056\,B03$ rated $56\,V$ and $130\,F$.

A controller composed of an integrator and a zero is designed and the loop crossover frequency is adjusted to 1 kHz for $V_B = 80\,V$ and $V_{SC} = 28\,V$ with an average inductor current of $I_L = 285\,A$. The duty cycle-to-output current transfer function has its maximum gain when the

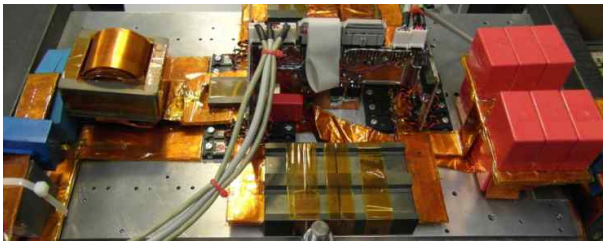

Fig. 19. Second PPIBC prototype.

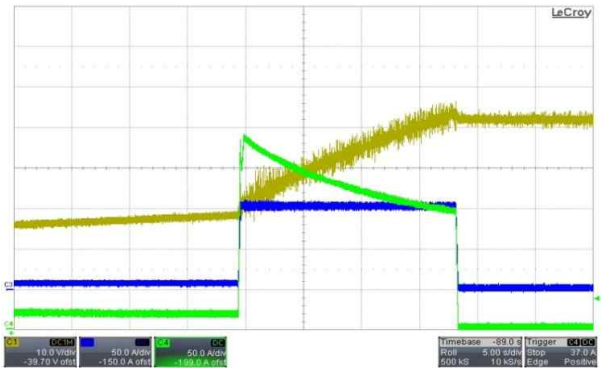

Fig. 20. Supercapacitor constant power charge event. Supercapacitor current (green, 50A/div). High side input current (blue, 50A/div) and supercapacitor voltage (light brown, 10V/div.)Time scale: 5s/div.

supercapacitor voltage is minimum. Therefore, by adjusting the controller for these operating conditions, stable operation of the converter can be guaranteed for the whole operating voltage of the supercapacitor. Fig. 20 shows a supercapacitor charge event with a constant input power level of 8 kW.

V. Conclusions

PPIBC is a high efficient isolated converter in low voltage high current applications. Bidirectional operation has been achieved by implementing synchronous rectification on the high voltage side. Accurate dynamic models have been derived and two different control strategies have been proposed for operation with supercapacitors.

Converter safe startup with batteries and supercapacitors regarding component stress is a non-trivial situation. The implemented DSP startup procedure proves that a soft start control of the current can be obtained and operation of the converter without any additional startup circuitry can be achieved.

The converter dynamic model has been shown to be the same independent of the power flow direction. The duty cycle-to-inductor plant transfer function is independent of the converter operating mode; therefore, a unified controller can be used for this control method. However, the duty cycle-to-output current transfer function dynamics present different behavior depending on the current flow direction due to the presence of a right half plane zero in boost operation mode. This situation forces the designer to implement two different controllers in order to maximize the dynamic performance of the control loops for each operation mode.

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Wide Operating Voltage Range Fuel Cell Battery Charger

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Wide Operating Voltage Range Fuel Cell Battery Charger

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***Abstract*—DC-DC converters for fuel cell applications require wide voltage range operation due to the unique fuel cell characteristic curve. Primary parallel isolated boost converter (PPIBC) is a boost derived topology for low voltage high current applications reaching an efficiency figure up to 98.2 %. This paper proposes a new operation mode for extending the input and output voltage range in PPIBC. The proposed solution does not modify PPIBC power stage; the converter gain is modified by short-circuiting one of the parallel connected primary windings in the topology. The change in operation mode divides by two the converter input-to-output voltage gain. This allows covering the conditions when the fuel cell stack operates in the activation region (maximum output voltage) and increases the degrees of freedom for converter optimization. The transition between operating modes is studied because represents a change in the converter steady-state conditions. A solution is proposed based on pre-calculation of the duty cycle prior to the transition.**

***Index Terms*—Isolated boost, fuel cell, battery, extended voltage range.**

I. INTRODUCTION

Due to the need for alternative energy resources, efficient power processing through power electronics circuits has been a popular academic field for the past decade. Fuel cells are one of the solutions widely adopted in uninterruptible power supplies (UPS), backup systems and electric vehicles. Fuel cells provide a clean and consistent source of energy by converting chemical energy into electrical energy. Power electronics interfacing fuel cell stacks and the rest of the power system should be designed considering some important electrical features of the fuel cell system, such as V-I characteristic curve. Among various converter topologies proposed and used in the literature, primary parallel isolated boost converter (PPIBC), derived from the conventional isolated boost converter, is a good candidate for such applications due to its simplicity and ability to handle high currents [1], [2]. However, boost type dc-dc converters have intrinsic start-up problems and limited input/output voltage range operation. Overcoming this limitation requires modification of the input inductor and employing additional circuitry [3]. In this paper an alternative solution with an extended voltage operation range is proposed based on modifying the operating mode of PPIBC. PPIBC schematic and steady-state operating waveforms under normal operating conditions are presented in Fig. 1 and Fig. 2.

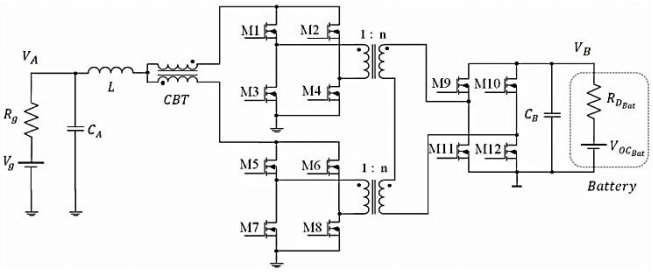

Fig. 1. Primary parallel isolated boost converter schematic.

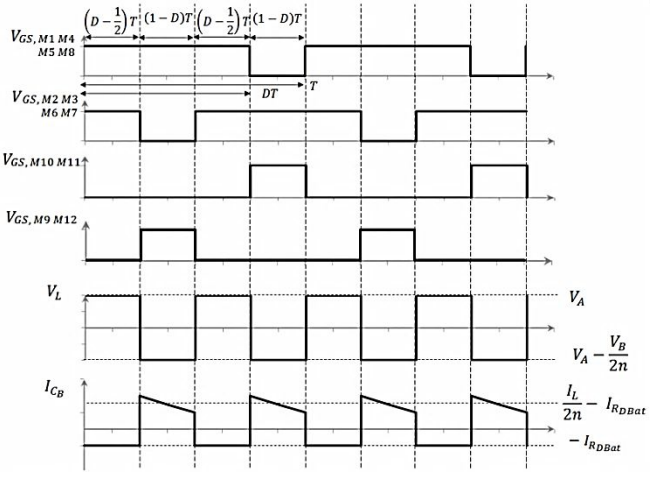

Fig. 2. Primary parallel isolated boost converter steady-state waveforms.

This topology increases the efficiency by splitting the primary current through two parallel primary stages. This approach results in reduced ac current loops, which helps reducing the power stage layout stray inductances. In addition, the secondary windings of the two transformers are connected in series, which reduces the number of turns on the secondary side for individual transformers allowing an

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easier magnetic component design. The primary switches in each parallel stage are driven with identical gate signals. Moreover, the two stages share the input inductor as well as the input and output filters, which makes this topology a simple solution. Due to the transformer series connection on the secondary side the two currents flowing through the two primary stages are forced to be equal during the inductor discharge state. In order to balance the current between the primary stages during the inductor charging subinterval, a current balancing transformer (CBT) [4] is inserted. This component is implemented as two inversely coupled inductors that present high impedance in case of current. imbalance, keeping the current equal in each parallel stage.

In this work, PPIBC acts as a battery charging unit in a fuel cell powered electric drive train in a low speed vehicle, as shown in Fig. 3. The V-I characteristic curve of a fuel cell is a nonlinear function [5], where three different regions can be distinguished as shown in Fig. 4. Moreover, as presented in the Shepherd model [6], the battery terminal voltage strongly depends on the charging current. Due to the battery terminal voltage dependence and the voltage rise in the activation region of the fuel cell (see Fig. 4), the converter needs to be designed for a wide operating input and output voltage range. When an acceleration event occurs, the inverter current demand will reduce the battery terminal voltage; if the fuel cell stack is operating in the activation region during this event, the converter will have to present minimum input to output voltage gain.

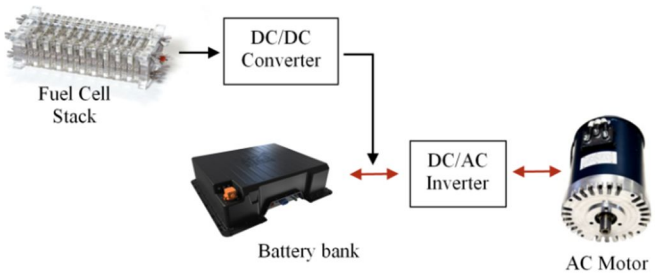

Fig. 3. Power drive train block diagram.

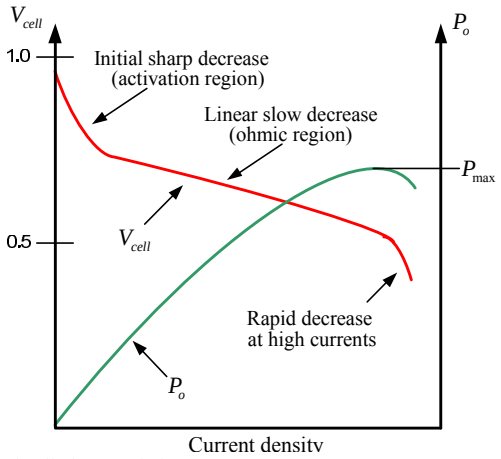

Fig. 4. Fuel cell characteristic V-I curve.

Therefore, in this application the transformer turns ratio has to be selected for the converter to operate with minimum duty cycle under these operating conditions. However, this solution will increase the converter voltage and current stresses negatively affecting the efficiency. Instead, this paper proposes a change in the converter operation mode, which increases the degrees of freedom in the design for the converter optimization.

II. Extended Operating Voltage Range

One of the disadvantages of isolated boost type dc-dc converters is the 50 % theoretical minimum duty cycle for each primary side switch, which corresponds to a "no boosting" operating point. Further decreasing the duty cycle is not possible since this will result in a practical "open circuit" situation for the input inductor. This lower limit for the switch duty cycle also puts a lower limit for the output voltage or an upper limit for the input voltage. The state of the art solution for extended voltage range in isolated boost converters has been presented in the literature [3], [7]. The solution in [3] proposes an auxiliary winding in the input inductor that will provide flyback operation to the converter, extending the operating voltage range and solving the intrinsic start-up problems in boost derived topologies. However, this is not an efficient solution in high power applications and makes the manufacturing process of the input inductor more complicated since extensive interleaving techniques will have to be adopted to increase the coupling coefficient of the flyback winding.

This work presents an efficient solution for extending the voltage range of PPIBC by implementing a new operation mode where the two upper side MOSFETs in one of the parallel stages are shut down while the lower side switches are kept in conduction mode. This new operation mode effectively reduces the equivalent converter conversion ratio by short-circuiting the primary winding in one of the primary stages, which deactivates the corresponding transformer.

As in the auxiliary flyback winding configuration, the main drawback of the proposed solution is the increased voltage stress on the primary switches during the extended operation mode. As shown in (3) the output voltage is no more divided in the series secondary windings of the two transformers. This situation will increase the requirement for the primary switch breakdown voltage, consequently increasing the device on resistance, which affects the converter efficiency. However, if the extended operation mode is only used to cover the operating conditions with minimum output voltage, the primary MOSFETs breakdown voltage requirement will not be affected.

$$V_{DS_{PPIBC}} = V_B / (2n), \quad (1)$$

$$V_{DS_{Flyback}} = V_A + V_B / (2n), \quad (2)$$

$$V_{DS_{PPIBC\_Extended}} = V_B / n. \quad (3)$$

This is an attractive solution in applications with variable output voltage, where the extended mode will be operated only under minimum output voltage.

Figure 5 shows the current path at the inductor discharge subinterval during extended operation mode of the PPIBC. As it can be observed from Fig. 5, the primary winding of the lower transformer is effectively shorted by the two low side switches, M7 and M8. The converter steady-state

waveforms are presented in Fig. 6. Figure 7 shows the converter voltage gain during extended voltage range operation; since only one transformer is active, effective voltage conversion ratio of the converter is halved as shown in (4).

$$M(D) = V_B / V_A = n / \left[2(1-D)\right]. \quad (4)$$

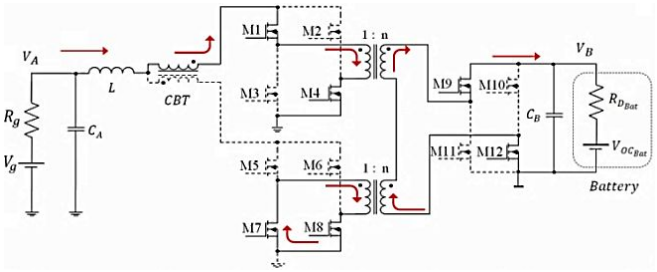

Fig. 5. PPIBC inductor discharge during extended voltage range mode.

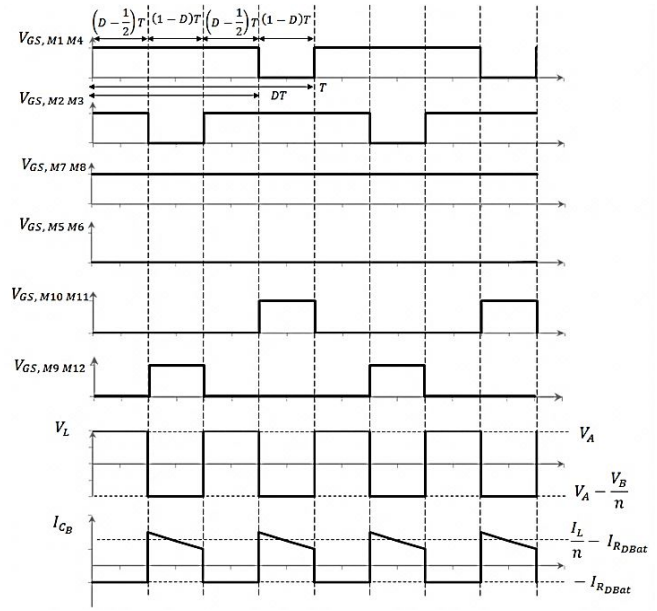

Fig. 6. PPIBC steady-state waveforms during extended voltage range operation.

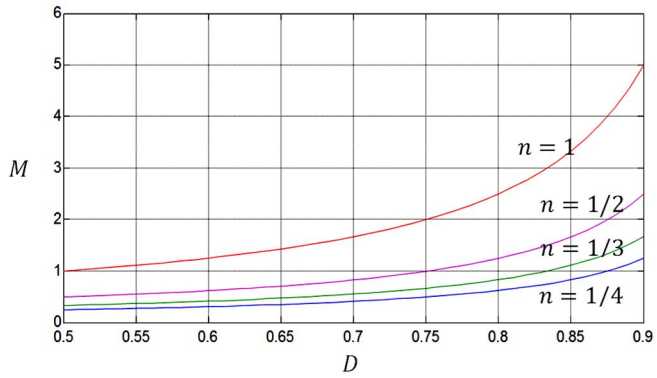

Fig. 7. Converter input to output voltage gain during extended operation mode for different transformer turns ratio.

III. Simulation of PPIBC with Extended Voltage Range Operation

The proposed solution is analysed by performing several LTspice simulations with the operating conditions shown in Table I. The transition of the converter between normal and extended operation mode needs to be investigated because the output current of the fuel cell should be stable during this event. If the operation of the converter has to be interrupted to switch from one mode to the other, a dummy load would have to be used in order to limit the output voltage of the fuel cell during the transition, and this would increase the complexity of the system.

TABLE I. PARAMETERS OF THE CONVERTER.

Source voltage	30 V
Battery terminal voltage	24 V
Transformer turn ratio	3:1
Inductor	13.5 µH
Capacitor A	40 µF
Capacitor B	120 µF
Switching frequency	50 kHz
Source output resistance	10 mΩ
Battery dynamic resistance	60 mΩ

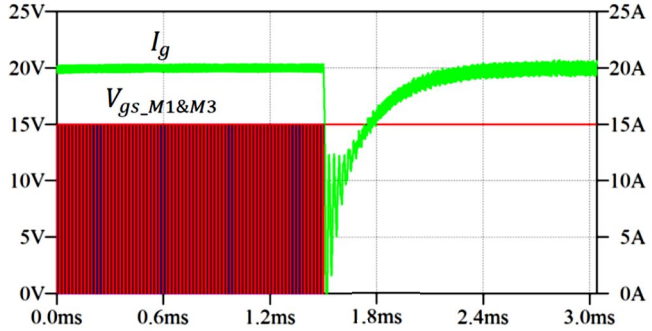

Fig. 8. Simulated transition from normal operation mode to extended operation mode. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

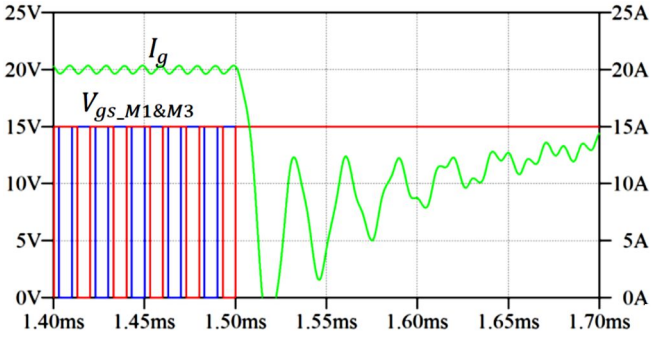

Fig. 9. Detailed enlarged area of the transition. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

Figure 8 and Fig. 9 present a simulation result where the inductor current level is fixed at $20A$ during closed loop operation of the converter. It can be observed that during the transition the current deviates from the reference value until the loop is able to compensate the error. The deviation in the current during the transition is caused by the change in the converter steady-state conditions and the sensitivity of the inductor current to duty cycle perturbations, as presented in [8]. This will increase the components current stress, which will reduce the converter reliability.

IV. Transition with Pre-Calculated Steady-State Duty Cycle

The current stress during the transition time can be

reduced if a steady-state duty cycle pre-calculation is performed based on an accurately derived model of the converter. In battery loading applications, as presented in [8]–[9], the duty cycle-to-inductor current transfer function is heavily affected by the converter parasitic resistances due to the low value of the battery dynamic resistance. Circuit models taking into account parasitic resistances for both inductor charge (Fig. 10) and discharge (Fig. 11) states during extended operation mode are derived. The simplified models, shown in Fig. 12 and Fig. 13, are obtained by reflecting the secondary side impedances to the primary side and combining the two parallel full-bridge transformers to a single structure with an effective transformer ratio N_e.

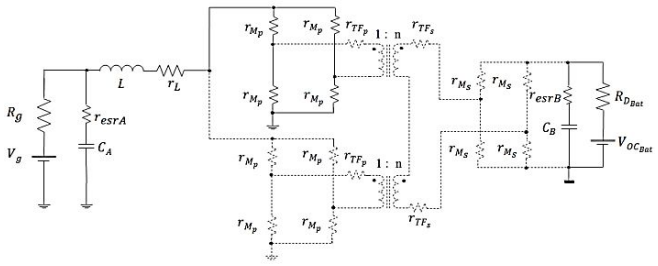

Fig. 10. PPIBC extended voltage range operation during the inductor charging subinterval.

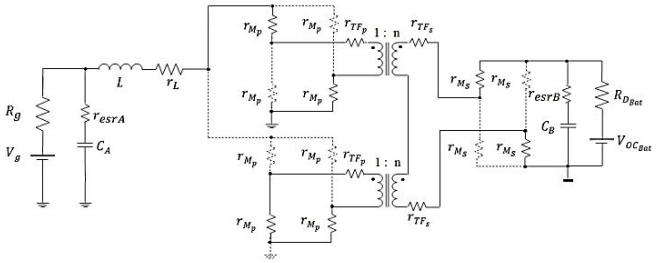

Fig. 11. PPIBC extended voltage range operation during the inductor discharging subinterval.

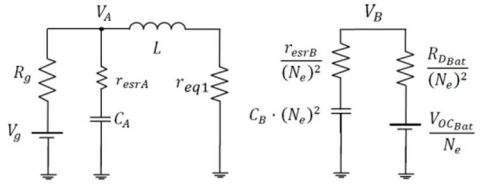

Fig. 12. PPIBC simplified equivalent circuit during the inductor charge.

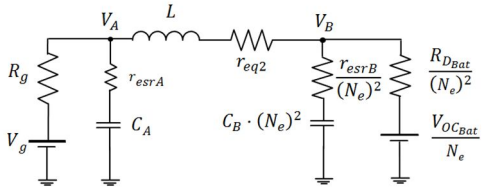

Fig. 13. PPIBC simplified equivalent circuit during the inductor discharge.

State-space equations are derived based on the two operating states of the converter [8]. The state matrixes are calculated for the inductor charging and discharging subintervals as shown in (16) and (17). The input matrix corresponding to the inductor charging subinterval is shown in (5), and the input matrix corresponding to the discharging subinterval is calculated as shown in (6):

$$B_1 = \begin{pmatrix} r_{esr_A} / \left[L\left(R_g + r_{esr_A}\right)\right] & 0 \\ 1/\left[C_A\left(R_g + r_{esr_A}\right)\right] & 0 \\ 0 & 1/\left[2C_B N_e \left(R_{D_{Bat}} + r_{esrB}\right)\right] \end{pmatrix}, \quad (5)$$

$$B_2 = \begin{pmatrix} r_{esr_A} / \left[L\left(R_g + r_{esr_A}\right)\right] & -r_{esr_A} / \left[2N_e L\left(R_{D_{Bat}} + r_{esrB}\right)\right] \\ 1/\left[C_A\left(R_g + r_{esr_A}\right)\right] & 0 \\ 0 & 1/\left[2C_B N_e \left(R_{D_{Bat}} + r_{esrB}\right)\right] \end{pmatrix}. \quad (6)$$

Equivalent transformation ratio N_e and equivalent resistances r_{eq1} and r_{eq2} are defined as shown in (7)–(9) for normal operating mode. These can be calculated in the same way for extended operating mode as shown in (10)–(12):

$$N_e = 2n, \quad (7)$$

$$r_{eq1} = r_L + r_{M\,P} / 2, \quad (8)$$

$$r_{eq2} = r_L + r_{M\,P} + r_P / 2 + \\ +2r_S / (2n)^2 + 2r_{M\,S} / (2n)^2, \quad (9)$$

$$N_e = n, \quad (10)$$

$$r_{eq1} = r_L + r_{M\,P}, \quad (11)$$

$$r_{eq2} = r_L + 4r_{M\,P} + 2r_P + \\ +2r_S / n^2 + 2r_{M\,S} / n^2. \quad (12)$$

Based on the conduction states shown in Fig.10 and Fig. 11, a new model can be obtained for normal and extended operating voltage mode. The state equation of the system is obtained as shown in (13)

$$d / dt \begin{pmatrix} i_L(t) \\ v_{C\,A}(t) \\ v_{C\,B}(t) \end{pmatrix} = A \cdot \begin{pmatrix} i_L(t) \\ v_{C\,A}(t) \\ v_{C\,B}(t) \end{pmatrix} + B \cdot \begin{pmatrix} V_g \\ V_{OC\,Bat} \end{pmatrix}. \quad (13)$$

The averaged value of the input and state matrixes is obtained by averaging (5), (6), (16) and (17) over the inductor period as shown in (14) and (15):

$$A = A_1 \cdot d + A_2 \cdot (1 - d), \quad (14)$$

$$B = B_1 \cdot d + B_2 \cdot (1 - d). \quad (15)$$

$$A_1 = \begin{pmatrix} -\frac{1}{L}\left(r_{eq1} + \frac{r_{esr_A} \cdot R_g}{R_G + r_{esr_A}} \right) & \frac{R_g}{L\left(R_g + r_{esr_A}\right)} & 0 \\ -\frac{R_g}{C_A\left(R_g + r_{esr_A}\right)} & -\frac{1}{C_A\left(R_g + r_{esr_{IN}}\right)} & 0 \\ 0 & 0 & -\frac{1}{C_B\left(R_{D_{Bat}} + r_{esr_B}\right)} \end{pmatrix}, \quad (16)$$

$$A_2 = \begin{pmatrix} -\frac{1}{L}\left(r_{eq2} + \frac{r_{esrB}\cdot R_{D_{Bat}}}{4N_e^2\left(R_{D_{Bat}} + r_{esrB}\right)} + \frac{r_{esr_A}\cdot R_g}{R_g + r_{esr_A}} \right) & \frac{R_g}{L\left(R_g + r_{esr_A}\right)} & -\frac{R_{D_{Bat}}}{L\left(R_{D_{Bat}} + r_{esrB}\right)} \\ -\frac{R_g}{C_A\cdot\left(R_g + r_{esr_A}\right)} & -\frac{1}{C_A\left(R_g + r_{esr_A}\right)} & 0 \\ \frac{R_{D_{Bat}}}{4\cdot C_B\cdot N_e^2\left(R_{D_{Bat}} + r_{esrB}\right)} & 0 & -\frac{1}{C_B\left(R_{D_{Bat}} + r_{esrB}\right)} \end{pmatrix}. \quad (17)$$

In order to reduce the current stress during the transition between normal and extended voltage range mode, the converter MOSFETs' duty cycle is computed prior to the transition by calculating the steady-state solution from (13) as shown in (18)

$$D = 2[1-(I_L\cdot\left(R_g + R_{D_{Bat}} / N_e{}^2 + r_{eq2}\right)+ +V_{OC\,Bat} / N_e - V_g) / (I_L\cdot(R_{D_{Bat}} / N_e{}^2 + +r_{eq2} - r_{eq1}) + V_{OC\,Bat} / N_e)]. \quad (18)$$

Equation (18) is simplfied by taking into account that the input and ouput capacitors do not affect the converter duty cycle-to-inductor current steady-state solution.

Nevertheless, a calculation based on this equation presents a very high computational demand because the battery dynamic resistance is strongly dependent on the battery state of charge (SOC). On the other hand, if the input and output voltages of the converter (V_A,V_B) are measured during operation, expression of (18) can be reduced to (19)

$$D = 2[1-\left(I_L\cdot r_{eq2} + V_B / N_e - V_A\right) / / \left(I_L\cdot\left(r_{eq2} - r_{eq1}\right) + V_B / N_e\right). \quad (19)$$

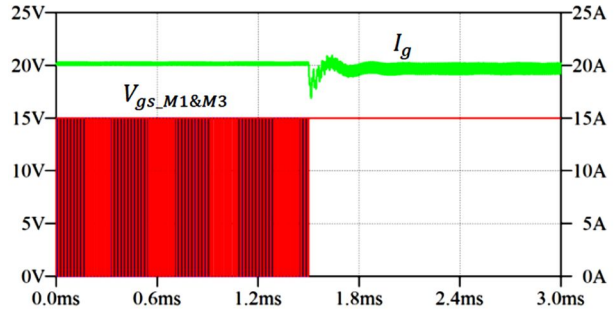

Fig. 14. Simulated transition between operating modes with pre-calculated steady-state duty cycle. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

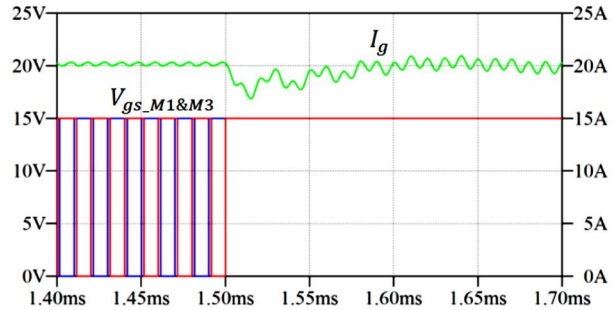

Fig. 15. Detailed enlarged area of the transition. Converter input current I_g (green), M1 and M3 gate signal (red and blue).

Figure 14 and Fig. 15 show an LTSpice simulation of a transition event where the controller has been set to produce the pre-calculated duty cycle before the transition event between normal and extended operating modes.

V. Experimental Results

A digitally controlled PPIBC has been used to experimentally verify the operation of the converter in extended mode. Each of the converter magnetic components is implemented with four planar ELP64/10/50 parts in N87 material. The primary and secondary switches are 150V N-channel MOSFETs IRFP4568. The converter control board is based on a 32 bit fixed point digital signal processor (DSP) TMS320F28035. The gate signals in one of the paralleled primary stages have been modified by inserting some control logic circuitry to produce the desired waveforms under the extended operation mode. The implemented prototype and the gate drive circuitry are shown in Fig. 16 and Fig. 17 respectively. Figure 18 shows the prototype operating waveforms during normal operation mode.

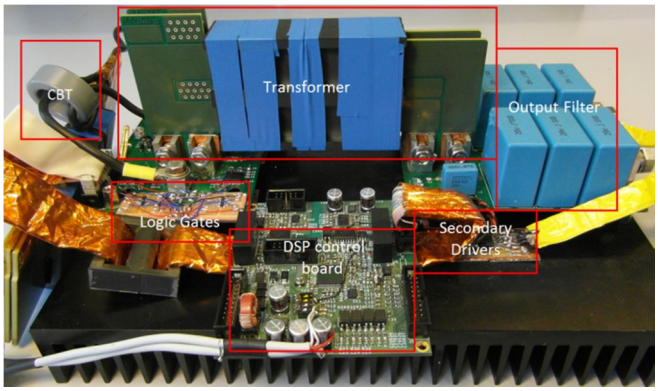

Fig. 16. PPIBC experimental prototype.

Figure 19 presents the converter operating waveforms during extended operating mode. The inductor current shows a change in the slope. During this mode, the magnetizing inductance of the current balancing transformer appears in series with the input inductor. However, the current balancing transformer saturates during this operation mode causing the change in the inductor current slope. The converter's efficiency in normal and extended operation modes can be observed in Fig. 20. The efficiency in the extended mode is measured at half the output voltage in normal mode. As it can be seen, the efficiency in extended operation mode decreases compared to the normal mode.

This is due to the higher current stress in the secondary side, the increased conduction losses in the primary side and

the increased transformer leakage inductance during the extended mode.

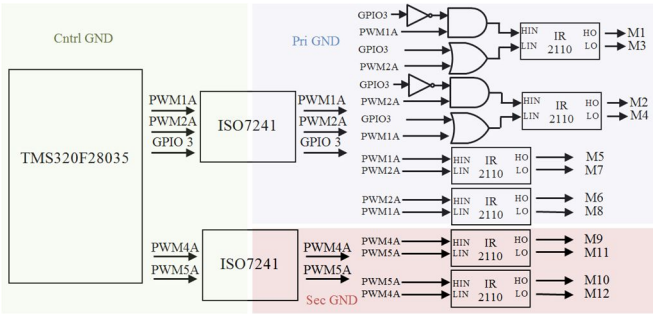

Fig. 17. Gate drive circuitry.

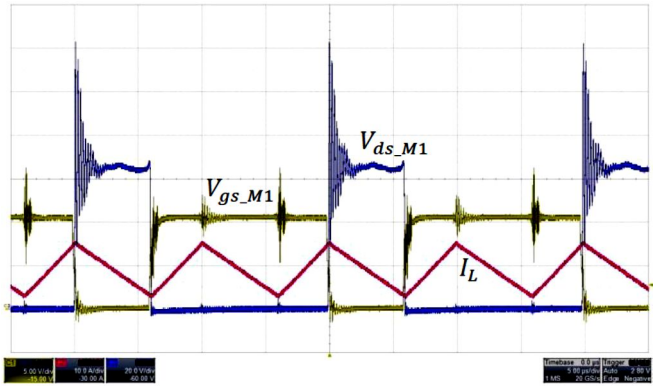

Fig. 18. Converter operating waveform during normal operation mode. M1 gate signal (brown, 5 V/div), M1 drain to source voltage signal (blue, 20 V/div) time scale 5 µs/div.

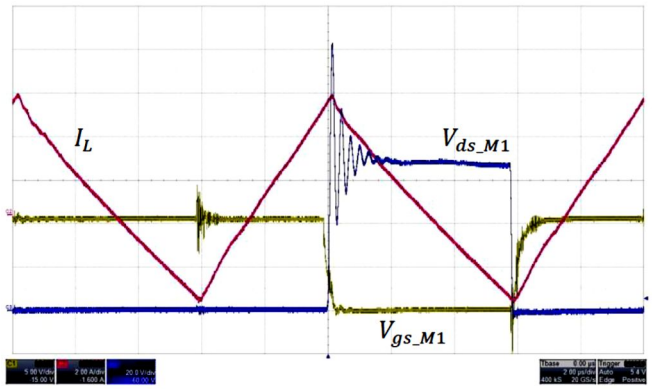

Fig. 19. Converter operating waveform during extended operation mode. M1 gate signal (brown, 5 V/div), M1 drain to source voltage signal (blue, 20 V/div) time scale 2 µs/div.

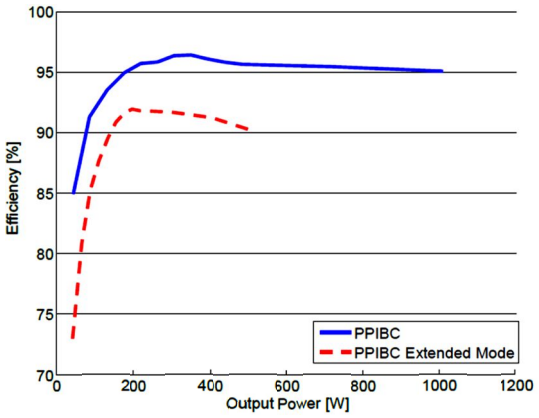

Fig. 20. Converter efficiency comparison between operating modes (blue, normal mode $V_{in} = 40\,V$ and $V_o = 45\,V$ and red $V_{in} = 40\,V$ and $V_o = 22.5\,V$).

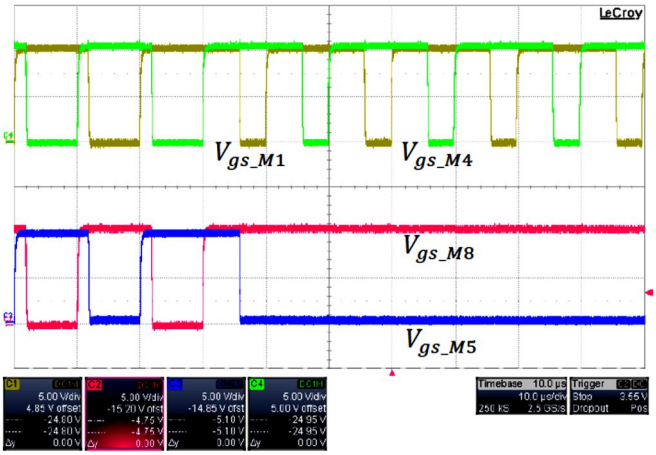

Fig. 21. Gate waveforms during normal to extended operating mode transition (b). M1 and M4 gate signals (brown and green, 5 V/div), M5 and M8 gate signals (blue and red, 5 V/div) time scale 100 µs/div.

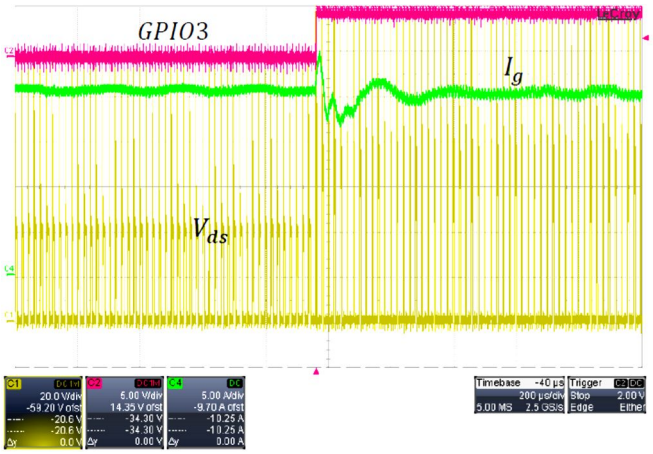

Fig. 22. Transition between operating modes with pre-calculated steady-state duty cycle. Time scale: 200 µs/div. Source output current I_g (green, 5 A/div), primary MOSFET drain to source voltage (brown, 20 V/div) and short circuit control signal GPIO3 (red, 5 V/div).

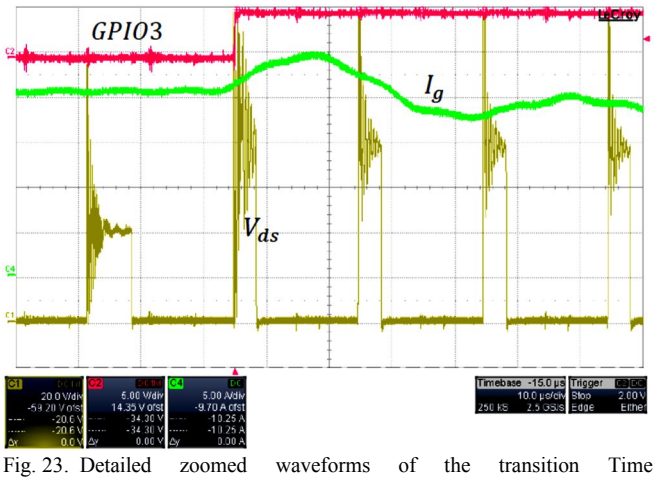

Fig. 23. Detailed zoomed waveforms of the transition Time scale:10 µs/div). Source output current I_g (green, 5 A/div), primary MOSFET drain to source voltage (brown, 20 V/div) and short circuit control signal GPIO3 (red, 5 V/div).

Figure 21–Fig. 23 show a transition event from normal to extended operating mode with pre-calculated duty cycle during converter closed loop operation for an inductor current level equal to 20 A. The change in duty cycle and voltage stress can be observed in one of the primary MOSFETs drain to source voltage waveform. It can be noticed that during extended operation mode, the voltage

ringing at the MOSFET off state increases with respect to the normal operation mode due to the effect of the leakage inductance of the short circuited transformer.

VI. Conclusions

In applications requiring wide operating voltage ranges, extreme duty cycles and extreme turn ratios for transformers have to be selected for covering the converter specifications, which will affect converter efficiency. Therefore, optimizing converter design for the most probable operating conditions and still covering all the possible operating points is desired. In order to do this, a new method for extending the operating voltage range has been proposed for PPIBC. The effective converter voltage conversion ratio is changed by deactivating one of the transformers through short-circuiting its primary windings. This new operation mode has been tested in a series of simulations and experiments where it has been observed that the transition between normal and extended operating modes is a disturbance to the converter due to the change in steady-state operating conditions. However, a smooth transition can be obtained if the steady-state duty cycle is pre-calculated based on an accurate model of the converter. This is an alternative solution to the auxiliary flyback winding in PPIBC.

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Component Stress Factor: Analysis of Dual Active Bridge and Isolated Full Bridge Boost Converter for Bidirectional Fuel Cells Systems

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Analysis and Comparison Based on Component Stress Factor of Dual Active Bridge and Isolated Full Bridge Boost Converters for Bidirectional Fuel Cells Systems

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***Abstract*—This paper presents an analysis and comparison of isolated topologies for bidirectional fuel cell systems. The analyzed topologies are the dual active bridge (DAB) and the isolated full bridge boost converter (IFBBC). The analysis is performed based on the component stress factor (CSF). Results highlight that the DAB has lower CSF than the IFBBC for narrow converter operating points. On the other hand the IFBBC presents a more homogeneous CSF over the entire converter operating range. Finally, experimental results obtained from a 30-80 V 80 A 6 kW 40 kHz IFBBC are presented. The converter achieves efficiencies up to 98.2% and 97.45% depending on the converter power flow.**

Keywords—Dual Active Bridge (DAB), Isolated full Bridge Boost Converter (IFBBC), Component Stress Factor (CSF), High Efficiency, Bidirectional Fuel Cells.

I. INTRODUCTION

Power converter's efficiency has been one of the major driving forces in power electronics especially over the last two decades. The latest developments in the power semiconductor technologies allowed developing converters with efficiency above 98% even with isolated topologies [1],[2]. However, selecting the latest silicon carbide (SiC) power semiconductors [3] it is not sufficient to achieve high efficiency. It is necessary to perform an analysis and optimization of different solutions in terms of converter topology, power semiconductors, magnetic component design as well as converter optimization.

Large scale integration of renewable energies requires grid tie energy storage to balance the energy production and consumption [4]. For these applications bidirectional fuel cells represent an attractive technology [5]. However, bidirectional fuel cells, also called regenerative or reversible fuel cells (RFCs), have wider operating conditions than conventional unidirectional fuel cells. Choosing the most suitable topology that can guarantee good performance over the entire system operating range is always troublesome and challenging. This is especially true for fuel cells applications where power converters are expected to operate at low-voltage and high-current levels.

This paper presents an analysis of two isolated dc-dc converter topologies: the isolated full bridge boost converter (IFBBC) [2] and the dual active bridge (DAB) [6]. The two topologies are analyzed in terms of component stress factor [7],[8] and compared based on the converter specifications for bidirectional fuel cell applications. Based on the analysis, a 6 kW bidirectional dc-dc IFBBC has been developed. The converter prototype achieves peak efficiencies of 98.2% and 97.45% depending on the converter power flow.

II. SYSTEM ANALYSIS AND SPECIFICATIONS

An energy storage bidirectional system based on regenerative fuel cells requires high efficiency dc-dc and dc-ac converters to effectively operate the system at its maximum performance. The cell technology strongly affects the system topology in fact, the voltage of a single cell is too low to realized multi-kW energy storage systems. It is necessary to stack several cells to achieve voltage levels that can better be processed by multi-kW power converters. Stacking a large number of cell increases the manufacturing challenges, such as homogeneous operating conditions of the cells stack and fuel pressure equalization. Moreover, not all fuel cells are suitable for bidirectional operation since operating in the two modes could significantly change the stress conditions of the cells and affect their reliability.

Based on a close cooperation with a large fuel cells manufacturer, it was determined that new solid oxide cell technology can be operated in both fuel cell mode (SOFC) and electrolyzer cell mode (SOEC). Table I shows the dc-dc converter specifications, which are defined based on a laboratory prototype of SOFC/SOEC cells stack. A 50 kW

TABLE I
SOFC AND SOEC DC-DC CONVERTER SPECIFICATIONS

	SOFC	**SOEC**
Low Voltage (LV) side	30-50 V	50-80 V
Current (LV) side	40-0 A	0-80 A
High Voltage (HV) side	700-800 V	700-800 V
Power Rating	~1500 W	~6000 W

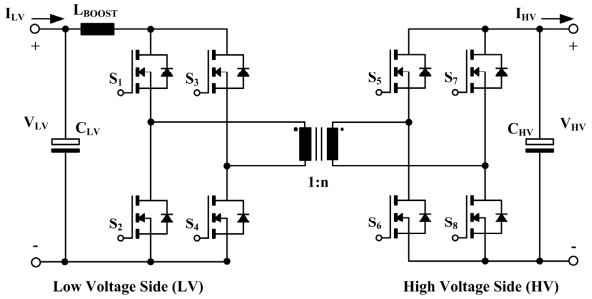


Fig. 1 IFBBC topology.

system for grid connected energy storage applications is presented in [9]. The system is composed by 10 cells stacks and each stack has a dc-dc converter. The operating mode of the system (SOFC or SOEC) determines the operating conditions of the dc-dc converter (I-V curve, [9]) and therefore, the system efficiency for the different operating points.

III. Isolated Topologies for Bidirectional Fuel Cells Systems: Selection and Analysis

Different isolated topologies can be candidate for energy storage systems based on bidirectional fuel cells. However, resonant topologies have difficulties to achieve suitable high efficiency when the converter ports voltage varies significantly (e.g. in this application by a factor 2.6). Another factor that influences the selection of the topology is its complexity in terms of number of power semiconductors, passive components and control. All these parameters will significantly affect also the cost of the converter and the economical sustainability of the system.

The results from the analysis of different isolated dc-dc converter topologies highlighted two candidate topologies suitable for the system: the isolated full bridge boost converter (IFBBC) and the dual active bridge (DAB).

A. Isolated Full Bridge Boost Converter (IFBBC)

The IFBBC topology shown on Fig. 1, has proved to achieve efficiency up to 98% [2] in fuel cell applications. The main CCM operating waveforms are presented in Fig. 2. The boost inductor L_{BOOST} is the component that controls the energy transfer from the converter low voltage side to the high voltage side and it has to handle the high current level I_{LV} on the converter low voltage side. Given an operating point, the duty cycle (0.5<D<1) is calculated according to (1).

$$D = 1 - \frac{nV_{LV}}{2V_{HV}} \tag{1}$$

For a given converter switching frequency $f_{SW}=1/T_{SW}$, the maximum and minimum boost inductor currents are expressed by (2) and (3) respectively. The transformer rms current of the low voltage side (4) can be calculated using (2) and (3).

$$i_0 = I_{LV} - \frac{V_{LV}T_{sw}(2D-1)}{4L} \tag{2}$$

$$i_1 = I_{LV} + \frac{V_{LV}T_{sw}(2D-1)}{4L} \tag{3}$$

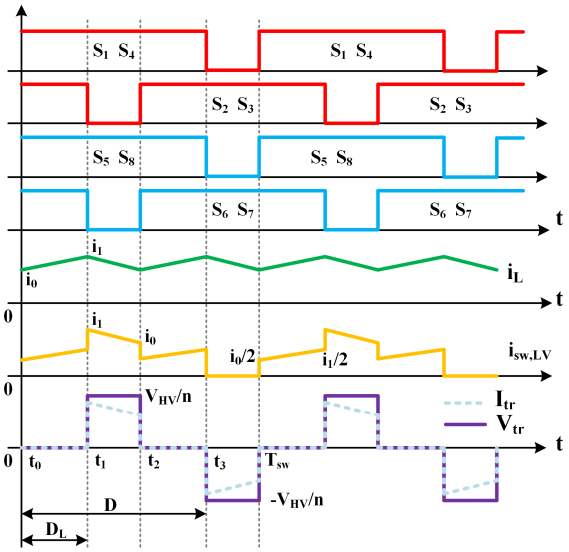


Fig. 2 IFBBC CCM main operating waveforms.

$$I_{tr.LV,rms} = \frac{\sqrt{2}}{\sqrt{3}}\sqrt{(1-D)(i_0^2 + i_1^2 + i_0 i_1)} \tag{4}$$

By neglecting the ripple in the boost inductor, it is possible to simplify (4) obtaining the transformer current in the low voltage winding as shown in (5).

$$I_{tr.LV,rms} = I_{LV}\sqrt{2(1-D)} \tag{5}$$

Assuming ideal current distribution in the converter switches, during the intervals t0-t1 and t2-t3 each switch on the converter low voltage side carries $I_{LV}/2$. During the intervals t1-t2 and t3-Tsw the full I_{LV} current flows through the switch. This results that the rms current of the low voltage side switches can be calculated as in (6).

$$I_{sw.LV,rms} = I_{LV}\sqrt{\frac{3}{4} - \frac{D}{2}} \tag{6}$$

The rms current of the high voltage side transformer winding and of the high voltage switches is expressed as a function of the current in the low voltage winding as in (7).

$$I_{tr.HV,rms} = \frac{I_{tr.LV,rms}}{n}; \quad I_{sw.HV,rms} = \frac{I_{tr.LV,rms}}{n\sqrt{2}}; \tag{7}$$

B. Dual Active Bridge (DAB)

In the DAB topology, shown in Fig. 3, the power flow is controlled through the ac-inductance in series with the transformer. Phase-shift modulation allows controlling the power flow in the converter with the phase-shift angle. By defining φ the phase-shift angle between the primary full bridge and the secondary full bridge, the power transfer between the low-voltage and the high voltage sides of the converter can be expressed as in (8). The maximum power transfer is achieved for $\varphi = \pi/2$; it can be observed that large

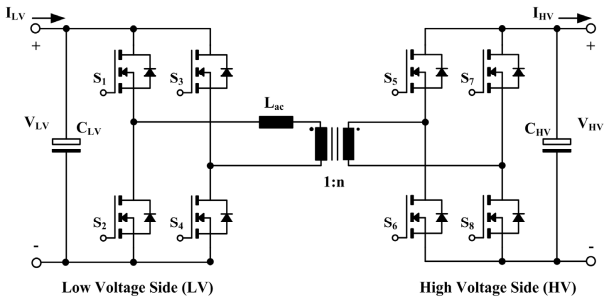


Fig. 3 DAB topology.

values of the L_{ac} would limit the maximum power flow in the converter.

$$P = \frac{V_{LV}V_{HV}}{n\omega L_{ac}}\varphi\left(1-\frac{\varphi}{\pi}\right) \tag{8}$$

Defining the voltage transfer ratio as in (9) allows expressing the transformer current at time intervals t0 and t1 as in (10) and in (11) respectively.

$$M = \frac{V_{HV}}{n\,V_{LV}} \tag{9}$$

$$i_0 = \frac{-V_{LV}}{2\omega L_{ac}}[(1-M)(\pi-\varphi)+(1+M)\varphi] \tag{10}$$

$$i_1 = \frac{V_{LV}}{2\omega L_{ac}}[(1+M)\varphi+(1-M)(\pi-\varphi)] \tag{11}$$

The symmetry of the transformer current (12) allows expressing the rms transformer low voltage side current as in (13). The transformer current on the high voltage winding is related to the rms current on the transformer low voltage side by the turns ratio *n*. The ac-inductor current rms current is the same as the rms current of the transformer low voltage side winding. It is a common design procedure to integrate the ac-inductor in the transformer by tuning the transformer leakage inductance.

$$i_2 = -i_0; \qquad i_3 = -i_1; \tag{12}$$

$$I_{tr.LV,rms} = \frac{1}{\sqrt{3}}\sqrt{i_0^2+i_1^2-i_0i_1+2\frac{\varphi}{\pi}i_0i_1} \tag{13}$$

The rms current of both low voltage and high voltage switches is defined as a function of the transformer low voltage windings rms current as in (14).

$$I_{sw.LV,rms} = \frac{I_{tr.LV,rms}}{\sqrt{2}}; \quad I_{sw.HV,rms} = \frac{I_{tr.LV,rms}}{n\sqrt{2}}; \tag{14}$$

IV. Component Stress Factor Analysis

Component stress factor (CSF) is an analytical method used to evaluate and compare different converter topologies for a specific application. The method provides an estimation of the converter stresses and gives a quantitative measure of converter performance. The CSF method is similar to the component load factor (CLF) [4],[5], the difference in the two methods lies in how the individual and total components are calculated. In order to perform a fair comparison of the topologies, CSF assumes that the same amount silicon, magnetic material and capacitor volume are used on the analyzed topologies. This is

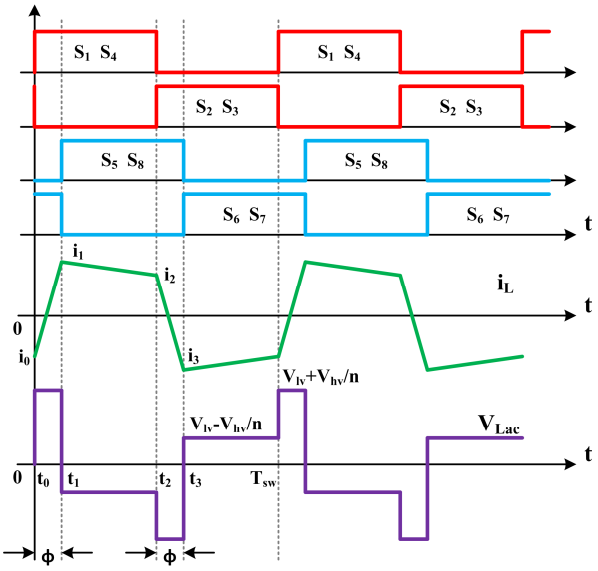


Fig. 4 DAB main operating waveforms with phase-shift modulation.

ensured by applying weighting factors to each component. The CSF analysis is performed based on three separate components: the semiconductor component stress factor (SCSF) (15), the winding component stress factor (WCSF) (16) and the capacitor component stress factor (CCSF) (17). The total stress over the different components is computed separately by adding together the relative components of the semiconductors (18), windings (19) and capacitors (20).

The different CSF values are calculated based on the devices voltages and rms currents. For power semiconductors the maximum voltage that the devices have to withstand over the entire converter operating range is considered. For wounded components, such as inductors and transformers, V_{max} represents the maximum averaged value (based on duty cycle). For capacitive components V_{pk} is the maximum peak value. All the CSF values are scaled with the processed power, making the CSF a dimensionless quantity.

$$SCSF_i = \frac{\sum_j W_j}{W_i}\cdot\frac{{V_{max}}^2\cdot{I_{rms}}^2}{P^2} \tag{15}$$

$$WCSF_i = \frac{\sum_j W_j}{W_i}\cdot\frac{{V_{max}}^2\cdot{I_{rms}}^2}{P^2} \tag{16}$$

$$CCSF_i = \frac{\sum_j W_j}{W_i}\cdot\frac{{V_{pk}}^2\cdot{I_{rms}}^2}{P^2} \tag{17}$$

$$SCSF = \sum_{Semiconductors} SCSF_i \tag{18}$$

$$WCSF = \sum_{Windings} WCSF_i \tag{19}$$

$$CCSF = \sum_{Capacitors} CCSF_i \tag{20}$$

In (15)-(17) $\sum_j W_j$ represent the total available resources for each component and W_i represent the amount of resources assigned to the specific component. In order to minimize the different CSF values, the resources can be differently

distributed by using the W_i weighting factors however, as first iteration the resources are supposed equally distributed. In (18)-(20) each component represents a specific stress; therefore, a CSF comparison requires to compare only components of the same type.

A. CSF Analysis for the Candidate Topologies

The results from the CSF analysis are presented in Fig. 5. The plots are shown as function of the converters operating voltages and currents on the low voltage side. The converter voltage on the high voltage side is fixed at 750 V and a summary of the dc-dc converter specifications used for the analysis is presented in Table II. The maximums values have been limited in order to have more comprehensive plots.

From Fig. 5 it can be observed that the values of the IFBBC's CSF (SCSF, WCSF and CCSF shown in Fig. 5a, 5b and 5c respectively) increase as the converter operating voltage on the LV-side decreases and the values are independent on the operating current. The transformer turns ratio also affects the values of the CSF; in the case of the IFBBC, the transformer turns ratio n=8 is chosen in order to minimize the voltage stress on the LV-side power semiconductors. Similarly, the SCSF, WCSF and CCSF values for the DAB topology are presented in Fig. 5d, 5e and 5f respectively. In this case, all the CSF values vary with both converter voltage and current. This is due to the variation of the phase-shift angle that controls the power flow in the DAB. For all the CSF values of the DAB, there is a minimum defined by the transformer voltage transfer ratio between primary and secondary. In this case, the optimal transformer ratio n=14 was selected in the middle of the converter voltage operating range on the LV-side. By varying the number of transformer turns, it is possible to move the CSF minima to other converter operating points.

TABLE II
DC-DC CONVERTER PARAMETERS FOR CSF ANALYSIS

LV-side voltage	30-80 V
LV-side current	0-80 A
HV-side voltage	750 V
Transformer turns ratio	8 (IFBBC), 14 (DAB)

There is a major difference in the distribution of the CSF values within the two analyzed topologies: for specific operating points, the minimum value of SCSF and CCSF is lower for the DAB topology compared to the IFBBC. However, the IFBBC has lower WCSF over the entire converter operating range. In all the CSF values the DAB has a minimum at 54 V and 7 A; while, the IFBBC has always a minimum at 80 V on the converter LV-side. The major difference in the CSF values is observed for the WCSF: the IFBBC has very low WCSF while these values for the DAB are large due to the large ac-currents and voltages that continuously stress the magnetic components. The CSF values of the IFBBC increase at low voltage levels; this trend is homogeneous over the entire converter operating range. On the other hand, in the DAB, the CSF values widely increase especially at low current levels, when the converter is operating outside its optimal voltage transfer ratio, e.g. 54 V with n=14.

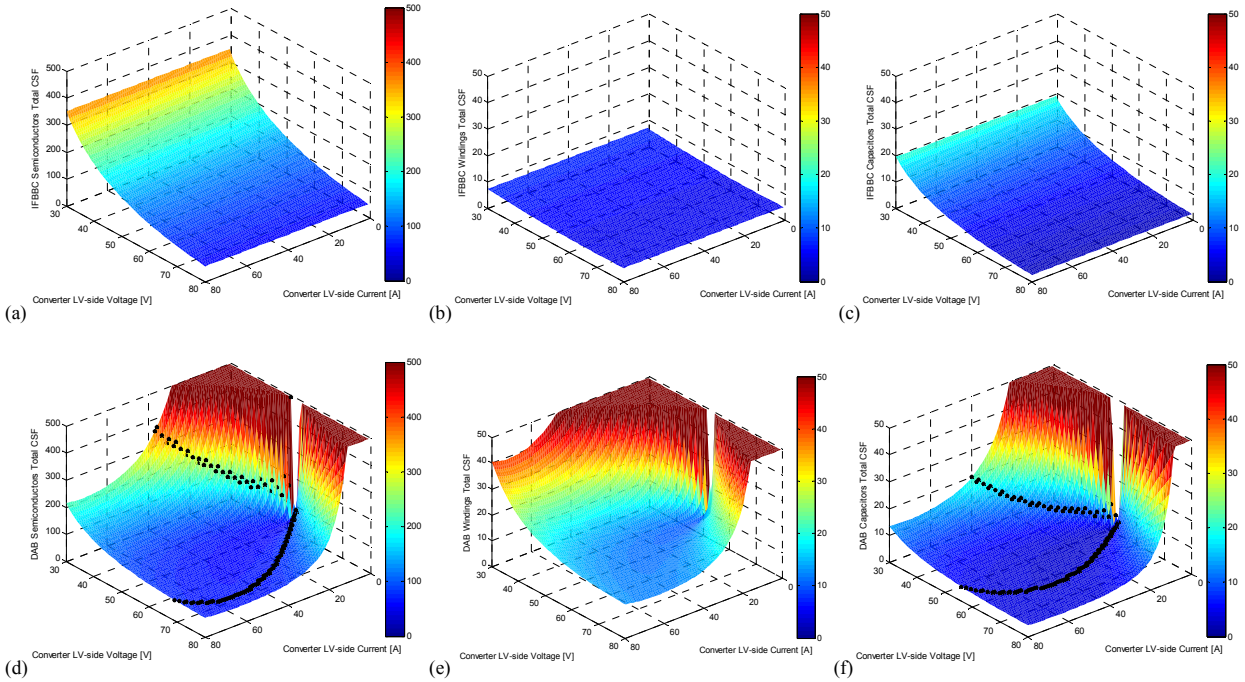


Fig. 5 IFBBC topology CSF: SCSF in (a), WCSF in (b) and CCSF in (c). DAB topology CSF: SCSF in (d), WCSF in (e) and CCSF in (f). Black dots in (d) and in (f) represent the intersection between the IFBBC CSF and the DAB CSF values.

TABLE III
AVERAGE CSF VALUES DEPENDING ON THE OPERATING MODE

Topology	SCSF	WCSF	CCSF
IFBBC FC-mode	217.8	6.5	11.3
DAB FC-mode	816.3	153.1	51.0
IFBBC EC-mode	109.0	5.5	5.3
DAB EC-mode	259.7	48.7	16.2

In order to select the most suitable topology, it is not only necessary to perform a CSF analysis, but it is also necessary to consider the overall system in which the dc-dc converter is expected to operate. Based on the cells stack characteristics presented in Section II, an I-V curve of the cell stack is built for both SOFC and SOEC operating modes [9]. The I-V model is used to determine all converter operating points. The converter CSF values are computed and averaged for all SOFC operating points and for all SOEC operating points. The obtained CSF values for SOFC and SOEC operation of the dc-dc converter are presented in Table III.

From the averaged CSF values it is interesting to observe that for both system operating modes (SOFC and SOEC) the average CSF of the IFBBC is significantly lower than the DAB. The IFBBC's average SCSF in FC-mode is 1/4 of the DAB's average SCSF in the same mode. The difference in average SCSF is to 1/2-1/3 in EC-mode. Similar differences are observed also in the average CCSF values. The IFBBC's average CCSF is about five times lower in FC-mode than the DAB; this difference is reduced down to three times for the EC operating mode. The largest difference is observed in the magnetic components stress factor, in this case the IFBBC has an average WCSF which is almost $1/20^{th}$ in FC-mode and $1/10^{th}$ in EC-mode compared to the DAB's average WCSF. The DAB has a high average WCSF due to the ac current circulating in the transformer windings and to the fixed duty cycle of the phase-shift modulation.

On overall, the IFBBC has lower CSF values and a more homogeneous variation over the entire converter operating range. It should be observed that for fixed operating points the DAB would be preferable. However, when computing averaged values, the large CSF values that are observed in non-optimal operating points of the DAB give large contribution and therefore, they have a large weight on the overall average.

TABLE IV
IFBBC DC-DC CONVERTER CHARACTERISTICS

Voltage primary side (LV)	30-80 V
Maximum current primary side	80 A
Voltage secondary side (HV)	700-800 V
Maximum power	2400-6400 W
Low Voltage (LV) side MOSFETs	120V 4.1mΩ TK72E12N1 2 in parallel
High Voltage (HV) side SiC MOSFETs	SCT30N120 SiC MOS C4D15120 SiC diode
Inductor	20 µH
Inductor core size/material	3xE6030 KoolMu 90-26-90
Turn ratio n	1:8
Transformer core size/material	2xE64 pairs/Magnetics R
Switching frequency	40 kHz

V. EXPERIMENTAL PROTOTYPE OF A ISOLATED FULL BRIDGE BOOST CONVERTER

The dc-dc converter for fuel cells is expected to operate with a variety of cells stacks; therefore the dc-dc converter is required to operate over the entire I-V specification in Table I. This requirement is necessary since the SOEC/SOFC technology if not fully mature and variations in the I-V characteristics are expected. Moreover, the I-V curve of SOEC/SOEC stacks depends also on the stack operating conditions (temperature, fuel composition, etc.). The IFBBC topology is selected since it has a more homogenous distribution of the CSF thus, a more homogeneous distribution of the converter efficiency is expected.

The converter prototype of a high efficiency IFBBC for bidirectional fuel cells, shown in Fig. 6a, has been developed and tested. The initial converter prototype was based on Si MOSFETs, Si IGBTs and SiC diodes. This prototype was capable of achieving efficiencies up to 97.8% and 96.5% [9][10] depending on the power flow direction. The converter was then updated with SiC MOSFETs in the full bridge of the converter HV-side. Its main operating waveforms at 60 V 80 A are shown in Fig. 6b and a summary of the converter

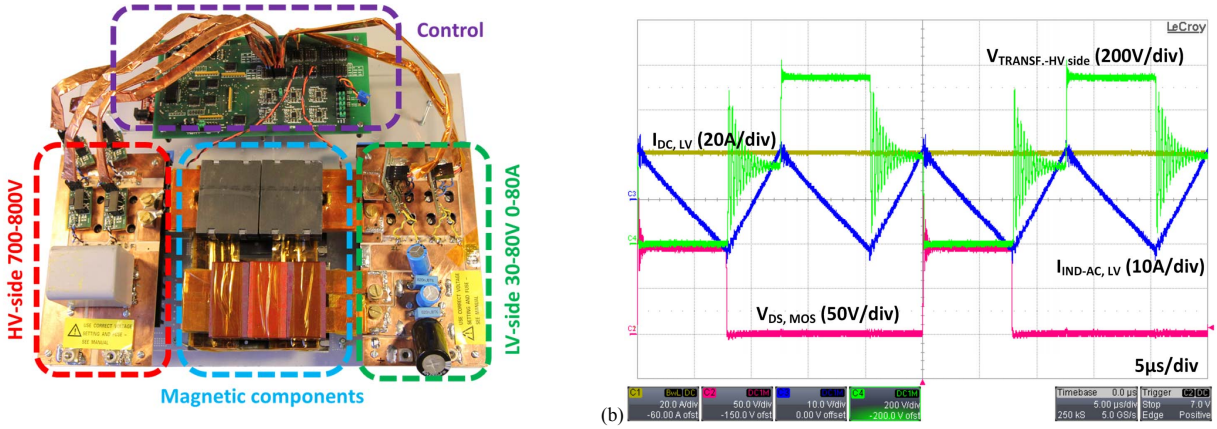
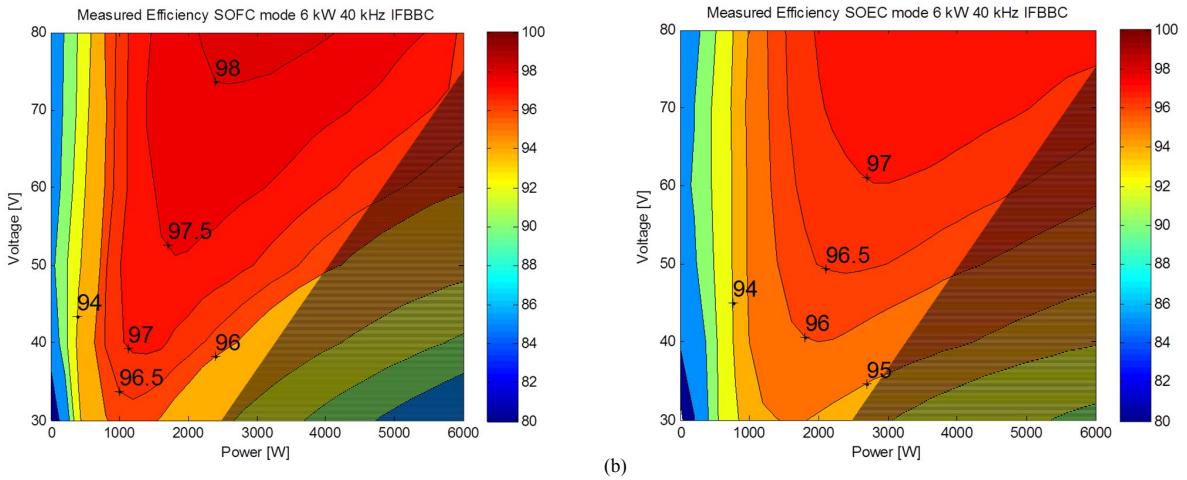


Fig. 6 IFBBC prototype highlighted its main components (a) and main operating waveforms at 60 V 80 A (b).



(a) (b)

Fig. 7 Measured efficiency of the IFBBC prototype for fuel cell operating mode (a) and for electrolyzer cell operating mode (b). Peak efficiency in SOFC mode 98.2% and in SOEC mode 97.45%. Darkened area indicates current limitation of the dc-dc converter.

characteristics is presented in Table IV. The converter magnetics are based on custom planar cores in high frequency ferrite for the transformer (Magnetics R-type material) and in distributed gap material (Magnetics KoolMu) for the boost inductor.

The new converter based SiC active switches is capable of achieving efficiencies up to 98.2% when operating in fuel cell mode (power flow from the converter LV-side to the HV-side) and up to 97.45% with reversed power flow, as shown in Fig. 7a and 7b respectively. The highest dc-dc conversion efficiencies are always measured with a current of ~40 A and at the highest converter voltage on the LV-side (80 V). At the lowest voltage on the LV-size (30 V) the converter achieved an efficiency above 96% and 95% depending on the direction of the converter power flow, as shown in Fig. 7a and 7b.

VI. Conclusions

This paper presents a component stress factor (CSF) analysis of the isolated full bridge boost converter (IFBBC) and of the dual active bridge (DAB) operating with phase-shift modulation. The analysis focuses on bidirectional dc-dc converters for fuel cell applications since they require wide operating voltage and current ranges.

The analysis highlights that the DAB has a lower absolute CSF however, the CSF in the DAB rapidly increases as the operating conditions deviate from the optimal operating point. In the DAB, the CSF varies along with both converter voltage and current; while in the IFBBC it depends only on the converter operating voltage. The IFBBC has a lower at average CSF which is also independent from the converter current. The bidirectional fuel cell I-V characteristic has been used to compute an average CSF for both fuel cell and electrolyzer cell operating modes. This highlighted that the IFBBC is a preferable topology for wide operating voltage ranges.

A 6 kW (30-80 V 80 A boosted up to 700-800 V) converter prototype of an IFBBC has been developed. The converter is based on high current fully planar magnetics and is capable of achieving peak efficiency of 98.2% in fuel cell mode and of 97.45% in regenerative mode.

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