Thermal Aware Floorplanning Incorporating Temperature Dependent Wire Delay Estimation - DTU Orbit (08/11/2017)

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Temperature has a negative impact on metal resistance and thus wire delay. In state-of-the-art VLSI circuits, large thermal gradients usually exist due to the uneven distribution of heat sources. The difference in wire temperature can lead to performance mismatch because wires of the same length can have different delay.

Traditional floorplanning algorithms use wirelength to estimate wire performance. In this work, we show that this does not always produce a design with the shortest delay and we propose a floorplanning algorithm taking into account temperature dependent wire delay as one metric in the evaluation of a floorplan. In addition, we consider other temperature dependent factors such as congestion and interconnect reliability.

The experiment results show that a shorter delay can be achieved using the proposed method.

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Authors: Winther, A. (Ekstern), Liu, W. (Ekstern), Nannarelli, A. (Intern), Vrudhula, S. (Ekstern)
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