Low Power High Dynamic Range A/D Conversion Channel

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PhD Thesis, August 2015

DTU Electrical Engineering
Department of Electrical Engineering

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To Marianne, Karen and Viggo

Preface and Acknowledgment

This thesis is submitted in partial fulfillment of the requirements for obtaining the PhD degree from the Technical University of Denmark. The project has been carried out as an Industrial PhD project in collaboration with DTU Electrical Engineering and the SAW Design Center Denmark, part of the SAW Business Group of EPCOS AG. The project was supervised by Professor Erik Bruun and company supervisor Pirmin Rombach in the period from March 2012 to August 2015, including 26 weeks of leave from the project. The project was partially by EPCOS AG and partially by Innovation Fund Denmark through the Industrial PhD program.

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Abstract

This work concerns the analysis of an adaptive analog-to-digital (A/D) conversion channel for use with a micro electromechanical system (MEMS) microphone for audio applications. The adaptive A/D conversion channel uses an automatic gain control (AGC) for adjusting the analog preamplifier gain in the conversion channel in order to avoid distortion for large input signals. In combination with a low resolution A/D converter (ADC) and a digital gain block, the adaptive A/D conversion channel achieves an extended dynamic range beyond that of the ADC. This in turn reduces the current consumption of the conversion channel in comparison to a static A/D conversion channel; this at the cost of a reduced peak signal-to-noise ratio (SNR).

The adaptive A/D conversion channel compensates for the change in analog gain by a digital gain, thus achieving a constant channel gain in the full dynamic range. However, this compensation results in the generation of audible transient errors in the conversion channel output. The adaptive conversion channel is modeled in order to analyze the factors that impact the performance of the conversion channel, including the generation of the transient error. To evaluate the audibility of the transient errors, an objective method based on the *Perceived Evaluation of Audio Quality* (PEAQ) method is investigated and compared with a subjective evaluation. The results of the evaluation provide key knowledge about the transient glitches from both a system and psychoacoustical point-of-view. Based on this knowledge, a new method is proposed for the reduction of the transient glitches, based on linear extrapolation of the channel output signal.

The design of a low power continuous-time (CT) Delta-Sigma ($\Delta\Sigma$) ADC for use in the adaptive A/D conversion channel is also presented. When designing a CT $\Delta\Sigma$ ADC, the choice of e.g. integrator topology, feedback waveform, feedback type, noise transfer function, and quantization levels, results in a large design space, both at the modulator and circuit level. A new optimization method is presented, that seeks to minimize the current consumption of the ADC. Based on an analysis of the modulator circuits and loopfilter, the optimization method determines a theoretical minimum current solution based on a set of performance requirements. Furthermore the use of current mode feedback in combination with active-RC integrators in the CT $\Delta\Sigma$ ADC is investigated as a method for reducing the current consumption of the ADC, without sacrificing the noise performance of the ADC.

The main scientific contributions described in this thesis can be divided into two parts: contributions related to AGC audio systems, and contributions related to low power CT $\Delta\Sigma$ ADC design. In the area of AGC audio systems, the main contributions are: an overview of the challenges in applying AGC to audio systems; a proposed objective method for evaluating the audibility of the transient glitches generated by the adaptive A/D conversion channel; and method for reducing the

transient glitches generated by the adaptive A/D conversion channel.

In the area of low power CT $\Delta\Sigma$ ADC design a substantial contribution is given. The presented optimization method and the use of current mode feedback identifies the possibilities of achieving a low power design by considering the modulator and circuit design as interdependent rather than two separate parts of the design.

Dansk Resumé

Denne afhandling vedrører analysen af en adaptiv analog-til-digital (A/D) konverteringskanal til anvendelse sammen med en mikro-elektromekanisk system (MEMS) mikrofon til audio brug. Med henblik på at undgå forvrængning af store indgangssignaler anvender den adaptive A/D konverteringskanal en automatisk forstærkningsstyring (AGC) til justering af forstærkningen af en analog forforstærker i konverteringskanalen. I kombination med en lav-opløsnings A/D konverter (ADC) og en digital forstærkerblok opnår den samlede adaptive A/D konverteringskanal et dynamikområde, som er større end ADC'ens eget dynamikområde.

Den adaptive A/D konverteringskanal kompenserer for ændringen i den analoge forstærkning via en digital forstærkning og opnår dermed en konstant kanalforstærkning i hele dynamik området. Imidlertid resulterer denne kompensering i generering af hørbare transiente fejl i udgangssignalet fra konverteringskanalen. Den adaptive konverteringskanal er blevet modelleret med henblik på at analysere de faktorer, der påvirker egenskaberne af konverteringskanalen, inklusiv genereringen af de transiente fejl. Til evaluering af hørbarheden af de transiente fejl er der udviklet en objektiv metode, baseret på *Perceived Evaluation of Audio Quality* (PEAQ) metoden. Metoden er blevet sammenlignet med en subjektiv evaluering baseret på lyttetests. Resultaterne heraf giver vigtig viden om de transiente fejl, både fra et systemperspektiv og fra et psykoakustisk perspektiv. På grundlag af denne viden foreslås en ny metode til reduktion af de transiente fejl. Metoden er baseret på lineær ekstrapolering af kanalens udgangssignal.

Afhandlingen omhandler også design af lav-effekt, kontinuert-tid (CT) Delta-Sigma ($\Delta\Sigma$) ADC'er til anvendelse i den adaptive A/D konverteringskanal. Ved design af en CT $\Delta\Sigma$ ADC fører valget af f.eks. integratortopologi, tilbagekoblingskurveform, støj-overføringsfunktion og antal kvantiseringsniveauer til et stort antal frihedsgrader, både på modulatorniveau og på kredsløbsniveau. Der præsenteres en ny optimeringsmetode til minimerering af strømforbruget af ADC'en. Baseret på en analyse af modulatorkredsløbene og sløjfefilteret bestemmer optimeringsmetoden en teoretisk løsning med et minimum af strømforbrug ud fra en række krav til øvrige specifikationer. Yderligere undersøges anvendelsen af strømbaseret tilbagekobling i kombination med *active-RC* integratorer til CT $\Delta\Sigma$ ADC'en som en metode til reduktion af ADC'ens strømforbrug, uden at der gås på kompromis med ADC'ens egenstøj.

De væsentlige videnskabelig bidrag i dette ph.d. projekt kan opdeles i to dele: bidrag vedrørende AGC i audio systemer og bidrag vedrørende design af lav effekt CT $\Delta\Sigma$ ADC'er.

Inden for AGC audio systemer er de primære bidrag følgende: (1) et overblik over udfordringerne ved anvendelse af AGC i audiosystemer; (2) en objektiv metode til evaluering af hørbarheden af de transiente fejl, der genereres i den adaptive A/D

konverteringskanal; (3) en metode til reduktion af de transiente fejl i udgangen af den adaptive A/D konverteringskanal.

Inden for området omhandlende CT $\Delta\Sigma$ ADC design er den udviklede optimeringsmetode et væsentligt bidrag. Denne metode samt anvendelsen af strømbaseret tilbagekobling viser, hvordan der er muligt at opnå et design med lavt strømforbrug ved at betragte design af modulator og kredsløb som indbyrdes afhængige opgaver fremfor som to separate dele af designet.

Contents

List of Abbreviations

3I2AFC	Three interval, Two Alternative Forced Choice
3I3AFC	Three interval, Three Alternative Forced Choice
A/D	Analog-to-Digital
AAF	Anti Aliasing Filter
ADB	Average Distorted Block
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AOP	Acoustical Overload Point
CIFB	Cascade of Integrators with Feedback
CIFF	Cascade of Integrators with Feedforward
CMFB	Common-Mode Feedback
CRFB	Cascade of Resonators with Feedback
CT	Continuous-Time
DEM	Dynamic Element Matching
DGB	Digital Gain Block
DR	Dynamic Range
DT	Discrete-Time
ECM	Electret Condenser Microphone
ENOB	Effective number of bits
ESD	Electrostatic Discharge
FIR	Finite Impulse Response
FoM	Figure-of-Merit
GBW	Gain-Bandwidth Product
IC	Integrated Circuit
LPF	Low-pass Filter

MEMS	Micro Electro Mechanical System
MFPD	Mean Filtered Probability of Detection
MIM	Metal-Insulator-Metal, in the context of MIM capacitors
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MOV	Model Output Variable
MSA	Maximum Stable Amplitude
MSE	Mean Squared Error
MUX	Multiplexer
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OpAmp	Operational Amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PDM	Pulse Density Modulation
PEAQ	Perceptual Evaluation of Audio Quality
PEX	Parasitic Extracted
PSD	Power Spectral Density
PVT	Process, Voltage and Temperature
RZ	Return-to-Zero
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SPL	Sound Pressure Level
SR	Slew Rate
STF	Signal Transfer Function
THD	Total Harmonic Distortion
VGA	Variable Gain Amplifier

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1

Introduction

This chapter provides an introduction to the PhD project documented by this thesis. The motivation for the project is given, and an overview of the sections of the thesis is provided.

In the last 30 years the research in Micro Electro Mechanical Systems (MEMS) has been continuously growing. This has led to the commercialization of several products, including MEMS microphones. Compared to electret condenser microphones (ECM), MEMS microphones are smaller, thereby allowing for integration into smaller devices or having multiple microphones in e.g. a smartphone. The ECM microphones require a permanent charge on the backplate of the microphone, miking it sensitive to high temperature. The MEMS microphone is instead charged by a charge-pump circuit when operating; as a result, it is possible to reflow solder the MEMS microphone when mounting it on a printed circuit board (PCB). The MEMS microphone is silicon based and fabricated using standard fabrication methods developed by the semiconductor industry over the years. Batch processing is therefore possible, resulting in a low variation in the performance of the fabricated microphones.

The market for MEMS microphones has increased significantly in recent years [1], with the market revenue in 2010 at $US 200 million and forecasted to increase to $US 1400 million in 2017. About 40 % of this market revenue in 2017 is from very high performance microphones, characterized by a high signal-to-noise ratio (SNR) and a high dynamic range (DR). Having a larger dynamic range in the microphone reduces the risk of clipping of the audio signal due to very large sound pressure levels; high sound pressure levels may occur at a concert venue from the subwoofers or due to wind noise.

To characterize the performance of the microphones, the microphone SNR is specified for an acoustical input of 1 Pa, equal to 94 dB sound pressure level (SPL). The acoustical overload point (AOP) defines the maximum acoustical input of the microphone at which the microphone output signal has 10 % total harmonic distortion (THD). From the reference SNR and the AOP the dynamic range of the microphone may be calculated as:

$$\mathrm{DR_{mic}} = \mathrm{SNR_{1Pa}} + \mathrm{AOP} - 94\ \mathrm{dB} \tag{1.1}$$

Table 1.1: Performance overview of some of the commercially available high SPL MEMS microphones

Microphone	SNR_{1Pa}	AOP	DR	I_{tot}	Interface
InvenSense					
INMP411 [2]	62 dB(A)	131 dB SPL	99 dB	250 µA	analog
INMP510 [3]	65 dB(A)	124 dB SPL	95 dB	180 µA	analog
ICS-40300 [4]	63 dB(A)	130 dB SPL	99 dB	220 µA	analog
INMP621 [5]	65 dB(A)	133 dB SPL	104 dB	1200 µA	digital
Knowles					
SPA2629LR5H [6]	65 dB(A)	123 dB SPL	94 dB	120 µA	analog
SPH0641LM4H [7]	64.3 dB(A)	120 dB SPL	90.3 dB	620 µA	digital
SPK1638LM4H [8]	64.5 dB(A)	122 dB SPL	92.5 dB	460 µA	digital
EPCOS					
C928 [9]	66 dB(A)	135 dB SPL	107 dB	140 µA	analog

In the current microphone market a range of microphones with a high dynamic range around 100 dB is available from different manufacturers. A list of analog and digital microphones is given in Table 1.1, stating the main performance parameters of the microphones. From the table it can be seen that for the same dynamic range, the current consumption of the digital microphones is significantly larger than for the analog microphones. Basically the analog microphone consists of a MEMS sensor and an analog amplifier circuit, while the digital microphone has an additional analog-to-digital converter (ADC). The ADC is thus the cause of the high current consumption of the digital MEMS microphones. As the market asks for digital MEMS microphones with dynamic ranges around 110 dB, the current consumption will increase further due to the increased dynamic range requirements of the ADC used in the microphone.

Designing an ADC with a dynamic range above 10 dB and with low current consumption is a difficult challenge, since all non-idealities need to be taken into account at this performance level. A state-of-the-art $\Delta\Sigma$ ADC for audio applications is presented in [10] that achieves a dynamic range of 106 dB, but with a current consumption of 5.4 mA. It should be noted that this is including the decimation filter of the ADC. In digital MEMS microphones the output signal is typically pulse density modulated (PDM) and output as a 1-bit data stream at the sampling frequency of the ADC; thus, the decimation filter is not needed in the digital MEMS microphone. The INMP621 digital microphone from InvenSense [5] achieves a dynamic range of 104 but with a current consumption of 1200 mA. The results from [10] and the available digital microphones indicate, that for digital microphones with 110 dB dynamic range the current consumption will be in range of 1.5 mA to 2 mA.

The main problem of the digital microphone is the requirement of the ADC to have a dynamic range larger than that of the MEMS sensor. Thus, if this ADC requirement is relaxed, a lower current digital MEMS microphone may be created. The C928 analog microphone from EPCOS [9] has a dynamic range of 107 dB

with a current consumption of 140 μA. If a digital microphone could be designed with a similar dynamic range and with a current consumption below 1 mA, this would be a significant benefit for the company from a commercial point of view.

The project documented in this thesis concerns the investigation of an adaptive analog-to-digital (A/D) conversion channel for use in a digital MEMS microphone. The preamplifier and the ADC of the microphone may be viewed as an A/D conversion channel. Typically the gain of the preamplifier is fixed, but by adaptively adjusting the gain of the preamplifier based on the input signal level, the dynamic range of the conversion channel may be extended. This has the benefit of not requiring that the ADC has a dynamic range equal to that of the conversion channel; thus, a lower performing ADC may be used, thereby reducing the total current consumption of the microphone.

1.1 Thesis Outline

This thesis consists of eight chapters that can be split into three parts. The first part of the thesis, consisting of Chap. 2-4, covers the system level aspect of the high dynamic range A/D conversion channel.

Chapter 2 provides an introduction to the topic of A/D conversion channels. A detailed description is given of the adaptive A/D conversion channel uses an automatic gain controller for adjusting the channel gain configuration, thereby extending the dynamic range of the channel. Important properties of the adaptive A/D conversion channel are described, with emphasis on the automatic gain controller. The non-idealities generated by the conversion channel and added to the channel output signal due to the gain adjustment in the channel, are discussed and possible solutions are described.

Chapter 3 presents an objective method for the evaluation of the audibility of the transient glitches generated by the adaptive A/D conversion channel. The objective evaluation is based on parts of the psychoacoustic model that is used in the objective *Perceptual Evaluation of Audio Quality* method. The proposed method is compared with the results of a subjective evaluation in the form of a listening test. The chapter is based on the ICASSP 2014 conference paper: *Objective Evaluation of the Audibility of Transient Errors in an Adaptive A/D Conversion Channel*.

Chapter 4 presents a method for reducing the transient glitches of the adaptive A/D conversion channel. The method replaces the output signal of the channel by a linear estimate, while the conversion channel settles after a gain change. The chapter is based on a patent application submitted to the European Patent Office: *PCT/EP2014/059488 - Circuit and Method of Operating Circuit*.

The second part of the thesis covers the design of low power continuous-time ΔΣ ADCs for application in the adaptive A/D conversion channel.

Chapter 5 presents a brief introduction to the topic of ΔΣ modulation and

continuous-time $\Delta\Sigma$ modulators. An optimization method is then presented for the design of low power continuous-time $\Delta\Sigma$ ADC. The optimization is based on an analysis of the modulator and the circuit blocks of the ADC. By taking the circuit implementation into account when designing the modulator, the method tries to determine the minimum current design based on a set of performance requirements. The chapter is based on the NORCHIP 2014 conference paper: *Optimization of Modulator and Circuits for Low Power Continuous-Time Delta-Sigma ADC*.

Chapter 6 presents the design of a low power continuous-time $\Delta\Sigma$ ADC, where a current mode DAC is used in combination with active-RC integrators. This combination relaxes the noise requirements of the 1st integrator of the ADC, resulting in a lower power solution in comparison to the use of voltage mode feedback. The designed ADC is described in detail, and the performance results are presented including suggestions on how further to improve the design . The chapter is based on the ECCTD 2015 conference paper: *Low Power Continuous-Time Delta-Sigma ADC with Current Output DAC*.

Chapter 7 summarizes the results of the thesis project, and the recommendations for future work.

Chapter 8 briefly describes the other research work that has been carried out during the PhD project. This includes the design of a new university course on practical IC design; a study on the use of coaching and personal feedback as a way of improving the generic engineering competences of students; and a study on the problems of using automatic gain control in audio applications. The chapter is based on three conference publications presented at the NORCHIP 2013 conference, the CDIO 2014 conference, and the PRIME 2015 conference.

A graphical overview of the thesis chapters and related publications is given in Fig. 1.1.

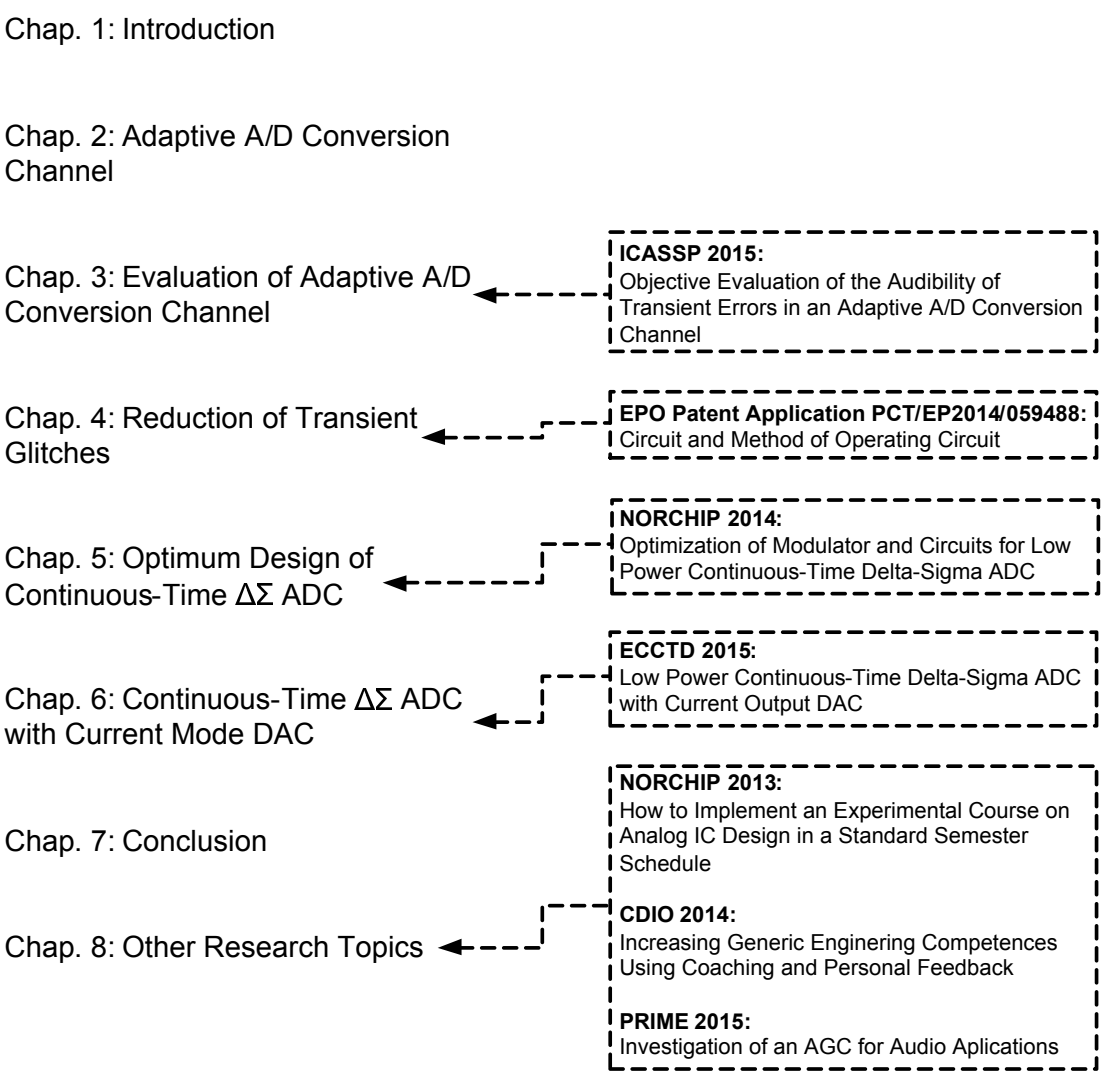


Figure 1.1: Overview of thesis chapters and related publications

2

Adaptive A/D Conversion Channel

This chapter introduces the adaptive A/D conversion channel for the purpose of achieving a high dynamic range conversion channel with a low power consumption. The chapter is intended as an overview to the topic, and provides a description of the different parts of the conversion channel, with the main emphasis being on the automatic gain controller that is at the core of the channel. The issues related to the application of the automatic gain control are discussed and possible solutions are presented.

2.1 Static A/D Conversion Channel

When considering an A/D conversion channel for a sensor, the dynamic range of the conversion channel should be larger than, or equal to, that of the sensor. The simplest A/D conversion channel consists of a preamplifier with a fixed gain and an analog-to-digital converter, as shown in Fig. 2.1. The dynamic range of the channel is limited by two factors: the supply voltage and the noise floor. The supply voltage sets an upper limited on the input signal that the channel is able to process without clipping the signal. Clipping is unwanted as it causes harmonic distortion in the output signal. The noise floor determines the minimum signal power that may be detected.

The noise of the static A/D conversion channel, when referred to the input of the channel, is given as:

$$v_{n,irn}^2 = v_{n,mic}^2 + \frac{1}{G_a^2}\left(v_{n,preamp}^2 + v_{n,ADC}^2\right) \tag{2.1}$$

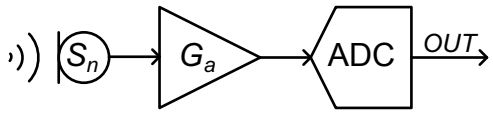


Figure 2.1: Block diagram of static A/D conversion channel

where $v_{n,irn}^2$ is the input referred noise power of the channel, $v_{n,mic}^2$ is the microphone noise power, $v_{n,preamp}^2$ is the output noise power of the preamplifier, $v_{n,ADC}^2$ the equivalent ADC noise power at the input of the ADC, and G_a is the analog preamplifier gain. Generally, the A/D conversion channel should be designed so that the microphone noise is the dominant noise source. Furthermore, $v_{n,preamp}$ should be smaller than $v_{n,ADC}$ in order to fully utilize the resolution and dynamic range of the ADC. From (2.1) it is seen, that the noise of the preamplifier and the ADC is reduced by the gain of the preamplifier.

Generally the circuit noise relates to the current consumption of the circuits: the gate referred thermal noise power of a MOSFET is given as [11]:

$$v_{g,therm}^2(f) = \frac{8}{3}kT\frac{1}{g_m} \tag{2.2}$$

where k is the Boltzmann constant, T the absolute temperature, and g_m the transistor transconductance. From the Schichmann-Hodges model of the MOSFET, the value of g_m relates to the biasing current as:

$$g_m = \frac{2I_d}{V_{ov}} \tag{2.3}$$

where I_d is the biasing current, and V_{ov} is the transistor overdrive voltage. Thus, the thermal noise power of the MOSFET is inversely proportional to the biasing current, resulting in a large current consumption for low noise operation. The gate referred 1/f noise power of the MOSFET is given as [11]:

$$v_{g,1/f}^2(f) = \frac{K}{WLC_{ox}f} \tag{2.4}$$

where K is a process dependent constant, W the MOSFET gate width, L the MOSFET gate length, and C_{ox} is the gate capacitance per unit area. A low 1/f noise requires large transistors, which in turn results in a large gate capacitance. This adds a capacitive load to the preceding stages, thus implicitly increasing the current consumption. Finally, the quantization noise of the ADC depends on the ADC topology used in the conversion channel. Generally speaking, the larger the resolution, the higher the current consumption due to the increased number of active components in the ADC or higher sampling frequency.

In order to achieve a low current conversion channel, it is thus preferable to have a large preamplifier gain. However, this may conflict with the goal of utilizing the dynamic range of the sensor. Consider the case where a given static conversion channel has been designed, but it lacks 6 dB in dynamic range to match the dynamic range of the sensor. One solution is to increase the internal supply voltage of the circuit by the use of e.g. a voltage doubler. Assuming a constant current consumption and MEMS sensor sensitivity, then by doubling the supply voltage, the maximum signal level that may be processed in the channel without clipping is increased by 6 dB. However, doubling the supply voltage also double the power consumption since the biasing currents are unchanged. An alternative solution is to keep the supply voltage constant and instead dampen the sensor

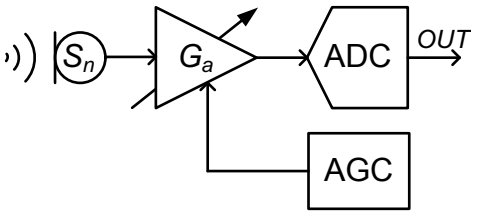


Figure 2.2: Block diagram of adaptive A/D conversion channel

signal by 6 dB. This also reduces the noise of the sensor by the same amount, thus requiring that the circuit noise of the conversion channel is reduced by 6 dB as well. Considering only thermal noise from the MOSFETs in the circuit, then from (2.2)-(2.3) a 6 dB improvement in noise would require quadrupling the biasing current; similarly, this increases the power consumption by a factor of four.

To obtain an increase of the dynamic range by 6 dB, the obvious solution appears to be applying a voltage doubler in the conversion channel. However, the voltage doubler circuit also requires current and area. Furthermore, the higher supply voltage may not be compatible with the process technology used for implementation of the circuits. Thus the

Overall the static A/D conversion channel is limited by the requirement that the circuits blocks need a dynamic range equal to that of the MEMS sensor. In applications where a very high dynamic range is required, but where the related increase in power consumption is not acceptable, the static A/D conversion channel is not a viable solution.

2.2 Adaptive A/D Conversion Channel

The alternative to the static A/D conversion channel is an adaptive A/D conversion channel, where the preamplifier is realized as a variable gain amplifier (VGA), as shown in Fig. 2.2. The gain of the VGA may then be adjusted based on the level of the input signal from the sensor. For small input levels, a large gain is used in the VGA, while a small gain is used for large input levels. The gain level of the VGA may then be controlled by an adaptive gain controller (AGC) that monitors the signal level and adjusts the VGA gain accordingly.

The input referred noise of the adaptive A/D conversion channel is similar to that of the static A/D conversion channel given in (2.1), except for the variable gain:

$$v_{n,irn}^2 = v_{n,mic}^2 + \frac{1}{G_{a,VGA}(t)^2}\left(v_{n,VGA}^2 + v_{n,ADC}^2\right) \tag{2.5}$$

where $G_{a,VGA}(t)$ is the gain time-dependent of the VGA, and $v_{n,VGA}$ is the output noise of the VGA. From (2.5) it is given that for large $G_{a,VGA}$ the circuit noise is low; this occurs for small input signal levels. For large input signal levels the value of $G_{a,VGA}$, is reduced, thus increasing the circuit noise. Due to the gain

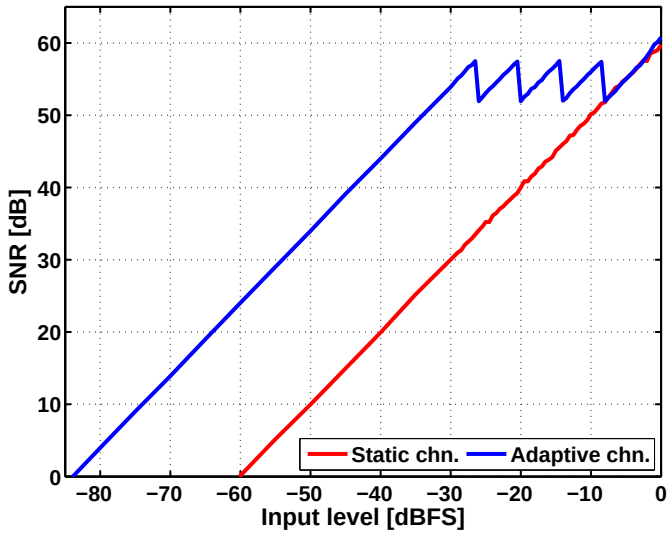


Figure 2.3: Example of SNR as a function of the input level for the static and the adaptive A/D conversion channel

adjustment, the dynamic range is in essence extended in comparison to the static gain conversion channel. This gain adjustment is handled by the AGC. In Fig. 2.3 is plotted the SNR as a function of the input signal level for both the static and the adaptive A/D conversion channel. As seen from the figure the dynamic range of the adaptive channel is extended beyond that of the static channel.

With AGC it is thus possible to design the VGA with a large gain for small input signals, which may relax the noise requirements of the VGA and the ADC. The peak SNR of the adaptive conversion channel is still limited by the noise of the VGA and the ADC. As the input signal increases, the SNR of the conversion channel stops to increase at the input level that triggers the first VGA gain reduction. As a result, dynamic range of the adaptive A/D conversion channel is not equal to the peak SNR of the channel. This behavior of the adaptive A/D conversion channel is clearly seen from the plots shown in Fig. 2.3. Nevertheless, the dynamic range of the conversion channel is improved without increasing the supply voltage of the circuits or reducing the noise of the circuit. Thereby for the same dynamic range, the current consumption of the adaptive A/D conversion channel will ideally be smaller than that of the static A/D conversion channel. The power consumption of the AGC and support blocks needs to be taken into account, when evaluating the overall reduction in current consumption. Overall, the adaptive conversion channel can primarily be used in applications where high dynamic range combined with low current consumption is more important than the peak SNR of the channel.

Unfortunately the addition of the VGA and the AGC in the conversion channel adds complexity to the system. Some of the questions that arise are:

- How many gain levels should the VGA have?
- How should the AGC detect the level of the signal being processed by the

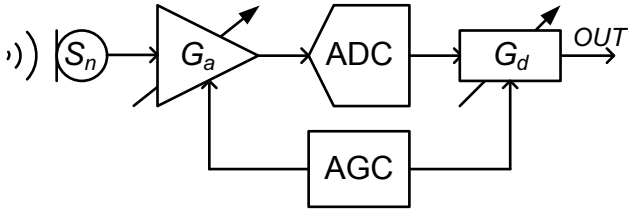


Figure 2.4: Block diagram of adaptive A/D conversion channel with digital compensation

channel?

- How should the AGC be implemented: analog or digital?
- How should the AGC block adjust the VGA gain?
- How should the varying channel gain be handled?
- How to handle transient errors generated when adjusting the VGA gain?

In the following sections these questions will be discussed in more detail.

2.3 Constant Channel Gain

For a microphone it is a desired property that the sensitivity is a time-invariant parameter, so that a given sound pressure level results in a specific output signal. With the adaptive A/D conversion channel depicted in Fig. 2.2, the same output level may be generated from several different input levels, due to the change of the VGA gain depending on the signal level; thus, the constant sensitivity property of the microphone is violated. In order to achieve a constant channel gain it is necessary to compensate for the reduction of the VGA gain. With the output of the A/D conversion channel being digital, the change in analog gain may be compensated digitally, as shown in Fig. 2.4. A similar approach was used in [12] for an adaptive A/D conversion channel for a bio-sensor array.

Thus, the total conversion channel gain, G_{chn}, is given as:

$$G_{chn} = G_a \cdot G_d \tag{2.6}$$

where G_d is the digital gain. When G_a is reduced, G_d is increased by the same factor, and vice versa when the G_a is increased. From a digital point of view, it is preferable that the digital gain levels are different by a factor in powers of 2, as this can easily be implemented digitally by a bit shift operation. Other gain factors require dedicated multiplier blocks which increases the digital power consumption, thus increasing the complexity. This also limits the gain steps used by the conversion channel to factors of powers of 2, thus minimum 6 dB.

A problem related to compensating the change in analog gain by means of a digital gain is the introduction of transient errors or transient glitches. The glitch

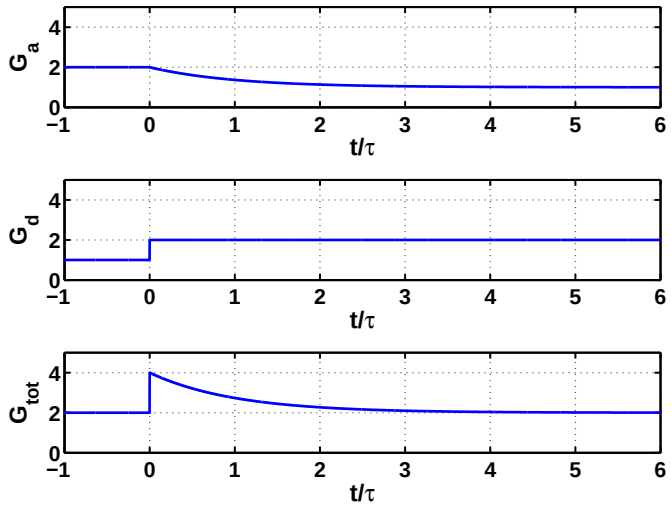


Figure 2.5: Analog gain, digital gain and channel gain during adjustment event

occurs due to different transition times when changing the analog and the digital gain, thus resulting in a non-constant channel gain during the gain transition. This is shown in Fig. 2.5 for a 1st order analog system. While the digital gain can be changed almost instantly on a sample by sample basis, the settling time of the preamplifier output after a gain change depends on the bandwidth of the amplifier.

A change of gain for a constant input level is equal to the situation of having a step pulse on the input of the preamplifier. For a 1st order system, with a time-constant τ, the time-constant is given as:

$$\tau = \frac{1}{f_{BW}} \tag{2.7}$$

where f_{BW} is the system frequency bandwidth. Applying the gain change at $t = 0$, then after $t = \tau$ the preamplifier output has settled to 63.2% of the final value. At $t = 5\tau$ the output is within 99.3% of the final value. Consider the case of an adaptive A/D conversion channel where the sampling frequency, f_s, is at the Nyquist rate of the signal bandwidth, $f_s = 2f_{BW,sig}$. For the output of the preamplifier to have settled to within 99.3% of the final value within a sampling period, requires that:

$$\tau = \frac{1}{5f_s} \Leftrightarrow f_{BW} = \frac{1}{\tau} = 5f_s = 10f_{BW,sig} \tag{2.8}$$

The result in (2.8) is only valid in case of the digital part of the conversion channel operating at the Nyquist rate. Thus in order to avoid any transient glitches in the channel output, the preamplifier needs to be significantly faster than dictated by the signal bandwidth. Higher bandwidth requires higher transconductance of the MOSFETs in the amplifier, which in turn requires higher biasing current. Avoiding transient glitches by increasing the bandwidth of the preamplifier is thus not an attractive solution for low power systems.

The generation of transient glitches is practically unavoidable in the adaptive A/D conversion channel, when applying digital gain compensation. A relevant question is then how large a transient glitch that can be tolerated in the output of the conversion channel. The transient glitch error, $e(t)$, may be analytically expressed as:

$$e(t) = \Delta G \cdot [h(t) - s(t)] \cdot x(t) \tag{2.9}$$

where ΔG is the change in gain, $h(t)$ is the Heaviside step function, $s(t)$ is the step response of the signal path from the amplifier output to the digital gain block, and $x(t)$ is the input signal to the digital gain block and the AGC detector. The peak glitch error thus depends on the gain step ΔG, the value of $x(t)$ at the moment of the gain change and the step response $s(t)$. The minimum value of ΔG is directly related to the step sizes used in the VGA, the value $x(t)$ is dependent on the signal level at the moment of the gain change, and $s(t)$ is dependent on the settling time of the VGA and conversion time of the ADC. By adjusting either one, the peak value of the glitch may be reduced. These parameters are discussed in more detail in Sec. 2.4.

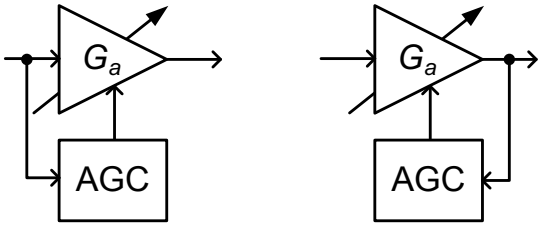
The question of how large a glitch that may be tolerated is more difficult to answer. Since the conversion channel is for audio applications, sound recorded using a MEMS sensor in combination with the conversion channel, will be played back to a person. Since the hearing of each individual is different, so is the perception of how large a glitch that may be tolerated. Thus, the psychoacoustical performance needs to be taken into account. This topic is evaluated further in Chap. 3.

Finally follows the question of how best to reduce the glitch error in the output of the conversion channel. From (2.9) it seems obvious to adjust ΔG, but this may not be the best solution. This is discussed further in Chap. 4.

2.4 Automatic Gain Control

The automatic gain control is a key part of the adaptive A/D conversion channel as it handles all changes of the VGA gain and the digital compensation. The topic of AGC systems has been thoroughly researched in the past, and are used in e.g. RF circuits for expanding the dynamic range of a receiver circuit. In [13] is presented a general overview of the topic for RF applications, including circuit examples. Some of the considerations for applying AGC to RF systems can also be applied to audio systems. A review of AGC theory is provided in [14], focusing on the theory for mainly analog AGC systems. In [15] is presented an analysis of AGC systems for audio applications, also with the focus on the theoretical analysis of the analog implementation. In [16] is given an analysis of distortion in AGC for audio systems, where the impact of the AGC loop delay on the signal distortion is discussed. However, in [13–16], the application of digital gain compensation is not investigated.

In this section an overview is given for the important properties and related



(a) AGC with feedforward **(b)** AGC with feedback

Figure 2.6: Types of AGC loops

Table 2.1: Pros and cons of feedback and feedforward AGC loops, adapted from [13]

	DR of input detector	Stability	Settling time
Feedforward	-	+	+
Feedback	+	-	-

considerations when designing the AGC system for the adaptive A/D conversion channel with digital gain compensation and for audio signals.

2.4.1 AGC Loops

The purpose of the AGC system in the adaptive A/D conversion channel is to adjust the channel gain settings. This with the aim of avoiding clipping in the analog domain for large input signals. Ideally, the AGC loop is able to instantly adjust the gain of the preamplifier in order to avoid clipping. In reality such an AGC is not realizable, as the AGC loop inherently has a delay that depends on the type of loop.

The loop of the AGC can be either feedback or feedforward based, depending on whether the AGC input is taken from the signal path before or after the preamplifier. Both loop types are depicted in Fig. 2.6.

Using a feedback based AGC has the benefit that the dynamic range of the peak detector only has to be as good as the dynamic range of the output of the preamplifier. However, feedback systems may be unstable which is a concern when controlling the amplifier gain. Furthermore, a feedback loop inherently increases the delay time of the AGC. A feedforward system is inherently stable, since there is no loop. For the same reason, the delay time of the AGC is much lower, making it possible for the AGC to react almost instantly when a large input signal occurs. However, with the peak detector connected to the input of the conversion channel, the peak detector requires a dynamic range equal to that of the input signal. For large dynamic ranges, this may be a problem. A summary of the pros and cons of the two loop types is given in Table 2.1.

For the A/D conversion channel it is also necessary to consider whether the peak detector and the AGC controller should be implemented in the analog domain,

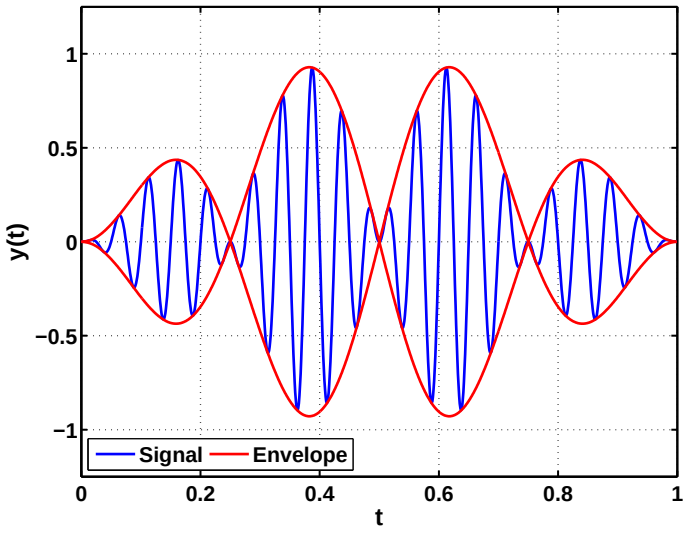


Figure 2.7: Signal and the associated signal envelope

the digital domain, or in mixed-mode. Since the output of the VGA is already converted to the digital domain, a solution is to realize both the peak detector and AGC in the digital domain. The attack and release levels of the AGC can be defined precisely in the digital domain and the AGC controller is easily realized using digital logic. The penalty is an additional delay in the control loop due to the delay of the A/D conversion, and an added delay due to the clock period of the system clock used for the digital circuits. Alternatively, a mixed-signal AGC may be used, where the peak detector is realized using analog circuits and the AGC in the digital domain. In the case of a feedback type AGC loop, the peak detector would only need a 2 bit output to identify whether the detected signal is above or below the attack and release levels. The mixed-signal approach would remove the detection delay due to the ADC, but would require the additional detection circuit.

Since the adaptive A/D conversion channel is intended for use with audio signals, the signal bandwidth of 20 kHz is fairly small. If the digital circuits are operated at a frequency of a few MHz, the processing delay of the ADC would be negligible. Since the adaptive A/D conversion channel already converts the signals to the digital domain, the simplest solution is to realize both the peak detector and the AGC controller in the digital domain. With the detector in the digital domain, the AGC loop is feedback based and the inherent delay somewhat counteracts the instability. However, the AGC may still oscillate if not designed properly.

2.4.2 Peak Detection

An important part of the AGC design is the detection principle to be used by the peak detector. A possible solution is to detect the signal level based on the signal envelope. The signal envelope is essentially the boundary in which the signal is contained in the time-domain, as depicted in Fig. 2.7. Alternatively, the signal

envelope can be described as the amplitude of a time-varying signal:

$$y(t) = A(t)\sin(2\pi f_0 t + \phi) \tag{2.10}$$

where $A(t)$ is the time-varying amplitude, f_0 is the signal fundamental frequency, and ϕ is the time-varying phase of the signal. The signal envelope, $e(t)$ is then given as:

$$e(t) = |A(t)| \tag{2.11}$$

The envelope of a signal may thus be found by determining the absolute value of the signal and low-pass the absolute value. From a digital point of view, the process of detecting the signal envelope is thus simple. However, the low-pass filter will add an extra delay to the AGC loop. Depending on the allowed ripple of the signal envelope, the delay of the envelope detector may be significant. Thus rapidly changing signals may not be detected sufficiently fast, resulting in signal clipping at the output of the preamplifier.

The alternative solution to envelope detection is to evaluate the instantaneous signal level, and then adjust the analog gain accordingly. This detection principle avoids the low-pass filter required by the envelope detector, and thus reduces the AGC loop delay. It is therefore faster at responding to a rapidly increasing signal at the input of the conversion channel. The downside of evaluating the instantaneous signal level is that for a constant amplitude sine wave, the signal will pass the attack level several times during a single signal period. Thus, additional control mechanisms are necessary in the AGC controller to avoid that the channel gain is adjusted up and down unnecessarily.

Since the main purpose of the AGC is to avoid clipping in the conversion channel, detecting the instantaneous signal level is preferred compared to the signal envelope, due to the added AGC loop delay.

2.4.3 Attack Level

Attack and release levels are defined for the AGC in order to set when the AGC should adjust the VGA gain based on the signal level sensed at the AGC input. More specifically, the attack level specifies when the AGC should reduce the VGA gain, while the release level specifies when the AGC should increase the VGA gain. To fully utilize the dynamic range of the VGA and ADC, the attack level should ideally be set at the clipping level of the VGA. However, due to the delay of the AGC loop it is necessary to set the attack level below the clipping level to avoid signal clipping. A valid question is then, how low the attack level should be set.

The attack level has a direct impact on the peak SNR that may be achieved in the conversion channel. Evaluating the SNR at the output of the preamplifier, the peak SNR may be expressed as:

$$SNR_{peak} = \frac{V_{attack}}{\sqrt{2} \cdot v_{n,rms}} \tag{2.12}$$

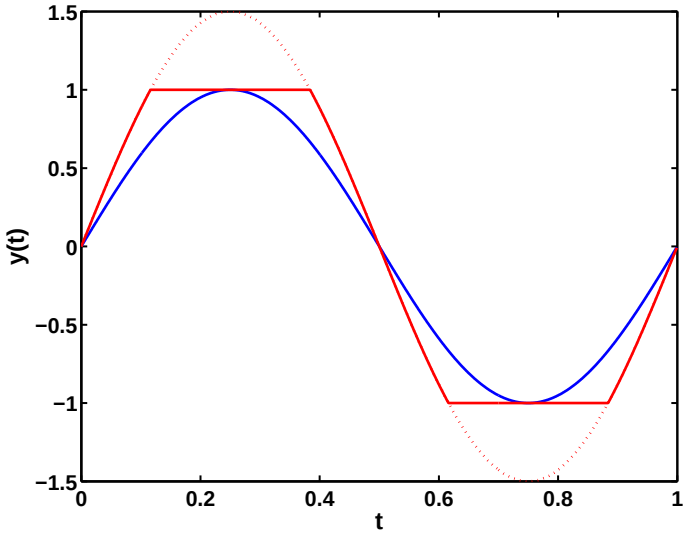


Figure 2.8: Sine wave without clipping (blue) and with clipping at $y(t) = 1$ (red)

where V_{attack} is the equivalent attack level voltage referred to the input of the ADC, and $v_{n,VGA+ADC,rms}$ is the rms noise from the conversion channel referred to the input of the ADC. From (2.12) it is evident that lowering the attack level reduces the peak SNR.

If the attack level is set too low, the dynamic range of the VGA and ADC are not fully utilized except in the case of VGA gain being at the minimum gain factor. On the other hand, if the attack level is too close to the clipping level, clipping may occur. An upper limit on the attack level may be determined from the knowledge of the maximum signal from the sensor and the signal bandwidth.

The selection of the attack level is thus a trade-off between avoiding signal clipping, and achieving the required peak SNR of the conversion channel.

To illustrate this problem, it is relevant to evaluate the worst case rise time of all input signal. The rate of change of a single frequency sine-wave given as:

$$y(t) = A \cdot \sin(2\pi f_0 t) \tag{2.13}$$

$$\Leftrightarrow \frac{dy}{dt} = 2\pi f_0 A \cdot \cos(2\pi f_0 t) \tag{2.14}$$

From (2.14) it follows that the maximum rate of change occurs periodically for $t = k/(2f_0)$, where k is an integer number. The maximum rate of change thus equals:

$$\left.\frac{dy}{dt}\right|_{max} = 2\pi f_{0,max} \cdot A_{max} \tag{2.15}$$

Thus, the maximum rate of change is given from the maximum signal frequency and the maximum input signal amplitude.

Based on (2.15), the worst case signal has a frequency of 20 kHz, being the upper limit of the audio signal band. However, from an acoustical point of view, this is not the worst case signal with respect to clipping. When clipping a sine-wave,

the top of the signal curve is flattened, as depicted in Fig. 2.8. In the extreme case, the sine-wave is converted into a square wave that may be expressed as a sum of sine-waves including the fundamental frequency and the odd harmonic frequencies:

$$x_{square}(t) = \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{\sin\left[(2k-1)\, 2\pi f_o t\right]}{2k-1} \tag{2.16}$$

When clipping a sine-wave, the resulting tones in the output are the fundamental, the 3rd harmonic, the 5th harmonic, and so on. Thus for a signal band of 20 kHz, clipping of a signals with frequencies above 6.67 kHz generates out-of-band distortion, that is not audible. It is thus the 6.67 kHz tone that is the worst case frequency that generates distortion products in the audio band. Based on this knowledge, it is possible to estimate the worst case slope, and how fast this signal reaches the supply limit. This knowledge may then be used to evaluate how fast the AGC loop needs to be, in order to avoid clipping.

Consider a conversion channel, where the signal amplitude from the MEMS sensor equals $V_{sens} = 500$ mV, the max VGA gain is $G_A = 16$ and the supply voltage is 1.5 V. The audio frequency equals 6.67 kHz, and inserting these values in (2.15), the resulting slope equals 0.335 MV/s. Assuming a near constant signal slope, the output of the amplifier reaches the supply rail after 1.5 µs. For an AGC operating with a clock frequency of 2 MHz, this time equals approx. 9 clock cycles. For the ideal adaptive A/D conversion channel there may only be a single sampling delay from the output of the VGA to the input of the AGC. However, as will be described in Sec. 2.5, additional filters are required in the signal path, which will increase the AGC loop delay. It is thus evident that for an AGC with a feedback loop, it may be difficult to avoid clipping from occurring for this worst case signal.

The distortion that will occur due to the delay of the AGC loop is only for a short period of time, before the VGA gain is reduced. The question is thus whether this distortion is audible or not. The problem was investigated in [16], concluding that audible distortion would occur and could be classified as "stutter". However, the paper does not fully describe how long the distortion should occur before it becomes audible. It would thus be necessary to carry out a subjective evaluation in the form of a listening test, in order to determine how audible the distortion is.

Another more relevant consideration is that the above example was based on the maximum amplitude signal from the MEMS sensor. In relation to this, it is relevant to consider the distortion of the MEMS sensor itself at these signal levels. The harmonic distortion from the MEMS sensor may be in the range of 1% - 5 % at levels 6 dB below the acoustical overload point. The acoustical signal is thus already heavily distorted by the MEMS sensor, and further distortion by the conversion channel is of limited importance.

If it is determined that distortion is generated by the conversion channel, and that it is audible, the only solutions are to either reduce the AGC loop delay or alternatively lower the AGC attack level. Lowering the attack level has the

unwanted effect that the VGA gain may be reduced without it being necessary, since the sensed signal just crossed the attack level but would not have clipped if the VGA gain was not adjusted. The lower the attack level, the more likely is it that the AGC reduces the VGA gain without it being necessary; a so-called false positive detection. The selection of attack level is thus a trade-off between avoiding signal clipping, due to the AGC loop delay, and the number of false positive detections, which creates unnecessary transient glitches.

2.4.4 Attack Time

To reduce the problem of false positive detection by the AGC, an attack sense period, or attack time, may be defined. This sets for how long the sensed signal should be above the attack level before the AGC reduces the VGA gain. In a digital AGC, this may be implemented as a number of consecutive sensed samples that are above the attack level. The minimum is a single sample, while increasing the number of consecutive samples will reduce the number of false positive detections. The immediate problem with an attack sense period is the increased possibility of signal clipping, before the VGA gain is reduced. Since the main purpose of the AGC is to avoid signal clipping, by reducing the analog gain, the AGC should react as soon as the signal is level detected to be above the attack level. False-positive detections are essentially unavoidable, since the input signal of the conversion channel is non-deterministic. As such false-positive detections should be avoided by increasing the AGC attack level, but should also be accepted as an inherent part of the adaptive conversion channel.

2.4.5 Release Level

Similarly to the attack level, the release level of the AGC sets the signal level limit for when the VGA gain may be increased. Generally, the release level and the attack level should be different in order to avoid unnecessary gain changes. Consider the case where the AGC attack and release levels are identical. As the detected signal increases above the attack level, the AGC and reacts by reducing the gain of the VGA. As soon as the VGA output has settled to the new level, then due to the lower gain level the VGA output is below the release level. As a result, the AGC reacts by increasing the VGA gain. The VGA output will once again be above the attack level, which causes the AGC to reduce the VGA gain. This pattern continues until the VGA output at the maximum gain setting is below the attack level.

To avoid this unstable oscillating behavior of the feedback type AGC, it is necessary that the release level is lower than the attack level by a factor larger than the gain steps used for the VGA. The attack and release level thus forms an amplitude hysteresis window for the AGC.

An example of an AGC amplitude hysteresis window is depicted in Fig. 2.9, where

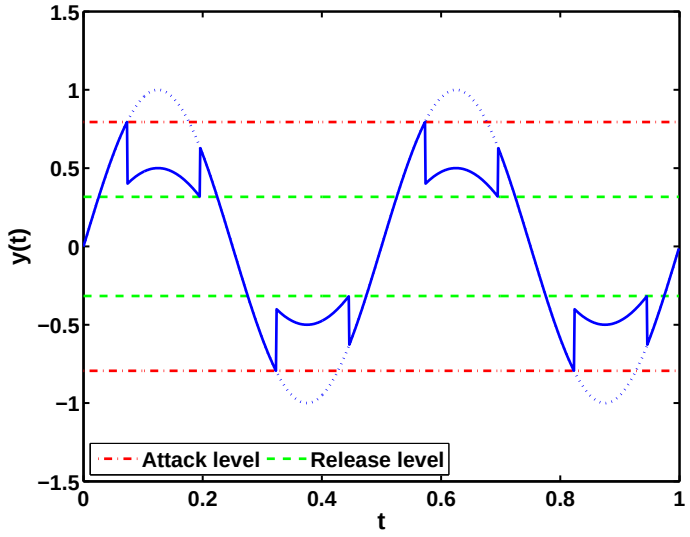


Figure 2.9: Signal output from ideal VGA, showing the amplitude hysteresis window of the AGC. Dashed curve is the ideal output, and the full drawn curve is the gain adjusted output

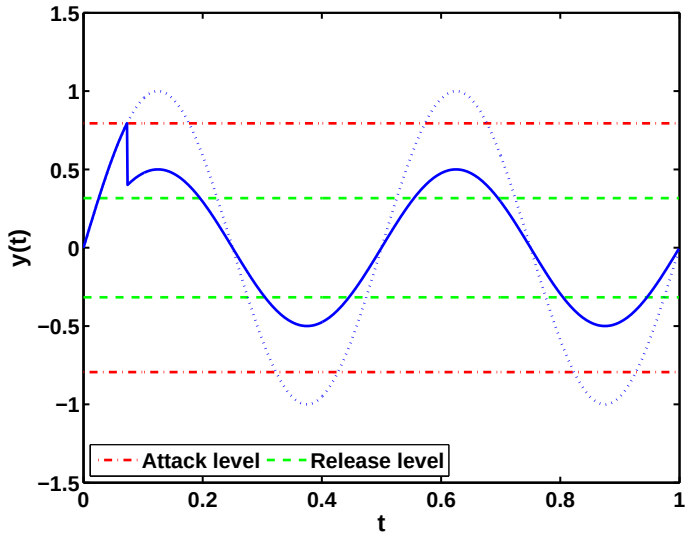


Figure 2.10: Signal output from ideal VGA, for AGC with amplitude hysteresis window and non-zero release time

the attack and release levels are set to –2 dB and –10 dB respectively, and with a VGA gain step of 6 dB. As seen from the figure, as the output of the VGA crosses the attack level, the gain of the VGA is reduced by 6 dB. The signal level is still above the release level, thus avoiding a cyclic decrease and increase of the VGA gain. Not until the signal level drops below the release level is the analog gain increased again.

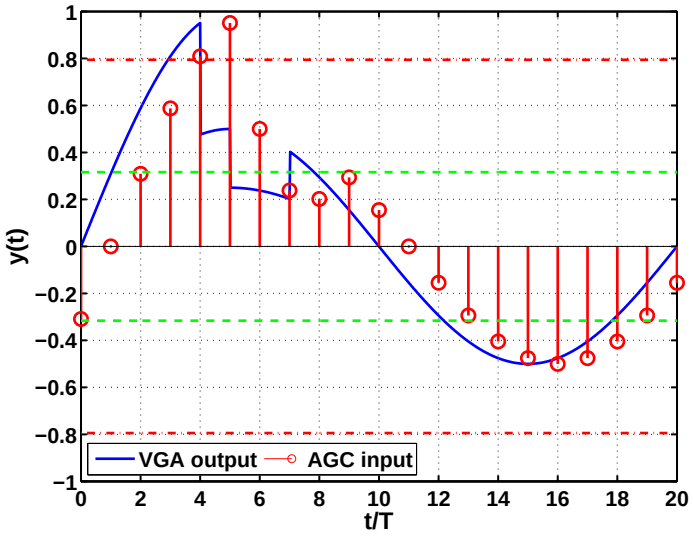


Figure 2.11: Plot of VGA output and AGC input for a system where the AGC input is delayed one clock period, T, compared to the VGA output

2.4.5.1 Release Time

An interesting property shown in Fig. 2.9, is that for each half-period of the sine wave, the VGA gain is decreased and increased. This occurs even though the peak level of the signal is unchanged, and is due to the detection of the instantaneous signal level instead of the signal envelope. Since each gain change introduces a transient glitch, as described in Sec. 2.3, this is an unwanted behavior.

The solution to the problem is solved by defining a release time for the AGC, that sets a minimum time period in which the detected signal should be below the release level before increasing the VGA gain. The conversion channel processes audio signals with a he lower signal frequency of 20 Hz that equals a time-period of 25 ms. Thus by setting the release time to 25 ms, the problem is avoided. This is easily implemented in the digital domain, and thus removes the main problem of detecting the instantaneous signal level instead of the signal envelope. In Fig. 2.10 is shown the resulting VGA output for a constant amplitude sine wave, when having a non-zero release time for the AGC, resulting in only a single gain change for multiple periods of the sine wave.

2.4.5.2 Dead time

In the feedback type AGC loop, the delay from the output of the VGA to the input of the AGC detector has further implications on the implementation of the AGC controller. In case of an attack event ,the VGA gain is reduced, but due to the loop delay, the AGC controller does not immediately detect the change in the signal level following from the VGA gain reduction. If this loop delay is not taken into account, the AGC may also in the following sample detect that the signal level is too high. This would cause another attack event, thus reducing the

VGA gain unnecessarily.

This behavior is depicted in Fig. 2.11, showing the output signal of the VGA and the input signal of the AGC. The AGC input is a sampled version of the VGA output, delayed by one clock period. At $t = 3T$, the VGA output crosses the attack level but this is not detected by the AGC until at $t = 4T$. The VGA gain is then reduced, lowering the signal level at the output of the VGA. However, at $t = 5T$ the AGC again detects that the signal level is above the attack level although the first gain adjustment has sufficiently reduced the signal level at the VGA output. Thus, the VGA gain is further reduced. At $t = 7T$ the AGC detects that the signal level is below the release level, and increases the VGA gain to the final value. Overall, two unnecessary gain changes were done, resulting in increased noise for short period of time and two transient glitches.

To avoid this overcompensation, a dead time period may be introduced in the AGC, during which no gain adjustments occur. The length of the dead time should be minimized to avoid distortion caused by rapidly increasing signals, as discussed in Sec. 2.4.3. Thus, the dead time should equal the total loop delay of the AGC input plus the settling time of the VGA.

2.4.6 Gain Levels and Steps

The gain levels of the VGA directly determines the improvement in the dynamic range that is obtainable for the given adaptive A/D conversion channel. The dynamic range of the channel, DR_{chn} may be expressed as:

$$DR_{chn} = DR_{ADC+VGA} + (G_{a,\max,\mathrm{dB}} - G_{a,\min,\mathrm{dB}}) \tag{2.17}$$

where $DR_{ADC+VGA}$ is the dynamic range of the ADC and VGA at the maximum gain setting, $G_{a,max}$ is the maximum VGA gain, $G_{a,min}$ is the minimum VGA gain.

The difference in the minimum and the maximum VGA gain determines the extension of the dynamic range of the conversion channel in comparison to the ADC. In Fig. 2.12 is shown the SNR when sweeping the input amplitude of an adaptive A/D conversion channel. The SNR curve is for a conversion channel with $G_{a,max} = 24$ dB and $G_{a,min} = 0$ dB, with $\Delta G = 6$ dB, and where the peak SNR of the VGA and ADC is 60 dB. As seen from the plot, the dynamic range of the conversion channel is 84 dB, thus 24 dB larger than that of the VGA and ADC alone. Following the first gain change, the SNR of the channel saturates, and peaks at 60 dB for the largest input levels where the minimum VGA gain is applied.

The size of the gain steps used by the AGC has several implications on the performance of the conversion channel. The gain step may be defined as the difference in the VGA gain from one gain setting to the next, e.g. a change in gain from 16 V/V to 32 V/V equals a gain step by a factor of 2, or 6 dB. To be able to digitally compensate for the change in analog gain, the gain steps in the

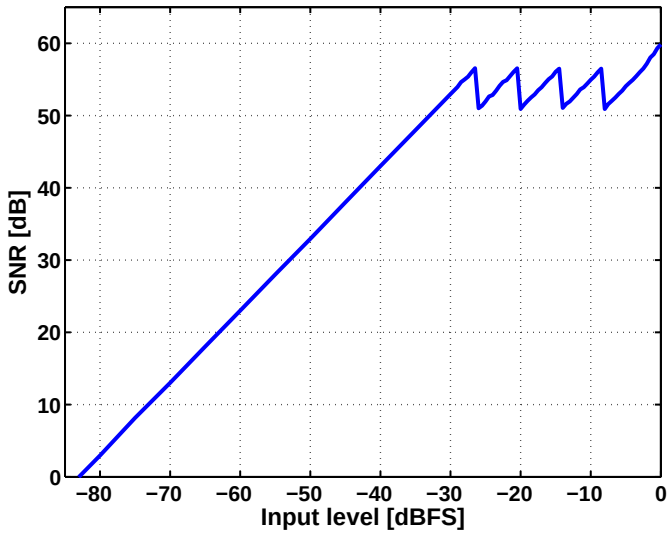


Figure 2.12: Example SNR vs input amplitude for adaptive A/D conversion channel

Table 2.2: Pros and cons of using small and large gain steps

	Large gain step	Small gain step
Circuit complexity	+	-
SNR variation	-	+
Number of gain changes	+	-
Transient glitch peak value	-	+

digital domain should be equal those in the analog domain. This favors having a gain step in powers of 2, as this is easily implemented digitally as a bit-shift. From an analog design point of view, the gain is most likely implemented as a ratio of the values of two components, e.g. resistors, and preferably with the ratio as an integer number. Larger gain steps are also preferred as the larger the gain steps, the fewer gain settings, and thus the smaller the circuit area needed for the component selection array.

Besides from circuit complexity there are other important aspects of selecting the number of VGA gain levels and thus the minimum gain step. As it was stated in (2.5) in Sec. 2.2, the noise of the conversion channel depends on the VGA gain. Thus, when reducing the VGA gain, the channel noise will increase. The larger the gain change, the large the change in noise. The peak SNR is independent of the gain step size, but the variation in the SNR across the dynamic range will have a larger variation when applying larger gain steps. Thus, from a circuit noise point of view, smaller gain steps are preferred.

Small gain steps are also preferred from a transient glitch point-of-view. As given in (2.9), the gain step has a direct impact on the peak value of the transient glitch generated by the gain adjustment in the adaptive A/D conversion channel. However, small gain steps are problematic when considering the gain adjustments, as the number of gain changes necessary is inherently larger than when using larger gain steps.

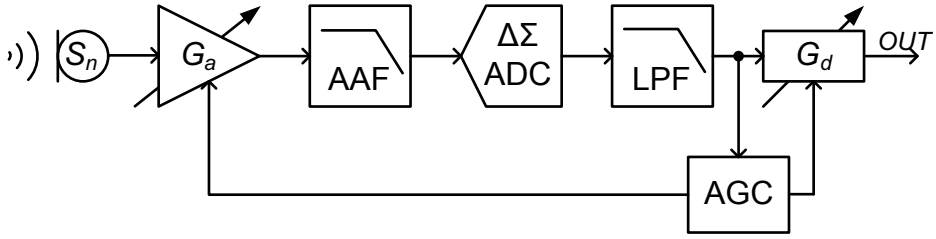


Figure 2.13: Adaptive A/D conversion channel with channel filters

This adds the question of how to switch between the different gain levels of the VGA and the digital counterpart. One approach is to change the gain by one step at a time, e.g. from a gain of 32 V/V to a gain of 4 V/V via the gain values 16 V/V and 8 V/V, thus one step per AGC cycle. With the aim of reducing clipping, this approach is problematic when using small gain steps, and a large input is applied while the VGA gain is at the maximum level. If the input signal requires a reduction of the gain from e.g. 32 V/V to 4 V/V using 6 dB steps, this would require three AGC cycles including the AGC dead-time. This could be solved by using larger gain steps when reducing the VGA gain, while using smaller gain steps when increasing the VGA gain. Alternatively, the AGC algorithm could adjust the gain steps based on the signal level, e.g. by keeping track of whether the gain was reduced in the previous AGC cycle, and if so, reduce the VGA gain using a larger step. Also the signal slope might be used as an indicator of whether a larger change in gain is necessary or not.

As always, since the input signal is non-deterministic these added precautions may result in the AGC over-compensating the change in VGA gain. Larger gain steps also cause a larger transient glitch in the output, as given from (2.9). On the other hand, the number of gain transitions is reduced when using larger gain steps, thus reducing the number of transient glitches in the channel output. A summary of the pros and cons of using small or large gain steps is given in Table 2.2. Generally, the simplest approach is preferred from a system point of view. Thus, a single gain step per adjustment using large gain steps in powers of two.

The problem of gain steps in relation to the transient glitches is discussed further in Chap. 3 and Chap. 4.

2.5 Other System Blocks

The AGC is at the core of the adaptive A/D conversion channel. However, the other blocks of the conversion channel are of high importance when designing the system. In Fig. 2.13 is shown an expanded block diagram of the adaptive A/D conversion channel, with the addition of filters. In this section the remaining blocks are briefly discussed to provide an overview and reference to relevant literature.

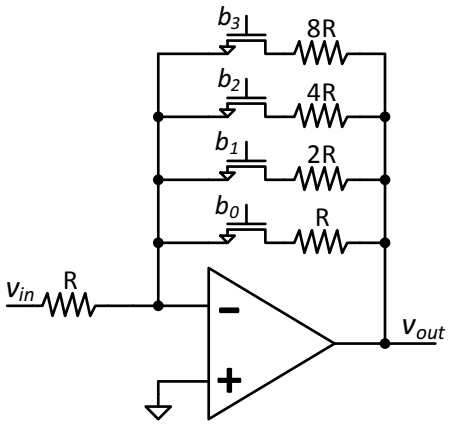


Figure 2.14: Example of variable gain amplifier based on inverting amplifier configuration, with four gain levels and one-hot control

2.5.1 Variable Gain Amplifier

The variable gain amplifier may be realized in multiple ways, with the most simple implementation being an inverting feedback amplifier with adjustable feedback resistance. In Fig. 2.14 is shown such an amplifier configuration where the variable feedback resistance is realized using four binary scaled resistors and associated switches. Controlling the switches using a *one-hot* encoding, only one feedback path is connected at a time. The gain of the VGA in Fig. 2.14 is given as:

$$G_a = -\frac{R_{fb}}{R_{in}} = -\frac{kR}{R} = -k \tag{2.18}$$

where R_{fb} is the feedback resistance, R_{in} is the input resistance, R is a unit resistor, and k is {1,2,4,8}.

The configuration in Fig. 2.14 is only an example, and other configurations of the resistors may be better suited. The main concerns when designing the VGA are noise, harmonic distortion and the precision of the gain levels. The resistors, switches and the operational amplifier (OpAmp) will generate noise, which needs to be taken into account. Generally, feedback applied to an amplifier linearises the amplifier, thus reducing signal distortion. However, the switches in the feedback path will add some distortion. The switches are typically realized using transmission-gates, being a parallel connection of a NMOS and a PMOS transistor. With the switches being non-linear voltage dependent resistances, they will add distortion which needs to be minimized. Furthermore, the switches will add a parasitic resistance to the feedback path and thus affects the gain of the amplifier.

In the adaptive A/D conversion channel, the gain levels of the digital gain block can be set accurately, but this does not guarantee the same total channel gain for all channel gain settings. As for all analog integrated circuits, the analog gain levels are dependent on process variations. Thus, the analog gain steps will not be exactly equal, and furthermore they will not match perfectly with the digital gain steps. Assuming that the preamplifier is realized as an amplifier with

resistive feedback as shown in Fig. 2.14, the gain may be set by the ratio of two resistors and the relative accuracy can be made within ±0.1% with proper layout techniques [17]. However, the preamplifier gain is also dependent on the feedback amplifier, and furthermore the switching network required to configure the gain of the preamplifier also has an impact on the actual gain levels that are realized.

For a microphone with an adaptive A/D conversion channel, the microphone sensitivity will inherently be non-constant over the dynamic range of the channel. It is therefore necessary to consider the maximum variation of the sensitivity when designing the conversion channel and the VGA in particular.

The design of a low noise, low current, and low distortion VGA is an important part of the adaptive A/D conversion channel. However, the topic is beyond the scope of this thesis.

2.5.2 Analog-to-Digital Converter

The ADC is at the core of the A/D conversion channel, and performs the actual data conversion. A wide range of A/D converter topologies exists, but for audio applications, the $\Delta\Sigma$ ADC is the common choice. The $\Delta\Sigma$ ADC depends on oversampling of the input signal in order to push the quantization noise away from the signal band, or base band, and up to higher frequencies. This is done by the loop filter that essentially high-pass filters the quantization noise of the quantizer. Because of the oversampling and noise shaping, it is possible to apply single bit quantization and still achieve peak signal-to-noise ratios and dynamic ranges above 100 dB [18]. At the same time, the loop filter also filters other non-idealities generated in the $\Delta\Sigma$ modulator, including circuit noise, DC offset and harmonic distortion. This has further the benefit, that the performance of the $\Delta\Sigma$ ADC is not limited by component matching as is the case in e.g. Flash ADCs [11]. Due to the small signal band of audio signals, it is possible to use a sampling clock in the MHz range and still achieve a large oversampling ratio. A high dynamic range and peak SNR can thus be achieved without too high a current consumption.

The topic of $\Delta\Sigma$ converters is extensively covered in the literature. A review of the topic is given in [18], while more detailed descriptions are given in [19], [20] and [21]. A brief introduction is also provided in Chap. 5, and a detailed description of the design of a low power continuous-time $\Delta\Sigma$ ADC for application in the adaptive A/D conversion channel is given in Chap. 5 and Chap. 6.

2.5.3 Filters

As shown in Fig. 2.13, filters are required in the signal path of the conversion channel. The anti-aliasing filter (AAF) placed in front of the ADC is required in order to avoid aliasing components when sampling the signal in the ADC. When sampling a signal using a specific sampling clock, f_s, only frequencies up to $f_s/2$

may correctly be represented in the sampled domain. Any frequencies above $f_s/2$ are folded down into the base band frequency range, thus adding unwanted frequency components in the sampled signal. In order to avoid aliasing, an anti-aliasing filter, in the form of a low-pass filter (LPF), is required prior to the sampling process of the ADC.

With the ADC being realized as a $\Delta\Sigma$ ADC, the requirements of the AAF are relaxed due to the high sampling frequency used in a $\Delta\Sigma$ ADC. Thus, the AAF may have a corner frequency much higher than the signal bandwidth and may be realized as a simple passive 1st order low-pass filter. In the case of a CT $\Delta\Sigma$ ADC the AAF is an inherent part of the design [22].

Another low-pass filter is placed in between the $\Delta\Sigma$ ADC and the AGC and digital gain block. As described in Sec. 2.5.2, the output of the $\Delta\Sigma$ ADC is single-bit, but may also be multi-bit. However, there is no sample-by-sample relation between the input and the output of the $\Delta\Sigma$ ADC, due to the oversampling and low-resolution quantization. Thus, it is not possible by the AGC to directly detect the signal level of the converted signal. Typically a decimation filter is placed after a $\Delta\Sigma$ ADC, with the purpose of removing all frequencies above the signal band and also downsampling the output to the Nyquist rate. Thus, the oversampled single-bit ADC output is converted to a full resolution digital signal. A decimation filter is typically realized as multistage filters, using Sinc and finite-impulse response (FIR) with a large number of taps [19]. With the sampling frequency of the output filter being ideally at the Nyquist rate, in the case of a $\Delta\Sigma$ ADC with an oversampling ratio of 60, there is an ideal minimum delay of 60 clock cycles through the decimation filter. Typically this delay is longer due to the delay of the filters and the downsampling blocks. As discussed in Sec. 2.4.4, the delay from the output of the VGA to the input of the AGC is critical as it directly affects the AGC loop delay. Using a full decimation filter would thus significantly increase the risk of clipping in the conversion channel due to the long time delay of the AGC. However, it is not necessary for the AGC input to have the full signal resolution in order to detect the signal levels. Thus, a much simpler filter may be applied, reducing the delay added to the AGC loop by the filter.

Further details on the AAF and the digital low-pass filter are given in Chap. 4. The design of decimation filters is outside the scope of this thesis, but a detailed description of the topic may be found in [19–21].

2.5.4 Digital Filters and Gain Block

The digital LPF following the ADC and the gain block needs to be designed for low power consumption, as the current consumption of these blocks and the AGC reduce the improvement in current consumption of the adaptive A/D conversion channel when compared to the static channel. The topic is beyond the scope of this thesis, and details on the topic may be found in the existing literature. In [23] is described low power solutions from a system point of view, while [24, 25]

cover the realization of the block in CMOS.

2.6 Summary

The application of a VGA and AGC in the A/D conversion channel is an interesting solution to achieve a high dynamic range conversion channel. The VGA gain is reduced for large input signal in order to avoid signal clipping, and at the same time the reduced gain is compensated in the digital domain. Thus, the system efficiently extends the dynamic of the conversion channels range, but at the cost of the peak SNR. For a single channel implementation, the solution provides a reduction in the power consumption in comparison to a static A/D conversion channel with the same dynamic range.

However, the adjustment of the gain settings in the channel generates a transient error signal due to the finite transition delay of the channel. The peak value of the transient glitches are proportional to the gain step size used by the system, and this is problematic as large gain steps generally are preferred from a circuit point of view. Fewer gain levels reduce the complexity of the VGA and also the number of gain changes in the system; the number of transient glitches is thus also reduced.

The control of the channel gain is handled by the AGC block, that detects the level of the signal being processed in the channel. The key point of the AGC is to adjust the gain levels in order to avoid signal clipping. Although a feedforward based AGC has a lower delay, the feedback based AGC is preferred in the A/D conversion channel as the AGC may then be realized in the digital domain; this simplifies the implementation. The delay of the AGC due to the A/D conversion and filtering of the signal is considered acceptable, as the signal bandwidth is limited to 20 kHz. The peak detector of the AGC senses the instantaneous signal level rather than the signal envelope, due to the added delay of estimating the signal envelope.

Important aspects of the AGC are the attack and release levels, that determine the signal levels at which the channel gain is adjusted. The attack level should be set below the clipping level due to the delay of the AGC loop. The release level should be set below the attack level by a factor larger than the gain step size used by the system. This in order to avoid cyclic gain adjustment, resulting in an increased number of gain changes and associated transient glitches. Furthermore, a release time is necessary to avoid unnecessary gain changes in the case of constant amplitude periodic signals. Finally a dead time is needed in the AGC to avoid unnecessary gain adjustment due to the delay of the AGC loop.

The problem of transient glitches is an inherent property of the adaptive A/D conversion channel, and thus needs to be evaluated in further detail.

3

Evaluation of Adaptive A/D Conversion Channel

This chapter presents an objective method for evaluating the audibility of the transient glitches generated by the adaptive A/D conversion channel. The objective evaluation is based on submodels from the standardized Perceptual Evaluation of Audio Quality (PEAQ) method, which based on psychoacoustic models of the human hearing, can be used for grading the audio quality of audio systems. The submodels Mean Filtered Probability of Detection (MFPD) and Averaged Distorted Block (ADB) are used in the PEAQ for modeling the probability of detection errors in the evaluated signal. Based on a high-level model of the adaptive A/D conversion channel, the audibility of the glitches are evaluated using the objective models and compared with the results from a subjective evaluation in the form of a listening test. The comparison shows a good correlation between results of the listening test and the results from the ADB and MFPD models. The objective method may thus be used for evaluation of the transient glitches of the conversion channel during the design phase. The presented work is based on the ICASSP 2014 paper, App. A.

3.1 Evaluation of Audio Quality

A problem when designing the adaptive A/D conversion channel is the evaluation of the audibility of the transient glitches generated when adjusting the gain levels in the channel. The evaluation of audio quality is a difficult task, as audio quality is a very subjective matter. It is impacted by the hearing of the person listening to the audio, the persons musical preference, etc.

Audio systems are typically evaluated using the standard metrics of THD and

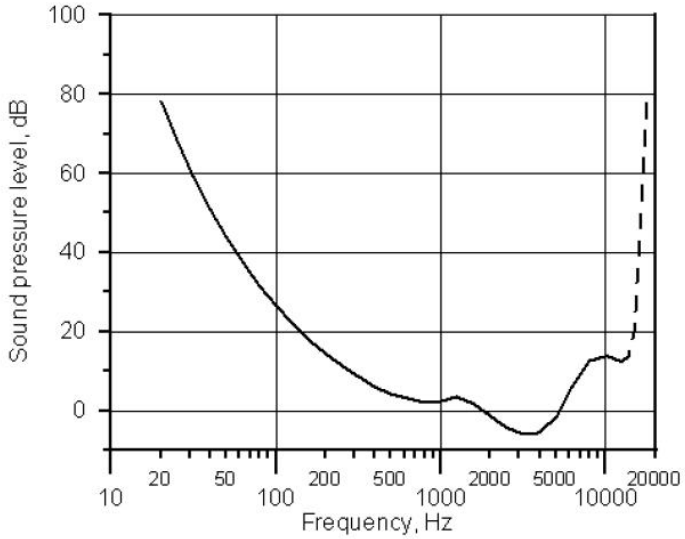


Figure 3.1: Loudness contour plots of the binaural hearing threshold in free field [28]

SNR, that are defined as:

$$SNR = 10 \log_{10} \left(\frac{P_s}{P_n} \right) \tag{3.1}$$

$$THD = \frac{\sum_{k=2}^{N} P_{H,k}}{P_s} \tag{3.2}$$

where P_s is the power of the signal fundamental, P_n is the noise power, and $P_{H,k}$ is the power of the *kth* harmonic and N is the maximum harmonic. For a given system, these numbers may be given for a wide range of input signal frequencies and output levels. The SNR performance is commonly weighted using an A-weighting filter defined in the IEC 61672 standard [26]. The A-weighting weights the frequency of the audio spectrum, 20 Hz to 20 kHz, based on the binaural hearing threshold curve. A plot of the binaural hearing threshold is shown in Fig. 3.1, thus indicating for each frequency in the audio band, the lowest sound pressure level that is detectable by the human ear. Other weighting filters are used by the industry, including ITU-R 468 [27], also known as CCIR 468-4. The main problem when applying the weighting filters to the SNR of a system is, that the SNR and THD are based on a single test signal frequency.

The human hearing is a complex system, where the sensitivity to a specific frequency depends on the presence of other signal frequencies. In psychoacoustics this effect is called *masking* and physically relates to the anatomy of the human ear and the Basilar membrane [28]. The result of the masking is that the presence of one signal frequency will alter the sensitivity to other signal frequencies. This change in sensitivity may be visualized using loudness contour plots with a masker present, as shown in Fig. 3.2.

Another problem with THD and SNR as performance metrics is, that they are based on steady-state system measurements. The glitch generated by the adaptive

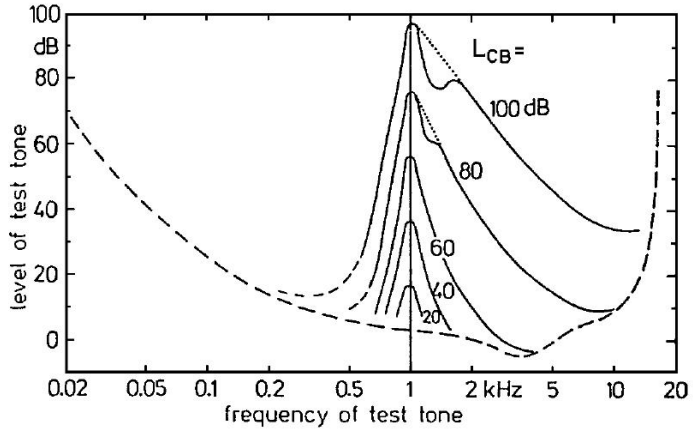


Figure 3.2: Loudness contour plots with a masker present at 1 kHz [28]

Table 3.1: Subjective grading scale used in ITU-R BS.1116 [29]

Impairment	Grade
Imperceptible	5.0
Perceptible, but not annoying	4.0
Slightly annoying	3.0
Annoying	2.0
Very annoying	1.0

A/D conversion channel is transient in nature. Due to the masking effect and the transient nature of the glitch, the SNR and THD are not suitable for evaluating the glitches of the conversion channel.

An alternative method is to subjectively evaluate the audio quality of the conversion channel, this may be done using the ITU-R BS.1116 standard [29]. This standard describes how to subjectively evaluate the audio quality of high-fidelity audio equipment using a trained group of persons. The standard uses a continuous grading scale from 1.0 to 5.0, as shown in Table 3.1, to evaluate impairments in the tested audio system. Since the listening test is conducted using trained persons, the grading of different systems is comparable to a certain degree.

Carrying out listening tests by the BS.1116 standard is a time consuming task requiring trained test subjects. This makes it impractical to continuously use during the development of the adaptive A/D conversion channel. An objective method that could be evaluated using a computer would be preferred, as this significantly reduces the time required for each new evaluation of the conversion channel.

3.2 Existing Objective Methods

3.2.1 Mean Squared Error

The mean squared error (MSE) is a mathematically simple method for objectively evaluating the error of a signal. Based on a comparison of two signals, a reference and the test signal, the MSE is given as:

$$e[n] = x[n] - y[n] \tag{3.3}$$

$$\mathrm{MSE}(x, y) = \frac{1}{N} \sum_{\forall n} e[n]^2 \tag{3.4}$$

where N is an integer number defining the number of samples, $x[n]$ is the *nth* sample of the test signal x, and $y[n]$ is the *nth* sample of the reference signal y. As detailed in [30] the MSE has several benefits, including the simplicity and that it is way of defining the error energy of the signal. However, the MSE does not model the human hearing, and thus does not take any masking effects into account. More importantly, the same MSE may be found for two very different signals.

Consider the three signal x, y and z that are given as:

$$x = \{1, 2, 3, 4\} \tag{3.5}$$

$$y = \{0, 1, 2, 3\} \tag{3.6}$$

$$z = \{0, 1, 4, 3\} \tag{3.7}$$

From (3.3)-(3.4) the associated error signals and MSE values are:

$$e_{x,y} = \{1, 1, 1, 1\} \tag{3.8}$$

$$\mathrm{MSE}(x, y) = \frac{1}{4}\left(1^2 + 1^2 + 1^2 + 1^2\right) = 1 \tag{3.9}$$

$$e_{z,y} = \{0, 0, 0, 2\} \tag{3.10}$$

$$\mathrm{MSE}(z, y) = \frac{1}{4}\left(0 + 0 + 2^2 + 0\right) = 1 \tag{3.11}$$

The two error signals are very different while the calculated MSE is the same for both signals. From audio perception point of view the two signals are very different, with x being a DC offset while z is a short impulse.

The MSE is not based on any model of the human hearing, and as the above example showed, the calculated MSE may be the same for two different error signals. Based on this the MSE is not a suitable objective method for evaluating the audibility of the transient glitches.

3.2.2 Structural Similarity Index

An alternative measure is the structural similarity index (SSIM) as described in [30] where the MSE and SSIM are compared for evaluation of the perception of

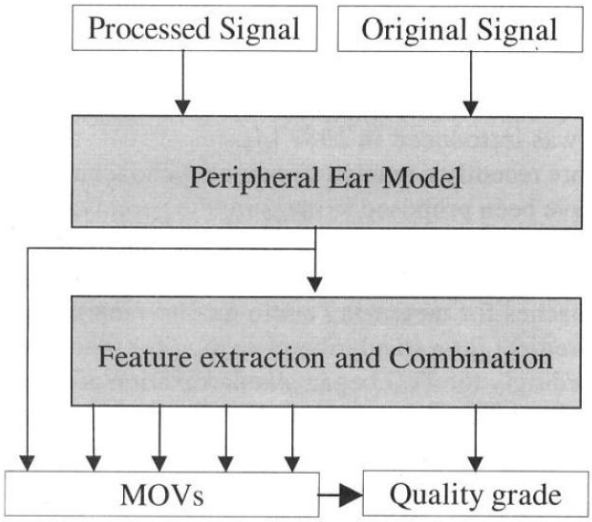


Figure 3.3: High-Level block diagram of the PEAQ model [34]

errors in images. In [31–33] the SSIM was adapted to audio signals and used for evaluating the audio quality of signals with temporally varying distortions. The authors applied the SSIM in combination with other objective metrics, to develop a new metric. The method was compared with results from a subjective test, showing a good correlation between the results from the subjective test and those obtained using the developed model. However, the SSIM and the model presented in [33] is intended for evaluating the audio quality and not the audibility of the error signals.

3.2.3 PEAQ MOVs

An objective method for replacing the BS.1116 listening tests was developed at Fraunhofer IIS in the 1990's to evaluate the audio quality of the MPEG-1 audio layer 3 codec being developed at the same time. The method named the *Perceptual Evaluation of Audio Quality* (PEAQ) [34, 35] was subsequently standardized by the ITU in ITU-R BS.1387 [36]. The PEAQ method applies the same grading scale as used in BS.1116, when evaluating the audio quality of an audio system. Thus, making the results of PEAQ and a BS.1116 test comparable.

The PEAQ method is based on several psychoacoustical submodels that each model different parts of the human hearing, as shown in Fig. 3.3. First excitation patterns are generated from the input signal using a model of the basilar membrane of the ear named the peripheral ear model. These excitation patterns are then split into time-frames that are analyzed in the frequency domain. This is then evaluated using the submodels, that model the different parts of the human hearing, and each submodel generates an intermediate model output variable (MOV). Each MOV is given a weighting factor and is then used to calculate the final score based on the BS.1116 grading scale.

The peripheral ear model exists in two versions: a simple version based on the fast Fourier transform (FFT), and an advanced version based on a filter-bank based model of the ear. The two models also use different MOVs for evaluating the audio quality. More details on the peripheral ear model may be found in [34, 36].

The PEAQ method is intended as an objective evaluation of the audio quality of hi-fi audio systems instead of the BS.1116 listening tests. However, in [37] the PEAQ method was used for evaluating the reduction in audio quality caused by audio ADCs, DACs and sample-rate converters showing good results. In some cases part of the MOVs have been used for special applications, like. In [31, 33] a part of the MOVs where together with the SSIM as described in Sec. 3.2.2.

Concerning the evaluation of the transient glitches in adaptive A/D conversion channel, when used for a MEMS microphone such a system is not a high fidelity system. What is important is the audibility of the transient glitches, or whether or not the glitches may be heard in the output of the conversion channel. Since the PEAQ method evaluates the audio quality and not the audibility of transient errors, it is considered to be unsuitable for this specific task. Instead an approach somewhat similar to the one applied in [31, 33] may be applied here. From the BS.1387 standard it is found that the FFT based version of the PEAQ model uses two MOVs to model the probability of detecting impairments in the test-signal: the *Maximum Filtered Probability of Detection* (MFPD) and the *Average Distorted Block* (ADB). These may then be evaluated as possibly objective measures of the audibility of the transient glitches generated by the conversion channel.

In the FFT based version of the peripheral ear model, the signal is split into frequency auditory filter bands. These are weighted based on the ears frequency sensitivity as given from binaural hearing threshold. Similarly, the signal is split into time-frames, and each time-frame is evaluated. From [36] the MFPD is calculated from the total probability of detection for each channel, P_c, that is given as:

$$P_c[n] = 1 - \prod_{\forall k} (1 - p_c[k, n]) \tag{3.12}$$

where k defines the auditory filter band, n is the time-frame, and p_c is the binaural detection probability based on the error signal. The filtered probability of detection is given as:

$$\tilde{P}_c[-1] = 0 \tag{3.13}$$

$$\tilde{P}_c[n] = 0.1 \cdot P_c[n] + 0.9 \cdot \tilde{P}_c[n-1] \tag{3.14}$$

where P_c is the unfiltered probability of detection, and n is the frame being evaluated. From (3.14) the maximum filtered probability, PM_c, is simply given as:

$$PM_c[n] = \max\left(PM_c[n-1], \tilde{P}_c[n]\right) \tag{3.15}$$

The MFPD value is then the value of $PM_c[n]$ for the last frame.

The ADB relates to the number of frames containing audible distortions. First the number of frames of the signal where the probability of detection, P_c, is above 50

%, $n_{distorted}$, is counted. For all frames is then found the number of *steps*, $Q_{bin}[n]$ that the distortion or error is above the binaural threshold. The specific step size relates to the frequency content of the specific frame and band. Based on this the total number of steps above the binaural threshold for frames is found as:

$$Q_{sum} = \sum_{\forall n} Q_{bin}[n] \tag{3.16}$$

Then from (3.16) and $n_{distorted}$ the ADB score is calculated as:

- if $n_{distorted} = 0 \Rightarrow ADB = 0$
- if $n_{distorted} > 0$ and $Q_{sum} > 0 \Rightarrow ADB = 10\log_{10}(Q_{sum}/n_{distorted})$
- if $n_{distorted} > 0$ and $Q_{sum} = 0 \Rightarrow ADB = -0.5$

Thus, when distortions are detected and above the binaural threshold, the ADB is the averaged number of steps above this threshold.

For a more detailed description of the mathematics behind the FFT based version of PEAQ, and the ADB and MFPD MOVs, see [36].

3.3 High-Level Conversion Channel Model

To evaluate the transient glitches of the adaptive A/D conversion channel, a high-level system model was developed using MATLAB. A block diagram of the model is shown in Fig. 3.4. The main purpose of the model was, to generate output signals with the transient glitch present. Thus, the channel model was made noiseless, and not modeling any circuit noise or quantization noise. If noise was present this might affect the results of the listening test and the objective test. The subblocks of the model were modeled as follows. The MEMS sensor was modeled as an ideal signal source without noise or distortion and with unity sensitivity. The VGA was modeled as a zeroth order system and with a limiting function to model clipping in the analog domain. The AAF was modeled as a 1st order low-pass filter with a corner frequency of 200 kHz. The ADC was modeled as a 4th order $\Delta\Sigma$ modulator without any quantization. The LPF following the ADC was modeled as a 16 tap FIR averaging filter. The digital gain block was modeled as an ideal digital multiplier with the same gain levels as the VGA. The AGC was modeled with attack and release levels and a release timer. The details of the subblocks are summarized in Table 3.2. In the system model the VGA was for simplicity modeled as a zeroth order system, and the glitch would then be generated due to the delay of the AAF, signal transfer function of the $\Delta\Sigma$ ADC, and the averaging filter.

Both the analog and digital parts of the model were realized as sampled systems, with the input signal being upsampled to the 2 MHz sampling frequency of the ADC. An summary of the model properties are given in Table 3.2.

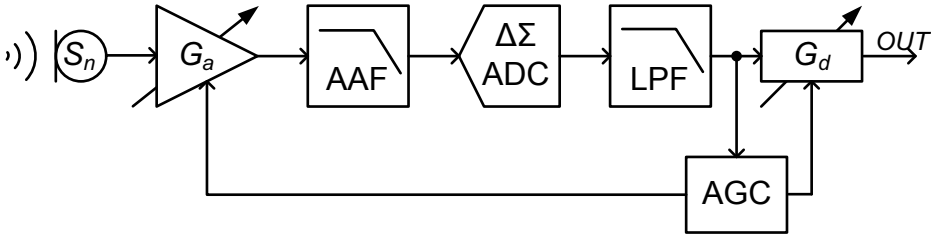


Figure 3.4: Block diagram of adaptive A/D conversion channel

Table 3.2: Properties of noiseless adaptive A/D conversion channel model used for generation of test signals

Property	**Value**
Sampling frequency	2 MHz
Signal bandwidth	20 kHz
Channel gain	18 dB
Gain levels	0 dB, 6 dB, 12 dB, 18 dB
Gain step	6 dB
Analog full-scale level, V_{FS}	1
Analog limiter level	-4 dBFS
AGC Attack level	-6 dBFS
AGC Release level	-14 dBFS
AGC Attack sense time	0 s
AGC Release time	50 ms
AGC dead time	0 s
ADC loopfilter	4th order
Quantization levels	∞
Anti-aliasing filter	1st order, $f_c = 200$ kHz
Low-pass filter (LPF)	16 tap FIR averaging filter

For the objective evaluation a reference model was also developed, in order to generate a reference signal with the same output phase shift as in the adaptive A/D conversion channel. The reference model is a static A/D conversion channel, but without a limiting function in the VGA to avoid clipping.

3.4 Test Signals

To evaluate the audibility of the transient glitches, sound samples with different properties were used. Generally, the AGC adjusts the gain of the conversion channel when the input level increases above the attack level. Due to the release time, the AGC does not instantly increase the VGA gain as soon as the signal level is below the release level. Thus, for signals that have a somewhat constant envelope, there will be fewer gain changes than for a signal with a more varying envelope. Thus, both sound samples with a slowly changing envelope and a rapidly changing envelope are necessary to evaluate the audibility of the glitches.

Table 3.3: Properties of sound samples used for evaluation of the adaptive A/D conversion channel

Sound sample	Envelope	Frequency components
Double-Bass	Slowly changing	Low frequency
Tuba	Rapidly changing	Low frequency
English Male Speech	Rapidly changing	High frequency

The frequency components of the signal also has an impact on the audibility of the transient glitch, due to the masking effects of the human hearing. With the glitches being short pulses that are primarily high frequency components, it is necessary to evaluate the conversion channel using both signals with mainly low frequency components and some with mainly high frequency components.

Three different test sounds were used for the evaluation, all being 2.5 second cut-out versions of the *Double-Bass*, *Tuba* and *English Male Speech* signals from the Sound Quality Assessment Material CD [38] by the European Broadcasting Union. In Fig. 3.5-3.7 are shown the time-series and spectrogram plots of the three sound samples. From the time-series plot of the *Double-Bass* in Fig. 3.5 it is seen that there are no abrupt changes in the signal level thus having a slowly changing envelope. Furthermore, the content is primarily low frequency as is visible in spectrogram. From Fig. 3.6 the *Tuba* sample also primarily contains low frequency components, but in contrast to the *Double-Bass* sample the *Tuba* has a more rapidly changing envelope. Finally, the *English Male Speech* sample has more high frequency components and also a rapidly changing envelope, as seen from the plots in Fig. 3.7. The properties of the sound samples are summarized in Table 3.3.

3.4.1 Generation of Test Signals

The test signals used for the evaluation of transient glitches were based on the three sound samples that had been processed by the noiseless system model. All three sound samples were used as input to the conversion channel model, with the output being written to a WAVE audio file at a sampling frequency of 48 kHz and 24 bit resolution. The audio files were upsampled to 2 MHz and the peak signal level scaled to -5 dBFS.

3.4.2 Scaling of Transient Glitch

The purpose of the evaluation was to identify whether the transient glitch would be audible, for a given peak value of the glitch. The glitch may be reduced or increased by changing the gain steps in the model of the A/D conversion channel, but this changes the dynamic properties of the channel, thus generating more or fewer glitches than in the ”standard” version of the model.

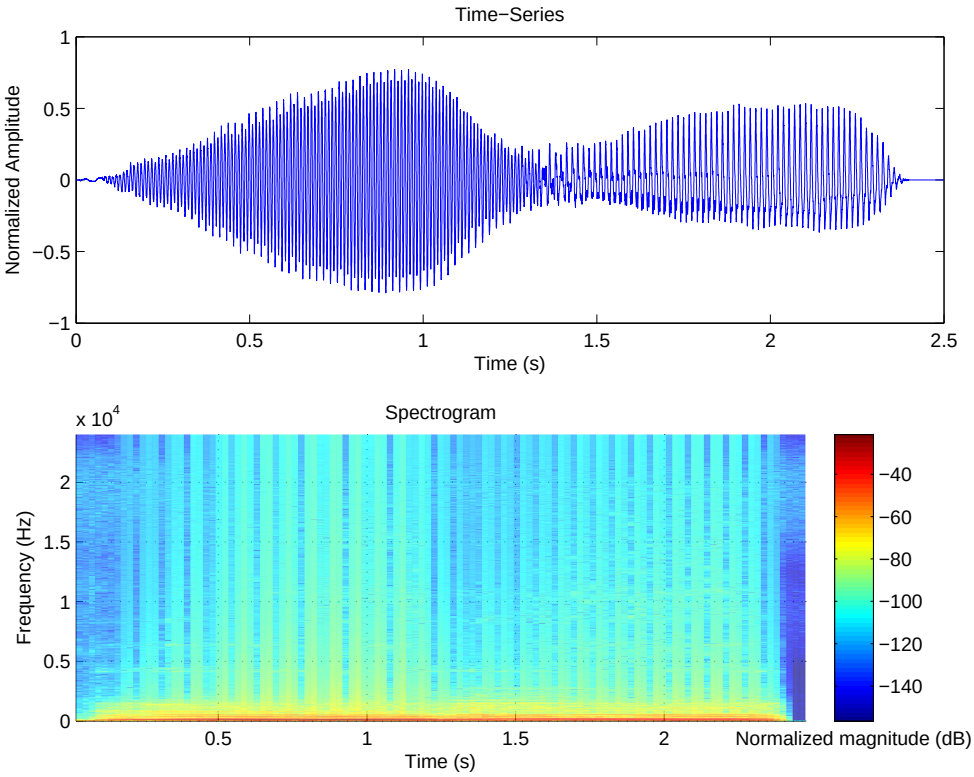


Figure 3.5: Time-series (top) and spectrogram (bottom) plots of *Double-Bass* sound sample

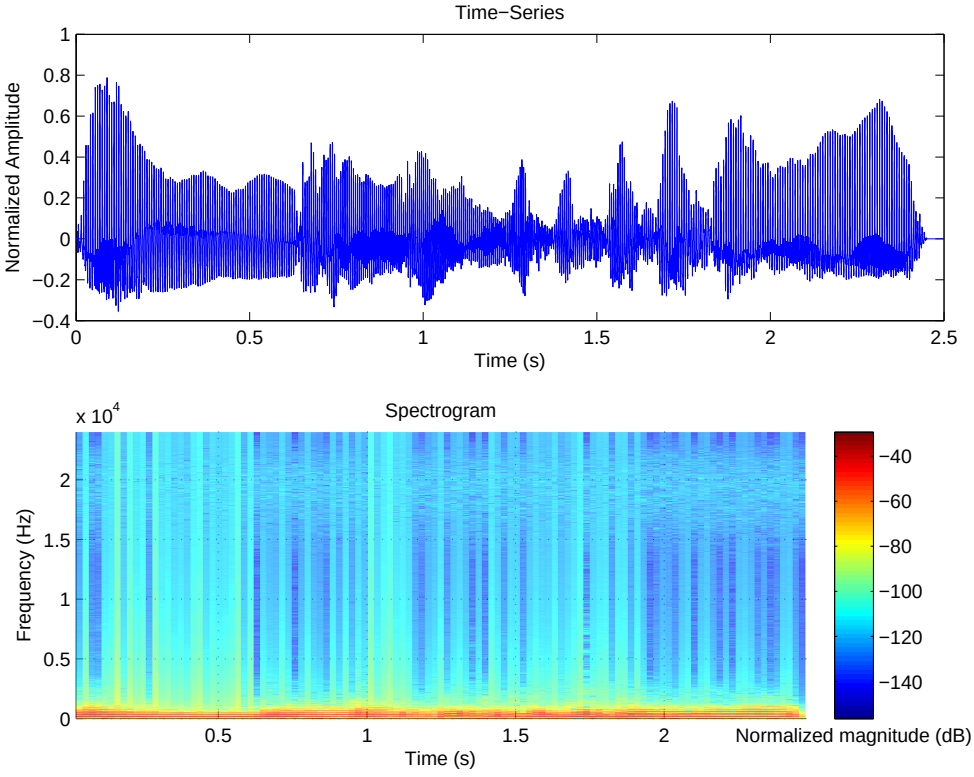


Figure 3.6: Time-series (top) and spectrogram (bottom) plots of *Tuba* sound sample

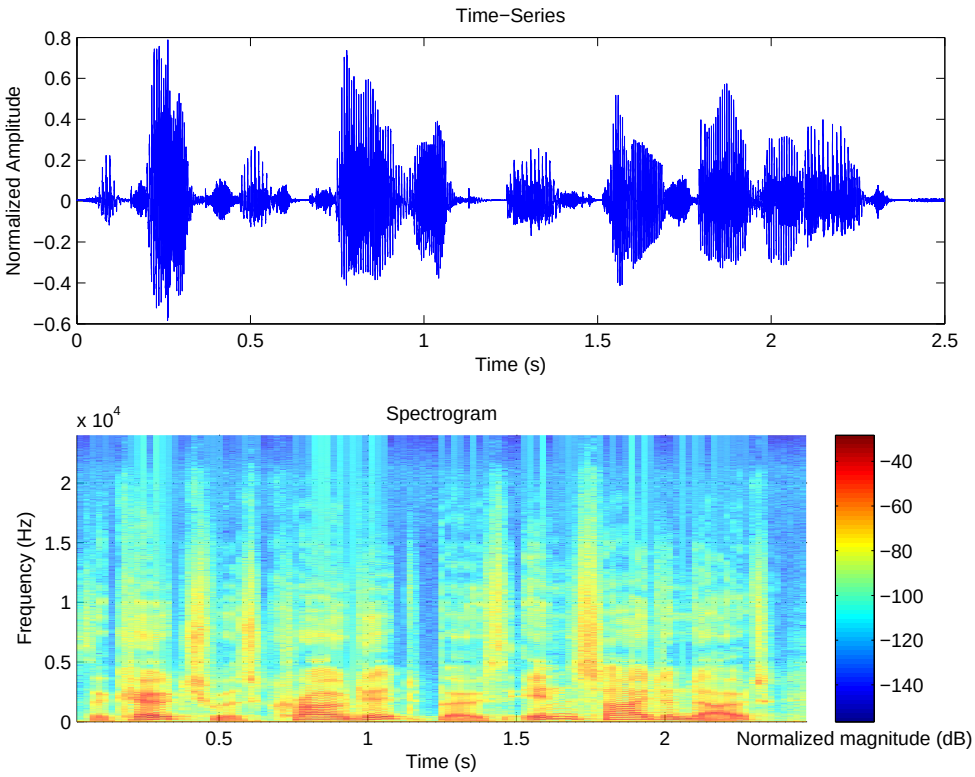


Figure 3.7: Time-series (top) and spectrogram (bottom) plots of *English Male Speech* sound sample

Instead the transient error was extracted from the output of the system model and then scaled. This method is described in [39], and extracts the error signal by subtracting the reference output signal from the signal with the transient glitch. The error signal is then scaled by a given factor, and added to the reference signal, thus generating a test file with a scaled glitch error. For application in a reference listening test, the error was scaled in 1 dB steps from 6 dB to −60 dB, generating a total of 67 test files for each sound sample. For the objective evaluation a finer granularity was used, with the error being scaled in 0.1 dB steps from 6 dB to −60 dB. All three sound samples used for the evaluation were normalized to have the same peak levels, thus generating approximately the same glitch peak error value. The peak value of the glitch is given by the gain steps and the attack level as described in Sec. 2.3. However, since the AGC operates in discrete time the actual glitch peak level will not be exactly the same for all three sounds samples.

3.5 Reference Listening Test

In order to assess the possibility of using the ADB and MFPD models for objectively evaluating the audibility of the transient glitches, a reference subjective evaluation was required. Thus, a listening test was carried out. Since it is the audibility of the glitches and not the audio quality that is of importance, non-trained test subjects were used in the listening test all with presumably having normal hearing. All experiments were approved by the Science-Ethics Committee for the Capital Region of Denmark (reference H-3-2013-004).

3.5.1 Alternative Forced Choice Test

To subjectively evaluate the audibility of transient glitches the listening tests were conducted using a three interval three alternative forced choice (3I3AFC) test [40]. In this test the subject is presented with three identical sound samples, or intervals, where one of the intervals contains the transient glitch. Each sound sample is played once, and after all sound samples have been presented, the test subject has to select which of the three samples, or alternatives, that contained the transient glitch. For each test the order that the samples are presented is randomized.

An alternative to the 3I3AFC test is the 3I2AFC, where the first interval always plays the sound sample without the transient error, and is thus used as a reference to compare against. The test subject then only has to select which of the latter two intervals that contains the transient error, thus only having two alternatives. From a statistical point of view, this increases the probability that the test person by random selects the sample with the distortion: from 1/3 in the 3I3AFC test to 1/2 in the 3I2AFC test.

By using the alternative forced choice test, the evaluation of the audio samples is binary; either the test subjects are able to hear the transient glitch or they are

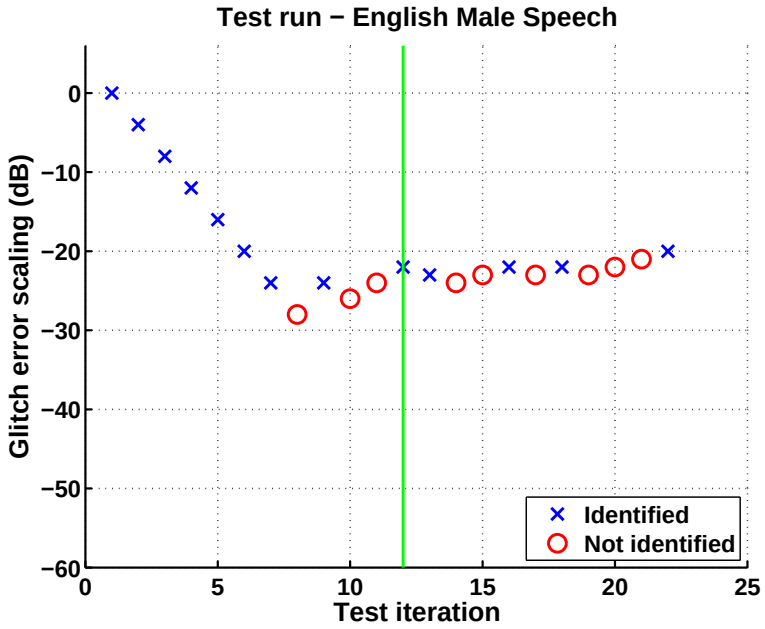


Figure 3.8: Listening test run example. Search part of test to the left of the vertical green line; measurement part to the right

not. The test subjects do not have to grade the audio quality using a specific grading scale, similar to the one used in the BS.1116 standard. This has the benefit that the test subject does not need to be trained in using the scale in order to get useful result, making the subjective evaluation of the adaptive A/D conversion channel more easily conducted.

3.5.2 Up-Down Test Method

To determine the level at which the transient glitches were no longer audible, an Up-Down test was used [41]. The purpose of the Up-Down method is to adjust the level of the error that is to be evaluated, based on the past answers of the test subject. For a given test with a specific transient glitch peak level, if the test subject was able to identify the interval containing the glitch, then the peak level of the transient glitch would be lowered in the following test. If the test subject was unable to identify the interval containing the glitch, the following test would have a larger peak value of the glitch.

This equals a 1-up 1-down test, and it was used as it identifies the point of 50 % probability of detecting the glitch. This is the same point that is found using the MFPD and ADB, making the results of the subjective and objective tests comparable.

An example of a single test run is shown in Fig. 3.8. As seen from the figure the change in the glitch level is different in different parts of the test run. Basically the test tries to identify the detection point by doing a search. In the first part the glitch level was adjusted in steps of 4 dB, in order to more rapidly get to

the level at which the glitch was no longer detectable by the test subject. After the first point, where the glitch could no longer be detected by the test subject, the glitch was increased by 4 dB until the glitch could once again be detected. Then followed another search using a smaller step size of 2 dB when adjusting the glitch level. Once the glitch could no longer be detected, the glitch level was increased by 2 dB until once again being detectable. This initial part, using 4 dB and 2 dB steps, is identified as the search part of the test where the approximate detection level is determine. Then followed the actual measurement part, where a 1 dB step was used.

By using adaptive steps in the test run, the approximate detection point is more quickly determined in comparison to only using a 1 dB step throughout the whole test. Thus, the duration of each test run would shorter, reducing fatigue of the test subject, which may affect the results of the test.

From the measurement part of the test run, the average of six test points were used to determine the threshold. The six points were chosen as the three peaks and three valleys, as identified in Fig. 3.8.

3.5.3 Conducting the Listening Tests

The listening test was carried out using 15 untrained persons in the age range from 24 to 34 years; all were assumed to be normal hearing based on interviews prior to the actual tests. The test persons were placed in a double-wall sound-attenuating listening booth, as shown in Fig. 3.9. The sound samples were played back using a pair of Sennheiser HD 580 Precision headphones connected to a RME DIGI96/8 24 bit D/A converter with a 48 kHz sample rate. The signal playback level was 68 dB SPL, with peak level at 76 dB SPL. The test was carried out using the AFC MATLAB package [42] on a PC, and the test subjects were guided through the listening test. A screen dump of the user interface is shown in Fig. 3.10.

Each test consisted of ten test runs; an initial training run and three runs for each sound sample. The training run was used for training the test subjects in the usage of the interface, thus removing this distraction during the real test runs. The test was repeated three times for each sound sample to reduce the variance of the estimated threshold level for each test person. Each test took approximately 1 hour, depending on how quickly the measurement phase was reached during each test run.

The results of the listening test are summarized in Table 3.4, listing the mean threshold value for each sound sample together the 25% and 75% quartiles. The values were calculated for each sound sample from the mean of the 50% probability point of detection for each test subject. To validate that the results were normally distributed, as expected, the results were plotted in a normal probability plot. For normal distributed data the data points would placed along the straight line. The normal probability plots of the results for the three sound samples is shown

Figure 3.9: Picture of the listening booth used for conducting listening tests

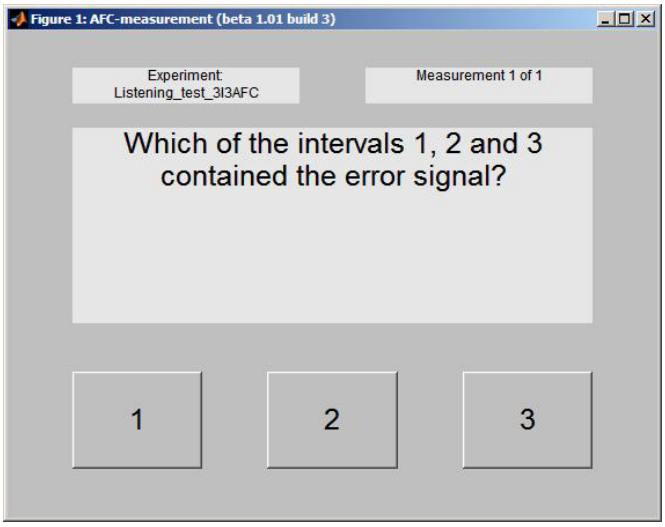


Figure 3.10: Interface of the AFC MATLAB package used for the listening test

in Fig. 3.11. As seen from the figure, for each sound sample the results follow somewhat the straight probability lines, indicating normal distributed results. However, with only 15 test subjects the statistics are somewhat weak.

Based on the results listed in Table 3.4, it is clear that the transient glitch is more easily masked by the audio content in the *English Male Speech* sound sample compared to the two others. This is the case even though the *English Male Speech* sound sample generated the largest number of gain changes and thus glitches. As already discussed, the frequency content of this sound sample has more high frequency content, and the results were as expected. Similarly, the *Double-Bass* and *Tuba* sound samples have primarily low frequency content, that does not easily mask the transient glitch. Of the two sound samples, the results of the listening test indicate that the *Tuba* sound sample is the worst of the three in relation to masking the transient glitch. Based on these results, the *Tuba* has subsequently been used for evaluating the adaptive A/D conversion channel as a

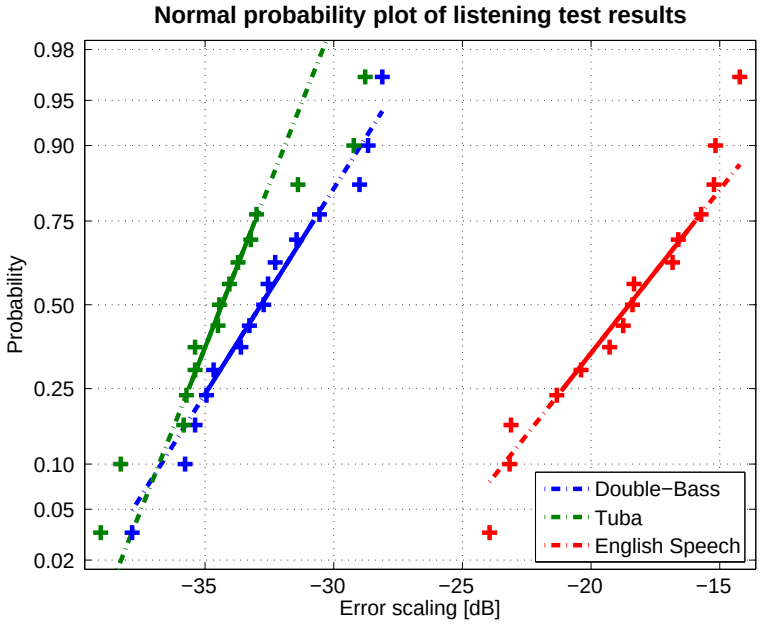


Figure 3.11: Normal probability plot of listening test results

Table 3.4: Statistics for the transient error detection threshold levels from the results of the listening test, based on 15 test subjects

	Test signal group		
	Double-Bass	*Tuba*	*English Male Speech*
$Q1$	-34.9 dB	-35.6 dB	-21.1 dB
$Q2$	-32.7 dB	-34.4 dB	-18.4 dB
$Q3$	-30.8 dB	-33.1 dB	-15.9 dB
$\bar{x}$	-32.7 dB	-34.1 dB	-18.7 dB
s	2.81 dB	2.84 dB	3.15 dB
Steps {up,down}	{4,4}	{10,11}	{17,17}

reference worst case signal.

Another important result from the listening test is the scaling necessary to reach the 50% probability point of detection; for the *Tuba* signal a reduction of approx. 34 dB on average, being equal to a factor of 50. Note that this results is dependent on the actual playback level used for the test, but nevertheless it is a significant reduction in the peak level of the transient glitch. Based on these results it seems evident that simply reducing the gain step size is not a possible solution for making the transient glitches inaudible. The small gain step sizes would require a large increase in the circuit area needed for the VGA as discussed in Sec. 2.5.1. Also due to the AGC loop delay, the AGC would be too slow to avoid distortion of the signal processed by the conversion channel. A similar result was found in [43], identifying that another solution is needed in order to reduce or remove the transient glitches from the adaptive A/D conversion channel.

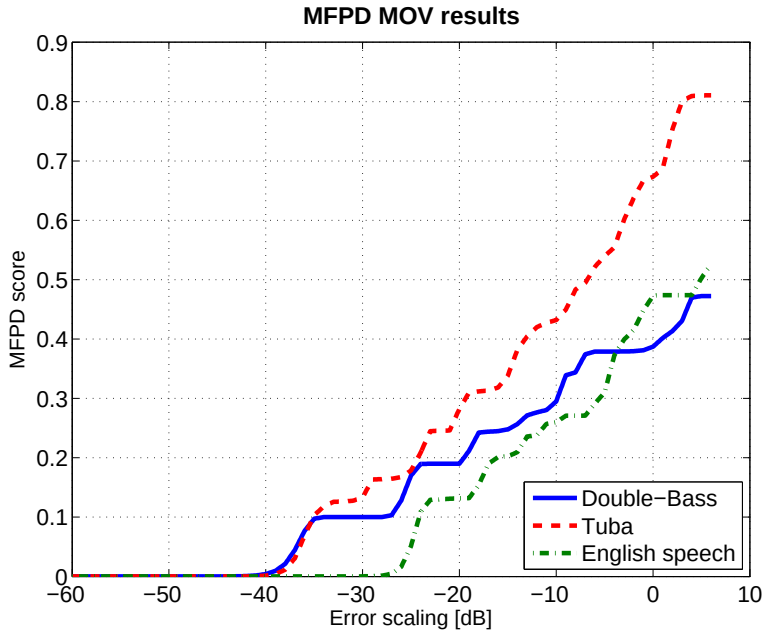


Figure 3.12: Results from MFPD evaluation of the conversion channel

3.5.4 Bias Errors

A problem when simply scaling the peak value of the transient glitch is that the transient glitch occurs at the same time instance in each sound sample. When conducting the reference listening test, some test subjects noticed that the glitch occurred at the same time instance, thereby being better at detecting the glitch, than if this was not the case. This bias in results causes the detection threshold to lower than in real life applications, where the occurrence of a glitch is unknown.

3.6 Objective Evaluation

For the objective evaluation an implementation of FFT based PEAQ model was used [44]. This implementation outputs the score of each MOV, making it possible to extract the score from the ADB and MFPD MOVs. The sound samples used with for the listening test were also used with the PEAQ model, but with a finer granularity in the error scaling; here a 0.1 dB step was used while a granularity of 1 dB were used for the listening test. The results of the objective evaluation are shown in Fig. 3.12 and Fig. 3.13 for the evaluation using the MFPD and ADB respectively.

The results for the MFPD evaluation, in Fig. 3.12, shows that there is a difference between the three sound samples. The MFPD score equals the probability of detecting, with the output 0 being equal to the distortion not being detectable. As seen from the plots, the error scaling at which the glitch becomes inaudible is lower for the *Tuba* and *Double-Bass* sound samples compared to the *English*

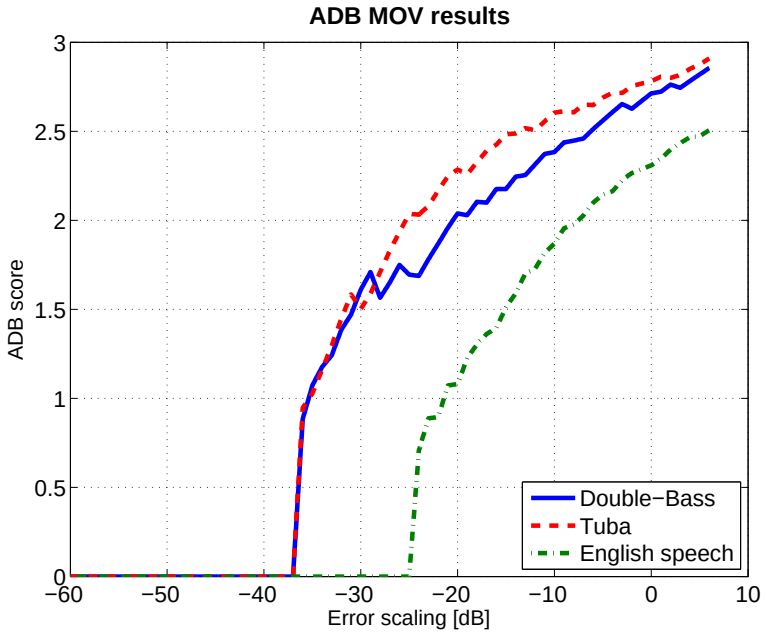


Figure 3.13: Results from ADB evaluation of the conversion channel

Male Speech. The same result was found in the listening test, and identifies that the MFPD may be a useful objective measure for the audibility of the glitches. Similarly, it is interesting to note that the MOV output for the *Tuba* sound sample is consistently higher than for the *Double-Bass* sound sample. As given in Table 3.4, the *Tuba* sample has more gain changes and thus glitches than the *Double-Bass*, which should result in a larger probability of detecting the glitches.

For all three sound samples, the MFPD curves have plateaus where the MFPD score is constant even though the error is different due to the scaling. To understand this behavior, a more detailed understanding of the psychoacoustical modeling behind the MFPD MOV would be required, and is beyond the scope of this thesis.

The results of the ADB MOV are shown in Fig. 3.13. Similar to the MFPD, an ADB score of 0 equals that no distortion is audible in the test signals. The same trends found in the MFPD output are identifiable in the ADB output. The *English Male Speech* sound sample reaches an ADB value of 0 for larger transient glitches than for the two other sound samples. Similarly, the *Double-Bass* and *Tuba* samples reach an ADB score of 0 at the same scaling of the transient glitch. Also for larger scaling values, the ADB score is higher for the *Tuba* sample than for the *Double-Bass* sample. The ADB curve does not have the plateaus as was the case for the MFPD.

When comparing the error scaling value at which the MFPD and ADB MOVs reach the value 0 for each sound sample, the results are in the same range.

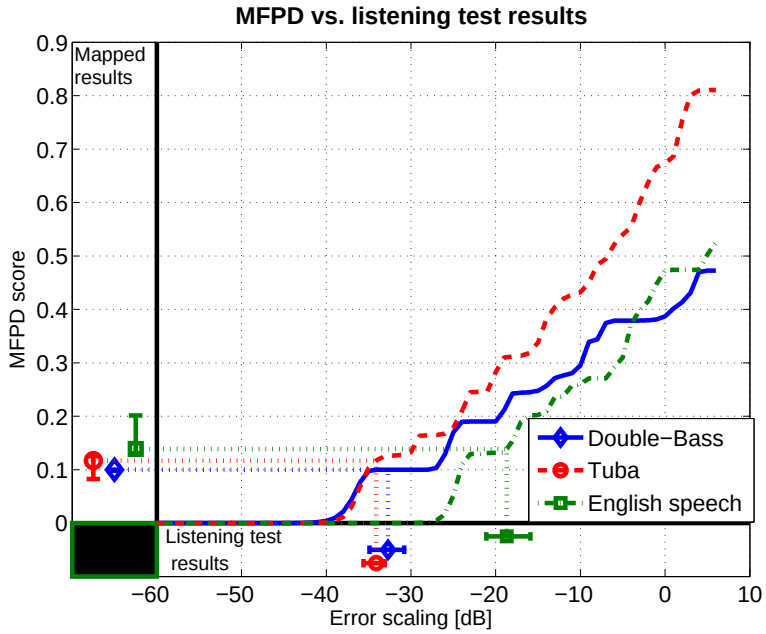


Figure 3.14: Mapping of listening test results onto MFPD results

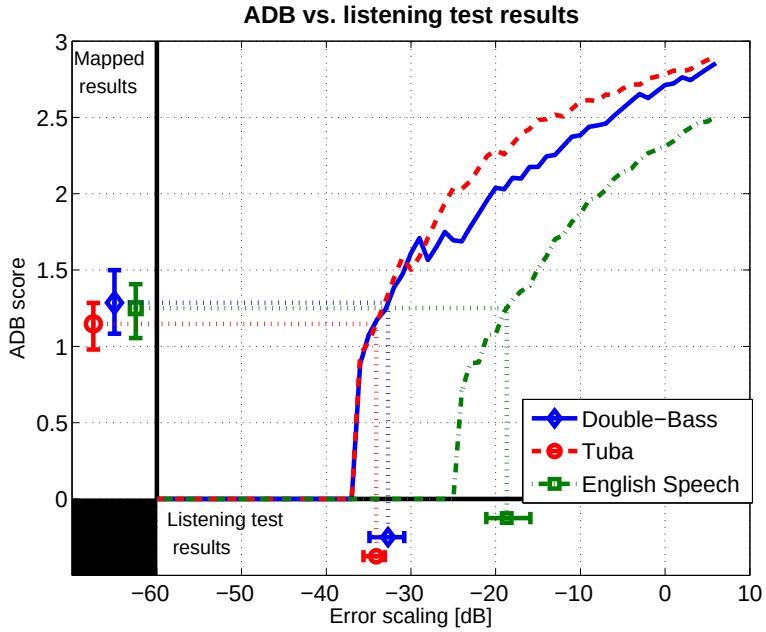


Figure 3.15: Mapping of listening test results onto ADB results

3.7 Comparison of Subjective and Objective Evaluation

To evaluate the applicability of the ADB and MFPD as objective measures for the audibility of the transient glitch, the results of the listening tests have been mapped onto the curves of the MOVs.

The resulting mappings can be seen from Fig. 3.14 and Fig. 3.15 for the MFPD and ADB respectively. From the listening test results the mean value and the 25% and 75% quartiles of the error scaling level is mapped onto the curves to determine the equivalent MFPD and ADB scores at these levels.

For a good mapping of the listening test results to the MOVs, the resulting mapped MFPD and ADB scores should be in the same range for all three sound samples. For the ADB the listening test results all are mapped to the same range on the y-axis, thereby identifying a good correlation between the objective and subjective tests. Thus, the ADB appears from the mapping to be a good candidate for objectively evaluating the audibility of the transient glitches.

For the MFPD the listening test results also map to the same range on the MFPD score axis. However, the variations defined by the 25% and 75% quartiles do not map similarly well as for the ADB. From the curves in Fig. 3.14 this poor mapping is due to the plateaus in the MFPD curves.

Generally, none of the listening test results mapped to a score of 0 for either the ADB or the MFPD. This may be due to the fact, that the test signals were played back at a reasonable playback level, at which the test subjects would not experience fatigue or pain in their ears. The playback level is not defined in the PEAQ method, and is not modeled in the MOVs. Thus, it is expected that for higher playback levels, the detection threshold level found in the listening test be lower even lower, meaning a smaller peak error level would be needed.

3.8 Applicability of Objective Method

Assuming that the ADB and MFPD are able to model the audibility of the transient glitches, the relevant question is then which ADB and MFPD score to aim for when evaluating the audibility of the transient glitches in the adaptive A/D conversion channel. Based on the mapping of the listening test results onto the MOVs, an ADB score between 1 and 1.5, and a MFPD score below 0.1 and 0.2 would seem to be sufficient. However, due to the playback level used during the listening tests, it would be safer to aim for an ADB and MFPD score of 0. From the mathematics behind the MFPD, briefly described in Sec. 3.2.3, a score of 0 equals that the distortion is inaudible. An ADB score of 0 only identifies that there are no distortions with a probability of detection above 50%. The conclusion is thus, that the conservative estimate would be to aim for an ADB and MFPD score of 0. If the the acceptable ADB and MFPD ranges achieved from the listening test are used, the evaluation should be combined with a final evaluation based on a listening test. In the end the subjective evaluation is the true tests of the audio performance of the channel.

The ADB and MFPD were used in a system model, where it was possible to generate a reference signal that was in phase with the actual test signal. The requirement of the reference and test signal to be in phase, somewhat complicates the usefulness of the objective method. In a real life system, other non-idealities

are present in the test signal. For a MEMS microphone this includes harmonic distortion and noise. It is thus relevant to investigate the sensitivity of the MFPD and ADB MOVs to these other non-idealities when evaluating test signals with transient glitches.

3.9 Summary

The evaluation of the audibility of the transient glitches generated by the adaptive A/D conversion channel is an important task, as the glitches are an inherent non-ideality of the conversion channel that needs to be minimized. In order to minimize the transient glitch it is necessary to be able to continuously evaluate this design parameter during the design phase of the conversion channel. In this chapter an objective method has been presented for carrying out this task.

The method is based on the MOVs ADB and MFPD, that are submodels used in the PEAQ method for evaluating the probability of detecting the presence of a errors in a given audio signal. The ADB and MFPD scores are based on a comparison of the signal under test with an error free reference version of the signal. The proposed objective method was compared with the results obtained from a listening test, and the comparison showed a good correlation between the results from the objective evaluation and the listening test. However, the interpretation of the results from the ADB and MFPD models is still an open question. From the theory behind the ADB and MFPD an output of zero for both MOVs would indicate that the error is inaudible in the test signal. In the comparison of the ADB and MFPD with the listening test results, the detection threshold found from the listening test did not equal a score of 0 in the MOVs.

The objective method also requires access to a reference signal to compare against the signal under test, and furthermore the two signals need to be in phase to obtain correct results. The impact of errors, other than the transient glitch, on the ADB and MFPD scores has not yet been investigated. This is necessary if the method is to be applied to real systems where noise and distortion may be present in the signal under test.

The presented method is a promising tool to the problem of evaluating the transient glitches generated in the adaptive A/D conversion channel. It may be applied during the design phase, to evaluate whether the transient glitch has been sufficiently suppressed. However, the method does not replace the use of standardized listening tests for the final evaluation of the system.

4

Reduction of Transient Glitches

This chapter presents a method for reduction of the transient glitch errors generated in the adaptive A/D conversion channel during a gain change event. The method is based on generating an estimate of the output signal during the gain change event and output the estimate during the transition period; the transient glitch is thereby removed from the conversion channel output signal. The output estimate is generated as a linear extrapolation of the output signal, based on the signal slope prior to the gain change. The linear extrapolation generates another transient error, but one that is smaller. The method has been evaluated using audio samples, and from inspection of the spectrogram of the processed sound samples it is found that the method effectively removes the glitches from the channel output. From both objective and subjective evaluations the errors generated by the method are inaudible. Thereby the method solves the main problem of the adaptive A/D conversion channel, as the conversion channel no longer needs to be optimized for a reduction of the transient glitches. This is a significant result of this project, that simplifies the design of the subblocks of the adaptive A/D conversion channel; in particular the design of the AGC and the VGA. The presented work is based on the European Patent Office application PCT/EP2014/059488, App. B.

4.1 Existing Methods

It is unwanted to have the transient glitches present in the output of the adaptive A/D conversion channel; this in particular for audio systems where the glitch is audible by the receiver and thus cannot be simply filtered when detected.

There already exist different methods for reducing switching transients in AGC based conversion channel, all based on having multiple gain channels with different gain levels operating concurrently. The extra paths can have either static or adaptive gain settings. An example of this approach is described in [45] using multiple signal paths, all optimized for a predefined dynamic range, as shown

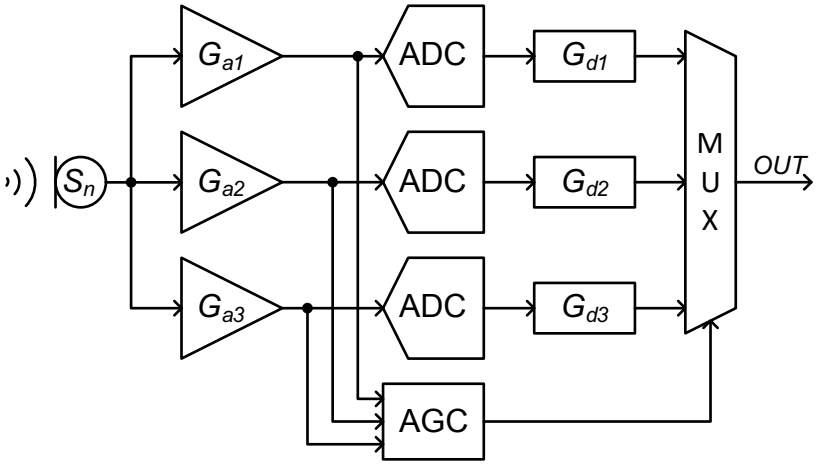


Figure 4.1: Adaptive A/D conversion channel based on multiple static conversion channel [45]

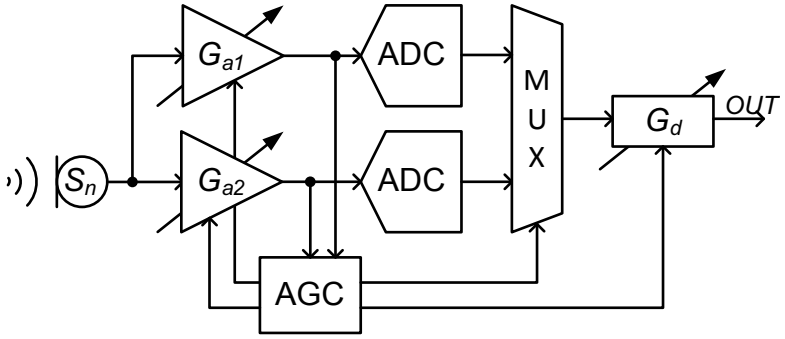


Figure 4.2: Adaptive A/D conversion channel based on two adaptive conversion channels [46]

in Fig. 4.1. A lower analog gain in a signal path is compensated digitally, so that the overall channel gain is constant. Each signal path consist of a static analog gain stage, an ADC and a static digital gain stage, with all signal paths operating concurrently. When the analog gain is to be adjusted, it is only a matter of selecting the correct output digitally, and no transients are generated in the channel. However, the major drawback of this approach is the high current consumption resulting from all channels operating continuously. As the paper suggests, this current consumption is lower, since the requirements of each path is significantly smaller than for a single path which has to handle the full dynamic range. In comparison with the adaptive A/D conversion channel presented in this thesis, the current consumption of the solution presented in [45] will be larger due to the multiple analog amplifiers and ADCs. Area wise the design will also be larger than the single adaptive channel solution. The circuit may be able to avoid transient glitches, but at the cost of larger circuit area and current consumption.

A somewhat similar solution was investigated in [46], where a dual channel solution was used, with each channel consisting of a VGA and an ADC, as shown in Fig. 4.2. With two channels, the channels are configured to have different gain settings at any given time. Consider the case of channel 1 having the VGA

gain, G_{a1}, set to the maximum gain, while in channel 2 G_{a2} is set to a gain one gain step lower than G_{a1}. It is then possible to switch to a lower gain setting by switching the input to the digital gain block from the output of channel 1 to that of channel 2. At the same time, the gain level of channel 1 is reduced to one gain step below that of channel 2, and channel 1 is then allowed to settle to the new gain level. This solution requires fewer channels than the solution described in [45], while still avoiding switching glitches; however only for the case where a single gain step is sufficient. If a large change in gain is necessary, transient glitches will be generated and be present in the conversion channel output. The solution in [46] thus only partly solves the problem of transient glitches, while still requiring more circuit blocks than the single channel solution.

A combination of the two above described solutions, is presented in [47]. This patent describes a system with multiple signal paths, all containing a VGA. The gain levels in the different paths are adjusted on a turn-by-turn basis, and thus reducing the number of extra signal paths required.

For all of the above described solution, the main drawback is the need for multiple channels to operate concurrently, but more importantly, larger circuit area is required for realizing the channels. Thus, for applications with limited circuit area and current consumption, the single channel implementation is the preferred choice.

4.2 Gain Step Size

The expression for the glitch error was given in Sec. 2.3, and is repeated here for reference:

$$e(t) = \Delta G \cdot [h(t) - s(t)] \cdot x(t) \tag{4.1}$$

where ΔG is the change in gain, $h(t)$ is the Heaviside step function, $s(t)$ is the step response of the signal path from the amplifier output to the digital gain block, and $x(t)$ is the input signal to the digital gain block and the AGC detector. From (4.1), the size of the gain step used by the AGC has an impact on the peak value of the transient glitch. By simply reducing the gain steps, it is possible to reduce the peak value of the glitch error. However, as already mentioned in Sec. 2.4.6, when using smaller gain steps for a specific change in gain level more steps may be required. This causes more gain switching events and thus more glitches to appear in the channel output. Using smaller gain steps also introduces the risk of signal clipping for input signals with large amplitudes, due to the longer gain transition time.

To compensate for this, larger step sizes could be used by the AGC when needed, but larger gain steps would cause glitches with large peak values, and thus remove the benefit of having smaller gain steps.

As seen from (4.1), the signal level at the moment of the gain change has an impact on the peak value of the glitch. Since this is set by the attack level of

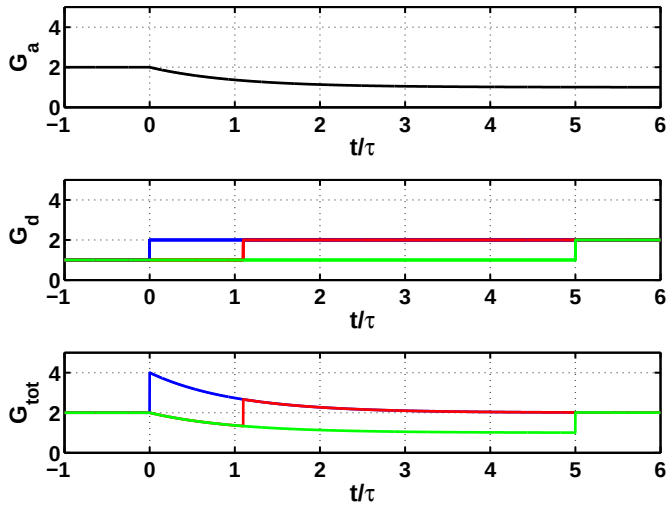


Figure 4.3: Total channel gain, G_{tot}, when delaying the change of G_d by 0τ (blue), 1.1τ (red) or 5τ (green)

the AGC, the glitch peak value could be reduced by lowering the attack level. As already discussed in Sec. 2.4.3 this is not a practical solution due to the reduced SNR of the conversion channel.

In [43], App. G, it was investigated how small the gain steps should be in order for the transient glitches to be inaudible; this evaluation was based on a subjective evaluation similar to the one described in Chap. 3. From the subjective listening test it was found, that with a gain step of 0.01 dB the glitches were still audible. A similar result was found in the listening tests described in Chap. 3. From an application point of view, this makes it impossible to remove the transient glitches simply by reducing the gain steps in the VGA. With a gain step of 0.01 dB it would require 600 gain changes to change the VGA gain by a total of 6 dB. Thus, a system level solution is required to remove or reduce the audibility of the transient glitches.

4.3 Digital Gain Adjustment

The transient glitch occurs due to the finite transition delay of the VGA and filters in the signal path between the VGA and the digital gain block. Since there is a delay in the conversion channel from the VGA output to input of the digital gain block, the glitch peak value may be reduced by delaying the gain change of the digital gain block.

Consider the case of an adaptive A/D conversion channel, with a VGA with a 1st order low-pass transfer function, and an ideal ADC. The total gain, G_{tot}, of the channel equals 2 and initially $G_a = 2$ and $G_d = 1$. Assume that G_a at t = 0 changes from 2 to 1 as shown in Fig. 4.3. At t = 5τ the gain has fully settled. The digital gain change from 1 to 2 should then occur within this time-frame. If it occurs at t = 0, the channel gain will increase abruptly and, to a 1st

order approximation, will then fall exponentially towards the final value. If the digital gain changes at t = 5τ, the channel gain will settle exponentially and then abruptly increase to the final gain level. If the digital gain change occurs at t = 1.1τ, the total gain will drop exponentially, abruptly increase at t = 1.1τ and then again drop exponentially towards the final value at t = 5τ. As seen from Fig. 4.3 the resulting gain errors are very different and with different steps in the total gain. The minimum amplitude gain error occurs when delaying the digital gain change to t = 5τ, but the error still generates an unwanted step in the gain curve.

The maximum peak error occurs when the digital gain change occurs at t = 0, since both the VGA and the digital gain block will be at the maximum gain setting. By delaying the digital gain change, the peak error value will be reduced. Overall delaying the change of the digital gain does not solve the problem of generating unwanted transient glitches in the channel output. They may be different from an psychoacoustic point of view, but simple listening test have shown that the glitches are still audible.

4.4 Zero Crossing Gain Change

As described in Sec. 2.3 and from (4.1), the peak value of the transient glitch depends on the signal value at the VGA output at the moment of the gain change. From this observation the peak value of the transient glitch would be minimized if the gain change occurred near the zero crossing of the signal. In the case of an attack event, where the analog gain is reduced, this is not a suitable approach, as an attack event occurs at the rising edge of the signal. If the AGC was to delay the gain change until the zero-crossing of the signal, clipping would occur far a large part of the signal; this clipping period would depend on the signal frequency, therefore being more problematic for low frequency signals.

For release events the approach is better suited, where clipping is not an issue. The worst case delay for the zero crossing transition is the half-period of the minimum signal frequency; for a 20 Hz signal the added delay equals 25 ms. The penalty of this increased release delay is an extension of the time-period where the analog circuit noise is higher. If this higher noise is acceptable, then the application of zero crossing gain change for release events is a simple method for reducing the peak value of the transient glitches during release events.

4.5 Glitch Reduction by Output Extrapolation

The problem with the transient glitches are, that they are present in the output signal from the adaptive A/D conversion channel. Reducing the peak value of the glitches by scaling only solves the problem, by making the glitches very small using small gain steps. In the existing solutions described in Sec. 4.1, instead

of the reducing the glitches they are instead removed by switching between the active signal path in the multipath conversion channels. In essence these methods replace the output signal from the gain adjusted channel with that from another channel, and thereby effectively remove the glitches.

Applying the same idea to the single path conversion channel, the glitches may be removed from the output signal by replacing the output signal with another signal during the gain transition period. With only a single channel it is necessary to generate an estimate of the output signal during the transition period. The signals processed by the conversion channel are audio signal, thus a composition of sine waves with frequencies from 20 Hz to 20 kHz.

The simplest estimate of the output may be found from a linear approximation. This may be generated based on two points on the curve. Based on the two points the slope of the curve, α may be estimated as:

$$\alpha = \frac{y_2 - y_1}{n_{est}} \tag{4.2}$$

where y_1 and y_2 are the output value at the two points, and n_{est} are the number of clock cycles between the two sampling points. The slop should be estimated continuously, since the input signal of the conversion channel is non-deterministic and a gain change thus may occur at any point in time. Therefore, the latest output value is continuously written to a register for use during the gain transition.

When the AGC detects that the signal in the channel has crossed the attack level, a gain change event occurs where the gain of the VGA is reduced and the gain of the digital gain block (DGB) is increased. At the same time the output of the conversion channel switches from the output of the digital gain block to the linear estimate. The output value during the gain transition period is the linear estimate, which is given as:

$$OUT\,[n] = OUT\,[n-1] + \alpha \tag{4.3}$$

where $OUT\,[n]$ is the output value at *nth* clock cycle, and $OUT\,[n-1])$ is the output value of the previous clock cycle. This continuous for a given number of clock cycles that equals the settling time of the channel gain.

An example of the linear extrapolation is given in Fig. 4.4, showing the linear estimate together with the ideal output and the output with the transient glitch. As seen from the plot, linear estimate does generate an error as expected. The estimate is only of the 1st order, and thus does not perfectly estimate the sinusoidal curves. Furthermore the error of the linear estimate depends on at what point on the sine wave the gain change occurs. The largest error would occur if the slope is based on the top of the sine wave, where the slope is minimum but the change in the slope is the largest. Another important aspect is the rate of change of the signal processed by the conversion channel. Since the duration of the gain transition period sets the length of the linear estimate, the linear approximation works best for slowly changing signals e.g. low frequency signals. For high frequency signals the output value will change more rapidly, increasing the

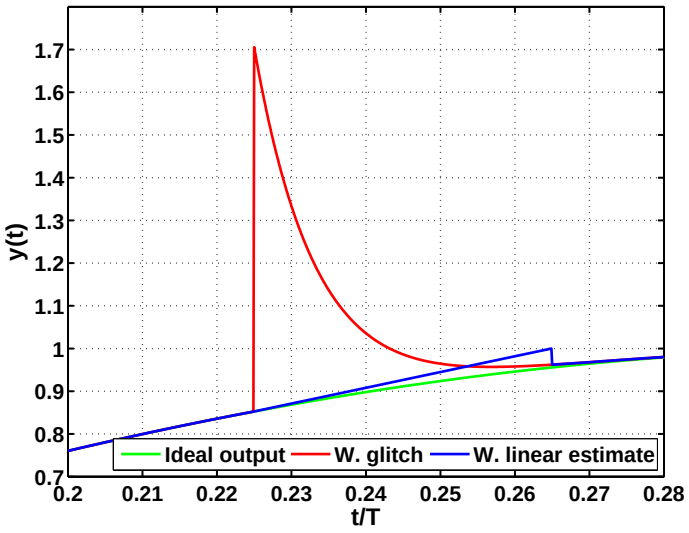


Figure 4.4: Example of glitch removal by linear extrapolation of output signal

error generated by the linear estimation; the duration of the estimation period is thus of importance. Overall the delay of the signal path should be minimized to reduce the extrapolation period.

Since the input signal to the conversion channel is an audio signal, containing multiple frequencies, it is difficult to quantify what the maximum error generated from the linear extrapolation is. It will depend on both the estimation period and the accuracy of the slope estimate.

As given from (4.2), the slope of the signal is estimated from two values of the signal. However, depending on the noise power of the signal, it may be necessary to further filter the signal in order to achieve a sufficiently good estimate of the signal points. As described in Sec. 2.5.2-2.5.3, the output of the $\Delta\Sigma$ ADC is a low-resolution oversampled signal, that is sufficiently low-pass filtered for the AGC to detect the signal level. However, in order to minimize the AGC loop delay, the LPF is not a full decimation filter. Therefore, a significant noise is still present in the signal after the digital gain block. It is thus necessary to further filter the signal in order to acquire a sufficiently good estimate of the signal slope. To avoid further delay of the signal the filtering may be done for the slope detection alone, by estimating the values of the output signal as time averages of the output signal. The averaging functions as a low-pass filter, and by having the number of samples used for the averaging to be in powers of 2, the averaging is easily realized using bit-shifts.

4.6 Extended Conversion Channel Model

To evaluate the ability of the output extrapolation method to reduce the audibility of the transient glitches, a high-level model of the adaptive A/D conversion channel was developed in MATLAB. The model is an extension of the high-level

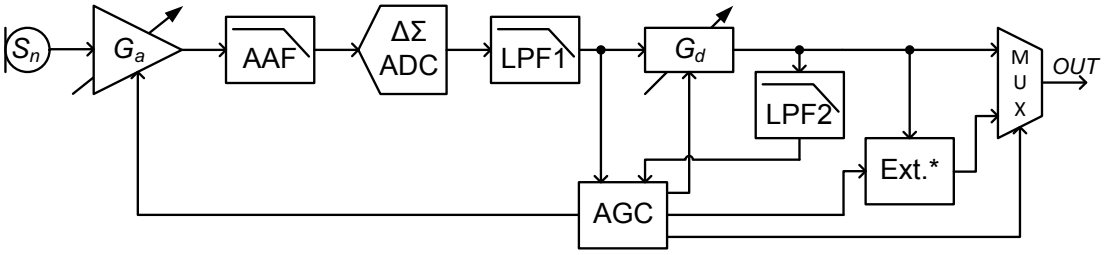


Figure 4.5: Block diagram of adaptive A/D conversion channel with glitch removal

model used for the listening test, as described in Sec. 3.3. The model has been extended to include a full model of a ΔΣ ADC including quantization, more elaborate low-pass filtering and with the addition of the output extrapolation method to the AGC controller. A block diagram of the model is shown in Fig. 4.5.

The VGA was modeled as a zeroth order system with an output limiting function to model clipping in the analog domain. The VGA has a gain range from 0 dB to 18 dB with 6 dB gain steps. The AAF was realized as a 1st order low-pass filter. The ΔΣ ADC was realized with a 4th order loopfilter with a 2 MHz sampling rate and a 5 level quantizer. Due to the low bit resolution at the output of the ADC, more elaborate filtering was needed in between the ADC and the AGC. Therefore, the *LPF1* block was realized as a cascade of a 2nd order Bessel filter and a 1st order Sinc filter. The digital gain block was realized with the same gain levels as for the VGA, in order to achieve a conversion channel gain of 18 dB. The analog blocks and the ADC were modeled without circuit noise, but the quantization noise of the ADC is present in the system.

After the digital gain block follows a multiplexer (MUX), in order to output the extrapolated output signal during a gain change event. The *LPF2* block is used by the AGC to acquire a sufficiently good estimate of the output signal value, for use when estimating the signal slope. Since the *LPF1* does not filter out all noise in the ADC output signal, there is still a significant amount of noise in the output signal of the digital gain block. This results in a large variation between each sample, but the average value of a number of samples may be used as an estimate of the actual output signal value. Thus, the *LPF2* block is realized as a Sinc filter, that calculates a running average of the output signal. Since two output values are needed to estimate the signal slope, as given from (4.3), the AGC continuously estimates the output signal values. Once a new point has been estimated the signal slope is determined based on (4.2). Once a gain change event occurs, the latest calculated slope estimate is used for the output signal extrapolation.

The output estimation is enabled by the AGC once a gain change event occurs, and the output of the channel is, via the MUX, switched from the output of the digital gain block to the output of the extrapolation block *Ext.**. After the output estimation period the output is switched back to the output of the digital gain block.

Both the analog and digital parts of the model were realized as sampled systems,

Table 4.1: Properties of noiseless adaptive A/D conversion channel model used for evaluation of glitch reduction method

Property	**Value**
Sampling frequency	2 MHz
Signal bandwidth	20 kHz
Channel gain	18 dB
Gain levels	0 dB, 6 dB, 12 dB, 18 dB
Gain step	6 dB
Analog full-scale level, V_{FS}	1
Analog limiter level	-4 dBFS
AGC attack level	-6 dBFS
AGC release level	-14 dBFS
AGC attack sense time	0 s
AGC release time	50 ms
AGC dead time	20 µs
AGC digital gain delay	0 s
AGC output estimation time	40 µs
ADC loopfilter	4th order
Quantization levels	5
Anti-aliasing filter	1st order, $f_c = 300$ kHz
Low-pass filter (LPF1)	2nd order Bessel filter, $f_c = 20$ kHz and 1st order Sinc filter, $N_{taps} = 50$
Low-pass filter (LPF2)	1st order Sinc filter, $N_{taps} = 16$

with the input signal being upsampled to the 2 MHz sampling frequency of the ADC. A summary of the specific model properties used for the model are given in Table 4.1.

4.7 Evaluation

4.7.1 Constant Amplitude Sine Wave

To see the extrapolation function in action, the system was first evaluated using a constant amplitude sine-wave with a frequency of 1 kHz and a normalized amplitude of 0.05. The outputs of the sub-blocks of the conversion channel during a gain transition event are shown in Fig. 4.6, with a zoom-in around the gain transition event shown in Fig. 4.7 In Fig. 4.7b is shown the output of the VGA, clearly showing the zeroth order response when adjusting the gain. From Fig. 4.7c and Fig. 4.7d are shown the output of the AAF and LPF1 respectively, from which the delay of the low-pass filters is evident. The output of LPF1 is also the input to the AGC peak detector, and in Fig. 4.7d the attack level is plotted as well. At $t = 0.19$ ms an attack event triggers the reduction of the VGA gain and, at the same time, an increase of the digital gain. From Fig. 4.7e is

shown the output of the digital gain block, clearly showing the generation of the transient glitch. However, as shown in Fig. 4.7f the channel output during the gain transition period is the estimated output, until the end of the estimation period at $t = 0.23$. The transient glitch is thus effectively removed, and replaced by the linear extrapolation of the output. A small step at the end of the estimation period still remains.

4.7.2 Audio Signals

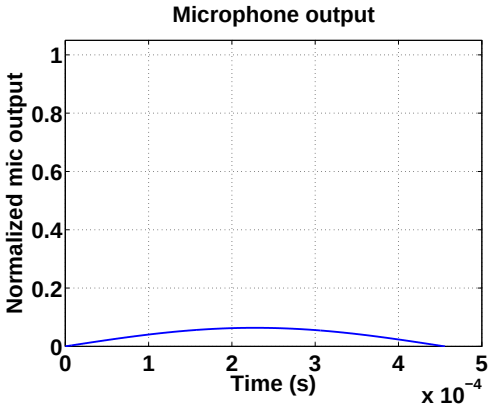
Next the glitch reduction method was evaluated by using as input signal the same sound samples that were used for the objective evaluation investigation, as described in Chap. 3. The amplitude of the sound samples were normalized, so that the peak signal value was -9 dB of the analog full-scale level. The sound samples were upsampled to the sample rate of the conversion channel model. The output of the model were filtered and downsampled to 48 kHz sample rate using the `resample` function that is part of the *Signal Processing Toolbox* for MATLAB. This function also includes decimation filtering.

For reference the sound samples were also processed using a model of the conversion channel with the same properties listed in Table 4.1, but with the output estimation method disabled. To compare the result of the extrapolation method with the digital gain delay method, another conversion channel model was also used. This model also used the same properties listed in Table 4.1, but with the estimation method disabled and with the digital gain delay set to 20 µs.

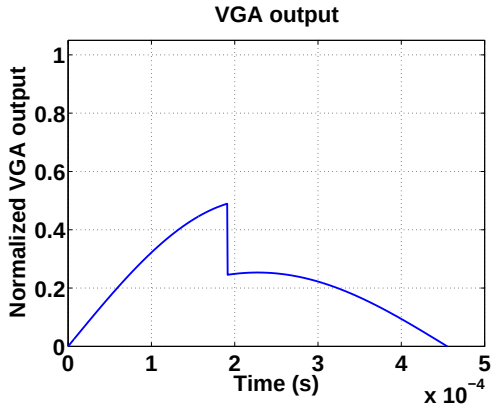
The spectrogram of the resulting output signals for the *Double-Bass*, the *Tuba*, and the *English Male Speech* sound samples are shown in Fig. 4.8, Fig. 4.9 and Fig. 4.10 respectively.

For the *Double-Bass* sound sample, in Fig. 4.8a the output signal is shown without any glitch reduction method applied. The glitches may be seen as full drawn yellow/green lines along the y-axis. Several glitches are present in the output, one of them at $t \approx 1.9$ s. In Fig. 4.8b is shown the spectrogram of the output when applying the digital gain delay method. The glitches are not as clearly seen, but at $t \approx 1.9$ s a full drawn green line is present. From the color bar, a green color indicates a lower signal power, thus meaning that the digital gain delay method does reduce the signal power of the glitches, as expected. In 4.8c is shown the spectrogram of the channel output when applying the output extrapolation method. The glitches can no longer be clearly identified, and the remaining high frequency content is due to harmonic tones present in the input signal.

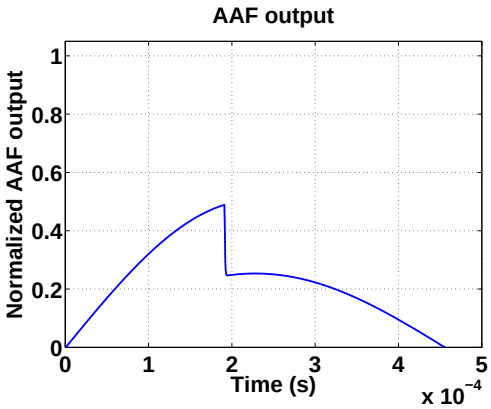
The results for the *Tuba* sound sample without glitch reduction is shown in Fig. 4.9a, where several glitches are present, one at $t \approx 2.2$ s. Comparing this with the spectrogram of the output with the digital gain delay method and the linear extrapolation method, in Fig. 4.9b and Fig. 4.9c respectively, it can again be seen that the linear extrapolation method is better at suppressing the transient glitches.



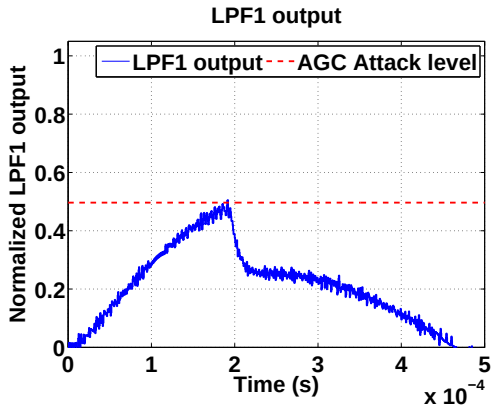
(a) Microphone output



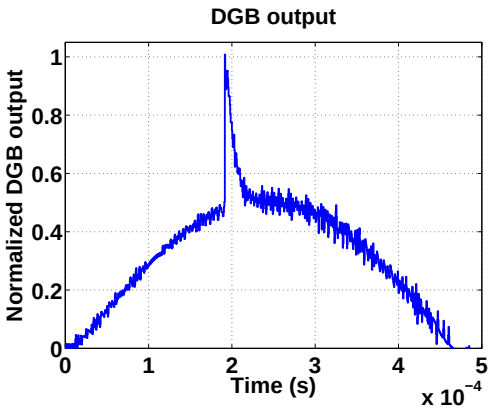
(b) VGA output



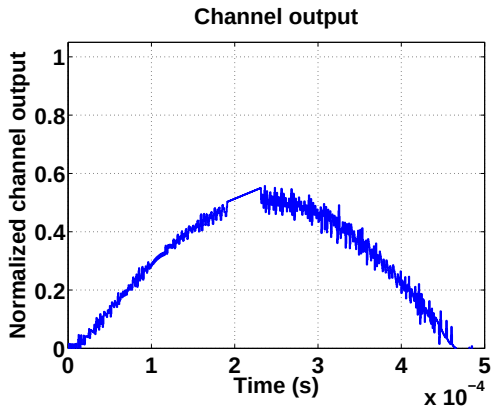
(c) AAF output



(d) LPF1 output



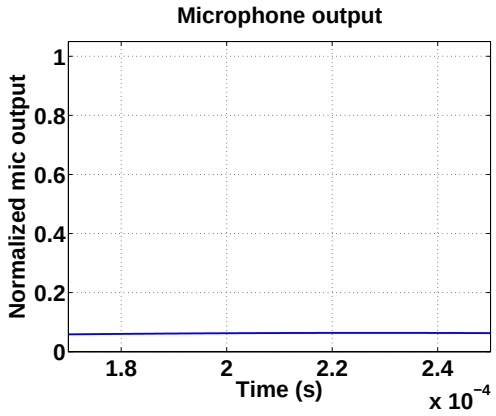
(e) Digital Gain Block output



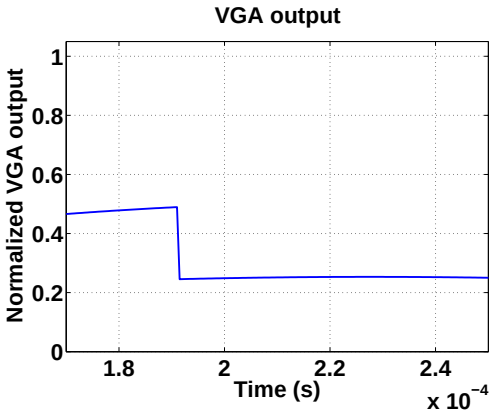
(f) Channel output

Figure 4.6: Signal along conversion channel for sine-wave input at 1.1 kHz

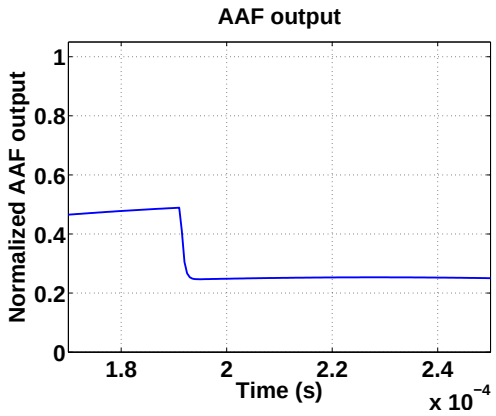
Finally for the *English Male Speech* sound sample, the output signal from the model without glitch reduction is shown in Fig. 4.10a. The glitches are not as clearly seen, due to the high frequency content of the signal. A glitch may be seen



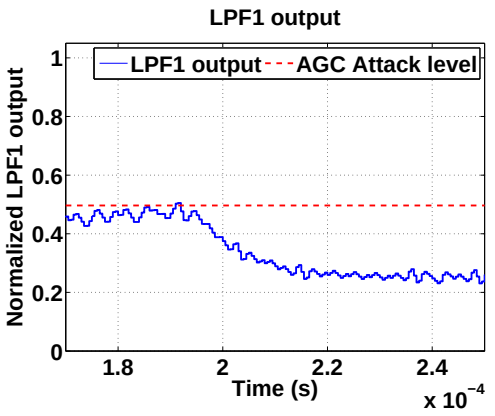
(a) Microphone output



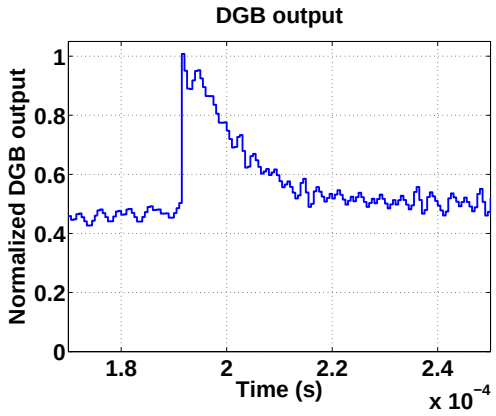
(b) VGA output



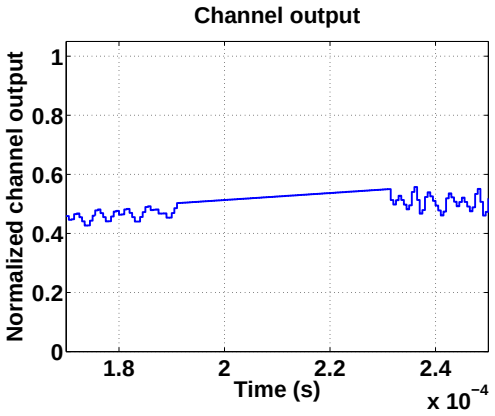
(c) AAF output



(d) LPF1 output

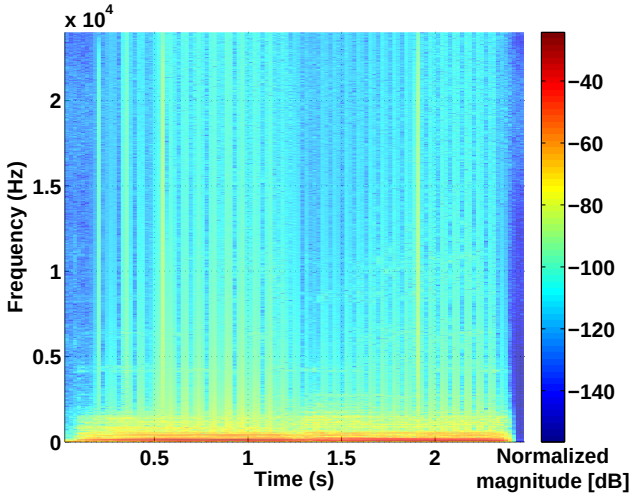


(e) Digital Gain Block output

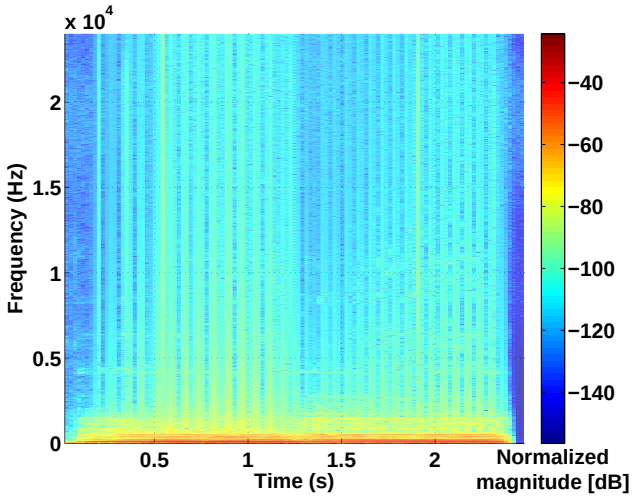


(f) Channel output

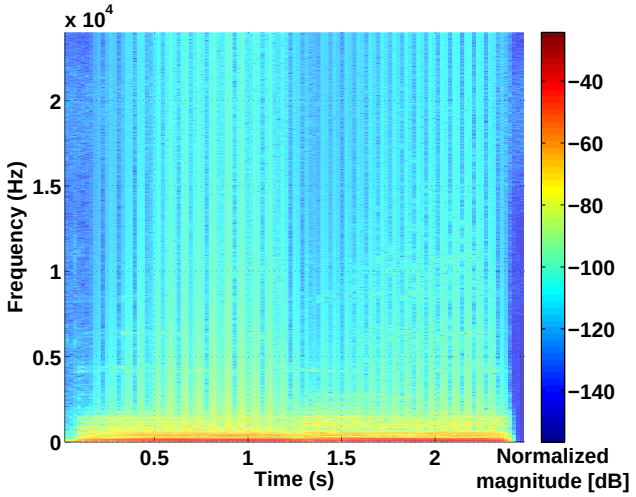
Figure 4.7: Signal along conversion channel for sine-wave input at 1.1 kHz, zoom in around gain transition event



(a) Without glitch reduction

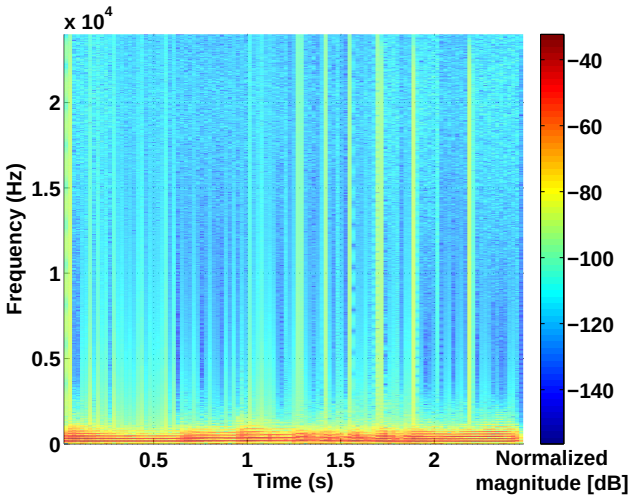


(b) With glitch reduction by digital gain delay

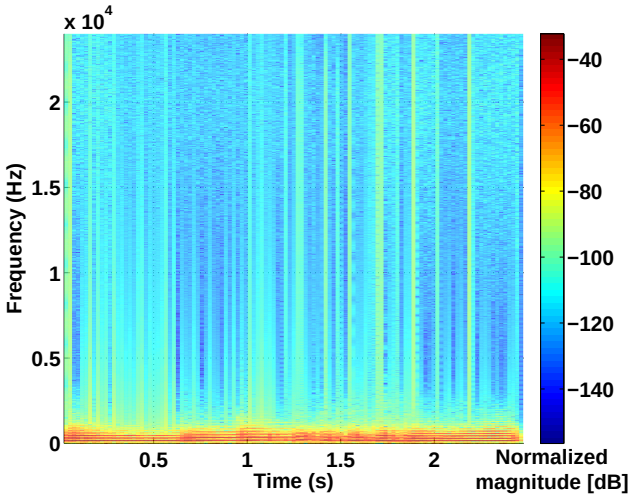


(c) With glitch reduction by output extrapolation

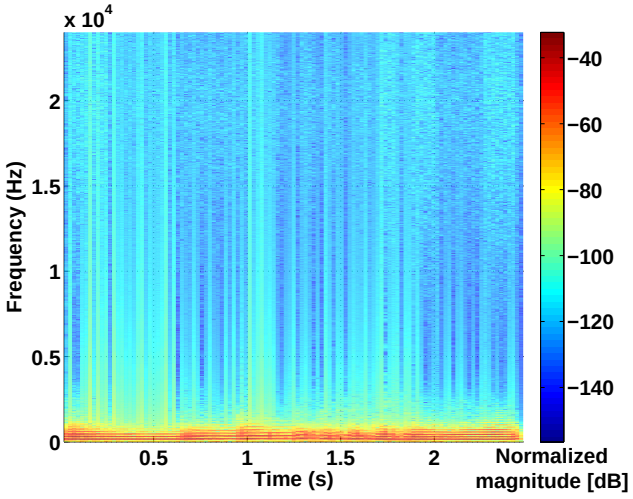
Figure 4.8: Spectrogram of *Double-Bass* sound sample



(a) Without glitch reduction

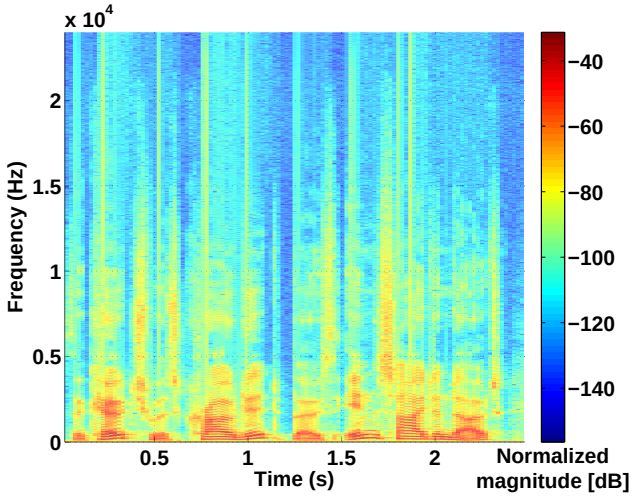


(b) With glitch reduction by digital gain delay

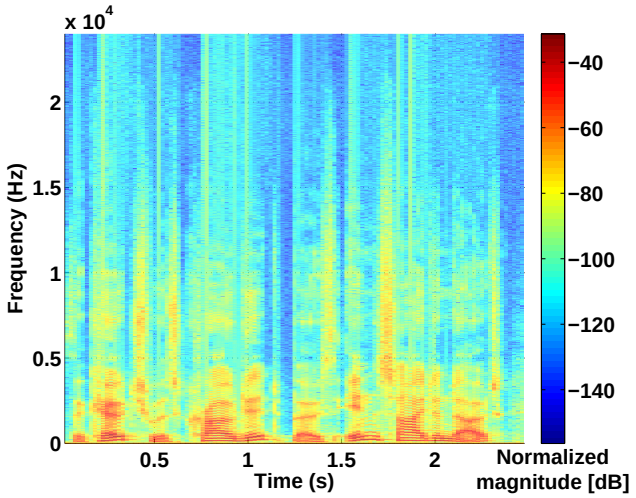


(c) With glitch reduction by output extrapolation

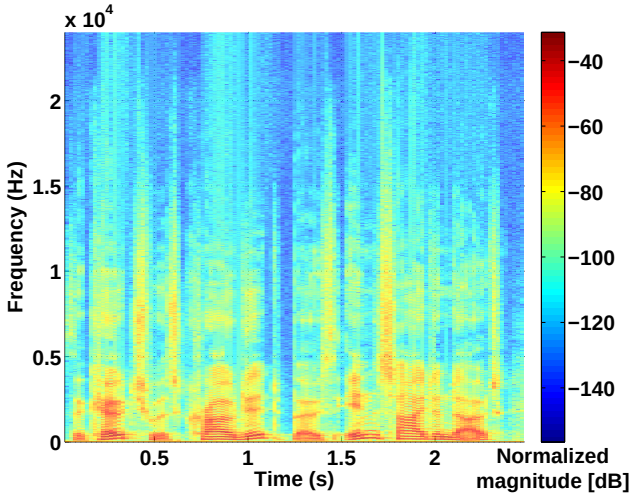
Figure 4.9: Spectrogram of *Tuba* sound sample



(a) Without glitch reduction



(b) With glitch reduction by digital gain delay



(c) With glitch reduction by output extrapolation

Figure 4.10: Spectrogram of *English Male Speech* sound sample

at $t \approx 0.75$ s. Once again comparing with the spectrogram of the output with the digital gain delay method and the output with the linear extrapolation method, in Fig. 4.9b and Fig. 4.9c respectively, it can be seen that the linear extrapolation method successfully reduces the transient glitches; however, for this sound sample it is more difficult to observe this from the spectrograms.

4.8 Audibility of Reduced Glitches

Based on the spectrograms of the sound samples processed by the model of the conversion channel, it could be seen that the output extrapolation method effectively reduces the transient glitches. However as discussed in Chap. 3, it is necessary to also evaluate the audibility of the error signal generated by the glitch reduction method. For this evaluation, the objective method proposed in Chap. 3 was used. Furthermore a listening test was also performed, to evaluate if the glitches were audible or not.

Note that the listening test performed here was not formalized like the listening tests described in Chap. 3. Due to a lack of time in the project, a formalized listening test was not carried out. However, in order to not rely fully on the objective method, a simple listening test was carried out, simply to validate the results of the objective method.

The output samples from the model were processed using the FFT based PEAQ implementation [44], and the outputs from the ADB and MFPD MOVs were extracted. The results are summarized in Table 4.2, showing the ADC and MFPD scores for the three sound samples processed by the conversion channel model without glitch reduction; with glitch reduction by digital gain delay; and with glitch reduction by output extrapolation. The results of the simple listening test are also listed, identifying whether the glitches were audible or not.

In Sec. 3.7 it was found that the detection threshold from the listening tests equaled an ADB score in the range from 1 to 1.5. With these ranges in mind, it is seen from the results in Table 4.2, that without glitch reduction, the glitches were audible in all three sound samples. This was confirmed by the listening test. When applying the glitch reduction method by digital gain delay, the glitches are only inaudible for the *English Male Speech* sound sample. This was also confirmed by the listening test. Finally the glitch reduction by output extrapolation successfully reduces the glitches below the detection threshold, as also verified by the listening test.

For the MFPD MOV is was found in Sec. 3.7, that the detection threshold equaled a MFPD score between 0.1 and 0.2. The MFPD results in Table 4.2 for the *English Male Speech* shows the almost the same score both with and without glitch reduction, thus no improvement is observed. This is contrary to the results from the simple listening test and the ADB, both showing an improvement when applying the glitch reduction methods. The results for the MFPD thus cast doubt on the applicability of the MFPD as an objective measure of the audibility of the

Table 4.2: Summary of results from evaluation of audibility of transient glitches, when applying glitch reduction methods

	Double-Bass	***Tuba***	***English Male Speech***
No glitch reduction			
ADB	2.68	2.88	2.04
MFPD	0.46	0.71	0.57
Listening test	Audible	Audible	Audible
Glitch reduction by digital gain delay			
ADB	2.18	2.52	1.41
MFPD	0.27	0.46	0.57
Listening test	Audible	Audible	Not audible
Glitch reduction by output extrapolation			
ADB	1.43	1.39	1.31
MFPD	0.10	0.15	0.54
Listening test	Not audible	Not audible	Not audible

transient glitches.

Another important observation from the results is, that none of the sound samples achieved an ADB and MFPD score of zero. As discussed in Sec. 3.8 this score should be achieved in case no glitches are audible. This observation in combination with the unexpected results from the MFPD MOV clearly identifies, that further investigation is needed on the topic of objective evaluation of the audibility of the transient glitches.

4.9 Summary

The main problem of the adaptive A/D conversion channel is the generation of transient glitches during a gain change event. When using the conversion channel for audio processing, the glitches are audible as ”clicks” and are generally unwanted. Thus, it is necessary to reduce the glitches to a point where they are no longer audible.

In this chapter a method has been presented for removing the glitches from the conversion channel output, by estimating the signal output using linear extrapolation. The extrapolation is based on the slope of the signal prior to the glitch event, and the slope is continuously estimated while there are no gain changes occurring. Since the estimate is a linear extrapolation, the transient glitch is replaced by another error. Although this glitch reduction method replaces one error signal with another, what is important is whether the new error is audible or not.

Based on a high-level model of an adaptive A/D conversion channel for audio, sound samples were processed and subsequently evaluated. Based on inspection of the spectrogram of the output samples, it was found that the glitches were

successfully removed, and the new error was not visible in the frequency domain. Furthermore, from the evaluation of the processed sound samples using the ADB MOV from the PEAQ method, and from simplified listening tests, the same results were achieved.

These preliminary evaluations of the method showed good results. More thorough evaluations are necessary, preferably in the form of standardized listening tests. Furthermore, the glitch reduction method needs to be implemented in a real adaptive A/D conversion channel, to fully evaluate the audibility of the errors generated by the method.

The ability of the glitch reduction method by output extrapolation to remove the audible glitches from the output of the conversion channel is an important result. As discussed in Chap. 2, one of the main problems of the single-channel version of the adaptive A/D conversion channel is the generation of glitches. With the glitches effectively being removed, it is possible to use large gain steps in the AGC. Furthermore, the problem of false-positive gain changes are less of a concern, as a gain change no longer generates an audible glitch. The channel noise will be increased unnecessarily when reducing the VGA gain without it being necessary, but this may not be a significant problem. The removal of the transient glitches also simplifies the design of the VGA, as larger gain steps results in fewer gain levels for the VGA. The preferred gain steps, from a digital point of view, in power of 2, are thus also realizable. The implementation of the digital gain block is also simplified.

The cost of applying the extrapolation method is an increase in the digital circuit part, as an additional averaging filter is required, and is also an accumulator for generating the linear output estimate. This will result in an increase of the total current consumption of the system, but with the additional blocks being digital, both the increase in area and current consumption can be kept low.

5

Optimum Design of Continuous-Time $\Delta\Sigma$ ADC

This chapter presents an method for optimizing the design of a Continuous-Time $\Delta\Sigma$ ADC for minimum current consumption. Based on the observation that modulator design, including the corner frequency of the noise transfer function and the number of quantization levels, has a direct impact on the circuit level implementation of the loopfilter, an analysis is carried out for an active-RC integrator used as the 1st integrator of the loopfilter. This with aim of finding expression for estimating the necessary integrator OTA bias current for achieving a given performance by the continuous-time $\Delta\Sigma$ ADC. By designing a large set of modulators, the current consumption of the related circuits can be estimated, and the minimum current solution may be determined. A design example is given for the design of a 3rd order continuous-time $\Delta\Sigma$ ADC, and from simulations the performance is compared with the estimated values, showing that the estimated current consumption is optimistic. Taking the circuit level implementation into account when designing the modulator an then comparing a large set of designs, simplifies the process of achieving a minimum current solution; thus, it is considered an important contribution of this project. The chapter is based on the NORCHIP 2014 paper, App. C

5.1 $\Delta\Sigma$ Modulator Basics

The ADC is the core of the A/D conversion channel, as it is essential for converting the processed signal from the analog to the digital domain. For audio signals the $\Delta\Sigma$ ADC is the common choice, as oversampling and noise shaping attenuates the quantization noise, and thereby achieving a high SNR. In comparison to Nyquist rate ADCs, the resolution of the $\Delta\Sigma$ ADC is not limited by matching of circuit components. The loopfilter noise shapes non-idealities generated inside the loop, thus attenuating both circuit noise, distortion, and DC offsets. Furthermore, the quantization can be realized using a single comparator, generating a single-

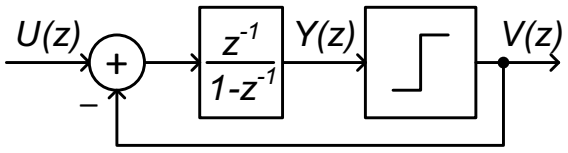


Figure 5.1: 1st order discrete-time ΔΣ modulator

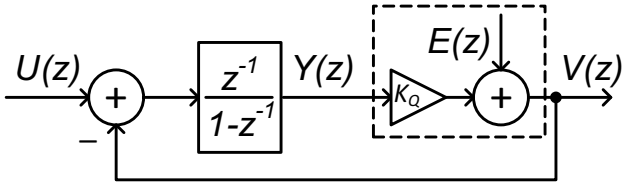


Figure 5.2: Linearized model of 1st order ΔΣ modulator

bit output stream, classified as a pulse density modulated (PDM) signal. The challenge when designing the ΔΣ ADC is thus shifted from the quantizer to the loopfilter.

In Fig. 5.1 is shown the simplest discrete-time (DT) ΔΣ modulator: a 1st order loopfilter with a single-bit quantizer. As seen from the figure the modulator is a feedback system, where the single-bit output signal is subtracted from the input, and the result is integrated and quantized. To analyze the modulator it is convenient to use a linear model of the system, as shown in Fig. 5.2, where the quantizer is replaced by a quantizer gain, K_Q, and an error signal, $E(z)$. Generally, the value of K_Q depends on the signal level, but in the case of the single-bit quantizer, the quantizer is a single comparator that determines whether the input signal is above or below a reference common-mode level. It is thus the sign of the signal that matters and not the signal level. Thus, K_Q may be ignored. From Fig. 5.2, the output, $V(z)$, can be expressed as:

$$V(z) = Y(z) + E(z) = \frac{z^{-1}}{1 - z^{-1}} \left(U(z) - V(z)\right) + E(z) \tag{5.1}$$

$$\Leftrightarrow V(z) = z^{-1}U(z) + \left(1 - z^{-1}\right) E(z) \tag{5.2}$$

From (5.2) it can be seen that the output is simply a delayed version of the input with an added error signal that is high-pass filtered. Generally, the transfer functions for the signal and the noise are defined as:

$$STF(z) = \frac{V(z)}{U(z)} \tag{5.3}$$

$$NTF(z) = \frac{V(z)}{E(z)} \tag{5.4}$$

where $STF(z)$ is the signal transfer function, and $NTF(z)$ is the noise transfer function. The NTF and STF of the 1st order modulator described by (5.2), are

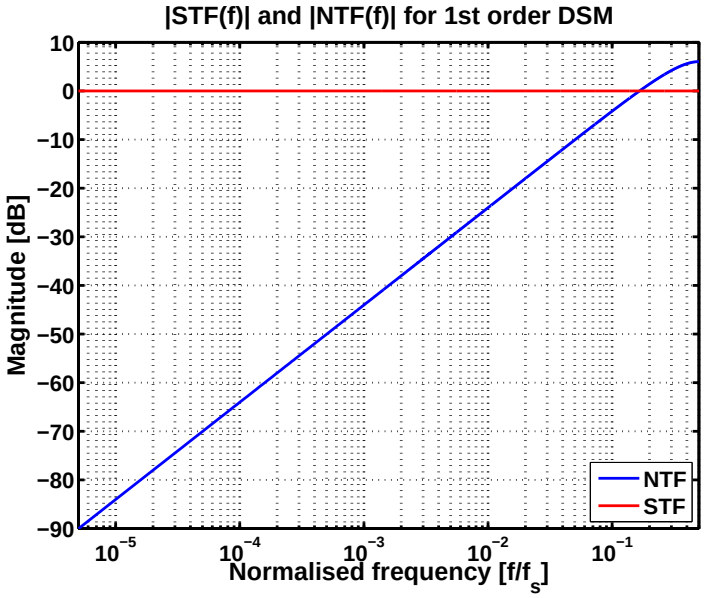


Figure 5.3: Magnitude response of NTF and STF for 1st order ΔΣ modulator

shown in Fig. 5.3. As seen from the figure, the NTF realizes a 1st order high-pass function and thus attenuates the noise $E(z)$ at low frequencies.

The order of the modulator may be increased by replacing the quantizer of the 1st order modulator by another 1st order modulator; thereby the loopfilter becomes a 2nd order loopfilter. This increases the slope of the NTF, thereby further attenuating the quantization noise.

For higher order modulators it is convenient to use a more generic model of the ΔΣ modulator. The block diagram of the generic discrete-time ΔΣ modulator shown in Fig. 5.4. From this figure, the output $V(z)$ may be expressed as:

$$V(z) = L_0(z)U(z) + L_1(z)V(z) + E(z) \tag{5.5}$$

$$\Leftrightarrow V(z) = \frac{L_0(z)}{1 - L_1(z)}U(z) + \frac{1}{1 - L_1(z)}E(z) \tag{5.6}$$

The resulting expression for the STF and NTF are:

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} \tag{5.7}$$

$$NTF(z) = \frac{1}{1 - L_1(z)} \tag{5.8}$$

The magnitude responses shown in Fig. 5.3 are in the discrete-time domain, as the ADC performs sampling of the input signal. When sampling the input signal, the frequencies of the input signal are mapped to a relative frequency that is

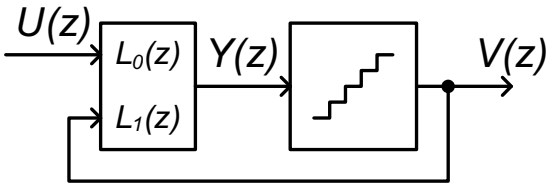


Figure 5.4: Block diagram of generic ΔΣ modulator

relative to the sampling frequency, f_s. In Fig. 5.3 the smaller the signal band, the lower the quantization noise in power in that frequency band. This is a general property of oversampling, and this property of the converter is given from the oversampling ratio (OSR):

$$OSR = \frac{f_s}{2f_B} \tag{5.9}$$

Thus, a larger OSR results in a larger attenuation of the quantization noise in the signal band of interest.

A more detailed introduction to the topic of ΔΣ modulators is given in [19].

5.2 Modulator Design

When designing the ΔΣ modulator, the primary focus is achieving a sufficient attenuation of the quantization noise. Generally, the quantization noise may be reduced by:

- Increasing the oversampling ratio of the modulator
- Increasing the loopfilter order
- Increasing the corner frequency of the NTF
- Increasing the number of quantization levels
- Selection of loopfilter topology

5.2.1 Oversampling Ratio

Increasing the oversampling ratio of the modulator, reduces the amount of noise power in the band of interest. With the signal band typically being fixed for a given application, a larger OSR requires that the sampling frequency is increased. In a discrete time modulator, the increase of f_s does not change the loopfilter of the modulator, but only the mapping of the signal band of interest to the relative frequency band in the discrete-time domain.

From a circuit point of view, the increased sampling frequency requires the circuit blocks to operate at a higher speed, which increases the current consumption. Thus, for achieving a minimum current consumption, the OSR should be minimized within the acceptable noise limits.

5.2.2 Loopfilter Order

When increasing the loopfilter order, more integrators are required in the modulator. A larger number of integrators results in a larger number of active circuit blocks all consuming current. From a current consumption point of view, it is therefore preferred to minimize the loopfilter order.

Increasing the loopfilter order also affects the stability of the modulator. Generally, the stability of the modulator relates to the maximum input signal that the modulator is able to handle, without the integrator outputs saturating. If the input to the modulator is larger than the maximum feedback signal, then the output of the 1st integrator will ideally increase infinitely. In a real integrator the integrator output will saturate at the supply rails. Thus, the quantizer input is saturated, and the modulator becomes unstable.

Generally, the 1st and 2nd order modulator are considered stable for full-scale input signals, but for higher order modulators the behavior of the modulator becomes more chaotic [48]. To characterize the stability of a $\Delta\Sigma$ modulator, the maximum stable amplitude (MSA) is used. In [48, 49] is shown for the single-bit modulator how the MSA may be determined analytically for a specific loopfilter. The analysis is based on the fact, that the quantizer K_Q depends on the amplitude of the input signal.

For a modulator applying multi-level quantization, the quantizer gain is fixed for large input signals, since the multiple levels makes it possible to define an exact relation between the input signal and the output signal. Because of the more complex nature of K_Q in a multi-level quantizer, it is not possible to apply the same method for analytically determining the MSA, as for the single-bit quantizer. In [50] is presented an alternative model, that tries to analytically determine the MSA of multi-level quantizers. However, the method only appears to be applicable for modulator orders larger than 3 and with 5 quantization levels or more. The reference method for evaluating the MSA is by simulation, where the input signal level is swept. From this it is then possible to determine at which input signal level that the modulator becomes unstable.

5.2.3 NTF Corner Frequency

By increasing the corner frequency of the NTF, the quantization noise is attenuated more in the signal band. However, this has the unwanted property of also increasing the out-of-band noise gain, thereby increasing the overall noise power in the signal processed by the loopfilter. This may lead to saturation of the in-

tegrators, and thereby causing the modulator to become unstable. In essence this may be seen by the MSA of the modulator decreasing when the NTF corner frequency is increased.

5.2.4 Quantization Levels

The quantization noise in the modulator is noise-shaped by the loopfilter, thus allowing for the use of a single-bit quantizer while still achieving a high SNR. The quantization noise power, P_Q, may generally be expressed as [51]:

$$\Delta = \frac{V_{ref}}{N} \tag{5.10}$$

$$P_Q = \frac{\Delta^2}{12} = \frac{V_{ref}^2}{12 \cdot N^2} \tag{5.11}$$

where V_{ref} is the reference voltage of the quantizer, and N is the number of quantization levels. From (5.11) it is given, that by increasing the number of quantization levels the quantization noise is reduced. Increasing the number of quantization levels also has the property that the quantization process is more linear, which stabilizes the modulator. Thus, for a specific NFT with a given corner frequency, a larger MSA may be achieved by using multi-level quantization in comparison to single-bit quantization.

A problem with an increased number of quantization levels is, that the feedback DAC used in the feedback path also requires more output levels. In contrast to the quantizer, the single-bit DAC is inherently linear, as the gain curve of the DAC is between two fixed output levels. When increasing the number of output levels, the DAC is thus no longer guaranteed to be linear. This in turn may lead to harmonic distortion components being injected from the DAC to the input of the modulator. As with any signal at the input, the distortion components are not attenuated by the NTF but are processed by the STF. Thus, the non-linearity of the feedback DAC may be of concern when using multi-level quantization.

Finally, the additional quantization levels requires more comparators in the quantizer, thereby increasing the current consumption of this block.

5.2.5 Loopfilter Topology

The loopfilter may be realized by different topologies, that can be categorized as:

- Feedback or feedforward based
- Integrator or resonator based

The feedback based, or cascade-of-integrators-with-feedback (CIFB) topology is shown in Fig. 5.5 for a 2nd order discrete-time modulator. The CIFB topology has

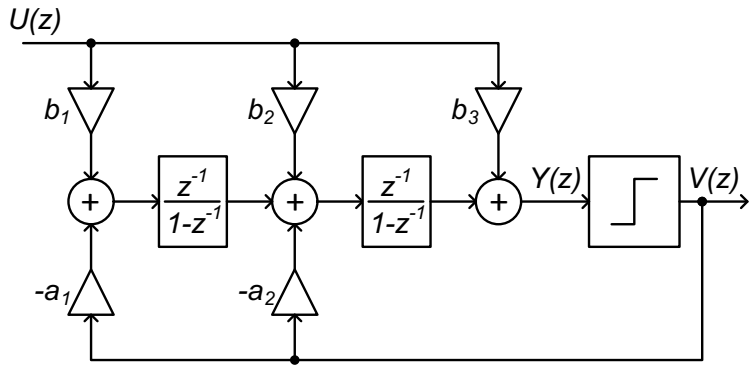


Figure 5.5: CIFB topology for 2nd order modulator

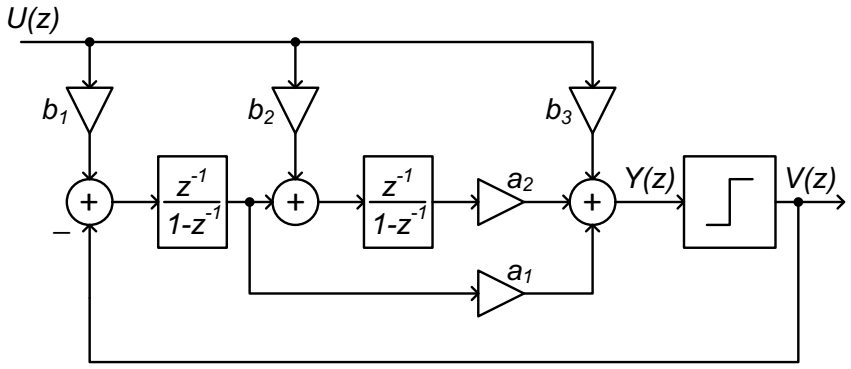


Figure 5.6: CIFF topology for 2nd order modulator

a feedback path from the quantizer output to the input of each integrator. The feedforward based, or cascade-of-integrators-with-feedforward (CIFF), topology is shown in Fig. 5.6 for a 2nd order modulator. For CIFF only a single feedback path is used from the quantizer output to the input of the 1st integrator. Thereby only a single DAC is needed when realizing the modulator. Instead a summing circuit is required in front of the quantizer. In Fig. 5.5 is appears that a summing circuit is also needed in front of the quantizer, but this depends on the STF that is to be realized. The summing circuit is thus not required in a CIFB toplogy while it is in the CIFF topology.

When realizing the loopfilter using integrators, the zeros of the NTF are all placed at DC. Instead of integrators one may use resonators in the loopfilter, to add a degree of freedom with respect to the placement of the loopfilter poles. By optimal placement of the NTF zeros, it is possible to further reduce the quantization noise power [52]. The cascade-of-resonators-with-feedback (CRFB) topology is shown in Fig. 5.7, where a feedback path around the integrators have been added to form a resonator.

5.2.6 Modulator Summary

Overall the modulator may be optimized for a low current implementation, by considering all five properties. Multi-level quantization is in particular of interest.

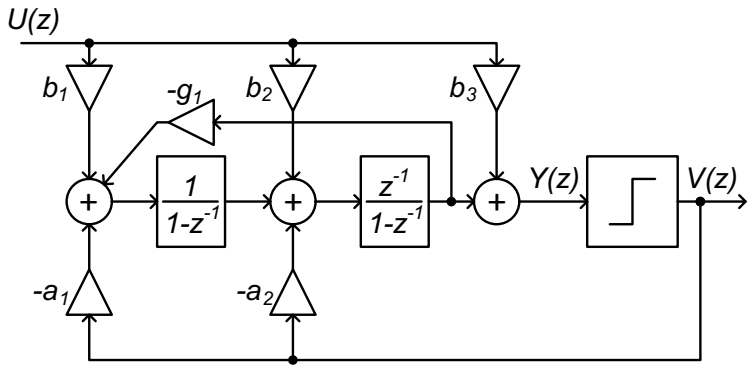


Figure 5.7: CRFB topology for 2nd order modulator

By using a multi-level quantizer it is possible to use a higher order loopfilter, without reducing the MSA. Similarly, the NTF corner frequency may be increased. By using multi-level quantization, it may also be possible to use a lower order loopfilter due to the reduced quantization noise, thereby further improving the stability of the modulator. This also reduces the number of integrators and thereby the current consumption. Similarly, the OSR may be increased, in order to use a lower order loopfilter.

5.3 Continuous-Time ΔΣ ADC

When implement a ΔΣ ADC this may be done either using discrete-time or continuous-time (CT) circuits. The DT is commonly implemented using switched-capacitor circuits, but alternative solutions using switched currents have been reported [49]. Overall, the loopfilter is realized as a sampled system, thereby sampling the signal at the input of the modulator. In order to avoid aliasing in the sampled signal, it is necessary to precede the DT ΔΣ ADC by an anti-aliasing filter. Furthermore, since the input and feedback signals are steps, the integrator outputs need to settle with a single sampling period. The switched capacitor integrator there requires high speed operational transconductance amplifiers (OTA) , with a gain-bandwidth product upto 10 times the modulator sampling frequency [53]. The benefit of the DT implementation is the ability of precisely realizing the coefficients of the loopfilter as a ratio of capacitances. For analog integrated circuits (IC) this is an important property, as the absolute values of components in an IC may vary upto 20 % while the relative value of two identical components may vary as little as 0.1 %. Furthermore, since the loopfilter is realized using switched-capacitor integrators that samples the signals, the integration is not continuous in time. As a result, the DT modulator has a low sensitivity to both clock jitter and delay in the feedback loop.

In the CT implementation of the ΔΣ modulator, the integrators are realized using continuous-time filters. CT filters are dependent on the absolute component values, thus making the implementation of the loopfilter coefficients challenging due to process variations. Another problem is that the integration of the signals

Table 5.1: Overview of advantages of CT and DT implementations of ΔΣ ADCs

Advantages of CT	Advantages of DT
Lower speed requirements of integrators	Coefficients rely on relative matching
High f_s possible	Low sensitivity to clock jitter
Sampling errors are noise shaped	Low sensitivity to loop delay
Inherent AA filter	Only signal value at sampling instance is important

in the loopfilter is continuous in time, resulting in the modulator being sensitive to clock jitter and loop delay. However, the continuous-time operation of the modulator reduces the speed requirements of the integrator circuits; the gain-bandwidth product (GBW) of the OTAs used in active-RC integrators may be as low as two times f_s [22]. This relaxed GBW requirement may be used for increasing the sampling frequency of the modulator. Another big advantage is the placement of the sampling process, as this occurs at the input of the quantizer rather than at the input of the modulator. The errors generated in the sampling process are thus attenuated by the loopfilter similarly to the quantization noise. Furthermore, the placement of the sampler results in the STF of the modulator acting as a prefilter, thus possibly removing the requirement of a AAF in front of the ADC. The pros and cons of the DT and CT modulator implementations are summarized in Table 5.1.

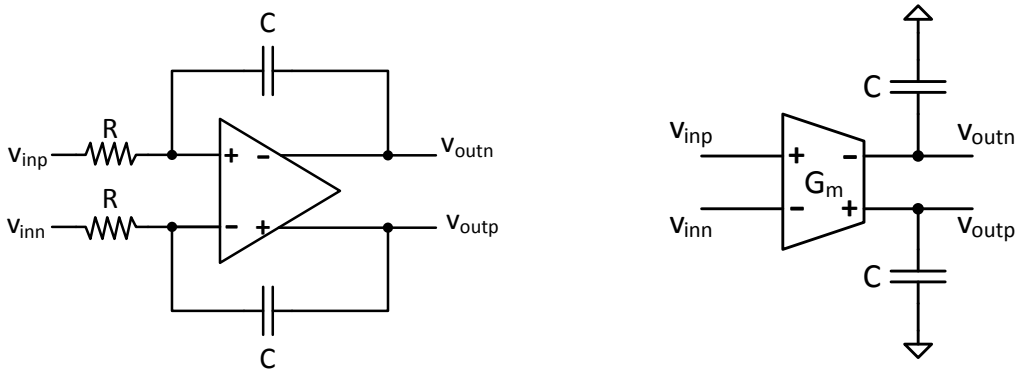
From audio applications, the sampling frequency of the ΔΣ modulator may be kept fairly low, in the range of MHz. Because of this, the DT modulators have been the dominant in the past. With the loopfilter being dependent on the ratio of capacitor values, it is possible to achieve high SNR ΔΣ ADCs for audio [54–58].

In the past 20 years there has been an increased focus on the CT implementations, due to the possible reduced current consumption in comparison to the DT equivalent [10, 59–61]. The low current consumption primarily follows from the reduced speed requirements of the integrators. Significant research has been carried out by S. Pavan to analyze and solve many of the issues in CT ΔΣ ADCs [62–67]. An overview of ΔΣ ADCs is given in [18], showing that CT ΔΣ ADC for audio that achieve an SNR of 94 dB while achieving a Figure-of-Merit (FoM) as low as 50 fJ/conversion [65]. The FoM is given as:

$$FoM = \frac{P_{mod}}{2^{ENOB} \cdot 2f_B} \tag{5.12}$$

where P_{mod} is the power consumption of the ΔΣ modulator, and $ENOB$ is the effective-number-of-bits of the modulator. For DT modulators, a similar FoM was achieved but only with a SNR of 83 dB [68].

As described in Chap. 2, for the adaptive A/D conversion channel an ADC with a high dynamic range is not needed to achieve a high dynamic range in the conversion channel. For the adaptive A/D conversion channel, the CT ΔΣ ADC is a good choice, as a sufficiently good dynamic range may be achieved, in the



(a) Active-RC integrator **(b)** Gm-C integrator

Figure 5.8: CT integrator topologies

order of 90 dB, while achieving a low current consumption.

In the following subsections, a brief overview of the relevant considerations when designing CT ΔΣ ADCs are presented.

5.3.1 Integrator Topology

In CT ΔΣ modulators the integrators may be realized in several ways. The main integrator topologies are the active-RC integrator and the Gm-C integrator, both shown in Fig. 5.8. The primary difference is in the application of feedback in the active-RC integrator; the feedback linearizes the operation of the OTA, thereby reducing the harmonic distortion. Due to the lack of feedback, the Gm-C integrator is faster but also highly non-linear. The Gm-C integrator may achieve a THD in the range of 1% while the active-RC integrator can achieve a THD in the range of 0.01% [22]. For audio applications the THD is an important performance parameter and 1% is not acceptable performance. Thus, the active-RC integrator is the preferred integrator topology for audio CT ΔΣ ADCs.

For the active-RC integrator, the loopfilter coefficients relate to the integrator resistor and capacitor by:

$$k_i = \frac{1}{f_s R_i C} \tag{5.13}$$

where k_i is the *ith* CT coefficient, f_s is the sampling frequency, and R and C are the integrator resistor and capacitor respectively.

5.3.2 Feedback DAC

The design of the feedback DAC is more complex in a CT ΔΣ ADC in comparison to the DT equivalent. The DAC converts the modulator output signal from a discrete-time and discrete-value signal, to a continuous-time and continuous-value signal. since the DAC output signal is continuously integrated, any errors in time are integrated as well and will reduce the ADC performance.

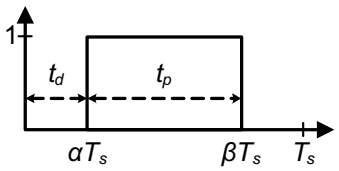


Figure 5.9: Generic rectangular feedback DAC waveform

Although the signal is integrated continuously, it is the signal value at the sampling instance at the input of the quantizer, that is important. Thus, the DAC feedback waveform can take any shape, as long as the integrated feedback signal results in the same value. The simplest waveform is the non-return-to-zero (NRZ), where the duration of the feedback pulse equals the sampling period. The alternative is the return-to-zero (RZ), where the duration of the feedback pulse is smaller than the sampling period.

To describe the rectangular waveforms, one may define the beginning and the end of the signal with respect to the sampling period. The generic rectangular feedback waveform is shown in Fig. 5.9, and from this the factors α and β may be defined as:

$$\alpha = \frac{t_d}{T_s} \tag{5.14}$$

$$\beta = \frac{t_d + t_p}{T_s} \tag{5.15}$$

where t_d is the time-delay of the waveform, t_p is the duration of the pulse, and T_s is the sampling period. From Fig. 5.9, (5.14) and (5.15) it is given that the NRZ waveform is a special case of the RZ waveform, as for an ideal NRZ waveform $\{\alpha, \beta\} = \{0, 1\}$.

The two waveform types have different properties with respect to timing related non-idealities of the modulator. Clock jitter results in uncertainty in the time instance of sampling, resulting in a variation of the duration of the sampling period, and thereby width of the feedback pulse; this causes an error in the integrated value. The RZ waveform is more sensitive to clock jitter, since this waveform always has a rising and a falling edge during a single sampling period, independent of the value before and after. This is in contrast to the NRZ, where the number of edges depends on the previous and past value. Consider the case of an output stream of continuous 1's. Then for the NRZ waveform there are no edges in each sampling period, while for the RZ there are always two.

When increasing the number of quantization levels in the modulator, the jitter sensitivity is reduced for the NRZ waveform [22, 69]. This follows, as the output of the modulator tries to resemble the input signal. Thus, for a sine-wave input signal, the consecutive output of multi-level modulator will generally vary by a single level. With each change in value being smaller for increasing number of levels, the error in the integrated value will be reduced; this is not the case for the RZ waveform. Thus, from a clock jitter point of view, the NRZ is the preferred waveform.

Table 5.2: Overview of pros and cons of RZ and NRZ feedback DAC waveforms

Property	**RZ**	**NRZ**
Clock jitter sensitivity	-	+
Excees loop delay sensitivity	+	-
Intersymbol interference sensitivity	+	-

Another non-ideality is excess loop delay, which relates to the delay from the output of the quantizer to the input of the quantizer. Since this delay is non-zero, the feedback pulse will be slightly delayed, $t_d \neq 0$. For the NRZ waveform, this results in the pulse being partly shifted into the following sampling period. As shown in [70], the delay of the NRZ pulse may be represented by a RZ pulse with $\{\alpha = t_d, \beta = 1\}$ in the sampling period and a RZ pulse with $\{\alpha = 0, \beta = t_d\}$ in the following period. This results in the modulator order increasing, which reduces the MSA and may causing the modulator to be unstable. For the RZ waveform, if $t_d \leq (1 - \beta)T_s$ the excess loop delay is not a problem, as the pulse is only time-shifted within the same sampling period. However, if the pulse is delayed by a larger amount, the result is the same as for the NRZ waveform.

Finally, the DAC has a limited output slew-rate, thus limiting the rise and fall time of the feedback pulses; this causes an error in the integrated feedback signal. In case the rise and fall time are not identical, then for the NRZ waveform this results in the integrated error being dependent on the modulator output stream; this will generate unwanted tones in the output spectrum [71]. For the RZ waveform the error generated is the same in each period, as there is always a rising and a falling edge in each pulse; thus no tones but only noise is generated. However, intersymbol interference may be reduced by implementing the modulator using fully-differential circuits.

A summary of the advantages and disadvantages of the RZ and NRZ feedback waveforms is given in Table 5.2. Other waveforms exist, including the exponential shaped curves. This waveform has a significantly lower sensitivity to clock jitter, equivalent to that of DT ΔΣ modulators [72–75]. This follows since the feedback signal mimics that of the DT ΔΣ ADC, with the majority of the charge transfer from the DAC to or from the integration capacitors takes place in the initial part of the pulse. A variation in the duration of the pulse due to clock jitter thus has a limited effect on the feedback signal, thereby reducing the resulting error and the sensitivity to clock jitter.

5.4 Optimum Design of Modulator and Circuits

As described in the previous section, there is a large set of design choices when designing a CT ΔΣ ADC. Due to the large design space, a structured approach to the design is necessary in order to achieve a high performing circuit with low current consumption. In the literature different design approaches have been presented based on different aspects of the modulator design. In [60] is presented a

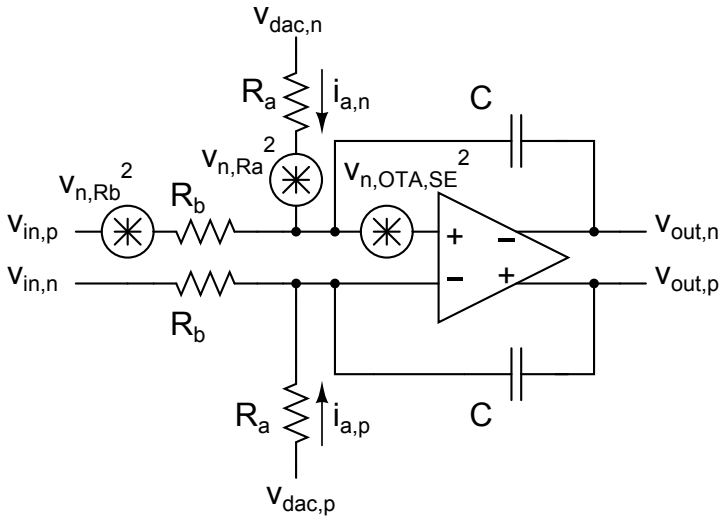


Figure 5.10: Fully differential active-RC integrator with single-ended noise sources

power optimized CT $\Delta\Sigma$ ADC for audio applications, where general modulator choices are discussed while focusing the optimization on the circuit level implementation. In [22, 76] is presented a FoM based method that based on circuit analysis and the modulator OSR determines the minimum FoM that may be achieved. This method is interesting, as it combines the modulator design with the circuit design in order to achieve the optimum solution. However, part of the noise analysis is simplified.

Based on the idea behind the method in [22, 76], it is possible to achieve a low current CT $\Delta\Sigma$ modulator by taking both the modulator loopfilter and the circuit realization into account. The 1st integrator of the loopfilter is the most critical, as all non-idealities referred to the input of this integrator are not noise shaped by the modulator. This integrator has the highest current consumption and thus the focus of the optimization.

For audio applications the active-RC integrator is the preferred choice, due to the low harmonic distortion. In Fig. 5.10 is shown the schematic for the active-RC integrator when used as the 1st integrator in a CT $\Delta\Sigma$ ADC. For this integrator topology, a given filter coefficient is realized from the selection of the integration resistor and capacitor. For reference, (5.13) is repeated here, describing the relation between the loopfilter coefficient, the integrator components, and the sampling frequency:

$$k_i = \frac{1}{f_s R_i C} \tag{5.16}$$

As shown in Fig. 5.10 the same integrator realizes two coefficients; the input coefficient, k_{b1}, and the feedback coefficient, k_{a1}. Each coefficient requires a separate resistor, but shares the capacitor. Because of this restriction, it is not possible to arbitrarily select a resistor and capacitor value for each coefficient. Once the capacitance has been selected for one coefficient, the resistor for the other coefficient is implicitly determined.

From (5.16) for a given sampling frequency and coefficient value, the RC product is fixed, but the value of either R or C may be selected arbitrarily. Considering the input resistor in Fig. 5.10, R_b, the thermal noise of this resistor is directly present at the input of the integrator. Thus, from a noise perspective the value of R_b should be small. This has the added benefit, that by reducing the resistor noise, the integrator OTA noise may be increased and allowing a reduction of the OTA biasing current. However, by reducing the resistance the currents sourced from the modulator input and the feedback DAC are increased. When considering the GBW and the slew rate (SR) of the OTA, it is preferred that the integration capacitance is small, as this minimizes the capacitive load on the OTA; thereby reducing the biasing current of the OTA. The question is then, whether a small integrator resistor or a small integrator capacitor should be used for realizing the input coefficient?

If the sampling frequency is not fixed, both R and C could be reduced while increasing f_s. However, this has the side-effect that the GBW requirement of the OTA is increased. Furthermore, the current consumption of the quantizer and any digital blocks will increase due to the higher sampling frequency.

Since the loopfilter coefficient has an impact on R and C of the integrator, the loopfilter design needs to be taken into account. This may be done by selecting the corner frequency of the NTF that maximizes the loopfilter coefficients. Another aspect of the loopfilter is the MSA, as this impacts the circuit noise requirements. For a given SNR, a lower MSA requires a reduction of the circuit noise. Thus, the MSA should maximized. In order to do this, the number of quantization levels may be increased, thereby making the quantization process more linear. In turn the current consumption of the quantizer is increased.

From these modulator and circuit considerations, it is evident that the design space is large, and for a given set of performance requirements an optimum low power design exists. With the modulator loopfilter affecting the circuit implementation, it may be possible to estimate the current consumption of a given loopfilter; this may be based on analytical expressions of the current consumption of the 1st integrator. Thereby different modulators may be compared and the minimum current design can be found.

5.4.1 Loopfilter Coefficients

As described, both the integrator resistor and capacitor should be minimized to minimize the current consumption of the OTA. Thus, from (5.16) the integrator coefficients should be maximized. Considering the CT ΔΣ modulator with a CIFB topology, as shown in Fig. 5.11, the NTF may be expressed as:

$$NTF(s) = \frac{1}{1 + \sum_{i=1}^{N} k_{ai} \cdot \left(\frac{f_s}{s}\right)^{N+1-i}} \tag{5.17}$$

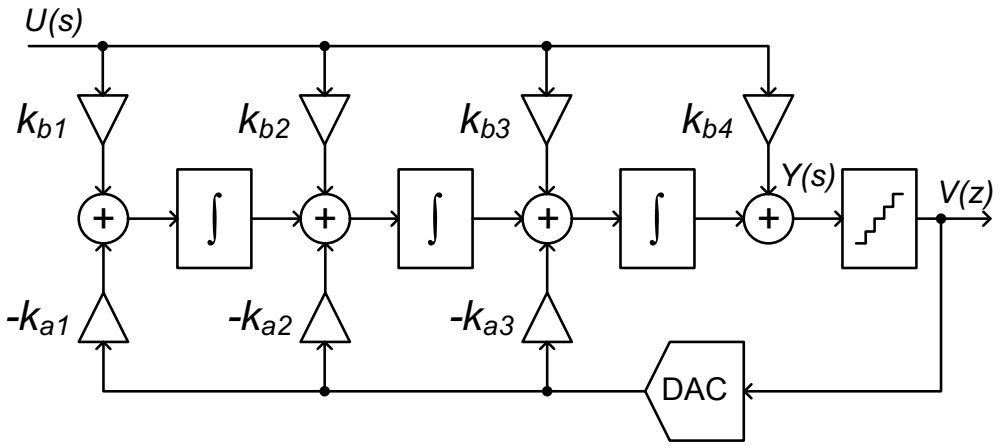


Figure 5.11: Block diagram of 3rd order CT ΔΣ ADC with CIFB topology

where N is the loopfilter order, and k_{ai} is the *ith* feedback coefficient. Similarly, the STF may be expressed as:

$$STF(s) = \frac{\sum_{i=1}^{N+1} k_{bi} \cdot \left(\frac{f_s}{s}\right)^{N+1-i}}{1 + \sum_{i=1}^{N} k_{ai} \cdot \left(\frac{f_s}{s}\right)^{N+1-i}} \tag{5.18}$$

where k_{bi} is the *ith* input coefficient. Assuming $OSR \gg 10$, the signal band of interest is close to $s = 0$. The signal gain in the modulator may thus be approximated as the DC gain of the STF:

$$|STF(0)| = \frac{k_{b1}}{k_{a1}} \tag{5.19}$$

For the NTF, in order to maximize the quantization noise attenuation in the signal band of interest, the expression for the NTF magnitude response may be determined for $s \to 0$:

$$\lim_{s \to 0} NTF(s) \approx \frac{1}{k_{a1}} \cdot \left(\frac{s}{f_s}\right)^N \tag{5.20}$$

From (5.20) it is given that the quantization noise is minimized at low frequencies by maximizing the feedback coefficient of the 1st integrator. It is known that by increasing the corner frequency of the NTF, the quantization noise is also minimized. From this observation, in order to minimize the RC product for the 1st integrator, the corner frequency of the NTF should be increased. With f_c also affecting the MSA, it is relevant to also include the NTF corner frequency when optimizing the modulator for low current consumption.

The loopfilter for the CT ΔΣ modulator may be designed either directly as a continuous-time filter with a given order and corner frequency. Alternatively a DT loopfilter may be designed and afterwards converted into the equivalent CT filter. From a simulation point-of-view it is preferred to design the modulator in the discrete-time domain, where it may easily be evaluated using numerical tools e.g. MATLAB. For a modulator, with a specific loopfilter and number of

quantization levels, the MSA may then be determined based on simulations. The DT loopfilter may be designed by using built-in filter functions in the MATLAB Signal Processing Toolbox.

The designed loopfilter can then be converted from the discrete-time domain to the continuous-time domain by applying the impulse-invariant transform [22, 70]. The method converts the DT filter into a CT equivalent, by making the CT filter generate the same signal value at the input of the quantizer the sampling instance. Thereby the same discrete time output of the modulator may be achieved.

5.4.2 Noise of Integrator

The input referred noise of the fully differential integrator in Fig. 5.10 may be determined by analyzing the differential half-circuit. The input referred noise power of the positive half-circuit is multiplied by a factor of two to get the differential noise power at the integrator input; this follows as the noise of the two half-circuits is uncorrelated. The noise of the integrator may be split into two parts: one for the resistor power and another for the OTA noise power.

5.4.2.1 Resistor Noise

The thermal noise from the resistors R_a and R_b is given as [77]:

$$v_{n,Ri}^2 = 4kTR_i f_B \tag{5.21}$$

where k is the Boltzman constant, T is the absolute temperature, R_i is the resistance of the specific resistor, and f_B is the frequency band of interest. From Fig. 5.10, the total input referred noise from the resistors R_a and R_b is given as:

$$v_{\text{IRN},R}^2 = 2\left(v_{n,Rb}^2 + \left(\frac{R_b}{R_a}\right)^2 v_{n,Ra}^2\right) \tag{5.22}$$

where $v_{n,Rb}$ and $v_{n,Ra}$ are the noise voltage sources from R_b and R_a respectively. It is interesting to note that the noise from R_a is scaled by the value of R_b. Combining (5.21) and (5.22), results in the following expression for the input referred resistor noise:

$$v_{\text{IRN},R}^2 = 8kTR_b f_B\left(1 + \frac{R_b}{R_a}\right) \tag{5.23}$$

From (5.23) is it seen, that from a noise point of view the resistance of R_a should be maximized or R_b should be minimized, to minimize $v_{\text{IRN},R}^2$. However, from a modulator point of view neither solution is preferred. From (5.13) it is given, that a large resistor results in a small loopfilter coefficient. Since both k_a and k_b are realized via the same capacitor, it is not possible to compensate for a large resistor by reducing the capacitance without at the same time affecting the value of k_b.

From (5.19) a small value of R_b or a large value of R_a results in $|STF(0)|$ becoming larger than one. Assuming a large OSR, $|STF(0)|$ approximates the input signal gain, thus for $|STF(0)| > 1$ the input signal is amplified. This in turn reduces the MSA of the modulator. Thus, it is not possible to remove the noise from R_a by simply increasing it, due to the resulting effects on the loopfilter coefficients.

5.4.2.2 OTA Noise

From a similar noise analysis of the integrator circuit in Fig. 5.10 the input referred noise of the OTA, $v_{\text{IRN,OTA}}$, can be expressed as:

$$v_{\text{IRN,OTA}}^2 = 2\left(\frac{4}{3}\pi^2 R_b^2 C^2 f_B^2 + \left(1+\frac{R_b}{R_a}\right)^2\right) v_{n,\text{OTA,SE}}^2 \tag{5.24}$$

where $v_{n,\text{OTA,SE}}$ is the single-ended noise from the OTA. From (5.13) the integration capacitance C may be expressed as:

$$C = \frac{1}{k_b R_b f_s} = \frac{1}{2k_b R_b f_B OSR} \tag{5.25}$$

where OSR is the oversampling ratio of the modulator. Combining (5.24) and (5.25) the expression for $v_{\text{IRN,OTA}}^2$ becomes:

$$v_{ni,OTA}^2 = 2\left(\frac{\pi^2}{3k_b^2 OSR^2} + \left(1+\frac{R_b}{R_a}\right)^2\right) v_{n,OTA,SE}^2 \tag{5.26}$$

Assuming that $3k_b^2 OSR^2 >> \pi^2$, then the first term may be neglected resulting in the input referred noise of the OTA being equal to:

$$v_{\text{IRN,OTA}}^2 \approx 2\left(1+\frac{R_b}{R_a}\right)^2 v_{n,\text{OTA,SE}}^2 \tag{5.27}$$

From (5.27) is seen that $v_{\text{IRN,OTA}}$ is minimized when $R_a >> R_b$. Again this is not preferred from a modulator point of view, since from (5.19) the STF gain is increased.

5.4.2.3 Voltage Mode DAC Noise

The feedback DAC also adds noise to 1st integrator, and may be found by adding the DAC noise in the feedback "input" of the integrator. For voltage mode feedback, when referring the noise of the DAC to the input of the integrator it may be expressed as:

$$v_{\text{IRN,DAC}}^2 = 2\left(\frac{R_b}{R_a}\right)^2 v_{n,\text{DAC}}^2 \tag{5.28}$$

5.4.2.4 Current Mode DAC

As it was observed from (5.27), $v_{\text{IRN,OTA}}$ is minimized when $R_a >> R_b$, which is not realizable when using a voltage mode feedback DAC, due to the implications on the modulator. However, a large value of R_a may be achieved if current mode feedback is applied instead. Ideally a current source has an infinite output impedance, and with the current source replacing R_a, the OTA noise may be estimated as:

$$v^2_{\text{IRN,OTA}*} \approx 2v^2_{n,\text{OTA,SE}} \tag{5.29}$$

The input referred noise from the resistors is now only the contribution from R_b:

$$v^2_{\text{IRN},R*} = 2v^2_{n,Rb} \tag{5.30}$$

The DAC noise current, when input referred to the integrator input, is given as:

$$v^2_{\text{IRN,IDAC}} = 2R_b^2 i^2_{n,\text{IDAC}} \tag{5.31}$$

where $i_{n,\text{IDAC}}$ is the noise current from the DAC.

To replace the voltage mode DAC by the current mode DAC, the feedback current of the current mode DAC should equal the feedback current generated by the equivalent voltage mode DAC. Referring to Fig. 5.10 the maximum feedback current is given as:

$$i_{\text{FS}} = \frac{V_{\text{FS}}}{R_a} \tag{5.32}$$

where V_{FS} is the modulator full-scale input amplitude.

5.4.2.5 Input Referred Noise of Integrator

For the voltage mode DAC, the input referred noise of the integrator may be found by summing (5.22), (5.27), and (5.28). For the modulator to have $|STF(0)| = 1$, it is given from (5.19) that $R_a = R_b$, resulting in:

$$v^2_{\text{IRN}} = v^2_{\text{IRN},R} + v^2_{\text{IRN,OTA}} + v^2_{\text{IRN,DAC}} \tag{5.33}$$

$$\Leftrightarrow v^2_{\text{IRN}} = 4v^2_{n,Rb} + 8v^2_{n,\text{OTA,SE}} + 2v^2_{n,\text{DAC}} \tag{5.34}$$

For the current mode DAC, the input referred noise of the integrator may be found by summing (5.29), (5.30), and (5.31):

$$v^2_{\text{IRN}*} = v^2_{\text{IRN},R*} + v^2_{\text{IRN,OTA}*} + v^2_{\text{IRN,IDAC}} \tag{5.35}$$

$$\Leftrightarrow v^2_{\text{IRN}*} = 2v^2_{n,Rb} + 2v^2_{n,\text{OTA,SE}} + 2R_b^2 i^2_{n,\text{IDAC}} \tag{5.36}$$

Comparing (5.36) with (5.34) it is clear, that by using a current mode feedback DAC it is possible to reduce the input referred noise power of the OTA by a factor of 4. Furthermore, the input referred noise power from the resistor is reduced by a factor of 2; also assuming the DAC noise is the same for the current mode

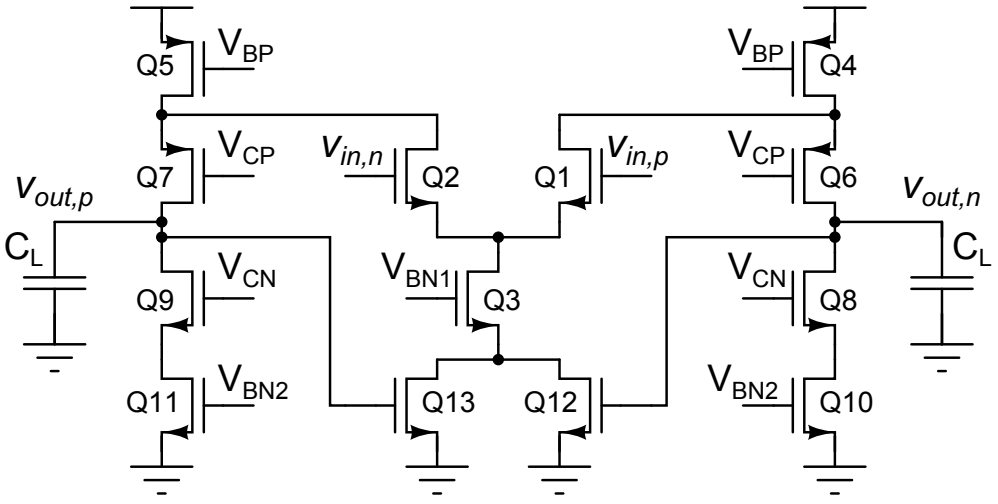


Figure 5.12: Fully differential folded-cascode OTA

DAC and voltage mode DAC. If the thermal noise of the OTA is limiting the biasing current of the OTA, then it may be possible to reduce the OTA current consumption without reducing the noise performance of the integrator. With the noise from the resistor being reduced as well, it may be possible to further relax the noise requirements of the OTA, reducing the biasing current further. Alternatively, the reduced input referred noise may be used to relax the noise requirements of other parts of the modulator including the DAC.

5.4.3 GBW and SR of Folded-Cascode OTA

The value of the integration capacitance in the active-RC integrator impacts the current consumption of the OTA. It is thus relevant to estimate the biasing current related to specific GBW and SR requirements. This depends on the specific OTA topology, and is here carried out for the folded-cascode OTA. This specific topology was selected, as it present a good compromise between speed, noise, and current consumption [78]. A schematic of a fully-differential folded-cascode is shown in Fig. 5.12. From [77], the GBW and SR of the folded-cascode OTA are given as:

$$GBW = \frac{2I_{d1}}{V_{ov}C_L} \tag{5.37}$$

$$SR = \frac{I_{d3}}{C_L} = \frac{2I_{d1}}{C_L} \tag{5.38}$$

where I_{d1} is the drain current of Q1, V_{ov} is the transistor overdrive voltage, and C_L is the load capacitance. For the active-RC integrator in a CT $\Delta\Sigma$ ADC, C_L may be approximated by the integration capacitance C. In reality the succeeding integrator stage will add a capacitive load to the output of the OTA, but this is ignored here in order to simplify the modeling. This additional capacitive loading may be added by multiplying C_L with a scaling factor.

From Fig. 5.12 it can be seen, that the current flowing in Q4 equals the sum of the drain currents in Q1 and Q10. During a slewing condition all of I_{d3} will flow through either Q4 or Q5, depending on the polarity of the input signal. To avoid that the transistors Q6-Q11 enter the triode region during an output slewing condition, the bias current of Q4 needs to be larger than that of Q3. The ratio of the currents is designated M:

$$M = \frac{I_{d4}}{I_{d3}} = \frac{I_{d4}}{2I_{d1}} \tag{5.39}$$

where $M > 1$. Based on (5.39), the required biasing current of Q4, to obtain a specific GBW and SR of the OTA, may be found by inserting (5.39) into (5.37) and (5.38):

$$I_{d4,GBW} = GBW \cdot M \cdot C_L \cdot V_{ov} \tag{5.40}$$

$$I_{d4,SR} = SR \cdot M \cdot C_L \tag{5.41}$$

Based on specified values for V_{ov} and M it is then possible to determine the minimum bias current needed in Q4.

5.4.4 Noise of Folded-Cascode OTA

When optimizing the modulator design based on the noise relations derived in Sec. 5.4.2, it is necessary to determine an expression for the OTA noise. By expressing the noise as a function of M it is possible to relate the biasing current in Q4 with a specific noise requirement for the OTA.

As it was the case for the integrator, the noise of the fully differential OTA may be analyzed by considering the differential half-circuit of the OTA. Referring to Fig. 5.12, and analyzing the input referred noise at the positive input, $v_{in,p}$, only the transistors Q2, Q4 and Q10 contribute noise. Q6 and Q8 are cascoding devices and their noise may be neglected. Transistors Q3, Q12 and Q13 only add common-mode noise and may also be neglected at the differential input. From [77] the flicker noise as a function of the frequency is given as:

$$v_{n,1/f}^2 = \int_{f_{B,l}}^{f_{B,u}} \frac{K}{WLC_{ox}f} df \tag{5.42}$$

where K is a device specific parameter, W and L are the MOSFET channel width and length respectively, C_{ox} is the gate capacitance per unit area, f is the frequency, and $f_{B,l}$ and $f_{B,l}$ are the lower and upper limits of the frequency band of interest. Since the flicker noise may be reduced by using large devices, it does not directly affect the required biasing current of the OTA. However, indirectly the size of the devices does affect the GBW and the phase margin of the folded-cascode OTA, as larger devices increase the parasitic capacitances in the internal nodes of the OTA. For simplicity this effect is not considered here. When optimizing the OTA, the flicker noise is considered by including the flicker noise in the noise budget for the OTA.

From [77] the thermal noise of the MOSFET, when referred to the gate, is given as:

$$v_{n,th}^2 = \frac{8}{3}kT\frac{1}{g_m}f_B = \frac{4}{3}kT\frac{V_{ov}}{I_d}f_B \tag{5.43}$$

where f_B is the frequency band of interest. Referring to Fig. 5.12, the thermal noise of the Q1, Q4 and Q10, when referred to the *INP* node, can be expressed as:

$$v_{n,\mathrm{OTA,SE}}^2 = v_{n1}^2 + \frac{g_{m4}^2}{g_{m1}^2}v_{n4}^2 + \frac{g_{m10}^2}{g_{m1}^2}v_{n10}^2 \tag{5.44}$$

where v_{nx} and g_{mx} are the noise voltage and transconductance of transistor Qx. Since the current flowing in Q1, Q4 and Q10 are related by the factor M, it is possible to express the transconductance and gate referred noise of Q4 and Q10 by those of Q1. From Fig. 5.12 and (5.39) the biasing current of Q10 can be expressed as:

$$I_{d10} = I_{d4} - I_{d1} = (2M-1)I_{d1} \tag{5.45}$$

For simplicity it is assumed that the overdrive voltage is the same for Q1, Q4 and Q10. As a result, g_m of Q4 and Q10 can be expressed from M and g_{m1} as:

$$g_{m4} = 2\frac{2MI_{d1}}{V_{ov}} = 2Mg_{m1} \tag{5.46}$$

$$g_{m10} = \frac{2\left[(2M-1)I_{d1}\right]}{V_{ov}} = (2M-1)\cdot g_{m1} \tag{5.47}$$

Similarly, the gate-referred thermal noise of Q4 and Q10 may be expressed from M and v_{n1}:

$$v_{n4}^2 = \frac{8}{3}kT\frac{1}{2Mg_{m1}}f_B = \frac{1}{2M}v_{n1}^2 \tag{5.48}$$

$$v_{n10}^2 = \frac{8}{3}kT\frac{1}{(2M-1)g_{m1}}f_B = \frac{1}{2M-1}v_{n1}^2 \tag{5.49}$$

By combining (5.44) and (5.46)-(5.49) the input referred noise power at the $v_{in,p}$ input is given as:

$$v_{n,\mathrm{OTA,SE}}^2 = v_{n1}^2 + 2Mv_{n1}^2 + (2M-1)v_{n1}^2 = 4Mv_{n1}^2 \tag{5.50}$$

By combining (5.43) and (5.50), the input referred thermal noise of the OTA can be expressed as:

$$v_{n,\mathrm{OTA,SE}}^2 = \frac{16}{3}MkT\frac{V_{ov}}{I_{d1}}f_B \tag{5.51}$$

To relate the input referred noise of the OTA to the biasing current of Q4, (5.51) may be rearranged and combined with (5.39) to give:

$$I_{d4,\mathrm{IRN}} = \frac{32}{3}M^2kT\frac{V_{ov}}{v_{n,\mathrm{OTA,SE}}^2}f_B \tag{5.52}$$

The expression in (5.52) may then be used for determining the OTA biasing current based for a given OTA thermal noise specification.

5.5 Optimization Method

To begin the design of the modulator, a set of requirements are needed, including the peak SNR of the ADC and a noise budget for the subblocks of the ADC. The noise budget may be divided as:

- Quantization noise power, $f_{np,\text{quan}}$
- Noise power from 1st integrator, $f_{np,\text{int1}}$, split into:
  - → Resistor thermal noise power, $f_{np,R}$
  - → OTA noise power, $f_{np,\text{OTA}}$, split into:
    - → OTA thermal noise power, $f_{np,\text{OTA,th}}$
    - → OTA flicker noise power, $f_{np,\text{OTA},1/f}$
- Noise from remaining modulator blocks, $f_{np,\text{rem}}$ (DACs, remaining integrators, and quantizer)

For a given modulator loopfilter the feedback coefficients are known. From the feedback coefficients the RC product for the integrator is given for a specific sampling frequency, f_s. From simulations of the modulator with quantizer with a given number of quantization levels, the associated MSA of the modulator can be estimated.

Based on thermal noise requirement of the 1st integrator, the input resistor may be found from (5.21). From this resistor value, the associated integration capacitor is given from the integrator RC product. The minimum biasing current related to the thermal noise requirement of the OTA can be found from (5.52) for a given value of M and V_{ov}. The GBW requirement of the OTA may be set based on experience, and in [22] a recommended minimum value of the GBW is 2-3 times f_s. From this requirement and (5.40), the minimum OTA biasing current related to the GBW can be found. The slew-rate requirement of the OTA is highly dependent on the number of quantization levels in the feedback DAC, which is equal to the number of levels in the quantizer. By increasing the number of quantization levels, the step size of the feedback signal is reduced, thus reducing the required SR of the OTA. From [22], and with reference to Fig. 5.10, the maximum slew-rate, $SR_{\max}$, of the 1st integrator in a CT ΔΣ modulator can be expressed as:

$$SR_{\max} = \max\left[f_s\left(k_b V_{in}(t) - k_a V_{dac}(t)\right)\right] \tag{5.53}$$

where V_{in} is the modulator input and V_{dac} is the DAC feedback signal. In case of a current mode DAC (5.53) may still be used, as the resulting output swing of the integrator due to the DAC is the same. The equivalent feedback voltage may then be used in (5.53). Using (5.53) it is thus possible to estimate the maximum SR of a given modulator based on a simulation of the equivalent DT modulator. The associated biasing current is then found from (5.41). The minimum biasing current of the OTA is then given as:

$$I_{OTA} = 2 \cdot \max\left\{I_{d4,\text{IRN}}, I_{d4,GBW}, I_{d4,SR}\right\} \tag{5.54}$$

As described in Sec. 5.2.4, by increasing the number of quantization levels a higher MSA may be achieved for the same loopfilter. With more quantization levels, more aggressive noise shaping may be applied, while achieving the same MSA. Thereby the loopfilter coefficients are further increased, which reduces the integrator RC product. However, the increased current consumption related to the increased number of quantization levels needs to be taken into account. Assuming a Flash ADC as quantizer, each quantization level requires an additional comparator [51]. Based on the current consumption of a comparator, the current consumption of the quantizer, I_Q, may be estimated as:

$$I_Q = (N_Q - 1) \cdot I_{comp} \tag{5.55}$$

where N_Q equals the number of quantization levels, and I_{comp} is the current consumption of a comparator.

Finally, the current consumption of the feedback DAC may be estimated, by considering the current injected from the DAC to the input of the OTA. This is a rough estimate, as in the case of a voltage mode DAC, voltage buffers are needed that also consume current. In the case of a current mode DAC the estimate is more precise. For a differential output DAC, the DAC current, I_{DAC}, may be estimated from the modulator full-scale input amplitude, V_{FS}, and the equivalent feedback resistance, R_{ai}:

$$I_{\mathrm{FS}} = \frac{V_{FS}}{R_{ai}} \tag{5.56}$$

The total current consumption of a design is then the sum of the current of the OTA of the 1st integrator, the quantizer and the feedback DAC:

$$I_{tot} = I_{OTA} + I_Q + I_DAC \tag{5.57}$$

The value of I_{tot} may then be found from a large set of modulator designs, by sweeping the NTF corner frequency and the number of quantization levels. The minimum total current consumption may be evaluated for each modulator configuration, and the overall minimum value may be determined. When optimizing the current consumption of the OTA, the noise power split via the values of $f_{np,R}$, $f_{np,\mathrm{OTA,th}}$, and $f_{np,\mathrm{OTA},1/f}$ may be fixed or swept as well, while keeping the sum equal to $f_{np,\mathrm{int1}}$.

5.5.1 Optimization Routine

Based on the listed information the optimization procedure is as follows:

1. Set f_c and find the modulator coefficients for the DT modulator
2. Find CT coefficients for the 1st integrator
3. Simulate the DT modulator to estimate the MSA, the peak signal to quantization noise ratio (SQNR), and $SR_{\max}$ for each quantizer configuration

4. Determine ADC input referred quantization noise power from estimated SNR, MSA and peak input signal level
5. Set noise partition between resistor and OTA noise powers
6. Calculate maximum integrator resistance from noise budget
7. Calculate integrator capacitance from integrator resistance and coefficients
8. Determine biasing current of Q4 to meet GBW, SR, and the OTA thermal noise requirement
9. Determine summed current consumption of OTA and quantizer from (5.57) for each quantizer configuration
10. Adjust noise power partition between resistor and OTA noise powers, and repeat step 6-9
11. Repeat step 2-10 for all values of f_c
12. Find the design solution with the minimum value of I_{tot}

The procedure is also graphically shown in Fig. 5.13.

The method is a brute force method, and thus the larger the set of values for f_c and quantizer levels, the longer the computational time is required to carry out the optimization method. Prior to running the optimization a set of parameters are needed. The modulator order and loopfilter topology is required, for the design of the loopfilter. The ADC full-scale voltage, V_{FS}, which equals the input amplitude for 0 dBFS input signal, is required in order to determine the equivalent input referred quantization noise of the modulator. In combination with the MSA for a given modulator, the associated noise floor may be determined. The modulator sampling frequency also needs to be defined in combination with the OSR, in order to calculate the SNR of the ADC. For evaluation of the current consumption of the folded cascode OTA, it is necessary to specify the M factor as well as V_{ov}. Finally, the feedback DAC waveform is needed for the conversion of the DT loopfilter to the CT equivalent.

Since it is necessary to provide a set of given parameters when carrying out the optimization procedure, the found solution is not necessarily the global minimum solution in the design space. Knowledge of CT ΔΣ modulators and circuit level realization of the blocks is therefore essential in order to achieve a useful results from the optimization routine.

5.6 Design Example

As an example of the application of the optimization method, a 3rd order CT ΔΣ ADC for audio signals range has been designed using the method. The

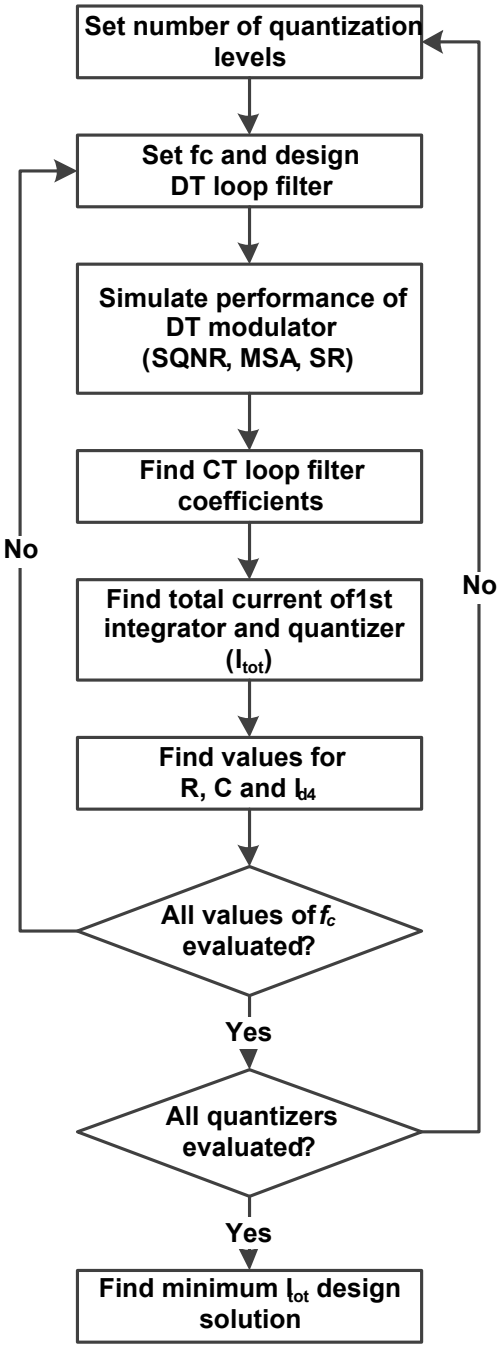


Figure 5.13: Flowchart of optimization routine

Table 5.3: Design parameters used for the optimization of the 3rd order CT ΔΣ ADC

Parameter	Value	Parameter	Value
Modulator order	3	SNR	84 dB
f_c range	150 kHz - 400 kHz	f_c sweep step	1 kHz
DAC type	NRZ	Feedback signal	Voltage
f_B	20 kHz	f_s	2.4 MHz
M	1.2	V_{FS}	1.4 V_{p}
V_{ov}	100 mV	GBW	$3f_s$
N_{quan}	3 - 9	I_{comp}	1.25 µA
$f_{np,\mathrm{int1}}$	55 %	$f_{np,\mathrm{quan}}$	20 %
$f_{np,\mathrm{rem}}$	25 %	$f_{np,\mathrm{OTA1},1/f}$	50 %

Table 5.4: Summary of results from optimization and simulation

Parameter	Value	Parameter	Value
Quantizer levels	7	f_c	398 kHz
k_{b1}	0.5047	k_{a1}	0.5047
k_{a2}	1.1319	k_{a3}	1.3744
R_a, R_b	711 kΩ	C	1.16 pF
Target $\mathrm{SNR}_{\mathrm{q+int1}}$	85.2 dB	Realized $\mathrm{SNR}_{\mathrm{q+int1}}$	84.3 dB
Target MSA	-2.25 dBFS	Realized MSA	-2.9 dBFS
Target I_{tot}	20.1 µA	Realized I_{tot}	28.1 µA

modulator uses a CIFB topology but only with the modulator input connected to the 1st integrator. Thus, k_{b2}, k_{b3} and k_{b4} are equal to zero. It was designed using fully differential circuits, and with the integrators implemented as active-RC integrators using a folded-cascode OTAs. The feedback DAC was designed as a voltage mode DAC.

The optimization method was implemented as a MATLAB script, and the loop filters were designed as Butterworth filters using the MATLAB Signal Processing Toolbox. For the design example only the OTA of the 1st integrator and the quantizer were at transistor level. The remaining blocks were modeled using Verilog-AMS. All design parameters used for the optimization are listed in Table 5.3. The current consumption of the used comparator at a sampling frequency of 2.4 MHz was 1.25 µA.

From the optimization method the resulting minimum current I_{sum} for the range of quantizers is shown in Fig. 5.14, showing a minimum for the solution using 7 quantization levels. The associated ADC design parameters are listed in Table 5.4 together with the results from simulation of the ADC. The power spectral density (PSD) of the output of the simulated modulator is shown in Fig. 5.15 for an input signal at MSA.

As seen from the results in Table 5.4 and in Fig. 5.15, the SNR from the optimization was almost achieved with the design; the difference was primarily due to lower MSA in the realized modulator. Note that the target and achieved SNR

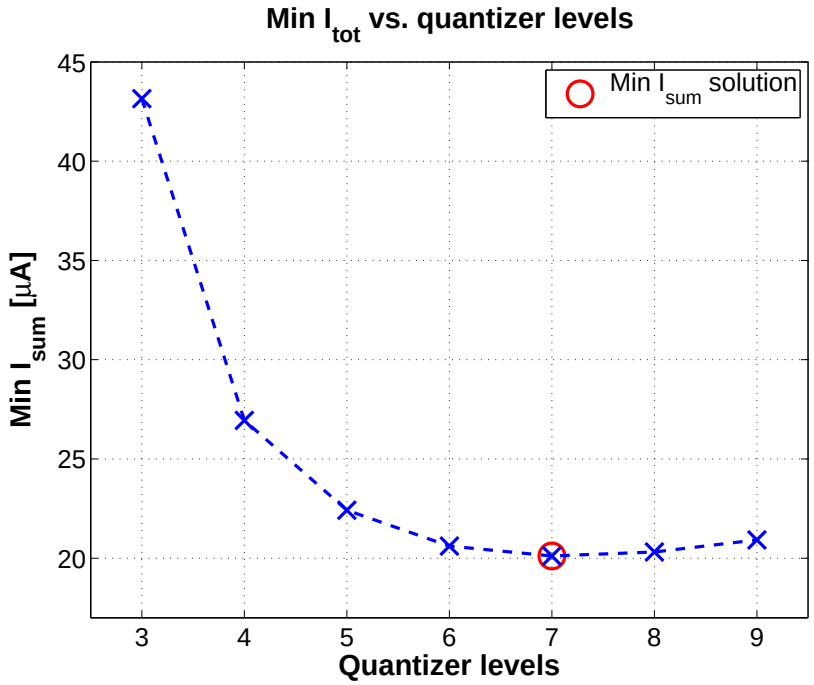


Figure 5.14: Minimum I_{tot} as a function of quantizer levels

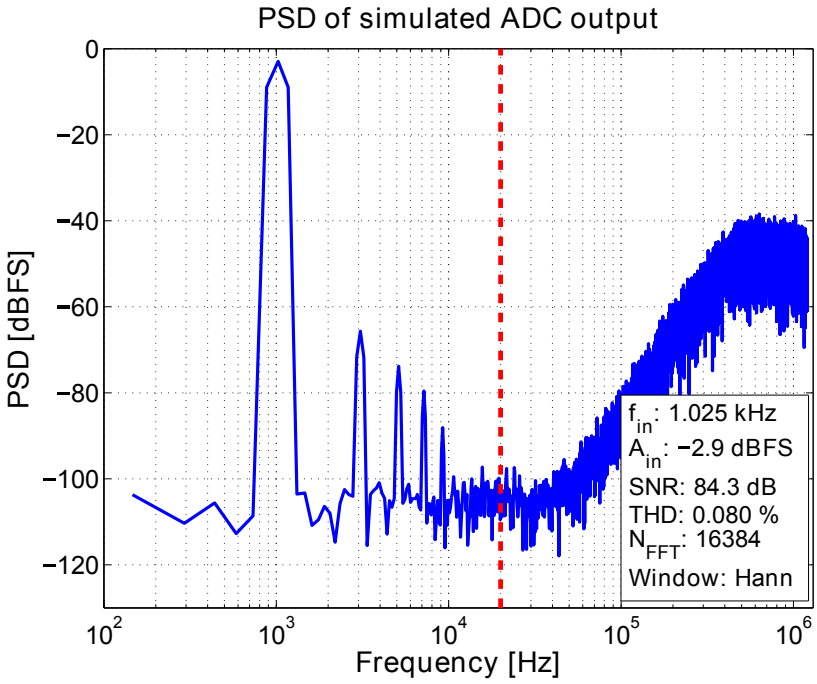


Figure 5.15: PSD of simulated ADC output, with dashed line indicating the signal bandwidth

values in Table 5.4 are for the quantization noise, and the flicker and thermal noise from the 1st integrator. Thus, the simulated SNR is larger than the value specified for the optimization. The current consumption of the realized design is approx 40 % above the design target. This discrepancy primarily follows from

the use of the Schichmann-Hodges model for the circuit analysis of the folded cascode OTA. Nevertheless, the found solution is still considered to be the minimum current solution, as the same increase in the current consumption would be expected in the other non-minimum current design solutions.

From Fig. 5.14 it is interesting to note, that the estimated current consumption is almost the same for modulator with 6 to 9 quantization levels; the difference is in the range of 1 μA. The optimization method only considers the current consumption of the quantizer. Other properties, like the number of output bits needed or the relation to the clock jitter are not included. Furthermore, the optimization method is based on the expected performance in the typical process corner. When designing the circuits to achieve the required performance in all process, voltage and temperature (PVT) corners, the current consumption of the final circuit is expected to be larger than estimated from the optimization method. The result of the optimization is therefore not to be considered the final solution. Instead it may be used as a very good starting point for achieving a low current design.

5.7 Summary

In the adaptive A/D conversion channel a CT ΔΣ ADC is a good choice of ADC due to the ability of achieving a high dynamic range while also having a low current consumption. However, for a given set of performance requirements, the design space of a CT ΔΣ ADC is very large. For the modulator alone the selection of the OSR, the loopfilter order, the NTF corner frequency, and the number of quantization levels is not a straight forward task. Similarly, for the circuit implementation of the modulator, even when restricting the design to the use of a specific integrator topology.

In this chapter it was shown how the choice of the modulator, and the resulting loopfilter coefficients directly affect the implementation of the active-RC integrator. Based on a set of performance requirements it is possible for a specific set of loopfilter coefficients to determine the current consumption of the modulator circuits. By the use of a brute force method, a large set of modulators can be designed and simulated to estimate the expected performance. In combination with the expressions for the integrator OTA current consumption, the current consumption of each design can be estimated. Thereby the current consumption of different modulator designs may be compared, and the optimal design from a current consumption point of view can be determined.

The method was demonstrated for the design of a 3rd order CT ΔΣ ADC, and simulation results showed that the optimization method underestimates the biasing current needed for the integrator OTA. This is in part due to the OTA biasing circuit not being included in the estimated current consumption; in part to the simplified assumptions regarding the loading of the OTA output and equivalent overdrive voltage for all transistors; and in part due to the use of the Schichmann-

Hodges model for analytically estimating the biasing current of the MOSFET used in the design. It is expected that by using more detailed transistor models, e.g. the EKV-model [79, 80], a more accurate current estimate may be obtained from the derived expressions for the circuits.

Nevertheless, the idea of considering the circuit level implementation of the loop-filter when designing the modulator, and thereby determine the minimum current design, is an important contribution of this project to the field of low power CT $\Delta\Sigma$ design. Since the current consumption would be underestimated for all designs, and since the OTA consumes the dominant part of the total current, the found solution may be considered a minimum current solution for the given design restrictions.

6

Continuous-Time $\Delta\Sigma$ ADC with Current Mode Feedback

This chapter describes the design of a low power CT $\Delta\Sigma$ ADC, by combining the active-RC integrator with a current mode feedback DAC. The use of current mode feedback is shown to reduce the noise of the integrator OTA. Thereby the noise requirements of the OTA may be relaxed, and the current consumption reduced. Furthermore it is shown, how the use of an odd number of quantization levels reduces the circuit noise of the current mode DAC for low modulator input signals. Based on this, and by the use of the optimization method presented in Chap. 5, a CT $\Delta\Sigma$ ADC with a current mode DAC is designed for audio applications. The circuit design is described, and the performance results of the designed ADC are presented. The simulation results show a dynamic range of 95 dB was achieved for a current consumption of 283 μA, resulting in a Figure-of-Merit of 262 fJ/conversion. The use of current-mode feedback in combination with the active-RC integrator for achieving a low current design is considered a significant contribution of this project to the field of low power CT $\Delta\Sigma$ ADC design. Measurement results of the fabricated design showed significantly degraded performance than simulatied. The error is identified and design changes are suggested for improving the performance of the ADC. The chapter is based on the ECCTD 2015 paper, App. D.

6.1 Modulator Design

The adaptive A/D conversion channel has the benefit of achieving a high dynamic range while using an ADC with a dynamic range below that of the conversion channel. Thus, a lower power ADC may be used that achieves a sufficient peak SNR for the specific conversion channel. With the reduced dynamic range requirement the CT $\Delta\Sigma$ ADC is a good candidate, due to the relaxed speed requirements of the integrators in comparison to a DT $\Delta\Sigma$ ADC. For audio applications the active-RC integrator is the preferred integrator topology for realizing the CT inte-

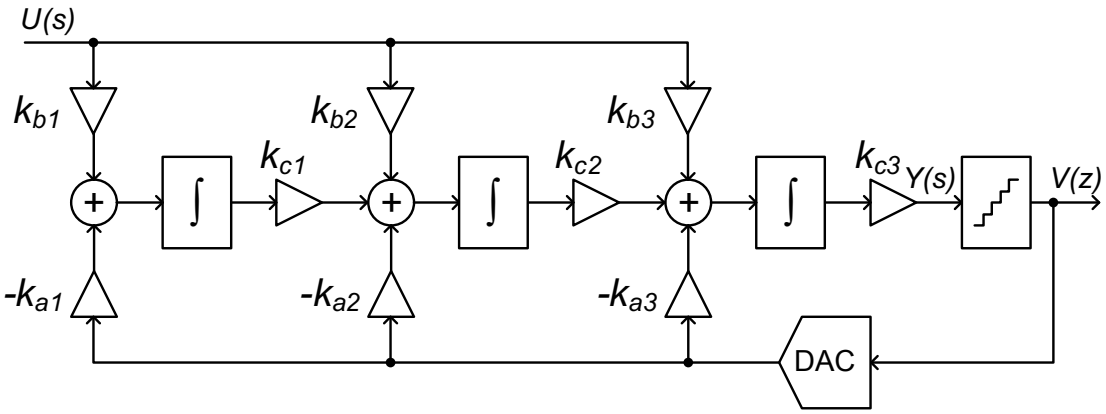


Figure 6.1: Block diagram of the designed 3rd order CT ΔΣ modulator

grators, due to the good linearity performance. In a CT ΔΣ ADC, the active-RC integrator is typically used in combination with voltage mode feedback. This has the benefit of achieving good matching between the input and the feedback coefficients, by matching of the equivalent resistors realizing the input and feedback coefficients. However, as shown in Sec. 5.4.2.5, the voltage mode feedback results in the noise of the integrator OTA being increased when referring the noise to the input of the integrator. If instead current mode feedback is used, the OTA noise is referred directly to the input; this results in a reduction of the OTA noise by a factor of 4. Thereby the noise requirement of the integrator OTA may be relaxed, which in turn reduces the minimum OTA biasing current. Thus, for an active-RC integrator with a specific noise requirement, the application of current mode feedback results in a lower current solution than when applying voltage mode feedback. With the feedback signal being a current, the is no longer good matching between the input and feedback coefficient. This may be solved by tuning of the coefficients, in order to achieve the required performance.

Based on the above observations, a 3rd order CT ΔΣ ADC with current mode feedback has been designed in a 0.18 μm standard CMOS process. The block diagram of the modualtor is shown in Fig. 6.1. The design of the modulator is based on the optimization method described in Chap. 5. A CIFB topology was selected for the modulator, as this topology does not require a summing circuit in front of the quantizer, thereby reducing the number of active blocks. The modulator was designed to have the input signal forwarded to the output of the 1st and the 2nd integrator, due to the resulting reduction in the output swing of the OTAs. This was not done for the 3rd integrator as this would require a summing circuit after the integrator.

The optimization method was updated, to reflect the use of current mode feedback. The total current, that was estimated, included the current consumption of the 1st OTA, the Flash ADC and the three feedback DACs; the DAC currents were estimated using (5.32), p. 86. Another addition to the optimization routine was the scaling of the filter coefficients to compensate for the worst case process variations [60]. The coefficients are reduced by a factor equal to the worst case increase of the coefficients in the fast process corner for both resistors and capac-

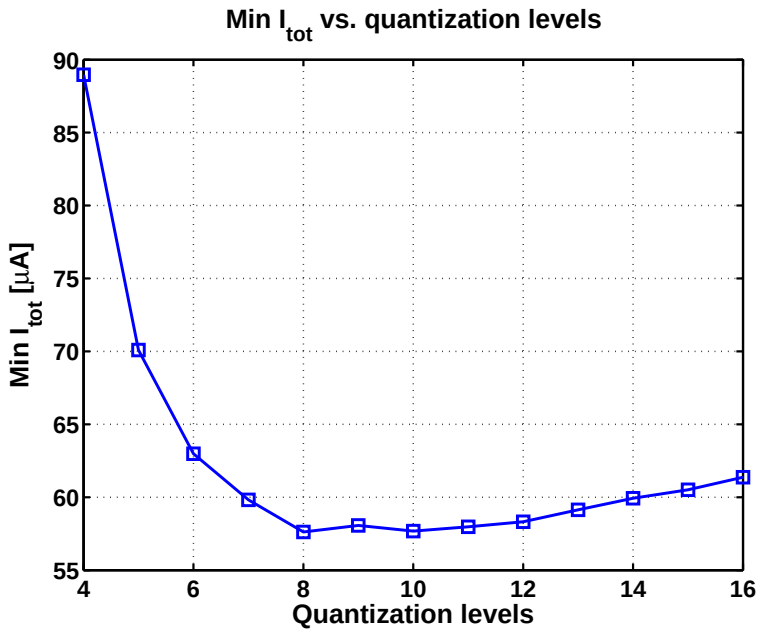


Figure 6.2: Total current consumption for different quantization levels

itors. Thereby the nominal loopfilter is obtained in the worst case corner. The reduction of the coefficients increases the values of the resistors and capacitors needed to realize the coefficients. To compensate for this decrease, the coefficients for the input and feedback coefficients of the 1st and 2nd integrator were scaled back to the unscaled value, by the use of the k_{c1} and k_{c2} coefficients in the modulator, thereby the same scaled down loopfilter transfer function is achieved. This was not done for the coefficients of the 3rd integrator, due to the lack of a summing block after the 3rd integrator, and k_{c3} is therefore implicitly equal to 1. The scaling of the coefficients results in a non-optimal NTF, and the scaled CT modulator loopfilter was therefore evaluated for the variation of the coefficients using a CT Simulink model of the modulator; this in order to verify that the modulator would be stable in all process corners.

A summary of the modulator design properties are listed in Table 6.1, including the main circuit specifications resulting from the optimization. The minimum current consumption as a function of the number of quantization is shown in Fig. 6.2, and with the estimated current consumption for the 1st OTA, the quantizer and the three DACs shown in Fig. 6.3. From the optimization it was found that a modulator with 8 quantization levels and a NTF corner frequency of 475 kHz would result in the minimum current solution. A schematic of the CT $\Delta\Sigma$ ADC is shown in Fig. 6.4.

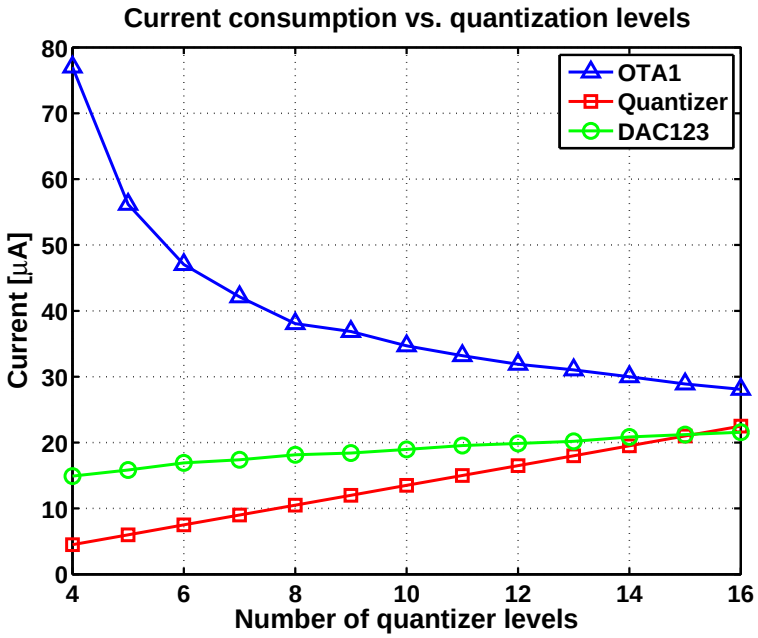


Figure 6.3: Current consumption of OTA1, DAC and Quantizer for different quantization levels

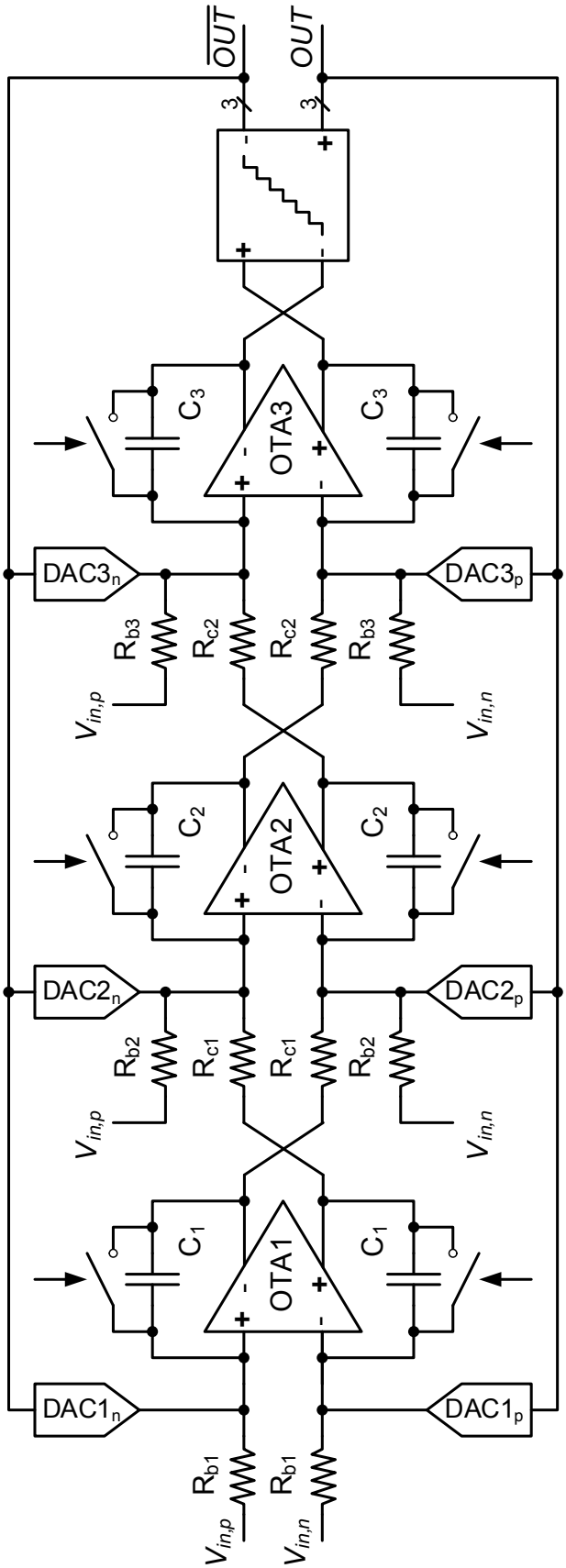


Figure 6.4: Schematic of the designed 3rd order CT ΔΣ ADC

Table 6.1: Summary modulator properties from optimization routine

Property	Value	Property	Value
Optimization input design output parameters			
Modulator order	3	Topology	CIFB
f_s	2.4 MHz	f_b	20 kHz
f_c range	300 kHz - 600 kHz	N_{quan}	4 - 16
f_c sweep step	5 kHz	|STF(0)|	-3 dB
DAC feedback type	Current mode	DAC waveform	NRZ
V_{FS}	1.53 V_p	VCM	0.85 V
M	1.2	V_{ov}	75 mV
$f_{np,q}$	22.5 %	$f_{np,jit}$	25 %
$f_{np,int}$	22.5 %	$f_{np,dac}$	20 %
$f_{np,rem}$	10 %	$f_{np,\mathrm{OTA1,1/f}}$	50 %
Target MSA	-3 dBFS	Target SNR	92 dB
Optimization output design parameters			
Quantization levels	8	f_c	475 kHz
MSA	-3 dBFS	$\{k_{a1}, k_{a2}, k_{a3}\}$	$\{0.769, 0.997, 1.110\}$
$\{k_{b1}, k_{b2}, k_{b3}\}$	$\{0.544, 0.705, 0.785\}$	$\{k_{c1}, k_{c2}, k_{c3}\}$	$\{0.493, 0.758, 1\}$
$v_{n,q,\mathrm{max}}$	11.0 μV_{rms}	$v_{n,\mathrm{int1}}$	11.4 μV_{rms}
$v_{n,\mathrm{int1,R,max}}$	10.2 μV_{rms}	$v_{n,\mathrm{int1,OTA,therm}}$	3.5 μV_{rms}
$v_{n,\mathrm{int1,OTA,flick}}$	3.5 μV_{rms}	I_{OTA1}	36.9 µA
$g_{m1,\mathrm{OTA1}}$	205 µA/V	GBW	$2.5 \cdot f_s$
SR	4.7 V/µs	$i_{a1,\mathrm{unit}}$, $i_{a2,\mathrm{unit}}$, $i_{a3,\mathrm{unit}}$	1.93 µA
R_{b1}, R_{b2}, R_{b3}	178.5 kΩ	R_{c1}	266.9 kΩ
R_{c2}	193.1 kΩ	C_1	4.11 pF
C_2	3.17 pF	C_3	2.85 pF

6.2 Current Mode DAC Noise

As it was shown in Sec. 5.4.2.5, when using a current mode feedback DAC in combination with the active-RC integrator, the noise power of the OTA when referred to the integrator input, is reduced by a factor of 4. Assuming that the biasing current of the OTA is limited by the thermal noise requirement, the current may be reduced by a factor of 4. With the 1st integrator in the modulator being the most critical, and thus having the largest current consumption, this improvement in current consumption is a significant part of the total current consumption of the CT $\Delta\Sigma$ ADC.

The output noise of a current mode DAC is a noise current, equal to the drain noise current of a MOSFET, which is given as [77]:

$$i_{d,n}^2 = \frac{8}{3} kT g_m \Delta f \tag{6.1}$$

where k is the Boltzmann constant, T is the absolute temperature, g_m the transistor transconductance, and Δf the noise frequency band. The current noise is thus proportional to the biasing current via g_m, where g_m given as:

$$g_m = \frac{2I_d}{V_{ov}} \tag{6.2}$$

In order to reduce the noise current, then from (6.1) and (6.2) the biasing current should be decreased or V_{ov} increased. Since the current flowing in the current source is related to the number of quantization levels, the number of quantization levels needs to be considered.

The DAC noise depends on the actual current being sourced or sunk from the integration capacitor. In the case of a single-bit modulator, the output current is numerically always the same: with only two output levels the same amount of current is either charging or discharging the capacitor. Thus, the noise from the DAC is always the same, independent of the input signal. In the case of a multi-level DAC this is not the case. Consider the case of a 3-level DAC that has the bipolar output values {-1,0,1}; an additional zero output has been added in comparison to the single-bit DAC. When the feedback value is zero, no DAC current is charging or discharing the capacitor, and no DAC noise is added to the capacitor. By adding more levels to the quantizer, the noise from the DAC depends on the quantizer output, which depends on the input signal.

Since the DAC noise is not constant for all modulator input levels, it is necessary to estimate the actual DAC noise for a given modulator input level. This may be done based on the noise of the minimum output current of the DAC. For a given input level, the average noise power may be estimated as a weighted average of the activity of the different output levels from the DAC, where the activity describes the percentage of a number of output samples that a number of current cells are connected to the DAC output. This weighted average is here defined as the DAC

noise factor, n_f, and may be expressed as:

$$n_f = \frac{1}{N} \sum_{\forall k} n_k \cdot k \tag{6.3}$$

where N equals the number output samples, k equals the number of current cells, and n_k equals the number of samples where k unit current cells were active. For the 8-level quantizer there are 8 distinct output levels given as $\{-4, -3, -2, -1, 1, 2, 3, 4\}$. These current levels may be described as ratios of the full-scale current, with the following ratios $\{-1, -\frac{5}{7}, -\frac{3}{7}, -\frac{1}{7}, \frac{1}{7}, \frac{3}{7}, \frac{5}{7}, 1\}$ times the full-scale current i_{FS}; thus, a unit current of $i_{unit} = \frac{1}{7} i_{fs}$ is used for the 8-level bipolar current mode DAC. The noise current is independent of the polarity of the output current, and it may be represented by the number of current cells that are active. To calculate the noise current power of the current mode DAC, this is given as:

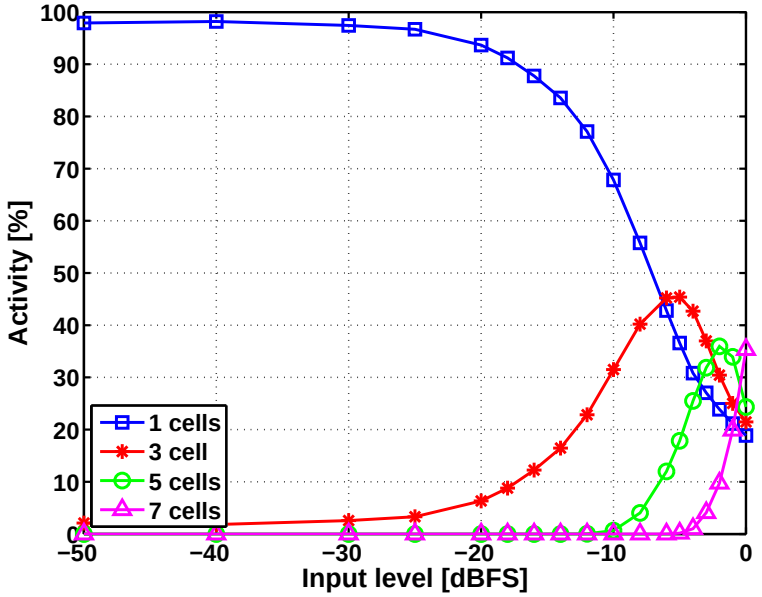
$$i^2_{n,\mathrm{IDAC}} = n_f \cdot i^2_{n,\mathrm{unit}} \tag{6.4}$$

where $i_{n,\mathrm{unit}}$ is the noise current of the unit current.

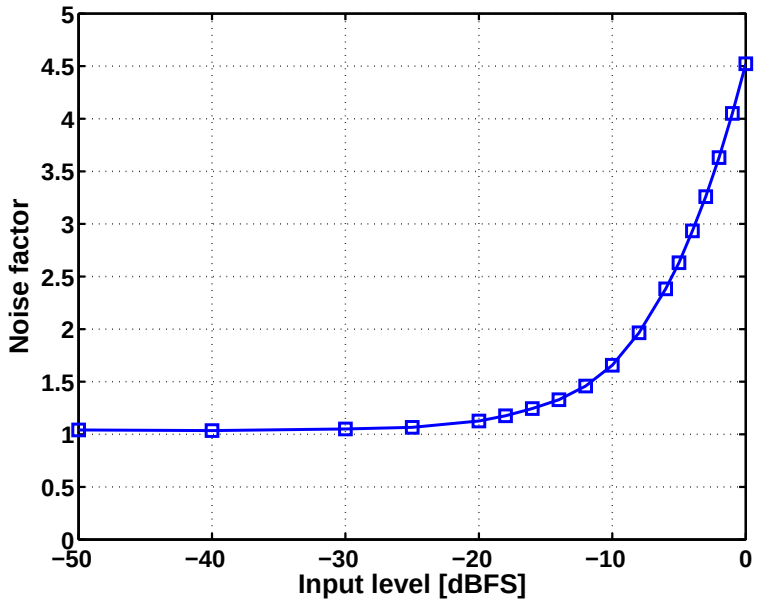
For the modulator with 8 quantization levels, the activity of the DAC output levels as a function of the input signal is shown in Fig. 6.5a. The resulting n_f as a function of the input level is shown in Fig. 6.5b. As seen from Fig. 6.5a, for input levels up to -20 dBFS, it is primarily a single current unit cell that is active. This results in the noise factor being approximately 1 up to -20 dBFS, as shown in Fig. 6.5b. However, as the input signal level increases, more current cells are active, thereby increasing the noise factor from 1 up to approximately 3.2 at the MSA.

As described for the 3-level DAC, an odd number of quantization levels adds the feedback value zero. If for the optimized modulator a 7-level quantizer is used instead, this significantly changes the activity of the current cells. For the 7-level quantizer there are 7 distinct current levels, given as $\{-1, -\frac{2}{3}, -\frac{1}{3}, 0, \frac{1}{3}, \frac{2}{3}, 1\}$ times the full-scale feedback current; thus a unit current of $\frac{1}{3} i_{FS}$. The activity and noise factor for the 7-level quantizer is shown in Fig. 6.6. As seen from Fig. 6.6a, the feedback value of zero is dominant up to an input level of -15 dBFS. As a result, the noise factor for the 7-level quantizer is approx. 1/3 for low input levels, as seen in Fig. 6.6b. Similarly, if 9-level quantization is used, the 9 distinct current levels are $\{-1, -\frac{3}{4}, -\frac{2}{4}, -\frac{1}{4}, 0, \frac{1}{4}, \frac{2}{4}, \frac{3}{4}, 1\}$ times i_{FS}, resulting in a unit current of $\frac{1}{4} i_{FS}$. The activity and noise factor for the 9-level DAC is shown in Fig. 6.7, from which it can be seen that the zero feedback value also dominates for small modulator input levels.

When comparing the DAC noise for DACs with a different number of output levels, it is important to not only consider n_f; the noise of the unit current should also be taken into account, as given from (6.4). Comparing the 7-level and 9-level DAC with the 8-level DAC, the unit currents in the 7-level DAC and 9-level DAC are 7/3 and 7/4 times larger respectively than the unit current in the 8-level DAC. This results in the noise power of unit current of the 7-level and 9-level DACs to be higher than for the 7-level DAC by a factor of 7/3 and 7/4 respectively. In

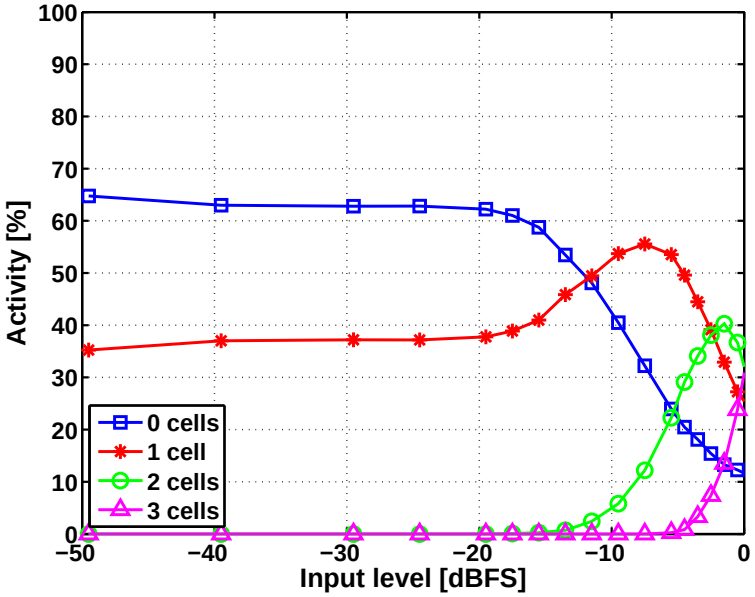


(a) Activity of DAC current cells

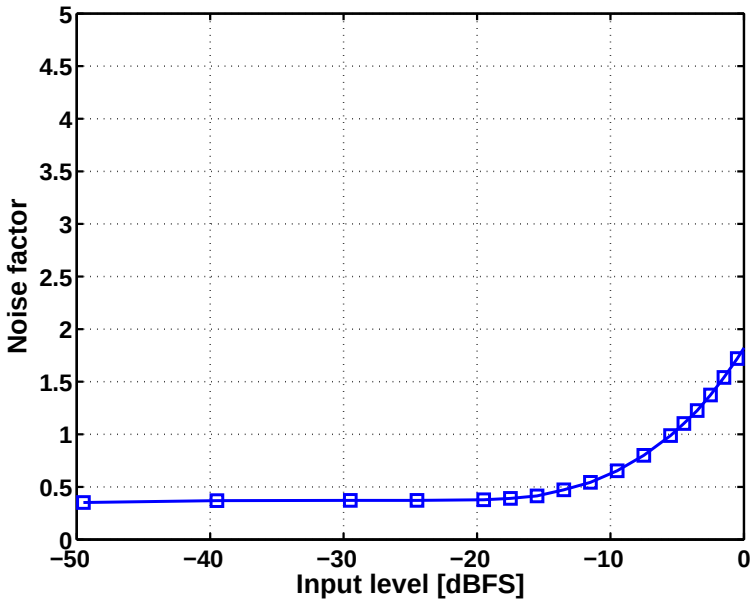


(b) DAC noise factor

Figure 6.5: Activity of current unit cells and current mode DAC noise factor for 3rd order modulator, with an 8-level quantizer

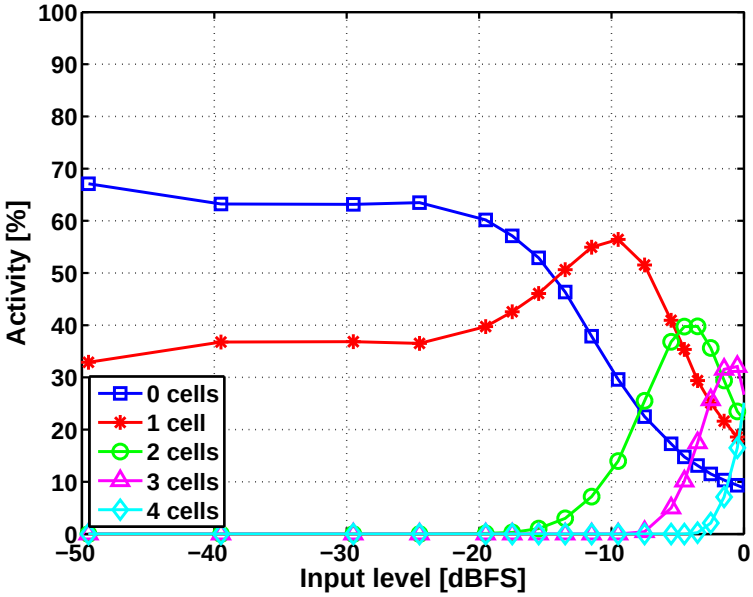


(a) Activity of DAC current cells

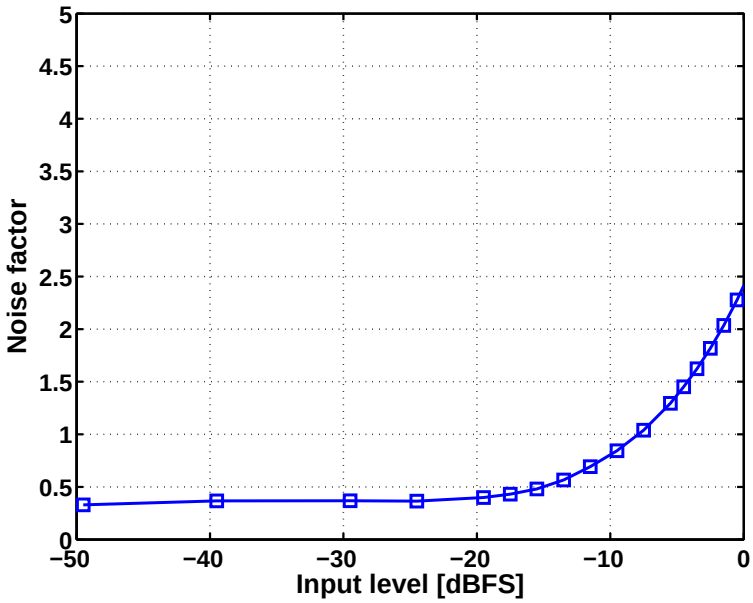


(b) DAC noise factor

Figure 6.6: Activity of current unit cells and current mode DAC noise factor for 3rd order modulator, with a 7-level quantizer



(a) Activity of DAC current cells



(b) DAC noise factor

Figure 6.7: Activity of current unit cells and current mode DAC noise factor for 3rd order modulator, with a 9-level quantizer

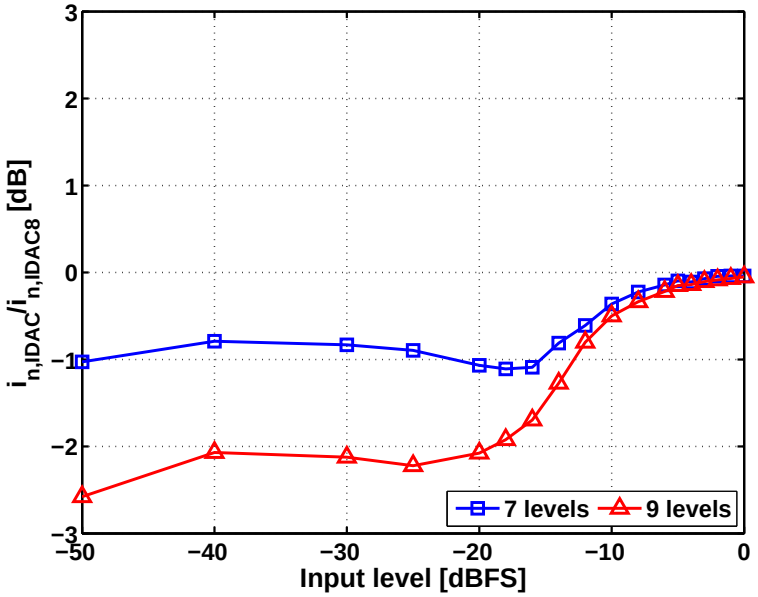


Figure 6.8: 7-level and 9-level DAC noise normalized to noise of 8-level DAC, as a function of input level

Fig. 6.8 is shown the ratio of the noise from the 7-level and 9-level DAC when normalized to the noise of the 8-level DAC and as a function of the modulator input level. As seen from the figure, by using a 7-level or 9-level DAC the noise is reduced for the low input levels by 1 dB for the 7-level DAC and by 2 dB for the 9-level DAC; at higher input levels, the noise is approximately the same as for the 8-level DAC. This comparison was based on the assumption, that V_{ov} is the same for the unit current cells in all three DACs. This is not necessarily the case, as the overdrive voltage may more easily be increased for current cells with a larger current. Thus, for both the 7-level and the 9-level DAC, it may be possible to further reduce the noise; Overall, both DACs may achieve a lower DAC noise than for the 8-level DAC.

The above noise considerations were not taken into account when carrying out the optimization routine for the design. Based on the noise improvement shown in Fig. 6.8, a 9-level quantizer may be the better option. However, with 9 quantization levels an additional bit is required in the modulator output as well as an additional comparator in the quantizer. Both additions will increase the current consumption of the modulator, although only slightly. Nevertheless, based on the above observations regarding the DAC noise, the modulator quantizer was selected to have 7 quantization levels. Investigation of the optimization results showed, that by using the same modulator loopfilter but with a 7-level quantizer, the MSA was only reduced by 0.5 dB and the minimum SQNR reduced from 96 dB to 92 dB; both reduction were considered to be acceptable.

6.3 Circuit Design

6.3.1 Integrator

The active-RC integrators were implemented using P-doped polysilicon resistors and the capacitors were implemented using metal-insulator-metal (MIM). Switches were connected between the capacitor terminals in order to reset the integrators at start-up. The values of the passive components are listed in Table 6.1.

The integrators were implemented using fully-differential folded-cascode OTAs, as shown in Fig. 6.9 as also done in the optimization routine for the design. Since the modulator uses a CIFB topology with the input forwarded to the output of the 1st and 2nd integrators, these integrators only process the feedback signal. The limited output swing of the folded-cascode OTA is therefore not a problem. The OTA for the 2nd integrator was edsigned as a scaled down version of the OTA in the 1st integrator, thereby reducing the current consumption. Since the non-idealities at the output of the 2nd integrator are 2nd order noise-shaped, increased circuit noise and distortion due to a lower GBW and SR are not considered a problem.

The modulator input is not forwarded to the output of the 3rd integrator, and OTA of this integrator therefore processes both the feedback signal and the input signal. The increased signal swing may cause the integrator output to saturate, which would make the modulator unstable. Therefore, in order to handle the increased output signal swing, the cascode transistors Q8 and Q9 were removed. This has the side-effect of reducing the OTA output impedance, which in turn reduces the DC gain. Also, the improvement in signal-swing is only single sided. However, due to the high gain of OTA1 and OTA2, a lower gain in OTA3 was not considered to reduce the loop gain too much. Furthermore, this would reduce the output signal level for lower input frequencies, thus reducing the risk of the integrator output saturating. For large modulator input signal levels, clipping may also occur at the output of the 3rd integrator, but the generated distortion is noise shaped by the modulator. The biasing currents and transistor dimensions in the 3rd integrator OTA were also scaled down in comparison to OTA1.

The biasing circuit for the OTAs was implemented using wide-swing cascode current mirrors [11]. A schematic of the biasing circuit is shown in Fig. 6.10, and the transistor dimensions are listed in Table 6.3. The wide-swing current mirror has a stable state, were no current is flowing in the transistor despite of the supply voltage has been ramped up to the final level. To avoid this zero state, a starter circuit was used to initialize bias circuit when ramping up the supply voltage.

With the OTAs being fully-differential, linear common-mode feedback (CMFB) is applied to set the correct common-mode level at the OTA output. In Fig. 6.9, the transistors Q12 and Q13 operating in the triode region realize the linear CMFB function [22, 81]. The common-mode reference level is connected to Q16b in the biasing circuit, which is placed in the same branch of the bisa circuit as

Q15b that biases Q3 in the OTA. The benefit of this CMFB implementation is that no additional current is needed for the CMFB circuit. To avoid that the output swing of the OTA was reduced significantly due to the CMFB circuit, Q12 and Q13 were implemented using native NMOS transistors. The benefit of the native transistor is the near zero volt threshold voltage, thereby avoiding that the CMFB is turned off due to the output nodes of the OTA dropping below V_{th} of Q12 and Q13. The drawback of using the native transistors is the resulting large overdrive voltage that reduces the transconductance of the transistors. As a result, the common-mode GBW is low in comparison to the differential-mode GBW by a factor of approximately 20. This is fairly low, but simulations showed that it was sufficient.

In Table 6.2 are listed the main properties for the implemented OTAs. The current consumption of the 1st integrator OTA is 2.3 times larger in the final design than estimated in the optimization. This was necessary in order to achieve the required noise performance of the OTA. The poor estimate is primarily due to the inaccuracy of the Schichmann-Hodges model when relating the MOSFET transconductance to the biasing current and V_{ov}. Furthermore, the noise analysis of the folded-cascode, described in Sec. 5.4.4, does not consider the impact of the flicker noise. To reduce the noise from Q4 and Q10 in the differential half-circuit, it is necessary to either have a large g_{m1} or small g_{m4} and g_{m10}. Reducing g_{m4} and g_{m10} requires increasing the overdrive voltage, which impacts the output swing of the OTA. In order to reduce flicker noise from Q4 and Q10 they should have large gate areas, but if made too large the parasitic capacitance will reduce the phase margin of the OTA. Therefore, g_{m1} needs to be increased as well, to a larger value than estimated with the optimization routine. Thus, the total current consumption of the OTA increases.

Based on this design it can be seen, that a more even split of the noise power budget between the integrator resistor and the OTA may have been better then determined from the optimization method.

6.3.2 Quantizer

The quantizer was implemented as a fully-differential 7-level Flash ADC, with a resistor string for generating the reference levels. A block diagram of the Flash ADC is shown in Fig. 6.11, and the schematic for the designed comparators is shown in Fig. 6.12. The comparators were designed using a differential preamplifier stage followed by a dynamic latch stage with a SR-latch at the output. The preamplifier has two functions: it amplifies the difference between the differential input signal and the differential reference level, thereby reducing the decision time for the dynamic latch; and it reduces kick-back noise from the dynamic latch at the input of the comparator.

The dynamic latch is clocked, and enters the decision period when the clock signal is high. Based on the output from the preamplifier, the output of the latch is either pulled low or high. When the clock signal is low, the latch is reset, thereby

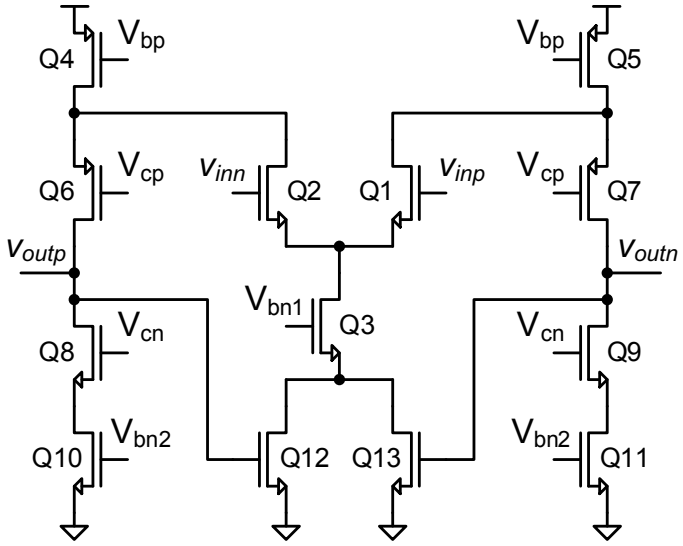


Figure 6.9: Schematic of folded-cascode OTA

Table 6.2: Summary of simulated circuit properties for OTA1, OTA2 and OTA3

Property	**OTA1**	**OTA2**	**OTA3**
$\left(\frac{W}{L}\right)_{1,2}$	$28 \cdot \frac{3.745\ \mu m}{4.0\ \mu m}$	$12 \cdot \frac{3.745\ \mu m}{4.0\ \mu m}$	$10 \cdot \frac{3.745\ \mu m}{4.0\ \mu m}$
$\left(\frac{W}{L}\right)_{3}$	$28 \cdot \frac{5.615\ \mu m}{3.0\ \mu m}$	$12 \cdot \frac{5.615\ \mu m}{3.0\ \mu m}$	$10 \cdot \frac{5.615\ \mu m}{3.0\ \mu m}$
$\left(\frac{W}{L}\right)_{4,5}$	$140 \cdot \frac{2.170\ \mu m}{4.0\ \mu m}$	$60 \cdot \frac{2.170\ \mu m}{4.0\ \mu m}$	$50 \cdot \frac{2.170\ \mu m}{4.0\ \mu m}$
$\left(\frac{W}{L}\right)_{6,7}$	$84 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$	$36 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$	$30 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$
$\left(\frac{W}{L}\right)_{8,9}$	$84 \cdot \frac{0.350\ \mu m}{3.0\ \mu m}$	$36 \cdot \frac{0.350\ \mu m}{3.0\ \mu m}$	-
$\left(\frac{W}{L}\right)_{10,11}$	$84 \cdot \frac{1.405\ \mu m}{3.0\ \mu m}$	$36 \cdot \frac{1.405\ \mu m}{3.0\ \mu m}$	$30 \cdot \frac{1.405\ \mu m}{3.0\ \mu m}$
$\left(\frac{W}{L}\right)_{12,23}$	$14 \cdot \frac{0.855\ \mu m}{12.0\ \mu m}$	$6 \cdot \frac{0.855\ \mu m}{12.0\ \mu m}$	$5 \cdot \frac{0.855\ \mu m}{12.0\ \mu m}$
I_{tot}	86.4 µA	36.4 µA	24.2 µA
$g_{m,1,2}$	302 µA/V	125 µA/V	96 µA/V
$g_{m,4,5}$	510 µA/V	216 µA/V	179 µA/V
$g_{m,10,11}$	427 µA/V	180 µA/V	162 µA/V
$g_{m,12,13}$	14.5 µA/V	6.2 µA/V	4.6 µA/V
$v_{\text{IRN,OTA,therm}}$	2.8 μV_{rms}	5.1 μV_{rms}	5.4 μV_{rms}
$v_{\text{IRN,OTA,flick}}$	3.5 μV_{rms}	9.8 μV_{rms}	12.8 μV_{rms}
$v_{\text{IRN,OTA}}$	4.5 μV_{rms}	11.0 μV_{rms}	13.8 μV_{rms}
GBW @ C_{int}	8.32 MHz	4.99 MHz	4.27 MHz

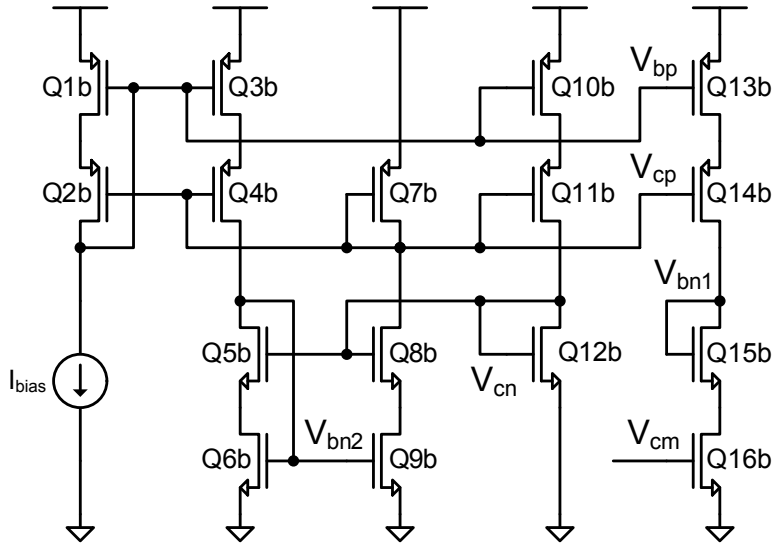


Figure 6.10: Schematic of OTA biasing circuit

Table 6.3: Summary of simulated circuit properties of the OTA biasing circuit

Property	Value	Property	Value
$\left(\frac{W}{L}\right)_1$	$5 \cdot \frac{2.170\ \mu m}{4.0\ \mu m}$	$\left(\frac{W}{L}\right)_9$	$5 \cdot \frac{1.405\ \mu m}{3.0\ \mu m}$
$\left(\frac{W}{L}\right)_2$	$5 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$	$\left(\frac{W}{L}\right)_{10}$	$3 \cdot \frac{2.170\ \mu m}{4.0\ \mu m}$
$\left(\frac{W}{L}\right)_3$	$4 \cdot \frac{2.170\ \mu m}{4.0\ \mu m}$	$\left(\frac{W}{L}\right)_{11}$	$3 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$
$\left(\frac{W}{L}\right)_4$	$4 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$	$\left(\frac{W}{L}\right)_{12}$	$3 \cdot \frac{0.350\ \mu m}{3.0\ \mu m}$
$\left(\frac{W}{L}\right)_5$	$4 \cdot \frac{0.350\ \mu m}{3.0\ \mu m}$	$\left(\frac{W}{L}\right)_{13}$	$4 \cdot \frac{2.170\ \mu m}{4.0\ \mu m}$
$\left(\frac{W}{L}\right)_6$	$4 \cdot \frac{1.405\ \mu m}{3.0\ \mu m}$	$\left(\frac{W}{L}\right)_{14}$	$4 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$
$\left(\frac{W}{L}\right)_7$	$1 \cdot \frac{0.540\ \mu m}{1.0\ \mu m}$	$\left(\frac{W}{L}\right)_{15}$	$1 \cdot \frac{5.615\ \mu m}{3.0\ \mu m}$
$\left(\frac{W}{L}\right)_8$	$5 \cdot \frac{0.350\ \mu m}{3.0\ \mu m}$	$\left(\frac{W}{L}\right)_{16}$	$1 \cdot \frac{0.855\ \mu m}{12.0\ \mu m}$
I_{bias}	1.5 µA	I_{tot}	6.3 µA

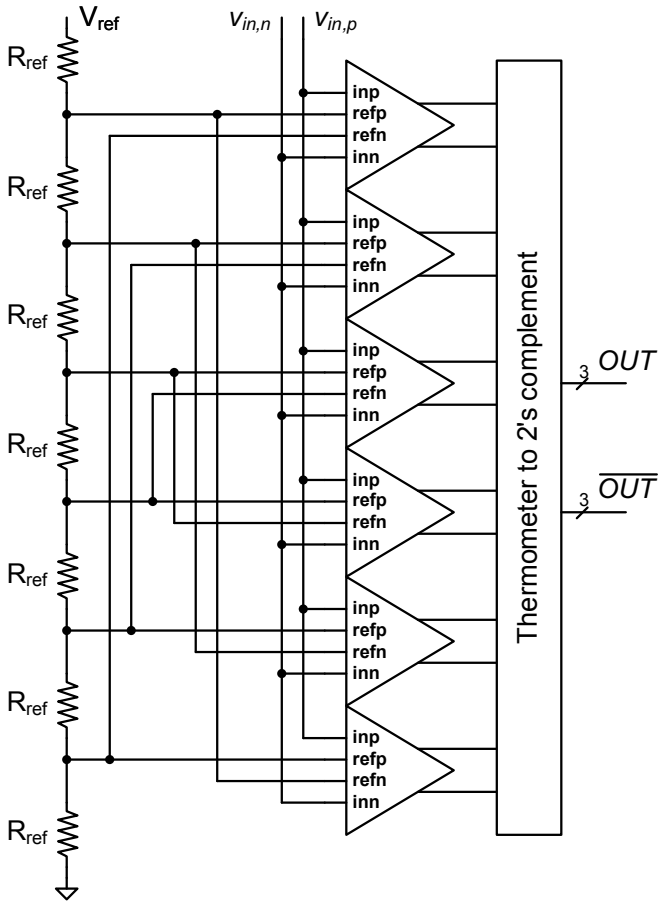


Figure 6.11: Schematic of 7-level flash ADC

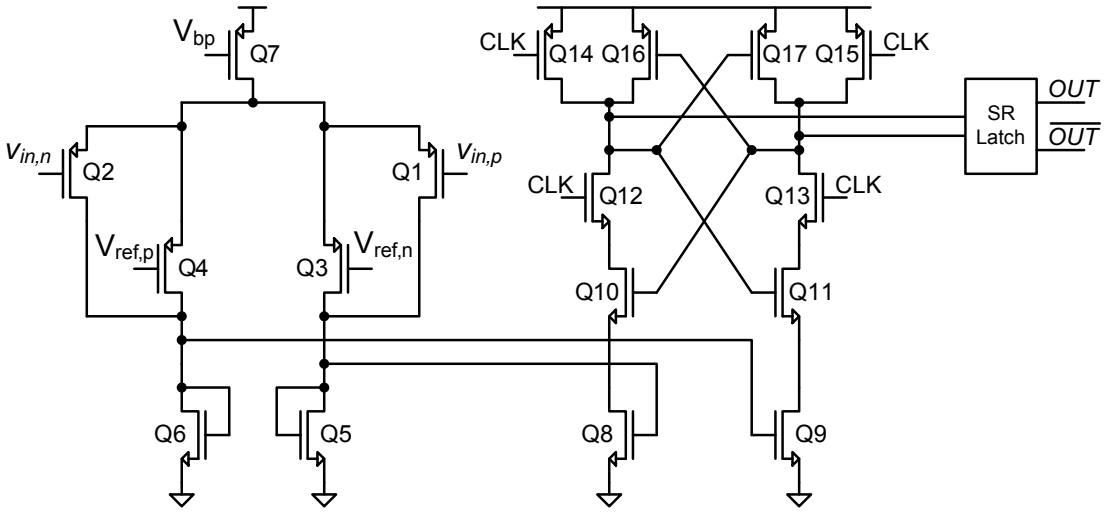


Figure 6.12: Schematic of comparator

Table 6.4: Summary of quantizer circuit properties

Property	Value	Property	Value
Comparator transistor dimensions			
$\left(\frac{W}{L}\right)_{1,2}$	$1 \cdot \frac{0.410\ \mu m}{1.0\ \mu m}$	$\left(\frac{W}{L}\right)_{10,11}$	$1 \cdot \frac{0.220\ \mu m}{0.180\ \mu m}$
$\left(\frac{W}{L}\right)_{3,4}$	$1 \cdot \frac{0.410\ \mu m}{1.0\ \mu m}$	$\left(\frac{W}{L}\right)_{12,13}$	$1 \cdot \frac{0.220\ \mu m}{0.180\ \mu m}$
$\left(\frac{W}{L}\right)_{5,6}$	$1 \cdot \frac{0.220\ \mu m}{0.180\ \mu m}$	$\left(\frac{W}{L}\right)_{14,15}$	$1 \cdot \frac{0.220\ \mu m}{0.180\ \mu m}$
$\left(\frac{W}{L}\right)_{7}$	$4 \cdot \frac{0.410\ \mu m}{1.0\ \mu m}$	$\left(\frac{W}{L}\right)_{16,17}$	$1 \cdot \frac{0.220\ \mu m}{0.180\ \mu m}$
$\left(\frac{W}{L}\right)_{8,9}$	$8 \cdot \frac{0.220\ \mu m}{0.180\ \mu m}$		
Flash ADC circuit properties			
I_{tot}	9.2 μA	$t_{d,\max}$	1.5 ns

reducing memory effects.

The dynamic latch was designed with minimum length transistors in order to reduce parasitic capacitances, and thereby reduce the decision time. Since all non-idealities of the comparators, including circuit noise and input offset, are noise-shaped, these are not of any concern. Thus, the current consumption can be kept very low. The output of the comparators was converted from thermometer code to 2's complement using combinational logic implemented with CMOS standard cells. The comparator preamplifier stage was biased using a simple current mirror and a reference current. The circuit properties for Flash ADC and comparators are summarized in Table 6.4. The property $t_{d,\max}$ identifies the maximum settling time of the output of the quantizer, when also considering process corners. Based on this value the time delay of the delayed clock signal for the DACs was set to be above this maximum settling time of the quantizer.

6.3.3 Current Mode DAC

As described in Sec. 6.2, the DAC was designed with 7-levels and bipolar output, using three unary weighted current cells as seen in Fig. 6.14, where the block diagram of the DAC is shown. A schematic of the current unit cell is shown in Fig. 6.13. The current cells consists of two cascode current sources that either source or sink a unit current from the output nodes. Cascodes are used in order to increase the output impedance of the DAC, and to reduce modulation of the output current due to variation on the OTA inputs. Depending on the feedback value, the current source consisting of Q1 and Q3 sources a current to the output, and can be connected to the positive or the negative output via the output transmission gates T3-T6. Similarly, for the current sink formed by Q2 and Q4. Each DAC consists of three cells, that all connect to the same output node, thus being able to feedback the values {-3,-2,-1,0,1,2,3}.

In case of a feedback value of zero, the both current sources are disconnected from the output and connected directly via the transmission gates T1 and T2. In

Table 6.5: Summary of the main circuit properties of the DAC current unit cell

Property	Value	Property	Value
$\left(\frac{W}{L}\right)_1$	$4 \cdot \frac{8.73\ \mu m}{10.0\ \mu m}$	$\left(\frac{W}{L}\right)_2$	$4 \cdot \frac{5.025\ \mu m}{26.68\ \mu m}$
$\left(\frac{W}{L}\right)_3$	$10 \cdot \frac{2.795\ \mu m}{2.0\ \mu m}$	$\left(\frac{W}{L}\right)_4$	$10 \cdot \frac{1.36\ \mu m}{4.5\ \mu m}$
g_{m1}	21.0 µA/V	g_{m2}	19.5 µA/V
$R_{out,p}$	438 MΩ	$R_{out,p}$	668 MΩ
I_{unit}	1.92 µA	$i_{irn,DAC1}$	116 pA_{rms}

this manner, the current sources are always active and there is no start-up delay when reconnecting the current cells to the DAC output nodes.

Since the feedback currents are integrated continuously, an error in the output current results in an error being injected into the modulator. This is especially critical for the DAC connected to the 1st integrator, where the errors injected to the integrator input are not noise-shaped. When the current sources are disconnected from the output and instead directly connected internally, a reference common-mode voltage, V_{cm} is connected to the drain nodes of Q3 and Q4 via T1 and T2; this reference voltage is identical to the common-mode level at the input of the OTAs. The reference voltage is needed in order to avoid the drain voltages of Q3 and Q4 shifting to another level when not connected to the DAC output. This would lead to charging or discharging of the parasitic capacitances at these nodes. When the current sources are reconnected to the OTA input, then due to the change in voltage level at the drains of Q3 and Q4, the parasitic capacitances are charged or discharged to the input level of the OTA. This redistribution of charge to and from the parasitic capacitances steals charge from the feedback current signal, resulting in an error in the integrated feedback signal. This in turn lead to added noise in the modulator output. By applying the reference common-mode level when the cells are inactive, the charge lost to the parasitic capacitances is reduced. Since the reference buffer is not generated to the DAC output, the buffer noies was considered to be unimportant.

As discussed in Sec. 6.2, the noise current of the current mode DAC is proportional to the transconductance of the current sources, Q1 and Q2. With the biasing current being fixed, a large V_{ov} in the range of 150 mV was used to reduce the g_m of Q1 and Q2. The properties of the unit current cells are summarized in Table 6.5.

The biasing circuit for the DAC unit current cells was implemented using wide-swing cascode current mirrors, similar to the current mirrors used for the OTA biasing circuit. The schematic for the DAC biasing circuit is shown in Fig. 6.15. Since the DAC output is pseudodifferential, the DAC biasing circuit is critical from a noise point of view. The noise generated by transistor Q3b in the biasing circuit, is connected to Q1 in the current cell via the gate. Thus, the noise current

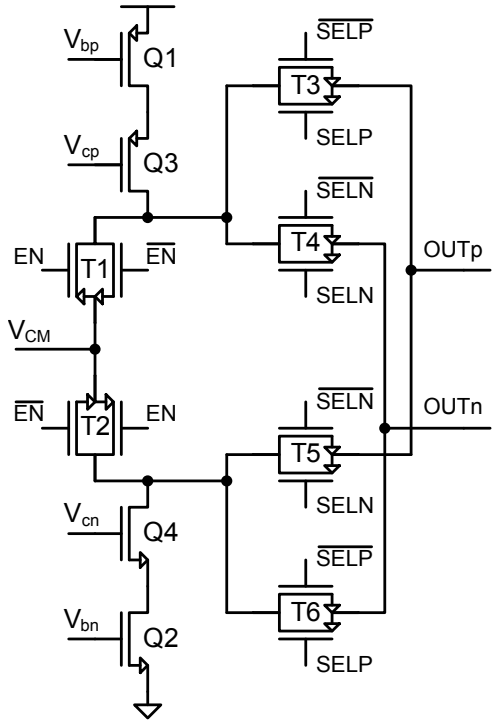


Figure 6.13: Schematic of current unit cell of current mode DAC

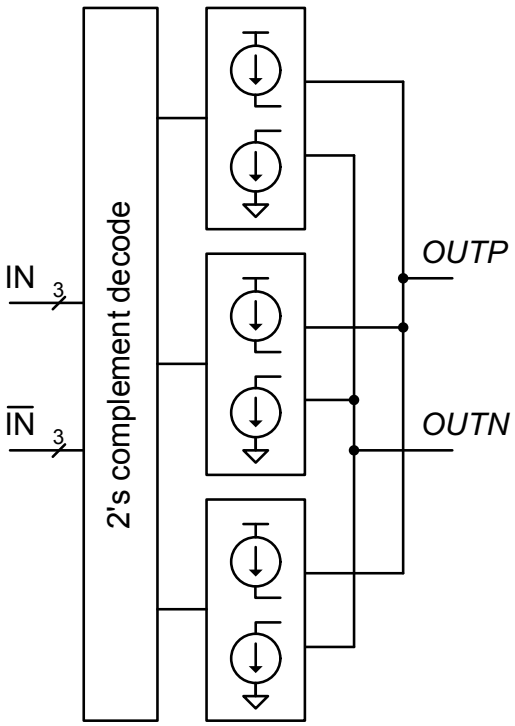


Figure 6.14: Block diagram of current mode DAC

generated at the *outp* node of the current cell is given as:

$$i^2_{n,\text{outp}} = i^2_{n,Q1} + g^2_{m1} v^2_{ng,Q3b} \tag{6.5}$$

where $v_{ng,Q3b}$ is the gate-referred noise of transistor Q3b. To reduce the noise from the bias circuit, g_{m1} should be low compared to g_{Q3b}. Increasing g_{Q3b} has the double effect of also reducing the thermal noise of Q3b. The same observations are valid for Q9b, which biases Q2 in the current cell. Thus, in order to reduce noise in the bias circuit, the current consumption of the bias circuit is high in comparison to the current flowing in the current unit cells. The properties for the DAC bias circuit are listed in Table 6.6.

The control signals for the three current cells of each DAC were generated using combinational logic, that converts the 2's complement input signal to the control signals. The inputs to the decoding logic is sampled by a latch, that was clocked by a delayed version of the sampling clock. This was needed due to the settling time of the Flash ADC output. If the latch clock is not delayed in relation to the sampling clock of the quantizer, glitches or incorrect output values will occur at the output of the DAC. This in turn adds an error to the feedback signal. By clocking the latches at the input of the DAC by a delayed clock, the signal glitches are effectively removed [59]. The delayed clock was generated using inverter-based delay cells from the standard cell library. The clock delay was between 2 ns and 5 ns when including process and temperature variations.

The clock delay increases the excess loop delay of the modulator. From simulations it was found, that the modulator could handle an excess loop delay up to 20 ns before becoming unstable. Thus, with a maximum clock delay of 5 ns, excess loop delay compensation was not considered necessary.

With 7 output levels the DAC is not inherently linear, as is the case for the single-bit DAC. The non-linearity may be compensated for by applying dynamic element matching (DEM) to the DAC. With DEM then instead of using the same current unit cell when e.g. feeding back a value of 1, either one of the three unit cells is used. The selection is based on a randomization algorithm, effectively scrambling the distortion generated by the DAC and converting it to wide-band noise [51]. However, the use of DEM increases the excess loop delay of the modulator and increases the design complexity of the DAC. Thus, instead of applying DEM it was decided to improve the linearity of the DAC via a well matched layout.

6.4 Tuning of STF

The use of current mode feedback with the active-RC integrator, results poor matching between the input coefficient k_b and the feedback coefficient k_a. The feedback current is based on a reference current generated on-chip from a bandgap voltage reference and a resistor. However, the resistor used for the current reference and the active-RC integrator may not be of the same type, same value or

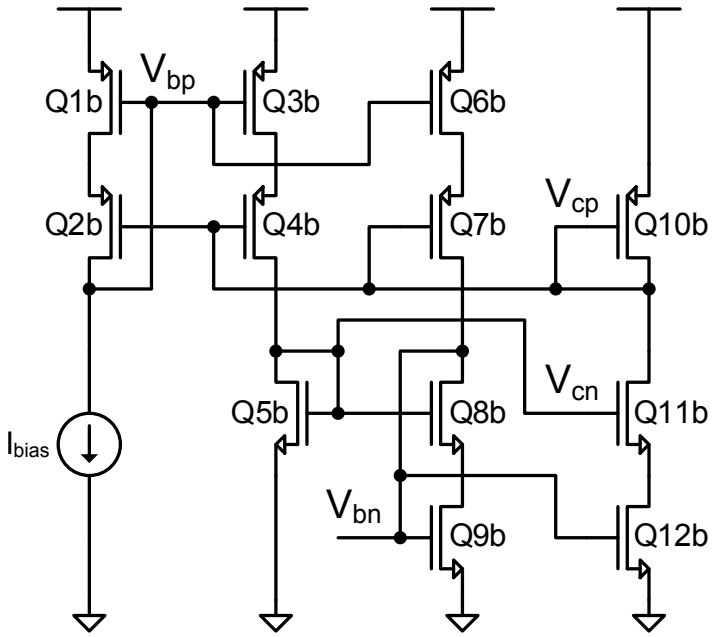


Figure 6.15: Schematic of DAC biasing circuit

Table 6.6: Summary of DAC biasing circuit properties

Property	Value	Property	Value
$\left(\frac{W}{L}\right)_1$	$8 \cdot \frac{8.730\ \mu m}{10.0\ \mu m}$	$\left(\frac{W}{L}\right)_7$	$20 \cdot \frac{2.795\ \mu m}{2.0\ \mu m}$
$\left(\frac{W}{L}\right)_2$	$20 \cdot \frac{2.795\ \mu m}{2.0\ \mu m}$	$\left(\frac{W}{L}\right)_8$	$20 \cdot \frac{1.360\ \mu m}{4.5\ \mu m}$
$\left(\frac{W}{L}\right)_3$	$8 \cdot \frac{8.730\ \mu m}{10.0\ \mu m}$	$\left(\frac{W}{L}\right)_9$	$8 \cdot \frac{5.025\ \mu m}{26.68\ \mu m}$
$\left(\frac{W}{L}\right)_4$	$20 \cdot \frac{2.795\ \mu m}{2.0\ \mu m}$	$\left(\frac{W}{L}\right)_{10}$	$2 \cdot \frac{2.795\ \mu m}{2.0\ \mu m}$
$\left(\frac{W}{L}\right)_5$	$2 \cdot \frac{1.360\ \mu m}{4.5\ \mu m}$	$\left(\frac{W}{L}\right)_{11}$	$20 \cdot \frac{1.360\ \mu m}{4.5\ \mu m}$
$\left(\frac{W}{L}\right)_6$	$4 \cdot \frac{8.730\ \mu m}{10.0\ \mu m}$	$\left(\frac{W}{L}\right)_{12}$	$8 \cdot \frac{5.025\ \mu m}{26.68\ \mu m}$
g_{m3}	41.9 µA/V	g_{m9}	38.9 µA/V
I_{bias}	3.86 µA	I_{tot}	15.44 µA

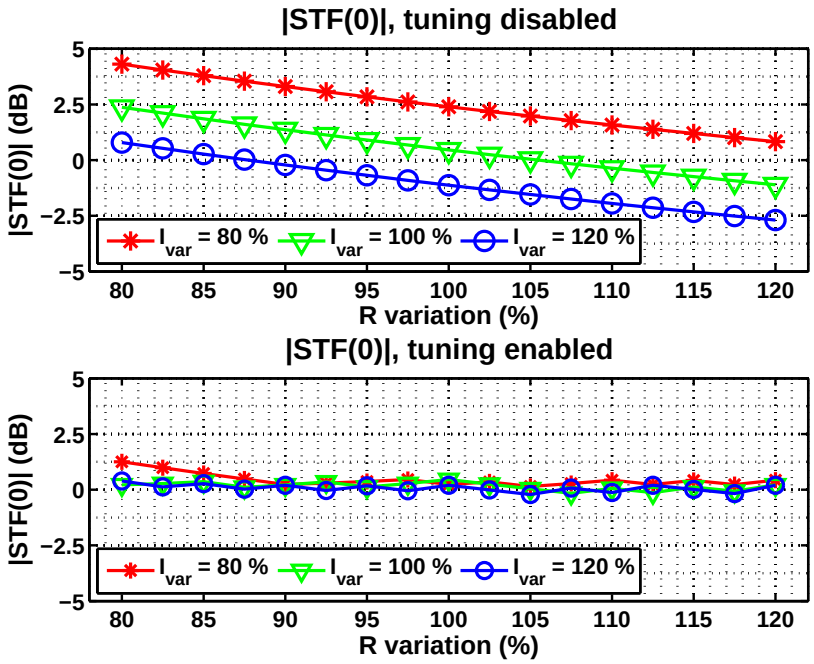


Figure 6.16: Variation of $|STF(0)|$ for variations of reference current (I_{var}) and resistor values, with tuning disabled (top) and enabled (bottom)

physical size. Furthermore, the two resistor may not be placed in the same area of the chip. Considering this, it can then be expected that the variation of the resistor values due to the variation in the fabrication process will be different for the resistors in the ADC and the resistor in the current reference block. This variation will result in a variation of signal gain in the modulator due to the variation of $|STF(0)|$.

In the context of the adaptive A/D conversion channel, the channel gain is directly affected by the variation of the ADC gain. Depending on the acceptable variation of the channel gain, it may be necessary to tune |STF(0)| for the CT $\Delta\Sigma$ modulator. This may be done by tuning the input resistor of the active-RC to match the feedback current, or alternatively tune the current to match the resistor value. As part of this PhD project a novel tuning method has been developed, that without the use of external references is able to tune the |STF(0)| with a relative accuracy $\pm 0.75dB$ of the target value. In Fig. 6.16 is shown the variation of |STF(0)| with the tuning method disabled and enabled, when the integrator resistors and feedback current varying by $\pm 20\%$. A patent application based on the tuning method has been submitted [82], but for confidentiality reasons it is not possible to explain the details behind the method. As a result, the patent application has not been included as part of this PhD thesis.

6.5 Other Circuit Considerations

Besides from the main circuit blocks, other blocks were used for the tape-out of the circuit. The 3-bit output of the quantizer was buffered digitally by three flip-flops clocked by the same delayed clock used for the current mode DAC. For driving the output of the test chip, three output buffers were placed after the flip-flops. For initializing the circuits in a known state at start-up, a power-on reset circuit was used; this circuit that generates a reset signal for a period of time after the supply voltages have ramped up to the final levels. The reset signal was used as input to a digital state-machine that generated the correct control signals for resetting the modulator subblocks.

The analog and digital parts of the modulator were supplied from separate supply lines. This was done in order to avoid injection of noise from the digital part to the analog part due to ripple on the supply line; both supply line voltages were generated off-chip and at 1.7 V. For generation of a reference current, a bandgap reference bias block was used. This was needed in order to evaluate the impact of variations of the reference current on the performance of the ADC due to variations in the DAC feedback current. Voltage references for the Flash ADC and for the common-mode reference, were generated based on resistor strings and an off-chip reference voltage.

MOSFET transmission-gate switches were placed at the input of the modulator, as part of the circuit for tuning the STF of the modulator. Since the switches are placed in front of the resistors of the 1st integrator, the maximum voltage across the switches almost equals the maximum input level. Due to the non-linearity of the switches and the large signal swing, the switches generate harmonic distortion that is injected directly at the modulator input; Thus, the distortion is not noise shaped. However, the resulting distortion was found to be acceptable. This will be discussed further in Sec. 6.6.1.

6.5.1 Layout Considerations

A die photo of the fabricated test chip is shown in Fig. 6.17. For the layout of the circuits, the primary concern was having a symmetrical layout for the fully-differential integrators. Each OTA has a separate bias circuit, to achieve good matching between the bias blocks and the OTAs. Furthermore, to avoid injection of noise from the digital circuits to the input of the modulator via the substrate, the digital blocks were placed near the output of the modulator. The current mode DACs also required good matching in order to achieve good linearity and the correct feedback current. As a result, the bias circuit was repeated for each DAC despite the increase in the total current consumption of the CT ΔΣ ADC.

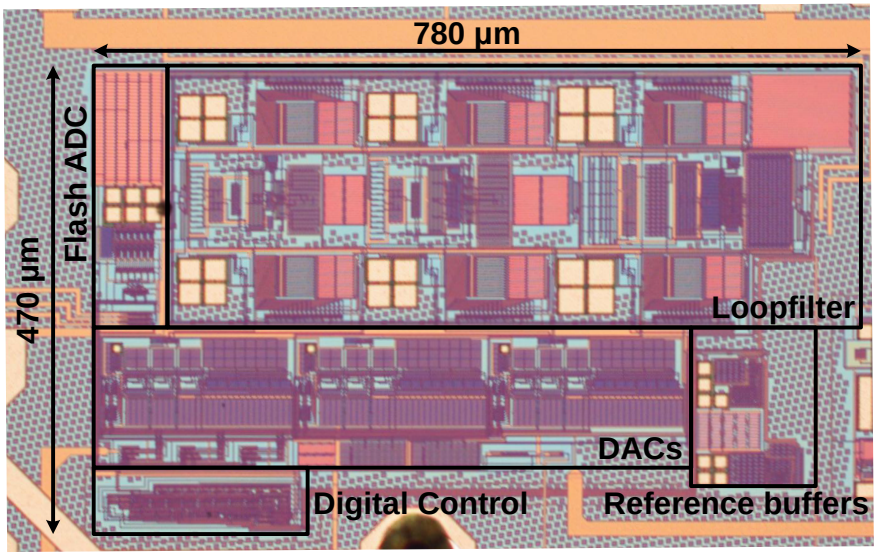


Figure 6.17: Die-photo of the fabricated test IC, with modulator input on the right side and output on the left

6.6 Evaluation

6.6.1 Simulation results

6.6.1.1 Noise Results

The designed CT ΔΣ ADC was prior to tape-out evaluated with simulations using to estimate the expected performance of the fabricated circuit. For evaluation of the noise performance, the CT ΔΣ ADC was simulated using the models from the process design kit (PDK) for all passive components, the 1st integrator, and the 1st DAC, while the remaining blocks were modeled using Verilog-AMS. This was done in order to reduce the simulation run-time, and was considered sufficient, as noise from the other circuit blocks would be noise shaped by the modulator. The simulations were carried out using an input sine wave with a frequency of 2 kHz instead of the more commonly used 1 kHz frequency, also in order to reduce the simulation run time. The ADC output was dumped to a data file and analyzed using MATLAB.

A plot of the PSD of the simulated modulator output is shown in Fig. 6.18 for a high and a low input level. The variation in the noise floor, due to the input level dependent noise of current mode DAC, can clearly be seen from the plot. A plot of the SNR and the signal to noise and distortion ratio (SNDR) as a function of the modulator input level is shown in Fig. 6.19. As seen from the figure, for low input levels the SNR increases with the input level with an almost constant slope. However, at -30 dBFS the slope of the curve drops and the SNR saturates at 75 dB. Similarly, for the SNDR curve, it stops increasing at -30 dBFS, drops

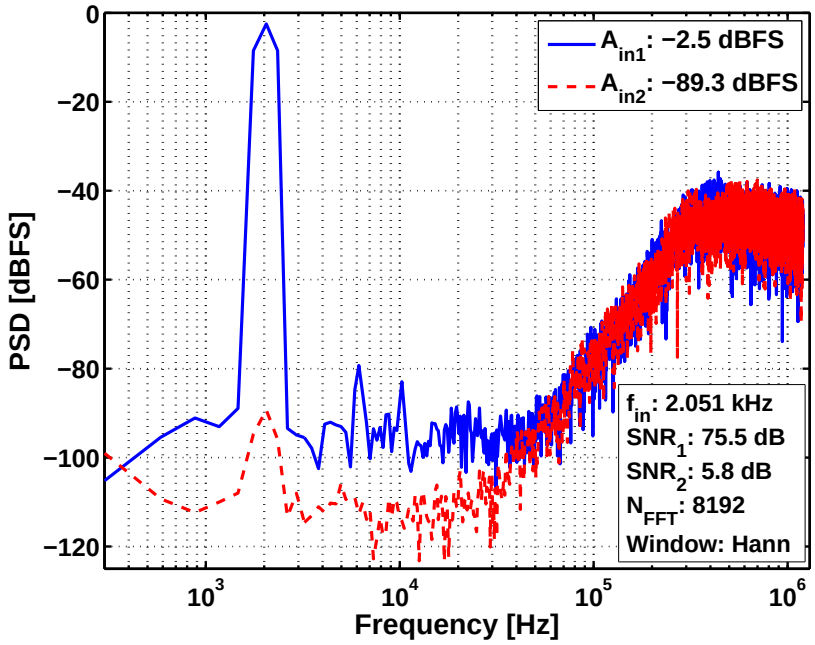


Figure 6.18: PSD of simulated ADC output, using averaging of two simulations

below 70 dB and ends at 72 dB. The drop in the SNDR curve is assumed to be caused by the switches at the input of the modulator. The modulator THD as a function of the input level is shown in Fig. 6.20, showing that the minimum THD is almost 0.01 %. This is not an impressive result, but in the context of a MEMS microphone for audio, it is considered acceptable. It should be noted that the distortion caused by non-linearities are not present in the simulation, but are expected to further increase the minimum THD. From the THD curve it can also be seen, that around -30 dBFS the THD increases but then drops again, as it was also observed for the SNDR plot. The reason why the THD drops again as the modulator input is increased further, is unknown at the time of the writing of this thesis.

Returning to Fig. 6.19, it may be seen that the dynamic range of the modulator is around 95 dB, which is significantly higher than the peak SNR achieved. At first, the low peak SNR may be explained by the noise of the current mode DAC being dependent on the input level. In order to verify this, the SNR of the CT ΔΣ ADC was estimated based on the noise of the 1st integrator and the noise of the DAC; the DAC noise was estimated based on the noise factor for the modulator. The resulting curve is plotted in Fig. 6.21 together with the simulated SNR curve. As seen from plot, the SNR estimate fits well with the simulated noise for input levels below -30 dBFS. However, the saturation in SNR does not match the estimated SNR. Based on this observation, the low SNR at the high levels is not due to the increased noise from the current unit cells following from the increased activity cells.

At the time of the design, the cause of this problem was not identified and no solution found. However, a possible explanation may be given from the work

presented in [83], published in July 2015. In this paper it is shown that the offset at the input of the integrator OTA will result in charged and discharged of the parasitic capacitances at the positive and negative output nodes of the current cells when connected to a node with a different voltage: either switching from the positive to the negative input of the OTA, or switching to the internal node reference node of the DACs. As the activity of the current cells increases, thereby switching more often between the different nodes, the parasitic capacitors will get charged or discharged more often. Every time this occurs, an error is generated in the feedback signal. Since the error is not common on both output nodes of the DAC, it is present in the output as differential noise.

As seen in Fig. 6.6a, p. 108, there is increased activity of the current cells for modulator input levels above -20 dBFS. At -30 dBFS the zero feedback signal is still dominant, but the activity shown in this plot may not show the full picture. Even though the zero feedback signal occurs most often, the single unit cell may be switched to and off the OTA input more often. Due to the voltage differences this may cause an increase in the noise floor, as described in [83].

An alternative explanation for the increased noise floor at the high input levels, is that the noise of the common-mode reference voltage buffer has an impact on the noise performance, contrary to what was expected when the circuit was designed. The noise generated by the buffer will be stored on the parasitic capacitances at the drain nodes of Q3 and Q4 in the current cells. As the activity of the modulator and DAC increases, the current cells are switched on and off more often, thus more often sampling the noise from the buffer. In effect the buffer noise is sampled on the parasitic capacitances, but with an aperiodic sampling clock. This hypothesis has not yet been tested, and further investigations are required in order to determine the cause of the reduced SNR at high input levels.

No simulations for evaluation of the jitter performance was carried out, due to the lack of a verified model of a clock generator with a known clock jitter. Instead, a theoretical estimate was used for determining the maximum allowed clock jitter in order to achieve the required noise performance. In [69] an expression for the theoretical jitter noise for a multi-bit CT $\Delta\Sigma$ ADC is given as:

$$SNR_{\text{jitter}} = \frac{V_{FS}^2}{2} \cdot \frac{OSR}{\alpha^2} \cdot \left(\frac{1}{f_s \sigma_{\Delta T}} \right)^2 \tag{6.6}$$

where α is an activity factor dependent on the feedback waveform and the number of quantization levels, and $\sigma_{\Delta T}$ is the jitter of the sampling clock. The value of α may be estimated from simulations of the modulator without clock jitter, and for a NRZ DAC waveform it is given as:

$$\alpha^2 = \sum_{n=1}^{N} \frac{(v(n) - v(n-1))^2}{N} \tag{6.7}$$

where N is the total number of samples, and $v(n)$ is the modulator output for sample n. From simulations of the modulator for a 1 kHz input signal at the MSA, the value of $alpha^2$ was estimated to equal 0.2. From the noise budget in

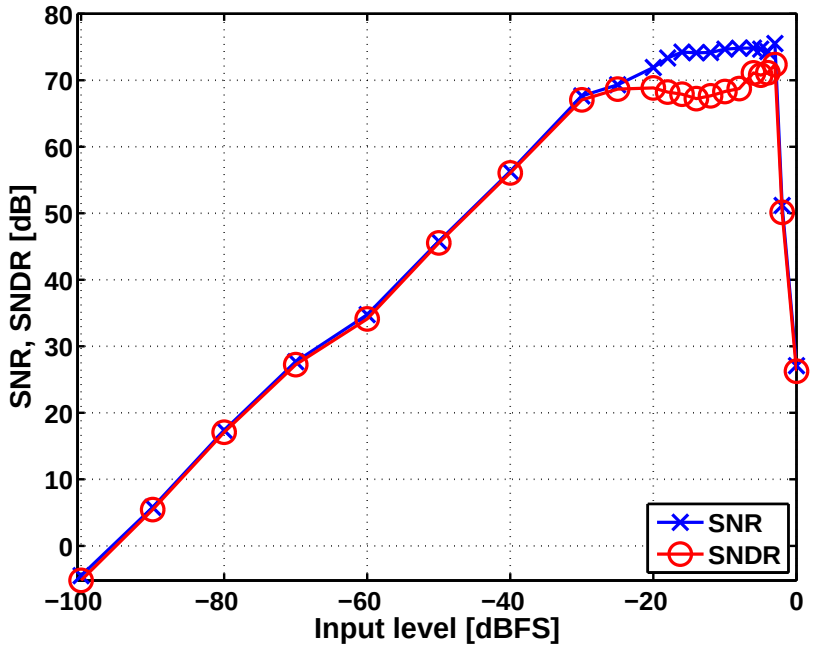


Figure 6.19: Simulated SNR and SNDR as a function of the modulator input level

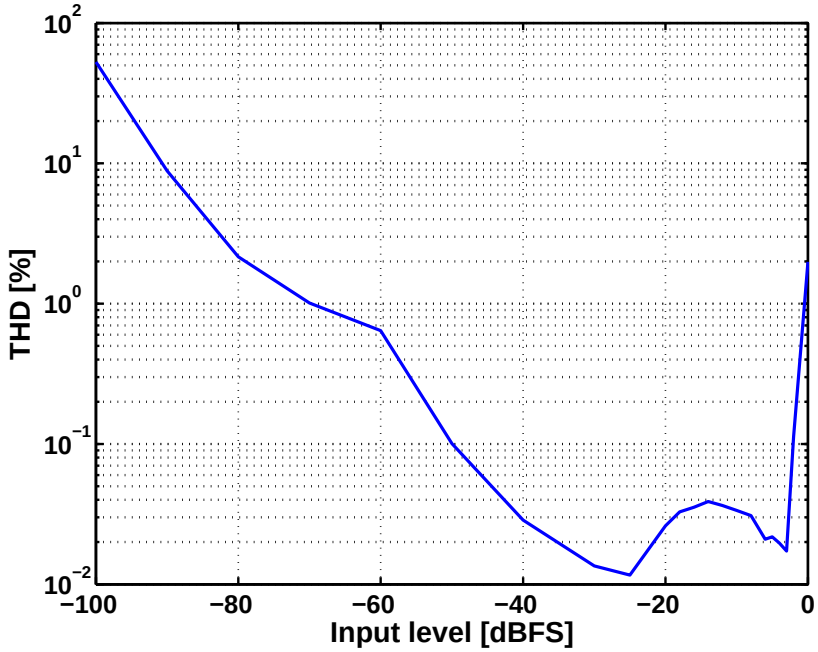


Figure 6.20: Simulated THD as a function of the modulator input level

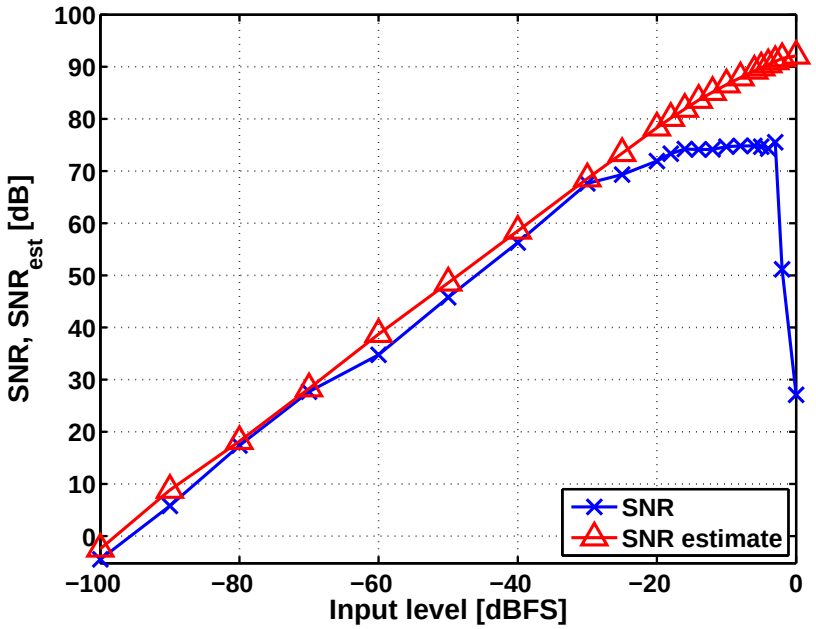


Figure 6.21: Simulated SNR and estimated SNR based on noise of 1st integrator and 1st feedback DAC

Table 6.1, the peak SNR for the jitter noise is 98 dB. Inserting these numbers into (6.6) the maximum clock jitter is found to equal 99 ps. This value of the clock jitter was then taken into account during the evaluation of the fabricated IC.

6.6.1.2 Current Consumption

The simulated current consumption of the CT ΔΣ ADC, under typical process and temperature conditions, is summarized in Table 6.7. The current consumption of the current reference generator and power-on reset circuit are also listed. As seen the table the loopfilter is dominant part of the modulator with respect to the current consumption, consuming a total of 173 μA, with half of this current consumed by OTA1. The current mode DAC consumes also consumes approximate 1/3 of the total current, with each DAC consuming roughly 31 μA. A large of part of this is due to the biasing circuit that was replicated in each feedback DAC. Furthermore generation of internal bias currents from the on-chip current reference and the buffer for the common-mode reference voltage further adds to the current consumption of the DAC. The quantizer and the digital blocks consume only a minor part of the total current consumption.

The simulated performance of the CT ΔΣ ADC under typical conditions is summarized in Table 6.8, also listing the total active area of the ADC.

Based on the simulated current consumption, the resulting FoM for the CT ΔΣ ADC may be calculated. The FoM is given in (5.12), and is repeated here for

Table 6.7: Overview of modulator current consumption, total and for subblocks

Property	Value	Percentage
i_{tot}	282.7 µA	-
i_{OTA1}	92.8 µA	32.8 %
i_{OTA2}	43.4 µA	15.5 %
i_{OTA3}	37.2 µA	13.1 %
$i_{\text{quan.}}$	9.2 µA	3.2 %
i_{DACs}	94.7 µA	33.5 %
i_{other}	5.4 µA	1.9 %
i_{AVDD}	278.9 µA	98.7 %
i_{DVDD}	3.8 µA	1.3 %
i_{iref}	18.8 µA	-
i_{POR}	2.0 µA	-

Table 6.8: Summary of simulated performance of the CT ΔΣ ADC in typical process corner at 27°C

Parameter	Value
Supply voltage / Process	1.7 V / 0.18 µm
Bandwidth / Sampling frequency	20 kHz / 2.4 MHz
Current consumption	284 µA
MSA / Peak SNR amplitude	-0.6 dBFS / -2.5 dBFS
Dynamic range / SNR / SNDR	95.0 dB / 75.7 dB / 72.4 dB
Active area	0.37 mm^2

reference:

$$FoM = \frac{P_{mod}}{2^{ENOB} \cdot 2f_B} \tag{6.8}$$

In most papers the ENOB is surprisingly based on the dynamic range of the ADC, in which case the designed ADC achieves a FoM of 262 fJ/conversion. If instead the ENOB is based on the peak SNR, the resulting FoM is 1.97 pJ/conversion.

In Table 6.9 the FoM based on the dynamic range is compared with the state-of-the-art CT ΔΣ designs for audio applications. As seen from the table, the FoM achieved with the presented CT ΔΣ ADC is in the same range as the state-of-the-art, but still far from the excellent work by S. Pavan [60, 61, 84]. In [60] the low current consumption is achieved by the design of very low power subblocks, including the integrators. In [84] the ADC uses a FIR feedback DAC, which relaxes the linearity requirements of the 1st integrator; the OTA is implemented using a two-stage feedforward compensated architecture. Both methods significantly

Table 6.9: Comparison of FoM with other audio CT ΔΣ ADCs

Reference	Tech.	BW	Dynamic range	Power	FoM [fJ/conv.]
[60]	180 nm	24 kHz	93.5 dB	90 μW	49
[84]	180 nm	24 kHz	103 dB	280 μW	61
[61]	180 nm	24 kHz	92.5 dB	110 μW	67
[85]	40 nm	24 kHz	101 dB	1.7 mW	386
[86]	180 nm	20 kHz	101.3 dB	1.1 mW	290
[87]	130 nm	20 kHz	83 dB	60 μW	130
This work, simulated	180 nm	20 kHz	95.0 dB	482 μW	262

reduce the current consumption of the OTA. In [61] the designed ADC uses an assisted OpAmp technique that relaxes the slew-rate and speed requirements of the OTA in the 1st integrator; this is done by using a transconductor stage to assist the OpAmp with charging and discharging the integrator capacitors, thereby reducing the ripple on the input nodes of the OTA without requiring a high speed OTA.

Based on the results achieved in [60, 61, 84] it is clear, that in the designed CT ΔΣ ADC a lower total current consumption could have been achieved if another OTA topology had used instead of the folded-cascode. At the time of the design this was considered as an option. However, the folded-cascode OTA was selected as it was a well-known OTA topology.

For the future work of the project, it is highly relevant to investigate the use of more advanced low power OTA topologies, in order to improve the designed CT ΔΣ ADC. The improvements achieved by using current mode feedback are still valid, as the noise reduction of the OTA noise is independent of the choice of OTA topology.

6.6.1.3 Corner Simulations

The performance of the designed CT ΔΣ ADC was evaluated in the PVT corners using transient simulations of the ADC; all circuit blocks were modeled using transistor level models and simulated without circuit noise. The results are summarized in Table 6.10. As seen from the results, the SNR drops dramatically when both resistors and capacitors are in the fast process corner; the corners #2-#4, #8, and #10. At the time of the tape-out of the circuit, the cause of this problem was unknown; since it only occurred in the fast corner for the resistors and capacitors, it was expected to not impact the performance of the fabricated test chip.

In the fast corner both resistors and capacitors are at their minimum value. From the expression for the loopfilter coefficients realized with an active-RC integrated, given in (5.16), p. 81, for reduced resistor and capacitor values the loopfilter

coefficient increases, which may lead to instability. When designing the loopfilter, the coefficients were scaled in order to handle this extreme case. The hypothesis is that this scaling was insufficient; this has partially been confirmed by inspection of signal output of the 1st integrator from the simulations in the critical corners. Here it was observed, that the 1st integrator output saturates and clips; this in spite of the feedforward of the modulator input to the output of the 1st modulator.

In the slow corner for the resistor and capacitor, it can be seen that the SNR is up to 10 dB lower than in the typical corner. However, when using an A-weighting filter for the SNR calculation, the change in SNR is not as significant; for corner #5 the A-weighted SNR is even better than for the typical corner. In the slow corner, the resistors and capacitors are at the maximum value, and thereby are the loopfilter coefficents reduced; this leads to a reduction of the corner frequency of the loopfilter. The results of the corner simulations indicate, that due to the NTF being shifted down in frequency, some of the noise in the band of interest is amplified by the NTF to a level above the noise floor. When applying the A-weighting filter, the higher frequency content is attenuated this counteracting this increased noise when calculating the SNR.

Based on the issues for both the fast and the slow corner of the passive components, it would seem that the scaling method applied is insufficient in handling the process variations. It would thus be a better choice to use regular tuning of the loopfilter coefficients rather than scaling them.

In Table 6.10 is also listed the total current consumption of the CT ΔΣ ADC, which varies from 223 μA to 356 μA. This variation is due to the variation of the reference current generated on-chip from a bandgap voltage reference and a resistor. Thus, the current consumption varies with the process corner of the resistors as expected.

6.6.2 Measurements

6.6.2.1 Measurement Setup

A PCB was developed for evaluation of the fabricated test IC. Reference voltages used in the IC were generated on the PCB using linear voltage regulators with filtered outputs. The PCB is shown in Fig. 6.22.

For the measurement of the test IC, the following test equipment was used:

- Audio signal generator: Rohde & Schwartz UPV Audio Analyzer
- Clock generator: Agilent 81104A Pulse Generator
- Power Supply Unit: Rohde & Schwartz Hameg HMP2020
- Multimeter: Hewlett Packard 34401A
- Oscilloscope: LeCroy Waverunner 620 Zi

Table 6.10: Simulated performance of the designed CT ΔΣ ADC in PVT corners for -15 dBFS input signal

	MOS	BJT	R,C	Temp	VDD	SNR	THD	I_{tot}
#1	TT	TT	TT	27 °C	1.7 V	84.7 dB, 87.9 dB(A)	0.35 %	284 µA
#2	FF	FF	FF	-40 °C	1.7 V	52.0 dB, 54.0 dB(A)	0.05 %	356 µA
#3	FF	FF	FF	27 °C	1.7 V	45.5 dB, 49.8 dB(A)	0.19 %	356 µA
#4	FF	FF	FF	85 °C	1.7 V	45.2 dB, 48.7 dB(A)	0.31 %	356 µA
#5	SS	SS	SS	-40 °C	1.6 V	72.9 dB, 89.9 dB(A)	1.48 %	223 µA
#6	SS	SS	SS	85 °C	1.6 V	74.7 dB, 85.6 dB(A)	0.14 %	231 µA
#7	SF	TT	FF	-40 °C	176 V	72.9 dB, 76.5 dB(A)	0.10 %	342 µA
#8	SF	TT	SS	85 °C	1.6 V	77.4 dB, 83.9 dB(A)	0.11 %	232 µA
#9	FS	TT	FF	-40 °C	1.7 V	56.5 dB, 60.0 dB(A)	0.08 %	346 µA
#1	FS	TT	SS	85 °C	1.6 V	77.0 dB, 80.5 dB(A)	0.04 %	231 µA

- Logic Analyzer: LeCroy MS-250

The input signal was generated using the signal generator of the R& S UPV, and the digital output was measured using the LeCroy MS-250 logic analyzer, capable of sampling data at 250 MHz. Using the LeCroy oscilloscope, the data from the logic analyzer was exported to a data file and imported into MATLAB for further analysis. From the equipment list, the pulse generator is of special interest. With a clock jitter in the range of 80 ps at a pulse frequency of 2.4 MHz, this was generator was used in order reduce the impact of jitter noise on the measurements. A block diagram of the measurement setup is shown in Fig. 6.23.

6.6.2.2 Noise Measurements

The evaluation of the noise performance of the fabricated CT ΔΣ ADC was carried out using a 1 kHz sine wave input signal, generated using the differential signal generator in the R& S UPV audio analyzer. The measured SNR and SNDR as a function of the input level are shown in Fig. 6.25, showing a peak SNR of only 30 dB. The PSD of the ADC output for an input level of -15 dBFS is shown in Fig. 6.24, clearly showing the high noise floor. The peak in the noise floor at 500 kHz, indicates that the output is noise shaped by the loopfilter, and thus

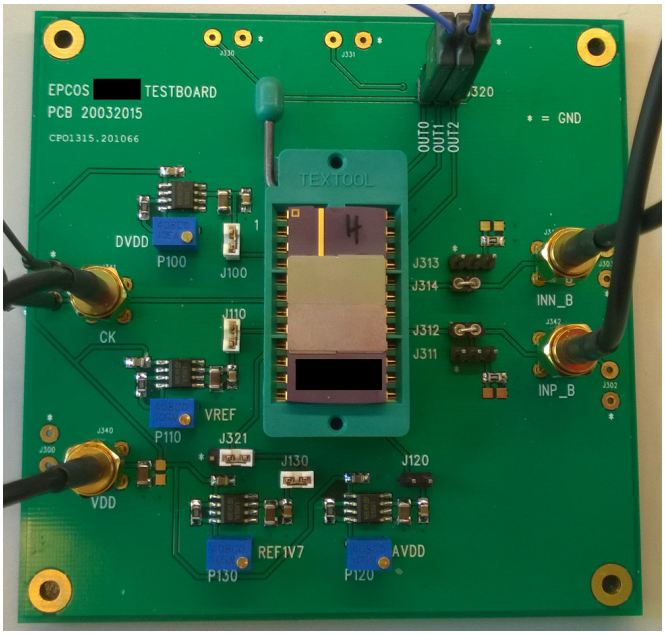


Figure 6.22: Test PCB for evaluation of the test IC

that the modulator is operating. Furthermore, the SNR improves with increasing input level, further indicating that the input signal is modulated by the ADC.

Based on an analysis of the output data from the 6 test ICs it was found, that in the 3-bit output stream an output value of -4 was present. For the combinational logic used for the generation of the 2's complement output of the quantizer, an output value of -4 would not possible. Due to the occurrence of this incorrect output value, the quantizer was considered to be the possible source of the problem.

To further analyze the problem, a simulation model of the Flash ADC was generated that included the parasitic extracted (PEX) resistors and capacitors based on layout of the Flash ADC. This model was used in a transient simulation of the CT ΔΣ ADC, where all other circuit blocks where modeled using the transistor level schematic models and without circuit noise. The modulator was simulated for a -15 dBFS input signal at 2 kHz, and the resulting PSD of the output is shown in Fig. 6.26. As seen from the plot, the noise floor of the modulator output was quite high, similar to the results observed from the measurements. Further analysis of the Flash ADC using the PEX model showed, that the settling time of the Flash ADC was in the range of the delay DAC clock in comparison to the quantizer sampling clock; the delayed clock was used for clocking both the latches of the DAC and the flip-flops in the digital output buffer. Due to this increased delay of the Flash ADC, the time between the arrival of the data at the input of the flip-flops and the rising edge of the delayed clock was sometimes smaller than the setup time of the flip-flops. Thus, in some cases the flip-flops did not read the input data correctly. Since the three output bits of the Flash ADC have different

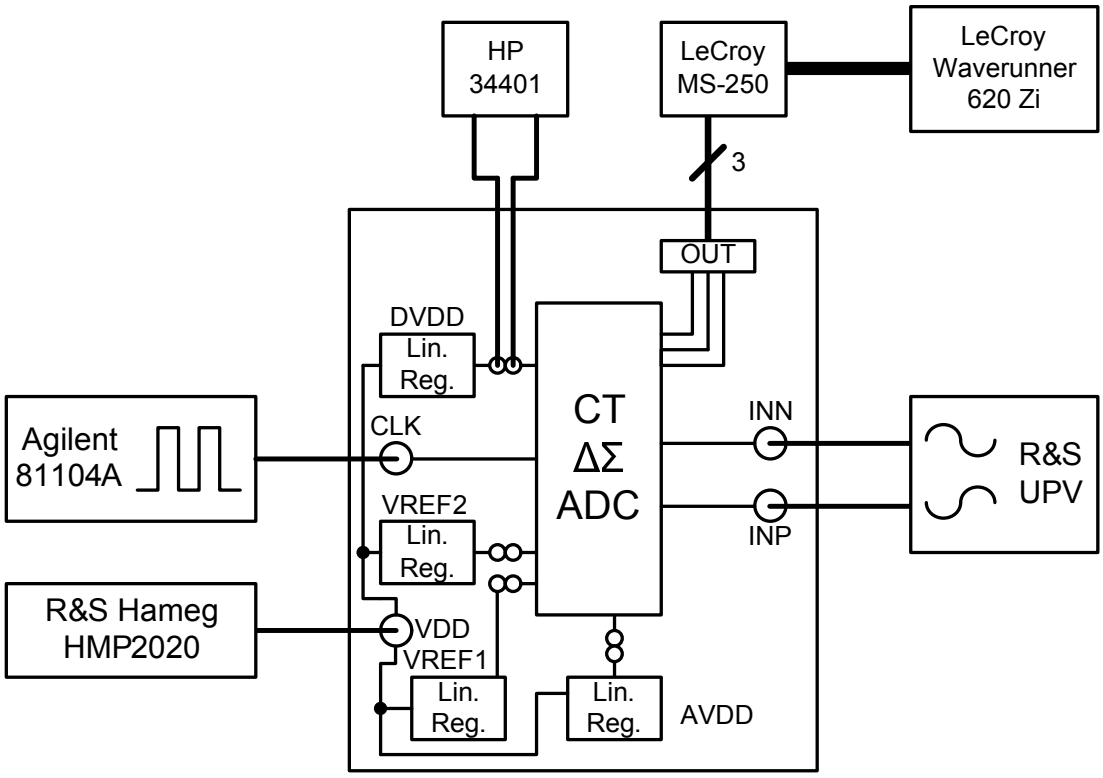


Figure 6.23: Block diagram of measurement setup for evaluation of test IC

settling time, depending on the output of the comparators, it is may occur that only some of the data bits are read correctly by the flip-flops.

For the input of the DAC latches were used instead of flip-flops, and thus a delayed arrival of some of the data-bits only results in a temporary error in the feedback signal until all output data bits of the Flash ADC have settled. Thus, while the output data of the ADC could not be correctly measured, the modulator may still be operating correctly. However the noise performance would still be degraded due to the short error signals in the feedback DAC. To verify this hypothesis, a transient simulation was carried out for the CT $\Delta\Sigma$ ADC without circuit noise, with the PEX model of the Flash ADC, and with the flip-flops removed from the digital output buffer. The resulting PSD of the simulated output is shown in Fig. 6.27, from it can be seen that the SNR is significantly improved. To further improve the SNR, an identical transient simulation was carried out where the delay of the DAC clock signal was doubled. The resulting PSD of the output is shown in Fig. 6.28, showing a further improvement in the SNR. The results of the simulation thus verified the assumption of the Flash ADC being the cause of the problem.

The Flash ADC was designed using minimum sized transistors, and the layout was not considered to be critical; both decisions proved to be bad.

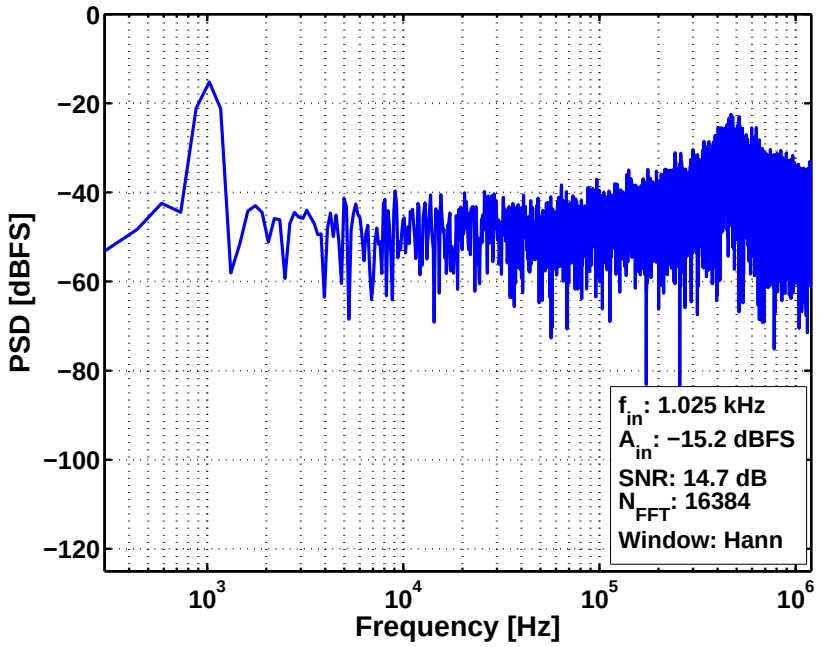


Figure 6.24: PSD of measured output

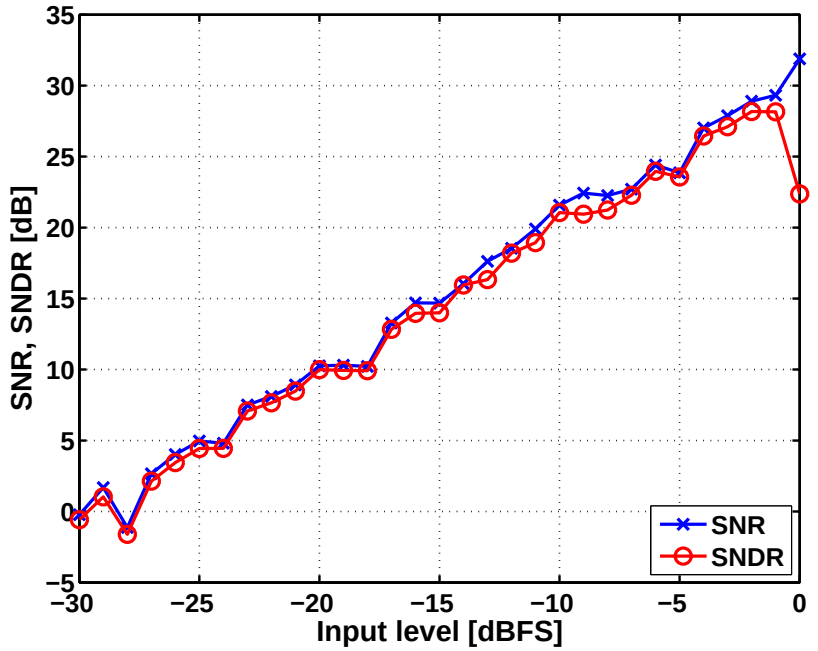


Figure 6.25: Measured SNR and SNDR as a function of the modulator input level, for input sine wave at 1 kHz

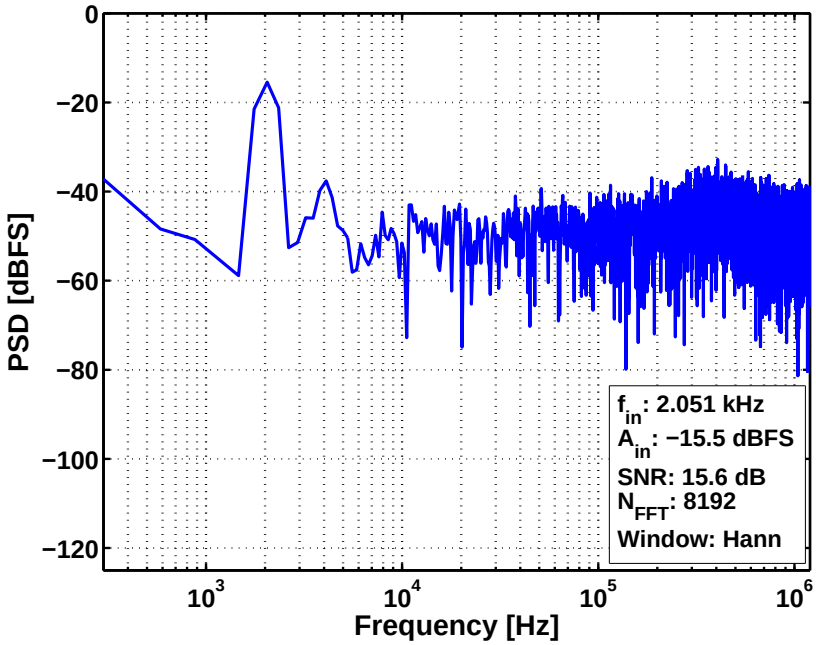


Figure 6.26: PSD of simulated CT ΔΣ ADC output, with PEX model for the Flash ADC and without circuit noise

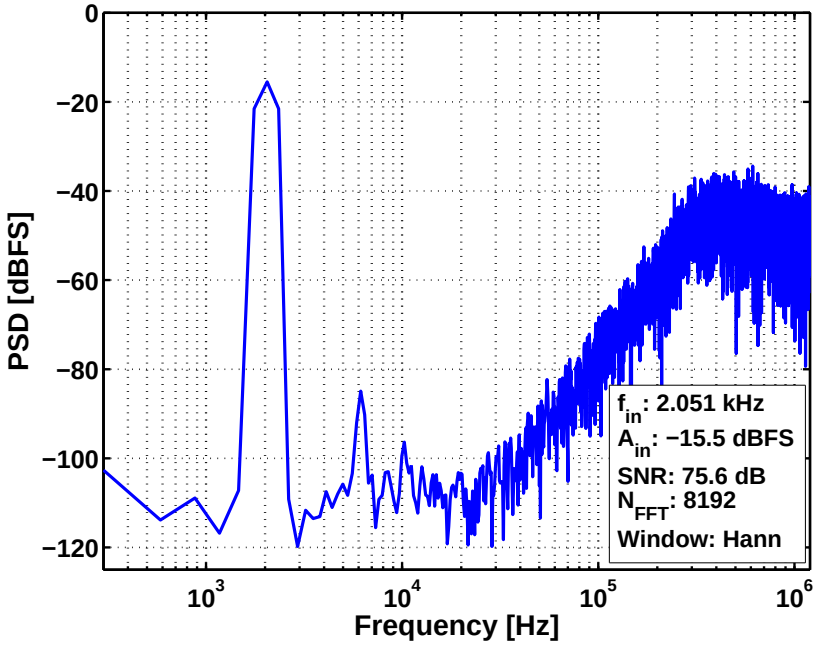


Figure 6.27: PSD of simulated CT ΔΣ ADC output, with PEX model for the Flash ADC, without circuit noise, and without flip-flops in output buffer

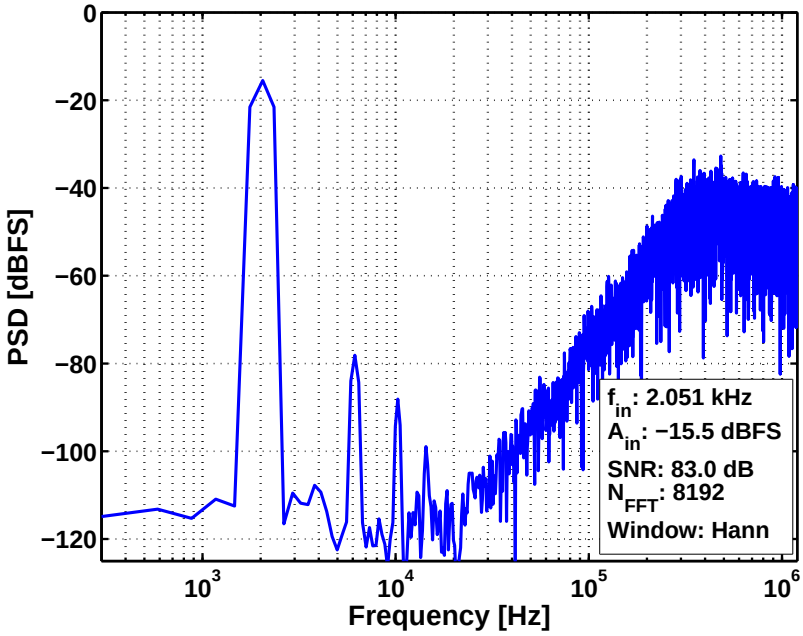


Figure 6.28: PSD of simulated CT ΔΣ ADC output, with PEX model for the Flash ADC, without circuit noise, without flip-flops in output buffer, with doubled time delayed of DAC clock

6.6.2.3 Current Consumption

The current consumption for the AVDD and DVDD supplies was measured for 6 test chips, and the results are summarized in Table 6.11. Comparing the measured values with the simulated values listed in Table 6.7, the analog current consumption is close to the simulated value; when taking the current consumption of the current reference and power-on reset circuits, the measured current was approx. 12 % below the simulated values in the typical process corner. The measured digital current consumption was much larger than simulated, by a factor of more than 20 when comparing with the simulated value of 3.8 μA under typical conditions.

Generally, the digital power consumption may be split into two parts: a static part and a dynamic part. The dynamic current consumption relates to the charging and discharging of capacitances, including gate capacitance of the MOSFET transistor in the CMOS standard cell and parasitic capacitances. The dynamic current consumption may be estimated as [24]:

$$I_{\mathrm{DVDD,dynamic}} = \alpha C_L V_{DD} f_{sw} \tag{6.9}$$

where α is an activity factor indicating the average number of switching events in each clock cycle, C_L is the load capacitance, V_{DD} the supply voltage, and f_{sw} the clock switching frequency. Since the digital circuits were implemented using CMOS standard cells, the static current consumption is only related to the leakage current of the transistors, and is independent of the switching frequency.

Table 6.11: Measured modulator current consumption, based on 6 chips

Supply	I_{avg}	$\hat{s}$
AVDD	270.0 µA	5.0 µA
DVDD	81.2 µA	11.7 µA
AVDD + DVDD	355.7.0 µA	10.4 µA
Digital Current Consumption of Chip #4		
$I_{\text{DVDD,static}}$	23.7 µA	
$I_{\text{DVDD,dynamic}}$	59.6 µA	
$C_{L,\text{eq}}$ for $\alpha = 0.5$	29.2 pF	

The total digital current consumption may then be calculated as:

$$I_{\text{DVDD}} = I_{\text{DVDD,static}} + I_{\text{DVDD,dynamic}} \tag{6.10}$$

To further investigate this behavior, for one of the test chips the digital current consumption was measured when the sampling frequency for was swept between 1.20 MHz and 4.8 MHz in steps of 240 kHz. The measured change in current consumption was linear with the change in frequency, and by extrapolation of the linear relation to a switching frequency of 0, the static current consumption was extracted from the measurement data. Based on the static current consumption and the total digital current consumption, the dynamic current consumption was calculated from(6.10). The resulting static and dynamic current consumptions for the measured chip are also listed in Table 6.11. The static current consumption is very high, considering that 0.18 µm technology was used for the design. Since the chip was found to be operating correctly with modulation, it is believed that there are no short-circuits in the digital blocks due to fabrication errors. A possible explanation is, that there may be a problem with the electrostatic discharge (ESD) protection cells connected to the digital supply line.

From the measured dynamic current consumption, the equivalent load capacitance was found by assuming an activity factor of 0.5. From (6.9), an equivalent load capacitance of 29 pF was found. This is a quite large load capacitance, which can not be explained by parasitics from the layout of the digital standard cells. The measurements were repeated without the logic analyzer probes connected to the PCB, without a change in the current consumption. The dynamic current consumption may then be explained by the loading of the digital output buffers by the output ESD protection cells. Unfortunately it was not possible to simulate the load of the ESD protection cells, due to an error in the transistor level models of the ESD cells.

6.7 Summary

In a CT ΔΣ ADC the current consumption is dominated by the current consumption of the 1st integrator. Although the GBW and SR requirements of the integrator OTA are lower in a CT ΔΣ ADC in comparison to the DT equivalent, the noise requirement is still a concern that may lead to a high current consumption in the OTA.

In this chapter it was shown, that by combining the active-RC integrator with a current mode DAC for the feedback, the noise requirements of the integrator OTA are relaxed. This follows as a result of the high output impedance of the current mode DAC. The relaxed noise requirements makes it possible to reduce the current consumption of the 1st OTA, or alternatively reduce the current requirements of other parts of the ADC. It was also shown, that due to the noise of the multi-level current mode DAC being dependent on the modulator input signal level, it is possible to reduce the noise of the DAC at low modulator input levels, by using an odd number of quantization levels; in the presented design the use of a 7-level DAC reduced the noise of the DAC by 1 dB at low input levels compared to an 8-level DAC, due the zero feedback signal.

The design of a low power CT ΔΣ ADC with a current mode DAC was presented, with the design being based on the optimization method presented in Chap. 5. The designed circuit blocks for the ADC were described, highlighting the performance in comparison to the estimated performance from the optimization method. This showed that the current consumption estimated in the design optimization was too optimistic, as the designed OTA of the 1st integrator consumed 2.3 times more current than estimated. The main problem is the use of Schichmann-Hodges MOSFET model in the optimization method, as this model underestimates the current required to obtain a specific transistor transconductance. Furthermore, the impact of the flicker noise on the OTA biasing current is not part of the optimization method. Based on this, it is believed that a lower current design may have been achieved if the noise power of the 1st integrator was split more equally between the input resistors and the OTA.

The designed CT ΔΣ ADC was evaluated with simulations and by measurements on a fabricated prototype of the circuit. The simulation results showed that under typical conditions, the designed ADC achieved a dynamic range of 95 dB with a current consumption of 283 μA; the resulting FoM was 262 fJ/conversion, being in the range of the state of the art. In order to further improve the design, other OTA topologies should be investigated for replacing the folded-cascode OTAs used in the actual design. Corner simulations identified that in the fast process corner for the resistors and capacitors, the ADC becomes unstable with the result of significantly reduced performance. This was found to be due to insufficient compensation for the impact of process variations on the modulator loopfilter coefficients. Similarly, in the slow process corner for the passive components, the SNR is degraded due to a reduction of the loopfilter coefficients that leads to less aggressive noise shaping. Based on these observations, it is believed that tuning

of the filter coefficients is necessary to achieve sufficiently good performance in all process corners.

From the simulated current consumption of the circuit, it was found that the three feedback DACs consume 33 % of the total current consumption of the ADC. This was primarily due to the replication of the DAC biasing circuit in each feedback DAC, but also due to the biasing circuit adding noise to the output of the DAC. To reduce the noise of the biasing circuit, a large current was needed. Based on this observation, it is believed that a CIFF modulator topology would be a better solution than the CIFB topology used in the design, as the CIFF toplogy only uses a single feedback DAC. The total current consumption of the ADC may then be reduced by 20 %. For the CIFF topology, a summing circuit is needed in front of the quantizer, but since all non-idealities are 3rd order noise shaped, it is believed to be possible to design a low current block for this operation.

The measurements of the fabricated test IC showed issues related to the settling time of the Flash ADC used for the modulator quantizer; this in combination with the use of flip-flops in the digital output buffer resulted in a high noise floor that limited the peak SNR of the ADC to 30 dB. Simulations results showed, that by removing the flip-flops and by increasing the delay of the internally delayed clocked, used for clocking the DAC, the problem may be solved. Alternatively the comparators of the Flash ADC should be redesigned, to make them less sensitive to layout parasitics. The resulting increase in current consumption is considered to be acceptable, since the Flash ADC in the current design only consumes 2 % of the total current.

Measurements of the ADC current consumption also showed a total current consumption of 356 μA, with a digital current consumption 81 μA. Investigations showed issues with both a high static and a high dynamic current consumption from the digital voltage supply. This problem is believed to be related to the ESD protection cells used in the fabricated IC.

7

Conclusion

In this chapter the results of PhD are summarized and evaluated in a larger perspective. Furthermore, the future work of the project is described.

The PhD project documented in this thesis has focused on the investigated of the adaptive A/D conversion channel as a possible solution for achieving a digital MEMS microphone with a high dynamic range and with a low current consumption. The system level analysis showed that by using an AGC with the A/D conversion channel to adaptively adjust the gain configuration of the channel, the dynamic range of the channel is effectively extended beyond that of the ADC in the channel. The cost of the dynamic range extension is a peak SNR that is limited by the ADC, and furthermore the generation of transient glitches in the output signal of the conversion channel. The transient glitches are highly unwanted, as they may be audible when listening to the output signal.

In order to evaluate the audibility of the transient glitches, an objective method has been presented as an alternative to the use of subjective evaluations in the form of listening tests. The objective method is based on the ADB and MFPD model output variables from the PEAQ method, as these model the detectability of errors in an audio signal by a human being with normal hearing. From a comparison of the objective method with the results of a formalized listening test, it was found that the objective method may be used as a tool for evaluating the glitches generated in an adaptive A/D conversion channel during the development process of the channel.

The results of the listening test also showed, that in order to reduce the transient glitches to a level where they are no longer audible, it would be necessary to use very small gain adjustment steps when adjusting the gain settings of the adaptive A/D conversion channel. From both a circuit and system point of view this is not a feasible solution. An alternative method for reducing the transient glitches in the conversion channel output has been presented. The method replaces the conversion channel output by a linear estimate of the signal during the settling period of the channel gain. Thereby the transient glitches are effectively removed. The error generated from the linear estimate of the output signal was in a preliminary investigation found to be inaudible, thus solving the main problem of

using the adaptive A/D conversion channel in a digital MEMS microphone.

The use of the adaptive A/D conversion channel reduces the dynamic range requirements of the ADC, and thus the use of continuous-time $\Delta\Sigma$ ADCs in the conversion channel was investigated. For the design of low power continuous-time $\Delta\Sigma$ ADCs, a new optimization method was presented. The method uses a brute force search to design a large set of modulators, where both the NTF corner frequency and the number of quantization levels are swept. By relating the designed modulator to the circuit level implementation of the 1st integrator in the loopfilter, the minimum current solution can be found. Based on a design example it was shown, that the optimization method can be used as a good starting point when designing the circuits for the CT $\Delta\Sigma$ ADC.

As an additional way of reducing the current consumption of the CT $\Delta\Sigma$ ADC, the use of current mode feedback in combination with the active-RC integrator was investigated. An analysis was presented showing that by using current mode feedback the noise from the OTA of the 1st integrator may be significantly reduced. The resulting relaxed noise requirement of the OTA may then be used for reducing the overall current consumption of the CT $\Delta\Sigma$ ADC. The design of a 3rd order CT $\Delta\Sigma$ ADC with current mode feedback realized in a 0.18 µm process was presented. From the simulation results is was shown, that the ADC achieved a dynamic range of 95 dB while consuming 283 µA of current; this results in figure-of-merit of 262 fJ/conv, being in the range of the state-of-the-art. The simulated peak SNR was only 76 dB, due to higher noise at for large modulator input levels in comparison to the theoretical estimated value. The high noise is presumably due to errors in the feedback DAC signal, that are dominant at high modulator input levels where all current unit cells of the DAC are active.

When comparing with the state-of-the-art designs, a better FoM may be achieved by using another OTA topology than the folded-cascode. Furthermore, changing the loopfilter topology from CIFB to CIFF would reduce the current consumption of the DACs by 2/3. The results from corners simulations of the CT $\Delta\Sigma$ ADC showed degradation of the SNR, due to variations of the loopfilter coefficients. This was despite scaling of the coefficients in order to compensate for the process variations.

The designed CT $\Delta\Sigma$ ADC was fabricated, and measurement results showed very poor noise performance, only achieving a peak SNR of 30 dB. The settling time of the Flash ADC was identified as the cause of the problem, as the increased settling time resulted in incorrect sampling of the modulator output by the output buffers used on the chip. Measurement of the current consumption also showed, that the current consumption from the digital supply line was larger too high, presumably due to the ESD protection cells connected to the digital supply.

When evaluating the results of the project in a larger perspective, it is interesting to combine the use of the adaptive A/D conversion channel with the designed CT $\Delta\Sigma$ ADC. The analog MEMS microphone C928 by EPCOS [9] has a current consumption of 140 µA and a dynamic range of 107 dB. Combining the analog amplifier of this MEMS microphone with the designed CT $\Delta\Sigma$ ADC in the adap-

tive A/D conversion channel, it would be possible to achieve a similar dynamic range; this at a combined current consumption equal to approx. 425 μA based on simulation results. However, this does not include the current consumption of the digital blocks of the conversion channel. A large amount of digital signal processing is needed for signal filtering, reduction of the transient glitches, and the operation of the AGC block. Nevertheless, when compared with the competing digital microphones available in the market, the use of the adaptive A/D conversion channel is a very attractive method for achieving a digital microphone with both a high dynamic range and a low current consumption. The results of this PhD project are thus not only a contribution to the scientific community but also highly attractive from a business point of view.

7.1 Future Work

At the end of the project, further investigations are still required before the presented methods and design solutions are fully evaluated and developed. The following topics should be further investigated in the future:

- A further investigation of the use of the ADB and MFPD model output variables for use as objective measures of the audibility of the transient glitches generated by the adaptive A/D conversion channel. This in particular based on the results observed for the MFPD model when applied on the output of the adaptive A/D conversion channel with the glitch removal by output estimation.

- A more detailed evaluation of the ability of the glitch reduction by linear output estimation in removing the transient glitches effectively. A formalized listening test is required in order to verify that the errors generated by the method are not audible in the conversion channel output signal.

- An improvement of the CT $\Delta\Sigma$ ADC circuit analysis used in optimization method, where the current estimation based on the Schichmann-Hodges transistor model is replaced by an analysis based on the EKV-model. An expansion of the optimization method to also include the DAC noise and the impact of the biasing circuits when determining the minimum current solution. The theoretical estimate of the jitter noise may also be included as a design parameter.

- In the designed CT $\Delta\Sigma$ ADC, the modulator topology should be changed from CIFB to CIFF, to reduce current consumption required for the feedback DACs. The use of scaling of the loopfilter coefficients needs to be further investigated, and possibly replaced by regular coefficient tuning. The flip-flops should be removed from the digital output buffer, and the delay of the internally delayed clock signal used for clocking the DAC input latches should be increased to take the the longer settling time of the Flash ADC into account.

- The use of a more low power OTA topology for the integrators should be investigated, with the aim of further improving the FoM for the CT $\Delta\Sigma$ ADC.

- An investigation of the jitter sensitivity should be carried out of the designed CT $\Delta\Sigma$ ADC. This in order to evaluate whether the use of a 7-level quantizer and a NRZ feedback waveform reduces the jitter sensitivity as predicted theoretically or if other solutions are needed.

8

Other Research Topics

This chapter briefly presents the other research topics, that were co-authored during the PhD studies.

8.1 How To Implement an Experimental Course on Analog IC Design in a Standard Semester Schedule

The work concerns the development of a new course line in the field of analog integrated electronics at the Technical University of Denmark, with the courses teaching the engineering students the entire development process when designing analog integrated circuits. The paper describes in detail how the course was developed and the results of the evaluation of the course by the students taking the first edition of the course. The paper was presented at the NORCHIP 2013 conference, see App. E

8.2 Increasing Generic Engineering Competences Using Coaching and Personal Feedback

The work concerns the use of coaching and feedback in order to improve the engineering students general engineering competences; thereby better preparing the students for the work life in a company after graduation. This was done in a project course on practical analog IC design, where the setting of the project is that of a fictional company with the students "employed" as development engineers for the duration the project period. The paper describes how the students during the course are provided with feedback on their performance, and how they are coached during problem solving. The paper was presented at the CDIO 2014 conference, see App. F

8.3 Investigation of an AGC for Audio Applications

The work concerns the investigation of an adaptive A/D conversion channel for use in hearing aids, similar to the conversion channel presented in Chap. 2. The paper describes the investigation of the maximum allowed gain steps that may be used when changing the gain settings of the gain channel, without the resulting transient glitches being audible. The system was evaluated using a listening test, with the results showing that gain steps down to 0.01 dB were necessary for the glitches to be inaudible. Based on this the paper concludes that this approach is not feasible from a circuit implementation point-of-view. An alternative conversion channel containing two separate channels is then presented as a solution to the problem of transient glitches. The paper was presented at the PRIME 2015 conference, see App. G.

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A

Objective Evaluation of the Audibility of Transient Errors in an Adaptive A/D Conversion Channel

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OBJECTIVE EVALUATION OF THE AUDIBILITY OF TRANSIENT ERRORS IN AN ADAPTIVE A/D CONVERSION CHANNEL

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ABSTRACT

An adaptive analog-to-digital conversion channel for audio, using automatic gain control, generates transient errors that may be audible. Evaluating the audibility of such errors requires subjective evaluation using listening tests. From an electrical circuit design point-of-view this is not feasible, due to design time constraints.

This paper investigates the use of the model output variables (MOVs) from the Perceptual Evaluation of Audio Quality (PEAQ) method, for objectively evaluating the transient errors of the conversion channel, in order to optimize the design and reduce design time.

The objective method is compared with results from an alternative forced choice listening test. The comparison shows that the objective method can be used to evaluate the audibility of the transient errors; thus the method can be applied when designing the circuit implementing the channel.

Index Terms— Objective Audio Evaluation, PEAQ, Alternative Forced Choice, Analog-Digital Conversion

1. INTRODUCTION

When designing electrical circuits, evaluating the circuits performance is crucial. For audio electronics, the circuits should be transparent from a signal quality point-of-view, to avoid reducing audio quality.

An adaptive analog-to-digital (A/D) conversion channel for audio has been developed, shown in Fig. 1. Based on [1] the main property of the channel is a dynamic range that is larger than the peak signal-to-noise ratio (SNR). This makes the current consumption in the analog part smaller than for a channel with a dynamic range equal to the peak SNR, since the current consumption is directly proportional to the peak SNR. However, as the channel is adaptively reconfigured, a transient error glitch is added to the output. This error may be audible, which is highly unwanted, and the audibility needs to be evaluated. Commonly the SNR and the total harmonic distortion (THD) are used as metrics when evaluating audio quality. Since they are only useful for steady state evaluation, carrying out listening tests is necessary. Unfortunately,

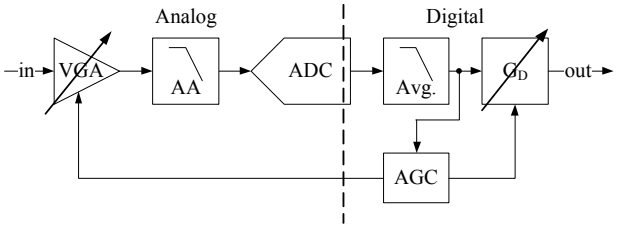

Fig. 1. Block diagram of adaptive A/D conversion channel

conducting a listening test is time-consuming, making trade-off evaluations in the design phase practically impossible. An objective evaluation using a computer based model would be preferred, for faster evaluation of the channel.

The mean squared error (MSE) would be a simple and useful metric to objectively evaluate the audibility of the transient error, by measuring the mean error energy. However, the calculated MSE can be the same for very different error signals [2], and does not take into account the frequency and temporal masking effects of the human hearing. To objectively evaluate the sound quality of high-fidelity audio systems with small impairments, the *Perceptual Evaluation of Audio Quality* (PEAQ) method can be used [3], [4]. Benjamin [5] used with good results the PEAQ method to evaluate audio quality degradation due to noise in analog-to-digital, digital-to-analog and sample-rate converters. Different parts of the human hearing are modelled and evaluated in the PEAQ method using model output variables (MOVs). Creusere and Hardin [6], [7] used the MOVs for objective evaluation of the audio quality of signals with temporally varying errors, also with good results.

Since the PEAQ evaluates systems with small impairments and grades the audio quality, it is not directly applicable for evaluating the audibility of the errors generated by the adaptive A/D conversion channel. This paper investigates the use of PEAQ MOVs to evaluate the audibility of transient errors generated by the adaptive A/D conversion channel. Specifically the *Maximum Filtered Probability of Detection* (MFPD) and *Average Distorted Block* (ADB) MOVs from the PEAQ method were used as they model the probability of detecting impairments present in the signal under test. To

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validate the usage of the MFPD and ADB, the computed results have been compared with the results of an alternative forced choice listening test.

2. ADAPTIVE A/D CONVERSION CHANNEL

An A/D conversion channel with a static gain is often used in e.g. microphones, which require a constant sound pressure level (SPL) sensitivity. For this type of channel, signal clipping occurs when the input signal becomes too large. This can be avoided by increasing the dynamic range of the channel, either by increasing the supply voltage, by decreasing the noise floor via increased bias currents, or by decreasing the overall channel gain. Unfortunately, these options may not be possible due to the specific application of the microphone.

Alternatively an adaptive A/D conversion channel can be used, with an analog and a digital part. A block diagram of this channel is shown in Fig. 1, consisting of an analog variable gain amplifier (VGA), an anti-aliasing (AA) filter, an analog-to-digital converter (ADC), an averaging filter, a digital gain block and an automatic gain controller (AGC). The overall gain of the channel is given as:

$$G_{tot} = G_a \cdot G_d \tag{1}$$

where G_{tot} is the total channel gain, G_a is the analog gain and G_d is the digital gain. The AGC adjusts G_a while simultaneously compensating by adjusting G_d, in order to achieve a constant channel gain. When the input signal level increases above a specific threshold level, the AGC decreases the analog gain and increases the digital gain, and vice versa when the signal level is reduced. In this manner the input dynamic range of the channel is increased, while maintaining a constant channel gain. The disadvantage is that the input referred noise of the ADC is increased when G_a is reduced, causing an increase in the input referred noise of the channel for large input signals.

A more prominent problem is that when the channel gain is reconfigured, a transient error signal is generated due to the non-zero step response time from the output of the VGA to the input of the digital gain block. Assuming that the gain change occurs at $t = 0$, the error can be modelled as:

$$e(t) = \Delta G \cdot [h(t) - s(t)] \cdot x(t) \tag{2}$$

where ΔG is the change in gain, $h(t)$ is the Heaviside step function, $s(t)$ is the step response of the channel from the VGA output to the averaging filter output, and $x(t)$ is the input signal. This error equals a pulse, with a roll-off dependent on $s(t)$, and may be heard as a click. From (2), the peak value of the error is determined by ΔG and by $x(t)$. The value of $x(t)$ is related to the AGC threshold level, making both ΔG and $x(t)$ design parameters. The problem is to determine the optimum value for these parameters to avoid audible glitches in the output of the conversion channel. Thus an evaluation of the audibility of the transient errors is necessary.

3. OBJECTIVE EVALUATION OF ERROR SIGNAL

The PEAQ method evaluates the audio quality of a signal in several steps [3]. First the input signals (the reference and the signal under test) are transformed, using a model of the basilar membrane of the human ear, to generate excitation patterns. These are split into time-frames that are analysed in the frequency domain. The excitation patterns are further analysed for differences based on different aspects of the human hearing, represented using intermediate MOVs. The FFT based version of PEAQ uses two MOVs for modelling the probability of detection of a difference between the two signals: the MFPD and ADB.

For each frequency band in a frame, the probability of detecting the difference between the two signals is found, and used to determine the overall detection probability of the difference in each frame. The MFPD is calculated from the filtered probabilities as the maximum worst case filtered probability. The ADB models the distortion severity of the signal-under-tests as caused by the error signal. It is calculated as the average of the severity of distortion for each frame having a probability of detection above 50 %. For a more detailed description see [3], [8].

4. EXPERIMENTS

4.1. Listening Tests

To verify the results of the objective method when evaluating the transient errors of the A/D conversion channel, a subjective evaluation of the threshold level of hearing the error signal was carried out. A three interval, three alternative forced choice (3I3AFC) test was used together with the 1-up 1-down method [9]. The 1-up 1-down method was selected as it determines the point of 50 % probability of detection, as also used when computing the MFPD and ADB MOVs [4]. A 3I3AFC test was used instead of a 3I2AFC, to reduce the impact of random test answers on the overall test results.

The test subjects first did a training run, where feedback was given on the ability of the test subject to identify the correct error interval. The actual test consisted of three repeated runs for each of the three groups of test signals, each group using a different signal, resulting in a total of nine test runs. For all runs, the level of the transient error in the test signals was adjusted in steps of 4 dB and 2 dB during the search part, while 1 dB steps were used for the actual measurement part.

The scaling of the transient error signal was based on the method used in [10]. The generation of the tests signals is described further in Sec. 4.3.

The three test signal groups were created from 2.5 second long cut-outs of the *Double-bass*, *Tuba* and *English Male Speech* signals from the EBU Sound Quality Assessment Material CD [11]. The signals were selected in order to stress the conversion channel. The *Double-bass* and *Tuba* signals have

low frequency content, which initial investigations showed decreases the error detection threshold level compared to signals with more high frequency content. The *English Male Speech* has a higher frequency content and is more complex, due to the many breaks and signal level variations. In this way the AGC would change gain settings more often, generating more transient errors in the output.

The test was carried out on a PC using the AFC MATLAB package [12]. A double-wall sound-attenuating listening booth was used for the test, and the signals were played back using a pair of *Sennheiser HD 580 Precision* headphones connected to a *RME DIGI96/8* 24 bit D/A converter with 48 kHz sample rate. The signal playback level was 68 dB SPL, with peak levels at 76 dB SPL, and the duration of the entire test was less than 1 hour for each test subject.

A total of 15 untrained test subjects were used, age range from 23 - 34, and all assumed to have normal hearing based on interviews prior to the tests. All experiments were approved by the Science-Ethics Committee for the Capital Region of Denmark (reference H-3-2013-004).

4.2. Model Simulations

For the objective evaluation of the test signals, the PEAQ implementation by Kabal [13] was used. This version implements the FFT based version of the PEAQ method, with the computed MOVs output scores directly available.

4.3. Generation of Test Signals

The test signals used for both the listening test and the objective method were generated using a high-level model of the A/D conversion channel. The VGA was modelled as a gain stage with a limiter function and gain settings from 0 dB to 18 dB in 6 dB steps. The AA filter was modelled as a 1st order low-pass filter with $f_{-3dB} = 200\ kHz$. The ADC was modelled as a linearized 4th order $\Delta\Sigma$ ADC, to only model the signal transfer function of the modulator. The averaging filter was implemented as a 16 tap FIR filter. Finally, the digital gain block was implemented as a multiplier with gain coefficients from 0 dB to 18 dB in 6 dB steps. The AGC was modelled with upper and lower signal threshold levels and with time-hysteresis to prevent the gain settings from constantly changing.

The transient errors for each input signal were found by subtracting a reference signal from the output signal of the A/D conversion channel model. Ideally the channel input signal would be used as the reference. However, due to the transfer function of the A/D conversion channel, the extracted error signal would also contain the difference caused by the phase shift of the channel. As only the transient error is of interest, the reference signal was generated using a reference model of the A/D conversion channel. The reference model was similar to the adaptive conversion channel, with the AGC and VGA limiter functions removed.

	Test signal group		
	Double-Bass	*Tuba*	*English-Speech*
$Q1$	-34.9 dB	-35.6 dB	-21.1 dB
$Q2$	-32.7 dB	-34.4 dB	-18.4 dB
$Q3$	-30.8 dB	-33.1 dB	-15.9 dB
$\bar{x}$	-32.7 dB	-34.1 dB	-18.7 dB
s	2.81 dB	2.84 dB	3.15 dB

Table 1. Statistics for the transient error detection threshold levels from the results of the listening test

Both channel models were discrete time models implemented in MATLAB, using a sample rate of 2 MHz equal to the sample rate of the $\Delta\Sigma$ ADC. To simulate the A/D conversion channel using audio signals, the input signals were up-sampled from 48 kHz to 2 MHz. Using the extracted transient error signal, the test signals were generated by scaling the transient error signal from -60 dB to 6 dB and adding it to the reference signal. The model output signals were down-sampled to a 48 kHz sample rate and exported to WAVE files with 24 bit resolution.

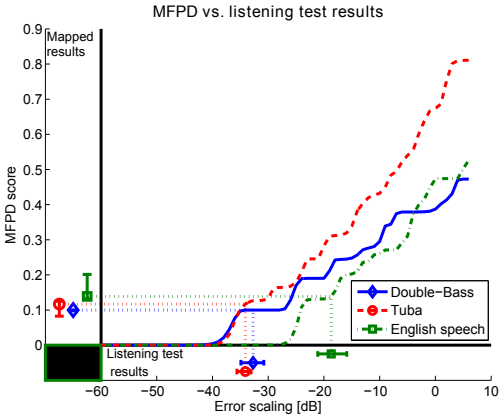
The peak value of the extracted transient error signals was approximately the same for all three input signals, as follows from (2) due to the fixed ΔG and AGC threshold levels. Nevertheless, the peak error value was not exactly the same for the three input signals since the AGC operates in discrete time. As a result, the error scaling rather than the peak error level was used for describing the transient error signal level in the test signals.

5. RESULTS

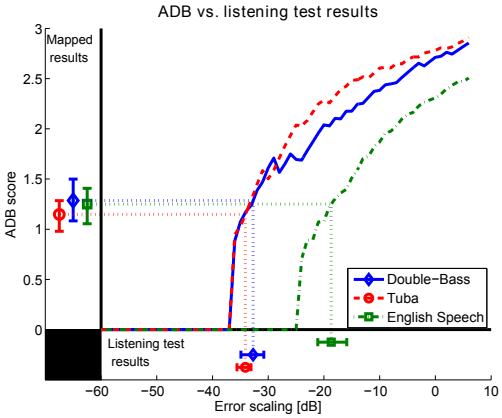
The mean detection threshold level for each test signal was determined based on the results of each test subject, and values for each test signal group were confirmed to be normal distributed by using normal probability plots. The mean threshold values are presented in Table 1, listing for each test signal group the 1st, 2nd and 3rd quartile ($Q1,\ Q2,\ Q3$), the sample mean $\bar{x}$, and the sample standard deviation s.

The calculated ADB and MFPD outputs for the three test signal groups are shown in Fig. 2. These outputs are the plotted curves, showing the equivalent MOV output value for each scaled error signal. The x-axis represents the error scaling factor used in the test signals, while the y-axis is the output value of the specific MOV.

The listening test results have been plotted in the bottom of the subfigures, and show for each signal group the found threshold mean and the 1st and 3rd quartiles. The mean value has been plotted with a marker while the 1st and 3rd quartiles are plotted as the edges of the variation lines. The plots on the left are the means and quartiles from the listening tests that have been mapped onto the MOV curves.



(a) MFPD



(b) ADB

Fig. 2. Calculated output values from MOVs

6. DISCUSSION

6.1. Bias Effects in Listening Tests

Due to the way the test signals were generated, the error was always present at the same time-instant for a given test signal group, independent of the error scaling. This effect is caused by the way the AGC works, as it triggers when the signal level crosses the specific threshold levels. Thus for a given input signal the error is always present at the same time-instant, independent of the size and shape of the error. Some test persons noticed this during the tests, resulting in a lower detection threshold. Consequently a lower mean threshold level was expected from the listening test in comparison to a test using non-repeated signals.

6.2. Evaluation of Results

The test results show that the error signal is easier to detect in the *Double-Bass* and *Tuba* signals compared to the *English Speech* signal; a consequence of signal frequency content and masking effects in the human hearing. Fig. 2 shows that for the ADB, the placement of the curves along the x-axis is similar to the test results. The MFPD output curves show the same trend, although not as clearly as for the ADB curves.

To compare the ability of the MOVs to evaluate the audibility of the transient error signals with results of the listening test, the test results were mapped onto the MOV output curves. The mappings showed that both MOVs generated output values in the same range for all test signals groups. In particular, the mapped variations for the ADB were closely matched, while the mapped results for MFPD had a larger variation. For the *Double-Bass* signal there was no variation in the MFPD mapping, because of the plateaus in the MFPD output curves. Generally these plateaus make the interpretation of the MFPD output difficult.

Based on these observations, we find that the ADB is an accurate method for objectively evaluating the transient errors of the adaptive A/D conversion channel, while the MFPD may be used for binary evaluation together with the ADB.

In relation to the optimization of the conversion channel in the design phase, it is relevant to consider which ADB and MFPD values one should target, to make the transient errors inaudible. The channel should be designed for the worst case situation, which from Fig. 2 is the threshold for the *Tuba* and *Double-Bass* signals. An option would be to aim for the lowest threshold levels found. However, during the tests the signals were played back at a specific SPL, which affected the error audibility. In contrast the MFPD and ADB output values were calculated from the unscaled test signals. It may be possible that the errors are audible if the signals are played back at a higher SPL; this makes it difficult to use the mapped MOV threshold values as a design target. Alternatively a goal is to achieve both ADB and MFPD outputs equal to zero; this equals a 50 % probability that there is no audible difference between the reference signal and the signal under test [4]. When designing and optimizing the adaptive A/D conversion channel this would be a conservative first design goal.

7. CONCLUSION AND FUTURE WORK

The adaptive A/D conversion channel has been evaluated using both subjective listening tests and objective computational methods. The results showed that the ADB is a good candidate for evaluating the audibility of the transient errors generated by the conversion channel while the MFPD is a less accurate tool. Based on the results, an output value of zero for both MOVs is a conservative first design goal when designing and evaluating the adaptive A/D conversion channel.

Future work includes evaluation of the objective method using more test signals, and also applying the method in an actual channel design and compare the computed results with results from a listening test.

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B

Circuit and Method of Operating a Circuit

European Patent Office application PCT/EP2014/059488

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Number of applicants	1
Country	DE
Title	CIRCUIT AND METHOD OF OPERATING A CIRCUIT

Documents submitted		
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	eolf-appb.xml	eolf-fees.xml
	eolf-vlog.xml	eolf-othd-000001.pdf (30 p.)
	eolf-abst.txt	eolf-appb-P000001.pdf (2 p.)

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Description

CIRCUIT AND METHOD OF OPERATING A CIRCUIT

The present invention concerns a circuit and a method of operating a circuit. In particular, the circuit is configured to receive an input signal, to amplify the input signal and to provide an output signal corresponding to the amplified signal. Moreover, the circuit may be configured to convert an analog input signal into a digital output signal.

The input signal may be provided by a MEMS microphone. Accordingly, the circuit may be an analog-to-digital conversion channel for audio signals. In an analog-to-digital conversion channel for audio signals, achieving both a high signal-to-noise ratio and the capability of handling large input signals is challenging.

In order to increase the dynamic gain, amplifiers with variable gain are used. An automatic gain control system comprising an analog variable gain amplifier, an analog-to-digital converter, a digital variable gain amplifier and an automatic gain controller can be used. With this system, for large input signals the analog gain of the analog variable gain amplifier can be reduced to avoid signal clipping in the analog variable gain amplifier and/or in the analog-to-digital converter. To maintain a constant channel sensitivity, the reduction in the analog gain is compensated by an increase in the gain of the digital variable gain amplifier.

However, a disadvantage of this system is that, when the analog gain and the digital gain are changed, a transient

audible glitch is created in the circuit. The glitch is created due to the time-delay in the conversion channel. In particular, a digital variable gain amplifier is enabled to carry out a change in its variable gain instantaneously as its components are digital. However, the analog variable gain amplifier carries out the change in its gain setting exponentially over time as its components require a ramp-up time to adjust to its settings. For example, a capacitor requires a certain time to adjust its capacitance. Thus, in a short period of time after the changes of the two gain settings, the overall gain is not constant. Thereby, the transient glitch is created, resulting in an audible distortion of the output signal.

The peak value of the glitch depends on the change of the gain in the analog variable gain amplifier and the gain of the digital variable gain amplifier, wherein a smaller gain change creates a less audible transient glitch in the output signal.

WO 2004/095709 A2 describes a solution to remove the glitch in such a system. Here, a gain of an analog variable gain amplifier and a gain of a digital variable gain amplifier are not changed simultaneously. Instead, the gain of the analog variable gain amplifier is changed at a time t1 and the gain of the digital variable gain amplifier is changed at a time t2 different from t1. The difference between t2 and t1 roughly equals the delay in the analog-to-digital conversion channel from the output of the analog variable gain amplifier to the input of the digital variable gain amplifier. This allows to reduce the peak value of the transient glitch, but not to completely remove the glitch. Depending on the size of the gain change of the two amplifiers, the reduced transient

glitch may still be audible. Thus, the solution requires using very small gain changes in order to make the transient glitch inaudible. Smaller gain changes increase the complexity of both of the analog variable gain amplifier and the digital variable gain amplifier. This method further requires a fine tuning of the delay in the channel from the analog variable gain amplifier output to the input of the digital variable gain amplifier in order to minimize the transient glitch optimally.

In US 2003/083031 A1 an alternative solution is described wherein two parallel and concurrently operating analog-to-digital conversion channels are used. Both channels comprise an analog variable gain amplifier, an analog-to-digital converter, a digital variable gain amplifier and an automatic gain control. When the input signal increases, the gain of the analog variable gain amplifier is reduced and simultaneously the gain of the digital variable gain amplifier is increasing by the same amount in one of the channels. This causes a transient glitch in this adapted channel. While the adapted channel settles due to the gain change, only the output of the respective other channel is fed to an overall channel output. Once the adapted channel has settled, the overall output is fed from this channel instead of the other channel. In this manner the transient glitch is avoided. However, this solution requires two identical and concurrently running channels. Accordingly, this solution doubles the circuit area and the current consumption of the circuit. It also requires extra digital signal processing for combining the output signals from the two channels. Thus, this solution is not feasible for a low power application with limited circuit area.

It is an object of the present invention to provide a circuit which overcomes at least some of the above-discussed disadvantages. Moreover, it is another object to provide a method of operating such a circuit.

This object is solved by a circuit according to claim 1. The further object is solved by a method according to the second independent claim.

A circuit is proposed comprising a first amplifier with a variable gain, a second amplifier with a variable gain configured to provide an output signal, a control unit configured to adjust the variable gain of the first amplifier and the variable gain of the second amplifier, a memory element configured to store a sample of the output signal and a switching member configured to connect an output port of the circuit either to the second amplifier or to the memory element.

Thus, the circuit is configured such that the output port of the circuit can either be fed with the output signal from the second amplifier or with a signal stored in the memory element. Thereby, the circuit allows for removing the transient glitch by providing the stored signal during an adjustment time in which the glitch occurs.

Only the memory element and the switching member are required as additional components over a basic analog-to-digital conversion channel such that the glitch removal can be carried out with a minimal number of total components and with only a very small increase in the chip size.

Moreover, no added digital signal processes are required. Multiple copies of the same circuit block are also not required. Overall, the added area and the added current consumption of the circuit is much smaller than in the above cited prior art.

The sample stored by the memory element may correspond to the last N values of the signal outputted by the second amplifier. Thus, at a given point of time, the signal stored in the memory element corresponds to the latest signal provided by the second amplifier.

In particular, the memory element may comprise a memory block. Accordingly, the term "the memory element is configured to store a sample of the output signal" is to be understood such that the memory element stores or writes values in its memory block which corresponds to the recently provided output signal. The memory element may be configured to store N values in its memory block corresponding to the last N bits outputted by the second amplifier. These N values may define the stored sample.

The switching member is configured such that the output port of the circuit is connected at a given point of time either to the second amplifier or to the memory element. The switching member is configured to switch between a state wherein the output port is connected to the second amplifier and a state wherein the output port is connected to the memory element.

When the output port is connected to the second amplifier, the output signal from the second amplifier is provided at the output port as the output signal of the circuit. When the

output port is connected to the memory block, a signal provided by the memory block may be provided at the output port as the output signal of the circuit.

Accordingly, the circuit may be configured to provide an output signal wherein the output signal is either the output signal of the second amplifier or a signal provided by the memory element.

In one embodiment, the memory element may be configured to provide a signal to the output port when the output port is connected to the memory element wherein the signal provided by the memory element is based on the stored sample.

When the memory element is connected to the output port, it may operate in a read-only manner such that no new values are stored in the memory element. In particular, the memory element may be connected to the output port by the switching member after a change in the gains of the first and the second amplifier has been carried out. In this case, the first and the second amplifier can settle to the adjustment of the gains. In this time, a glitch is present in the output signal of the second amplifier. However, the glitch does not reach the output port as the output port is connected to the memory element and not to the second amplifier. The stored sample from the memory element is provided to the output port, thereby effectively removing the glitch from the output signal of the circuit.

In one embodiment, the memory element is configured to provide a signal to the output port when the output port is connected to the memory element wherein the signal provided by the memory element is identical to the stored sample.

Thus, in this case, the last signal from the second amplifier before the adjustment of the gains is repeated at the output port. It can be assumed that the last signal before the adjustment is very close to the correct signal. The correct signal corresponds to an amplification of the input signal.

A distortion occurs when the output port is connected back to the second amplifier and the output signal of the second amplifier is again outputted at the output port. However, by repeating the last signal before the adjustment, it is ensured that the distortion will be very small in most cases.

In one embodiment, the memory element is configured to provide a signal to the output port when the output port is connected to the memory element wherein the signal provided by the memory element is an extrapolation of the stored sample.

This allows for an improved estimate of the correct signal during the time when the output port is connected to the memory element. Thus, the above discussed distortion will be reduced even further in most situations.

In one embodiment, the circuit may be configured such that the switching member connects the output port to the memory element for a predetermined period of time when the control unit adjusts the variable gain of the first amplifier and the variable gain of the second amplifier.

The predetermined period of time may be chosen such that it is longer than the ramp-up time required by the amplifiers to adjust to a change in their gain. The predetermined period of

time may be chosen such that a transient glitch which occurs due to the gain change has settled before the end of the predetermined period of time. Further, the predetermined period of time is chosen as small as possible with the limit that the transient glitch has to be settled before the end of the predetermined period of time. The exact value of the predetermined period of time depends on the parameters of the amplifiers of the circuit. In particular, the predetermined period of time can be chosen in view of the first and the second amplifier. Thus, the circuit is robust against any variations in the time-delay of the two amplifiers, therefore allowing to use the circuit with all kinds of amplifiers.

In one embodiment, the circuit may be configured such that the switching member connects the output port to the second amplifier after the predetermined period of time.

Thus, after the predetermined period of time is elapsed, the output signal of the second amplifier may again be provided as an output signal of the circuit. This signal will be free from the glitch.

Further, in one embodiment the circuit may be configured such that, when the output port is connected to the second amplifier, the output signal of the second amplifier is constantly written into the memory element and the memory element constantly overwrites previously stored samples in a first-in, first-out manner. Thus, the sample stored in memory element corresponds to the latest output signal of the second amplifier when the output port is connected to the second amplifier.

In one embodiment, the circuit may be configured such that the memory element is prevented from overwriting the stored sample when the output port is connected to the memory element. In particular, the memory element may be configured to be in a read-only mode when connected to the output port.

In one embodiment, the control unit may be configured to adjust the variable gain of the second amplifier reciprocally proportional and simultaneously to an adjustment of the variable gain of the first amplifier.

The first amplifier may be an analog amplifier. The second amplifier may be a digital amplifier. The circuit may further comprise an analog-to-digital converter arranged between the first amplifier and the second amplifier. A sample rate of the analog-to-digital converter may be larger than the Nyquist rate for sampling of audio signals in the range from 20 Hz to 20 kHz.

The circuit may further comprise at least one filter. The filter may be a bandpass filter, a lowpass filter, a highpass filter, an allpass filter or a combination of different types of filters. The filter may be arranged in a main signal path connecting an input port of the circuit with the output port. Overall, the filter improves the quality of the provided output signal as the filter is configured to filter out unwanted noise.

The present invention further concerns a method of operating a circuit. The circuit may be the above-disclosed circuit. Thus, any structural or functional feature disclosed with respect to the circuit may also be present with respect to the method. Vice versa, any functional or structural feature

disclosed with respect to the method may also be present with respect to the circuit.

The method comprises the steps of:

- monitoring a first output signal of the first amplifier,
- adjusting the variable gain of the first amplifier and the variable gain of the second amplifier if the first output signal is below a first predefined threshold level or above a second predefined threshold level,
- connecting the memory element to the output port for a predetermined period of time if the variable gain of the first and the second amplifier is adjusted.

The first threshold level may be chosen such that it is exceeded when the first amplifier is close to its clipping threshold. The second threshold level may be chosen such that the first output signal falls below the second threshold level when a signal strength of the first output signal is weak.

The monitored output signal of the first amplifier may either be directly the output signal of the first amplifier or may be processed first, e.g. in an analog-to-digital converter and afterwards monitored.

The method may further comprise the step of connecting the second amplifier to the output port after the predetermined period of time.

In the following, the disclosed circuit and the method are described in further detail with reference to the drawing, wherein

Figure 1 shows a circuit.

Figure 1 shows a circuit 1. The circuit 1 is configured to receive an input signal and to amplify the input signal. Further, the circuit 1 is configured to provide an output signal which is based on the received input signal.

In particular, the circuit 1 is configured to receive an input signal from a MEMS microphone (not shown). The input signal from the MEMS microphone is an analog signal.

Moreover, the circuit 1 is configured to convert an analog signal into a digital signal. Accordingly, the input signal is an analog signal and the output signal of the circuit 1 is a digital signal.

The circuit 1 comprises an input port 2. The circuit 1 further comprises an output port 3. The input port 2 and the output port 3 are connected by a main signal path 4. In the main signal path 4, a first amplifier 5 and a second amplifier 6 are arranged. The first amplifier 5 is connected to the input port 2. The first amplifier 5 is an analog amplifier. The first amplifier 5 is configured to receive an analog input signal from the input port 2 and to provide an analog output signal which corresponds to the input signal amplified by a first gain factor.

Between the first amplifier 5 and the second amplifier 6 an analog-to-digital converter 7 is arranged. The analog-to-digital converter 7 is configured to receive the analog output signal from the first amplifier 5 and to provide a corresponding digital output signal.

The analog-to-digital converter 7 can be of any type, for example a Delta-Sigma analog-to-digital converter, a flash analog-to-digital converter or a successive approximation analog-to-digital converter. If the analog-to-digial converter 7 is a Delta-Sigma converter, it may be continuous time, switched-capacitor or a hybrid of the two. The output of the analog-to-digital converter 7 can be single-bit or multi-bit.

The analog-to-digital converter 7 is connected to the second amplifier 6. The second amplifier 6 is a digital amplifier. Accordingly, the second amplifier 6 is configured to receive a digital signal from the analog-to-digital converter 7 and to provide an amplified digital output signal wherein the amplified digital output signal is amplified by a second gain factor.

Each of the first amplifier 5 and the second amplifier 6 has a variable gain. Accordingly, the first gain factor of the first amplifier 5 is variable. The second gain factor of the second amplifier 6 is also variable.

The circuit further comprises a control unit 8. The control unit 8 may be an automatic gain control. The control unit 8 is configured to adjust the variable gain of the first amplifier 5 and the variable gain of the second amplifier 6.

In the embodiment shown in Figure 1, the control unit 8 receives the output signal of the first amplifier 5 and the output signal of the analog-to-digital converter 7 as input signals. However, in alternate embodiments, the control unit 8 may receive only one of said two signals as an input signal. When the input signal of the control unit 8 exceeds a

first predefined threshold level or when the input signal of the control unit 8 is below a second predefined threshold level, the control unit 8 will adjust the variable gain of the first amplifier 5 and the variable gain of the second amplifier 6.

In particular, the variable gain of the first amplifier 5 and the variable gain of the second amplifier 6 are adjusted by the control unit 8 simultaneously and reciprocally proportional to each other. Accordingly, when the variable gain of the first amplifier 5 is adjusted by a factor A_i, the variable gain of the second amplifier 6 is adjusted by a factor $1/A_i$. Thus, an overall gain of the first amplifier 5 and the second amplifier 6 remains unchanged. The overall gain corresponds to the product of the gain of the first amplifier 5 multiplied with the gain of the second amplifier 6.

Moreover, the circuit 1 comprises a memory element 9. The memory element 9 is configured to receive the output signal of the second amplifier 6. In particular, the memory element 9 is configured to store a sample of the output signal of the second amplifier 6.

The circuit further comprises a switching member 10. The switching member 10 is configured to connect the output port 3 of the circuit 1 either to the second amplifier 6 or to the memory element 9. When the output port 3 is connected to the second amplifier 6, the output signal of the second amplifier 6 is provided as an output signal of the circuit 1. When the output port 3 is connected to the memory element 9, the memory element 9 is configured to provide an output signal based on the stored sample.

In the embodiment shown in Figure 1, the switching member 10 comprises an inverter 11, a first switch 12 and a second switch 13. The first switch 12 is arranged in the main signal path 4 between the second amplifier 5 and the output port 3. The second switch 13 is arranged between the memory element 9 and the output port 3. The inverter 11 is arranged between the control unit 8 and the first switch 12. Thus, the inverter 11 is arranged such that it inverts a control signal sent by the control unit 8.

As discussed above, the control unit 8 is configured to send control signals to the first and the second amplifier 5, 6. Accordingly, the control unit 8 is configured to control the gain setting of the first and the second amplifier 5, 6. Moreover, the control unit 8 is also configured to control the operation of the memory element 9 and of the switching member 10.

The control unit 8 is configured to send a control signal to the switching member 10. As the inverter 11 inverts the control signal for the first switch 12, the control signal sent by the control unit 8 has an opposite command for the first switch 12 and for the second switch 13. Accordingly, at any given time, one of the first switch 12 and the second switch 13 is open and the respective other of the first switch 12 and the second switch 13 is closed.

Further, the memory element 9 is also configured to receive the control signal from the control unit 8. The command of control signal with respect to the memory element 9 will be discussed later-on.

The circuit 1 has a normal operation mode and a gain adjustment mode. Fig. 1 shows the circuit 1 in the normal operation mode.

The circuit 1 usually operates in the normal operation mode. The circuit 1 switches to the gain adjustment mode for a predetermined period of time, when the control unit 8 adjusts the variable gain of the first amplifier 5 and the variable gain of the second amplifier 6. The circuit 1 switches from the gain adjustment mode back to the normal mode when the predetermined period of time is elapsed.

The normal operation mode is characterized by the output port 3 of the circuit 1 being connected to the second amplifier 6 by the switching member 10. The gain adjustment mode is characterized by the output port 3 being connected to the memory element 9 by the switching member 10.

First, the normal operation mode of the circuit 1 is considered in detail. In the normal operation mode, the switching member 10 connects the second amplifer 6 to the output port 3. In particular, the first switch 12 is closed. The output signal of the second amplifier 6 is provided as an output signal of the circuit 1 at the output port 3.

Further, in the normal operation mode, the memory element 9 is configured to receive the output signal of the second amplifier 6. The output signal of the second amplifier 6 is constantly written into the memory element 9 and the memory element 9 constantly overwrites a previously stored sample in a first-in, first-out manner. A corresponding control signal is sent by the control unit 8 to the memory element 9.

In particular, the memory element 9 is configured to store N values. Thus, the memory element 9 is configured to store a sample consisting of the last N output values of the second amplifier 6. In each clock cycle, the present output value of the second amplifier 6 is written into the memory element 9. This latest value is stored in the memory element 9, thereby overwriting the value stored N clock cycles ago. The memory element 9 keeps the values in its memory block which have been stored in the previous N-1 clock cycles.

However, if a change of the variable gain of the first amplifier 5 and of the variable gain of the second amplifier 6 is carried out in the normal operation mode, this would result in a distortion of the output signal. This distortion is called glitch. In particular, in the above mention case, a transient audible glitch would be created.

The glitch is created due to an unavoidable time-delay in the adjustment for the variable gain of the first amplifier 5 and the second amplifier 6. As the first amplifier 5 is an analog amplifier, it needs a certain ramp-up time to amend its components to allow for the gain change. Accordingly, the gain of the first amplifier 5 is changed not instantaneously, but has an exponential change over time. In contrast to this, the second amplifier 6 is a digital amplifier which carries out a gain change instantaneously. Thus, in a short period of time after the control unit 8 sends a control signal to adjust the variable gains of the first and the second amplifier 5, 6, the product of the two gains is not constant. Thereby, the glitch is created.

The present invention removes the glitch from the output signal.

In the following, the gain adjustment mode of the circuit is considered in detail.

The circuit 1 is configured to switch from its normal operation mode to its gain adjustment mode when the variable gain of the first amplifier 5 and the variable gain of the second amplifier 6 are amended. Further, the circuit 1 is configured to switch from its gain adjustment mode to its normal operation mode when the predetermined period of time has passed wherein the predetermined period of time is started by a switch to the gain adjustment mode.

As an example, a situation is considered wherein the input signal has a very strong signal strength such that one of the first amplifier 5 and the analog-to-digital converter 7 is close to its clipping threshold. Accordingly, the input signal of the control unit 8 exceeds the first predefined threshold level. The first threshold of the control unit 8 is chosen such that it is exceeded when one of the first amplifier 5 and the analog-to-digital converter 7 is close to its clipping threshold.

When the control unit 8 detects that the input signal is too strong, it sends a control signal to the first amplifier 5 and to the second amplifier 6. The variable gain of the first amplifier 5 is reduced by a given factor according to the control signal. At the same time, the control unit 8 increases the variable gain of the second amplifier 6 by the same factor. The given factor can in principle have any value. The exact value of the given factor depends on the programming of the control unit 8. Further, the possible values that may be chosen for the given factor also depend

on the configuration of each of the first amplifier 5 and the second amplifier 6. In particular, each of the first amplifier 5 and the second amplifier 6 has a defined range of values to which the respective variable gain can be set. Thus, the given factor has to be chosen such that the variable gain of each of the first amplifier 5 and the second amplifier 6 is within this range.

Further, the control unit 8 sends a control signal to the memory element 9 and to the switching member 10. The memory element 9 stops writing new values to its memory block. Further, the switching member 10 connects the memory element 9 to the output port 3 and disconnects the second amplifier 6 from the output port 3. In particular, the control signal orders the second switch 13 to close. Accordingly, in the gain adjustment mode, the memory element 9 is connected to the output port 3 via the closed second switch 13. Further, the inverter 11 inverts the command “close” into the command “open” such that the first switch 12 is opened. Thus, the second amplifier 6 is disconnected from the output port 3.

Further, the control unit 8 orders the memory element 9 to provide an output signal to the output port 3 wherein the output signal is based on the stored sample.

In particular, the values of the stored sample of the memory element 9 are fed into the output port 3 in a first-in, first-out manner. This is be repeated multiple times, e.g. M times. The predetermined period of time corresponds to N-times M clock cycles.

After the predetermined period of time is elapsed, the circuit 1 switches back to its normal operation mode. In

particular, after the predetermined period of time is elapsed, the control unit 8 sends a control signal to the memory element 9 such that the memory element 9 stops sending an output signal and, instead, starts storing new values from the output signal of the second amplifier 6. At the same time, the control signal changes the state of the switching member 10 such that the switching member 10 again connects the second amplifier 8 to the output port 3 and disconnects the memory element 9 from the output port 3. Accordingly, the circuit 1 is in its normal operation mode again.

The predetermined period of time is chosen such that the glitch has faded away in the signal provided by the second amplifier 6. Accordingly, after the predetermined period of time, the product of the gain of the first amplifier 5 and gain of the second amplifier 6 is constant. In other words, the predetermined period of time is chosen such that the first amplifier 5 can adjust to the change of its gain during the predetermined period of time.

The circuit 1 provides the advantage that the transient glitch is removed from the output signal of the circuit 1. During the time, when the glitch is present, the output signal of the second amplifier 6 is not provided to the output port 3. Instead, the output signal from the memory element 9 is provided to the output port 3. This signal is free from the glitch. Thus, the glitch is effectively removed from the output signal of the circuit 1.

When repeating the prior N values of the second amplifier 6 at the output port 3, this also introduces another distortion of the output signal. However, this distortion is different and smaller in amplitude than the transient glitch created by

the change of the two gain settings. Further, due to the limited bandwidth and masking effects of human hearing, the new distortion is not audible, or is at least much less audible. In particular, if the predetermined period of time is sufficiently short, the alteration to the memory element 9 and back to the second amplifier 6 is not audible.

As another example a situation is considered wherein the control unit 8 detects that its input signal is below the second threshold level. In this case, the control unit 8 increases the variable gain of the first amplifier 5 by a given factor and simultaneously decreases the variable gain of the second amplifier 6 by the same given factor. Again, the given factor can in principle have any value and the exact value of the given factor depends on the programming of the control unit 8.

The control unit 8 further orders the memory element 9 to stop storing further values from the output signal of the second amplifier 6 and, instead, to provide the stored sample as an output signal. Simultaneously, the control unit 8 orders the switching member 10 to connect the output port 3 to the memory element 9 and to disconnect the output port 3 from the second amplifier 6.

The N values stored in the memory element 9 are fed to the output port 3 in a first-in, first-out manner. This is repeated M times. After a predetermined period of time corresponding to N-times M clock cycles, the control signal of the control unit 8 is again inverted, thereby connecting the output port 3 again to the second amplifier 6 and disconnecting the output port 3 from the memory element 9. Further, the control signal orders the memory element 9 to

store new values from the output of the second amplifier 6 after the predetermined period of time is elapsed.

The circuit 1 shown in Figure 1 is implemented on a single chip. In an alternative embodiment, the analog components and the analog-to-digital converter 7 may be implemented on a first chip and the remaining part of the circuit 1 may be implemented on one or more integrated circuits. This could be a dedicated digital integrated circuit or a digital signal processor. The separation of the circuit 1 in an analog part and a digital part is indicated in Fig. 1 with a dashed line 14.

In an alternative embodiment, the memory element 9 is configured to provide a signal which is an extrapolation of the stored sample when the memory element 9 is connected to the output port 3. Thus, instead of repeating M times the sample consisting of the last N output values of the second amplifer 6, an extrapolation of the output signal of the second amplifier 6 is provided.

For this purpose, the memory element 9 may be configured to carry out a filtering of the output signal of the second amplifier 6 such that the influence of noise is reduced. The filtering of the output signal may correspond to a smoothing of the signal.

Further, the memory element 9 is configured to estimate the slope of the stored sample. In particular, during normal operation mode of the circuit 1, the memory element 9 is configured to continuously carry out an estimation of the slope of the output signal of the second amplifier 6.

The estimation of the slope of the output signal is based on two values of the filtered signal of the second amplifier 6. These two values are continuously evaluated to be able to continuously estimate the output signal slope.

The slope may alternatively be estimated based on the output signal of the analog-to-digital converter 7. The output signal of the analog-to-digital converter 7 may be fed as an input signal to the memory element 9 such that the memory element 9 can calculate the slope from this signal.

The memory element 9 is configured such that, when it is connected to the output port 3, it provides an output signal corresponding to the stored sample plus an added value based on the estimated slope.

It is assumed that the memory element 9 has estimated a slope S. The memory element 9 will provide a first output signal consisting of the stored N values wherein the slope S is added to each value. Afterwards the memory element 9 provides an output signal corresponding to the previously provided sample plus again an added value S of the estimated slope. Thus, the provided signal corresponds of the stored N values plus 2 times the slope S. This is repeated M times. Accordingly, in the last cycle, the output signal of the memory element 9 consists of the stored N values plus M times the slope S.

After the predetermined period of time, the switching member 10 again connects the second amplifier 6 to the output port 3. Simultaneously, the switching member 10 disconnects the memory element 9 from the output port 3.

Further, figure 2 shows a second embodiment of the circuit 1 wherein optional filters have been added.

In particular, an analog band-pass filter 15 has been added in the main signal path 4 between the first amplifier 5 and the analog-to-digital converter 7. The analog band-pass filter 15 receives the signal provided by the first amplifier 5 as an input signal. Further, the analog band-pass filter 15 is configured to filter said signal and to provide a corresponding output signal which is further processed by the analog-to-digital converter 7. The output signal of the analog band-pass filter 15 is also provided to the control unit 8 as an input signal. In an alternative design, the control unit 8 may be configured to receive the output signal of the first amplifier 5 as an input signal.

Further, a first digital low-pass filter 16 and a second digital low-pass filter 17 have been added to the main signal path 4. The first digital low-pass filter 16 is arranged between the analog-to-digital converter 7 and the second amplifier 6. The second digital low-pass filter 17 is arranged between the second amplifier 6 and the output port 3.

In the embodiment shown in Figure 2, the control unit 8 is configured to receive an output signal of the first digital low-pass filter 16 as an input signal. In an alternative design, the control unit 8 may be configured to receive an output signal of the analog-to-digital converter 7 as an input signal.

Further, in the embodiment shown in Figure 2, the memory element 9 is configured to receive an output signal of the

second digital low-pass filter 17 as an input signal. In an alternative design, the memory element 9 may be configured to receive an output signal of the second amplifier 6 as an input signal.

Each of the analog band-pass filter 15, the first digital low-pass filter 16 and the second digital low-pass filter 17 is optional. Other embodiments may also exchange the filters 15, 16, 17 into other types of filters including, but not limited to, bandpass filters, lowpass filters, highpass filters and all-pass filters, or a combination of different types of filters. The order of the filters may be any order.

Reference numerals

1	circuit
2	input port
3	output port
4	main signal path
5	first amplifier
6	second amplifier
7	analog-to-digital converter
8	control unit
9	memory element
10	switching member
11	inverter
12	first switch
13	second switch
14	dashed line
15	analog band-pass filter
16	first digital low-pass filter
17	second digital low-pass filter

Claims (We claim)

1. A circuit (1) comprising,
a first amplifier (5) with a variable gain,
a second amplifier (6) with a variable gain configured to provide an output signal,
a control unit (8) configured to adjust the variable gain of the first amplifier (5) and the variable gain of the second amplifier (6),
a memory element (9) configured to store a sample of the output signal, and
a switching member (10) configured to connect an output port (3) of the circuit (1) either to the second amplifier (6) or to the memory element (9).

2. The circuit (1) according to claim 1,
wherein the memory element (9) is configured to provide a signal to the output port (3) when the output port (3) is connected to the memory element (9), and
wherein the signal provided by the memory element (9) is based on the stored sample.

3. The circuit (1) according to claim 1 or 2,
wherein the memory element (9) is configured to provide a signal to the output port (3) when the output port (3) is connected to the memory element (9), and
wherein the signal provided by the memory element (9) is identical to the stored sample.

4. The circuit (1) according to claim 1 or 2,
wherein the memory element (9) is configured to provide a signal to the output port (3) when the output port (3) is connected to the memory element (9), and

wherein the signal provided by the memory element (9) is an extrapolation of the stored sample.

5. The circuit (1) according to one of the preceding claims,
wherein the circuit (1) is configured such that the switching member (10) connects the output port (3) to the memory element (9) for a predetermined period of time when the control unit (8) adjusts the variable gain of the first amplifier (5) and the variable gain of the second amplifier (6).

6. The circuit (1) according to claim 5,
wherein the circuit (1) is configured such that the switching member (10) connects the output port (3) to the second amplifier (6) after the predetermined period of time.

7. The circuit (1) according to one of the preceding claims,
wherein the circuit (1) is configured such that, when the output port (3) is connected to the second amplifier (6), the output signal of the second amplifier (6) is written into the memory element (9) and the memory element (9) constantly overwrites a previously stored sample in a first-in, first-out manner.

8. The circuit (1) according to one of the preceding claims,
wherein the circuit (1) is configured such that the memory element (9) is prevented from overwriting the stored sample when the output port (3) is connected to the memory element (9).

9. The circuit (1) according to one of the preceding claims,
wherein the control unit (8) is configured to adjust the variable gain of the second amplifier (6) reciprocally proportional and simultaneously to an adjustment of the variable gain of the first amplifier (5).

10. The circuit (1) according to one of the preceding claims,
wherein the first amplifier (5) is an analog amplifier.

11. The circuit (1) according to one of the preceding claims,
wherein the second amplifier (6) is a digital amplifier.

12. The circuit (1) according to one of the preceding claims,
further comprising an analog-to-digital converter (7) arranged between the first amplifier (5) and the second amplifier (6).

13. The circuit (1) according to one of the preceding claims,
further comprising at least one filter (15, 16, 17).

14. Method of operating a circuit (1) according to one of the preceding claims,
comprising the steps of:
- monitoring a first output signal of the first amplifier (5),
- adjusting the variable gain of the first amplifier (5) and the variable gain of the second amplifier (6)

if the first output signal is below a first predefined threshold level or above a second predefined threshold level,

- connecting the memory element (9) to the output port (3) for a predetermined period of time if the variable gain of the first amplifier (5) and the variable gain of the second amplifier (6) are adjusted.

15. Method according to claim 14, further comprising the step of:

- connecting the second amplifier (6) to the output port (3) after the predetermined period of time.

Abstract

The present disclosure concerns a circuit (1) comprising, a first amplifier (5) with a variable gain, a second amplifier (6) with a variable gain configured to provide an output signal, a control unit (8) configured to adjust the variable gain of the first amplifier (5) and the variable gain of the second amplifier (6), a memory element (9) configured to store a sample of the output signal, and a switching member (10) configured to connect an output port (3) of the circuit (1) either to the second amplifier (6) or to the memory element (9). Further, the present disclosure concerns a method of operating said circuit (1).

Significant Figure: Fig. 1

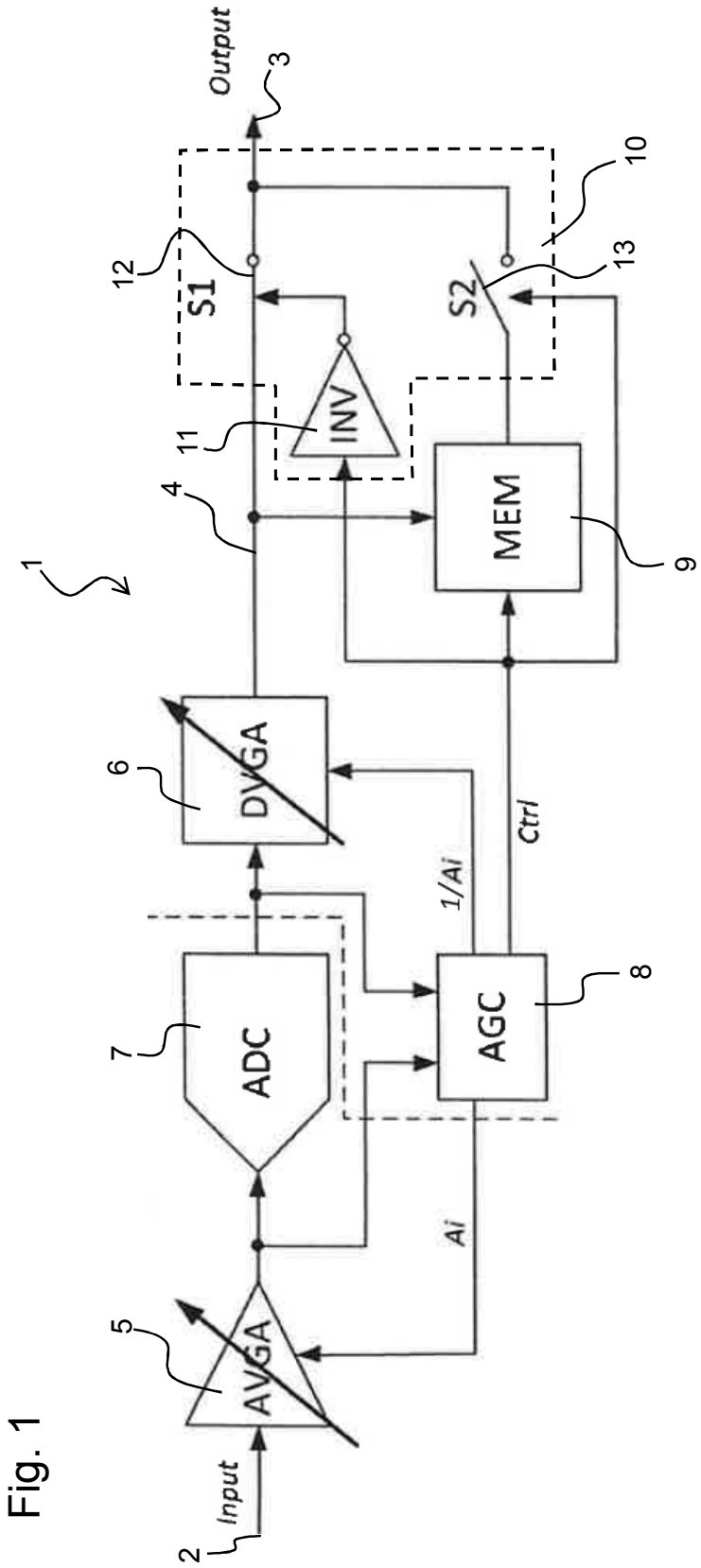
Output
3
10
12
S1
S2
13
INV
11
4
MEM
9
1
6
DVGA
1/Ai
Ctrl
7
ADC
AGC
8
Ai
5
AVGA
Input
2

Fig. 1

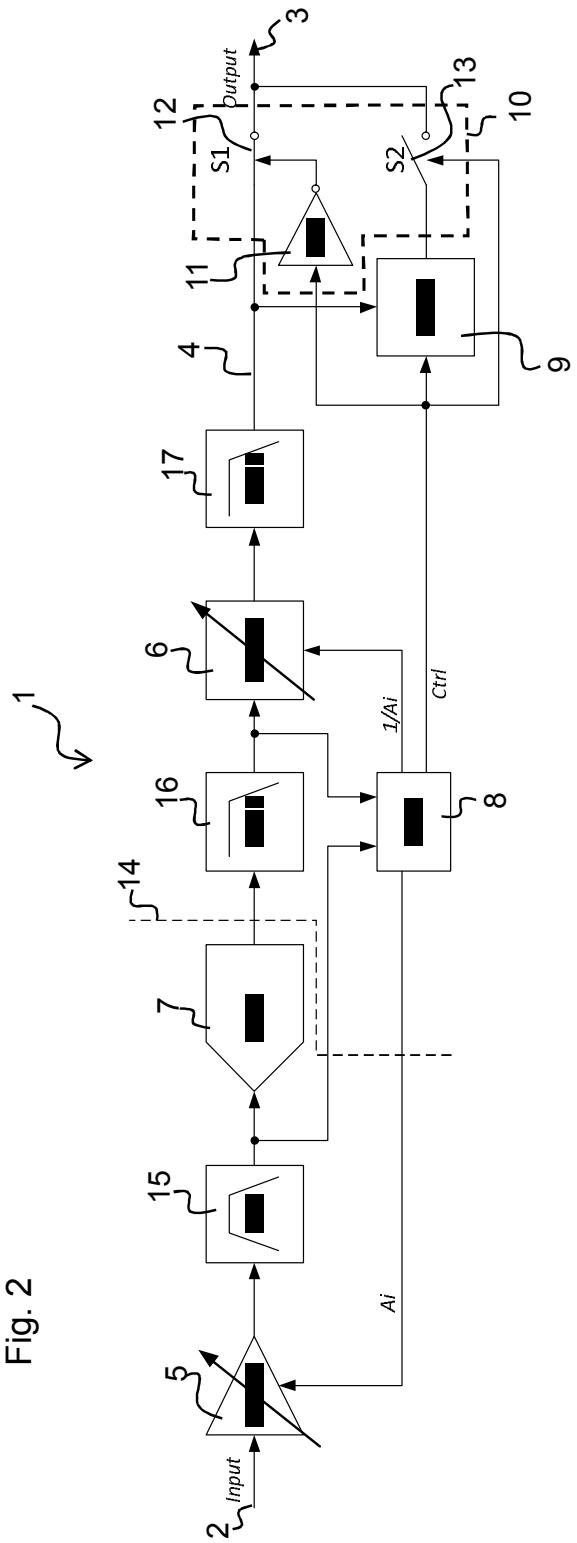

Fig. 2

C

Optimization of Modulator and Circuits for Low Power Continuous-Time Delta-Sigma ADC

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Optimization of Modulator and Circuits for Low Power Continuous-Time Delta-Sigma ADC

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***Abstract*—This paper presents a new optimization method for achieving a minimum current consumption in a continuous-time Delta-Sigma analog-to-digital converter (ADC). The method is applied to a continuous-time modulator realised with active-RC integrators and with a folded-cascode operational transconductance amplifier (OTA). Based on a detailed circuit analysis of the integrator and the OTA, key expression are derived relating the biasing current of the OTA to the noise requirements of the integrator. In the optimization the corner frequency of the modulator loop filter and the number of quantizer levels are swept. Based on the results of the circuit analysis, for each modulator combination the summed current consumption of the 1st integrator and quantizer of the ADC is determined. By also sweeping the partitioning of the noise power for the different circuit parts, the optimum modulator and circuit solution that fulfils a predefined set of performance requirements at minimum current is found. A design example is provided for a 3rd order modulator, achieving for the OTA of the 1st integrator and the quantizer a summed current consumption of 28 µA. An SNR of 84.3 dB in the 20 kHz audio band was achieved, when considering the noise from the 1st integrator and the quantizer.**

***Keywords*—Delta-Sigma ADC, Continuous-time, Circuit optimization, Circuit noise analysis**

I. Introduction

When designing analog-to-digital convertes (ADCs) for audio applications, the Delta-Sigma ($\Delta\Sigma$) modulator is often the preferred choice. Generally there are two variants of $\Delta\Sigma$ ADCs: the discrete-time (DT) and the continuous-time (CT) implementations. The DT modulators rely on switched-capacitor filters to implement the integrators of the modulator.

For CT $\Delta\Sigma$ ADC there exist several different topologies for implementing the integrator; the dominant ones are the active-RC integrator and the Gm-C integrator. The active-RC integrator is an opamp based integrator, with an input resistor and a capacitor in the negative feedback loop around the opamp. The Gm-C integrator is based on an open-loop transconductor and an integration capacitor. There are different pros and cons for both integrator realisations, with the main one being the linearity of the active-RC integrator being better due to the negative feedback compared to the open-loop transconductor of the Gm-C integrator.

An important aspect of the $\Delta\Sigma$ ADC is the fact that most circuit non-idealities, including circuit noise and distortion, are noise shaped by the modulator. This is the case for all non-idealities generated inside the modulator loop. Thus the performance requirements of the quantizer and the 2nd and higher order integrators may be relaxed compared to the overall ADC performance. However, all non-idealities that are present at the input of the modulator are only filtered by the signal transfer function (STF) of the modulator. For low-pass modulators the STF is generally flat within the signal band, causing non-idealities at the modulator input also to be present at the output.

Several design procedures have been proposed in the past for optimizing the circuits for CT $\Delta\Sigma$ ADCs. In [1] Brückner et al. describe a design tool for optimization of the loop-filter coefficients with the aim of maximizing the signal swing of the internal nodes when realising the circuits for the modulator. In this context the modulator is not optimized with respect to current consumption and noise performance, but primarily in order to avoid distortion due to signal clipping. In [2], [3] Ortmanns and Gerfers describe in detail a Figure-of-Merit (FoM) based optimization method for CT $\Delta\Sigma$ ADCs that are realised using active-RC integrators. By analytically estimating each part of the FoM, it is possible for a given set of performance specifications to determine the minimum FoM that may be achieved for a given oversampling ratio (OSR) of the modulator. In this way the power consumption of the ADC is minimized. However, in their analysis the noise of the OTA used in the active-RC integrator is ignored. In [4] Pavan et al. present a power optimized CT $\Delta\Sigma$ ADC for audio applications. They present general considerations for low power modulator design with respect to the selection of topology, loop filter order, and quantizer resolution, while the main emphasis of the paper is on circuit level power optimization.

In this paper a new optimization method is proposed, where the modulator design is considered in combination with the circuit design in order to minimize the current consumption of the ADC. The presented method is based on the fact, that the performance of the first integrator directly affects the performance of the ADC, as the non-idealities of this integrator are not noise shaped by the modulator loop filter. For audio applications, where the sampling frequency is typically in the MHz range, the first integrator consumes the major part of the overall current of the $\Delta\Sigma$ ADC; thus the 1st integrator is the focus of the optimization. By considering the required current needed for the integrator to meet the ADC performance requirements and also taking the loop filter and quantizer levels into account, the ADC is optimized with regard to current consumption.

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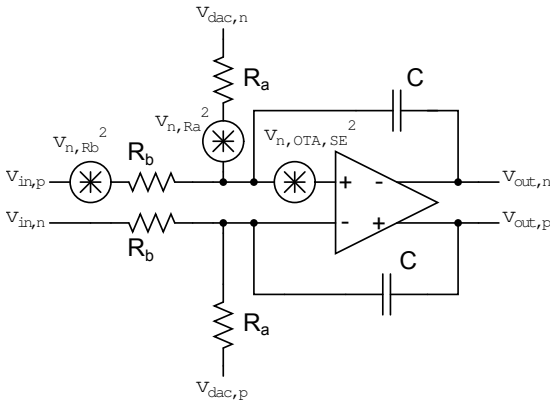

Figure 1. Fully differential active-RC integrator with single-ended noise sources

II. Optimization Method

In an active-RC integrator, as shown in Fig. 1, the loop filter coefficients are realised using resistors and capacitors, with the coefficient, k_i is given as:

$$k_i = \frac{1}{f_s R_i C} \tag{1}$$

where f_s is the ADC sampling frequency, and R_i and C are the values of the resistor and capacitor respectively. The active-RC integrator in Fig. 1 is a fully differential implementation intended for use as the 1st integrator of a CT $\Delta\Sigma$ ADC with a voltage based feedback DAC. From the figure two coefficients are realised using the resistors and capacitance: k_a is the feedback coefficient realised by R_a and C, and k_b is the feed-forward coefficient realised by R_b and C. It is seen, that the resistors R_b contribute noise directly at the input of the integrator and thus the modulator.

From (1) it is given that the R_iC product is fixed for a given value of k_i and f_s. Ideally the value of either R_i or C can be selected arbitrarily, with the other component given from the R_iC product. However, from a circuit noise perspective the value of R_i should be small in order to fulfil the the noise requirements of the integrator. Similarly the value of C should be small in order to reduce the current requirements of the OTA, due to requirements of the OTA with respect to the gain-bandwidth product (GBW) and the slew-rate (SR). The noise of the OTA should also be considered in this context, as it affects the noise performance of the integrator and thus the value of the integration resistors. From these observations, an optimum design must exist where the OTA biasing current is minimized and where the GBW and SR requirements of the OTA, and the noise requirements of the integrator are fulfilled.

The value of k_i is given from the loop filter. From [5] higher values of f_c results in larger modulator coefficients; from (1) this reduces the value of the R_iC product for a fixed f_s. Thus by also considering the value of f_c when designing the modulator, the current consumption of the integrator OTA may be reduced. However, increasing the f_c makes the noise-shaping of the modulator more aggressive, by increasing the high frequency gain of the noise transfer function (NTF). More of the quantization noise is pushed out of the band of interest and the total noise power is increased. This causes the modulator to become unstable at large input signal amplitudes, and thereby the maximum stable amplitude (MSA) is reduced.

From [5], the stability of the modulator may be improved by using a multi-bit quantizer, thus increasing the MSA of the modulator for a specific loop-filter. Alternatively the multi-bit quantizer can be used to increase the noise-shaping via a larger f_c without reducing the MSA. This in turn increases the integrator coefficients and thereby reduces the R_iC product. Increasing the number of levels in the quantizer does come at a cost, as the number of comparators needed increases by one per added quantizer level. Furthermore, decoding logic is required in order to convert the thermometer coded output of the comparators into a binary coded signal e.g. 2's complement or unsigned binary.

From these considerations it is clear that there exist a large design space when designing the loop-filter and the 1st integrator for the CT $\Delta\Sigma$ ADC. However, it also seems clear, that there must exist an optimum configuration that minimizes the current consumption of the ADC with respect to the OTA of the 1st integrator and the quantizer. By using a brute force method, a range of loop-filters and quantizers can be designed and combined, in order to analyse all modulator combinations with respect to the MSA and the quantization noise. Based on these results together with the associated CT loop-filter coefficients, the possible combinations of R, C and OTA current consumption can be evaluated for each modulator configuration in order to find the overall modulator configuration resulting in the minimum summed current consumption of the 1st integrator and the quantizer.

III. Circuit Analysis

In this section a circuit analysis of the fully differential active-RC integrator is carried out in order to determine an expression for the input referred noise (IRN) of the integrator. A fully differential folded-cascode OTA, to be used with the integrator, is also analysed with respect to the biasing current required to fulfil noise, GBW and SR specifications. These expressions are provided as they form the foundation of the optimization routine described in Sec. IV.

A. Noise of Integrator

To analyse the input referred noise of the fully differential integrator in Fig. 1, the input referred noise power at the input $v_{in,p}$ from the positive half-circuit can be analysed. The result is then multiplied by a factor of two, to get the differential noise power at the input; this follows as the noise of the two half-circuits is uncorrelated. The input referred noise can be split into two parts: a resistor part and an OTA part.

The thermal noise from a resistor R is given from [6] as:

$$v_{n,R}^2 = 4kTRf \tag{2}$$

where k is the Boltzman constant, T is the absolute temperature, and f is the frequency band of interest. From a circuit analysis of the active-RC integrator in Fig. 1, the integrator input referred noise from the resistors R_a and R_b is given as:

$$v_{\mathrm{IRN},R}^2 = 2\left(v_{n,Rb}^2 + \left(\frac{R_b}{R_a}\right)^2 v_{n,Ra}^2\right) \tag{3}$$

where $v_{n,Rb}$ and $v_{n,Ra}$ are the noise voltage sources from R_b and R_a respectively. From a similar analysis the input referred

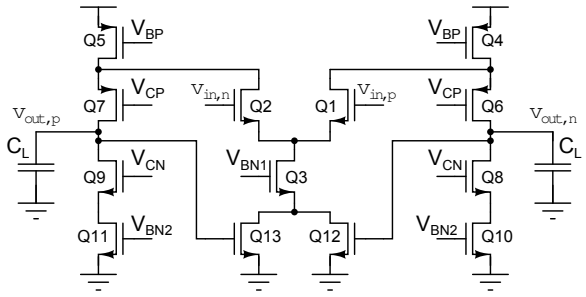

Figure 2. Fully differential folded-cascode OTA

noise of the OTA, $v_{\mathrm{IRN,OTA}}$, is given as:

$$v^2_{\mathrm{IRN,OTA}} = 2\left(\frac{4}{3}\pi^2 R_b^2 C^2 f_B^2 + \left(1+\frac{R_b}{R_a}\right)^2\right) v^2_{n,\mathrm{OTA,SE}} \tag{4}$$

where $v_{n,\mathrm{OTA,SE}}$ is the single-ended noise from the OTA. From (1) the integration capacitance C may be expressed as:

$$C = \frac{1}{k_b R_b f_s} = \frac{1}{2k_b R_b f_B OSR} \tag{5}$$

where OSR is the oversampling ratio of the modulator. Assuming that $OSR >> \pi$, and combining (5) and (4), $v^2_{\mathrm{IRN,OTA}}$ can be expressed as:

$$v^2_{\mathrm{IRN,OTA}} \approx 2\left(1+\frac{R_b}{R_a}\right)^2 v^2_{n,\mathrm{OTA,SE}} \tag{6}$$

For the modulator topology to have an input signal gain of 1 in the band of interest, $k_a = k_b$ which equals that $R_a = R_b$. Using this in (3) and (6), then the input referred noise (IRN) power of the integrator can be expressed as:

$$v^2_{\mathrm{IRN}} = v^2_{\mathrm{IRN},R} + v^2_{\mathrm{IRN,OTA}} = 4v^2_{n,Rb} + 8v^2_{n,\mathrm{OTA,SE}} \tag{7}$$

From (7) it is evident that in order to ignore the noise contribution of the OTA to the ADC's total input referred noise, as done in [3], then $v^2_{n,\mathrm{OTA,SE}} << v^2_{n,Rb}$. We find this to be an over-simplification, and believe that more low-current circuits may be achieved by including the OTA noise into the noise analysis of the ADC.

B. GBW and SR of Folded-Cascode OTA

As described in Sec. II the value of the integration capacitance in the active-RC integrator, impacts the current consumption of the OTA. It is thus relevant to estimate the biasing current related to a specific GBW and SR requirement. Referring to Fig. 2 and from [6] the GBW of the folded-cascode OTA is given as:

$$GBW = \frac{2I_{d1}}{V_{ov}C_L} \tag{8}$$

where I_{d1} is the drain current of Q1, V_{ov} is the transistor overdrive voltage, and C_L is the load capacitance. For the active-RC integrator in a CT $\Delta\Sigma$ ADC, C_L may be approximated by the integration capacitance C.

From [6] the SR of the folded-cascode OTA is given as:

$$SR = \frac{I_{d3}}{C_L} \tag{9}$$

The current flowing in Q4 equals the sum of the drain currents in Q1 and Q10. During a slewing condition all of I_{d3} will flow through either Q4 or Q5, depending on the input signal. In order to avoid that the transistors Q6-Q11 enter the triode region during an output slewing condition, the bias current of Q4 should be larger than Q3. This ratio M is here defined as:

$$M = \frac{I_{d4}}{I_{d3}} = \frac{I_{d4}}{2I_{d1}} \tag{10}$$

Using the definition in (10), the required biasing current of Q4 to obtain a specific GBW and SR of the OTA, may be expressed as:

$$I_{d4,GBW} = GBW \cdot M \cdot C_L \cdot V_{ov} \tag{11}$$

$$I_{d4,SR} = SR \cdot M \cdot C_L \tag{12}$$

These expressions may then be used during the optimization for a fixed value of M.

C. Noise of Folded-Cascode OTA

As it was the case for the integrator, the noise of the fully differential OTA may be analysed by considering the differential half-circuit of the OTA. This result may then be used in (7) to obtain the total input referred noise of the integrator. Referring to Fig. 2, and analysing the input referred noise at the positive input, $v_{in,p}$, only the transistors Q2, Q4 and Q10 contribute noise. Q6 and Q8 are cascoding devices and their noise may thus be neglected. Transistors Q3, Q12 and Q13 only add common-mode noise which may also be neglected at the differential input. From [6] the flicker noise as a function of the frequency is given as:

$$v^2_{n,1/f}(f) = \frac{K}{WLC_{ox}f} \tag{13}$$

where K is a device specific parameter, W and L are the MOSFET channel width and length repectively, C_{ox} is the gate capacitance per unit area, and f is the frequency. Since the flicker noise may be reduced by using large devices, it does not directly affect the required biasing current of the OTA. Indirectly it does affect the GBW and the phase margin of the folded-cascode OTA, as larger devices increase the parasitic capacitances in the internal nodes of the OTA. However, this effect is not considered here in order to simplify the analysis. Instead a part of the noise power budget is associated with the flicker noise of the OTA when optimizing the ADC.

From [6] the thermal noise of the MOSFET, when referred to the gate, is given as:

$$v^2_{n,th} = \frac{4}{3}kT\frac{V_{ov}}{I_d}f_B \tag{14}$$

Referring to Fig. 2, the thermal noise of the OTA referred to the *INP* input from Q1, Q4 and Q10 can be expressed as:

$$v^2_{n,\mathrm{OTA,SE}} = v^2_{n1} + \frac{g^2_{m4}}{g^2_{m1}}v^2_{n4} + \frac{g^2_{m10}}{g^2_{m1}}v^2_{n10} \tag{15}$$

where v_{nx} and g_{mx} are the noise voltage and transconductance of transistor Qx respectively. The currents flowing in the transistors are related by the factor M, and it is thus possible to express the transconductance and gate referred noise of Q4 and Q10 by those of Q1. From Fig. 2 and (10) the biasing current of Q10 can be expressed as:

$$I_{d10} = I_{d4} - I_{d1} = (2M-1)I_{d1} \tag{16}$$

Assuming that the overdrive voltage is the same for Q1, Q4 and Q10, then g_m of Q4 and Q10 can be expressed from M and g_{m1}:

$$g_{m4} = \frac{2 \cdot (2MI_{d1})}{V_{ov}} = 2Mg_{m1} \tag{17}$$

$$g_{m10} = \frac{2\left[(2M-1)I_{d1}\right]}{V_{ov}} = (2M-1) \cdot g_{m1} \tag{18}$$

Similarly the gate-referred thermal noise of Q4 and Q10 may be expressed from M and v_{n1}:

$$v_{n4}^2 = \frac{4}{3}kT\frac{V_{ov}}{2MI_{d1}}f_B = \frac{1}{2M}v_{n1}^2 \tag{19}$$

$$v_{n10}^2 = \frac{4}{3}kT\frac{V_{ov}}{(2M-1)I_{d1}}f_B = \frac{1}{2M-1}v_{n1}^2 \tag{20}$$

By combining (15) and (17)-(20) the input referred noise power at the $v_{in,p}$ input is:

$$v_{n,\mathrm{OTA,SE}}^2 = v_{n1}^2 + 2Mv_{n1}^2 + (2M-1)v_{n1}^2 = 4Mv_{n1}^2 \tag{21}$$

By inserting (14) into (21), the input referred thermal noise of the OTA may be expressed as:

$$v_{n,\mathrm{OTA,SE}}^2 = \frac{16}{3}MkT\frac{V_{ov}}{I_{d1}}f_B \tag{22}$$

Finally using (10) with (22), the biasing current of Q4 for a specific input referred noise power is given as:

$$I_{d4,\mathrm{IRN}} = \frac{32}{3}M^2kT\frac{V_{ov}}{v_{n,\mathrm{OTA,SE}}^2}f_B \tag{23}$$

IV. Applying Optimization Method

Based on the results of the analysis from Sec. III, primarily (2), (7), (11), (12), and (23), it is possible to determine the minimum bias current of Q4 where all requirements for GBW, SR and the input referred noise of the OTA are met. This may then be used to evaluate the current consumption of the different modulator configurations, in order to determine the minimum current solution.

Before carrying out the optimization procedure, some key specifications for the ADC are required. The range of f_c values for the loop-filter and the range of levels in the quantizer should be provided, in order to design all combinations of modulators. Next the SR and GBW requirements of the OTA for the 1st integrator are needed. The GBW may be set based on experience, and in [2] a recommended value of the GBW is 2-3 times f_s.

The slew-rate requirement of the OTA is highly dependent on the number of quantization levels in the feedback DAC, which is equal to the number of levels in the quantizer. Having a multi-bit quantizer, the step size of the feedback signal is smaller, thus reducing the required SR of the OTA. From [2], and with reference to Fig. 1, the maximum slew-rate, $SR_{\max}$, of the 1st integrator in a CT $\Delta\Sigma$ modulator can be expressed as:

$$SR_{\max} = \max\left[f_s\left(k_bV_{in}(t) - k_aV_{dac}(t)\right)\right] \tag{24}$$

where V_{in} is the modulator input and V_{dac} is the DAC feedback signal. Using (24) it is possible to estimate the maximum SR of a given modulator based on a simulation of the equivalent DT modulator.

Next, a noise budget for the ADC is needed, specifying the percentage of the total noise power of the ADC that is allocated to the different parts of the ADC. One possible budget split could be as follows:

- Quantization noise, $f_{np,\mathrm{quan}}$
- Noise from 1st integrator, $f_{np,\mathrm{int1}}$, split into:
  - → Resistor thermal noise, $f_{np,R}$
  - → OTA noise, $f_{np,\mathrm{OTA}}$, split into:
    - → OTA thermal noise, $f_{np,\mathrm{OTA,th}}$
    - → OTA flicker noise, $f_{np,\mathrm{OTA},1/f}$
- Noise from remaining modulator blocks, $f_{np,\mathrm{rem}}$

When optimizing the current consumption of the OTA, the values of $f_{np,R}$, $f_{np,\mathrm{OTA,th}}$, and $f_{np,\mathrm{OTA},1/f}$ may be fixed or swept as well. It is relevant to sweep the values of these parameters, while keeping the sum equal to $f_{np,\mathrm{int1}}$. This should be done, as a fixed noise split may not result in the optimal solution. There exist an optimum point where the OTA biasing current required to meet the thermal noise specification equals the larger of the biasing currents needed to fulfill the GBW and the SR specifications. At this point, the integrator resistance can not be increased without also increasing the OTA biasing current, to reduce the thermal noise of the OTA. Similarly a reduction of the resistance from this point increases the integrator capacitance, causing the OTA biasing current to be increased to fulfill either the SR or GBW specification, depending on which is the limiting factor.

From (11), (12) and (23) it is necessary to specify the V_{ov} for the OTA transistors, together with the factor M relating the bias currents of the folded-cascode OTA. In order to refer the quantization noise of the modulator to the input of the ADC, the input signal voltage equivalent to $0\,\mathrm{dBFS}$ is needed. Furthermore, to evaluate the current consumption of the quantizer from the number of quantizer levels, it is necessary to have an estimate of the current consumption of the comparator to be used. Finally the noise shaping order, the OSR, the f_B, and the feedback waveform should also be known.

When evaluating the summed current consumption of the OTA and the quantizer, it can be expressed as:

$$I_{\mathrm{sum}} = 2I_{d4,\min} + N_{\mathrm{quan}}I_{\mathrm{comp}} \tag{25}$$

where N_{quan} is the number of quantizer levels and I_{comp} is the current consumption of the comparator. The value of $I_{d4,\min}$ is the minimum biasing current for Q4 where all GBW, SR and thermal noise requirements are fulfilled. In (25) the overhead from the decoding network needed in the quantizer is not included. Also the current needed for bias generators has not been included.

Based on the listed information the optimization procedure is as follows:

1) Set f_c and find the modulator coefficients for the DT modulator
2) Find CT coefficients for the 1st integrator
3) Simulate the DT modulator to estimate the MSA, the peak signal to quantization noise ratio (SQNR), and $SR_{\max}$ for each quantizer configuration
4) Determine ADC input referred quantization noise power from estimated SNR, MSA and peak input signal level

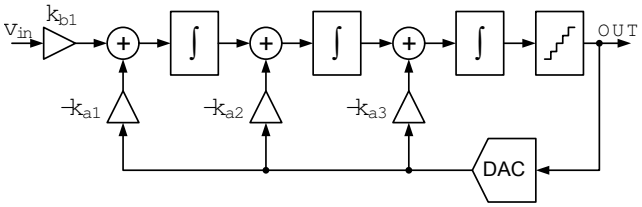

Figure 3. 3rd order CT ΔΣ modulator with CIFB topology

5) Set noise partition between resistor and OTA noise powers
6) Calculate maximum integrator resistance from noise budget
7) Calculate integrator capacitance from integrator resistance and coefficients
8) Determine biasing current of Q4 to meet GBW, SR, and the OTA thermal noise requirement
9) Determine summed current consumption of OTA and quantizer from (25) for each quantizer configuration
10) Adjust noise power partition between resistor and OTA noise powers, and repeat step 6-9
11) Repeat step 2-10 for all values of f_c
12) Find the design solution with the minimum value of I_{sum}

The method is a brute force method, and thus the larger the set of values for f_c and quantizer levels, the longer computational time is required to carry out the optimization method. Since it is necessary to provide a set of given parameters when carrying out the optimization procedure, the found solution is not necessarily the global minimum in the design space. Knowledge of CT ΔΣ modulators and circuit level realisation of the blocks is therefore necessary in order to achieve a useful result.

V. Design Example

As an example of the application of the optimization method, a 3rd order CT ΔΣ ADC for the audio signal range has been designed. A block diagram of the ADC is shown in Fig. 3, showing that the topology is a cascade of integrators with feedback [7]. The DAC is voltage based with a non-return-to-zero (NRZ) type feedback signal. The ADC is fully differential and all integrators are realised as active-RC integrators.

The optimization method has been implemented as a MATLAB script, for easy simulation and performance evaluation of the modulators when carrying out the optimization. The loop filters were designed from a Butterworth prototype filter using the MATLAB Signal Processing Toolbox. The loop filter coefficients were converted from the DT to the CT domain, using the impulse invariant method [8]. In this design example only the OTA for the 1st integrator and the quantizer have been realised at transistor level. The remaining blocks are ideal and have been modelled with Verilog-AMS. The circuits were implemented in a 0.18 µm process with a 1.8 V supply voltage. The design parameters used for the optimization are listed in Table I.

From the optimization the resulting minimum I_{sum} values for all quantizer variants are shown in Fig. 4, with a minimum current obtained for the solution using 7 levels in the quantizer.

Table I. Design parameters used for the optimization of the 3rd order CT ΔΣ ADC

Parameter	Value	Parameter	Value
Modulator order	3	SNR	84 dB
f_c range	150 kHz - 400 kHz	f_c sweep step	1 kHz
DAC type	NRZ	Feedback signal	Voltage
f_B	20 kHz	f_s	2.4 MHz
M	1.2	$V_{\text{in,FS}}$	1.4 V_{p}
V_{ov}	100 mV	GBW	7.2 MHz
N_{quan}	3 - 9	I_{comp}	1.25 µA
$f_{np,\text{int1}}$	55 %	$f_{np,\text{quan}}$	20 %
$f_{np,\text{rem}}$	25 %	$f_{np,\text{OTA},1/f}$	50 %

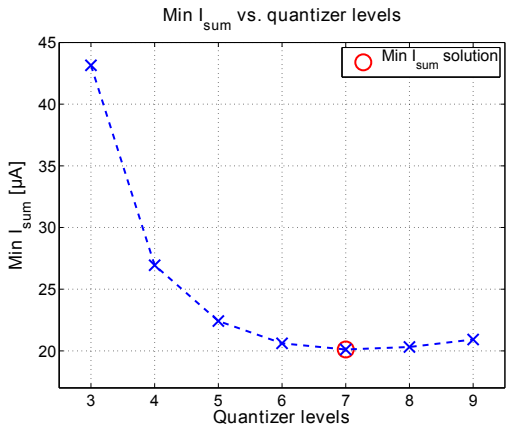

Figure 4. Minimum I_{sum} vs. number of quantizer levels for optimized modulators

The associated ADC design parameters are are listed in Table II together with the results from simulation of the ADC.

A circuit diagram of the folded-cascode OTA is shown in Fig. 2. Linear common-mode feedback was used, with the transistors Q12 and Q13 operating in the triode region. All transistors used were normal threshold transistor except Q12 and Q13 that were native NMOS transistors; this was in order to increase the output swing of the OTA. The common-mode output voltage was set to 0.9 V to maximize the differential output signal swing.

The schematic for the clocked comparator used in the design, is shown in Fig. 5. It consists of a preamplifier and a dynamic latch, with the latch being based on a design presented in [9]. The preamplifier was added in order to reduce the kick-back noise at the comparator inputs. At a sampling frequency of 2.4 MHz the total current consumption of the comparator alone is 1.25 µA. The quantizer was implemented as a FLASH ADC with six comparators, a reference generator and a digital decoding block. The reference voltages were generated using a string of resistors. The digital decoder block, realised using

Table II. Summary of results from optimization and simulation

Parameter	Value	Parameter	Value
Quantizer levels	7	f_c	398 kHz
k_{b1}	0.5047	k_{a1}	0.5047
k_{a2}	1.1319	k_{a3}	1.3744
R_a, R_b	711 kΩ	C	1.16 pF
Target $\text{SNR}_{\text{q+int1}}$	85.2 dB	Realised $\text{SNR}_{\text{q+int1}}$	84.3 dB
Target MSA	-2.25 dBFS	Realised MSA	-2.9 dBFS
Target I_{sum}	20.1 µA	Realised I_{sum}	28.1 µA

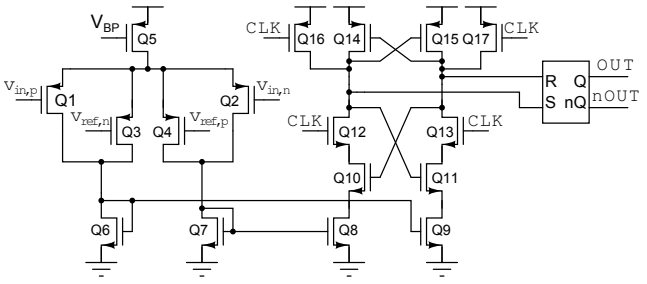

Figure 5. Fully differential clocked comparator

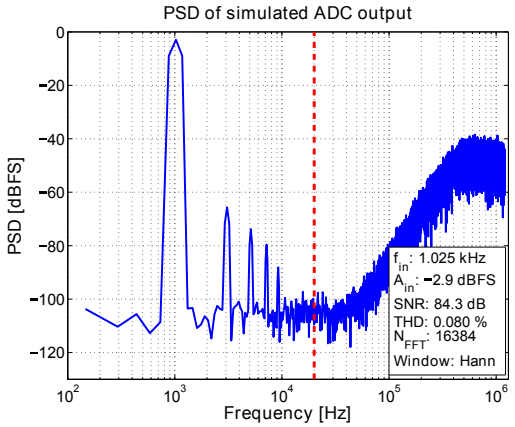

Figure 6. PSD of simulated ADC output, with dashed line indicating the signal bandwidth

standard cells, was used to convert the thermometer coded output of the comparators into a 3-bit unsigned binary output signal. All transistors used were normal threshold transistors.

The designed CT $\Delta\Sigma$ ADC was simulated with the transistor level implementations of the 1st integrator and the quantizer, and using Verilog-AMS models for the remaining blocks. The simulations were carried out as transient noise simulations, in the typical process corner and with $T = 300\,\mathrm{K}$, and using a 1 kHz sine wave input.

The PSD plot of the ADC output is shown in Fig. 6, including key performance parameters. As seen from the results in Table II and in Fig. 6, the SNR from the optimization was almost achieved with the design; the difference primarily being due to the lower realized MSA. Note that the target and achieved SNR values in Table II and in Fig. 6 are only for the quantization noise, and the flicker and thermal noise from the 1st integrator; this explains the higher SNR compared to the value specified for the optimization in Table I. However, the current consumption of the design is approx 40 % above the target.

VI. Discussion and Future Work

From the results of the design example in Sec. V, it is clear that based on the circuit analysis the estimated summed current consumption of the OTA and the quantizer are too optimistic. This is to be expected, as the circuit analysis was based on the Schichman-Hodges models for the MOSFET transistor operation and the expression for the transistor thermal noise, which does not take process specific details into account. Parasitic components of the circuits have also been ignored in the analysis. Nevertheless, the obtained minimum current design solution can still be considered as optimum, since the increase in the necessary current consumption can be expected to be the same for all optimization solutions. This follows as all solutions are realised using the same circuit topologies. For general application of the method, the estimated biasing currents have not been multiplied by a compensation factor to fit with the transistor models used for the circuit simulations.

Future work includes the adding scaling of the loop filter coefficients to the optimization method. Distortion generated by the 1st integrator is added to the $\Delta\Sigma$ ADC output, thus by scaling down the k_a and k_b coefficients and thereby reduce the output signal swing of the 1st integrator, the distortion in the ADC output can be reduced. However, adjusting the loop filter coefficients changes the associated RC product, as discussed in Sec. II. Thus it has an impact on the current consumption of the 1st integrator. A specification of the maximum total harmonic distortion of the ADC would then be needed as an input parameter for the optimization routine.

VII. Conclusion

In this paper an optimization method for the design of low power CT $\Delta\Sigma$ ADCs has been presented. The method optimizes the current consumption of the OTA of the 1st integrator and the quantizer, by determining the optimum choice of loop-filter coefficients, quantizer levels, and integrator resistor and capacitor values. This choice is based on a specified noise performance of the ADC, and by using the derived expressions for the biasing current of the OTA with respect to the GBW, SR and noise requirements of the integrator. A designed example was given for the design of a fully differential 3rd order CT $\Delta\Sigma$ ADC, realised with active-RC integrators and a folded-cascode OTA. Based on the design example it was shown, that the estimated current consumption is optimistic, but nevertheless the optimized modulator and circuit solution provides a good starting point for designing the subblocks of the ADC, with a minimum current consumption.

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D

Low Power Continuous-Time Delta-Sigma ADC with Current Output DAC

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Low Power Continuous-Time Delta-Sigma ADC with Current Output DAC

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***Abstract*—The paper presents a continuous-time (CT) Delta-Sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) using a current output digital-to-analog converter (DAC) for the feedback. From circuit analysis it is shown that using a current output DAC makes it possible to relax the noise requirements of the 1st integrator of the loopfilter, and thereby reduce the current consumption. Furthermore, the noise of the current output DAC being dependent on the ADC input signal level, enabling a dynamic range that is larger than the peak signal-to-noise ratio (SNR). The current output DAC is used in a 3rd order multibit CT $\Delta\Sigma$ ADC for audio applications, designed in a 0.18 µm CMOS process, with active-RC integrators, a 7-level Flash ADC quantizer and current output DAC for the feedback. From simulations the ADC achieves a dynamic range of 95.0 dB in the audio band, with a current consumption of 284 µA for a 1.7 V supply voltage; the resulting figure-of-merit is 262 fJ/conversion.**

***Keywords*—Delta-Sigma ADC, Continuous-time, Current output DAC, Low power design**

I. Introduction

Delta-Sigma ($\Delta\Sigma$) analog-to-digital converters (ADC) are typically used for audio applications due to the high signal-to-noise ratio (SNR) this type of ADC can achieve. Most non-idealities generated in the $\Delta\Sigma$ ADC are noise shaped by the modulator, making only few of the circuit blocks critical in the design. Thus low power blocks can be used while still achieving high performance. With the signal bandwidth being only 20 kHz for audio, a high oversampling ratio may be achieved with a sampling frequency of a few MHz.

Continuous-Time (CT) $\Delta\Sigma$ ADCs are typically used in high frequency applications, as the continuous-time integration of the signals relaxes the speed requirements of the integrator circuits [1]. In the past years there has been an increasing focus on using CT $\Delta\Sigma$ ADCs for audio applications, as the relaxed speed requirements of the integrators also allows for reduction of the ADC power consumption in this frequency range. S. Pavan has proposed several CT $\Delta\Sigma$ ADCs with excellent performance results [2], [3], and provided methods for optimizing the current consumption of the ADCs through optimization of the circuit blocks.

In [4] a new optimization method was proposed, with focus on the reduction of the current consumption of the critical 1st integrator in the loopfilter. As a continuation of the work in [4], this paper present a new CT $\Delta\Sigma$ ADC that uses a current output digital-to-analog converter (DAC) in order to further reduce the current consumption of the 1st integrator. The usage of a current output DAC is shown to also make the ADC noise floor input signal dependent, making it possible to optimize the noise performance of the ADC for low input signals; this at the cost of a lower peak SNR. This is useful in applications where the dynamic range is more important than the peak SNR, eg. in hearing aids and consumer microphones for mobile phones.

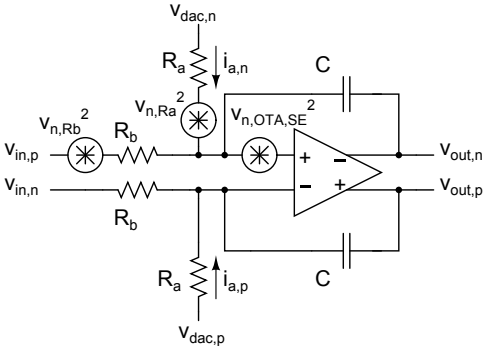

Figure 1. Fully differential active-RC integrator with single-ended noise sources

II. Noise Analysis

In a $\Delta\Sigma$ ADC the 1st integrator of the modulator is the most critical block, as the input referred noise of this integrator is not noise shaped by the loopfilter. Thus the integrator should be carefully designed in order to achieve the required ADC noise performance at a minimum current consumption. For audio applications high linearity is typically required, and this makes an active-RC integrator, as shown in Fig. 1, the optimal choice for the 1st integrator of the CT $\Delta\Sigma$ ADC.

For an active-RC integrator the relationship between the CT $\Delta\Sigma$ modulator coefficients and the resistor and capacitor values is given as:

$$k_i = \frac{1}{f_s R_i C} \tag{1}$$

where k_i is the *ith* loopfilter coefficient as shown in Fig. 2, f_s the ADC sampling frequency, R_i the associated resistor, and C the integration capacitance.

From (1) the RC product is dictated by the sampling frequency and loopfilter coefficient. However, the R and C values can be chosen arbitrarily while keeping the RC product constant. The resistor directly affects the noise performance of the integrator via the resistor thermal noise, whereas the capacitor affects the gain-bandwidth product (GBW) and the slew-rate (SR) of the operational transconductance amplifier (OTA) used for the integrator. This in turn affects the OTA bias current and thereby the thermal noise; thus the selection of both R and C affects the integrator noise.

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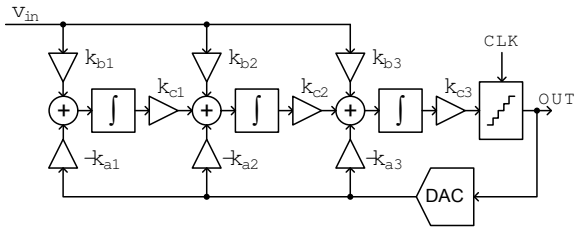

Figure 2. Block diagram of 3rd order modulator with CIFB-FF topology

By analysis of the fully-differential active-RC integrator shown in Fig. 1, it can be found that the noise of the OTA, referred to the integrator input, is given as:

$$v^2_{\mathrm{IRN,OTA}} \approx 2\left(1+\frac{R_b}{R_a}\right)^2 v^2_{n,\mathrm{OTA,SE}} \qquad (2)$$

where $v_{n,\mathrm{OTA,SE}}$ is the single-ended noise voltage of the OTA.

The ratio R_b/R_a also relates to the gain of the modulators signal transfer function (STF). For the modulator in Fig. 2, the STF gain at frequencies close to DC is approximately given as the ratio k_{b1}/k_{a1}. For a unity gain STF this requires that $R_{a1} = R_{b1}$. From (2) note that for the case of $R_a >> R_b$ the noise of the OTA is directly input referred to the integrator input; the input referred noise power of the OTA is thus reduced by a factor of 4 in comparison to when $R_a = R_b$. However, for $R_a > R_b$ the STF gain is larger than unity and thereby reduces the maximum stable amplitude (MSA) of the modulator.

An alternative solution is to replace the feedback resistors, R_a, and the voltage feedback signals, $V_{dac,p}$ and $V_{dac,n}$, by the equivalent currents, $i_{a,p}$ and $i_{a,n}$. For an ideal current output DAC the output impedance is infinity, making the impedance looking into the feedback loop infinity; thus $Z_a >> R_b$ and the noise of the OTA is directly referred to the integrator input. Furthermore, a unity gain STF may still be achieved by proper scaling of the feedback current.

By using a current output DAC instead of a voltage output DAC, it is possible to relax the noise requirements of the OTA without increasing the noise of the integrator. Assuming that the thermal noise is limiting the minimum biasing current of the OTA, this allows for a reduction of the OTA biasing current. Alternatively the reduced noise from the OTA may be used to relax the noise requirements in other parts of the modulator.

The output noise of the DAC is now present as a noise current. From Fig. 2 the input referred noise of the ADC from the 1st integrator and the current feedback DAC, is given as:

$$v^2_{\mathrm{IRN}} \approx 2\left(v^2_{n,Rb} + v^2_{n,\mathrm{OTA,SE}} + i^2_{n,\mathrm{DAC}}R_b^2\right) \qquad (3)$$

where $v_{n,Rb}$ is the noise voltage of R_b, and $i_{n,\mathrm{DAC}}$ the noise current of the DAC.

III. Circuit

The design of the CT $\Delta\Sigma$ ADC was based on the optimization method presented in [4]. The method is based on the ability to increase the corner frequency of the modulator noise transfer function (NTF) by increasing the number of quantization levels in the modulator output. From [5] a larger NTF corner frequency results in larger loopfilter coefficients, which from (1) reduces the RC product. Thereby the noise and the biasing current of the 1st integrator may be optimized. Using predefined requirements for the integrator noise, and the GBW and SR of the OTA, an optimal solution can be found where the total current consumption of the 1st integrator and the quantizer is minimized.

A. Modulator topology

The modulator has been designed with a 3rd order loopfilter, using a cascade of integrators with feedback and input feedforward (CIFB-FF) topology as shown in Fig. 2. The ADC signal bandwidth is 20 kHz and the sampling frequency is 2.4 MHz, both set by application requirements, and resulting in an oversampling ratio of 60. As a result of the optimization method, the modulator uses a multibit quantizer with 7-levels and has a NTF corner frequency of 475 kHz.

The feedback DAC signal is non-return-to-zero (NRZ), as this in combination with a multibit quantizer reduces the clock jitter sensitivity of the modulator. Feedforward of the input signal was used in order to reduce the signal swing at the output of the integrators by having $k_{ai} = k_{bi}$ for the *ith* feedback, thus avoiding clipping for large signals. Note that the input signal is not forwarded to the quantizer input, to avoid an additional summing circuit at this node. Because of this the value of k_{c3} is implicitly equal to 1.

When using active-RC integrators, the loopfilter coefficients are related to the RC product, which is very sensitive to process variations. Instead of using coefficient tuning, the coefficients have been scaled in order to avoid the modulator from becoming unstable due to process, temperature, and voltage variations, at the cost of a non-optimal NTF.

B. Integrators

The integrators were realised as active-RC integrators using fully-differential folded cascode OTAs with linear common-mode feedback (CMFB), as shown in Fig. 3. The folded cascode was chosen due to the good compromise between noise, speed and gain [6]. Due to the input feedforward in the modulator, the limited output swing of the folded cascode OTA is not critical in the 1st and 2nd integrator. However, since the modulator input is not forwarded to the input of the quantizer, the OTA of the 3rd integrator needs to process both the quantization noise and the signal. Distortion of the output of the 3rd integrator due to clipping in the OTA is noise shaped; nevertheless the OTA may still saturate and reduce the modulator order. To compensate for this, the folded-cascode OTA for the 3rd integrator was modified by removing cascode transistors, Q8 and Q9, of the current sinks. This reduces the gain of the OTA, but improves the output signal swing asymmetrically by an amount equal to the overdrive voltage of the cascode transistors. With the other two integrators having a large gain, this does not significantly affect the noise floor of the modulator. The output common-mode level of the 3rd integrator was not shifted due to the input range of the comparators in the quantizer.

C. Quantizer

The quantizer has been implemented as a 7-level fully-differential Flash ADC, with the comparators consisting of a preamplifier and a dynamic latch. The preamplifier was used for reducing kick-back noise at the comparators inputs and reduce the decision time. Also the dynamic latch uses minimum sized transistors for high speed operation. The reference voltages for the comparators were generated using a resistor tree supplied by a reference voltage. Finally the

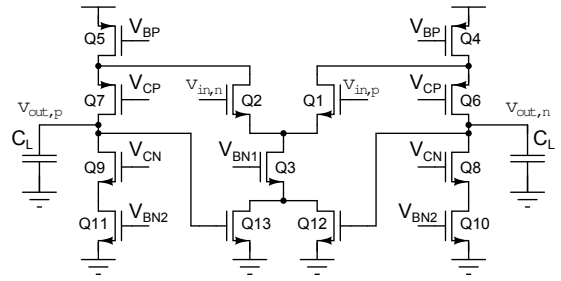

Figure 3. Fully differential folded-cascode OTA with linear CMFB

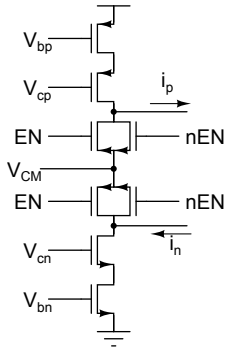

Figure 4. Schematic of bipolar cascode current cell

quantizer contains digital logic for converting the thermometer coded outputs of the comparators into a 2's complement representation with the output values $\{$-3,-2,-1,0,1,2,3$\}$.

D. Current Output DAC

The DAC was implemented as a current output DAC, thus requiring a separate DAC for each feedback path in the modulator, resulting in three identical DACs. Each DAC has 7 output levels and were implemented as a bipolar design to represent the 7-level 2's complement output of the ADC. With the loopfilter signal path being fully-differential, the output of the DAC is both a positive and a negative current with equal numerical value. The outputs were connected to the OTA inputs using a switch array. Depending on the sign of the feedback value, the positive current is either connected to the positive or negative OTA input, and vice versa for the negative current.

Having only 7 output levels the DAC was implemented with three bipolar unary current cells. To achieve a high output impedance the current sources were implemented as cascode current sources, as shown in Fig. 4. The generation of the specific current values needed to represent the equivalent feedback signals was done based on a reference current being input to the current cell wide-swing current mirror bias circuit. With the reference current being generated on-chip, the numerical value of the current will also be affected by process and temperature variations, thus affecting the realized feedback coefficients. As described in Sec. III-A this variation was compensated in the design of the modulator loopfilter.

Due to the differential signal path of the loopfilter, when a current cell is connected to an OTA input, both the current source and current sink are connected to the OTA. Since the DAC is multilevel not all current cells are necessarily connected to an OTA at a given time; when a bipolar current cell is not connected to an OTA input, the current source and current sink are connected directly via the pass gates. Since they source and sink the same numerical current, this approach keeps the transistors in the saturation region at all times. When the current cells are disconnected, the voltage of the outputs of the current source and sink are kept at the common-mode level of the OTAs. In this way the parasitic capacitancens of the current cell output nodes are not charged and discharged when the nodes are connected and disconnected to the OTAs.

With the DAC output being bipolar and with 7 quantization levels, for the feedback value of zero no current is fed to the inputs of the integrator OTAs; thus no noise current is injected into the integrator inputs. The DAC output noise is therefore heavily dependent on the input level of the modulator. By design the ADC noise is dominated by the noise from the 1st integrator OTA and input resistor for small input levels.

Digital logic is used at the input of the DAC to control the current cells based on the 2's complement output of the quantizer. With only three current cells in each feedback DAC and a fully-differential signal path, dynamic element matching (DEM) was not considered necessary to reduce harmonic distortion due to mismatch in the DAC. Without DEM and only simple decode logic, the delay in the DAC is below 4 ns, which is less than 1% of the sampling period. Thus no excess loop delay compensation has been used in the modulator.

Table I. SUMMARY OF SIMULATED PERFORMANCE OF THE CT $\Delta\Sigma$ ADC IN TYPICAL PROCESS CORNER AT 27°C

Parameter	Value
Supply voltage / Process	1.7 V / 0.18 µm
Bandwidth / Sampling frequency	20 kHz / 2.4 MHz
$V_{FS,diff}$ / V_{CM}	1.52 V / 0.85 V
Current consumption	284 µA
MSA / Peak SNR amplitude	-0.6 dBFS / -2.5 dBFS
Dynamic range / SNR / SNDR	95.0 dB / 75.7 dB / 72.4 dB
Active area	0.37 mm^2
FoM	262 fJ/conv.

IV. SIMULATION RESULTS

The ADC was evaluated using transient noise simulations, including thermal and flicker noise and with transistor models for all circuit blocks, but without extracted layout parasitics. Simulations of the modulator and subblocks have been carried out exhaustively in the typical process corner at 27°C; other process and temperature corners have only been simulated to evaluate the modulator operation. The simulated performance is summarized in Table I, showing a 95.0 dB dynamic range, with a MSA of -0.6 dBFS and a total current consumption of 284 µA. The peak SNR is only 75.5 dB, which follows from the signal dependent noise of the DAC. This behaviour can be observed from Fig. 5, showing the simulated SNR and signal-to-noise-and-distortion ratio (SNDR) of the ADC for a 2 kHz sine input signal. Up to an input level of -30 dBFS the SNR curve increases with an almost constant slope for increasing input levels; above -30 dBFS the curve starts to flatten and saturates above -18 dBFS. For input levels below -30 dBFS the noise of the resistors and OTA of the 1st integrator dominates. Above -30 dBFS the DAC noise dominates and keeps increasing as the modulator activity increases with the input signal level. This result underlines the usage of the CT $\Delta\Sigma$ ADC with a current output DAC in applications where low noise at low input levels is more critical than a large peak SNR. The same behaviour can be seen from Fig. 6 where the

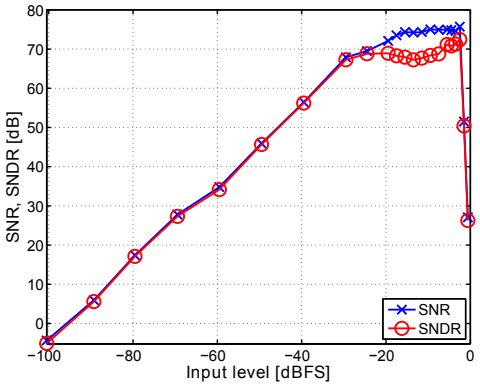

Figure 5. Simulated SNR and SNDR of ADC, for 2 kHz input signal

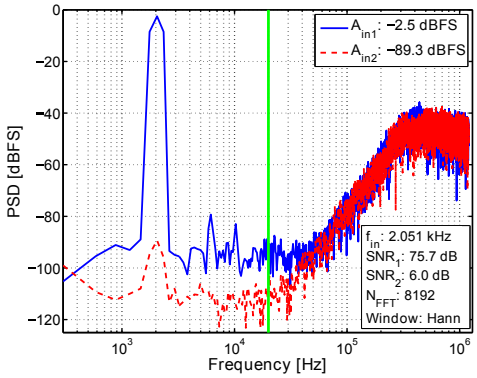

Figure 6. PSD of simulated ADC outputs, using averaging of two simulations. Vertical line indicates bandwidth.

power spectral density (PSD) plot of the ADC output for a small and large input signal level are shown.

The SNDR curve in Fig. 5 follows the SNR curve, but starts to drop for input levels above -18 dBFS. The drop in SNDR is mainly caused by input switches, used for input selection, and possibly also from the 3rd integrator, where input feedforward was not applied. However, the drop in SNDR reaches a minimum at the -14 dBFS input level and then increases again for higher input levels. At the time of writing, the authors have no explanation for this behaviour.

To compare the designed ADC with state of the art CT $\Delta\Sigma$ ADCs for audio applications, the Figure-of-Merit (FoM) from [1] was used:

$$FoM = \frac{P}{2 \cdot BW \cdot 2^{\frac{DR-1.76dB}{6.02dB}}} \quad (4)$$

From the simulation results the ADC achieves a FoM of 262 fJ/conv., and is listed in Table II together with state-of-the-art designs in the field. The low FoM merit achieved is comparable to the best designs presented in the literature. However, the performance needs to be verified with chip measurements, and the FoM is then expected to be higher. A test chip with the designed CT $\Delta\Sigma$ ADC has been taped-out in a 0.18 µm CMOS process; the layout is shown in Fig. 7.

V. Conclusion

Using a current output feedback DAC in a CT $\Delta\Sigma$ ADC with active-RC integrators, relaxes the noise requirements of

Table II. Comparison of FoM with other audio CT $\Delta\Sigma$ ADCs

Reference	Tech.	BW	DR	Power	FoM [fJ/conv.]
[2]	180 nm	24 kHz	93.5 dB	90 µW	49
[3]	180 nm	24 kHz	103 dB	280 µW	61
[7]	40 nm	24 kHz	101 dB	1.7 mW	386
[8]	180 nm	20 kHz	101.3 dB	1.1 mW	290
[9]	130 nm	20 kHz	83 dB	60 µW	130
This work, simulated	180 nm	20 kHz	95.0 dB	482 µW	262

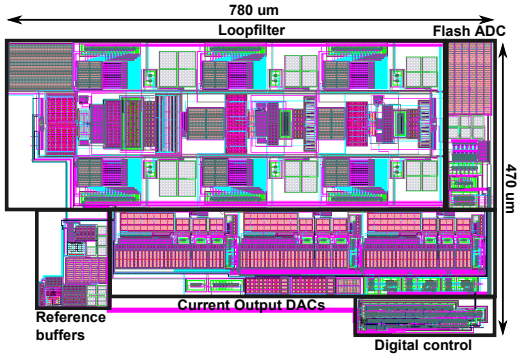

Figure 7. Layout of the CT $\Delta\Sigma$ ADC

the integrators and thereby allows for a reduction of the current consumption of the ADC. A 3rd order CT $\Delta\Sigma$ ADC using current output DACs has been presented, and based on simulations the ADC achieves a dynamic range 95.0 dB while consuming 284 µA at 1.7 V supply voltage in a 0.18 µm CMOS process. The peak SNR is 20 dB below the dynamic range, due to the signal level dependent noise of the DAC being the dominant noise source for large input levels. Based on simulations the resulting FoM is 262 fJ/conv, being in the range of the state-of-the-art. The ADC has been taped-out and the authors are currently awaiting the IC for evaluation.

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E

How to Implement an Experimental Course on Analog IC Design in a Standard Semester Schedule

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How to Implement an Experimental Course on Analog IC design in a Standard Semester Schedule

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***Abstract*— One of the challenges in teaching integrated analog electronics is that it is difficult to offer courses where the students can design, layout and tape-out a circuit and subsequently perform measurements on the device due to the long turn-around time in IC fabrication. In this paper it is described how the sequences of courses in integrated analog electronics at the Technical University of Denmark have been modified to enable this. It is outlined how a course can be designed using the three elements in constructive alignment: intended learning objectives, teaching activities and assessment. As an example it is described in detail how a new course is designed. The course is the first of two new courses and the scope of the course is to teach the students the flow an IC designer has to go through when designing analog circuits. Additionally the course has a large focus on strengthening the generic engineering competences of the students. This is achieved by running the course as a project in a company with status meetings and a review meeting where the teacher acts as a manager. Finally, the course evaluation based on the Course Evaluation Questionnaire (CEQ) is presented and based on this future improvements to the course are discussed.**

I. Introduction

Analog integrated circuits remain an important part of electronics today, and are practically present in all system-on-chip (SoC). Highly skilled and experienced engineers within integrated circuit design are thus still in high demand.

Integrated circuit design requires a high level of theoretical and analytical skills. However, practical experience is equally important due to vast design space and complex tools. Optimizing circuits using the available Electronic Design Automation (EDA) tools is a craftsmanship, and this requires years of experience to create state-of-the-art circuits.

Today the teaching of analog IC design at universities is most often focused on analytical skills and general circuit theories. The practical aspect is limited to schematic level simulations and possibly layout of circuit blocks. Full synthesis of a circuit, as shown in Fig. 1, including schematic level design, corner simulations, full-circuit layout, design-rule-checking (DRC) and layour-versus-schematic checking (LVS) before tape-out, is not possible to teach in a standard semester course. The multi-project-wafer (MPW) schedule of the foundry and the fabrication time for an IC of typically 3 months makes it practically impossible to incorporate the tape-out of an IC in a standard 13 week semester course. In a master thesis project, carried out over a period of 5 months, the same time-constraints apply. Overall this limits the possibility of the student to gain experience with the full design flow of an analog IC during his/her engineering studies.

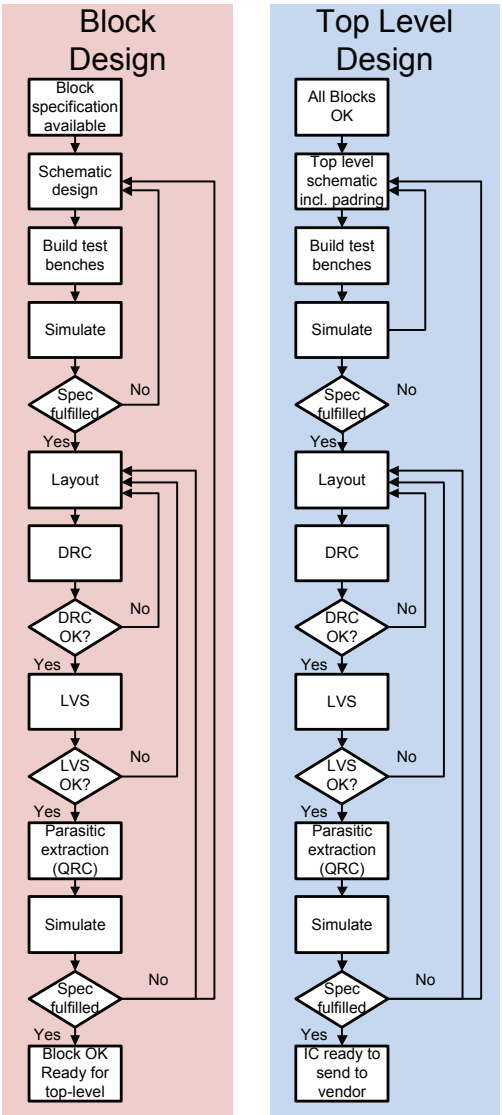

Fig. 1 The flow for analog circuit design and chip assembly.

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This paper concerns the design and implementation of a new course specifically aimed at teaching students the practical aspects of analog IC design, and focusing on the full design flow.

The outline of the remaining part of this paper is as follows: In section II is described the planning of the sequence of courses in analog IC design at DTU, incorporating two new practical courses. Section III presents a general strategy for designing courses based on constructive alignment [1], [2]. These strategies are used in section IV for implementing the course "Design and Layout of Integrated CMOS Circuits", [3]. This section also describes the important aspect of including in the course the development of the students' general engineering competences [4]. Section V present the students' learning in the course, based on the Course Experience Questionnaire (CEQ). A conclusion is given in Section VI.

II. Course sequence and new Experimental Courses

At the Technical University of Denmark (DTU) a semester is divided into two parts. First, a 13 weeks period mainly used for courses based on one weekly lecture and appertaining exercises followed by examination. The workload in the 13 week period is rated to 25 ECTS (European Credit Transfer System) points where a typical course is rated to 5 ECTS points. Second, after the 13 week examinations a 3 weeks period follows rated to 5 ECTS points. In this period the students typically work full time on a single project.

Up until a year ago no course was offered at DTU where a student had the opportunity to design a circuit on an IC, tape it out and subsequently perform measurements on the designed circuit. As discussed in the introduction the main reason for this being that the processing time for ICs is approximately 3 months, meaning that design of circuitry and tape out cannot be done within the time limits of a normal semester. The original sequence of courses in analog integrated circuit design at DTU is shown at the top of Fig. 2. It consists of two traditional lecture courses in integrated analog electronics [5], [6], a course in circuit synthesis where the students are offered the opportunity to design a circuit (without tape out) [7] and finally the M.Sc. thesis project.

To offer courses where a circuit can be designed and manufactured, two new courses have been created as shown in at the bottom of Fig. 2. The general idea is to separate the two course in time by approximately half a year to enable processing of the ICs in between the two courses. The 3 week period in the 8th semester takes place in June and here the first course "Design and Layout of an Integrated Circuit" [3] is allocated to design and layout an integrated circuit. All designs are assembled on a single chip that is taped out. The fabrication and handling of the IC is then performed in the period between the two new courses and thus the students are able to return for the 9th semester 3 week period in January to characterize the design they made. Both courses are rated to 5 ECTS points.

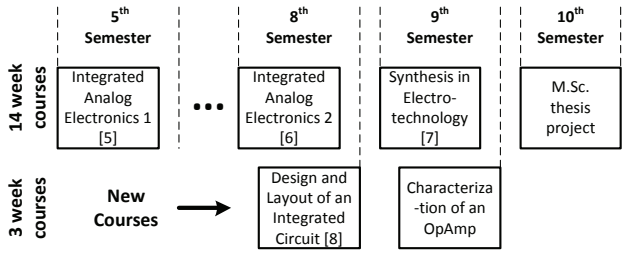

Fig. 2 Recommended course sequence in integrated analog electronics at DTU including two new experimental courses.

In the period between the two new courses the students are offered the course "Synthesis in Electrotechnology" [7] which is offered in a 5 or 10 ECTS point version. In the course the students agree with a teacher on an individual design tasks in any subject related to electronics. Often this course was used to introduce the students to the design flow of integrated analog electronics but as this is now done in the first of the two new courses more advanced topics can be addressed in this course.

III. Development of a Course

Over the last decade there has been an increasing focus on higher learning at universities and a large amount of research has gone into learning how students learn [1], [2]. To design a course many approaches exist and here constructive alignment [1], [2] is used. Constructive alignment uses three elements in the course planning (intended learning objectives, teaching activities and assessment) with the primary focus to increase student learning and competences as illustrated in Fig. 3. In the following the three elements in the course planning is described as a sequential process but in practice it is an iterative process where the three elements are revisited until they are aligned. Also, the three elements should be revised after the final course evaluation to ensure that the student learning and ILOs are aligned.

A. The Intended Learning Objectives (ILO)

The first step in planning the course is to identify the intended learning objectives (ILO). The ILOs are short statements of what a student will be able to do if they are met, i.e., what one would like the students to learn. For the teacher the ILOs serve two purposes. First, the ILOs greatly help to plan the course and the teaching activities (TA) as they serve as the goal for the teaching. Second, at the end of the course they are also very useful when designing an examination and

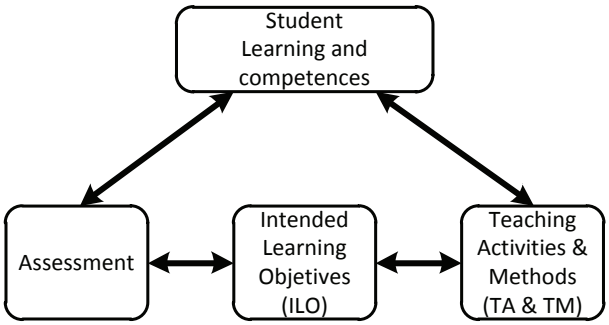

Fig. 3 A model for constructive alignment [1].

finally when assessing the students. When formulating the ILOs it is important to ensure that they address both lower and higher level learning, e.g., according to the SOLO [1] or Bloom's taxonomy [1], [2], [8].

The students also have great use of the ILOs, e.g., in case a written report is the basis for the assessment then the ILOs show the student the topics to cover in the report.

B. The Teaching Activities (TA) and Teaching Methods (TM)

Once the ILOs are made the teaching activities (TA) are planned and along with these the teaching methods (TM) are chosen. The TMs are the principles used to teach whereas the TAs are the actual activities planned in the course. The most commonly used TAs at universities are probably lectures, problem solving sessions and project work but they can in principle be anything like excursions, quizzes, etc. A large variety of teaching methods exist, e.g., inductive learning, problem based learning, learning by inquiry etc.

After choosing the TAs and TMs they are mapped against the ILOs to ensure that all ILOs are covered and thereby ensure the basis for student learning.

The TAs and TMs chosen naturally depend on the size of the classes. Classes with a large number of students cannot be taught on an individual basis and thus lectures and problem solving sessions are often used in this situation. Classes with few students offer the opportunity to teach the students individually or in small groups and thereby use many different teaching methods as will be illustrated in the example later in this paper.

C. Assessment

Based on the TAs and the ILOs it is decided how the level of formative and summative assessment [1] should be implemented in the course. Here the ILOs again hold a central role for both the students and the teacher. E.g., if a written examination is prepared one should try to cover all the areas stated in the ILOs and summative grading is typically used. This is in contrast to formative assessment which is better suited for providing the students personal feedback on their learning and generic engineering competences [4].

Finally, part of the assessment is also to decide how to grade the student, i.e., by grades of pass/fail.

IV. Course Planning Example

In section II it was described how the sequence of courses has been modified at DTU to provide courses where the students have the possibility to design an integrated circuit, tape it out and perform measurements on it after fabrication. In this section the planning and execution of the first of the two new courses "Design and Layout of an Integrated Circuit" [3] is described in detail.

A. Course Vision

The main idea behind the course is for the student to go through the flow of block design as shown in Fig. 1 and fabricate their designs on a chip. Besides teaching the students the flow for IC block design it is also the goal to strengthen the generic engineering competences of the students.

B. The Learning objectives

The ILOs, listed in Table I, are formulated to cover the flow for block design as shown in Fig. 1. As part of the flow the students are expected to try all the tools in the EDA software, i.e., using the schematic editor, the simulation environment, the layout editor and the DRC and LVS tool. As something new for the students they are asked to verify their design in all process corners. Due to time limitation in the 3 week course it was decided not to include parasitic extraction as a topic in the course.

The ILOs are formulated using different level of learning

TABLE I. Mapping of the intended learning objects (ILO) and the teaching activities (TA).

	Teaching Activities (TA)				
Intended Learning Objectives (ILO)	Lectures	Computer Work	Coaching & Guidance	Status Meetings	Review Meeting
Synthesis an Operational Amplifier according to a certain specification in a CMOS process	x	x	x	x	x
Use a schematic editor and simulation environment for design and analysis of analog circuitry	x	x	x	x	
Analyze the performance of the design in all process corners		x	x	x	x
Correlate simulated results with calculated value based on a small signal equivalent of the operational amplifier		x	x	x	x
Use a Layout Editor for making layout of analog circuitry	x	x		x	
Identify parts of the design critical to matching and make layout that ensure good matching for these parts	x	x	x	x	x
Use a DRC tool (Design Rule Checking) to ensure design fulfills design rules	x	x		x	
Use a LVS tool (Layout Versus Schematic) to ensure the layout matches the schematic design	x	x		x	
Design a simple padring for the design at schematic level		x	x	x	x
Document the work in a final report			x		

ranging from the lower level (e.g. “use” and “identify”) to higher level learning (e.g. “synthesis” and ”analyse”). The different levels are used to emphasize that IC design requires a significant portion of craftsmanship and also relies on the systematic analysis and creativity used in the design phase. Also, by defining the ILOs at different levels they enable “not so skilled students” to pass the course while still leaving room for the skilled students to excel.

C. Teaching Generic Engineering Competences using the Company model

Besides teaching the student the technical and practical aspects of doing analog IC design, the course is also designed to teach the student generic engineering competence [4]. This includes team work, problem solving, presentation technique etc. The generic engineering competences are the none-technical skills needed in a normal working environment and thus it is obvious to design the course to resemble a project in a company. This is done by welcoming the students to the virtual company “RealIC Inc.” and stating that the teacher is the manager and the students are the employees.

The students are told that a manager in the industry does not always know the answers nor has the time to assist in all aspects of the development tasks and problems the employees will encounter. This helps set the scene for student learning with respect to generic engineering competences. Therefore, it is required that the students take on the responsibility for their own design and learn to work with problem solving and decision making on their own, mainly using the teacher for sparring and coaching when doing so. The TMs and TAs are planned to support this.

As an example of improving the skills to search for relevant information the students are in the beginning of the course told where the IC process information is located. As the IC process has many different options the students are required to read through the documentation to find the relevant information.

D. The Teaching Method and Activities

Based on the idea of running the course as a project in a company it was obvious to base the course on project and problem based learning. The students were handed a one page specification for an operational amplifier and requested to deliver a layout ready for manufacturing 3 weeks later.

The teaching activities are planned to support the ILOs and the development of the generic engineering competences. Six different teaching activities are planned: pre-test, lectures, status meetings, a review meeting, coaching sessions and computer work. In Table I the TAs (except the pre-test) and the ILOs are mapped. The status meetings and review meeting are used in the course as these probably are the most common types of meetings used in the industry.

The pre-test is given to the student in the morning at the first day of the course. The test is formed as a multiple choice quiz with 20 questions that test the pre-requisites of the course. Based on the results of the pre-test the students are grouped in pairs with approximately the same level of skills. Besides from matching the students the pre-test also helps to determine the need for extra lectures to cover weak spots in the students’ background knowledge.

The lectures in the course are basically introductory lessons to various topics. The lectures are aligned with the progress of the students’ work, e.g., an introduction to layout is given at the time where the students are ready to begin layout. All the lectures are short and cover only the most basic aspects of the topic. It is then expected that the students continue learning as they work with the topic.

Two times every week a status meeting is held where all the students are requested to present a very short status on their design and findings, as well as highlight the challenges and tasks they will focus on until the next status meeting. The project manager makes notes on the discussions and identifies action points which are listed and sent out after the meeting. The main purpose of the meeting is to motivate the students to discuss their problems and share experiences and thereby self-assess their work. Therefore, it is important that the teacher intervenes as little as possible to leave room for the students to discuss. As a teacher these meeting are also a valuable help to identify where the students need guidance and to identify topics where extra lectures are needed.

Half way through the course a review meeting is held. In a 20 minutes presentation the students are requested to present the status of their design in detail and the design considerations for the remaining time of the course. After the presentation the other groups are requested to review what has been presented and thereby provide the group under review valuable information before proceeding. Again, the role of the teacher is to do notes and list action points and only at the end of the session share his observations. To facilitate a good review meeting a lecture was given by a manager from an external company on how they do review, but more importantly also to teach what good behavior and practice during a review meeting is.

The goal of the course being the design of an integrated circuit means that the student should have as much time for practical computer work as possible. The EDA tools for IC design are complex and require hand-on exercises to learn. Thus, all lectures, status meetings and the review meeting were kept short and held in the morning, leaving most of the day for design and computer work. The lectures are concentrated in the first 1½ weeks of the course as the time required for computer work intensifies as the course progresses.

The last and perhaps most important teaching activity is the coaching sessions. Each day during the course the teacher meets with each group to discuss their current challenges. To assist the students two techniques were used; coaching and problem solving. The students are introduced to the 4 steps problem solving methodology shown in Fig. 4 (simplified from the 7 step model used by the US Army [9]). The students are requested to work with their problem using the model before addressing the teacher. In this way the students are to present their ideas and views of the problem and possible solutions. The teacher mainly helps making sure that all alternatives are covered and that the solution the students

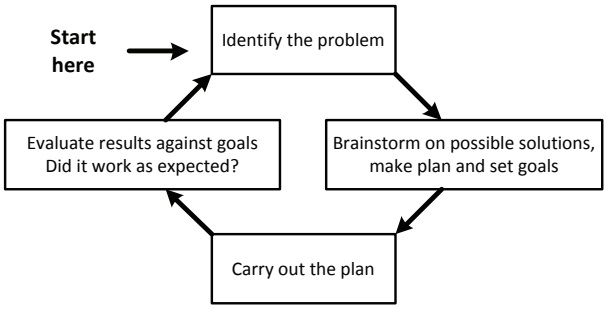

Fig. 4. Problem solving methodology simplified from [9].

choose is based on good argumentation. When using this methodology it is important to support the solution that the students choose rather than focus on them finding the best solution. This increase student learning and not least ensure ownership of their design.

A. Assessment

The main concern in the planning of the course is to create an environment where the student feels safe to participate in all the activities planned in the course, as this was mandatory for a success of the course. Therefore, the students are only assessed on a final written report and graded passed or failed. It is also clearly communicated that the students are not assessed on their performance during the course and that it is a natural part of development to make mistakes as long as one learns from these. The latter being supported by examples from the industry.

Assessing generic engineering competences is not as straightforward as assessing technical skills as these are difficult to measure objectively. This is also the reason for them not being incorporated in the ILOs. To provide the students feedback on the generic engineering competences a 4 step feedback method for formative feedback, very similar to the DESC (Describe – Express – Specify – Consequence) [10], [11], is used:

1. **Describe** the observed behavior/situation to the student
2. **Express** how it makes one feel (the impact is has on me)
3. Communicate the **consequence** of the behavior**.**
4. **Suggest:**
    a. a new behavior (developing feedback, change this)
    b. a continued behavior (positive feedback, more of this)

Note that the feedback method is used for both positive and developing feedback and that it is equally important to provide both kinds of feedback. It goes beyond the scope of this paper to discuss good feedback culture in detail but a feedback should be provided soon after the observation while the situation is fresh in memory. It must be kept in a constructive tone and one must always make sure the student is aware that a feedback is given. A feedback should not last for more than 2-3 minutes.

TABLE II. THE AVERAGE SCORE FROM THE CEQ

Category	**Average (1 -5)**
Good teaching (GT)	4.37
Clear Goals and Standards (CG)	4.07
Appropriate Workload (AW)	3.78
Generic Skills (GS)	4.17
Motivation (M)	4.83
Overall	***4.28***

B. Course Evaluation

At the end of the course the learning of the students was evaluated using the Course Experience Questionnaire (CEQ) [12]. Through 22 questions the students evaluated the course in the five categories listed in Table II, "1" and "5" being the lowest and highest score, respectively. In addition to the questions the students are also asked to state what they find to be good and what could be done to improve the course. The CEQ is based on answers from 6 students who completed the course (2 students dropped out of the course after only one week) and the average scores are shown in Table II.

In general all the scores are very good. The lowest score is the category Appropriate Workload (AW) = 3.78. Looking at the answers to the questions in this category it is clear that the reason for the relatively low score is that many topics were covered and also that it is hard for the student to know when their design is completed. However, some students also suggested that the course could be improved by covering more topics. Also, the very high score in the category Motivation (MS) = 4.83 shows that the students were highly motivated by the course and thus also motivated to learn more even though the workload in the course was already high.

The average score for the Clear Goals and Standards (CG) is 4.07, which is quite high but still the second lowest score. The reason for this relatively low score is most likely related to the coaching approach used in the course where the main idea is not always to provide straight answers. In one case one group of students decided to solve a problem in a certain way which was approved by the teacher. After two days the students realized that the proposed idea did not solve the problem. The students were very frustrated when realizing that the teacher knew that the proposed idea most likely did not work. After a discussion between the students and the teacher the students realized that they probably learned significantly more compared to a situation where the teacher had just suggested a solution. In another situation one group came up with a solution that turned out to be better than the one that the teacher would have proposed, clearly illustrating the strength of the coaching technique and the importance of not providing immediate solutions. Keeping in mind that the main objective of the course is for the students to learn rather than reaching a perfect design clearly justifies using coaching when guiding the students. However, during the first week some students were very frustrated that their questions were not answered directly, but as the course progressed and the students began to develop their circuit their satisfaction

increased drastically as they clearly felt that they made all the decisions.

The students clearly appreciate the teaching method and activities as the Good Teaching (GT) = 4.37 and the generic engineering competence is strongly improved GS = 4.17. Especially, the status meeting turned out a great success. As the teacher was engaged doing the notes the students quickly realized that the discussions had to take place among themselves. The discussion flourished and the students discussed and brainstormed about their problems. For the teacher it turned out that the strongest tool was to keep quiet while letting the students finish their discussions. After the discussions ended the teacher provided his view on various topics and occasionally made short (less the 15 minutes) ad-hoc lectures.

The review meeting was also highly appreciated by the students and the informal environment from the status meeting was also present in this meeting. The success of the review meeting would probably have been much lower if not for the status meetings where the open minded culture and positive atmosphere was founded. The students clearly felt the value for themselves in both the status and review meeting.

By creating an informal atmosphere in both the status meetings and the review meeting the students self-assessed their work providing both criticism and recognition of their respective designs. Finally, it was a general comment from most of the students that running the course using the company model was very inspiring to them.

C. *Future Improvements*

From the comments from the students a few topics were highlighted for future improvement to the course.

More lectures given by external lecturers are requested. In general the students appreciate all sort of information about being an engineer in the industry.

Even though the students in the CEQ rate the workload as above average for the course, many students requested that more topics like parasitic extraction, Monte Carlo and noise simulations are covered in the course. These topics could be covered in the course by letting each group get an individual topic, learn it and then teach it to the other students. An alternative is to incorporate these topics in the second new course where the students are to perform measurements on their devices and correlate these with simulations.

In case more students will attend the course in the future the course structure can be maintained by splitting the students up in different project groups. I.e., the students are divided into teams of maximum 10 students each having their own status meeting etc., the only penalty being the extra effort needed by the teacher.

V. CONCLUSIONS

A strategy has been presented for planning the sequence of courses in integrated analog electronics that offers the students the opportunity to design, layout and tape-out a circuit and after fabrication perform measurements on their circuit. It has briefly been described how a course can be designed using constructive alignment based on intended learning objective, teaching activities and assessment. The methodology for designing a course has been illustrated in detail by describing how the first of two new courses is designed. The primary objective of the course is to teach the students the flow that an IC designer must go through when doing analog integrated circuit design. The secondary objective of the course is to strengthen the generic engineering competences of the students. To support these two objectives the course is run like a project in a company with status meetings and a review meeting where the student self-assess their work. The course was evaluated using the Course Evaluation Questionnaire (CEQ) and showed excellent results with an overall average score of 4.28 out of 5. Especially, the teaching activities and the motivation had very high scores indicating that the students appreciate the company setup. Finally, a few suggestions on how to improve the course were discussed.

VI. ACKNOWLEDGEMENT

The authors would like to thank Analog Devices, Delta, Merus Audio, Oticon, GN Resound and Widex for their financial contribution that has enabled the fabrication the circuits made by the students and thereby enabling the new course sequence.

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F

Increasing Generic Engineering Competences Using Coaching and Personal Feedback

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INCREASING GENERIC ENGINEERING COMPETENCES USING COACHING AND PERSONAL FEEDBACK

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ABSTRACT

This paper presents the implementation of a new course in analog integrated circuit design at the Technical University of Denmark. The course deals with many of the practical aspects of doing integrated circuit design and is designed using constructive alignment. In the paper, the intended learning objective, teaching activities and the assessment are presented and it is demonstrated how coaching and personal feedback – often used in the industry – is used to improve the generic engineering competences of the students in alignment with CDIO. The course is conducted as if it was a project in a company using a minimum of traditional lectures. The central teaching activities in the course are the status meetings, a review meeting and the time the student use for the actual design task. During these activities the teacher mainly acts as a facilitator for the students using coaching and a four step problem solving methodology. In order to create an environment for the students to practice their generic engineering competences they are throughout the course provided personal feedback by the teacher using a four step feedback model. The course was evaluated using the Course Evaluation Questionnaire (CEQ) and the overall score was 4.3 out of 5.

KEYWORDS

Course planning, personal feedback, problem solving, generic engineering competences, Standards: 2, 4, 5, 6, 7, 8 and 11

INTRODUCTION

Teaching the students the technical skills of engineering has for many years been the main focus at technical universities at the expense of teaching the student more generic engineering skills. This problem has increased over the last 1-2 decades as the need for deeper technical insight has increased in a world of rapid development. As a response to this the CDIO concept of teaching has been developed where focus on improving the generic engineering competences of the students is incorporated in the teaching without compromising the technical skills of the students. None-technical learning outcomes (CDIO, standard 2) like inter-personal and human behavior is however not as easy to asses as the technical skills since these often rely on a subjective evaluation by the teacher. Also, these skills are difficult to evaluate in a time limited examination and are best observed and evaluated throughout the course.

In this paper the development, using constructive alignment (Biggs et al, 2011), (Biggs, 2003), of a new master level course at the DTU is described. The course teaches a curriculum not previously taught at DTU and is designed to improve both the technical and generic skills of the students and it is discussed how the environment for learning is created and how the students are assessed. In this new course the students are to design a circuit in an integrated circuit (IC) for a given specification. The course is conducted as a project in a company and has a large focus on the development of the engineering competences of the

students. In order for the students to train their generic engineering competences (Crawley et al., 2007) throughout the course it is mandatory for the students to participate actively. Two major conditions made this possible in the course. First, an environment was created where the students felt safe to participate and not at least safe to make mistakes. This was done by only assessing the students by a final written report and clearly communicating that it is a natural part of engineering development make fails as long as the students can show that they learn from these errors and mistakes. Second, the students are not formally assessed on the generic engineering competence but throughout the course they are provided personal feedback by the teacher on these using a 4-step feedback model. In the paper these two conditions and the motivation behind them are discussed in detail. In the course special attention is given to enhance the problem solving skills of the students as this is an essential skill in basically all engineering work. For this a 4-step problem solving methodology is introduced to the students and teacher use this methodology to coach the student during the design phase. The course setup, the coaching and the personal feedback (explained in detail later) ensures that CDIO standards 4, 6, 7, and 8 are incorporated in the course.

In the following section a brief introduction to course planning using constructive alignment is given. After this the design of the new course is discussed in detail and it is described which of the CDIO standards that are incorporated in the course. Next, the results of the course evaluation using the Course Experience Questionnaire (CEQ) is presented and it is discussed how the course and the teaching activities support improving the engineering competences of the students.

DEVELOPMENT OF COURSES USING CONSTRUCTIVE ALIGNMENT

Over the last decade there has been an increasing focus on higher learning at universities and a large amount of research has gone into learning how students learn (Biggs et al., 2011) and (Biggs, 2003). To design a course many approaches exist and here constructive alignment (Biggs et al. 2011 and Biggs 2003) is used. Constructive alignment uses three elements in the course planning (intended learning objectives, teaching activities and assessment) with the primary focus to increase student learning and competences as illustrated in Figure 1. In the following the three elements in the course planning is described as a sequential process but in practice it is an iterative process where the three elements are revisited until they are aligned. Also, the three elements should be revised after the final course evaluation to ensure that the student learning and intended learning objectives (ILOs) are aligned.

The Intended Learning Objectives

The first step in planning the course is to identify the intended learning objectives (ILO) in

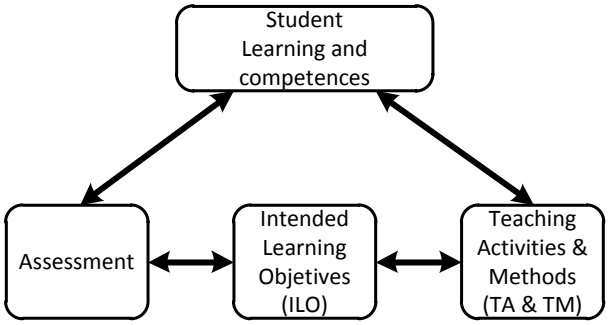

Figure 1. A model for constructive alignment (Biggs et al., 2011).

alignment with CDIO standard 2 and Biggs (2003). The ILOs are short statements of what a student will be able to do if they are met, i.e., what one would like the students to learn. For the teacher the ILOs serve two purposes. First, the ILOs greatly help to plan the course and the teaching activities (TA) as they serve as the goal for the teaching. Second, at the end of the course they are also very useful when designing an examination and finally when assessing the students. When formulating the ILOs it is important to ensure that they address both lower and higher level learning, e.g., according to the SOLO (Biggs et al 2011) or Bloom's taxonomy (Biggs et al., 2011), (Biggs, 2003) and (Felder et al., 2004). The students also have great use of the ILOs, e.g., in case a written report is the basis for the assessment then the ILOs show the student the topics to cover in the report.

The Teaching Activities and Teaching Methods

Once the ILOs are made the teaching activities are planned and along with these the teaching methods (TM) are chosen. The TMs are the principles used to teach whereas the TAs are the actual activities planned in the course. The most commonly used TA at universities are lectures, problem solving sessions and project work but they can in principle be anything like excursions, quizzes, etc. A large variety of teaching methods exist, e.g., inductive learning, problem based learning, learning by inquiry etc.

After choosing the TAs and TMs they are mapped against the ILOs to ensure that all ILOs are covered and thereby ensure the basis for student learning.

The TAs and TMs chosen naturally depend on the size of the classes. Classes with a large number of students cannot be taught on an individual basis and thus lectures and problem solving sessions are often used in this situation. Classes with few students offer the opportunity to teach the students individually or in small groups and thereby use many different teaching methods as will be illustrated in the example later in this paper.

Assessment

Based on the TAs and the ILOs it is decided how the level of formative and summative assessment (Biggs et al., 2011), (CDIO standard 11) should be implemented in the course. Here the ILOs again hold a central role for both the students and the teacher. E.g., if a written examination is prepared one should try to cover all the areas stated in the ILOs and summative grading is typically used. This is in contrast to formative assessment which is better suited for providing the students personal feedback on their learning and generic engineering competences (Crawley et al., 2007). Finally, part of the assessment is also to decide how to grade the student, i.e., by grades of pass/fail.

A NEW EXPERIMENTAL COURSE IN ANALOG INTEGRATED CIRCUIT DESIGN

At universities the fundamental theory of analog integrated circuit (IC) design is often taught in traditional lecture courses but doing analog integrated circuit design has many more aspects to it. The circuit components that one use are very complex and vary a lot from IC to IC and also a lot of unwanted parasitic components appear in the physical design. Furthermore, the flow for doing analog integrated circuit design is complex (see Figure 2) and requires the use of a large variety of software tools. Besides having a good fundamental understanding of circuit design a good portion of craftsmanship is therefore needed in order to excel analog integrated circuit design.

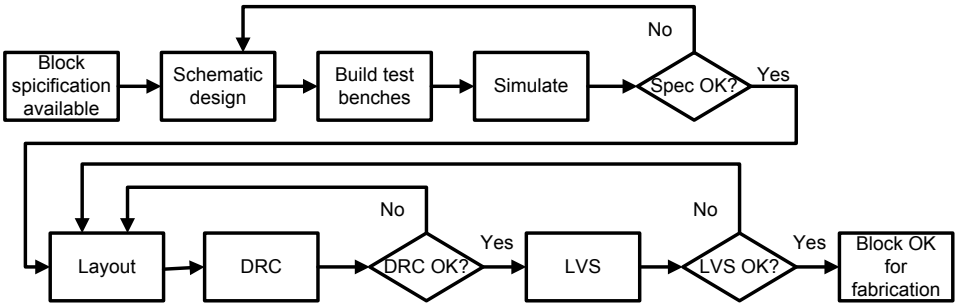

Figure 2. Simplified flow for integrated analog IC design.

At the DTU a new course has been designed that aims to add the practical aspects and craftsmanship of analog integrated circuit design to the portfolio of competences of the students. The curriculum of the course has not previously been taught at DTU. The course (Technical University of Denmark, 2014) is place in the 3-week period where the students are working full time on a single course for 3 weeks. The planning and the evaluation results of the course are described in the following.

Course Vision

The main idea behind the course is for the student to go through the flow of IC block design as described previously and subsequently fabricate their designs on a chip. Besides teaching the students the flow for IC block design, it is also the goal to strengthen the generic engineering competences of the students. To facilitate this, the course is constructed so it emulates a project being conducted in a company where the teacher is the manager and the student the employees.

The Learning objectives

The ILOs, listed in Table 1, are formulated to cover the different elements in the flow for block design as shown in Figure 2. As part of the flow the students are expected to use all the software tools needed in the different parts of the flow, i.e., doing schematic design, using the simulation environment and using the verification tools; design-rule-checking (DRC) and layout-versus-schematic (LVS). As something new for the students they are asked to verify their design in all process corners (the variation in the component parameters).

The ILOs are formulated using different level of learning ranging from the lower level (e.g. “use” and “identify”) to higher level learning (e.g. “synthesize” and ”analyze”). The different levels are used to emphasize that IC design requires a significant portion of craftsmanship and also relies on the systematic analysis and creativity used in the design phase. Also, by defining the ILOs at different levels they enable “not so skilled students” to pass the course while still leaving room for the skilled students to excel.

No ILOs are formulated related to the generic engineering competences of the students. Still, the students are assessed with respect to these by providing personal feedback throughout the duration of the course. The reasoning behind this is discussed later.

Teaching Generic Engineering Competences using the Company model

Besides teaching the student the technical and practical aspects of doing analog IC design, the course is also designed to teach the student generic engineering competence (Crawley et al. 2007), (CDIO standard 4). This includes team work, problem solving, presentation technique, inter personal skills etc. The generic engineering competences are the none-technical skills needed in a normal working environment and thus it is obvious to design the

course to resemble a project in a company. This is done by welcoming the students to the virtual company “RealIC Inc.” and stating that the teacher is the manager and the students are the employees.

The students are told that a manager in the industry does not always know the answers nor has the time to assist in all aspects of the development tasks and problems the employees will encounter. This helps set the scene for student learning with respect to generic engineering competences. Therefore, it is required that the students take on the responsibility for their own design and learn to work with problem solving and decision making on their own, mainly using the teacher for sparring and coaching when doing so. The TMs and TAs are planned to support this.

As an example of improving the skills to search for relevant information the students are in the beginning of the course told where the IC process information is located. As the IC process has many different options the students are required to read through the documentation to find the relevant information.

Table 1. Mapping of the intended learning objectives (ILO) and the teaching activities (TA).

	Teaching Activities (TA)				
Intended Learning Objectives (ILO)	Lectures	Computer Work	Coaching & Guidance	Status Meetings	Review Meeting
Synthesis an Operational Amplifier according to a certain specification in a CMOS process	x	x	x	x	x
Use a schematic editor and simulation environment for design and analysis of analog circuitry	x	x	x	x	
Analyze the performance of the design in all process corners		x	x	x	x
Correlate simulated results with calculated value based on a small signal equivalent of the operational amplifier		x	x	x	x
Use a Layout Editor for making layout of analog circuitry	x	x		x	
Identify parts of the design critical to matching and make layout that ensure good matching for these parts	x	x	x	x	x
Use a DRC tool (Design Rule Checking) to ensure design fulfills design rules	x	x		x	
Use a LVS tool (Layout Versus Schematic) to ensure the layout matches the schematic design	x	x		x	
Design a simple padring for the design at schematic level		x	x	x	x
Document the work in a final report			x		

The Teaching Method and Activities

Based on the idea of running the course as a project in a company it was obvious to base the course on project and problem based learning. This is in alignment with CDIO standards 4, 6, 7 and 8 as described below. The students were handed a one page specification for an operational amplifier and requested to deliver a layout ready for manufacturing 3 weeks later.

The teaching activities are planned to support the ILOs and the development of the generic engineering competences. Six different teaching activities are planned: pre-test, lectures, status meetings, a review meeting, coaching sessions and computer work. In Table 1 the TAs (except the pre-test) and the ILOs are mapped. The status meetings and review meeting are used in the course as these are probably the most common types of meetings used in the industry.

The pre-test is given to the student in the morning at the first day of the course. The test is formed as a multiple choice quiz with 20 questions that test the pre-requisites of the course. Based on the results of the pre-test the students are grouped in pairs with approximately the same level of skills. Besides from matching the students the pre-test also helps to determine the need for extra lectures to cover weak spots in the students' background knowledge.

The lectures in the course are basically introductory lessons to various topics. The lectures are aligned with the work progress of the students, e.g., an introduction to layout is given at the time where the students are ready to begin layout. All the lectures are short and cover only the most basic aspects of the topic. It is then expected that the students continue learning as they work with the topic.

Two times every week a status meeting is held where all the students are requested to present a very short status on their design and findings, as well as highlight the challenges and tasks they will focus on until the next status meeting. The project manager makes notes on the discussions and identifies action points which are listed and sent out after the meeting. The main purpose of the meeting is to motivate the students to discuss their problems and share experiences and thereby self-assess their work. Therefore, it is important that the teacher intervenes as little as possible to leave room for the students to discuss. As a teacher these meeting are also a valuable help to identify where the students need guidance and to identify topics where extra lectures are needed.

Half way through the course a review meeting is held. In a 20 minutes presentation the students are requested to present the status of their design in detail and the design considerations for the remaining time of the course. After the presentation the other groups are requested to review what has been presented and thereby provide the group under review valuable information before proceeding. Again, the role of the teacher is to do notes and list the action points and only at the end of the session share his observations. To facilitate a good review meeting a lecture was given by a manager from an external company on how to make good reviews, but more importantly also to teach what good behavior and practice during a review meeting is.

The goal of the course being the design of an integrated circuit means that the student should have as much time for practical computer work as possible. The software tools for IC design are complex and require hand-on exercises to learn. Thus, all lectures, status meetings and the review meeting were kept short and held in the morning, leaving most of the day for design and computer work. The lectures are concentrated in the first 1½ weeks of the course as the time required for computer work intensifies as the course progresses.

The last and perhaps most important teaching activity is the coaching sessions. Coaching is a technique where the coacher through open questions and discussions help the person(s) to find solutions and make decisions to his/her or their problems. One of the key aspects of coaching is for the coacher to remain objective and not provide concrete suggestions for solving the problems and thereby ensuring the decision making purely rely on the persons being coached. Each day during the course the teacher meets with each group to discuss their current challenges. To assist the students two techniques were used; coaching and problem solving. The students are introduced to the 4 steps problem solving methodology shown in Figure 3 (simplified from the 7 step model used by the US Army (UNC Charlotte Army ROTC, 2014)). The students are requested to work with their problem using the model before addressing the teacher. In this way the students are to present their ideas and views of the problem and possible solutions. The teacher mainly helps making sure that all

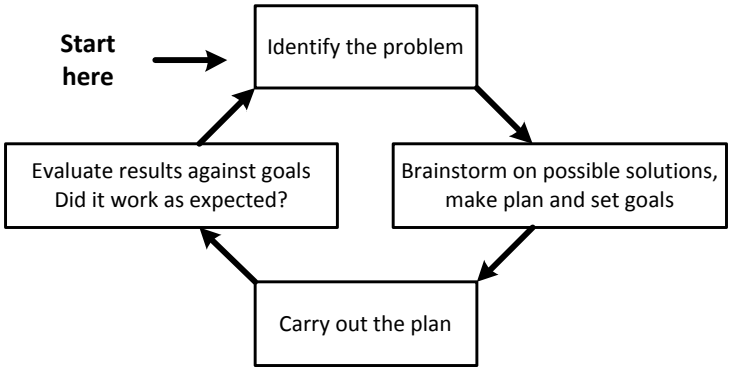

Figure 3. Problem solving method simplified from (UNC Charlotte Army ROTC, 2014).

alternatives are covered and that the solution the students choose is based on good argumentation. When using this methodology it is important to support the solution that the students choose rather than focus on them finding the best solution. This increases student learning and not least ensure ownership of their design. Using coaching and guidance also has a very positive effect on the motivation of the students (Hattie et al., 2007).

Assessment

The main concern in the planning of the course is to create an environment where the student feels safe to participate in all the activities planned in the course, as this was mandatory for a success of the course. Therefore, the students was only assessed on a final written report and graded passed or failed. It is also clearly communicated that the students are not assessed on their performance during the course and that it is a natural part of development to make mistakes as long as one learns from these. The latter being supported by examples from the industry.

Assessing generic engineering competences is not as straightforward as assessing technical skills as these are difficult to measure objectively. This is also the reason for them not being incorporated in the ILOs. To provide the students feedback on the generic engineering competences a 4 step feedback method for formative feedback, very similar to the model Describe – Express – Specify – Consequence or in short DESC (Supervisory Development Lab Course, 2014), (O'Rahily M, 2008), is used:

1. **Describe** the observed behavior/situation to the student
2. **Express** how it makes one feel (the impact is has on me)
3. Communicate the **consequence** of the behavior**.**
4. **Suggest:**
    a. a new behavior (developing feedback, change this)
    b. a continued behavior (positive feedback, more of this)

Note that the feedback method is used for both positive and developing feedback and that it is equally important to provide both kinds of feedback. It goes beyond the scope of this paper to discuss good feedback culture in detail but a feedback should be provided soon after the observation while the situation is fresh in memory. It must be kept in a constructive tone and one must always make sure the student is aware that a feedback is given. A feedback should not last for more than 2-3 minutes.

Course Evaluation

At the end of the course the learning of the students was evaluated using the Course Experience Questionnaire (CEQ) (Hand T. et al., 1999), (Ramsden P., 2003). Through 22 questions the students evaluated the course in the five categories listed in Table 2, "1" and "5" being the lowest and highest score, respectively. In addition to the questions the students are

Table 2. CEQ average scores based on the feedback of the 6 students completing the course

Category	**Average (1 -5)**
Good teaching (GT)	4.37
Clear Goals and Standards (CG)	4.07
Appropriate Workload (AW)	3.78
Generic Skills (GS)	4.17
Motivation (M)	4.83
Overall	***4.28***

also asked to state what they find to be good and what could be done to improve the course. The CEQ is based on answers from 6 students who completed the course and the average scores are shown in Table 2. Two students dropped out of the course after only one week as it turned out that they did not fulfil the pre-requisite for the course and thus did not participate in the course evaluation. The students were organized in groups of two where each group was responsible for a complete design task.

In general all the scores are very good. The lowest score is the category Appropriate Workload (AW) = 3.78. Looking at the answers to the questions in this category it is clear that the reason for the relatively low score is that many topics were covered and also that it is hard for the student to know when their design is completed. However, some students also suggested that the course could be improved by covering more topics. Also, the very high score in the category Motivation (MS) = 4.83 shows that the students were highly motivated by the course and thus also motivated to learn more even though the workload in the course was already high. The average score for the Clear Goals and Standards (CG) is 4.07, which is quite high but still the second lowest score. The reason for this relatively low score is most likely related to the coaching approach used in the course where the main idea is not always to provide straight answers. In one case one group of students decided to solve a problem in a certain way which was approved by the teacher. After two days the students realized that the proposed idea did not solve the problem. The students were very frustrated when realizing that the teacher knew that the proposed idea most likely did not work. After a discussion between the students and the teacher the students realized that they probably learned significantly more compared to a situation where the teacher had just suggested a solution. In another situation one group came up with a solution that turned out to be better than the one that the teacher would have proposed, clearly illustrating the strength of the coaching technique and the importance of not providing immediate solutions. Keeping in mind that the main objective of the course is for the students to learn rather than reaching a perfect design clearly justifies using coaching when guiding the students. However, during the first week some students were very frustrated that their questions were not answered directly. However, as the course progressed and the students began to develop their circuit their satisfaction increased drastically as they clearly felt that they made all the decisions.

The students clearly appreciate the teaching method and activities as the Good Teaching (GT) = 4.37 and the generic engineering competence is strongly improved GS = 4.17. Especially, the status meeting turned out a great success. As the teacher was engaged doing the notes the students quickly realized that the discussions had to take place among them. The discussion flourished and the students discussed and brainstormed about their problems. For the teacher it turned out that the strongest tool was to keep quiet while letting the students finish their discussions. After the discussions ended the teacher provided his view on various topics and occasionally made short (less than 15 minutes) ad-hoc lectures.

The review meeting was also highly appreciated by the students and the informal environment from the status meeting was also present in this meeting. The success of the review meeting would probably have been much lower if not for the status meetings where the open minded culture and positive atmosphere was founded. The students clearly felt the value for themselves in both the status and review meeting.

By creating an informal atmosphere in both the status meetings and the review meeting the students self-assessed their work providing both criticism and recognition of their respective designs. Finally, it was a general comment from most of the students that running the course using the company model was very inspiring to them. As this course is based on an entirely new curriculum it is not possible to compare the evaluation of this course against previous versions of the course.

Future Improvements

Based on the comments from the students a few topics were highlighted for future improvement to the course. More lectures given by external lecturers are requested. In general the students appreciate all sort of information about being an engineer in the industry.

Even though the students in the CEQ rate the workload as above average for the course, many students requested that more topics like parasitic extraction, Monte Carlo and noise simulations are covered in the course. These topics could be covered in the course by letting each group get an individual topic, learn it and then teach it to the other students. In case more students will attend the course in the future the course structure can be maintained by splitting the students up in different project groups. I.e., the students are divided into teams of maximum 10 students each having their own status meeting etc., the only penalty being the extra effort needed by the teacher.

CONCLUSION

Based on constructive alignment the design of a new course in integrated analog electronics that offers the students the opportunity to design, fabricate circuit and subsequently perform measurements on their circuit has been presented. The primary objective of the course is to teach the students the flow that an IC designer must go through when doing analog integrated circuit design. The secondary objective of the course is to strengthen the generic engineering competences of the students. To support these two objectives the course is conducted like a project in a company with status meetings and a review meeting where the students self-assess their work. In the paper it is argued that the foundation for improving the generic engineering competences of the students is to create a safe environment. The students are not assessed with respect to the generic engineering competences but are assisted using coaching technique and provided personal feedback throughout the course. The course was evaluated using the Course Evaluation Questionnaire (CEQ) and showed excellent results with an overall average score of 4.3 out of 5. The students score the category “generic skills” to 4.2 out of 5 clearly showing that the course setup supports the learning of generic engineering competences. Finally, a few suggestions on how to improve the course were discussed.

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Investigation of an AGC for Audio Applications

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Investigation of an AGC for Audio Applications

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***Abstract*—An investigation of an amplifier with discrete time Automatic Gain Control (AGC) which is intended for implementation in hearing aid is performed. The aim of this investigation is to find the AGC's minimum gain step size for which the glitches become inaudible. Such AGCs produce undesirable glitches at the output turning into audible sound effects. In order to find this minimum gain step size both objective and subjective evaluation methods have been used. The investigations show that the objective measures indicate a lower limit for the step size where the sound artefacts are no longer audible. This is in contrast with the subjective method where several test persons can hear the sound artefacts for all step sizes. Thus, the investigated AGC is not suitable for IC implementation therefore an alternative AGC system is proposed.**

Keywords— Hearing aid, Microphone Channel, Automatic Gain Control, PEAQ, Objective evaluation, Subjective evaluation

I. INTRODUCTION

Since using a hearing aid is associated with being old and senile, the persons wearing them have the tendency to hide them. Therefore the need for designing hearing aids which are so small that they are partially invisible is paramount. Small hearing aids restrict the designer in terms of power consumption and in the majority of the smallest hearing aids power consumption is limited to 1 mW. In addition to the power limitation, the required dynamic range is also very high (more than 100dB). In order to increase the dynamic range one can increase the supply voltage but the supply is limited to the voltage of a single zinc-air battery which is approximately 1.0-1.2V. Therefore making a microphone amplifier and a ADC (called a Microphone Channel) with a Signal to Noise Ratio (SNR) of more than 100dB will be too power hungry. Thus an AGC can be used in hearing aid to increase the DR and hence designing the circuitry for more moderate SNR[1]. A microphone channel for hearing aid applications is shown in Fig. 1.a. When the signal at the output of a variable gain amplifier (VGA) exceeds a certain level the AGC reduces the gain to avoid clipping. Simultaneously the digital gain will be increased by the same level to keep the total gain of the channel constant and will do vice versa when the signal level is reduced to a specific level to prevent the degradation of the SNR. Effectively the AGC increases the DR (Dynamic Range) by the amount, the gain can be adjusted in the AGC. However it introduces glitches into the system as a result of its gain switching. These glitches sound like clicks and are undesirable. The generation of a glitch is illustrated in Fig. 1.b.

Therefore the AGC should be designed in such a way that these glitches be so small that are not audible. One way of doing this is reducing the AGC's gain step size while increasing the number of the gain switching occurrences. On the other hand, decreasing the gain step size increases the AGC

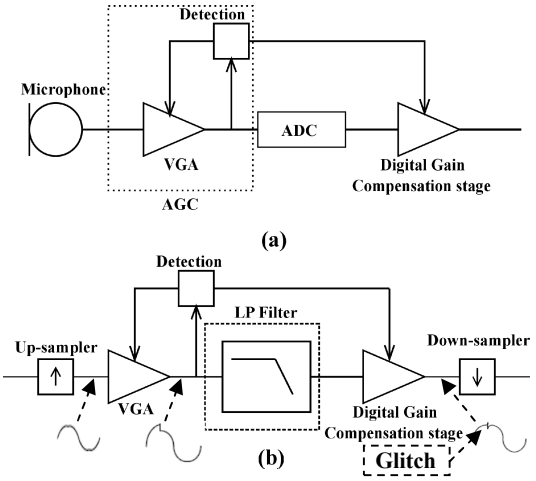

Fig. 1. (a) Hearing Aid Microphone Channel. (b) Model of the channel.

complexity in the sense of analog electronics design. Therefore it is needed to investigate that what is the minimum gain step size for which the glitch is not audible anymore and at the same time minimizing the complexity of the VGA. To do this an audio quality evaluation of the microphone channel output is required to find this minimum gain step size.

The modeled version of the microphone channel is shown in Fig 1.b. The model is implemented in MATLAB, it includes an up-sampling stage, an AGC (Automatic Gain Control) which acts as the mentioned gain control system for increasing the dynamic range of the system, a third order Butterworth low pass filter with the cut-off frequency of 30 kHz which is emulating the transfer function of the ADC, a digital gain compensation stage and finally a down-sampling stage, it should be mentioned that in this model and investigation, the circuit noise is not considered.

For evaluation of the sound quality two methods are available. One is the subjective method which is performed by running an alternative forced choice listening test [7] and the other solution is using an objective method. The subjective method is time consuming in comparison with the objective one, however it is more precise. The objective method which is used, is PEAQ (Perceptual Evaluation of Audio Quality) [10]. This method estimates the audio quality of the signal by incorporating the human auditory system properties. For our specific application (evaluation of the glitches audibility) the two recommended MOVs (Model Output Variables) of PEAQ [5,6] that are ADB (Average Distorted Block) which returns the logarithm of the ratio of the total distortion to the total number of severely distorted frames and MFPD (Maximum Filtered Probability of Detection) which measures the maximum of the probability of detection after low pass filtering, are utilized. These two objective metrics are used to

assess the transient error level of the signals. It is also important that the reliability of these metrics in defining the AGC's minimum gain step size for which the glitches cannot be audible anymore, be investigated. [2,3,4]

II. AUTOMATIC GAIN CONTROL

Three principal parameters are considered to be the foundation for an AGC implementation, these parameters which control the behavior (function) of an AGC are attack time, release time and the gain step size. Different combinations of them can produce glitches with different patterns and audibility level. The attack time is the time that we control between two attack events and the release time is the time that we control between two release events. Three different zones are defined for the AGC which are called attack zone, release zone and dead zone, shown in Fig. 2. The AGC's attack zone is set to be above 0.8 (relative to the supply voltage) and below -0.8. If the output of the VGA is within the attack zone the gain is reduced by one gain step for an attack time. The AGC's release zone is set to be between 0.6 to -0.6 and the zone between the attack and release zones is called dead zone which basically no attack or release happens in this zone. AGC makes decision based on in which zone, the detected output of the VGA (Variable Gain Amplifier) is lying and then it attacks or releases or does neither.

The AGC can be designed with different gain step sizes, reducing this gain step size makes the RMS error value of a glitch smaller, therefore the glitch becomes less audible. The RMS error value is obtained by subtracting the microphone channel output (Fig. 1.b) from the filtered value of the input (passed through the same filter as mentioned for the microphone channel) and taking RMS from it as it is shown in Fig. 3. The reason for filtering the input and then subtracting it, is to compensate the phase shift which is applied to the signal passing through the microphone channel. It is critical that the AGC's attack and release time effect on the audibility of the glitches be eliminated so that the RMS error value becomes only step dependent and only the effect of the step size choice on the audibility of the glitch is being investigated. Thus a total attack and total release time have been considered for the system which will be the same for all the step sizes. (1)-(3) show the logic for predefining the attack and release time. Based on (1)-(3), the smaller the step size, the faster the AGC attacks and releases per step, and the smaller the RMS error value for the resulted glitch (and less audible) will be.

$$Number\ of\ steps = \frac{Depth\ of\ AGC}{Gain\ Step\ Size} \tag{1}$$

$$T_{At,step} = \frac{T_{At,total}}{Number\ of\ steps} \tag{2}$$

$$T_{Re,step} = \frac{T_{Re,total}}{Number\ of\ steps} \tag{3}$$

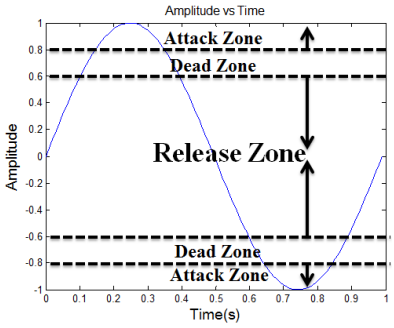

Fig. 2. Defining the AGC's Attack, Release and Dead zones.

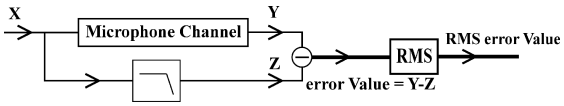

Fig. 3. RMS error value calculation.

In (1)-(3), $T_{At,total}$ is the total attack time, $T_{At,step}$ is the attack time per step, $T_{Re,total}$ is the total release time, $T_{Re,step}$ is the release time per step .

As a result of the above predefinitions of the attack time and release time, the total RMS error value will be almost the same for all the step sizes as will be proved further on. By assuming the RMS error value for 1dB step size to be $e_{rms,1}$ and assuming that N_1 is the number of the occurrences for the 1dB glitches, the total RMS error value will be:

$$e_{total\ rms\ error,1} = e_{rms,1} * \sqrt{N_1} \tag{4}$$

Now if the step size is reduced by a factor of K, each RMS error value of a glitch with the gain step size of K must be approximately:

$$e_{rms,K} = \frac{e_{rms,1}}{K} \tag{5}$$

However as $T_{At,step}$ and $T_{Re,step}$ is also reduced by a factor of K, the number of the occurrences must be increased approximately by a factor of K. Thus the total RMS error value for K is:

$$e_{total\ rms\ error,K} = \frac{e_{rms,1}}{K} * \left(\sqrt{N_1} * K\right) = e_{rms,1} * \sqrt{N_1} \tag{6}$$

This simplified analysis shows that there is no obvious choice for the step size, as the total RMS error value regardless of the step size is almost the same. Hence the need for investigation for finding the minimum gain step size arises which is fulfilled with audio quality evaluation methods.

Clearly using large gain steps in the AGC will result in large glitches and thereby a system of no practical use as the glitches will be very audible. On the other hand using very small gain steps introduces another problem. Consider a low frequency sinusoidal input. The main idea of the AGC system is to adjust the gain in the VGA such that the peak of the signal at the VGA output is located in the dead zone and thus the AGC enters a steady state. However, as the gain steps are very small the release time per step will also be very small and thus the AGC will increase the gain as the signal passes through the release zone. If this increase in the gain is sufficiently large the AGC then have to decrease the gain

again as the signal enters the attack zone. As the step size and thereby the release time is reduced this phenomenon occurs at higher and higher frequencies for the input signal. Again no obvious choice on the gain step size appears.

III. Evaluation Of The Audio Quality

A. Production of the test signals

The test signals for both subjective and objective methods were generated by modeling the microphone channel using MATLAB (Fig. 1.b). A Tuba music sample from the EBU Sound Quality Assessment Material CD [9], which lasts for 2.5s was chosen as the input of the channel (as it was reported to be the worst case scenario with regards to the level of the transient errors (glitches) based on [6]). For generating the sound files, initially each input signal was up-sampled by a factor of 8 from 44.1 kHz into 352.8 kHz to avoid the aliasing of the harmonic distortion which is the result of the AGC activity. At the end, the produced samples were down-sampled to 44.1 kHz and saved as WAVE files. The depth of the AGC was chosen to be -18dB. The test signals were generated by different AGC's gain step sizes ranging from 0.01dB to 1dB. They were generated with a variety of 100 different step sizes in this range. The reason that 0.01 dB was chosen as the smallest step size in these tests is that by reducing the steps size further the complexity of the circuit increases which makes it very difficult to be implemented in analog electronics. In total two groups of test signals were produced based on two different combinations of total attack time and total release time. One group was generated by choosing a shorter total attack and total release time (total attack time of 1ms and total release time of 100ms) and the other group by choosing a longer total attack and total release time (total Attack time of 4ms and total Release time of 400ms).

B. Objective Method

As the subjective method is time consuming, for finding the AGC's minimum gain step size for which the glitch is not audible anymore, an objective method can be used. However the selected objective method should prove itself as a reliable tool for the specific application. ADB and MFDB from the PEAQ's MOVs were used to define the minimum gain step size. The test signals for both test 1 and test 2 were fed into the PEAQ algorithm[8]. The results shown in Fig. 4 and Fig. 5 were obtained for ADB and MFPD, as it can be seen, ADB and MFPD metrics showed that for test 1, for a step size of 0.01dB , both metrics are zero (although for MFPD, it is very close to zero and negligible) and for test 2, for step sizes lower than 0.37dB, the values of ADB and MFPD will be zero, which means that based on these metrics by choosing these thresholds with the mentioned $T_{\mathrm{At,total}}$ and $T_{\mathrm{Re,total}}$, one can make sure that the glitches become inaudible or in the worst scenario, the chance of the glitch detection will be intensively minimized (almost no glitch is audible). Consequently for assuring of the accuracy of these metrics, listening tests as the subjective method were executed.

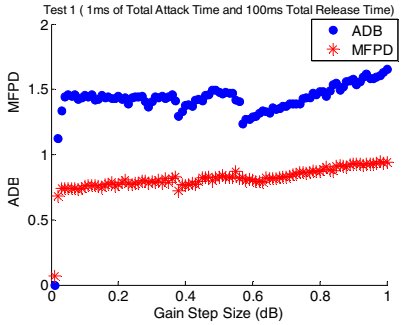

Fig. 4. ADB and MFPD MOVs for Test1's test signals.

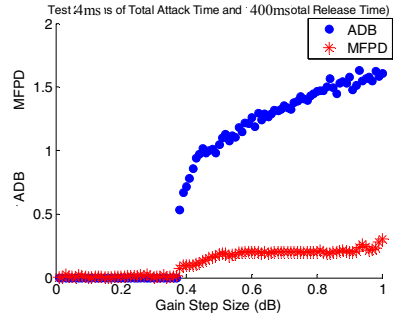

Fig. 5. ADB and MFPD MOVs for Test2's test signals.

C. Subjective Method

For investigating the reliability of the objective method in defining the gain step size, we tried to verify these results with a subjective one. Thus a listening test was executed at the Technical University of Denmark (DTU) double-wall sound-attenuating listening booth. The test was carried out with the total number of 15 participants in the age range of 25 to 35 years old. All the subjects were interviewed to assure that they are having normal hearing ability. The whole test procedure was approved by the Science-Ethics Committee for the Capital region of Denmark (reference H-3-2013-004).

The listening test was implemented based on three intervals, three alternative forced choice (3I3AFC) with 1-up 1-down method (which determines the fifty percent detection probability) [7] . The listening test consists of trials, each trial includes three windows, and windows are separated by a short pause. In each trial two of the windows play the reference signal (Tuba music without any error (glitch)), and the one remained is the one which contains the error for that specific step size, the order of the windows is set randomly. If the subject recognizes the window containing the erroneous signal in a trial correctly then the test will be run again with the same step size. If the second response will be correct as well, the step size will be decreased. However if the answer is wrong then the step size will be increased. The test starts from 1 dB step size, initially the attenuation starts with big jumps (step difference between the two consecutive steps) for finding the subject's threshold faster which the next following steps will be 0.5 dB, 0.1 dB, 0.05 dB and finally 0.01 dB. The test starts with large step differences, as it goes forward the step size difference will be reduced and at the final part ends into 0.01

dB step difference. The test continues till the minimum step size for which the test subject can no longer hear any glitches be detected, the mechanism is that, after getting into the minimum step difference (0.01dB) the test will continue for seven more trials and then stops. The mean value of these last 7 trials is the subject's detected minimum gain step size. Prior to the test execution, the test subjects were trained to increase the possibility of the correct detection of the errors during the test process (according to ITU standards), each subject carried out the two mentioned tests (test 1 and test 2). Fig. 6 shows the obtained listening test results for both test 1 and test 2. The results show the detected minimum gain step size by each test subject for which the glitch is no longer audible. The circle is representative for test1 and the star is representative for test 2. The mean of the obtained minimum step size detected by the subjects for test 1 is 0.06dB while for test 2 this value is 0.12dB. The minimum step size which is detected in test 2 is pushed up in compare to test 1, the reason is that the total attack and total release time for test 2 is higher than test 1 therefore the quantity of the glitches is lower for test 2 in compare to 1 which makes it more difficult for the test subject to detect the error and shifts the detected minimum gain step size upward. This can indicate that the $T_{\mathrm{At,total}}$ and $T_{\mathrm{Re,total}}$ should be made very large but then the AGC will become so slow that clipping at the output of the VGA will start to occur. However some of the test subjects have been able to reach into the minimum gain step size implemented in both test (0.01dB). In [6] it was claimed that for making the transient errors (glitches) to be inaudible, one can target ADB and MFPD for a specific range, which is mapped to step sizes larger than 0.01 dB step size, the reason for this claim is that in [6] the number of steps has been maintained while the step size has been reduced, although we have followed a different logic, which is reducing the step size while having more steps, therefore our results are different with [6]. Consequently we cannot use ADB and MFPD as the objective measures to make any conclusion as the glitch is audible where the ADB and MFPD are not able to evaluate the audibility.

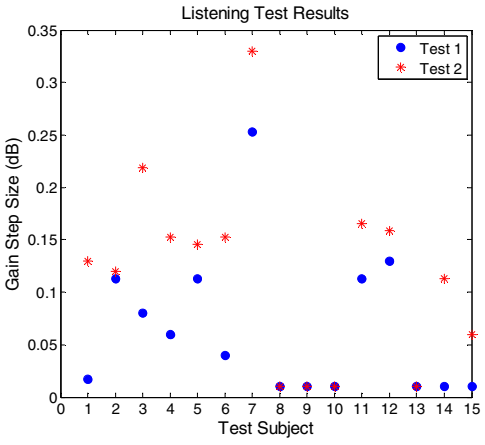

Fig. 6. Listening Test Results (Detected Minimum Gain Step Sizes).

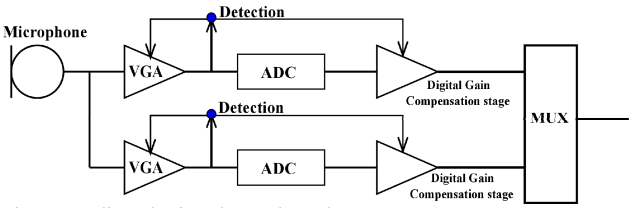

Fig. 7. Duplicated Microphone Channel.

IV. Future Work

The future work will be to implement a system with a duplicated microphone channel (Fig. 7) which avoids glitches by running the two microphone channels in parallel and then only switch between the two channels when the signal in the channel where the gain is changed has completely settled. This will provide a microphone channel without glitches.

V. Conclusion

In this paper an automatic gain control system is investigated to find the gain step size for circuit implementation. The system is evaluated using a MATLAB model for producing output sound. Initially the objective measures Average Distorted Block (ADB) and Maximum Filtered Probability of Detection (MFPD) indicate that a lower limit for the gain step in the AGC exists where the sound artefact are not audible. However, a subjective sound test show that many test subjects can hear the sound artefacts even at gain steps of 0.01dB. Thus, it is not practically possible to implement such an AGC system in circuitry with the sound artefacts being audible. A proposed solution is to implement two AGC channels in parallel using one when the gain in the other one is changed, thereby avoiding the glitches.

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