Very High Frequency Switch-Mode Power Supplies.

Miniaturization of Power Electronics.

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PhD Thesis, May 2015

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Preface and Acknowledgment

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The three years of my PhD studies have been an incredible journey. I have learned a lot, gone through a huge personal development and have numerous great memories to look back at. Through the three years I have engaged with many people, whom have all helped and supported me and without those people I would not be where I am today.

First of all I would like to give my sincerest thank to my girlfriend, Marlene. Your patience, compassion, support and endless love throughout the years, have made it possible for me to work hard and devoted on this project.

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Abstract

The importance of technology and electronics in our daily life is constantly increasing. At the same time portability and energy efficiency are currently some of the hottest topics. This creates a huge need for power converters in a compact form factor and with high efficiency, which can supply these electronic devices.

This calls for new technologies in order to miniaturize the power electronics of today. One way to do this is by increasing the switching frequency dramatically and develop very high frequency switch mode power supplies. If these converters can be designed to operate efficiently, a huge size, weight and cost reduction can be achieved due to the smaller energy storing elements needed at these frequencies. The research presented in this thesis focuses on exactly this.

First various technologies for miniaturization of power supplies are studied, e.g. piezo electric transformers, wide band gap semiconductors and integrated power supplies. Afterwards a wide range of topologies suited for operation at very high frequencies is investigated and the most promising ones are tested experimentally. Through a comparison of these topologies the class DE inverter is found to be superior to the other alternatives, at least for converters with hundreds of volts as input and a few tens of watts output power.

A class DE inverter does however require a high side gate drive, which have never been presented before for these frequencies and voltages. This thesis presents the worlds first high side gate drive capable of operating at these frequencies and voltage levels. With this gate drive the worlds first class DE inverter operating at very high frequencies with more than 100 V input is also developed and presented. These achievements are considered huge breakthroughs in the development of technologies for very high frequency switch mode power supplies.

At these highly elevated frequencies normal bulky magnetics with heavy cores consisting of rare earth materials, can be replaced by air core inductors embedded in the printed circuit board. This is investigated thoroughly and both spirals, solenoids and toroids are considered, both for use as inductors and transformers.

Two control methods are also investigated, namely burst mode control and outphasing. It is shown that a very flat efficiency curve can be achieved with burst mode. A 89.5% efficient converter is implemented and the efficiency only drops 5% at 10% load. This is some of the highest efficiencies presented for converters operating at these frequencies. Burst mode control does however have two major drawbacks,

introductions of low frequency harmonics and decreased control bandwidth. Outphasing is therefore investigated as an alternative, which does not introduce these drawbacks.

In the last chapter the conducted and radiated electromagnetic interference from two prototypes are investigated, one running with constant output and one with burst mode control implemented.

By the end of the thesis it is shown, that a size reduction of 70%, weight reduction of 81%, cost reduction of 56% and efficiency gain of 4.5%-points can be achieved with a very high frequency class DE converter, compared to a commercial product.

Resumé

Vigtigheden af teknologi og elektronik i vores hverdag er konstant stigende. Samtidig er portabilitet og energi effektivitet nogle af de mest populære emner. Det skaber et enormt behov for strømforsyninger i en kompakt form faktor og med høj effektivitet, som kan forsyne disse elektroniske enheder.

Dette kræver nye teknologier for at miniaturisere nutidens strømforsyninger. En made hvorpå dette kan gøres er at øge skifte frekvensen dramatisk og udvikle meget høj frekvente strømforsyninger. Hvis disse strømforsyninger kan designes til at fungere effektivt, kan en enorm størrelse, vægt og kost reduktion opnås på grund af de mindre energi lagrer der skal bruges ved disse frekvenser. Forskningen der er præsenteret i denne afhandling fokuserer netop på dette.

Først bliver en række teknologier til miniaturisering af strømforsyninger studeret, f.eks. piezoelektriske transformere, wide band gap halvledere og integrerede strømforsyninger. Herefter undersøges et bredt udvalg af topologier egnet til at arbejde ved meget høje frekvenser og de mest lovende testes eksperimentielt. Gennem en sammenligning af disse topologier bliver klasse DE vekselretteren fundet bedre end de andre alternativer, i hvert fald til strømforsyninger med hundrede af volt som indgangsspænding og et to cifret antal watt som udgangseffekt.

En klasse DE vekselretter kræver imidlertid en *high side gate driver*, hvilket aldrig før er blevet præsenteret til disse frekvenser og spændinger. Denne afhandling præsenterer verdens første *high side gate driver* i stand til at arbejde ved disse frekvenser og spændings niveauer. Med denne gate driver er verdens første klasse DE vekselretter der arbejder ved meget høje frekvenser med mere end 100 V som indgangsspænding udviklet og præsenteret. Disse bedrifter betragtes som meget store gennembrud i udviklingen af teknologier til meget høj frekvente strømforsyninger.

Ved disse meget hævede frekvenser kan normale klodsede magnetiske komponenter med tunge kerner bestående af sjældne jordarter erstattes af luft spoler indlagt i printpladen. Dette er undersøgt grundigt og både spiraler, solenoider og toroider er betragtet, både til anvendelse som spoler og transformatorer.

To kontrol metoder er også undersøgt, nemlig tænd-sluk kontrol og udfasning. Det er vidst at en meget flad effektivitets kurve kan opnås med tænd-sluk kontrol. En 89,5% effektiv strømforsyning er implementeret og effektiviteten falder kun 5% ved 10% belastning. Det er nogle af de højeste effektiviteter der er er præsenteret for strømforsyninger ved disse frekvenser. Tænd-sluk kontrol har dog to store ulemper,

introduktion af lav frekvente harmoniske og lavere kontrol båndbrede. Udfasning er derfor undersøgt som et alternativ, som ikke introducerer disse ulemper.

I det sidste kapitel er den ledningsbårne og udstrålede elektromagnetiske støj fra to prototyper undersøgt, en der kører med konstant effekt og en med tænd-sluk kontrol implementeret.

I slutningen af afhandlingen vises det, at en størrelses reduktion på 70%, vægt reduktion på 81%, kost reduktion på 56% og effektivitets stigning på 4.5%-point kan opnås med en meget høj frekvent klasse DE strømforsyning, sammenlignet med et kommercielt produkt.

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Chapter 1

Introduction

1.1 Background and Motivation

Electronics has forever changed the way we live and interact with each other. It is the basis for the information age and the importance of electronics in our daily life is constantly increasing. Few people can imagine even a single day without at least a few electronic devices such as artificial lighting, television, radio, kitchen appliances, computers and cell phones.

All of these devices require power conversion and power electronics has hence become one of the key enablers of modern civilization. In most cases power conversion is handled by a switch-mode power supply (SMPS) due to its high efficiency and power density. Traditional hard-switched SMPSs have, however, reached a point where only incremental improvements are achieved.

In order to fulfill the ever-increasing demand for miniaturization and portability, new ways of designing power converters is hence needed. The power converter is also the weakest link in regards to lifespan in many electronic products. A good example is the rapidly increasing market for LED lighting, where more than 50% of the products fail due to the LED driver [1].

Global warming and reduction of the global energy consumption is one of the main focus areas of the 20th century. Hence no new technology can come at the expense of increased energy consumption. High efficiency is therefore a must have for any new power conversion technology.

At the same time the market for power converters is, as most markets, driven by cost. Any new technology with the above-mentioned benefits should, therefore, come at the same price, preferably lower, as the technology of today.

The volume, weight, and cost of SMPSs are mainly governed by passive energy storing elements (inductors and capacitors). The value, size, weight, and price of these scales with the switching frequency and a dramatic increase in switching frequency will hence lead to highly increased power density and reduced cost.

Furthermore, decreased need for energy storage leads air core magnetics to be a feasible alternative to cored magnetics, which utilize rare earth materials that are primarily mined in an environmentally damaging process in China [2]. The reduced need for capacitance eliminates (or significantly reduce) the need for electrolytic capacitors, which are the main cause of failure in power converters [3, 4, 5].

SMPSs with highly increased switching frequencies thereby posses the ability to enable all the above-mentioned benefits. In order to make a real difference, the frequency has to be increased a decade or more. If the switching frequency is increased a decade from 1-2 MHz, which is state-of-art today [6, 7], a switching frequency of 10-20 MHz will be achieved. At these frequencies, the core loss in the core materials available today start to become significant and lead to decreased efficiency [8]. Using air core magnetics is as mentioned a feasible alternative, but less inductance per volume can be achieved without the core. The frequency, therefore, needs to be increased even further, to get the desired size reduction without the magnetic core.

1.2 Objective

The objective of this PhD thesis is to investigate, whether it is possible to increase the switching frequency of power converters into the Very High Frequency range (VHF, 30-300 MHz) [9].

The converters should achieve efficiencies at least on par with commercial products and use standard components in order to keep cost low. The aim is to show that a size and weight reduction of 80% can be achieved without compromising cost, efficiency or reliability.

1.3 Structure and Content

The structure and content of the PhD thesis are visualized in Table 1.1.

The first chapter covers an introduction to the thesis with background and motivation and the scope and objectives of the project. Chapter two covers a state-of-art analysis with special focus on technologies for miniaturization of power converters.

The circuit topologies suitable for use at these frequencies are analyzed in chapter three. Furthermore the option of stacking multiple converters with serial or parallel input and output are analyzed and a new arrangement of the input and output terminals is described.

Chapter four analyses the gate drives suitable for operation at these frequencies and especially centers on a new self-oscillating resonant gate drive. Chapter five covers the design of PCB embedded magnetics based on spirals, solenoids and toroids, both inductors and transformers are analyzed.

The control is covered in chapter six and in chapter seven the electromagnetic interference of the converters are analyzed and measured.

Finally chapter eight summarizes and concludes the thesis. The main results are

summerized and the work to be done in the future is described.

The chapters and sections are linked with the associated peer reviewed conference papers, journal paper and patent applications; these are all located in appendix A. These papers and patents are an integrated part of the thesis and the thesis mainly covers complementary information. This is to present a coherent and complete overview of the research work that has been done throughout the project.

Table 1.1: Structure and content of the thesis.

Chapters	Sections	Appendicies
1 Introduction	Background and motivation	
	Objective	
	Structure and content	
2 Switch Mode Power Supplies	Miniaturization	A.1 "On the Ongoing Evolution of Very High Frequency Power Supplies" A.2 "Evolution of Very High Frequency Power Supplies"
	Summary of trends	
3 Topologies	Single switch	A.3 "Low Power Very High Frequency Resonant Converter with High Step Down Ratio" A.4 "Low Power Very High Frequency Switch-Mode Power Supply with 50 V Input and 5 V Output" A.5 "Very High Frequency Resonant DC/DC Converters for LED Lighting"
	Half bridge	A.6 "Very High Frequency Half Bridge DC/DC Converter"
	Stacking	A.7 "Input-Output Rearrangement of Isolated Converters" A.8 "Step-up dc-dc Power Converter" A.9 "Step-down dc-dc Power Converter"
	Summary	
4 Gate drive	Externally driven	
	Self-oscillating	A.10 "Self-Oscillating Resonant Gate Drive for Resonant Inverters and Rectifiers Composed Solely of Passive Components" A.11 "Self-oscillating Galvanic Isolated Bidirectional Very High Frequency DC-DC Converter" A.12 "Self-oscillating Resonant Power Converter"
5 PCB embedded magnetics	Inductors	A.13 "Printed Circuit Board Embedded Inductors for Very High Frequency Switch-Mode Power Supplies" A.14 "Design Optimization of Printed Circuit Board Embedded Inductors through Genetic Algorithms with verification by COMSOL" A.15 "Investigation of a Hybrid Winding Concept for Toroidal Inductors using 3D Finite Element Modeling" A.16 "Optimizing Inductor Winding Geometry for Lowest DC-Resistance using Live Link between COMSOL and MATLAB"
	Transformers	A.17 "Investigation, development and verification of printed circuit board embedded air-core solenoid transformers" A.18 "Embedded solenoid transformer for power conversion"
6 Control	Burst Mode	
	Outphasing	A.19 "Outphasing Control of Gallium Nitride based Very High Frequency Resonant Converters"
7 Electromagnetic Interference		
8 Conclusion & Future Perspectives	Summary	
	Conclusion	
	Future work	

Chapter 2

Switch-Mode Power Supplies

The first switch-mode power supplies were developed in the early 70's [10] and have since become the market standard, due to amongst other the high power density, high efficiency and lower cost compared to iron core transformers.

The first SMPSs operated at 20 kHz with efficiencies around 75% and power densities of approximately 0.15 W/cm^3 [11]. Since then, the technology has been improved, matured, and components optimized for use specifically in power supplies developed.

This combined with more than 40 years of research and development has moved the technology far. Today efficiencies up to 99.7% [10] and power densities of more than 10 W/cm^3 [12] can be achieved. Through the past decade a doubling in power density have been seen and this is expected to continue for the next decade [13].

These efficiencies and power densities are, however, for kilo and mega watt power converters. The main focus of this thesis is converters with an output power in the range from a few to around hundred watts. At these power levels, the performance that can be achieved is lower, some of the best results published are efficiencies around 95% [14] and power densities of 0.88 W/cm^3 [15].

Figure 2.1: Apples 60 W sugar cube laptop charger.

These results are, however, achieved in a laboratory with a controlled environment and without a strong focus on cost. For commercial products, cost is one of the main concerns and reduced efficiency and power density is accepted in order to keep the cost low.

Apple is known for their sugar cube laptop adaptors, which are some of the smallest on the market, see Figure 2.1. The power density of the 60 watt version is 0.59 W/cm^3 (60 W/(6.4 cm·6.4 cm·2.5 cm), including casing and plug) and the efficiency is 90% [16]. For a USB charger, the efficiency and power density is even worse, with an efficiency of 75% and power density of 0.31 W/cm^3 (5 W/(2.54 cm)^3, including casing and plug) [17]. The same trend can be seen for LED drivers, where a 60 W driver with a power density of 0.15 W/cm^3 (60 W/(18.15 cm·6.2 cm·3.5 cm), including casing and plug) and efficiency of 89% is commercially available [18]. The drop in efficiency and power density is partly due to the fact that casing, plugs, control, start-up, protection and other housekeeping circuitry is needed independent of the power level and partly due to a tradeoff with price. As the power level increases, the efficiency becomes more important and it becomes more acceptable to increase the price slightly, if a higher efficiency can be achieved due to the larger amount of energy that can be saved.

2.1 Miniaturization

As mentioned in Chapter 1, the traditional SMPSs have reached a point where the technology is matured and only incremental improvements are achieved year-on-year.

The market for power supplies is huge ($21.6 billion in 2014 [19]) and the technology still posses some big drawbacks. It has become one of the major bottle necks for further size reduction of modern electronic products. Hence, there are large market forces driving the research and development of new technologies, which can improve or change the way power supplies are made, some of these are described in the following subsections.

2.1.1 Resonant Converters

As stated in Chapter 1, the size of modern SMPSs is mainly governed by the passive energy storing elements. The direct way to reduce the size of these is to increase the frequency. If this is done without paying special attention to the switching losses, the efficiency will be poor and most likely cause overheating and failure of the power semiconductors. With resonant converters, zero voltage switching (ZVS) can be achieved and losses due to parasitic switch capacitance can thereby be avoided [20].

Several types of resonant converters exist, but they can all be split into three groups, series resonant, parallel resonant and series-parallel resonant converters. The series resonant converter has the best efficiency and lowest complexity, but has fundamental challenges with output regulation, especially for light and no-load situations. Parallel resonant converter has better load regulation, but a major

drawback because the resonating currents do not scale with the output power. Hence it will have the full load losses even at light loads, causing very low light load efficiencies [21].

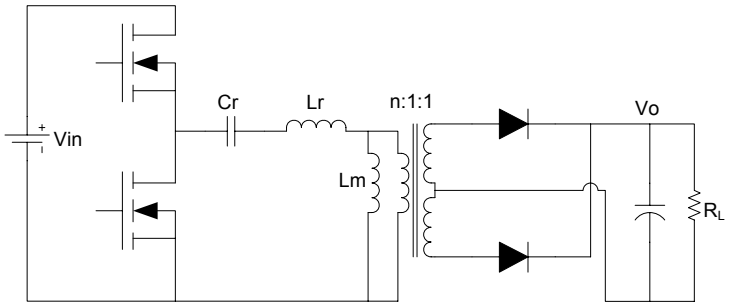


Figure 2.2: Schematic of a serial-parallel resonant LLC converter [22].

Series-parallel resonant converters have both a series resonant and a parallel resonant element. These elements can be balanced to get the advantages of both the series resonant and the parallel resonant topologies while reducing the drawbacks significantly. The LLC converter shown in Figure 2.2 is the most commonly used topology for resonant converters. It can be designed with zero voltage swithcing (ZVS) to reduce switching losses and increase frequency [23]. LLC converters are often used in step down application from several hundreds volts to a few tens of volts and commonly in the power range of 400-4000 W [24].

Several 1 kW LLC converters operating at 1 MHz with efficiencies over 90% have been made [22, 6, 24, 7]. The converter presented in [6] achieves a peak efficiency above 96% and a power density of 5.86 W/cm^3. The one in [7] has a power density of more than 50 W/cm^3 and in [24] a GaN based LLC converter operating at 350 kHz with 98% efficiency is presented.

For the last decade there has been an increasing focus on and research in resonant power converters operating at very high frequencies [25, 26, 27, 28, 29, 30]. Moving into this frequency range dramaticly reduces the need for passive energy storage and cored magnetics and electrolytic capacitors can be replaced by air-core magnetics and ceramic capacitors, hence minimizing size and price while extending the lifespan [31, 32] and A.2. This will be covered more in-depth in the following chapters.

2.1.2 Piezoelectric Transformers

The magnetics, and especially the transformers, are often the largest components in an isolated converter. Hence, reducing the size of the transformer would be a great step towards miniaturization of power electronics. One way to do this is by using a piezoelectric transformer, which utilizes two pieces of ceramic material with a piezoelectric property. When a material with a piezoelectric property is subjected to a mechanical stress it becomes electrically charged. Likewise, an electrical field will cause a deformation of the material. These effects are also known as the direct and converse piezoelectric effect, respectively [33, 34]. In the 1950's C. A. Rosen [35] utilized these properties to create the rosen type piezoelectric transformer, see Figure 2.3.

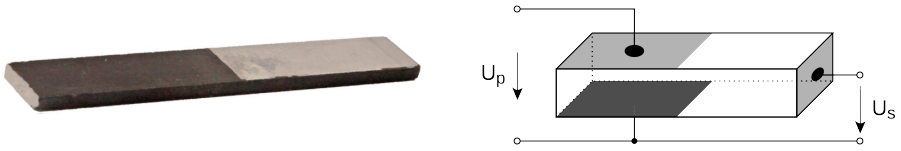


Figure 2.3: Picture and drawing of a rosen type piezoelectric transformer [36].

These transformers are especially suitable for applications where a high step ratio is required [37, 38]. The material exhibits a very high Q factor (>1000 [39]), high efficiencies (>98% [37]) and power density of more than 100 W/cm^3 [33] can be achieved. This is, however, for the transformer alone. For a complete converter, the efficiencies are closer to 80% and the power densities around 0.5 W/cm^3 [40, 41]. The piezo based converters operate around the resonance frequency of the transformer and for most available transformers this frequency is around 50 kHz [38, 34]. This limits the power density that can be achieved, as the converters will still require big input and output filters. Piezo based transformers have, however, been tested at more than 1 MHz [33], but here the efficiency of the transformer alone drops below 90%. Piezo based converters, therefore, seem to be best suited for high step up or down applications, where the limited efficiency and power density can be justified by the big conversion ratio.

2.1.3 Switched Capacitor

Another way to get rid of the bulky magnetics is to use switch capacitor (SC) circuits. These circuits do not rely on energy storage in magnetics, but use a network of switches and capacitors for energy conversion [42, 43]. An example of a switch capacitor circuit is shown in Figure 2.4.

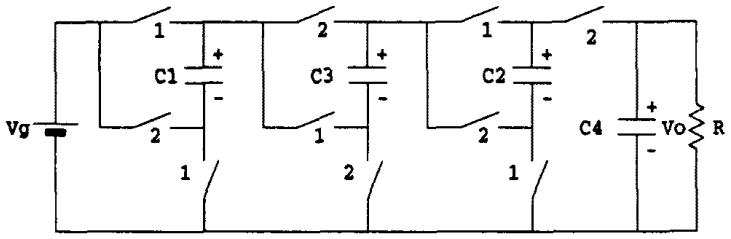


Figure 2.4: Schematic of a switch capacitor circuit with a step-up conversion ratio of 5 [42].

As the energy density of capacitors is over 1000 times higher than that of inductors, it is possible to achieve a large increase in power density with these circuits [44, 45]. Further fully monolithic integration in silicon becomes much easier as switches and capacitors are much easier to integrate than inductors [44, 46, 43]. Efficiencies up to 93% [47] and power densities of several watts per square millimeter [48, 49, 50] has been achieved in fully integrated circuits.

One of the main challenges of this type of circuits is control and especially efficiency when the converter is used to regulate the voltage [46, 43]. These converters are designed to operate with a fixed integer conversion ratio from input to output voltage where transition between parallel and serial connection of a finite number

of capacitors are used to achieve this conversion ratio. When operating at this optimum point the efficiency is ideally 100% [43], however the efficiency quickly rolls of when the point of operation moves away from this optimum. Lately a lot of research has been done within so called gear shifting switch capacitor circuits [46, 51]. These switched capacitor circuits have different modes of operation with different optimum conversion ratios, for instance 2:1 and 3:2. This increases the range in which the circuits can operate efficiently, but increases the complexity.

The number of switches and capacitor increases rapidly with the conversion ratio [42]. With a moderate conversion ratio of 5, 4 capacitors and 10 switches are required, see Figure 2.4. Further all of these switches requires a gate drive and 7 of them even a high side gate drive. This makes the complete circuit quite complex and a lot of components are required. This is not a big challenge in integrated circuits where the components can be scaled according to the application and placed very close to each other. For discrete circuits the size would however quickly increase as soon as the step ratio becomes more than a simple 2:1 or 1:2 converter.

For the above mentioned reasons, switched capacitor circuits are mainly used in fully integrated circuits and mainly with conversion ratios up to 8:1 [44, 43]. The highest power level presented so far is 10 W [51] and the voltage levels are typically from a few volts up to around 12 V [48, 45].

2.1.4 Wide Band Gap Semiconductors

Since the development of the switch mode power supply in the early 70s, one of the main drivers towards miniaturization of power electronics has been increased switching frequencies [13]. The ability to increase the switching frequency while still achieving the same, or even higher efficiencies, can greatly be attributed to the development of better power semiconductors. Silicon based power semiconductors have however reached the fundamental limit of the material properties. For now constant innovation has enabled semiconductor manufactures to push the boundaries, see Figure 2.5, but the pace is slowing down [52].

Lately there has been an increasing focus on so-called wide band gap power semiconductors. These power semiconductors are based on new materials, which require larger energy for an electron to jump from the top of the valence band to the bottom of the conduction band (the band gap) [54]. The band gap and other important parameters of these new materials are summarized in Table 2.1. Some of the materials have a range on some of the properties; this is not due to variations in these parameters, but due to in consistence in the literature. The references [55, 56, 57, 58] all list some or all of these parameters, but there is a significant variation in the values they list. Most of the values are showing the same trend, but for the break down field the literature is not consistent in which of the materials GaN and 4H-SiC that has the largest value ([56] states SiC > GaN whereas [57, 58] states GaN > SiC).

The literature is however consistent in stating that these materials are superior to silicon in terms of higher operating temperatures, higher power densities, higher voltages and higher frequencies [61, 62, 54]. Several different figures of merits (FOM) have been made in order to compare the different materials. The JFOM derived by Johnson in 1965 [59] and the BFOM derived by Baliga in 1982 [60] is

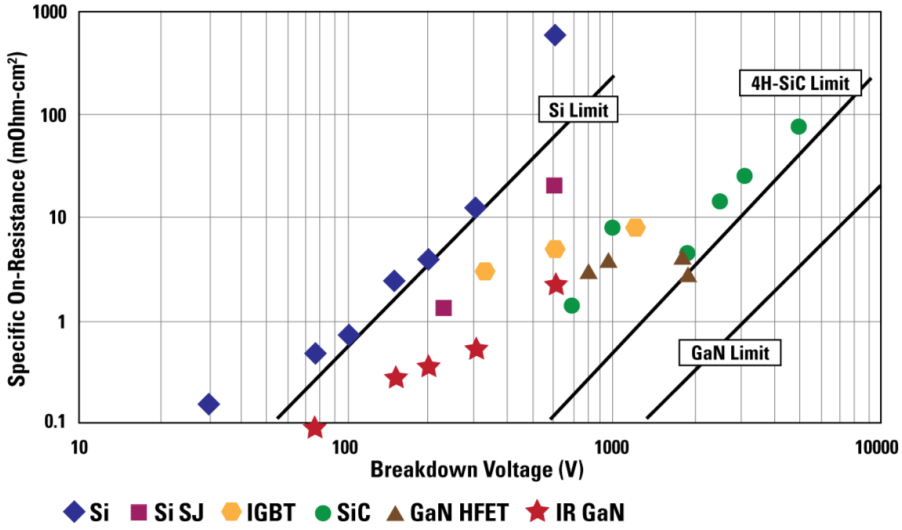


Figure 2.5: Bounderies of semiconductor materials and switch technologies [53].

Table 2.1: Material proporties related to performance in power electronics.

	Si	GaAs	4H-SiC	GaN	Diamond
Bandgap E_g (eV)	1.12	1.42	3.26	3.39	5.45
Dielectric constant ϵ (cm^{-3})	11.8-11.9	12.5-13.1	10	9.0-9.5	5.5
Mobility μ_n ($cm^2/V\ s$)	1300-1350	5000-8500	260-720	900-2000	1900
Saturation velocity v_{sat} (MV/cm)	1.0	1.0-2.0	2.0	2.5	2.7
Break down field E_{br} (MV/cm)	0.3	0.4	2.0-3.5	2-3.3	5.6
Thermal conducti. λ (W/cm K)	1.5	0.5	4.5	1.3	20
Johnson FOM [59] $E_{br} \cdot v_{sat}/2\pi$	1	2.7	20	27.5	50
Baliga FOM [60] $\epsilon \cdot \mu_n \cdot E_g^3$	1	9.6-17	3.1	24.6-134	5.45

the most widely adopted FOMs, for both high values are good. JFOM is based on the power-frequency product for low voltage transistors and BFOM is based on the conduction losses in power FETs [63]. The two FOMs are defined as:

$$JFOM = E_{br} \cdot v_{sat}/2\pi \tag{2.1}$$

$$BFOM = \epsilon \cdot \mu_n \cdot E_g^3 \tag{2.2}$$

GaAs Gallium Arsenide is without comparison the compound with the highest mobility. This makes it excellent for circuits were very fast switching speed is the main parameter. For this reason it is widely adopted in communication circuitry for cellphones, radars, satellites and other microwave applications. However the low break down field makes it unsuited for applications were more than a few volts are required.

4H-SiC Silicon Carbide is, contrary to GaAs, very well suited for high voltage applications. The 4H refers to the crystal structure of the material [64]. 4H-SiC has the highest electron mobility and is therefore considered to be the best structure [65]. Due to the high break down field it has been possible to fabricate a MOSFET with a break down voltage of 10 kV, the highest ever [62]. The combination of high break down voltage, the high thermal conductivity and the fact that SiC can operate at up to 350 °C [66] makes it extremely well suited for high power applications. Several implementations have shown the high efficiency and power densities which can be achieved with these new devices, two examples are a converter with an efficiency of 99% and power density of 3.3 W/cm^3 [67] and another with an efficiency of 98% and a power density of 62 W/cm^3 [68].

GaN Gallium Nitride is the least mature of the three wide band gap materials [61], at least for power electronics. The material is widely used for blue LED (which are then turned white by adding a layer of phosphor) [55]. The RF industry is also starting to adopt GaN, as it can be used for higher power and voltage levels than GaAs due to the higher break down field and thermal conductivity. With the high mobility and high break down voltage, GaN is also very well suited for switch-mode power supplies and class D amplifiers. Due to the lower thermal conductivity compared to SiC it is however most suited for power levels up to a few kW. Several examples of GaN based point of load converters are shown in [69], all operating at 1-5 MHz with 1.2 V output and achieve power densities around 60 W/m^3 and efficiencies between 85% and 95%.

The transition from silicon to wide band gap semiconductors will definitely help to move towards miniaturization of power electronics. Great results have already been achieved and the technologies, especially GaN, are just starting to become mature enough to be used in commercial products. Further each of the three materials seems to have found their own market niche, see Figure 2.6, and are starting to get traction.

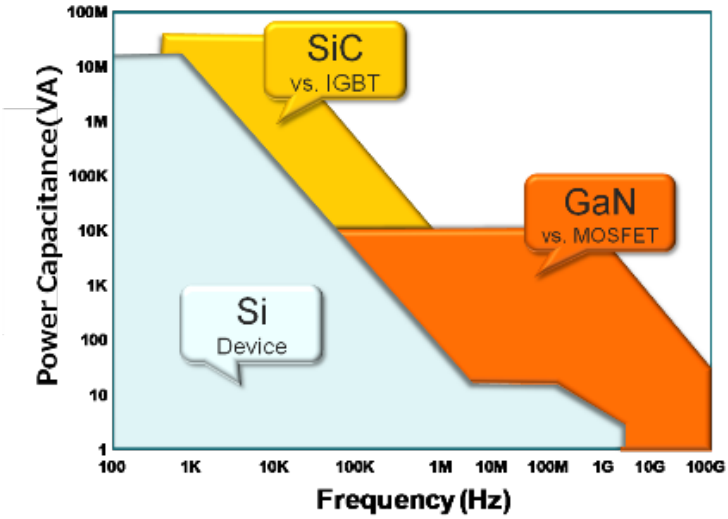
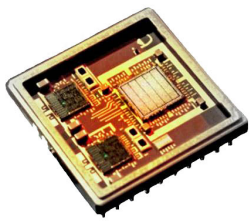


Figure 2.6: Material chioce depending on power level and operation frequency [70].

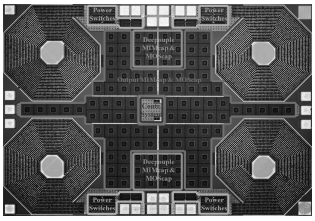
2.1.5 Power Supply in Package and on Chip

The ultimate goal for miniaturization of power electronics is to integrate the entire power supply on a chip (PwrSoC). However taking a 10 kW converter and just going for full integration in one step would be a very big and risky step. Therefore the road from complete discrete solutions to fully integrated converters has been split into different levels of integration. Figure 2.7 illustrates this with the three levels 2.7a Power modules, 2.7b Power Supply in a Package (PSiP) and 2.7c PwrSoC.

(a) Power converter module [71]



(b) Power Supply in Package [72]



(c) Power Supply on Chip [73]

Figure 2.7: Three levels of integration.

Modules Power modules are the first step towards integration. Here the entire converter is tightly packed in a single module. The converter design inside the modules are highly optimized and the interconnections between the components made much more advanced, than what can be done on a standard PCB with discrete components. Further the availability of complete modules with entire power converters ease the design for system engineers, as they can leave the converter design to the module manufactures. Vicor is one of the leading companies in this area, with a wide selection of modules and some of the best specifications. They have just released a new 400 W AC-DC module with PFC, 92 % efficiency and a

power density of more than 7 W/cm^3. The modules are however still to expensive for most applications, with a price point of more than $150 for the Vicor module just mentioned.

PSiP The next step towards full integration is PSiP. Here all the active components are integrated on the same die, but at least one of the passives are still discrete and co-packaged in the same package as the die. Here the advances in packaging and interconnection gained through the modules are taken one step further. The active die and the passives are now packed to a level, where it can be difficult to distinguish a PSiP and a PwrSoC just by looking at the size. The number of PSiP products available have greatly increased through the last years with more than 200 products on the market already in 2012 [74].

A good example of a PSiP is the 480 MHz buck presented in [75]. It has one air core inductor that is not on the chip, but the high switching frequency is only possible due to the tight interconnections between the die and the passives. The converter steps from 1.8 V to 0.9 V with 72% efficiency and the efficiency can be increase to 76% by decreasing the switching frequency to 250 MHz. In [76] a GaN buck with external filter, a switching frequency of 10-200 MHz and an output power of 10 W is presented. This is very close to a PSiP, but due to the fact that the control is not on the same die as the converter, it does not meet the definition of a PSiP [74]. Combinations of wide band gap devices and the tightly packed PSiPs are however expected to bring very interesting products on the market within the near future [77].

PwrSoC The final step towards monolithic integration, is to get the passives on the same die as the active components. It is a great challenge to integrate passives and due to the lack of core materials, the switching frequency should generally be above 50 MHz for PwrSoC to achieve higher power density than PSiP [78]. One solution to this is of course to use the switch capacitor circuits described in section 2.1.3, in this way no inductors are needed and only capacitors need to be integrated. Switch capacitors will however not be covered further in this section, as they have already been described.

The bond wires can be used as inductors as in [79], were a fully integrated 200 MHz converter with a peak efficiency of 89% is presented. This is efficient as bond wires have high Q factor compared to what can be achieved on chip, but it is not a true PwrSoC as the inductors are still of chip. In [73] the inductors are moved a bit closer to the chip by implementing them in the silicon interposer. In this way a converter with a switching frequency of up to 300 MHz, optimum at 200 MHz, and peak efficiency of 75% is designed. The next step toward true monolithic integration is to move the inductor to the bottom layer of a standard flip chip package, this is done in [80] were a 140 MHz 90% efficient converter is presented. Figure 2.7c shows the fully integrated buck converter presented in [73]. Though some of the other examples almost meet the definition of a PwrSoC, this is the only true PwrSoC. It has a switching frequency up to 225 MHz and converts from 2.6 V to 1.2 V with an efficiency of 58%, the die shown handles up to 800 mW.

It is very early days for PwrSoC with just a few experimental results and the

first commercial product presented in the fall 2014 [80]. Constant improvements in packaging and especially thermals are however needed to get more and better PwrSoC product on the market [74]. Finally all the PSiPs and PwrSoCs shown are working at very low voltages, the range of 0.5-3 V.

2.2 Summary of Trends

Several existing and new emerging technologies for miniaturisation of power electronics have been presented in this chapter. To give an overview the technologies and the voltage and power levels were they are most suited, they are mapped and shown in Figure 2.8.

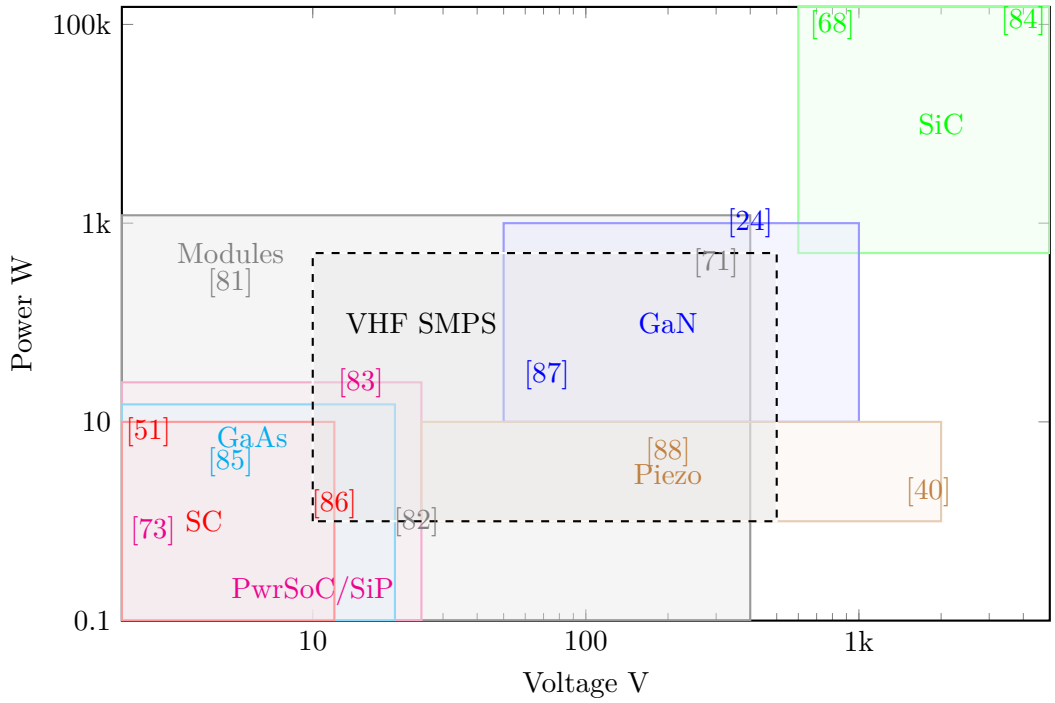


Figure 2.8: Material and technology selection depending on voltage and power level.

The general trend is to push for higher operating frequencies in order to minimize the passive elements. This is done both through new circuit topologies and new components/materials. The only technology not following this trend is the piezo transformer, they are best suited for operation at relatively low frequencies. With this technology the bulky transformers can be replaced by small ceramic elements, but big input and output filters are still needed.

The rest of the technologies support each other quite well and the different materials each have their own areas where they are best suited. For the voltage and power levels of interest in this thesis, the technologies from the modules/PSiP and GaN could go very well hand in hand with resonant VHF converters. SiC are generally better suited for higher power and voltage levels and GaAs, SC and PwrSoC are still to far from the power and voltage levels of interest.

Chapter 3

Topologies

Traditional SMPS topologies like Buck and Boost are hard switching, this means the MOSFET is switching while there is voltage across it and/or current running through it. The result is that energy is dissipated in the MOSFET every time it turns on, i.e. switching losses. In traditional converters the switching frequency is chosen as a tradeoff between switching losses, size and price. In most commercial product a switching frequency in the range 50-400 kHz is chosen as this gives a good tradeoff. When the frequency is increased to the Very High Frequency (VHF) range (30-300 MHz) the switching losses get almost 1000 times larger. This amount of energy would ruin the efficiency and require extreme cooling of the MOSFET.

In order to avoid switching losses and be able to increase the frequency while keeping the efficiency high, new topologies have to be used. Through three decades (since the 1980's [89, 90]) research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc/dc converters, see Figure 3.1. With this type of converters it is possible to achieve Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS). In this case the MOSFET turns on when the voltage and/or current across/through it is zero. Theoretically this should eliminate switching losses, if the switching is done instantaneously and at exactly the right time. This is not practically achievable, but even with slight deviations from the ideal case very high efficiencies can be achieved.

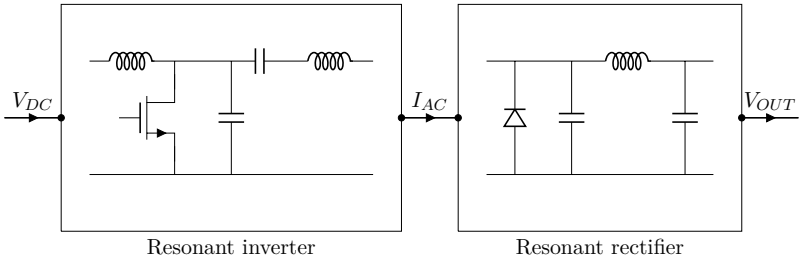


Figure 3.1: Block diagram of a VHF converter.

As already mentioned the value of the passive components depends on the switching frequency. Hence an increase in frequency will lead to a reduction in size, as long as the size of the passives scales with the value. This assumption generally holds, but magnetic materials and packaging introduce some challenges. When the frequency is pushed far into the MHz range, magnetic core loss increases rapidly and becomes unacceptably high for most core materials [91]. At this point air core and PCB embedded inductors become a viable solutions, as the inductances needed at these frequencies can be made in a small physical size and the core losses avoided [92, 93].

Increasing the switching frequency also leads to capacitors with lower values. Electrolytic capacitors, which often limits the overall lifetime, can hence be avoided [94, 95]. The reduction in component values also leads to a cost reduction, as smaller components are generally cheaper. If the frequency is increased enough, some of the components can even be left out, as they can be constituted by the parasitic parts of other components. The capacitor in parallel with the MOSFET will for instance often be, at least partly, constituted by the ouput capacitance of the MOSFET. An increase in switching frequency will also make it easier to comply with EMI requirements, as small and cheap filters can easily filter out switching harmonics.

Since the development of the first SMPSs, there has been a general push towards higher frequencies for the above-mentioned reasons. This and the recent development in wide band gap semiconductors has lead to switching frequencies at a few MHz in todays state-of-the-art SMPSs [96]. Following this trend with incremental improvements and increase in frequency, the next step would be to make SMPSs with switching frequency of 5-10 MHz. However at frequencies above a few MHz the core materials start to exhibit huge core losses and air core inductors becomes the only efficient solution. Without the core the structure needed to achieve the desired inductance at 5-10 MHz would however be even bigger, than the cored inductors that could be used at 1-2 MHz. Therefore the frequency needs to be pushed even further to achieve a size reduction without core materials. At frequencies around 20-25 MHz similar sizes can be achieved and beyond that size reduction can be achieved even with the air core inductors [97].

With a switching frequency between 30 and 300 MHz, the main concern when selecting topology is switching losses. The switching loss in a MOSFET due to the parasitic output capacitance increases linearly with the switching frequency and becomes the dominating loss mechanism at these frequencies, if the topology does not take this into account.

To illustrate the losses at these frequencies, the simplified equations for conduction and switching losses in a synchronous buck converter will be used [98, 99]:

$$P_{CON,LOSS} = I_{OUT}^2 \cdot R_{DS,ON} \tag{3.1}$$

$$P_{SW,LOSS} = 2 \cdot \frac{1}{2} \cdot C_{OSS} \cdot V_{DS}^2 \cdot f_S \tag{3.2}$$

Here V_{DS} is the voltage between the drain and the source of the MOSFET, C_{OSS} is the parasitic output capacitance of the MOSFET, $R_{DS,ON}$ is the on resistance of the MOSFET and I_{OUT} is the output current of the converter.

The two sets of converter specifications given in Table 3.1 will be used as exam-

Table 3.1: Two sets of converter specifications

	$\mathbf{V}_{IN}$	$\mathbf{V}_{OUT}$	$\mathbf{P}_{OUT}$
$SMPS_1$	50 V	5 V	5 W
$SMPS_2$	330 V	20 V	50 W

ples throughout this chapter. MOSFETs with high on resistance and low output capacitance will be used for both, in order to reduce the switching losses. The on resistance and output capacitance is linked due to the FOM of the material and the device structure, hence one have to be traded off to improve the other. The output capacitance domminates the switching losses, so for fast switching conveters it is essential to keep this low. For the 50 V converter, this gives $R_{DS,ON} = 1.6\ \Omega$ and $C_{OSS} = 10$ pF [100] and for the 330 V converter $R_{DS,ON} = 1.2\ \Omega$ and $C_{OSS} = 20$ pF [101]. With these values the losses for $SMPS_1$ becomes:

$$P_{CON,LOSS} = 1\ A^2 \cdot 1.6\ \Omega = 1.6\ W \tag{3.3}$$

$$P_{SW,LOSS} = 2 \cdot \frac{1}{2} \cdot 10\ pF \cdot 50\ V^2 \cdot 30\ MHz = 0.7\ 5W \tag{3.4}$$

and for $SMPS_2$ it becomes:

$$P_{CON,LOSS} = 2.5\ A^2 \cdot 1.2\ \Omega = 6.25\ W \tag{3.5}$$

$$P_{SW,LOSS} = 2 \cdot \frac{1}{2} \cdot 20\ pF \cdot 330\ V^2 \cdot 30\ MHz = 65.3\ W \tag{3.6}$$

These losses are clearly not acceptable. For the 5 W converter an efficiency of 68% could be achieved if all other components where ideal, but for the 50 W converter the maximum efficiency would be 41%.

Therefore all topologies investigated in this chapter will be so called zero voltage switching (ZVS) topologies. All the topologies are derived from the class E inverter, which utilizes the output capacitance in the design and insures that the capacitance is fully discharged before the MOSFET is turned on.

Some topologies can achieve zero current switching (ZCS) as well. This removes the loss caused by parasitic inductances in for instance the package of the MOSFET. This is generally not a big loss mechanism in power converters [99]. This is however very desirable due to the fact, that it leads the derivative of the voltage to be zero at the switching instance (ZdVS or ZDS). This reduces the impact if the MOSFET is not turned on exactly at the right time, as the voltage across it will be close to zero for an amount of time.

When designing resonant DC/DC converters it is very common to split the converter into two parts; 1) a resonant inverter converting the DC input voltage to an AC output current 2) a resonant rectifier rectifying the AC current to a DC output [102, 103, 104], see Figure 3.1.

It is possible to design the inverter to a load, which give optimal operating conditions for the inverter, and then use different resistance compression networks to make the impedance of the rectifier match [105, 106, 107]. Though this is a solution often used, it will increase the complexity of the converter unnecessarily and

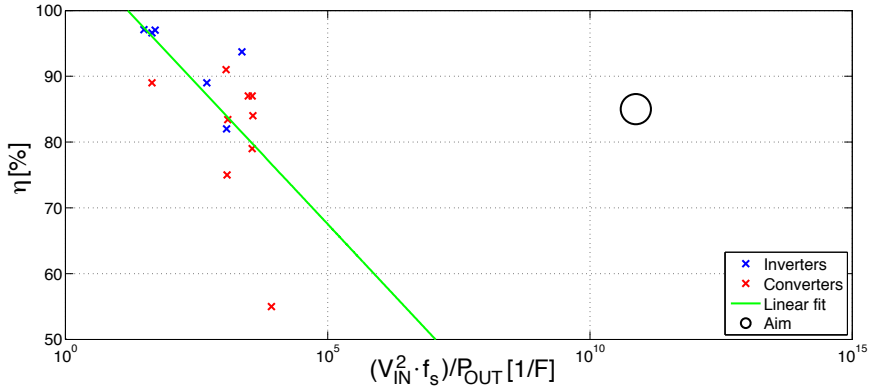


Figure 3.2: Relation between $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$ and η for the converters in table 3.2.

possibly reduce the achievable efficiency, size, and price. Therefore the best design procedure is firstly to design a rectifier for the given load and then design the inverter for the given input and rectifier impedance.

The most commonly used inverter is the class E, however several other topologies exist. Some of the research results are summed up in Table 3.2. From Table 3.2 it is seen that very high efficiencies are achievable for the inverters, up to 97%. However the efficiency drops around 10% for the complete DC/DC converters, i.e. when a rectifier is added. By further inspection of Figure 3.2, it can be seen that it is problematic to have a high input voltage and switching frequency while having a low output power and still keep the efficiency high. This is mainly due to the output capacitance, C_{OSS}, and the energy stored herein. The energy stored in C_{OSS} is set by the capacitance and the peak voltage across the MOSFET. The peak voltage varies between V_{IN} for a half bridge [108] and $3.56 \cdot V_{IN}$ for a class E [102], but is for all topologies a function of V_{IN}.

The energy stored in C_{OSS} has to be charged and discharged every switching cycle in order to achieve ZVS. Combining C_{OSS}, V_{IN} and f_S hence gives a measure for the minimum resonating currents needed inside the converter to achieve ZVS. If this current is much larger than what is needed to deliver the desired output power, losses will apear in the ESR of the components in the power stage without giving more power out. Hence the converter will exhibit higher loss without increased output power, causing the efficiency to drop. This relation can be described by eq. 3.7:

$$\frac{V_{IN}^2 \cdot C_{OSS} \cdot f_S}{P_{OUT}} \propto \frac{1}{\eta} \tag{3.7}$$

The next sections will describe and compare the various topologies suitable for operation in the VHF range.

Table 3.2: Results from previous research

Inverters

Topology	$\mathbf{f}_s$ [MHz]	$\mathbf{V}_{IN}$ [V]	$\mathbf{V}_{OUT}$ [V]	$\mathbf{P}_{OUT}$ [W]	η [%]	Year
Class DE	5.3	330	N/A	1154	89	1999 [109]
Class E	1	128	N/A	366	96.6	2006 [110]
Class ϕ_2	1	129	N/A	526	97.1	2006 [110]
Class ϕ_2	30	160	N/A	330	93.7	2007 [111]
Class E	1	129	N/A	322.7	97	2007 [112]
Class E	100	9	N/A	6.8	82	2011 [113]

Converters

Topology	$\mathbf{f}_s$ [MHz]	$\mathbf{V}_{IN}$ [V]	$\mathbf{V}_{OUT}$ [V]	$\mathbf{P}_{OUT}$ [W]	η [%]	Year
Class E	1	20	25	8.9	89	1989 [104]
Class ϕ_2	30	165	33	265	87	2006 [99]
Class E	100	11	12	10	75	2006 [32]
Class ϕ_2	30	150	33	180	84	2008 [103]
Class ϕ_2	10	170	75	250	91	2009 [31]
Class ϕ_2	30	165	33	225	87	2009 [31]
Class ϕ_2	30	330	50	900	79	2009 [114]
Class E	100	12	23.7	1.7	55	2010 [115]
Push-Pull ϕ_2	30	140	65.4	471.9	83.4	2010 [116]

3.1 Single Switch

Single switch inverters and rectifiers are by far the most common choice for VHF or even HF converters. Only one of the examples given in Table 3.2 is not a single switch topology.

The class E inverter is the fundamental ZVS single switch topology and the most commonly used [110, 112]. Several other topologies derived from the class E inverter exist, such as the class EF_2 (ϕ_2) [117, 103], the resonant SEPIC [118, 119] or the resonant boost converter [120, 121].

On the rectifier side it is more or less the same situation, with the class E being the most commonly used rectifier [104, 32, 114] and a few other alternatives derived hereof [102, 90, 108].

All the single switch topologies have a switch and an inductor coupled in series across the input or output, for the inverter and the rectifier respectively. In order to keep the volt-second balance across the inductor, the average drain-source voltage (V_{DS}) of the switch has to be equal to the input voltage. Even if V_{DS} is assumed constant when the switch is closed, the peak voltage has to be two times V_{IN} for a duty cycle of 50%. In reality the voltage across the switch is more like a half wave rectified sine wave in order to achieve ZVS, which result in a peak voltage of 3.56 times V_{IN} for the class E inverter [110]. This high voltage stress on the semiconductors is the biggest challenge with single switch topologies, but they are

often chosen due to the complexity and losses connected with a high side gate drive for operation in the VHF range.

This section will first introduce the class E inverter and its equivalent rectifier. Then three modifications of this will be covered, namely the class ϕ_2, the resonant single-ended primary-inductor converter (SEPIC) and the resonant boost.

3.1.1 Class E

The most commonly used resonant inverter is the class E, a schematic of it is shown in Figure 3.3. It consists of a single MOSFET, two inductors, and two capacitors. In optimum operation L_{IN} is an infinite choke providing a pure dc input current. The resonant circuit (L_R and C_R) is inductive at the switching frequency and the inverter is designed to have both ZVS and ZDS.

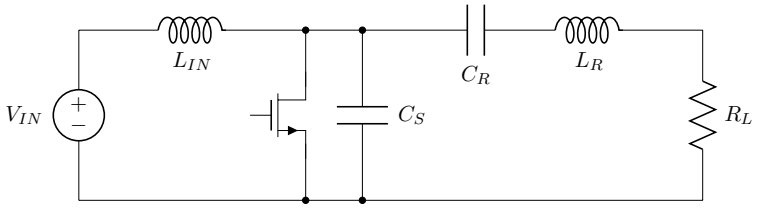


Figure 3.3: Schematic of the class E inverter.

The inverter can only achieve both ZVS and ZDS switching in very specific situations. According to [122, 123] this can only be achieved if:

$$R_L = \frac{8}{\pi^2 + 4} \cdot \frac{V_{IN}^2}{P_{OUT}} \tag{3.8}$$

$$f_{S,max} = \frac{P_{OUT}}{2 \cdot \pi \cdot C_S \cdot V_{IN}^2} \tag{3.9}$$

If the values from the two converter examples are put into these equations we get:

For the 50 V input and 5 W:

$$R_L = \frac{8}{\pi^2 + 4} \cdot \frac{50\ V^2}{5\ W} = 288\ \Omega$$

$$f_{S,max} = \frac{5\ W}{2 \cdot \pi \cdot 10\ pF \cdot 50\ V^2} = 31.8\ MHz$$

For the 330 V input and 50 W:

$$R_L = \frac{8}{\pi^2 + 4} \cdot \frac{330\ V^2}{50\ W} = 1.26\ k\Omega$$

$$f_{S,max} = \frac{50\ W}{2 \cdot \pi \cdot 20\ pF \cdot 330\ V^2} = 3.7\ MHz$$

It is possible to drive the 5 W converter at 31 MHz, i.e., in the VHF range, and achieve both ZVS and ZCS, but it requires a load impedance of 288 Ω. The

impedance of the load in this example is 25 Ω, but impedance matching networks can be used to adjust the impedance seen by the inverter [105, 106, 107]. These matching networks do however add to the complexity of the circuit and there will be losses associated with these components as well. Hence it might be more desirable to sacrifice the ZCS in order to keep the number of components low.

For the 50 W converter the maximum operating frequency is 3.7 MHz, high compared to commercial products, but way below the VHF range. The impedance of the load is 8 Ω, but the load impedance of the inverter should be 1.26 kΩ. Again impedance matching networks could be used to compensate for some of the misalignment, but the desired specifications are clearly too far from the specifications needed to achieve both ZVS and ZCS at VHF.

By sacrificing the ZCS for more design flexibility the control of the inverter becomes more important. The inverter will be running in a subnominal condition, as described further in [124, 113], and the derivative of voltage across the MOSFET will not be zero as it crosses zero volt. The result is that there will be one very specific point in time were ZVS can be achieved, if the MOSFET is turned on just a little earlier or later the voltage will have changed. The amount it has changed depends on how far the design is from the optimum case, i.e., how much current is running through the switch when the voltage crosses zero. If the MOSFET is turned on to early, the capacitor will not be fully discharged and switching losses will occur. If the MOSFET, on the other hand, is turned on too late, the body diode will start to conduct and prevent the voltage from dropping significantly below zero. Body diodes are generally lossy and this is hence not desirable [125].

Not designing for the optimal operation point of the class E inverter also makes it possible to change the duty cycle and remove the choke inductor at the input, hence increasing both power density and response. Doing so the standard equation found in RF amplifier text books [122, 123] cannot be used and a new set of design equations has to be derived.

If the drain source voltage of the MOSFET is assumed to be a half sine wave when it is off and zero when it is on, the peak voltage across the MOSFET will be:

$$V_{IN} = \int V_{DS} = V_{DS,peak} \frac{2 \cdot (1 - D)}{\pi} \tag{3.10}$$

$$\Updownarrow$$

$$V_{DS,peak} = V_{IN} \frac{\pi}{2 \cdot (1 - D)} \tag{3.11}$$

The rms value of a half wave rectified sine wave is:

$$V_{DS,rms} = V_{DS,peak} \sqrt{\frac{D}{2}} \tag{3.12}$$

And the rms value of the output voltage is:

$$V_{OUT,rms} = \sqrt{P_{OUT} \cdot R_L} \tag{3.13}$$

According to [99] the reactance of the resonance circuit can now be determined by:

$$X_{RC} = R_L \cdot \sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1} \tag{3.14}$$

By combining equation 3.11, 3.12, 3.13, and 3.14, an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained:

$$X_{RC} = R_L \cdot \sqrt{\frac{V_{IN}^2 \cdot \pi^2 \cdot D}{2 \cdot (2 \cdot D - 2)^2 \cdot P_{OUT} \cdot R_L} - 1} \tag{3.15}$$

It can be desirable to keep the duty cycle low in order to reduce the peak voltage across the MOSFET, however due to turn on and off times and delays it is desirable to keep it in the range 30-50%.

The values of the inductor and capacitor for the resonance tank can be calculated based on the reactance derived in equation 3.15 and the desired loaded Q factor of the resonant tank:

$$Q_R = \frac{1}{R_L}\sqrt{\frac{L_R}{C_R}} \tag{3.16}$$

$$X_{RC} = \omega_S \cdot L_R - \frac{1}{\omega_S \cdot C_R} \tag{3.17}$$

From these two equations expressions for L_R and C_R can be derived:

$$C_R = \frac{X_{RC} + \sqrt{4 \cdot Q_R^2 \cdot R_L^2 + X_{RC}^2}}{2 \cdot Q_R^2 \cdot R_L^2 \cdot \omega_S} \tag{3.18}$$

$$L_R = \frac{2 \cdot Q_R^2 \cdot R_L^2 + X_{RC} \cdot \sqrt{4 \cdot Q_R^2 \cdot R_L^2 + X_{RC}^2} + X_{RC}^2}{(X_{RC} + \sqrt{4 \cdot Q_R^2 \cdot R_L^2 + X_{RC}^2}) \cdot \omega_S} \tag{3.19}$$

In class E inverters for RF amplifiers, it is desirable to keep the loaded Q of the resonant tank high (>10) in order to insure a pure sinusoid at the output [126, 127]. For power conversion where a DC output is the target, this is however not necessary. In fact, there are a few good reasons not to have a high Q resonant tank. The resonant tank is inductive at the switching frequency in order to achieve ZVS, hence a high Q would require a large inductor, see equation 3.16. This is both the largest component in the circuit; it slows down the transient response and introduces a larger series resistance. It is generally good to keep the Q between 0.3 and 2. As seen in Figure 3.4 the size of the inductor increases rapidly beyond this range and the size of the capacitor start to increase significantly below this range.

Another important parameter when selecting the components for the resonant tank is component tolerances. Most components come with a given tolerance, which can be reduced for a premium on the price. Ceramic capacitors with 5% tolerances [128] and air core inductors with 2% tolerances [129] can generally be bought at fair prices. As the output power of the inverter is set directly by the reactance of the resonant tank, see equation 3.15, these tolerances will directly impact the output

power. Further the reactance of the resonance tank contributes to the resonance of the entire converter and thereby to achieving the crucial ZVS. Tolerances in the components will therefore affect the frequency at which ZVS can be achieved. As the resonant tank is inductive at the switching frequency, the inductor dominates the reactance of the tank and the tolerance of the inductor is therefore the most important.

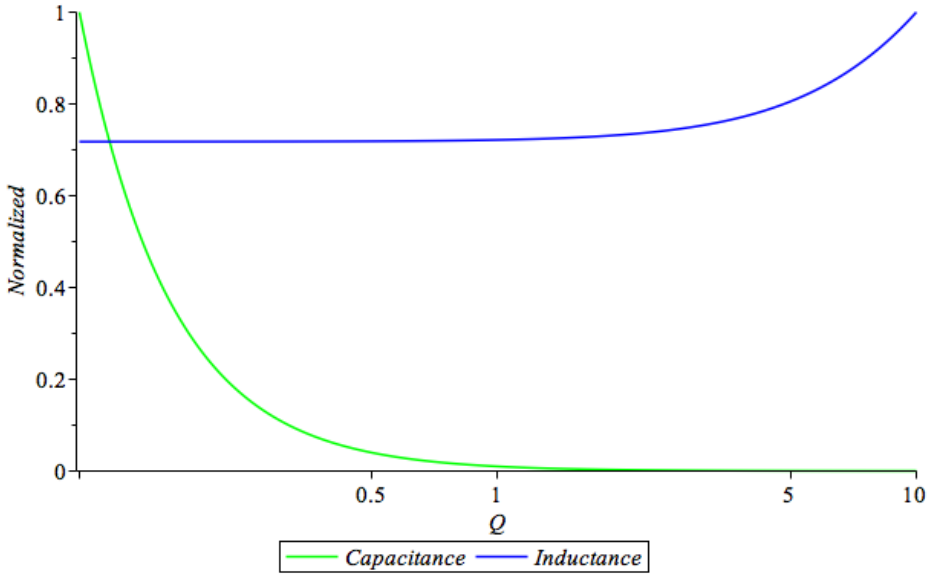


Figure 3.4: Normalized values of L_R and C_R as function of loaded Q factor.

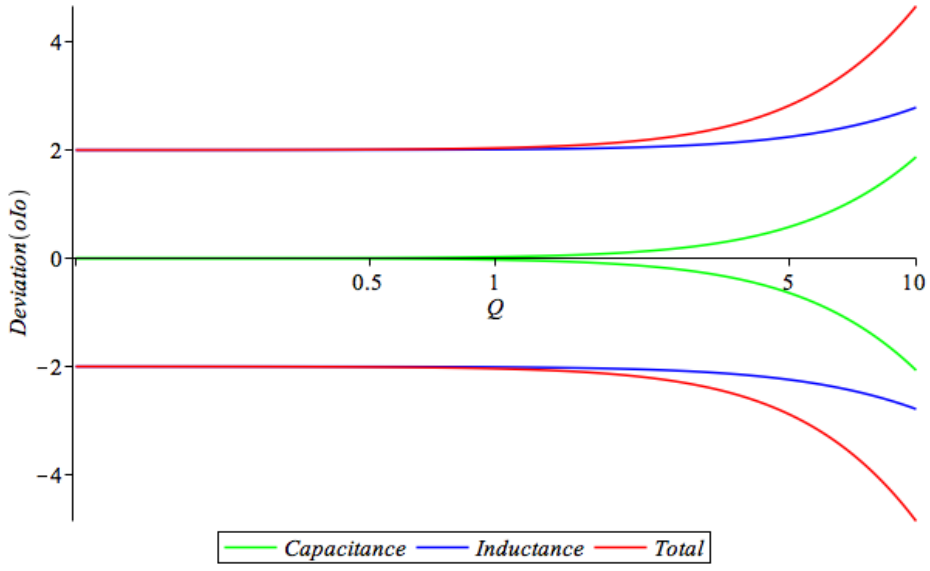


Figure 3.5: Deviation from the decired reactance depending on loaded Q factor.

Figure 3.5 shows the deviation in the reactance of the resonant tank that can appear with the mentioned tolerances depending on the selected Q. For a Q below 1 the deviation is directly dependent on the inductor, but for Q values above 1 the tolerances of the capacitor starts to add to the deviation. The plot in Figure 3.5

just shows the tolerances on the capacitors when the DC voltage across is zero. In the converter the capacitor in the resonant tank will be the part that blocks a DC current from running between the input and output, hence the capacitor will have a DC bias equal to the difference between the input and output. This DC bias can cause up to 50% [130] deviation form the rated value. For this reason it can be desirable to keep the Q below 1 if the converter is designed to have a big step ratio.

The two remaining components to be calculated are L_{IN} and C_S. From equation 3.9 it was seen that C_{OSS} will often set the upper limit for the switching frequency. As explained it is possible to design around this, but at the expense of increased switching currents. Therefore C_S will be constituted solely by the parasitic capacitance of the MOSFET in VHF converter operating with high input voltages and low power levels (compared to what is possible according to equation 3.9 and 3.8).

For class E inverters used for RF amplifiers the input inductor is normally a choke, but this limits the transient response and will be a bulky component. Further the inductor needs to be small enough to resonate with the resonant tank and C_S in order to achieve ZVS. The frequency at which these components have to resonate is equal to two times the period where the switch is open, i.e.:

$$T_R = 2 \cdot (1 - D) \cdot T_S \Leftrightarrow f_R = \frac{f_S}{2 \cdot (1 - D)} \tag{3.20}$$

In order to calculate the value of L_{IN}, it is necessary to calculate the effective value of C_S. The output capacitance of the MOSFET is only contributing to the resonance in the part of the period where the MOSFET is off, hence it has to be scaled by 1-D in order to find the effective capacitance. The effective capacitance of the output capacitor is $C_{S,eff} = \frac{C_S}{1-D}$. Knowing the values of X_{RC}, the input inductance can be calculated according to:

$$L_{IN} = \frac{1}{\omega_R^2 \cdot C_{S,eff} - \frac{\omega_R}{X_{RC}}} \tag{3.21}$$

The design equations for all the components in the class E inverter have now been given. In order to make a complete VHF converter a rectifier is needed. The class E rectifier shown in fig. 3.6 is equivalent to the inverter in many ways. The waveforms of the two circuits are shown and described in A.3.

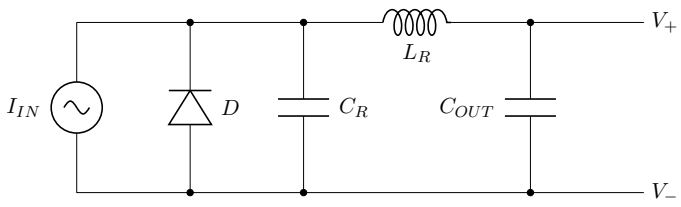


Figure 3.6: Schematic of the class E rectifier.

The rectifier is designed to appear resistive at the switching frequency, by insuring that L_R and C_R resonate at this frequency. This simplify the design of the inverter as the design equations are for a resistive load.

The duty cycle of the diode can be adjusted by these components. A long duty cycle will reduce the peak currents but increase the peak voltage across the diode and vice versa for a short duty cycle. With a diode duty cycle, D_D, of 50% the value of C_R should be [102]:

$$C_R = \frac{1}{2 \cdot \pi^2 \cdot f_S \cdot R_L} \tag{3.22}$$

With this capacitance the value of L_R can be calculated according to [102]:

$$L_R = \frac{1}{(2 \cdot \pi \cdot f_S)^2 \cdot C_R} \tag{3.23}$$

The complete design of a class E inverter with a class E rectifier is covered in A.4. The paper describes the design of a converter with 50 V input and an output of 5 V and 1 W. This places this design far from any other designs that had been made at that point, see Figure 3.7. Further this inverter was designed with a standard silicon MOSFET and achieved efficiencies up to 82.9%.

The low output voltage compared to the forward voltage drop of the diode, gave rise to a significant loss in the rectifier diode. Therefore synchronous rectification were investigated in A.11 and it was found that synchronous rectification of VHF converters can indeed give a significant efficiency boost for applications were the output voltage is low (<5 V) and the current high (>2 A).

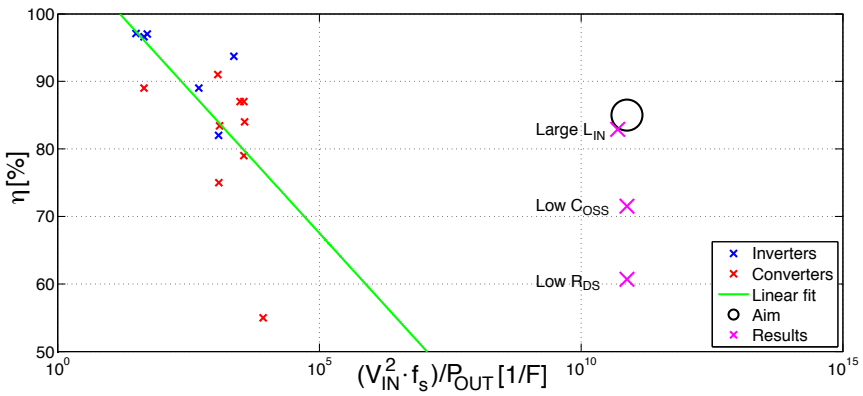


Figure 3.7: The $\frac{P_{OUT}}{V_{IN} \cdot f_S}$-factor and η achieved in A.4 next to previous results.

3.1.2 Class ϕ_2

As written in section 3.1, the large voltage peak across the MOSFET is the major problem for single switch inverters in application with high input voltage.

Voltage stress in these converters can be reduced by employing multi-resonant networks, either transmission line [131, 132, 133] or discrete with limited number of harmonics [111, 134, 103]. By implementing these techniques, switch voltage stress in VHF converters can be reduced to 2-2.5 times the input voltage for the same duty cycle, but this technique requires extra resonant elements.

The class ϕ_2 (or EF_2) inverter, which is a hybrid between the class E and F_2 inverters, was developed in order to make the voltage across the MOSFET closer to a square wave. The voltage across the MOSFET should thereby become significantly smaller (ideally $2 \cdot V_{IN}$ for $D = 50\%$). This is done by inserting an LC circuit in parallel with the MOSFET as shown in Figure 3.8. This circuit is designed to have a resonance frequency at the second harmonic, which causes the voltage across the MOSFET to become a trapezoidal wave consisting of the 1st and 3rd harmonic. The same benefits can be achieved with the flat-top class-E amplifier described in [135].

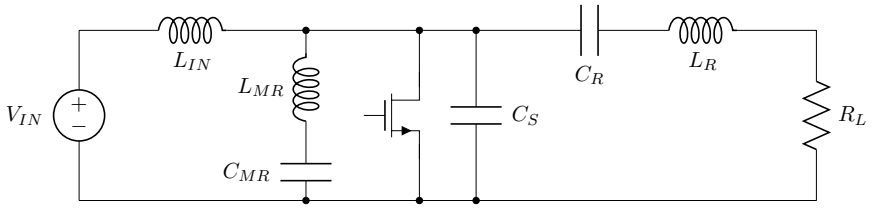


Figure 3.8: Schematic of the class ϕ_2 inverter.

According to [103] the rms voltage across the MOSFET can be estimated by $V_{DS,rms} = V_{IN}\frac{4}{\pi \cdot \sqrt{2}}$, thus the needed reactance of the resonant circuit is different (see equation 3.14). No exact equations for the calculations of the added LC circuit or the input inductance are given in literature, however the following gives results which are close [111]:

$$L_{IN} = \frac{1}{9 \cdot \pi^2 \cdot f_S^2 \cdot C_S} \tag{3.24}$$

$$L_{MR} = \frac{1}{15 \cdot \pi^2 \cdot f_S^2 \cdot C_S} \tag{3.25}$$

$$C_{MR} = \frac{15}{16} \cdot C_S \tag{3.26}$$

This topology was investigated in A.4, but it was found to have higher losses and a larger component count than the class E inverter due to the introduced third harmonics. The voltage across the MOSFET is indeed lowered, which can be an advantage in applications were a small reduction in required break down voltage makes new semiconductors available. The resonant currents at the switching frequency are however the same as for the class E, but with added currents at the third harmonics. This makes it even more difficult to achieve high efficiency at low power levels, due to the relation described in equation 3.7.

3.1.3 Single-Ended Primary-Inductor Converter

The Single-Ended Primary-Inductor Converter (SEPIC) has several semilarities to the class E inverter with a class E rectifier. As shown in Figure 3.9 the only difference is that the inductor in the resonant tank is removed. As explained in section 3.1.1 this inductor is however quite important and used both to regulate the output power and to insure that ZVS is achieved.

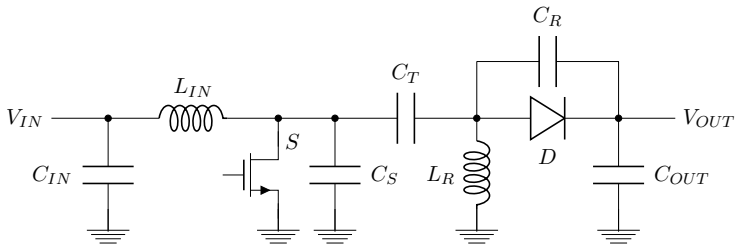


Figure 3.9: Schematic of the SEPIC converter.

Hence the design and behaviour of the SEPIC is different than that of the class E. No fixed equations are availible for this topology, but one design methodology is given in [118]. Here the converter is designed by firstly designing the rectifier part as a normal class E rectifier, were the rectifier is made to apear resistive at the switching frequency. However for the SEPIC described in A.5, the rectifier is designed to apear sligthly inductive at the resonance frequency, as this was found to give higher efficiency. Once the rectifier part is designed the capacitor, C_T, is set to get the desired output power and finally the input inductor, L_{IN}, is set to insure ZVS.

The design process of the SEPIC is more complicated than for the class E, due to the lack of equations to calculate the component values. However once the converter is designed it achieves better total specifications than seen for the class E. It has one inductor less than the class E and both of the two remaining inductors are smaller. This does not only increase the power density and reduce the bill of material, it also enables higher efficiency as the resonating current runs through less series resistance.

3.1.4 Resonant Boost

The resonant boost converter shown in Figure 3.10 is another class E derived topology suited for operation at VHF. During the design the converter is as for the other topologies split into a inverter and a rectifier; the inverter is constituted by the input inductor, L_{IN}, the MOSFET and the capacitor, C_S, and the rectifier is made up by the inductor, L_R, the capacitor, C_R, and the diode [136]. In practical designs the two capacitors may be constituted by the parasitic capacitances of the MOSFET and diode, respectively. Hence this converter can be made with only four components, a MOSFET, a diode and two inductors.

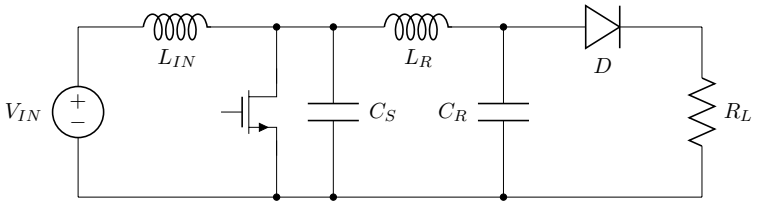


Figure 3.10: Schematic of the resonant boost converter.

The converter has a DC path from input to output, which makes it useless for buck

(step down) applications, but it is quite attractive for boost applications due to the low component count. As the focus of this thesis has been on buck applications this topology has not been tested, but good results have been shown with efficiencies of up to 87% [137, 138, 139].

3.2 Half Bridge

The research in VHF converters has been very focused on the single switch topologies. This is due to the fact that no high side gate drives have been available for operation above a few volts. A 200 MHz integrated buck converter with a high side gate drive was presented in [140],but it only had a 3.6 V input and peak efficiency of 77%. If a high side gate drive can be designed for operation at VHF and at higher voltages, it opens up a new range of topologies, which all deal with the major drawbacks of the single switch topologies, namely high voltage stress and large resonating currents.

Some of the topologies most suited for operation at VHF are investigated further in the following subsections.

3.2.1 Class DE

The class DE inverter is a merger of the class D half bridge converter and the class E zero voltage switching inverter. Hence this topology offers the low semiconductor stress of the half bridge with zero voltage switching. In the class DE inverter the switches are directly connected to the input and the voltage across them is therefore limited to the input voltage (see Figure 3.11). The class DE inverter has two other great advantages over the single switch topologies, it has only a single inductor and due to the lower peak voltage across the MOSFET, the stored energy is more than ten times lower than for the class E ($E = \frac{1}{2} \cdot C_{OSS} \cdot V_{IN}^2$ compared to $E = \frac{1}{2} \cdot C_{OSS} \cdot (3.56 \cdot V_{IN})^2$), leading to much smaller resonating currents in a buck type converter, see A.3.

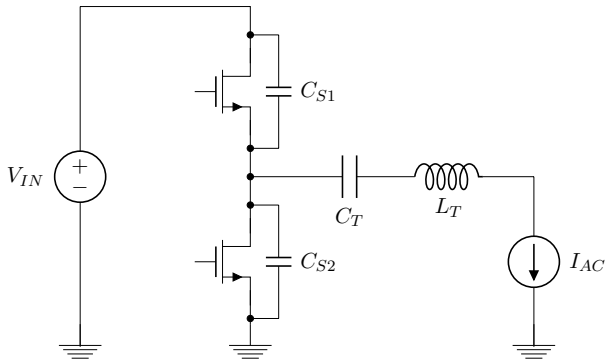


Figure 3.11: Schematic of the class DE inverter.

The component values can be derived with the same approach as used for the other topologies. If the voltages on both sides of the resonant circuit (C_T and L_T)

are assumed to be trapezoidal, the rms voltages in those nodes can be calculated according to equation 3.27 and 3.28.

$$V_{DS,rms} = V_{IN} \cdot \sqrt{\frac{D_M + 1}{3}} \tag{3.27}$$

$$V_{REC,rms} = V_{OUT} \cdot \sqrt{\frac{D_D + 1}{3}} \tag{3.28}$$

Where D_M and D_D is the duty cycle of the MOSFET and the diode, respectively. The reactance of the resonance circuit is calculated according to equation 3.29 [99].

$$X_{RC} = R_{REC} \cdot \sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1} \tag{3.29}$$

Once the reactance of the resonant circuit is calculated, a suitable capacitance can be chosen and the inductance calculated. The capacitors C_{S1} and C_{S2} need to resonate with the resonant circuit at a frequency given by:

$$\omega_R = \frac{\omega}{2 \cdot (1/2 - D_M)} \tag{3.30}$$

Hence:

$$\omega_R^2 = \frac{1}{2 \cdot C_S \cdot \frac{X_{RC}}{\omega_R}} \tag{3.31}$$

Combining equation 3.30 and 3.31 leads to the following expression for the value of C_{S1} and C_{S2}:

$$C_S = \frac{1/2 - D_M}{\omega \cdot X_{RC}} \tag{3.32}$$

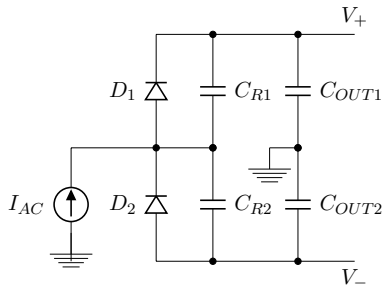


Figure 3.12: Schematic of the class DE rectifier.

For high output voltages, a class DE rectifier [141] also offers some advantages over the class E rectifier. As for the inverter the diodes are connected directly to the output and the voltage across them is hence limited to the output voltage (see Figure 3.12). It is a challenge to find schottky diodes suited for operation at VHF with break down voltages above 60-80 V, which limits the class E rectifier to output

voltages around 20 V ($\approx \frac{60-80V}{3.56}$). With a DE rectifier output voltages up to 60 V can be achieved with good design margin. This comes at the expense of twice the forward conduction loss, so this rectifier is not suited for low voltages. Furthermore the class DE rectifier is inductor less and hence offers a much higher power density, as the inductor is generally the biggest component.

3.2.2 LLC Converter

The LLC converter were presented in section 2.1.1 and is one of, if not the most, used topologies for resonant converters switching up to a few MHz. It is less load dependent than the purely series loaded resonant topologies, which the class DE with a class E or DE rectifier would be. At the same time it keeps the high efficiency, in contrast to the purely parallel loaded topologies. This topology is therefore very likely to be well suited for operation in the VHF range as well.

The first VHF half bridge was however demonstrated in A.6 and no other have been presented so far. Hence no experimental results are availible for a LLC converter operating at VHF. With the results from A.6, this is however a very interesting next step.

Another more or less equivalent option is the LCC, which would be equivalent to add more capacitance across the rectifier diodes, so in some way it is already there. However a converter with more capacitance, or with variable capacitance, need to be build to test the load dependence and efficiency variation to tell if this is an efficient solution.

3.3 Stacking

Another approach to reduce the voltage stress across the switches is stacking cells, i.e. coupling multiple small converters with serial input [119, 142]. This reduces the switch voltage stress by N compared to a single cell case, where N is the number of converter cells. This is a normal approach for low frequency converters when a large step down ratio is required [143]. By arranging several cells with serial input and parallel output (SIPO), a large overall step ratio can be achieved while keeping the stress on the individual cells low [114].

For resonant converters this does not only reduce the peak voltage across the MOSFET, it also makes it possible to get closer to the optimum point of operation. In section 3.1.1 it was found that the maximum operating frequency for the inverter with high input voltage, $SMPS_1$, was 3.7 MHz and the impedance was more than 100 times to high. If the converter where split into seven smaller cells in a SIPO configuration, it would be possible to use the 50 V MOSFET and run the inverter in the optimum point at more than 45 MHz. Further the load impedance required would be divided by 7, thus it would still be to high, but making the final adjustments with impedance matching circuits would be much easier.

Stacking has two main drawbacks, the component count increases significantly and control becomes much more complicated since it requires balancing of the voltages across the cells.

3.3.1 Input-Output Rearrangement

A way to achieve the benefits of stacking without the drawbacks, is to rearrange the input and output as proposed in A.8 and A.9. The converter needs to be isolated to apply this methodology and the isolation will be lost, but a technical isolation can easily be achieved with small ceramic capacitors in VHF converters.

Figure 3.13 shows the conventional input-output configuration of an isolated DC/DC converter. If two isolated converters have their inputs connected in parallel and outputs connected in series, we obtain the structure in Figure 3.14 (top). Similarly, if the inputs are connected in series and outputs in parallel, the structure in Figure 3.15 (top) is obtained.

If one of the converters in each configuration has a 1:1 voltage transformation ratio, it is possible to connect its input to its output directly and remove the 1:1 converter from the circuit, without affecting the rest of the system. In doing so, part of the delivered power flows directly from the input to the output, and is not processed by the converter. As a consequence, higher converter efficiency is achieved. Moreover, compared to the single cell design, voltage and/or current stresses on the switches are reduced, just as if stacking were applied but without the increased component count and complexity. The only difference is that the input is not galvanic isolated from the load. Figure 3.14 and 3.15 (bottom) demonstrate the final connection rearrangement to obtain step-up and step-down configuration, respectively.

To quantify the benefits from the proposed configurations, the case where input voltage V_{in} and output voltage V_{out} are held constant across all configurations is analyzed. Moreover, output current I_{out} and output power P_{out} are held constant as well. A distinction is made between the power processed by the converter P_C, and P_{out}.

The voltage transformation ratio of the conventional converter is

$$M = \frac{V_{out}}{V_{in}}. \tag{3.33}$$

In step-up and step-down configurations, transformation ratio of the converter cell is reduced to

$$M_{up} = \frac{V_{out} - V_{in}}{V_{in}} \tag{3.34}$$

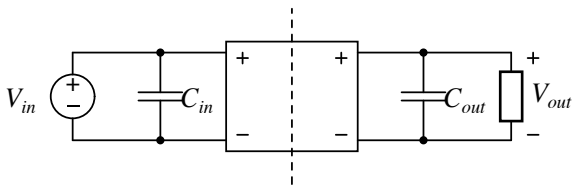


Figure 3.13: Conventional isolated dc/dc converter topology. Dashed line represents galvanic isolation.

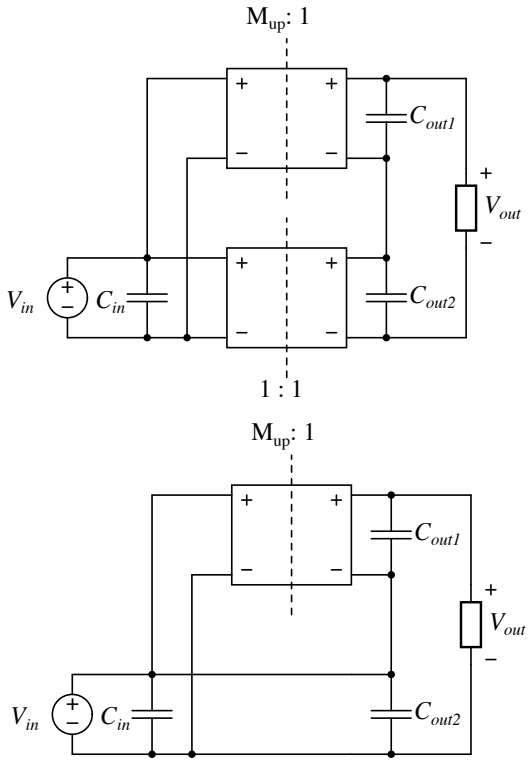


Figure 3.14: Step-up configuration: two converter cells with inputs in parallel and outputs in series (top) and a single cell equivalent (bottom).

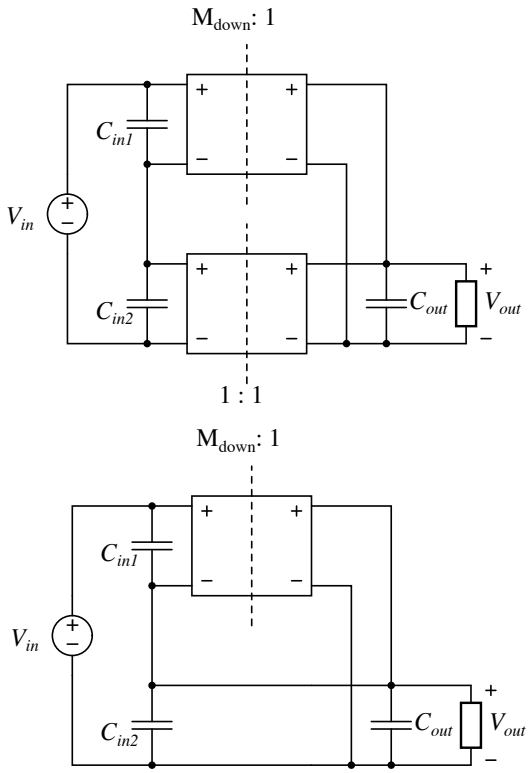


Figure 3.15: Step-down configuration: two converter cells with inputs in series and outputs in parallel (top) and a single cell equivalent (bottom).

and

$$M_{down} = \frac{V_{out}}{V_{in} - V_{out}}. \tag{3.35}$$

In general, switch voltage stress is a function of both input and output voltages. In step-up configuration, output voltage stress contribution is reduced by a factor of $(1 - V_{in}/V_{out})$. In step-down configuration, input voltage stress contribution is reduced by $(1 - V_{out}/V_{in})$.

Output power of all three configurations is the same:

$$P_{out} = V_{out}\, I_{out} \tag{3.36}$$

The power processed by the converter P_C in the conventional structure is equal to P_{out}. In the step-up and step-down cases, this power is given as:

$$P_{C,up} = P_{out} \left(1 - \frac{V_{in}}{V_{out}}\right) \tag{3.37}$$

$$P_{C,down} = P_{out} \left(1 - \frac{V_{out}}{V_{in}}\right) \tag{3.38}$$

$P_{C,up}$ and $P_{C,down}$ are smaller than P_{out}, and the remaining power is delivered through the DC path. Efficiency of that power transfer is very close to 100%. Assuming that P_C, $P_{C,up}$, and $P_{C,down}$ are transferred with the same efficiency η, effective efficiencies of the step-up and step-down configurations can be expressed in terms of η, P_{out}, and $P_{C,up/down}$:

$$\eta_{up/down} = \eta\, \frac{P_{C,up/down}}{P_{out}} + \frac{P_{out} - P_{C,up/down}}{P_{out}} \tag{3.39}$$

Equations 3.37-3.39 are illustrated in Figure 3.16. The plot clearly shows that for limited step-up or step-down ratios, the percentage of the output power processed by the converter is small and hence the efficiency improvement becomes significant. For a step-up converter with 330V input and 400V output, the converter would process only 17.5% of the output power. If the converter efficiency were 80%, the rearranged efficiency would be 96.5%. The converter would in that case have to be designed as a technically (i.e. not according to safety standards) galvanic isolated converter with 330V input, 70V output and a peak output power equal to 17.5% of the required power. Hence a low power flyback or SEPIC converter with moderate efficiency could replace a high power boost converter with high efficiency, while achieving the same overall system performance.

Adaptations shown in Figure 3.14 and 3.15 can be used for any type of isolated converter, regardless of the isolation type (inductive or capacitive). In A.7, a flyback converter is used in a step-up configuration and a class DE converter (DE inverter and DE rectifier) in step-down configuration.

The proposed technique may be used together with stacking as shown in Figure 3.17. That will introduce the drawbacks and advantages of stacking, but the drawbacks will still be reduced as one cell less might be needed.

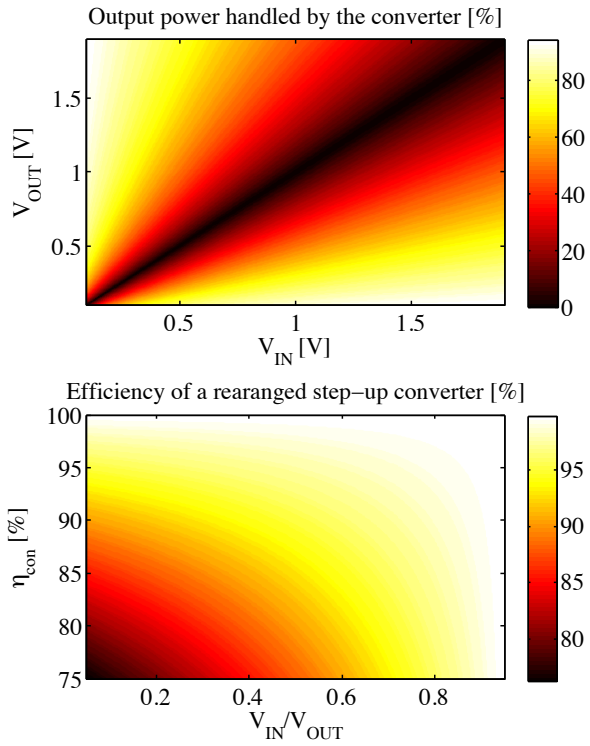


Figure 3.16: Power processed by the converter and efficiency improvement by rearranging.

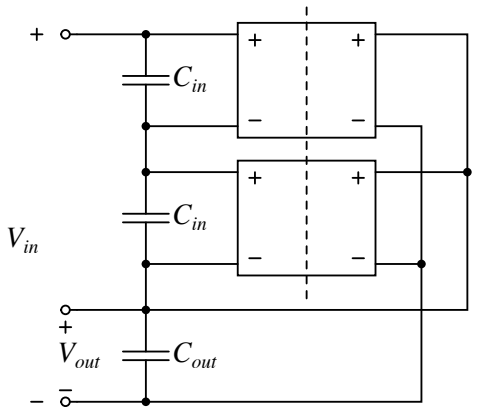


Figure 3.17: Two stacked converters in step-down configuration.

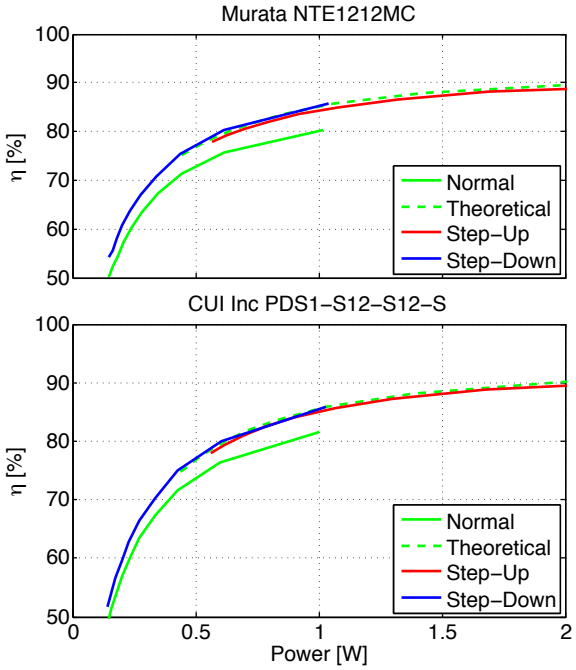


Figure 3.18: Measured efficiencies on two rearanged isolated converters.

The presented technique can be used to reduce voltage and/or current stress for isolated dc-dc converters, in applications where isolation is not a requirement. The technique provides higher efficiency compared to a conventional single cell design, and it can be combined with other methods of voltage stress reduction, as long as the initial converter provides capacitive or inductive isolation. The obtained benefits are very appealing for non-isolated applications. The experimental results shown in A.7 are in good agreement with the presented theory, see Figure 3.18. Twice the power handling capabilities and 5-10% higher efficiencies are shown for the tested converters.

3.4 Summary

Several topologies have been analyzed throughout this chapter. Experimental prototypes of the most suited have been presented in A.5, A.4 and A.6, the class E, SEPIC and class DE respectively. All the inverters had some pros and cons, thus the same inverter will not be best for all applications. The most important pros and cons of the class E, class ϕ_2 and class DE are listed in Table 3.3.

Table 3.3: Pros and cons of the investigated inverter topologies.

	Class E	**Class ϕ_2**	**Class DE**
Pros	• Low side switch • Easy tuning • Well documented	• Low side switch • Reduced stress	• One inductor • Low loss • Low stress
Cons	• Large stress • Large inductors	• Largest loss • Complex	• High side switch

The class E inverter is by far the least complex of the topologies. It is well described in textbooks and straightforward design process are available where the individual components do not severely affect each other. The inverter consists of only one MOSFET, two inductors, and a capacitor (if C_S is composed by the output capacitance of the MOSFET). The voltage stress is the main drawback of this topology for applications with high input voltage, but it is very well suited for applications with low input voltage. If designed to operate in the optimum situation the inductors are the largest for any of the topologies, this limits the transient response and the power density that can be achieved. The inverter can however be designed to operate in a subnominal situation with smaller inductors and faster transient response. The design process for this is not described as thoroughly as the optimal operation, but several publications with different descriptions are available [124, 144, 145].

The SEPIC converter can be seen as a slightly modified version of a class E inverter with a class E rectifier, the only difference in the schematic is that the inductor in the resonant tank is removed. This does not only reduce the number of inductors, but the two remaining inductors will also be smaller than those seen for the class E (if it is designed to operate close to the optimum). The design of the SEPIC is however more complex as the inverter and rectifier cannot be designed separately and all components thereby influence each other. Hence better performance in terms of efficiency, transient response, size and cost can be achieved with the SEPIC, but the design is more complex.

The class ϕ_2 inverter is also a modified version of the class E, the only difference being the added LC circuit put in to reduce the voltage across the MOSFET. While this is a good way to reduce the voltage stress, the steep voltage curves require larger currents, making the loss larger than seen for the class E inverter. Though it has 2 extra components, compared to the class E inverter, the physical size can be more or less the same as the inductors are smaller. The total loss is larger than for the class E inverter due to the higher resonant currents. This might be acceptable if it makes it possible to chose from another class of MOSFET, e.g. 100 V devices instead of 150 V devices, but if that is not the case the class E or SEPIC are better choices.

The class DE inverter is the only half bridge inverter that has been designed and tested experimentally. This is the first VHF half bridge converter operating at more than a few volts presented and thereby one of the major breakthroughs in the work presented.

As C_{S1} and C_{S2} can be composed by the parasitic capacitance of the MOSFETs, the total component count for the class DE inverter is the same as for the class E inverter. The peak voltage across the MOSFETs is by far the lowest seen in any of the inverters and the currents are also the lowest. For class E inverters the nonlinear output capacitance of the MOSFET can also be a big challenge, as it changes the peak voltage across the MOSFET [146, 147, 148], this problem is eliminated with the class DE due to the clamping across the input voltage. Further this topology only has one inductor, which at the same time is smaller than the once in any of the other circuits. The half bridge solution is therefore superior to all the single switch topologies if an efficient high side gate drive can be designed.

The class ϕ_2 inverter was the single switch inverter with the lowest voltage stress.

The voltage stress is approximately $2.5 \cdot V_{IN}$ which is still 2.5 times more than for the half bridge. This result in more than 6 times more energy stored in the output capacitance of the MOSFET, this is the minimum energy that needs to resonate in order to get ZVS. For low power applications with high input voltages this therefore sets the amount of resonant currents. Further the class ϕ_2 specifically has even more resonating current due to the 3rd harmonic introduced to reduce the peak voltage.

From this analysis the class DE inverter is by far the best solution and the SEPIC comes in second. However during this analysis the gate drive has not been considered. This will be done in the next chapter.

The development of each of the prototypes are described thoroughly in the appendices, but some common and important challenges were experienced. First of all it has been a big challenge to find MOSFET suitable for operation in these converters. Not because Si MOSFETs cannot be used for operation in VHF SMPSs, but because they are optimized for hard swicthed converters. In low frequency hard swicthing SMPSs the main optimization criterias for MOSFETs are on resistance and gate charge. These parameters are also important in VHF SMPSs, but the main design parameters are output capacitance and gate resistance, secondly on resistance and series resistane in the output capacitance. The series resistance of the output capacitance is normally not specified in the datasheet, but in VHF application it causes losses similar to those caused by the on resistance.

Further inductors has become a problem, due to the high resonating current caused by the high output capacitance in the MOSFETs availible. With large AC currents the AC resistance or Q factor of the inductors and capacitors becomes very important. Ceramic capacitors are almost lossless due to Q factors as high as 1000 [149, 150], but inductor are hard to find with Q factors above 100-150 [129]. This causes the inductors to be one of the most lossy components in the converters.

Measurements has also been a great challenge due to the low impedance of even a small capacitor at these frequencies. Measuring with a normal probe introduces 10 pF capacitance from the measurement node to ground, this can cause the converter to fail almost instantly. If the probe is added to measure drain-source voltage, the 10 pF ruins the ZVS and causes switching losses so severe that the MOSFET fails due to overheating. Capacitive voltage dividers with small capacitances (1 pF) have been used to get some waveform measurements. The most efficient way have however been to use a thermal camera to measure the hot spots and combine that with simulations to optimize the circuits.

Finally heat and thermal management have been a big challenge. When the power density is increased as dramatically as done in this work, it causes a large power loss in a small area. Even with the same or slightly higher efficiencies than traditional converters, this causes hot spots which has to be dealt with to insure reliable operation. Ceramic and aluminium PCBs have been tested to reduce the hot spots, but the ceramic do not improve the thermal proporties enough and the aluminium causes to high parasitic capacitances. Ceramic thermal bridges placed close to the components causing the hot spots and transfering the heat to large copper areas on the PCB, has been the most efficient way to reduce hot spots so far.

Chapter 4

Gate Drive

One of the most challenging parts in a reliable and efficient design of a VHF converter is the gate drive. This is especially the case if high side switches or synchronous rectifiers are used, but even the gate drive for a low side switch can be quite challenging. There are two important choices which need to be made early in the design process, should the gate drive be resonant or hard gating and should it be externally driven or self-oscillating.

The first choice is mainly a matter of power level and frequency. The losses associated with driving a MOSFET with a square wave and a sine wave is given in [32]:

$$P_{Gate,Square} = C_{ISS} \cdot V_G^2 \cdot f_S \tag{4.1}$$

$$P_{Gate,Sine} = 2 \cdot \pi^2 \cdot f_S^2 \cdot C_{ISS}^2 \cdot R_G \cdot V_{G,ac}^2 \tag{4.2}$$

In the same paper a comparison is made between the two drive schemes in a 100 MHz converter. The square wave results in gating losses of 1.17 W and the sine wave in 173 mW. The sine wave is the most efficient with more than 6 times lower losses, but from equation 4.2 it is seen that the loss increase with the frequency squared whereas the square wave increase linearly with the frequency. Hence the square wave will become more efficient at some point. Depending on the wave form of the current through the MOSFET, the square wave might also result in lower conduction losses in the MOSFET as it is fully on for the entire conduction period [151]. For the sine wave the MOSFET is turned on slowly as the sine wave rises, which results in higher conduction losses in the beginning and end of the conduction period [152].

For a low to medium power converter switching in the VHF range, the choice is however relatively simple as hard gating leads to gating losses which are unacceptably high, at least for the semiconductors available today and for low to medium power levels (0-200 W) [32, 153]. Resonant gating is therefore also the most used way to drive VHF converters [154, 155, 156] and A.3.

Hard gating will hence not be considered further in this thesis and the two following sections will describe externally driven and self-oscillating resonant gate drives.

4.1 Externally Driven

Several ways of designing externally driven resonant gate drives can be found in the literature [157, 158]. The most basic example is the gate drive shown in Figure 4.1 [140].

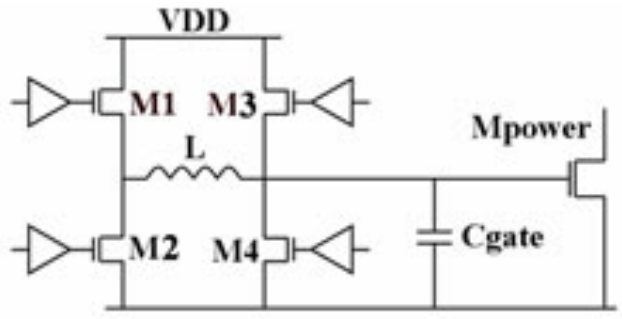


Figure 4.1: Examples of a resonant gate drive [140].

The MOSFET in the power stage, M_{Power}, is turned on by switching on M1 allowing C_{Gate} to be charged through the inductor, L. Once the gate has been charged to the desired voltage M1 is turned off and M3 turned on and the energy stored in the inductor is sent back to the supply through M3 and the body diode of M2. To turn of M_{Power}, M2 is switch on and the energy stored in C_{Gate} is transferred to the inductor. When the capacitor is discharged M2 is turned of and the inductor is discharged through M1 and M4.

Another common way to drive VHF converters, is to use a small inverter to drive the MOSFET, or even a small hard switched inverter to drive a resonant inverter which then drives the main switch as in [103]. This is a quite complex method with many components, but for high power application it can be the most efficient way of driving a large main switch. For the low to medium (0-200 W) power applications of interest in this thesis this would however be an overkill.

A very efficient way to drive the MOSFET is with a single multi resonant circuit [159, 118]. These circuits utilize the same method as shown in [160] and in the class EF_2 inverter explained in the previous section. In this way the gate drive can be made fully resonant, but achieve a trapezoidal waveform instead of a sine wave at the gate. In this way the power loss in the gate resistance is minimized as the applied current during the falling and rising edges of the gate voltage is constant [32].

Many other options for driving VHF converters with and without external signal exist [99, 161]. However all of these options add several components to the circuit, require an auxiliary supply and require close control between the timings of external signal and the resonances of the power stage. Self-oscillating circuits do not need this and are therefore considered more suitable for low to medium power application.

4.2 Self-Oscillating

Self-oscillating converters are very attractive for low to mid power applications were size and cost are main concerns. One example of a self-oscillating converter is described in [162, 115] and the schematic of the inverter is shown in Figure 4.2. In this way a complete converter can be designed with very few components besides the components in the actual power stage. This minimizes the cost and size and removes the losses, which would normally exist in the auxiliary circuits and the supply for this. Further the power stage and gate drive are linked closely together and a change in the power stage due to component tolerances will hence also affect the gate drive, making it less sensitive to component tolerances than an externally driven.

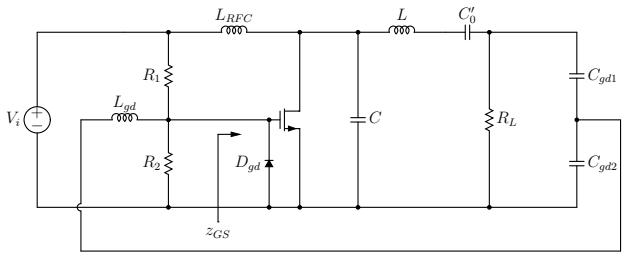


Figure 4.2: Example of a self-oscillating VHF inverter [115].

For externally driven inverters a small inverter is some times used as a resonant gate drive for a larger inverter [103]. In the same way [155] utilizes one inverter to drive another, but the second inverter is also used to drive the first inverter. In this way two equal inverters are used to drive each other and an interleaved operation and power sharing of the two inverters is achieved. This is particularly interesting for applications, where it is neccesary to parallel multiple converters to handle the power.

The gate drive presented in [163] and A.12 was invented just prior to the start of this thesis. It has hence been investigated thoroughly in the beginning of the project and been found to be superior for applications were size and cost are the main concerns. The new resonant gate drive is solely constituted by passive components around the main semiconductor. This leads to a robust and very simple and low cost gate drive.

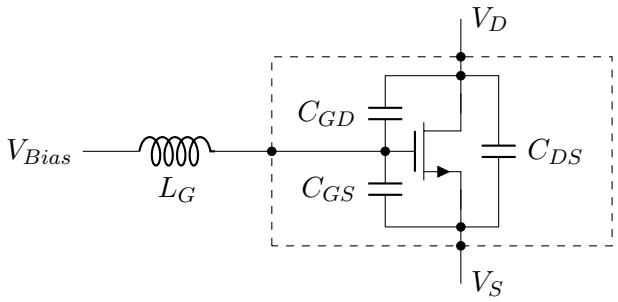


Figure 4.3: Schematic of the basic self-oscillating gate drive. The gate resistance and the body diode has been left out for simplicity.

The simplest implementation of the gate drive is shown in Figure 4.3, the only component added is an inductor at the gate of the semiconductor and a bias voltage. If V_D is seen as input and V_G as output, the inductor and the parasitic capacitances composes a high pass filter with a capacitive load.

If this high pass filter is designed to have a gain, $G = V_{GS,pp}/V_{DS,pp}$, and has a phase shift close to 180 ° at the resonance frequency of the power stage, it will create a sine wave at the gate with a peak to peak voltage swing of $V_{GS,pp}$ and a DC offset equal to V_{Bias}.

This DC offset can be used to control the switching frequency and the duty cycle of the power stage and thereby to regulate the output power. In some situations the parasitic capacitances of the MOSFET will lead to too high or too low gain at the desired frequency and additional capacitors, C_{GDext} and C_{GSext}, can be added to adjust this gain.

Most resonant circuits behave as voltage controlled current sources in open-loop situations; hence the output power increases with the input voltage. As the amplitude of the gate signal is a fixed ratio of the input voltage, a change in input voltage will lead to a change in amplitude of the gate signal. Hence the gate signal will be small at low input voltages, giving low gating losses at low power levels, and be large at high power, levels leading to lower conduction losses in the MOSFET.

In order to improve the turn on speed of the MOSFET, and thereby lower the drain to source resistance, higher order harmonics can be added to the fundamental sine wave leading to a more trapezoidal gate signal. This can be achieved by adding small LC circuits between the gate and drain or source of the MOSFET (see Figure 4.4). LC circuits connected to the drain will cause the higher harmonics to be in phase with V_{DS} and LCs circuit connected to the source will cause the harmonics to be out of phase with V_{DS} (see Figure 4.5).

The number of harmonics to include in a given design will depend on several parameters as price, complexity, efficiency etc. Adding higher order harmonics will in general increase the performance of the converter, but it is important to consider which harmonics to include and the magnitude of those harmonics compared to the fundamental. Figure 4.6 shows the fundamental and the 3rd and 5th harmonics in and out of phase with the drain signal. It is clear that it is desirable to have the fundamental out of phase with the drain signal, but for the 3rd and 5th harmonic it depends on the duty cycle and the current waveform. From the figure it can be seen that it is desirable to have the 3rd harmonic out of phase for a duty cycle of 50%, but for a duty cycle of 25% it has to be in phase and will only add to the center part of the conducting period where the current usually is the smallest [102, 164]. The gate signals that can be achieved by adding harmonics are shown in Figure 4.7.

As the resonant gate drive is only relying on the resonance of the power stage and is floating between the drain and source of the MOSFET, it can be used in all resonant circuits. It can for instance be used in the class E inverter [110, 112], a class EF_2 (ϕ_2) inverter [117, 103], a resonant SEPIC [118, 119], a resonant boost converter [121, 120] or a class DE inverter (including high side gate drive) [165, 108], but it can also be used for synchronous rectification and bidirectional power flow.

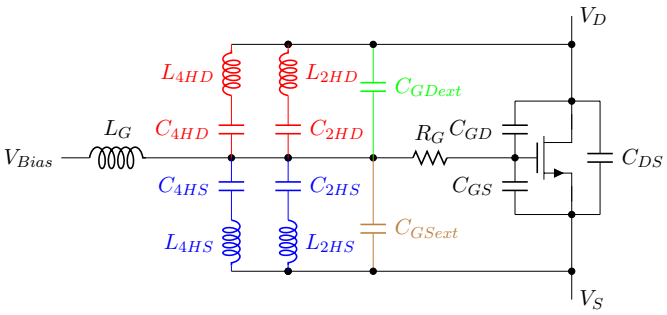


Figure 4.4: Schematic of the self-oscillating gate drive with the 2nd and 4th harmonic to source and drain.

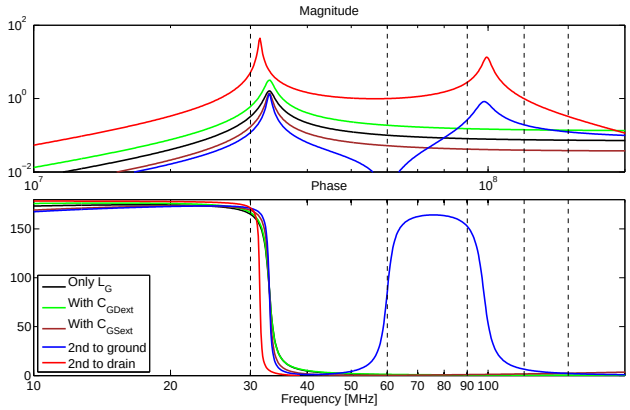


Figure 4.5: Examples of transfer functions from drain-source to gate-source for implementations of the resonant gate drive with added capacitance or 2nd harmonic LC filter.

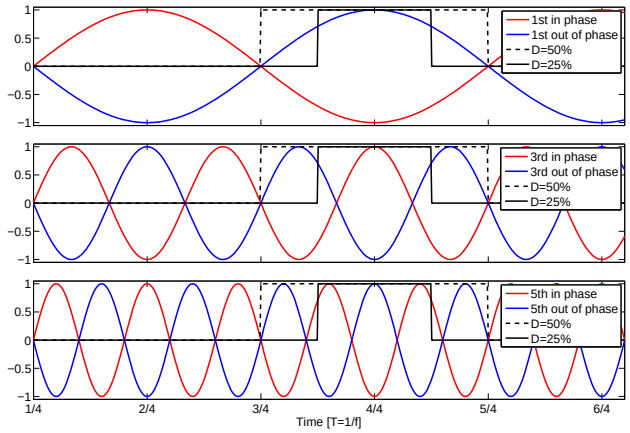


Figure 4.6: The 1st, 3rd and 5th harmonics in and out of phase with the drain signal.

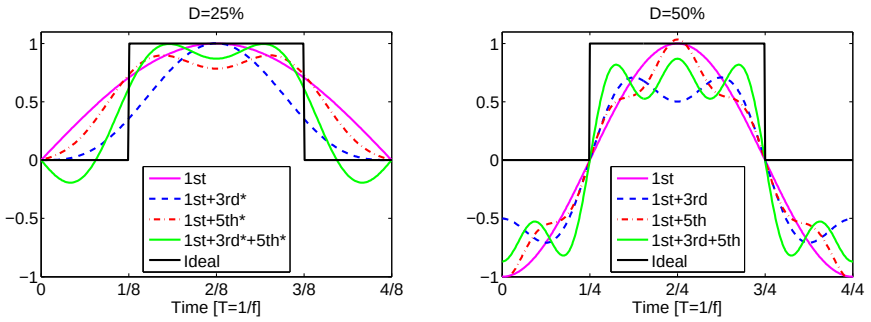


Figure 4.7: Gate signals with 1st, 3rd and 5th order harmonics for 25% and 50% duty cycle (*=signal in phase with V_{DS}).

A specific design example of the gate drive is given in A.10.

4.2.1 Synchronous Rectification

The self-oscillating gate drive is very well suited for synchronous rectification, as it does not require a control signal to control the phase between the two gate signals. The two gate signals will automatically oscillate out of phase with the drain-source voltage of the MOSFET they are controlling, hence the gate drive on the inverter side will act as a master drive and the rectifier drive act as a slave drive following the frequency set by the master drive. This principle automatically takes component tolerances and temperature variations of critical design parameters into account. If used in an isolated converter this will further more benefit from not having a control signal and hence no need for communication across the isolation barrier. Figure 4.8 shows how a dc/dc converter with synchronous rectification can be made with this gate drive. As it can be seen the converter is completely symmetric across the resonant tank, C_R and L_R, hence operation in both directions is possible allowing for bidirectional power flow.

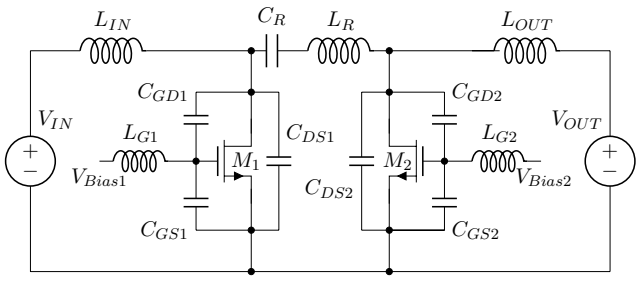


Figure 4.8: Schematic of a class E dc/dc converter with synchronous rectification.

Several resonant converters with bidirectional power flow have been published previously, e.g. a bidirectional full-bridge class-E converter in [166] and LLC converters in [167, 168, 169]. The use of synchronous rectification in VHF converters is however a bigger challenge due to the timing of the gate signals. The gate signals amplitude and duty cycle needs to be tightly controlled to ensure ZVS on the MOSFET in the rectifier and to keep the gate losses to a minimum.

This gate drive has the advantage of being controlled by the drain voltage, hence the oscillation will start when the inverter starts sending power through the resonant tank and the voltage across the MOSFET in the rectifier rises.

A specific design examples of the gate drive used for synchronous rectification and bidirectional power flow is given in A.11. This was proof of principle showing that the gate drive can indeed be used for synchronous rectification. Further it was found that the converter had almost exactly the same open loop gain in both directions when used for bidirectional power flow.

4.2.2 High Side Gate Drive

The biggest advantage of this gate drive is that it can be used to drive high side switches, hence enable the use of half and full bridge topologies like the DE inverter shown in Figure 3.2. These topologies offer several important advantages over the single switch topologies and the only drawback is the need for a high side gate drive. This gate drive is the first gate drive presented suited for high side gate drive at VHF. This hence enables a whole new set of topologies for VHF SMPS, which has major advantages over the single switch topologies.

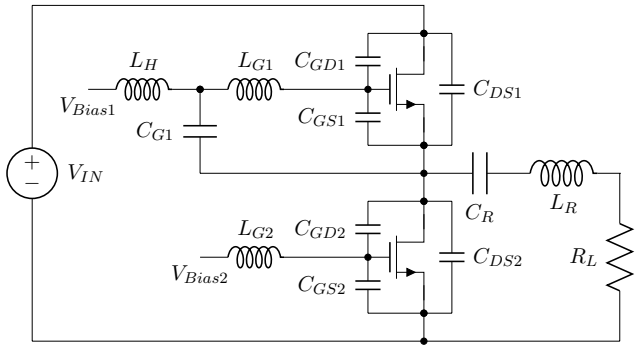


Figure 4.9: Schematic of the class DE inverter with self oscillating gate drive.

An implementation of the self-oscillating resonant gate drive in a half bridge is shown in Figure 4.9. Here the two MOSFETs have equally sized inductors at the gates, the only difference is that the other node of L_{G1} is connected to V_{bias} through L_H and to the switch node through C_{G1}. In this way the voltage at this node will follow the switch node but have a dc offset set by V_{Bias1}. As the phase of gate signals of the MOSFETs are directly coupled to drain source voltages, which are 180 ° shifted, the gate signals will automatically be phase shifted and shoot through is avoided.

In A.6 the worlds first half bridge VHF converter working with more than a few volts at the converters input is presented. The prototype is shown in Figure 4.12 and some of the measured waveforms are shown in Figure 4.11. The circuits is highly affected by the measurements (the capacitance added by the probe) and the efficiency drops significantly during the measurements. The efficiency and output power of the converter is shown as function of input voltage in Figure 4.12.

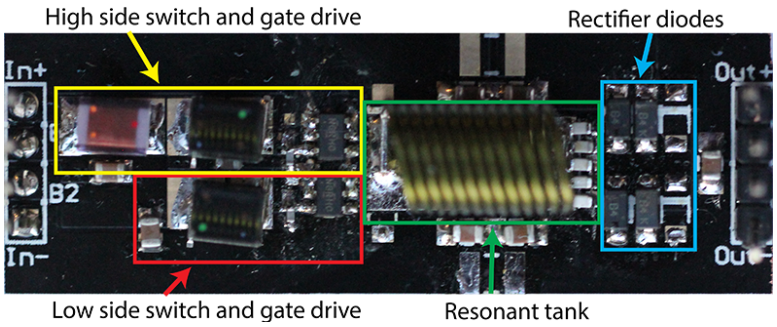


Figure 4.10: Picture of the worlds first descrite VHF class DE converter.

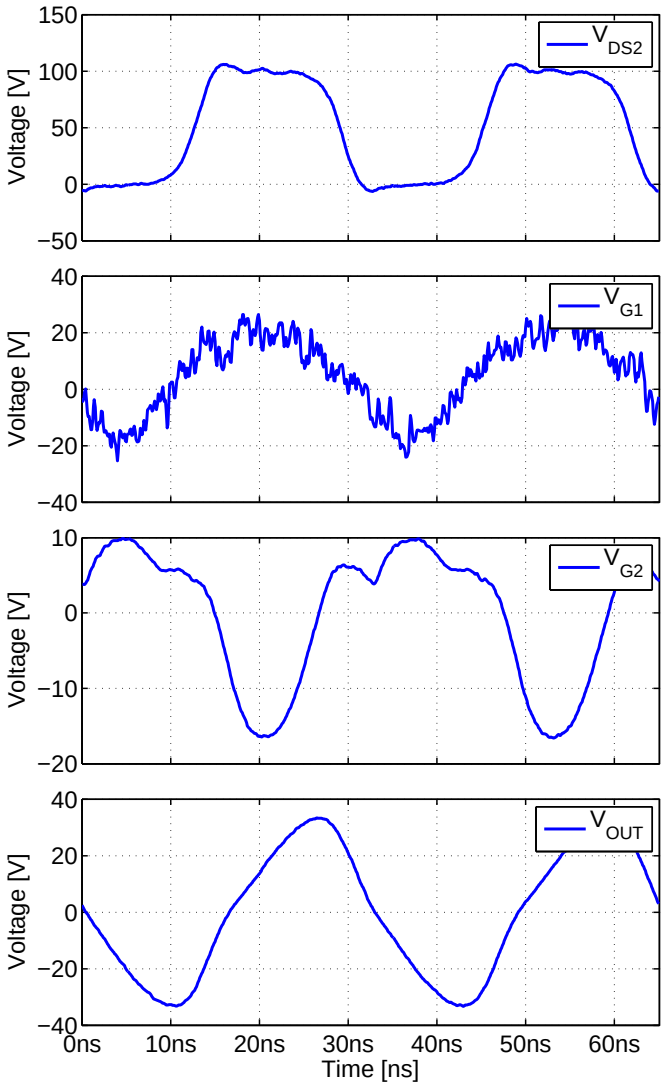


Figure 4.11: Measured waveforms on the class DE converter.

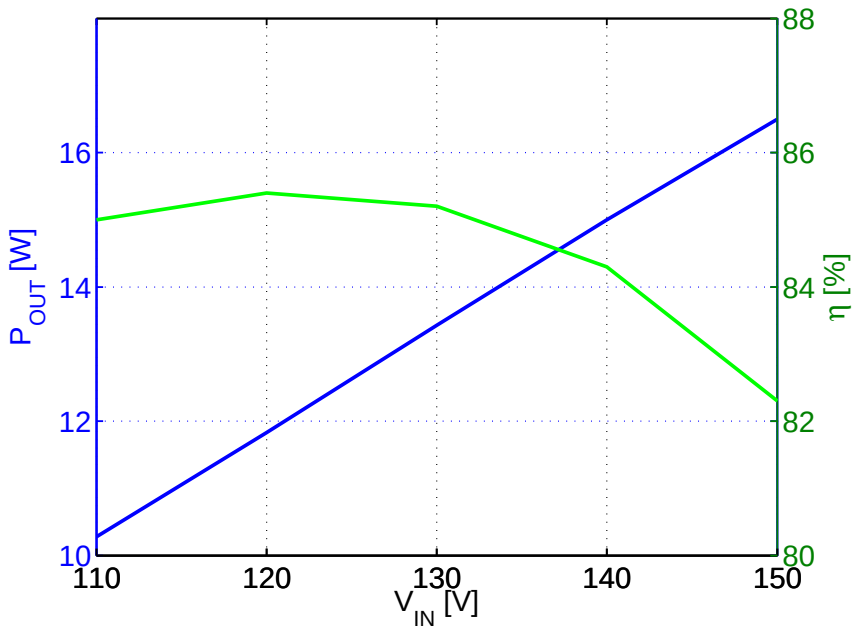


Figure 4.12: Efficiency and output power as function of input voltage for a VHF class DE converter.

Chapter 5

PCB Embedded Magnetics

Implementing the magnetics as part of the PCB is widely used in traditional converters [170, 171]. For VHF converters, the selection of suited magnetic materials is limited, due to extensive core losses in most materials at these frequencies, and air core inductors are therefore used [172]. In this chapter spiral, solenoid and toroid structures will be analyzed and compared for use as PCB embedded inductors and transformers in converters operating at VHF.

5.1 Inductors

One of the challenges to achieve high efficiency at VHF is to design high-Q inductors, as most magnetic materials are limited to operation up to a few megahertz. Even materials, which theoretically can be used with good performance up to 100 MHz, show poor performance in the VHF range [173]. At the high frequencies, the inductance needed is however also lowered significantly and it is hence possible to use relatively small air core inductors. So far, the type of inductor most commonly used are air core solenoids.

Given the small inductance, the inductors can, however, also be designed as Printed Circuit Board (PCB) embedded inductors. Several structures for the design of these inductors exist and many of them have been described several times in previous publications [174, 175, 176]. Spiral inductors are commonly used in Integrated Circuits (ICs) and hence several publications with design guides for these exists [177, 178, 179]. Though discrete air core solenoids are commonly used, solenoids are not as common for embedded inductors. Some publications are however available showing inductors with Q values of up to more than 300 [180, 181]. Toroid inductors are of specific interest due to their natural encapsulation of the field due to the shape of the structure. With no magnetic core to guide the flux, a structure which on its own encapsulates the field is necessary to avoid problems with electromagnetic interference (EMI) [174, 182, 183]. In the following subsections these structures will be investigated individually and then compared.

5.1.1 Spiral

Spiral inductors can be designed in many ways and the shape is often chosen due to limitations in production. Round shapes are some times not possible in IC processes and therefore square or octagonal spirals are often used in ICs [184, 185]. When core materials are used, it is desirable to utilize a shape were the tracks are shaped in a way that ease the design of the core. Racetracks are often used for this as it allows for the use of a straight and simple core shape along the length of the structure [186, 187].

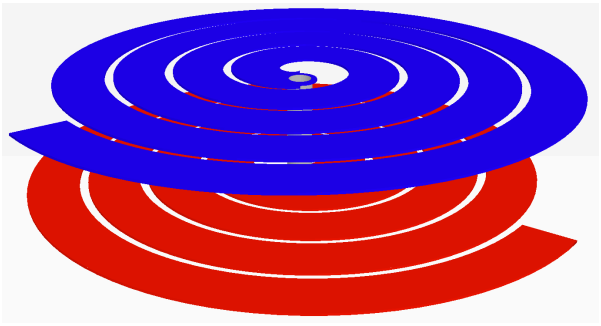


Figure 5.1: A two layer PCB embedded spiral inductor

In this section, air core spirals on a PCB will be investigated, hence no core will be used and circles and curves can easily be made in the production process. Therefore, the spirals are designed as archimedean spirals, i.e., with constant trace width and a constant distance between the traces, see Figure 5.1. The length of the trace in an archimedean spiral can be calculated according to equation 5.1 with the assumption that $1 + 2 + 3 + ... + N = N \cdot \frac{N+1}{2}$

$$l_{TRACE} = \pi \cdot N_{TURNS} \frac{D + d}{2} = \pi \frac{D^2 - d^2}{4 \cdot T_{TRACE}} \tag{5.1}$$

Here N_{TURNS} is the number of turns, T_{TRACE} is the thickness of the copper and D and d is the outer and inner diameter, respectively. MATLAB has been used to design the inductors; here the build in MATLAB function pdist2 can be used to get a more accurate length when the coordinates for the trace are known.

Now that trace length is known, the DC resistance is simply calculated from equation 5.2. If a two layer spiral is made, the resistance of course has to be doubled and the resistance of the via has to be added. The ac resistance, caused by the skin effect, of a planar inductor can, according to [188], be approximated by equation 5.3.

$$R_{DC} = \frac{\rho \cdot l_{TRACE}}{W_{TRACE} \cdot T_{TRACE}} \tag{5.2}$$

$$R_{AC} = \frac{\rho \cdot l_{TRACE}}{W_{TRACE} \cdot \delta(1 - e^{T_{TRACE}/\delta})} \tag{5.3}$$

Here ρ is the electrical resistivity of copper, W_{TRACE} is the width of a trace and δ is the skin depth.

The inductance of a spiral can be calculated by equation 5.4 [189]. Here c_1 and c_2 are constants of 2.46 and 0.20, respectively, and p is a fill ratio defined as $p = \frac{D-d}{D+d}$.

$$L = \frac{\mu \cdot N_{TURNS}^2 \frac{D+d}{2}}{2} \left(ln\left(\frac{c_1}{p}\right) + c_2 \cdot p^2 \right) \tag{5.4}$$

5.1.2 Solenoid

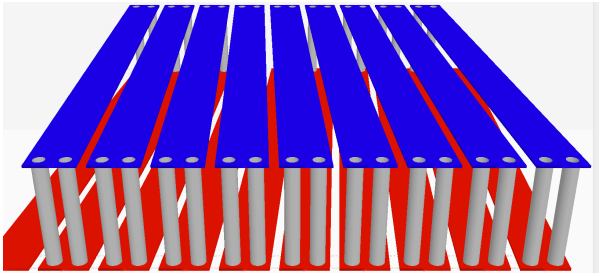


Figure 5.2: A PCB embedded solenoid inductor

In order to calculate the resistance of a solenoid, the structure is split in two; the vias and the traces. The dc resistance of a single via and a single trace, can now be calculated according to equation 5.5 and 5.6, respectively [113].

$$R_{DC,VIA} = \frac{\rho \cdot T_{PCB}}{A_{VIA}} = \frac{\rho \cdot T_{PCB}}{\pi \cdot T_{VIA}(D_{VIA} - T_{VIA})} \tag{5.5}$$

$$R_{DC,TRACE} = \frac{\rho \cdot W_L}{W_{TRACE} \cdot T_{TRACE}} \tag{5.6}$$

Here T_{PCB} is the thickness of the PCB, A_{VIA} is the area of a cross section of a via, D_{VIA} is the via diameter, T_{VIA} is the thickness of the copper in a via and W_L is the width of the inductor.

The total DC resistance can then be calculated as the sum of all the vias and traces. Using multiple vias in parallel for each turn will lower the total resistance. If this is done the total resistance can be calculated according to equation 5.7. Here N_{VIAS} is the number of parallel vias in a single turn.

$$R_{DC} = 2 \cdot N_{TURNS} \left(\frac{R_{DC,VIA}}{N_{VIAS}} + R_{DC,TRACE} \right) \tag{5.7}$$

The AC resistance is calculated as a first order approximation of the skin effect, hence neglecting the proximity effect. This will not give exact results, but it ease the comparison of the three structures and is sufficient for evaluation of pros and cons of each structure.

It is assumed that the ac current will run along the inner edge of the solenoid, hence along the inner edge of the traces and the inner edge of the inner half of the vias. This assumption has been verified through finite element (FEM) simulations in COMSOL in A.14. Using this assumption and the skin depth, the ac resistance is calculated according to equation 5.8.

$$R_{AC} = 2 \cdot N_{TURNS} \left(\frac{R_{AC,VIA}}{N_{VIAS}} + R_{AC,TRACE} \right) \tag{5.8}$$

Where:

$$R_{AC,VIA} = \frac{\rho \cdot T_{PCB}}{A_{VIA}} = \frac{2 \cdot \rho \cdot T_{PCB}}{\pi \cdot \delta(D_{VIA} - \delta)}$$

$$R_{AC,TRACE} = \frac{\rho \cdot W_L}{W_{TRACE} \cdot \delta}$$

The inductance of the solenoid can be calculated according to Niwas formula [190]. In equation 5.9, L_L is the length of the inductor and g is the square of the hypotenuse of a cross section of the inductor given by; $g^2 = W_L^2 + T_{PCB}^2$

$$\begin{aligned}
L = 8e^{-9} \cdot N_{TURNS}^2 \frac{W_L \cdot T_{PCB}}{L_L} \Bigg[& \frac{1}{2}\frac{L_L}{T_{PCB}} sinh^{-1}\frac{T_{PCB}}{L_L} \\
& + \frac{1}{2}\frac{L_L}{W_L} sinh^{-1}\frac{T_{PCB}}{L_L} \\
& - \frac{1}{2}\left(1 - \frac{T_{PCB}^2}{L_L^2}\right)\frac{L_L}{T_{PCB}} sinh^{-1}\frac{W_L}{L_L\sqrt{1 + T_{PCB}^2/L_L^2}} \\
& - \frac{1}{2}\left(1 - \frac{W_L^2}{L_L^2}\right)\frac{L_L}{W_L} sinh^{-1}\frac{T_{PCB}}{L_L\sqrt{1 + W_L^2/L_L^2}} \\
& - \frac{1}{2}\frac{T_{PCB}}{L_L} sinh^{-1}\frac{W_L}{T_{PCB}} - \frac{1}{2}\frac{W_L}{L_L} sinh^{-1}\frac{T_{PCB}}{W_L} \\
& + \frac{\pi}{2} - tan^{-1}\frac{W_L \cdot T_{PCB}}{L_L^2\sqrt{1 + g^2/L_L^2}} \\
& + \frac{1}{3}\frac{L_L^2}{W_L \cdot T_{PCB}}\sqrt{1 + \frac{g^2}{L_L^2}}\left(1 - \frac{1}{2}\frac{g^2}{L_L^2}\right) + \frac{1}{3}\frac{L_L^2}{W_L \cdot T_{PCB}} \\
& - \frac{1}{3}\frac{L_L^2}{W_L \cdot T_{PCB}}\sqrt{1 + \frac{W_L^2}{L_L^2}}\left(1 - \frac{1}{2}\frac{W_L^2}{L_L^2}\right) \\
& - \frac{1}{3}\frac{L_L^2}{W_L \cdot T_{PCB}}\sqrt{1 + \frac{T_{PCB}^2}{L_L^2}}\left(1 - \frac{1}{2}\frac{T_{PCB}^2}{L_L^2}\right) \\
& + \frac{1}{6}\frac{L_L^2}{W_L \cdot T_{PCB}}\left(\frac{g^2 - W_L^2 - T_{PCB}^2}{L_L^2}\right)\Bigg]
\end{aligned} \tag{5.9}$$

5.1.3 Toroid

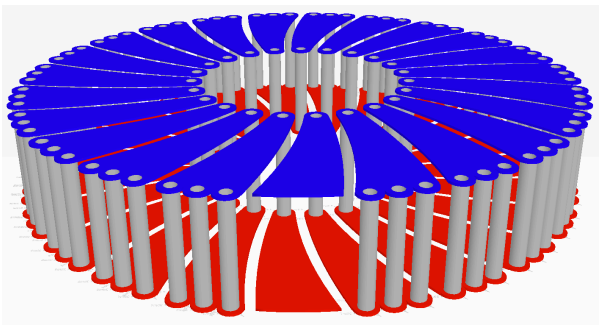


Figure 5.3: A two layer PCB embedded toroidal inductor

A toroid is a solenoid bent in a circle; hence the same procedure and some of the assumption can be used again. It is thus assumed that the current run along the inner edges and the toroid is split into slabs and vias to get the resistance. The dc resistance of a slab is determined by integration from the inner radius to the outer radius [182].

$$R_{DC,SLAB} = \int_{r_I}^{r_O} \frac{\rho}{T_{TRACE}\left(\frac{2\cdot\pi\cdot r}{N_{TURNS}} - C_{TRACE}\right)}$$
$$= \frac{\rho \cdot N_{TURNS}}{2 \cdot \pi \cdot T_{TRACE}} ln\left(\frac{2 \cdot \pi \cdot r_O - C_{TRACE} \cdot N_{TURNS}}{2 \cdot \pi \cdot r_I - C_{TRACE} \cdot N_{TURNS}}\right) \tag{5.10}$$

Here C_{TRACE} is the clearance between two slabs and r_I and r_O are the inner and outer radius, respectively. As for the solenoid a first order approximation of the skin effect is used for the ac resistance, hence this becomes:

$$R_{AC,SLAB} = \int_{r_I}^{r_O} \frac{\rho}{\delta\left(\frac{2\cdot\pi\cdot r}{N_{TURNS}} - C_{TRACE}\right)}$$
$$= \frac{\rho \cdot N_{TURNS}}{2 \cdot \pi \cdot \delta} ln\left(\frac{2 \cdot \pi \cdot r_O - C_{TRACE} \cdot N_{TURNS}}{2 \cdot \pi \cdot r_I - C_{TRACE} \cdot N_{TURNS}}\right) \tag{5.11}$$

The resistance of the vias are the same as for the solenoid and the total resistance becomes:

$$R_{DC} = N_{TURNS}\left(2 \cdot R_{DC,SLAB} + \frac{R_{DC,VIA}}{N_{INNER}} + \frac{R_{DC,VIA}}{N_{OUTER}}\right) \tag{5.12}$$

$$R_{AC} = N_{TURNS}\left(2 \cdot R_{AC,SLAB} + \frac{R_{AC,VIA}}{N_{INNER}} + \frac{R_{AC,VIA}}{N_{OUTER}}\right) \tag{5.13}$$

Here N_{INNER} and N_{OUTER} are the number of inner and outer vias, respectively. The inductance of a toroid is derived in [183] and repeated in equation 5.14.

$$L = \frac{\mu \cdot N_{TURNS}^2 \cdot T_{PCB}}{2 \cdot \pi} ln\left(\frac{r_O}{r_I}\right) ... + \frac{r_O + r_I}{2}\mu\left[ln\left(8\frac{r_O + r_I}{r_O - r_I}\right) - 2\right] \tag{5.14}$$

5.1.4 Design and Optimization

In order to design and produce the inductors, a MATLAB program with a GUI has been designed, see Figure 5.4. The program takes the production parameters and the desired inductance and size as input and uses a genetic algorithm and formulas from the previous subsections to find parameters for the initial design.

Then COMSOL is used to investigate the current distribution and magnetic fields and to verify the inductance and resistance. Once the design has been verified in COMSOL, a PCB file is generated directly from the same interface.

The optimization routine is used to find the best inductor, within a given area. Best is defined as the required inductance, with the highest Q factor and with the

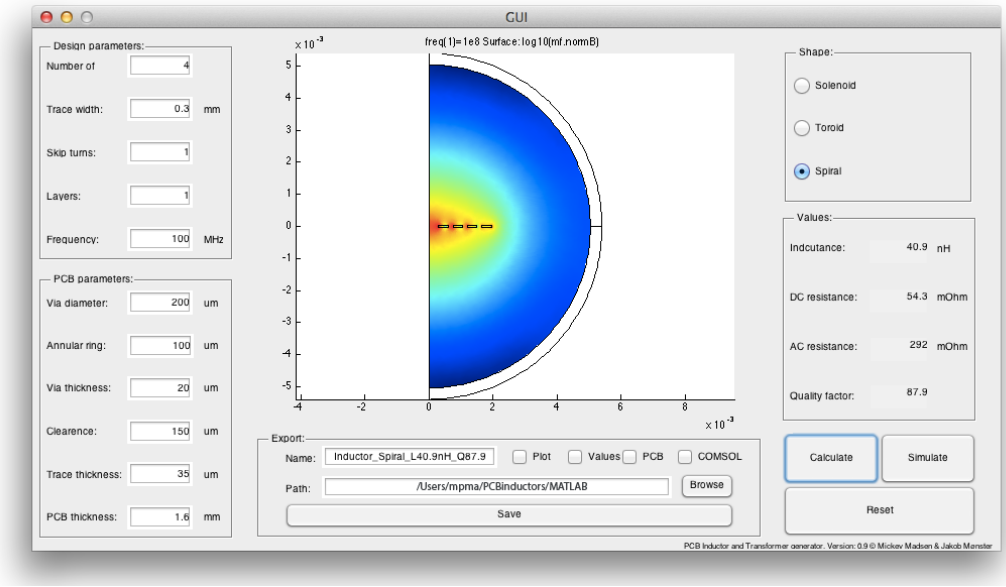


Figure 5.4: MATLAB GUI for design and optimization of PCB embedded inductors.

lowest area, in that preferred order. The optimization routine is based on a genetic algorithm already implemented in MATLAB and has a maximum area set by the user as a boundary condition.

The inductor should have the highest possible Q factor and the desired inductance. This is achieved by having a cost function that the genetic algorithm minimizes. The genetic algorithm takes any number of inputs, with possibility to define the variable as an integer. Each variable is setup so a closer value to the desired will lower the cost function, and each variable is weighted according to the importance of that specific parameter. The cost function used is:

$$Cost = a \cdot \left(\frac{L}{L_{spec}} - 1 \right) + b \cdot \frac{1}{Q} + c \cdot A \tag{5.15}$$

where L_{spec} is the specified inductance and A is the area of the inductor. The weight factors used are shown in Table 5.1.

Table 5.1: The weight factors used for the cost function.

a	b	c
100	10.000	1

To verify that the calculations used to derive the optimum structure, and evaluate that the formulas in overall, are usable the MATLAB program interfaces to COMSOL. The structure is then simulated in COMSOL which returns the resistance and inductance as results, this is described further in A.14. Also more than 50 different test structures of each type of inductor has been made and measured, see Figure 5.5, these are described further in A.13.

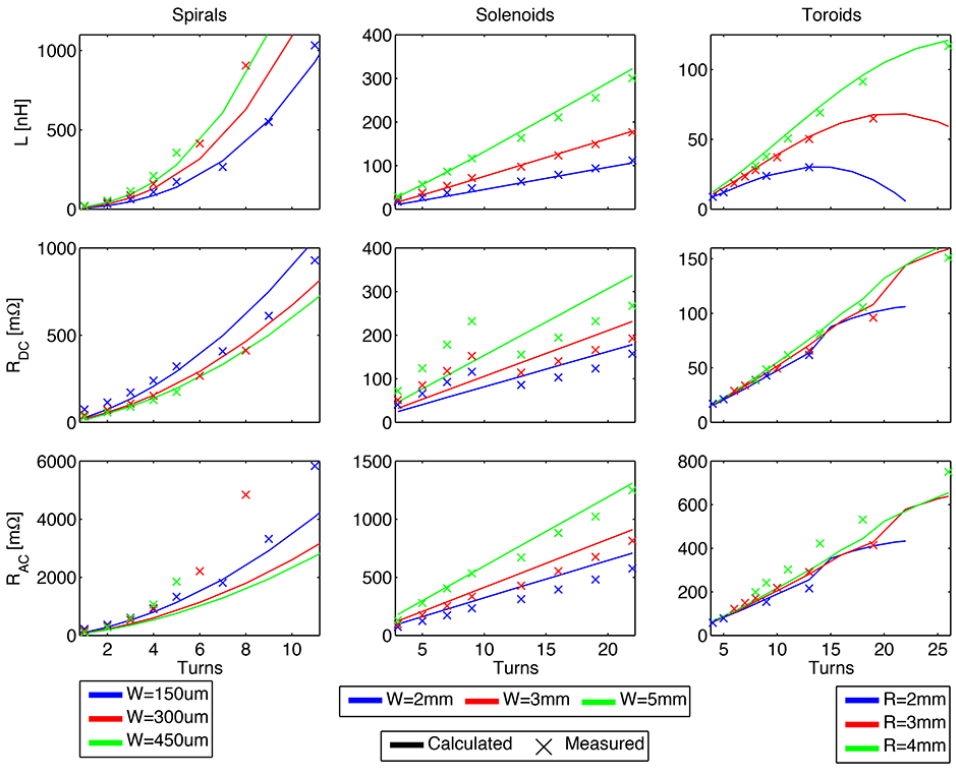


Figure 5.5: Measurements of the inductance and DC and AC resistance of some of the experimental prototypes.

5.1.5 Comparison

An example of the calculated impedances of the three structures optimized for 82 nH in 8x8 mm is given in Table 5.2. The table shows that the solenoid has almost twice the AC resistance of the spiral and 20% more than the toroid. It should however be noted that a quadratic solenoid is far from optimal and higher Q could be obtained, if a more narrow solenoid was designed. A 6mm wide solenoid with 8 turns can have 86nH and a Q factor of 92 in $48mm^2$.

Table 5.2: Parameters for three inductors with approx. 82 nH inductance in 8x8mm

Structure	Spiral	Solenoid	Toroid
N_{TURNS}	3.2	6	16
L	81 nH	81 nH	85 nH
R_{DC}	65 mΩ	72 mΩ	100 mΩ
R_{AC} @ 50 MHz	253 mΩ	495 mΩ	392 mΩ
Q @ 50 MHz	100	51	68

Figure 5.6 shows a frequency sweep of the three structures, both of prototypes with a low number of turns and of ones with a high number of turns. The inductance is very close to constant across the entire frequency range, except for the big spiral

which is close to the resonance at the higher frequencies. From Figure 5.6 it can be seen that the resistance of the spiral, starts to increase due to the skin effect much earlier than the two other structures. This is because the resistance of the spiral is almost entirely due to the resistance of the trace, here the skin effect starts at 1-5 MHz (δ = 65 - 30 μm). The resistance of the solenoid and the toroid only start to increase at approximately 10 MHz where the skin depth equals the thickness of the vias (20 μm). At 50 MHz the skin depth is approximately 10 μm and all the structures are clearly affected by the skin depth.

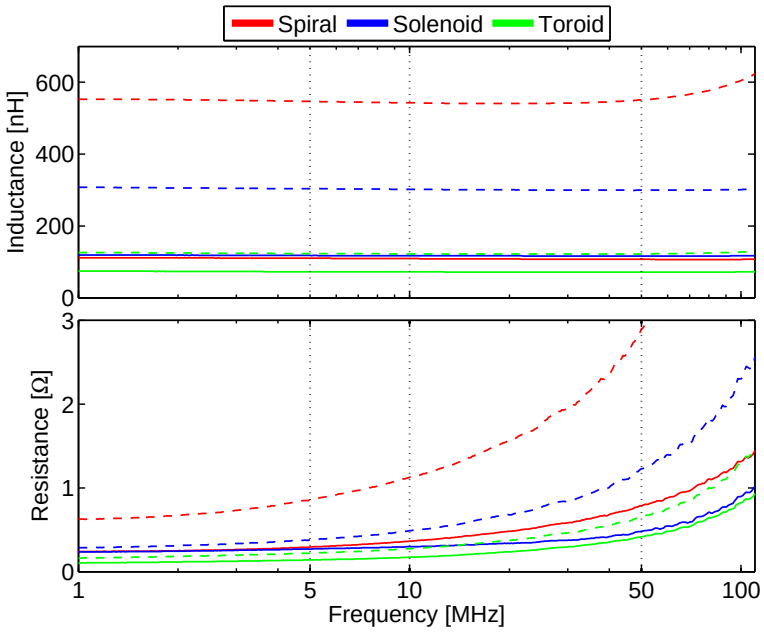


Figure 5.6: Inductance and series resistance of prototypes with a low number of turns (solid) and high number of turns (dashed).

From the formulas for the inductance of each of the three structures, it can be seen that each of the three structures has a limited number of parameters, which can be adjusted if the PCB parameters are given. The number of turns is the only common design parameter for the three structures.

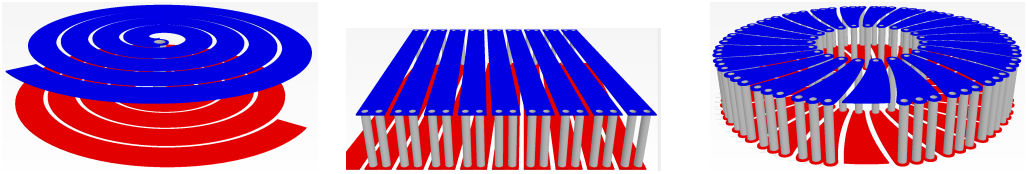
The only parameter left for the spiral, is the width of the trace (and the number of layers or inductors in series).

For the solenoid both the length and width can be adjusted and though it is generally best to avoid the extremes, i.e. long and narrow or short and wide, this gives a larger amount of design flexibility.

For the toroid it is possible to adjust both the inner and outer radius. For a small structure, the minimum inner radius will however be limited by the size of a via (incl. annular ring) and the number of turns. If the inner radius is increased, it is possible to ad more vias in parallel to reduce the resistance. The core of the inductor is then decreased and more turns are needed to keep the same inductance, thus the gain of doing so is limited.

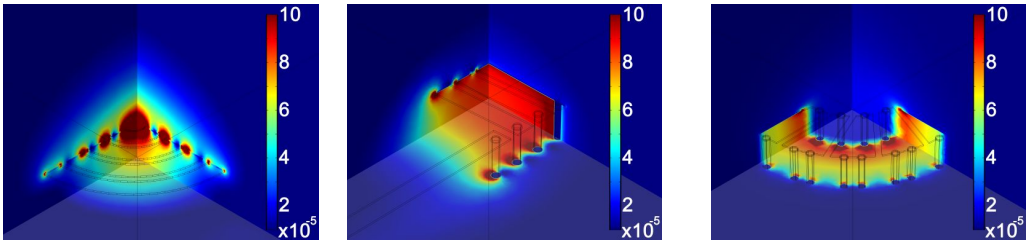
Both spirals and solenoids have strong external magnetics fields, see Figure 5.7a-5.10a and 5.7b-5.10b, respectively. This make them likely to cause Electromagnetic

Interference (EMI) problems, either by direct radiation or by coupling to nearby metallic structures such as cables and other circuit boards. The fields have been described for spirals in [174] and for solenoids and toroids in [175]. The external field from the toroid is much weaker than for the two other structures, see Figure 5.7c-5.10c.



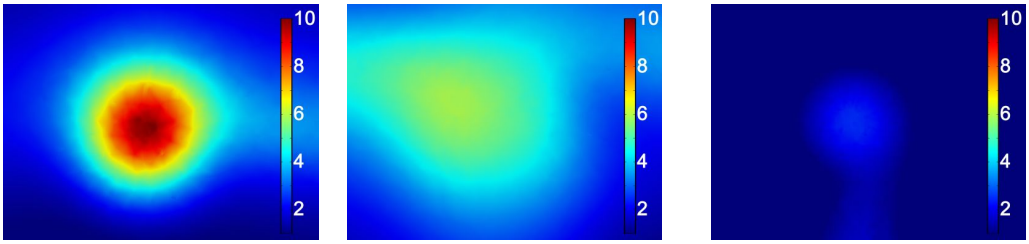
(a) Spiral **(b)** Solenoid **(c)** Toroid

Figure 5.7: Three types of PCB embedded inductors.



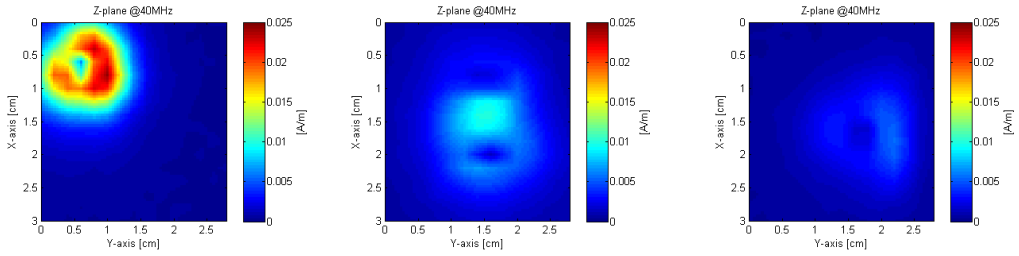
(a) Spiral **(b)** Solenoid **(c)** Toroid

Figure 5.8: Finite element simulations of the magnetic flux density (B-field [T]) inside the three types of PCB embedded inductors.



(a) Spiral **(b)** Solenoid **(c)** Toroid

Figure 5.9: Finite element simulations of the magnetic field (H-field [A/m]) 2 mm above the three types of PCB embedded inductors.



(a) Spiral **(b)** Solenoid **(c)** Toroid

Figure 5.10: Near-field scans of the field strength from the three types of PCB embedded inductors (z component not included as in simulation).

Another very important parameter is the flexibility or design freedom of the inductor types, both when scaling the inductor and laying out the complete PCB.

The spiral is by far superior in this perspective. It can be made in a single layer, the width of the trace can be scaled to get the desired relation between size and Q factor and finally it does not need and integer number of turns, which makes it possible to get the terminals placed in a way that fits into the rest of the circuit.

The solenoid also has some benefits over the two other structures. It has a rectangular shape and it has both the terminals on the same layer. The rectangular shape is much easier to align together with other rectangular components on a board, which most often also is rectangular. The ability to adjust the width and length and thereby design it to fit perfectly into the circuit is also very convenient.

The toroid is clearly the least flexible as the connectors are fixed to be right above each other. Furthermore it is the structure that can achieve the lowest inductance per area and both of the two other structures can be design with lower DC and AC resistances for a given inductance in the same area. The high resistance is partly caused by the poor fill factor of the vias used on the inner and outer edges of the toroid. A way of handling this and adding a core to the design has been investigated in A.16 and A.15. With the fully PCB embedded structure the only real advantage of the toroid is however the small external field.

Several aspects of the three PCB inductors have now been evaluated and the pros and cons has been summed up in Table 5.3.

Table 5.3: Pros and Cons of the three structures.

Structure	Pros	Cons
Toroid	Smallest external field	Least flexible
		Lowest Q and L pr area
Solenoid	Rectangular shape	Wide external field
	High Q	
Spiral	Highest Q	Strong external field
	Most flexible	
	Single layer	

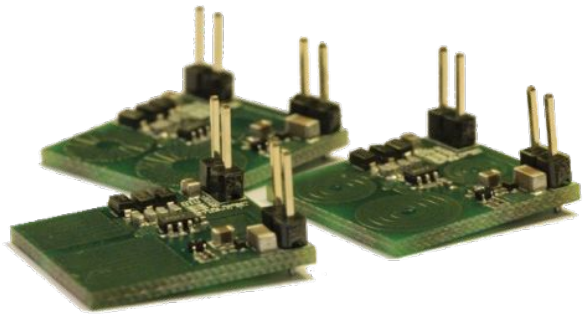


Figure 5.11: Resonant converters with the different structures for PCB embedded inductors.

The three converters in Figure 5.11 have been designed to give and idea of how the complete circuit with PCB embedded inductors will behave. Embedding the inductors in the PCB clearly gives some benefits, i.e. a much lower profile and a higher power density, this is described further and illustrated in a circuit in A.5. However the design still has to be optimized in order to compete with discrete air core solenoids which can have Q factors of more than 200 [129].

The three inductor types have now been compared with regard to resistance, inductance, magnetic field and design flexibility, both theoretically and experimentally.

The results show that there are huge differences in what can be achieved with the different structure and that a single structure cannot be selected as the superior for all applications. The spiral can achieve the highest inductance per area and is the only structure that can be made in a single layer; the solenoid is easy to scale and can be designed to fit perfectly into a complete design and the toroid is by far superior with regard to the external magnetic field.

5.2 Transformers

Galvanic isolation in traditional high-frequency SMPS is usually implemented with an isolation transformer, which utilizes a magnetic core. This approach is not suitable for VHF-SMPS as the core-losses, as previously described, will be significant at VHF [91]. Air-core magnetics with the lack of magnetic core removes the core-losses and the possibility of saturation, making them a suitable solution for VHF operation with the converters low inductance requirements.

Transformers in general exist in a vast number of designs, most focused on versions with a core to guide the flux to achieve a good coupling between the primary and secondary side. Air-core transformers can also be made in many designs, but are for practical purposes limited to structures that in itself will guide the flux through a common winding area, since there is no core to help guiding the flux.

In the following subsections it will be investigated how the three inductor structures can be used to design PCB embedded transformers suited for use at VHF. The spirals and toroids have been investigated thoroughly in previous literature [191, 192] and will therefore only be covered briefly. For the solenoids on the other hand several new ways of designing PCB embedded transformers will be described and investigated.

5.2.1 Spiral

Due to the strong vertical field in the center of the spiral inductors, see Figure 5.9b, a strong coupling between two inductors can be achieved, by placing them vertically aligned on two subsequent layers in a PCB [193, 194]. Figure 5.12 shows a example of a two layer structure, but the structure can easily be scaled two include more layers in a multilayer PCB [195].

As the primary and secondary winding are placed on seperate layers of the PCB, this structure is very well suited in applications were a safety isolation is required.

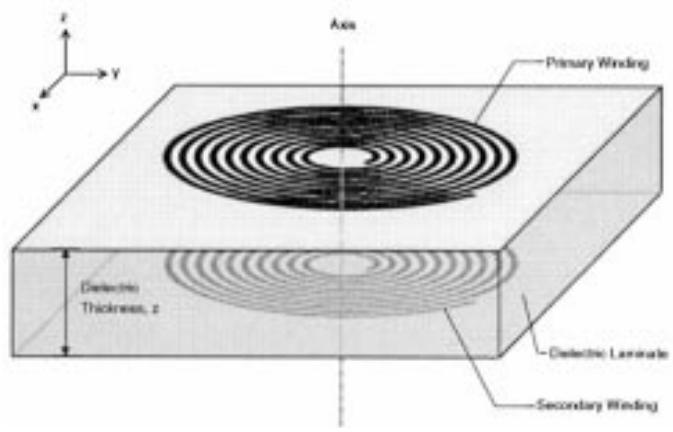


Figure 5.12: Example of a two layer PCB embedded spiral transformer [193].

The structure is however also well suited for signals and can be combined with PCB embedded spiral inductor to get a complete converter with all magnetic components embedded in the PCB [196, 197]. In [198] a 1 kW LLC converter with a power density of 12.2 W/cm^3 and an efficiency of 95.5% is demonstrated, this shows that very high power densities can be achived by embedding the magnetics in the PCB while keeping the efficiency high. Spiral structures, or arrays of these, is also the most commen way to get coupling between two units in a wireless charging system [199, 200].

5.2.2 Toroid

The PCB embedded toroidal transformer was first presented in [172]. The structure is made in a minimum 4 layer PCB were one of the windings is made in the inner layers with burried viases and the other winding is made in the outer layers completely surounding the first winding, see Figure 5.13.

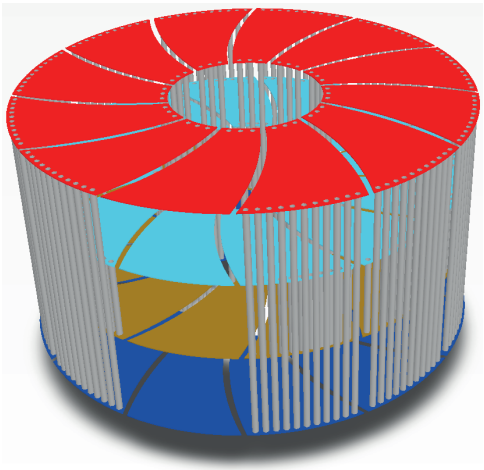


Figure 5.13: Example of a four layer PCB embedded toriodal transformer [172].

The structure were investigated further in [191] were analytic models were derived and verified through FEM simulations and measurements. The coupling which can

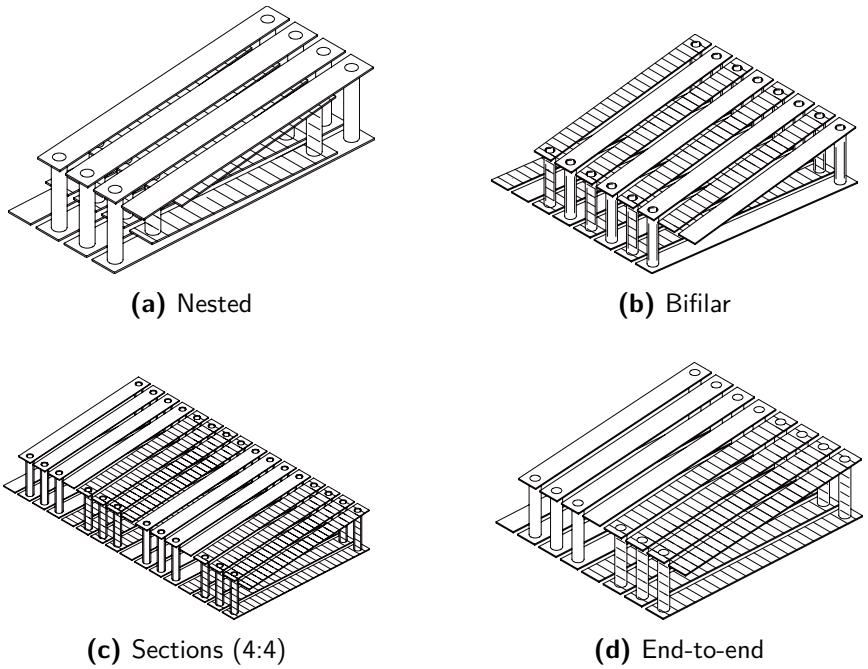
be achieved with this structure is highly dependent on the PCB processes, but coupling in the range 0.4-0.65 has been shown [191, 201]. Higher copuling can be achieved if a core is embedded in the PCB and utilized to guide the flux inside the center structure [202]. This is however a complex and costly process and the concept in A.15 and A.16 seems more apealing from a process/cost point of view, if a core is to be used.

A coupling of 0.65 is fully acceptable for resonant converters as the leakage inductance can be utilized in the resonant tank. So with the core materials available today and the complexity involved in embedding the core, the air core version is the most attractive for VHF converters. The structure was tested in a converter in [203] were the isolation voltage was also tested and shown to comply with the required safety standards.

5.2.3 Solenoid

The PCB embedded rectangular air-core solenoid transformer can be designed in different configurations, but only the two main configurations will be investigated.

The solenoid transformer can be made by one solenoid structure nested inside another slightly larger solenoid structure, giving the transformer a rectangular cross section as seen in Figure 5.14a. This requires minimum a four layer PCB with buried vias. The second configuration is two or more windings in an interleaved pattern on the same layers. The interleaved configurations ranges from the bifilar configuration to the end-to-end configuration as seen in Figure 5.14b, 5.14c and 5.14d. The interleaved configurations can be implemented in a two layer PCB without buried vias.



(a) Nested **(b)** Bifilar

(c) Sections (4:4) **(d)** End-to-end

Figure 5.14: Different winding configurations of rectangular PCB embedded air-core solenoid transformers

The inductive model of a transformer can be defined as a two-port passive device and is described by the inductance matrix in equation 5.16 [98]. The inductance matrix consists of the self-inductance for each winding, L_{pp} and L_{ss}, and the mutual inductances, L_{ps} and L_{sp}, which is determined by the flux that flows through the mutual area of the transformer. Note that L_{ps} and L_{sp} are equal since the transformer is a passive device.

$$\begin{bmatrix} v_p(t) \\ v_s(t) \end{bmatrix} = \begin{bmatrix} L_{pp} & L_{ps} \\ L_{sp} & L_{ss} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_p(t) \\ i_s(t) \end{bmatrix} \tag{5.16}$$

The coupling ratio is defined as equation 5.17, and is a ratio of how much flux couples between the primary and secondary windings. In regular transformers wound around a core, the coupling is in the range of $k = 0.99$ for the best [98].

$$k = \frac{L_{ps}}{\sqrt{L_{pp}L_{ss}}} \tag{5.17}$$

To find the inductance matrix, an Agilent 4396B was set up as a vector network analyzer and the S-parameters measured. The S-parameter measurements can then be converted to Z-parameters [204] and the inductances calculated by equation 5.18.

$$L = \frac{\Im(Z)}{\omega} \tag{5.18}$$

Prototypes of each of the configurations shown in Figure 5.14 were produced and measured. The resulting inductances are listed in Table 5.4 for comparison. To remove any small measurement noise the values are mean values from 1 MHz to 10 MHz.

Table 5.4: Inductances of different configurations of PCB embedded solenoid transformers.

Nested

Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	67.398	17.616	9.5757	69.8%

Bifilar

Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	42.247	18.945	41.866	45.5%

Sections (2:2)

Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	40.949	10.520	38.814	26.5%

End-to-end

Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	40.999	32.203	39.453	8.0%

The prototypes of the interleaved configurations have coupling factors in the range from 0.08 to 0.45. The more intertwined the primary and secondary side is, the

higher the coupling. The coupling is in general limited by the clearance between the traces on the PCB, leaving the end-to-end configuration with the lowest coupling. The configuration with sections shows better properties and the bifilar configuration is the optimum of the interleaved, with a coupling of 0.45. The nested configuration is superior to all the interleaved configurations, as the coupling for this configuration is 0.7.

Though these coupling factors are lower than what can be achieved with a core, they are still suitable for VHF converters as the leakage inductance can be utilized in the design as part of the resonant tank. The nested configuration has the best performance, but is also the most expensive to produce due to the buried viases. This configuration has been evaluated in a practical design which is described in A.17.

Chapter 6

Control

With a switching frequency in the VHF range, it will be possible to achieve very fast transient responses [121] which are highly demanded, e.g., for envelope tracking [205]. However, in order to fully benefit from this, an efficient and fast control loop has to be implemented. This is a big challenge and while some ways of achieving continuous regulation has been found [206, 207], the best results are still achieved using burst mode (or cell modulation) as in [99, 208, 118]. Due to the high switching frequency, the converter will reach steady state after just a few microseconds, this makes it possible to use an array of small converters and switch them on and off as needed. In this way, each converter is designed to operate with a defined load/output. This makes the design much easier as resonant inverters are generally very load dependent.

Control of these converters is also a challenge due to their resonant behavior and burst mode control has been used to overcome this challenge [99, 209], but it introduces spectral components at the bursting frequency and its harmonics.

Pulse width modulation (PWM) is the most commonly used control scheme for power converters, but if a resonant converter is controlled in this way, ZVS is lost as soon as the duty cycle moves away from one optimum value.

Pulse frequency modulation (PFM) is another option, but it requires a very wide frequency operation range to ensure even a limited controllability of the converter. Combinations of PWM and PFM have shown good results [210], but the control circuit becomes quite complex and still requires a wide frequency operation range.

Outphasing is another control option not as commonly used for VHF converters [211, 212]. Compared to burst mode control it has the advantage of not introducing low frequency harmonics.

Burst mode and outphasing control will be investigated in the following sections.

6.1 Burst Mode

So far the most commonly used control method for VHF converters has been burst mode control (also called cell modulation, on-off or bang-bang control) [103, 134, 213]. Here the entire converter is switched on and off in order to control the output. The benefit of controlling the converter in this way is that the converter will either be on and working in its optimal operating point or off with only small standby losses. The result is a wide control range with an almost flat efficiency curve [103, 134]. Further, the converter can be optimized for high peak efficiency in this specific operating point, instead of compromising the peak efficiency for higher average efficiency.

The major downside of burst mode control is that low frequency harmonics are introduced, which increases the size of the needed input and output filters. Another disadvantage is added circuitry that adds both to complexity and to the losses, which reduces the efficiency at full load. Further burst mode requires the converter to be able to start and reach steady state quickly, most implementations use a burst frequency approximately two decades below the switching frequency in order to insure that the converter has time to reach steady state and operate efficiently for some time before it is shut down again [103, 134, 213].

Several control schemes for burst mode control are available with hysteresis [103, 32] and PWM [118] being the most commonly used, phase shift [213] and constant on-time are two other alternatives.

Hysteresis control has the best transient response, as the transitions between the on- and off-states are defined by the hysteresis window, instead of a fixed frequency or times as in the other schemes. Another advantage is very good efficiency at light loads due to a very low burst frequency. These advantages come at the expense of widely varying burst frequencies, which increases the complexity and potentially size of the needed input/EMI filter.

Phase-shift control has the same pros and cons as hysteresis control, but the delay in the control circuitry is utilized in the design, which makes it possible to use slower components than would have been needed with hysteresis control.

The design of the input filter is more straightforward with PWM, where a fixed burst frequency is used, but the transient response and light load efficiency degrades. The EMI performance of a VHF converter controlled by PWM burst mode, is in many aspects similar to a conventional hard switched converter operating at the burst frequency.

A 27 MHz class DE converter with a 21 kHz PWM burst mode control has been implemented, see Figure 7.3. The converter converts from the US mains to a 60 V LED load, hence transient respons is not important and the control bandwidth can be very low. Therefore, 21 kHz was chosen in order to be out of the audible range, but keep the burst frequency as low as possible in order to reduce the number of start-ups and the losses introduces by these. With this control, a very flat efficiency curve was achieved. The peak efficiency was 89.5% at full load and only dropped 5% at 10% load, see Figure 7.3. This was possible due to a very fast start-up circuit that made it possible to turn the converter fully on within 100 μs, hence start up

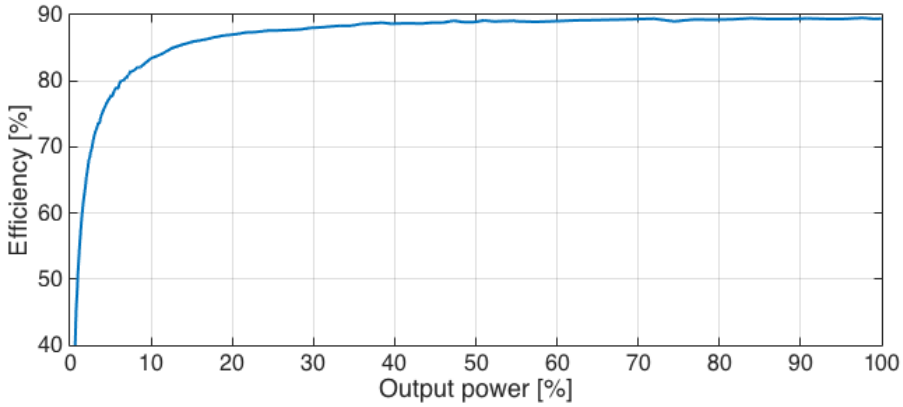


Figure 6.1: Measured efficiency curve for a DE converter switching at 27 MHz with fixed frequency burst mode control at 20 kHz.

losses were very low and only affected the efficiency when the ouput power became low.

Constant on-time control can be compared to PWM control, but with the on-time fixed instead of the frequency. This gives a more stable frequency than seen for hysteresis and phase-shift control, but still with good light load efficiency.

6.2 Outphasing

Outphasing, also referred to as Linear Amplification with Nonlinear Components (LINC), was introduced for RF amplifiers in the 1930s [214]. This control method has however only been used a few times in previous publication [211, 212] and posses several advantages compared to burst mode.

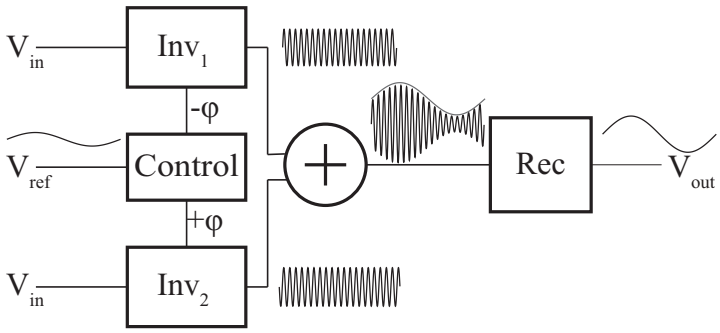


Figure 6.2: System view of a converter using outphasing modulation.

Outphasing control utilizes a phase shift between two or more inverters to control the combined output through a common rectifier, as illustrated with two inverters in Figure 6.2. In this way, the individual inverters run continuously at a fixed frequency while the total output to the load is regulated.

With this control method, all the benefits of the high switching frequency can be achieved, both fast transient response, wide control range and small input and output filters.

The main drawback of outphasing is that the losses in the inverters are almost constant at light and full load, which decreases the light load efficiency significantly. Further, the varying load and the inverters impact on each other is a challenge.

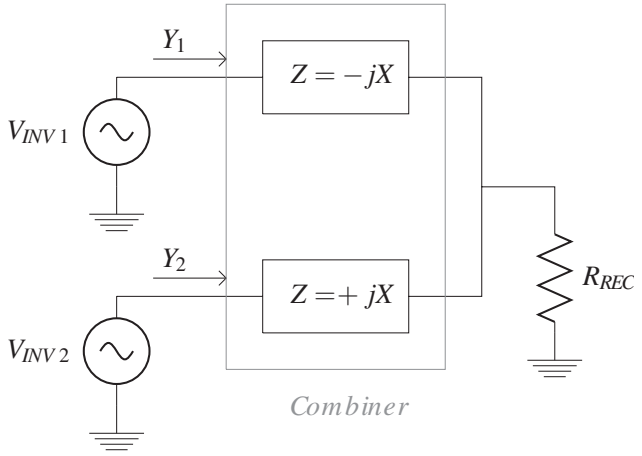


Figure 6.3: Schematic of the lossless combiner for outphasing modulation [215].

Selecting the right circuit to combine the output of the inverters (the combiner) is crucial to achieve a good result with outphasing. Several approaches have been suggested [216, 217, 218, 219], but the lossless combiner proposed in [215] (shown in Figure 6.3) posses several benefits for use in resonant converters. The combiner only consists of an inductor and capacitor, if these are assumed ideal the combiner is lossless. Further, the admittance seen by the two inverters can be made zero, ensuring purely resistive loading of the inverters. As resonant converters are very load dependent and quickly looses ZVS when loaded reactively, this is crucial in order to ensure high efficiency.

The input impedance of the rectifier, R_{REC}, can be assumed purely resistive at the switching frequency. Further, the output voltage of the two inverters, V_{INV1} and V_{INV2}, can be assumed equal to:

$$V_{INV1} = V_{IN} \cdot G_{INV} \cdot e^{-I \cdot \phi} \tag{6.1}$$

$$V_{INV2} = V_{IN} \cdot G_{INV} \cdot e^{I \cdot \phi} \tag{6.2}$$

Where V_{IN} is the input voltage amplitude, G_{INV} is a fixed gain between the input voltage to the converters and the peak output voltage.

The admittance seen by each inverter can now be written as:

$$Y_1 = \frac{1}{X} - \frac{I \cdot e^{I \cdot \phi} \cdot V_{OUT}}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \tag{6.3}$$

$$Y_2 = \frac{1}{X} - \frac{I \cdot V_{OUT}}{X \cdot e^{I \cdot \phi} \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \tag{6.4}$$

Where G_{REC} is a fixed voltage gain from the peak input voltage of the rectifier to

the output voltage, V_{OUT}. The imaginary part of the admittance is:

$$\Im(Y_1) = \frac{1}{X} - \frac{V_{OUT} \cdot cos(\phi)}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \tag{6.5}$$

$$\Im(Y_2) = \frac{1}{X} + \frac{V_{OUT} \cdot cos(\phi)}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \tag{6.6}$$

Setting this to zero and solving for the phase, ϕ, gives:

$$\phi = arccos\left(\frac{V_{IN} \cdot G_{INV} \cdot G_{REC}}{V_{OUT}}\right) \tag{6.7}$$

If the phase is controlled according to this equation, the loading of the inverters will be purely resistive. The real part of the admittance is:

$$\Re(Y_1) = \Re(Y_2) = \frac{V_{OUT} \cdot sin(\phi)}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \tag{6.8}$$

From this the output power, P_{OUT}, can be calculated for a given value of the combiner reactance, X, and input and output voltage by:

$$P_{OUT} = \frac{G_{INV} \cdot \sqrt{V_{OUT}^2 - V_{IN}^2 \cdot G_{INV}^2 \cdot G_{REC}^2}}{X \cdot G_{REC}} \tag{6.9}$$

From equation 6.8, it is seen that it is not possible to control the power, if the loading of the converters needs to be purely resistive. If the output voltage is kept fixed, the output power will, however, be a quadratic function of the input voltage that can be offset by the chosen reactance for the combiner.

A design example is given in A.19. The designed converter achieves very good performance with equally and purely resistive loading of the two inverters across the entire input voltage range. This combined with a design of the inverters that ensures that they can operate with ZVS across a wide load range, ensures efficient operation of the converter across the entire input voltage range. The aim was to achieve efficient line regulation with less than ± 20% output power variation for an input variation of ± 30%. This was achieved as the converters keept within ± 16.5% output power variation. Furthermore, the design exhibited very high efficiency across the entire input voltage range and only drops below 90% at the maximum input voltage.

Chapter 7

Electromagnetic Interference

Increasing the switching frequency into the VHF range reduces the value as well as the physical size of passive components significantly. This does not only reduce the size of the energy storing components inside the converter, but also the EMI filter can be greatly reduced [220, 221].

EMI problems arising from SMPS are well known and well described [222, 223, 224]. The vast majority of SMPS operate at switching frequencies well below 1 MHz and the size of the EMI-filter is governed by the limits regarding conducted emissions in the frequency range of 150 kHz to 30 MHz. Radiated emission in the range of 30 MHz to 1 GHz is typically a matter of proper PCB layout and design, not so much related to filter size. When the switching frequency is moved into the VHF range, above the range were conducted emissions are measured and into the range for radiated emissions, this changes and new challenges arise.

Table 7.1: EN55022 limits for conducted disturbance at the mains ports of class B ITE [225].

Frequency range MHz	**Limits** dB(μV/m)	
	Quasi-peak	**Average**
0.15 to 0.50	79	66
0.50 to 30	73	60

In terms of EMI emission test, there are two standard tests; conducted emission in the frequency range of 150 kHz - 30 MHz, see Table 7.1, and radiated emission in the frequency range of 30 MHz - 1 GHz, see Table 7.2. The separation of conducted and radiated at 30 MHz is made because Electro Magnetic (EM) disturbance is more likely to use near-field coupling paths such as inductive or capacitive at lower frequencies since impedance levels are below that of free space. At higher frequencies the characteristic impedance of traces and such increases and exceeds that of free space, making it more likely for the EM disturbance to radiate [226].

Table 7.2: EN55022 limits for radiated disturbance of class B ITE at a measuring distance of 10 m [225]

Frequency range MHz	**Quasi-peak limits** dB(μV/m)
30 to 230	30
230 to 1000	37

For non-VHF converters, the EMI-filter is mainly designed to attenuate the switching frequency and/or harmonics of this in the conducted emission range. The radiated disturbance encountered is usually caused by second-order effects such as oscillations caused by parasitics and diode reverse recovery issues [227]. Thus the radiated emissions from the converter are more related to layout issues and parasitics than the actual switching frequency.

For VHF converters, this is a lot different, since the fundamental switching frequency and not a secondary effect now generates the radiated emission. The major source is not an oscillation with small amplitude compared to the main switching waveform, it is main switching waveform.

If the physical size of the noise generator is much less than the wavelength, λ, of the disturbing frequency, it is normally assumed that there is no or little radiation from the source, since the generator does not constitute an effective antenna. The wavelength is given by:

$$\lambda = \frac{c}{f} \tag{7.1}$$

Where λ is the wavelength, c is the velocity, and f is the frequency. In the VHF range, the wavelength is 1-10 m, which is much longer than any dimensions in the converter. To be an effective antenna, the dimensions should at least be in the area of quarter wavelength.

For VHF converters, the noise source is much stronger than in traditional converters, so the assumption of no or little radiation from the converter does not apply. If the impedance to the outside world is larger than the intrinsic impedance of free air ($Z_0 = \mu_0 \cdot c_0 \approx 377\ \Omega$), we can estimate the maximum radiation from this source as [228]:

$$\mid E \mid = \frac{V \cdot l \cdot b \cdot (2 \cdot \pi/\lambda)^2}{4 \cdot \pi \cdot r} \tag{7.2}$$

Here V is the voltage, l is the length of the circuit, b is the width of the circuit, λ is the wavelength and r is the distance to the source.

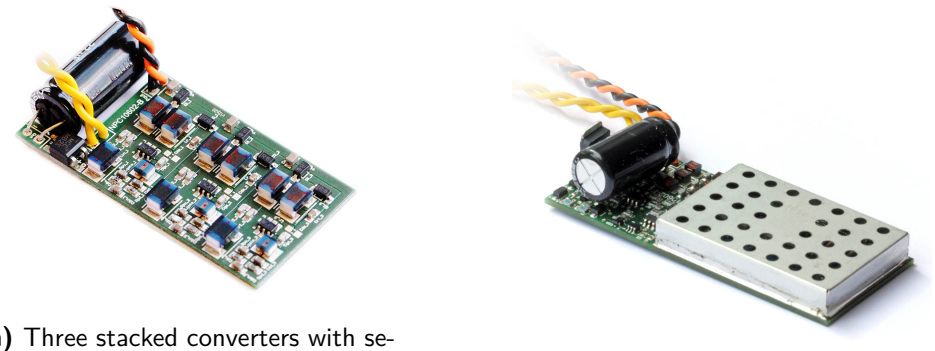
As an example, the VHF converter in Figure 7.1a will be used. This converter consists of three class E inverters with class DE rectifiers coupled with serial input and parallel output (SIPO). The converter operates at 37 MHz, converts a 120 V_{AC} input to a 60 V_{DC} output and delivers up to 20 W.

The main driver for the radiated emission is the drain node of the converter. The voltage swing at this node is approximately 120 V. The maximum noise from the circuit at a distance of 3 meters (assuming positive interference of the 3 VHF converters) will be approximately 79 dBμV. This is well above the limits of IEC55022B which is 40 dBμV at 37 MHz. Filters on the cables will hence not be enough to get the radiation below the limits. As a consequence, a shield has been mounted on the prototype in Figure 7.1b to reduce the radiation. Small filters are also needed to avoid radiation from the cables, these are however very small and can barely be seen under the electrolytic capacitor.

Figure 7.2a shows the conducted emissions measured on the prototype. As expected almost no emissions can be measured below 30 MHz. A small peak around 10 MHz is observed, the reason for this is unknown and due to the small amplitude this has not been investigated further. The radiated emissions on the other hand are very large for the unshielded prototype. At the switching frequency, the peak is almost 50 dBμV above the limit and all the harmonics are also way above the limits, see Figure 7.2b. Adding the shield and a small filter efficiently reduces these peaks well below the limits, see Figure 7.2c. This clearly shows that shielding is necessary, but also that it is a very effective way of reducing the radiated emissions.

As mentioned in chapter 6, one of the major drawbacks of burst mode control is the introduction of low frequency harmonics, which needs to be filtered to meet the EMI standards. For application were high control bandwidth is not required, but wide load range is, it is however very appealing and it is therefore interesting to investigate how big the drawback is. A class DE converter with specifications semilar to the one just descibed has been developed, but with a 21 kHz burst mode control added.

The prototype is shown in Figure 7.3 and the EMI measurements made on it is shown in Figure 7.4 and 7.5. The conducted emmisions were expected to be the biggest challenge due to the low frequencies introduced, but as seen in Figure 7.4b and 7.4c the prototype complies with EN 55022 both at full and 50% load. At full load the burst mode control is not active as the duty cycle is 100%, but at 50% load the full effect is seen as a lot of low frequency harmonics. It was however possible to reduce these harmonics to a level well below the limits with small filters. The electrolytic capacitor at the input was needed to reduce flicker on the output and



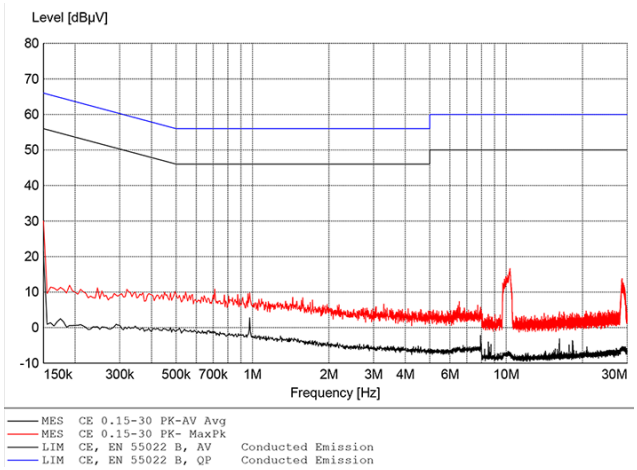
(a) Three stacked converters with serial input and parallel output

(b) With EMI filter and shield

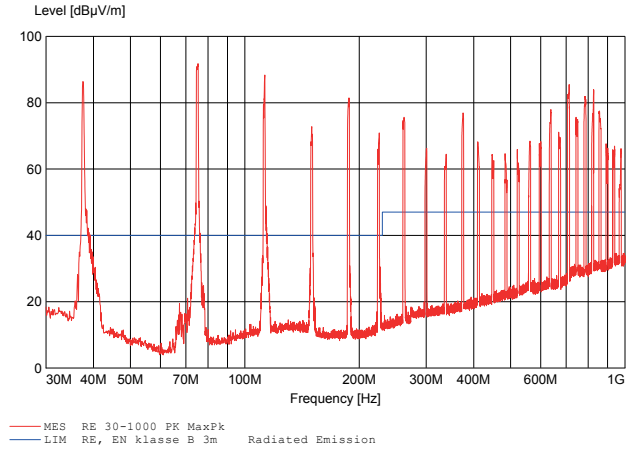
Figure 7.1: Pictures of 20 W converters operating at 37 MHz.

reduce the input voltage range for the converter, hence the only component added to attenuate the low frequency harmonics was a small inductor, which can hardly be seen under the capacitor.

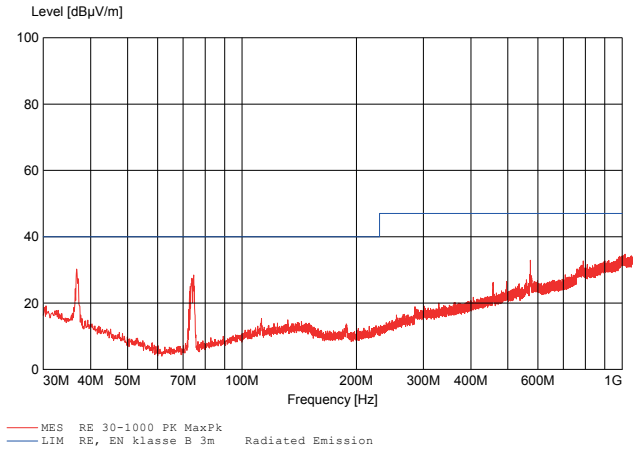
The radiated emmisions are seen in Figure 7.5a and 7.5b, without and with filter and shield, respectively. A lot of the radiated emmisions were removed by adding the shield and a small filter, but three of the peaks are still above the limits. It is expected that these peaks can be removed by optimization of the layout and use of three legged capacitors, but this has not been implemented yet.



(a) Conducted emmisions from the prototype



(b) Radiated emmisions from the prototype without filter and shield



(c) Radiated emmisions from the prototype with filter and shield

Figure 7.2: EMI measurements on a 20 W converter operating at 37 MHz.

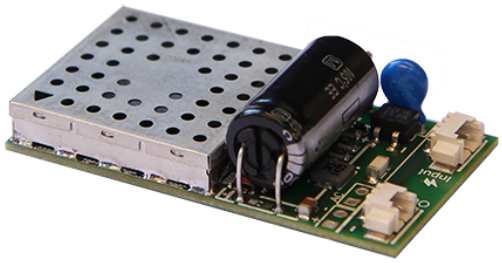
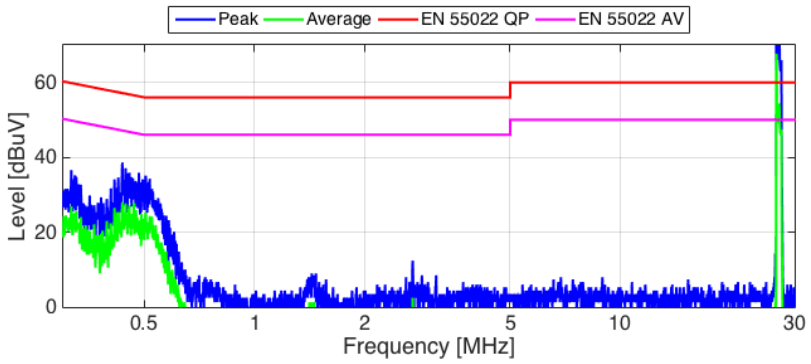
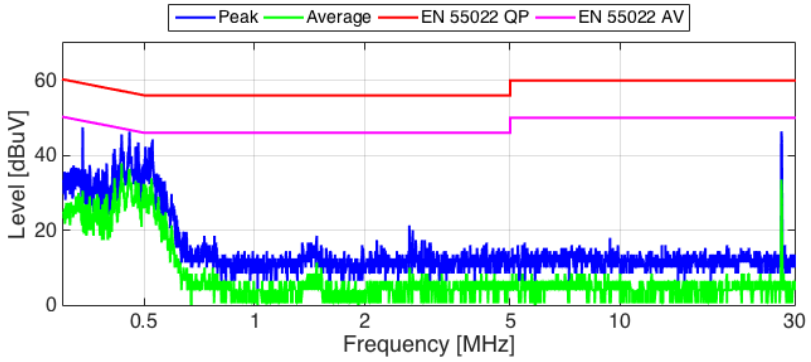


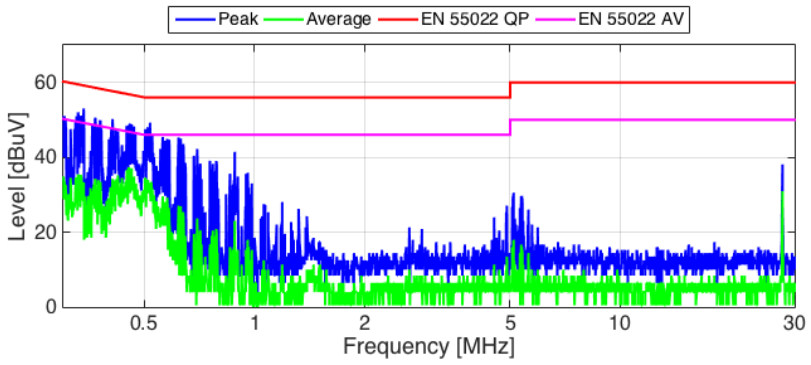
Figure 7.3: A 20 W prototype based on a 27 MHz class DE converter.



(a) Conducted emmisions without filter at full load

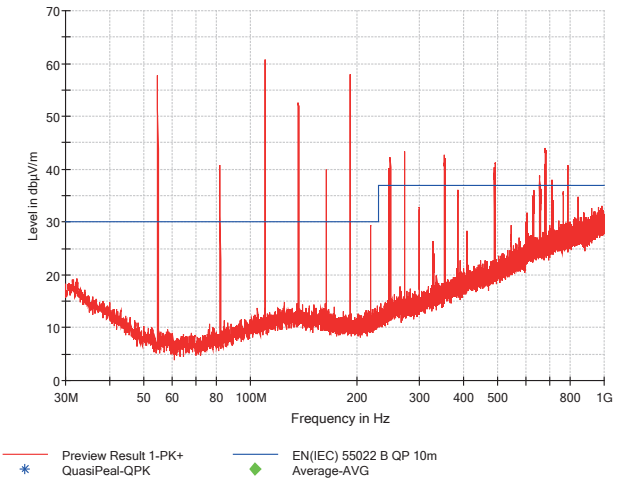


(b) Conducted emmisions with filter at full load

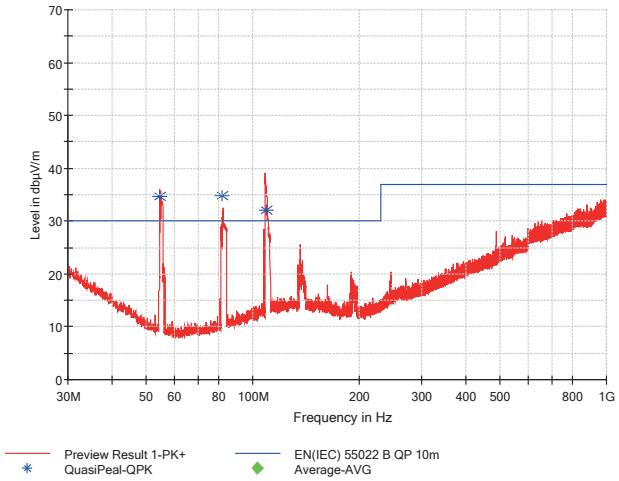


(c) Conducted emmisions with filter at 50% load

Figure 7.4: Conducted EMI measurements on a converter with burst mode control.



(a) Radiated emmisions without filter and shield



(b) Radiated emmisions with filter and shield

Figure 7.5: Radiated EMI measurements on a converter with burst mode control.

Chapter 8

Conclusion and Future Perspectives

8.1 Summary

Several interesting topics have been researched throughout this thesis, so before making the final conclusion a small summary will be made.

The single most innovative part of this thesis is the self-oscillating resonat gate drive, it is the basis for most of the other results that have been achieved. The gate drive described in section 4.2 was first described in [163], but has been investigated and applied much further during this work. The gate drive is simple, cost effective and reliable due to its low component count and its self-oscillating behavior, which automatically incorporates component tolerances. The gate drive has been used for low side switches as many other gate drives shown in the literature, but it has also been shown in a synchronous rectifier were the self-oscillating behavior and independency of signals from the primary side is great advantages. Further it has been shown working as a high side gate drive, this is the first VHF high side gate drive presented in the world.

The fact that there is now a gate drive that can drive high side switches in VHF converters opens up a whole new range of topologies. Half and full bridge topologies are commonly used at lower frequencies, especially for step down converters, but this is the first time that a VHF version has been shown. So far only a simple DE converter has been made, but with the high side gate drive new topologies as the LLC, LCC, full bridge etc. are to be explored.

Further, the gate drive has only been used in the simple version with just a sine wave as the gate signal. Adding more harmonics to get a more trapezoidal signal and thereby faster switching of the MOSFET is expected to make it possible to achieve even higher efficiencies.

The class DE converter lowers the voltage stress on the MOSFET, from 3.56 times the input voltage for the class E to just the input voltage. This is a great improvement on one of the biggest challenges for VHF converters, but with the introduced

input-output rearrangement presented in Section 3.3, this can be improved even further. For a non-isolated 2:1 converter the voltage stress on the MOSFET can now be reduced from 3.56 times the input voltage to just half the input voltage, hence 7.12 ($3.56 \cdot 2$) times. Further, half of the power is delivered to the load without going through the converter, hence almost 100% efficiently and without causing heat in the converter. This not only decreases the demand for break down voltage of the MOSFET, but also makes the resonating energy inside the converter more than 50 times lower ($(3.56 \cdot 2)^2$). This makes it much easier to make a VHF converter with a high input voltage, such as rectified mains, which delivers a low to medium level output power (0 to 200 W), for instance for charging a phone or laptop or for LED lighting.

With the very high frequencies air core inductors, and especially PCB embedded air core inductors, become a feasible alternative to cored magnetics. A MATLAB program with an intuitive and easy to use graphical user interface was made to design these. This program takes the PCB production parameters and the desired inductor specifications as input, uses a genetic algorithm to optimize the inductor structure and gives a PCB file with the inductor ready for production as output. This makes it very simple to design converters utilizing PCB embedded inductors and hence removes a great barrier for circuit designers.

Two widely different control algorithms have been investigated, namely burst mode and outphasing. Outphasing is great for applications were control bandwidth is the main concern and were the converter operates close to full load most of the time. For applications were light load efficiency is important, outphasing fails due to more or less constant loss independent on output power. Here burst mode is much more efficient and if control bandwidth is not a concern, particularly PWM burst mode with a low switching frequency. A prototype of a DE converter with PWM burst mode control was presented where the efficiency only dropped 5%-point from full load to 10% of full load.

Finally, the new electromagnetic challenges arising from the highly increased switching frequencies have been investigated. It has been shown how a shield around the power stage efficiently encapsulates the magnetic fields and makes it possible to pass EN 55022 [225]. Further, the EMI performance of a burst mode controlled VHF converter has also been presented for the first time. The measurements showed a lot of harmonics at low frequencies, but they could be filtered out with small and inexpensive filters in order to make the prototype pass the requirements for conducted emissions.

To sum up, the main contributions from this work are:

- Further investigation of the gate drive invented in [163]
- Proof of principle that the gate drive also work for synchronous rectification and high side gate drives
- The worlds first VHF half-bridge converter operating at more than a few volts
- Development of a rearranging method that significantly reduces the voltage stress and improves the efficiency

- The first direct comparison of toroid, spiral, and solenoid PCB embedded inductors
- Presentation of conducted and radiated EMI measurements with and without shield and burst mode control
- Development of prototypes that clearly shows the potential of VHF converters

8.2 Conclusion

This thesis started out with the objective:

"The objective of this PhD thesis is to investigate, whether it is possible to increase the switching frequency of power converters into the Very High Frequency range (VHF, 30-300 MHz).

The converters should achieve efficiencies at least on par with commercial products and use standard components in order to keep cost low. The aim is to show that a size and weight reduction of 80% can be achieved without compromising cost, efficiency or reliability."

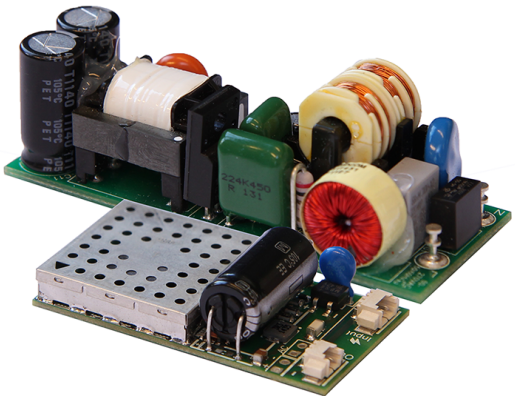


Figure 8.1: A 20 W prototype based on a 27 MHz DE converter compared with an equivalent commercial product.

Table 8.1: Performance improvements compared with a commercial product.

Parameter	Commercial	Thesis result	Improvement
Power	20 W	20 W	0%
Efficiency	85 %	89.5%	4.5%
Size	33 cm^3	9.9 cm^3	70%
Wheight	53 g	10 g	81%
Cost	≈3.2 $	≈1.4 $	56%

To verify if this has been achieved, the 20 W prototype with burst mode control is compared to commercial product in Figure 8.1 and Table 8.1. The picture clearly shows a dramatic size reduction, not the full 80%, but 70% size reduction was

achieved. This is more than has been achieved the last decade and more than predicted for the comming decade [13]. To be fair, the frequency is strictly speaking slightly outside the VHF range, but the technology and principles has been shown to work at VHF as well.

A weight reduction of 81% was achieved, hence more than 80% aimed for. This is largely due to the removal of magnetic core materials. The cost is not only kept low, but actually decreased more than 50%. The prices are calculated based on bill-of-materials and production of 100,000 units. These numbers are not exact, but clearly indicate that the cost is not compromised but reduced.

Early in the project, it became clear that heat would become the main challenge in order to achieve the desired size reduction. Focus has therefore been on improving the efficiency, as well. This has been done with an improvement of 4.5% or a 30% reduction of the losses generated in the converter.

These results clearly show a big potential for this technology. It is not only possible to get a converter that is significantly smaller and lighter, it is also more cost and power efficient. This project started out as an ambitious research project, but the results have been so promising that a company has been founded on this basis and commercial products are expected on the market by the end of the year.

8.3 Future Perspectives

Several aspects of VHF converters have been researched throughout this thesis, but there is still more to be done. The great achievements gotten so far leaves a good insentive to continue the research and develop the technology further and reach even higher level of miniaturization, higher efficiencies and wider control bandwidth. The future perspectives are split into two parts in the following, one focusing specificly on VHF converters and one on technologies for miniaturization.

8.3.1 Research within VHF SMPS

Some of the aspects that should be covered in the future research within VHF converters include:

- **Multi resonant gate drives**
  The simple version of the resonant self-oscillating gate drive has been used in most curcuits so far, but significant improvements are expected when the more advanced implementations are used.
- **LLC, LCC and full bridge**
  With a high side gate drive available the path is clear for research in a whole new range of toplogies suited for operation at VHF. All these topologies have yet to be investigated and evaluated at VHF for the first time.
- **Power factor correction**
  Power factor correction is already a requirement in many applications above 75 W, but the requirements are expected to be even more strict in the future.

The power level for LED lighting is for instance already lowered to 25 W. It is therefore of prime importance to investigate how VHF converters that can be compatible with the existing and comming requirements for power factor correction.

- **Control**
  Some control schemes have already been explored, but they are all a trade off between control bandwidth and efficiency. The high switching frequencies posses the opportunity to achieve very high control bandwidth and rapid transient respons, but so far the only control schemes achieving this either sacrifice light load efficiency or introduce low frequency harmonics.

- **Magnetics**
  Future research within PCB embedded inductors should include derivation of formulas to calculate the parasitic capacitance and thereby also the resonance frequency, as these will become important for designs where large structures are needed to get higher Q factors.

  Though there are many benefits of avoiding core materials, they also give some great advantages, such as smaller inductor sizes, better control of the magnetic fields and stronger coupling in transformers. Future research should therefore also include investigation in material suitable for use at these frequencies.

- **Semiconductors**
  Today semiconductors, especially MOSFETs, are mainly optimized for use in low frequency hard switching converters where on-resistance and gate charge are the two most important design parameters. For MOSFETs used in VHF converters these parameters are still important, but output capacitance and gate resistance are more important. Hence, MOSFETs which are optimized for this could increase the efficiency of VHF converters even further.

- **Gallium Nitride**
  From Figure 2.8, it is clear that there is a big area where both VHF converters and GaN FETs are well suited, hence GaN based VHF converters should be investigated further. With GaN, greater efficiencies can be achieved due to the better charge/resistance FOM, but GaN have also higher electron mobility enabling devices that can switch even faster and hence the opportunity to push the switching frequency even further.

- **Increased frequencies**
  The possibility of pushing the switching frequency even further should definitely be investigated further, with or without GaN, the limits of Si have not been reached.

- **Packaging**
  Packaging of semiconductors have to be researched further to push the frequency and insure thermal performance. In order to get MOSFETs with a trade off between on resistance and output capacitance more suited for VHF converter a smaller device is needed, hence the package has to handle the same heat from a smaller device. Further the parasitcs of the package, especially inductances, become extremely important when the frequency is pushed even

further, hence low inductance packages with great thermal performance will be needed for future VHF converters.

- **Integration**
  Several integrated VHF converters were presented in Section 2.1.3 and 2.1.5, but all for low voltage levels. Integration of medium voltage and power VHF converters have yet to be fully explored. The best way to do this would properly be to follow the three steps desribed in Section 2.1.5, by first intregating the discrete versions into modules, then to PSiP, and finally aim for fully monolithic integration in a PwrSoC.

- **Thermal management**
  Already during this project thermal management started to become the biggest challenge and this challenge will only increase as power density is pushed even further. Therefore, thermal management will be of prime importance in future research, heat sinks, thermal bridges, potting materials and PCB technologies have to be investigated to find the most efficienct ways of getting the heat away from the converter.

- **Electromagnetic Interference**
  Detailed investigation of the EMI from VHF SMPS is also needed. If it turns out that this is a problem, structures surrounding the inductor to encapsulate the field could be a solution, magnetic shielding or a secondary short-circuited winding might be a solution.

8.3.2 Technologies for Miniaturized Power Electronics

The VHF technology alone will not be enough to meet the constant requirement for miniaturization. As already mentioned in the previous section other technologies have to support this development. This section below gives the authors thoughts about how the technologies for power electronics suited for mid-range voltages (10-500 V), mid power (1-500 W) and consumer/mid-range products will develop during the next decade:

This year:

- Modules and PwrSiP - They are already here and the range of products increase fast, Vicor for instance released their newest module just last month [71]. The prices are however still high and need to go down to get mass adoption.

- GaN - The first semiconductor products have been on the market for a few years, but the first products are just about to reach the market [229].

- VHF SMPS - Several publications about VHF SMPS have been made during the last decade, but the first commercial products will reach the market this year [230].

Within five years:

- PwrSoC - The first commercial products operating at a few volts were presented in [80], but products will slowly start to move in to the lowest range of power electronics (10-50 V and 1-5 W).
- VHF GaN SMPS - Once both technologies are matured and adopted by the market, the volume will increase and price go down due to the economics of scale. Hence it will be possible to make very attractive products at a fair price by combining these technologies.
- VHF Modules/PwrSiP - As the power density continue to increase, this needs to happen to get full control of parasitics, interconnections and thermals.
- SC+VHF PwrSoC - Combining switch capacitor circuits and resonant converters in a fully integrated converter posses some great opportunities for exploring more advanced topologies and control methods. This can hence become a powerful combination again starting with the range 10-50 V and 1-5 W.
- GaN based ICs - With the first GaN semiconductors ready on the market, GaN is expected to follow the same roadmap as Si based semiconductors and ICs. The next step will hence be a few devices on the same die and later full ICs [77].

Within ten years:

- SC+VHF GaN PwrSoC - When both PwrSoCs with switch capacitor and VHF converters and GaN ICs are ready it will be a natural next step to combine these technologies to get even better performance.
- UHF - Ultra high frequency (0.3-3 GHz [9]) converters have already been published, for instance a 770 MHz converter with an efficiency above 70% [231]. Commercial products are, however, still a bit far out in the future, but might become availible within the next decade due to advances in both VHF technologies, wide band gap devices and packaging.

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Appendix A

Publications and Patents

List of patent applications and publications at conference and in journal:

A.1 A. Knott, T. M. Andersen, P. Kamby, **M. Madsen**, M. Kovacevic, M. A.E. Andersen: *"On the Ongoing Evolution of Very High Frequency Power Supplies"*, IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA, March 2013. Conference Proceedings p2514-2519.

A.2 A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, **M. Madsen**, M. Kovacevic, M. A.E. Andersen: *"Evolution of Very High Frequency Power Supplies"*, IEEE Journal of Emerging and Selected Topics in Power Electronics, September 2014, vol.2, no.3, pp.386-394.

A.3 **M. Madsen**, A. Knott, M. A.E. Andersen: *"Low Power Very High Frequency Resonant Converter with High Step Down Ratio"*, IEEE AFRICON, Mauritius, September 2013. Conference Proceedings p1-6.

A.4 **M. Madsen**, A. Knott, M. A.E. Andersen: *"Low Power Very High Frequency Switch-Mode Power Supply with 50 V Input and 5 V Output"*, IEEE Transactions on Power Electronics, December 2014, vol.29, no.12, pp.6569-6580.

A.5 **M. Madsen**, A. Knott, M. A.E. Andersen: *"Very High Frequency Resonant DC/DC Converters for LED Lighting"*, IEEE Applied Power Electronics Conference and Exposition, Long Beach, CA, March 2013. Conference Proceedings p835-839.

A.6 **M. Madsen**, A. Knott, M. A.E. Andersen: *"Very High Frequency Half Bridge DC/DC Converter"*, IEEE Applied Power Electronics Conference and Exposition, Fort Worth, TX, March 2014. Conference Proceedings p1409-1414.

A.7 **M. Madsen**, M. Kovacevic, J. D. Mønster, J. A. Pedersen, A. Knott and M. A.E. Andersen: *"Input-Output Rearrangement of Isolated Converters"*, IEEE Power and Energy Conference at Illinois, Champaign, IL, February 2015. Conference Proceedings p1-6.

A.8 M. Kovacevik and **M. Madsen**: *"Step-up dc-dc power converter"*, WO2015091590 A2, June 25th 2015

A.9 M. Kovacevik and **M. Madsen**: *"Step-down dc-dc power converter"*, WO2015110427 A1, July 30th 2015

A.10 **M. Madsen**, J. A. Pedersen, A. Knott, M. A.E. Andersen: *"Self-Oscillating Resonant Gate Drive for Resonant Inverters and Rectifiers Composed Solely of Passive Components"*, IEEE Applied Power Electronics Conference and Exposition, Fort Worth, TX, March 2014. Conference Proceedings p2029-2035.

A.11 J. A. Pedersen, **M. Madsen**, A. Knott and M. A.E. Andersen: *"Self-oscillating Galvanic Isolated Bidirectional Very High Frequency DC-DC Converter"*, IEEE Applied Power Electronics Conference and Exposition, Charlotte, NC, March 2015. Conference Proceedings.

A.12 **M. Madsen** and J. A. Pedersen: *"Self-oscillating resonant power converter"*, WO2014067915 A2, November 2nd 2012

A.13 **M. Madsen**, A. Knott, M. A.E. Andersen, A. P. Mynster: *"Printed Circuit Board Embedded Inductors for Very High Frequency Switch-Mode Power Supplies"*, IEEE Energy Conversion Congress and Exhibition Asia DownUnder, Melbourne, Australia, June 2013. Conference Proceedings p1071-1078.

A.14 **M. Madsen**, J. D. Mønster, A. Knott, M. A.E. Andersen: *"Design Optimization of Printed Circuit Board Embedded Inductors through Genetic Algorithms with verification by COMSOL"*, COMSOL conference 2013, Boston, MA, October 2013. Conference Proceedings.

A.15 H. Schneider, T. Andersen, J. D. Mønster, **M. Madsen**, A. Knott, M. A.E. Andersen: *"Investigation of a Hybrid Winding Concept for Toroidal Inductors using 3D Finite Element Modeling"*, COMSOL conference 2013, Boston, MA, October 2013. Conference Proceedings.

A.16 H. Schneider, T. Andersen, J. D. Mønster, **M. Madsen**, T. Andersen, A. Knott, M. A.E. Andersen: *"Optimizing Inductor Winding Geometry for Lowest DC-Resistance using LiveLink between COMSOL and MATLAB"*, COMSOL conference 2013, Boston, MA, October 2013. Conference Proceedings.

A.17 J. D. Mønster, **M. Madsen**, J. A. Pedersen and A. Knott: *"Investigation, development and verification of printed circuit board embedded air-core solenoid transformers"*, IEEE Applied Power Electronics Conference and Exposition, Charlotte, NC, March 2015. Conference Proceedings.

A.18 **M. Madsen** and J. Mønster: *"Embedded solenoid transformer for power conversion"*, WO2015092070 A1, June 25th 2015

A.19 **M. Madsen**, D. J. Perreault, A. Knott and M. A.E. Andersen: *"Outphasing Control of Gallium Nitride based Very High Frequency Resonant Converters"*, Accepted for presentation at IEEE COMPEL 2015 with subsequent publishing in the conference procedings.

A.20 M. Kovacevik and **M. Madsen**: *"Burst Mode Control"*, WO2015128398 A1, September 3rd 2015

A.21 **M. Madsen** and M. Kovacevik: *"On and Off Controlled Resonant dc-dc Power Converter"*, WO2015128397 A1, September 3rd 2015

A.22 **M. Madsen**: *Confidential*, DTU ref 95513

The full length versions of the papers and the four of the patent applications are included on the following pages.

A.1 **A. Knott, T. M. Andersen, P. Kamby, M. Madsen, M. Kovacevic, M. A.E. Andersen:**
***"On the Ongoing Evolution of Very High Frequency Power Supplies"*,**
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On the Ongoing Evolution of Very High Frequency Power Supplies

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***Abstract*—The ongoing demand for smaller and lighter power supplies is driving the motivation to increase the switching frequencies of power converters. Drastic increases however come along with new challenges, namely the increase of switching losses in all components. The application of power circuits used in radio frequency transmission equipment helps to overcome those. However those circuits were not designed to meet the same requirements as power converters. This paper summarizes the contributions in recent years in application of very high frequency (VHF) technologies in power electronics, describes the remaining challenges and shows results of the recent advances, among others a 120MHz, $9\ \text{W}$ LED driver with $89\ \%$ efficiency.**

I. Introduction

The continuing trend of miniaturization in industrial and consumer electronics is continuously driving a demand for smaller power supplies. Weight and cost reduction demands accompany this trend. Within power supplies the major size, weight and cost drivers are typically the passive components. Increasing the switching frequency of power converters can reduce the size, weight and therefore the cost of those. For substantial size and weight reduction, the switching frequencies are increased up to the very high frequency (VHF) band (30 MHz to 300 MHz), which leads to a merge in circuit technologies used in radio frequency transmitters [1]–[6] and the classical power electronics circuits.
The VHF amplifiers are designed for DC-AC conversion, where the AC simultaneously is the switching frequency. Generally those circuits [1], [2] drive a known load impedance, typically a $50\ \Omega$ antenna. The most efficient standard representatives of radio frequency amplifiers are class-E [3], [4] and class-F [5], [6], where Class-E applies zero-voltage-switching (ZVS) and Class-F applies zero-current-switching (ZCS) techniques. Similarly to switch-mode power supplies, those VHF amplifiers convert the constant supply voltages into a high-frequent voltage by operating power semiconductors in the cut-off or saturation region only. The major difference is, that VHF amplifiers do not convert the energy back into a constant voltage or current level.
Numerous research works have been published [7]–[18], filling this gap and making VHF technologies available for power electronics. This paper describes the individual contributions of those in greater detail. However there are still some challenges left, before VHF switch-mode power supplies can relieve their advantages for products in industrial and consumer electronics.
This paper elaborates on the remaining challenges based on previous work and characterizes them in Section II. Section III describes the most recent advances, showing prototypes and measurement results. Section IV concludes the paper.

II. Challenges of VHF Converters

VHF operation of power supplies differs from sub-megahertz operated power supplies (here called traditional power converters) mainly by the following subjects:

- Electronic components, both active and passive,
- Circuit architectures for power stages and control parts,
- Adjacent behavior, such as electromagnetic compatibility (EMC) and mechanics.

A. Components

Especially inductive components are size, weight and cost optimization limitations in nowadays power circuits. Simultaneously VHF converters provide a major opportunity to overcome those.
Among the challenges are core losses, skin and proximity effect [19]–[25]. Another challenge within passive components for VHF is the creation of a galvanic isolation barrier [26], [27].
Despite passive components also active components, i.e. the power semiconductors, need to fulfill other requirements than in usual power supplies [28]–[30]. The parasitic components have a big influence on the design of the overall converter, as they are part of the design parameters. Unlike traditional power stages, the parasitic elements are therefore not considered undesired, but form an integral part of the stage. An example is the output capacitance C_{oss} of the power semiconductor in a Class-E based power supply. According to [17] it is dependent on output power P_{out}, input voltage V_{in} and switching frequency f_{sw} as shown in equation 1.

$$P_{out} = 2\pi^2 f_{sw} C_{oss} V_{in}^2 \tag{1}$$

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B. Architectures

Where traditional power electronics circuits use square wave gate drive signals, the presented VHF converters so far utilized sinusoidal gate drive [16], [31]–[33]. This is mainly due to the input capacitance C_{iss} of VHF power semiconductors, which require a high peak current at extremely high speed. To consider the drive trapezoidal, the rise and fall times have to be less than $1\ \mathrm{ns}$ [33]. A trapezoidal or square wave drive would minimize the time of the power switch in linear operation and therefore decreases the losses.

The degrees of freedom in terms of modulation principles are less for VHF converters. Whereas power electronics circuits usually use pulse width modulation or phase modulation, the VHF converters efficiency is dependent on those parameters. Therefore they need to be adjusted statically to avoid losses by leaving the ZVS (or ZCS) range. A way to get around this is to apply burst mode control [15], [31], [34]. This method however introduces another low frequency component in the spectrum, which has to be buffered or filtered at both the in- and output of the converter. A requirement that enforces the use of bulky components and therefore is counterproductive to the intended advantages of VHF converters in the first place. While the VHF converters offer good possibilities for fast transient regulations, their low frequency control performance is limited by intrinsic bandpass behaviors through serial capacitors. Even though some rectifiers are available with parallel capacitances and impedance transformation [17], [35], more suitable architectures are missing. Thereby it needs to be taken into account, that the original VHF power circuits are designed to match a defined load (typically the impedance of the antenna) and therefore impedance transformation circuits can be realized in a passive way. Power converters however are connected to highly varying loads, i.e. load circuit in idle - drawing no energy from the supply - and full load - demanding the maximum output from the supply. Therefore active and lossless impedance matching circuits are required. Having such circuits at hand opens for utilization of the high gain bandwidth in VHF converters for line and load regulation.

C. Adjacencies

Lastly the interaction of VHF converters with its physical environment is different than the one of traditional power converters.

On the one hand, the electromagnetic interaction between circuits increases, the higher the relevant frequencies are [36]–[39]. Fields are distributed easier both inside the converter and to its surroundings. The electrical behavior also becomes highly dependent on electromechanical interfaces, such as cooling and housing. However the harmonics of the resonant waveforms are falling faster, than the harmonics in hard switched traditional power converters [18]. Also the harmonics of the fundamental switching frequency are spaced wider. That means the distance can be used to place strategically important EMC bands, dependent on the application.

On the other hand, the carefully adjusted operating points of VHF converters (for efficiency purposes) are highly dependent on temperature [17], [18]. Adaptive mechanisms for ensuring optimal operation over industry standard temperature ranges are yet to come.

III. Recent Advances

Despite those challenges recent research results enhanced the state-of-the art in VHF converters and gives hope to overcome the remaining challenges.

The Class-E based power circuits allow for a second degree of soft switching. Despite turning the power switches on, when the voltage across them is zero (ZVS) or off, when the current through them is zero (ZCS), also the derivatives of these signals are taken into account. This is called ZdVS and ZdCS respectively. The technique has been applied to power converters in [17]. Figure 1 shows the full schematic of the power part of the self-oscillating VHF converter (DC-DC) from [17], [32].

Figure 2 shows the simulated waveforms of this converter, where v_s and i_s are the voltage and the current across and through the switch and v_D and i_D are voltage and current across and through the rectifier diode. v_G is the control signal of the power switch and V_o and V_i are input and output voltages of the converter. The top graph v_s visualizes the optimization of the converter for both ZVS and ZdVS.

Figure 3 is a photograph of the implementation of this converter. The overall efficiency of the $97\ \mathrm{MHz}$ converter is $55\ \%$.

Due to the tight adjustment of the turn on instance of the power switch for achieving ZVS and ZdVS the degrees of freedom in this converter are low. That limits the input and output voltage ranges. Furthermore the efficiency is not acceptable. In this case, the majority of the losses are due to conduction losses in the power semiconductors.

Suboptimal operation of Class-E converters as described in [4] opened for higher degrees of freedom in the design of Class-E based DC-DC converters. This means, that the ZdVS condition is only fulfilled under nominal load conditions and only ZVS is fulfilled otherwise. The effects of these operation mode as described in [40] has been extended in [18] to LED lighting applications.

Furthermore [18] provides a detailed analysis of the power components parasitics and the effect of their nonlinearities. The most relevant parasitics of the power switch are the input and output capacitances. They are typically highly nonlinear. Figure 4 shows the relative voltage stress of the power switch

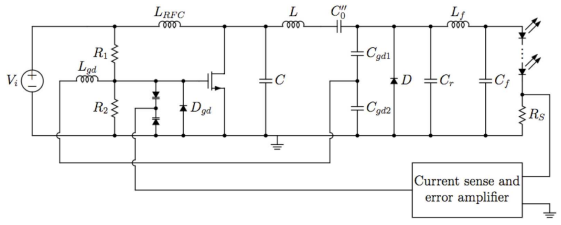


Fig. 1: Complete schematic of a self-oscillating VHF converter [32] with LED load.

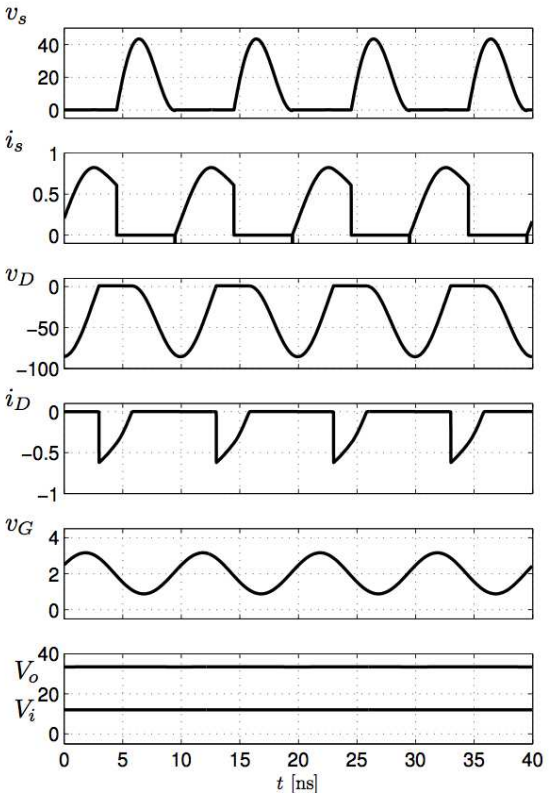


Fig. 2: Simulation of waveforms for a ZVS and ZdVS Class-E based converter from [17].

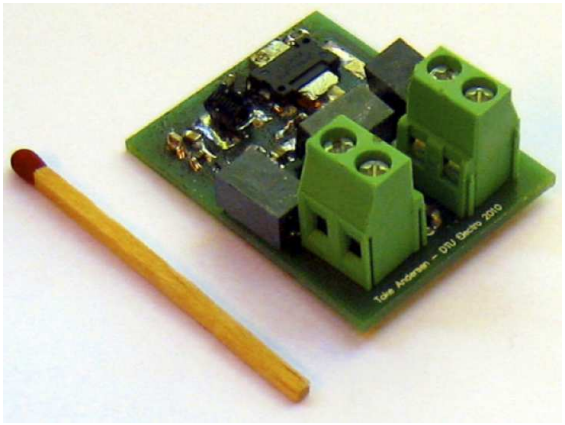


Fig. 3: Photograph of the self-oscillating VHF converter from [32].

as a function of time and junction potential.

The other components of the power stage have been investigated in [18] as well. Thereby most focus is on the inductors, as these are the most volume consuming parts, have the biggest weight and typically a big impact on the overall price of the converter. Therefore the inductors have been integrated as toroids into the printed circuit board (PCB). This process

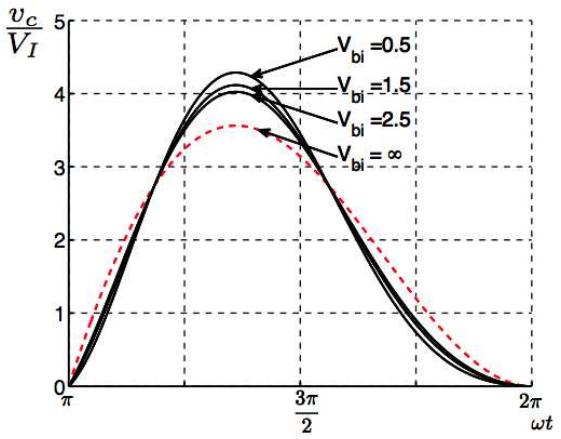


Fig. 4: Voltage stress of the power switch in relation to DC input voltage for a nonlinear output capacitance from [18]. V_{bi} is the junction potential of the process.

is described in [41] and Figure 5 shows the principle.

The resulting converter waveform in the optimal and suboptimal operating regions are shown in Figure 6. The converters efficiency is in the same area as the previous presented. For dealing with the efficiency challenge, [42] compared a number of power switches both in simulation and experiment. Figure 7 shows photographs of the implementations. On top of that an effective line- and load regulation scheme was implemented in those.

Figure 8 shows the implementation of the final prototype with 70 MHz switching frequency. The voltage step-down ratio of the converters is 10 and the output power range is between 1

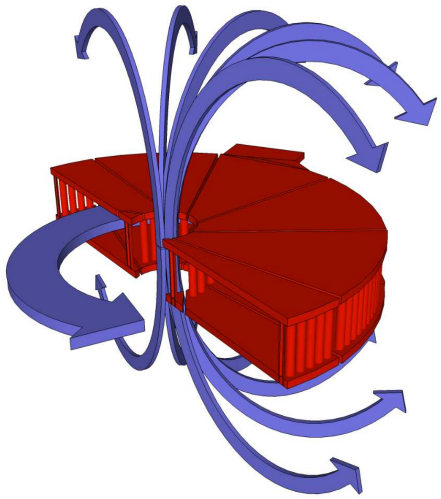
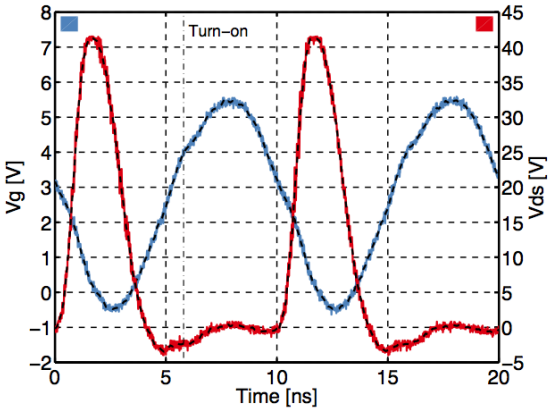
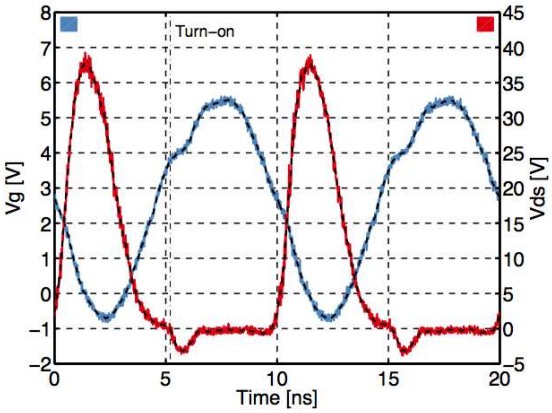


Fig. 5: PCB integrated inductor from [41]. The copper contained in the PCB is shown in red. The blue arrows mark the magnetic field.



(a) optimal operation



(b) suboptimal operation

Fig. 6: Measurements of gate-source and drain-source voltages V_{gs} and V_{ds} of the power switch and the turn-on instances. Note that the drain-source voltage has an offset of -0.5 V, due to the oscilloscopes offset.

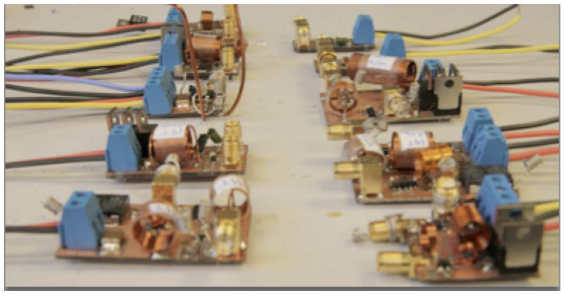


Fig. 7: Photograph of numerous prototypes for comparing measured efficiency with simulations [42].

and 4W at an efficiency within this range beyond 70 %.

Additionally the self-oscillating principle from [17], [32] was applied to an interleaved Class-E converter in [43], resulting into a significant efficiency improvement. The complete schematic is shown in Figure 9. The realized converter is switching at 120 MHz, i.e. beyond the FM band, converts

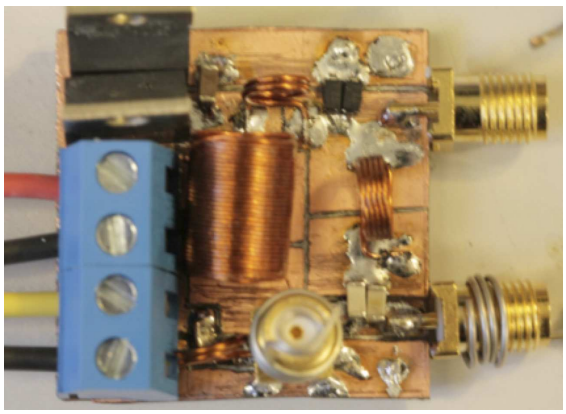


Fig. 8: Photograph of a closed loop low-power VHF converter with an efficiency beyond 70 % from [42]. The TO220 components on the upper left is the dummy load resistance.

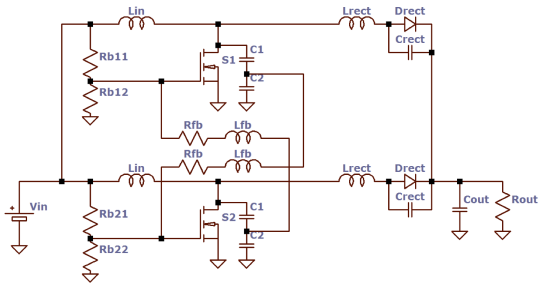


Fig. 9: Full schematic of interleaved Class-E converter from [43].

an input voltage between 6 and 9 V into an output current between 0.4 and 0.5 A and has an efficiency between 80 and 89 % within this operation range. The output power range is 3 to 9 W and the converter is built for LED drive. Figure 10 shows both a SPICE based simulation and a the measurement of the power switches voltage waveforms.

IV. Conclusion

The merge of techniques used in radio communication electronics and power electronics was pointed out. The development through the previous decades has been revisited and recent developments were summarized. Remaining challenges and the latest advances were described. The implementations of numerous VHF converters were presented. Among them are low-power, high-step-down converters with a switching frequency of 70 MHz and an efficiency beyond 70 % as well as a 120 MHz, 9 W LED driver with an efficiency up to 89 %. Both converters maintain high efficiencies over a wide load range.

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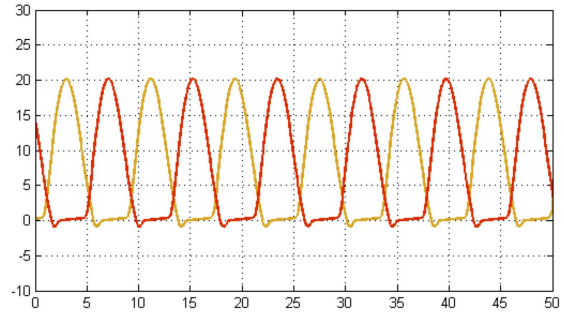
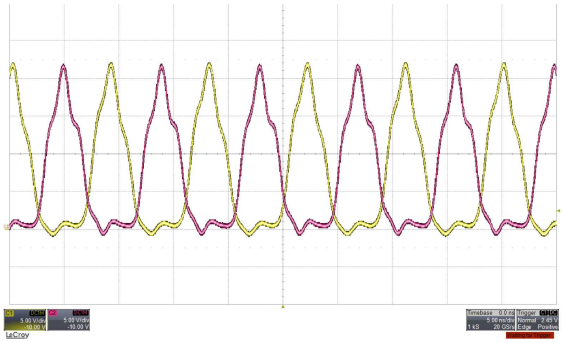


(a) simulated waveforms



(b) measured waveforms

Fig. 10: Drain-source waveforms of the two power switches in the interleaved converter from [43].

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Evolution of Very High Frequency Power Supplies

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***Abstract*—The ongoing demand for smaller and lighter power supplies is driving the motivation to increase the switching frequencies of power converters. Drastic increases however come along with new challenges, namely the increase of switching losses in all components. The application of power circuits used in radio frequency transmission equipment helps to overcome those. However those circuits were not designed to meet the same requirements as power converters. This paper summarizes the contributions in recent years in application of very high frequency (VHF) technologies in power electronics, shows results of the recent advances and describes the remaining challenges. The presented results include a self-oscillating gate-drive, air core inductor optimizations, an offline LED driver with a power density of $8.9\ \mathrm{W/cm^3}$ and a $120\ \mathrm{MHz}$, $9\ \mathrm{W}$ DC powered LED driver with $89\ \%$ efficiency as well as a bidirectional VHF converter. The challenges to be solved before VHF converters can be used effectively in industrial products are within those three categories: components, circuit architectures and reliability testing.**

***Index Terms*—VHF circuits, power conversion, DC-DC power converters, resonant inverters, zero voltage switching**

I. Introduction

The continuing trend of miniaturization in industrial and consumer electronics is continuously driving a demand for smaller power supplies. Weight and cost reduction demands accompany this trend. Within power supplies the major size, weight and cost drivers are typically the passive components. Increasing the switching frequency of power converters can reduce the size, weight and therefore the cost of those. For substantial size and weight reduction, the switching frequencies are increased up to the very high frequency (VHF) band ($30\ \mathrm{MHz}$ to $300\ \mathrm{MHz}$), which leads to a merge in circuit technologies used in radio frequency transmitters [1]–[6] and the classical power electronics circuits.

The VHF amplifiers are designed for DC-AC conversion, where the AC simultaneously is the switching frequency. Generally those circuits [1], [2] drive a known load impedance, typically a $50\ \Omega$ antenna. Traditionally the topologies used for those circuits have been characterized as classes with running labels following the alphabet. Class-A, class-B and class-C are described in [2], [7]. These classes are characterized through the relative amount of time, the power transistor is conducting the load current with respect to the period of the VHF signal. For class-A the transistor conducts the load current $50\ \%$ of the time. Class-B operates between $25\ \%$ and $50\ \%$ and class-C between $0\ \%$ and $25\ \%$. This leads to theoretical maximum achievable efficiencies of $50\ \%$, up to $78.5\ \%$ and up to $100\ \%$ for class-A, B and C respectively. Their power electronics counter parts are linear regulators. Class-D is described in [8] and the first power circuit topology, that allows for theoretical $100\ \%$ efficiency under all operating conditions. The equivalent are strictly all hard-switched power converters. Class-E as described in [3], [4] and class-F as demonstrated in [5], [6] correspond to all power converters, that apply zero voltage switching (ZVS) and zero-current switching (ZCS) techniques respectively.

Similarly to switch-mode power supplies, those VHF amplifiers convert the constant supply voltages into a high-frequent voltage by operating power semiconductors in the triode region only. The major difference is that VHF amplifiers do not convert the energy back into a constant voltage or current level. Numerous research works have been published [9]–[20], filling this gap and making VHF technologies available for power electronics. This paper describes the individual contributions of those in greater detail. However there are still some challenges left, before VHF switch-mode power supplies can relieve their advantages for products in industrial and consumer electronics.

This paper elaborates on the most recent advances, showing prototypes and measurement results in section II. Section III describes the remaining challenges based on previous work and characterizes them. Section IV concludes the paper.

II. Recent Advances

Recent research results enhanced the state-of-the art in VHF converters. Most of the work in recent years has focused on class-E derived topologies.

A. Optimal operation

The class-E based power circuits allow for a second degree of soft switching. Despite turning the power switches on, when the voltage across them is zero (ZVS), also the derivatives of these signals are taken into account. This is called ZdVS and ZdCS respectively. The technique has been applied to power converters in [19]. The schematic in Fig. 1 shows the adoption of the principles of a class-E oscillator, e.g. shown in [21]–[23], to a class-E based power self-oscillating VHF converter (DC-DC) [19], [24]. A converter achieving both ZVS and ZdVS at all times operates in optimal mode.

Other implementation replaced either the resonant tank [25],

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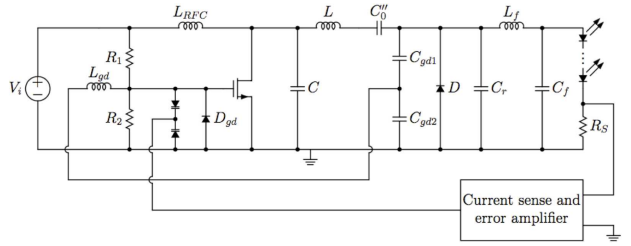

Fig. 1: Schematic of a self-oscillating VHF converter [24] with LED load.

[26] or the input inductor [11], [27] with a transmission line. The resulting waveforms of this circuit have been reported in e.g. [28]–[33] and Fig. from 2 repeats the simulated waveforms of this converter, where v_s and i_s are the voltage and the current across and through the switch and v_D and i_D are voltage and current across and through the rectifier diode. v_G is the control signal of the power switch and V_o and V_i are input and output voltages of the converter. The top graph v_s visualizes the optimization of the converter for both ZVS and ZdVS.

Fig. 3 is a photograph of the implementation of this converter. The overall efficiency of the 97 MHz converter is 55 %.

The advantage of this converter is, that it is based on a widely documented circuit topology from the communication electronics applications. As implemented here, it also provides means of output regulation. The downside is the voltage stress across the power switch, 3.6 times higher as in hard-switched converters.

B. Suboptimal operation

Due to the tight adjustment of the turn on instance of the power switch for achieving ZVS and ZdVS the degrees of freedom in this converter are low. That limits the input and output voltage ranges. Furthermore the efficiency is not acceptable. In this case, the majority of the losses are due to conduction losses in the power semiconductors, which are due to the on-resistance of the power switch. As the gate voltage is not significantly higher than the threshold voltage, the devices minimum on-resistance could not be achieved.

Suboptimal operation of class-E converters as described in [4] opened for higher degrees of freedom in the design of class-E based DC-DC converters. This means that the ZdVS condition is only fulfilled under nominal load conditions and only ZVS is fulfilled otherwise. The resulting converter waveform in the optimal and suboptimal operating regions are shown in Fig. 4. The effects of these operation mode as described in [34] have been extended in [20] to LED lighting applications.

Note that the body diode of the MOSFET is conducting in the beginning of the MOSFETs conduction period. This is due to wrong timing in the turn-on of the power device. The energy lost in the body diode ruins the efficiency of this particular converter.

Furthermore [20] provides a detailed analysis of the power components parasitics and the effect of their nonlinearities. The basis for this analysis has been, among others, laid in

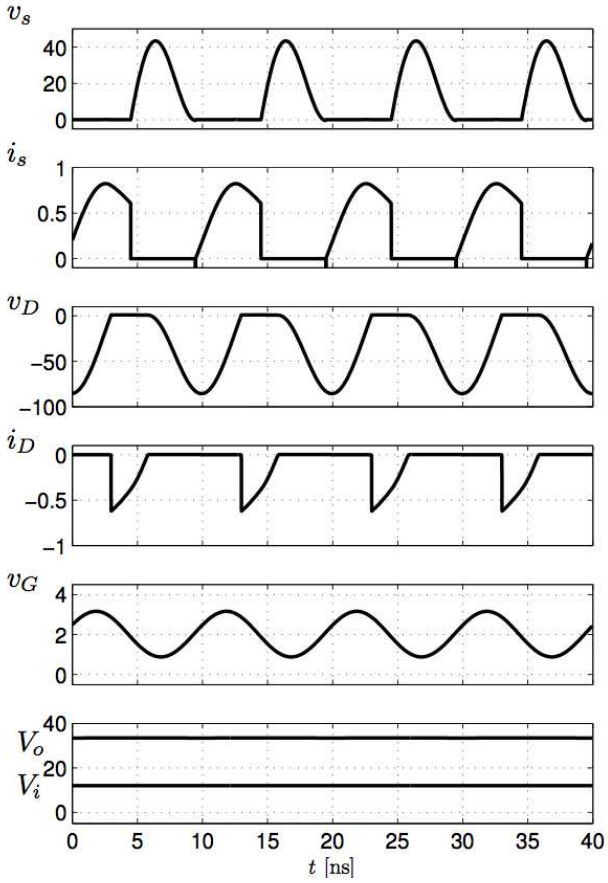

Fig. 2: Simulated waveforms for a ZVS and ZdVS class-E based converter from [19].

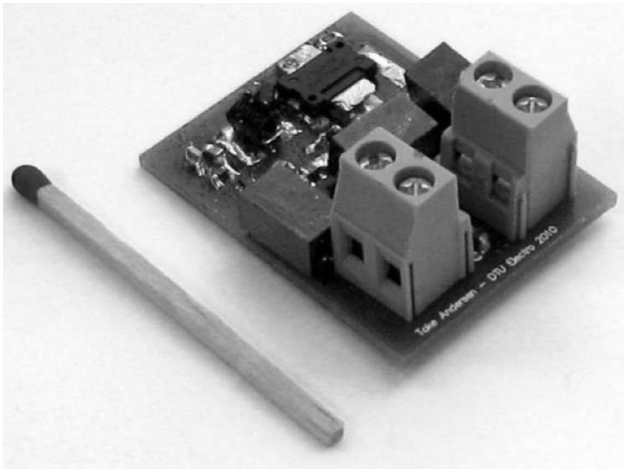

Fig. 3: Photograph of the self-oscillating VHF converter from [24].

[35], [36] for the analysis of class-E amplifiers, which is fully applicable to class-E based power converters when tuning the rectifier to act as a an ohmic load. The most relevant parasitics of the power switch are the input and output capacitances. The later is the most critical for the design of the converter.

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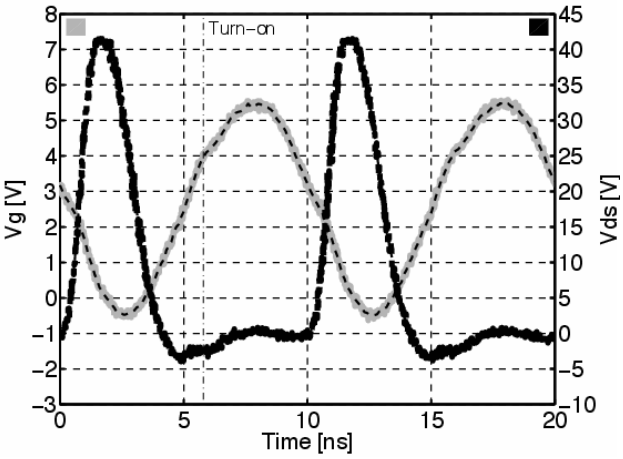
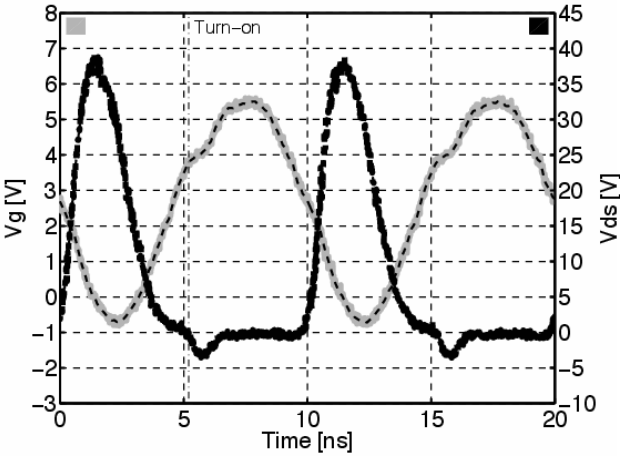


(a) optimal operation



(b) suboptimal operation

Fig. 4: Measurements of gate-source and drain-source voltages V_{gs} and V_{ds} of the power switch and the turn-on instances. Note that the drain-source voltage has an offset of -0.5 V, due to the oscilloscopes offset.

Simultaneously the output capacitance is highly nonlinear, which was taken into account in the analysis in [20]. There the nonlinearity of the output capacitance C_{ds} is modeled with (1)

$$C_{ds}(V_c) = \frac{C_{j0}}{(1+\frac{V_c}{V_{bi}})^{\gamma}}, \tag{1}$$

where

- C_{j0} is the junction capacitance at 0 V,
- V_{bi} is the built-in junction potential, typically $0.5-0.9$ V [29],
- γ is the junction sensitivity or gradual coefficient. Typically $\gamma = 1/3$ for gradient junctions, while $\gamma = 0.5$ for abrupt junctions [1] hence junction diodes [29], and
- v is the junction voltage.

This results in a voltage waveform V_c of the power switch as a function of the converters input current I_{in} and the above

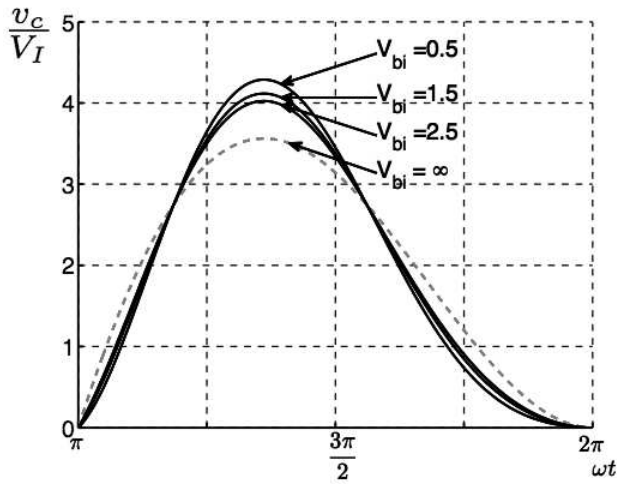


Fig. 5: Voltage waveform of the power switch in relation to DC input voltage for a nonlinear output capacitance from [20]. V_{bi} is the junction potential of the process.

output capacitances parameters as given in (2).

$$V_c = V_{bi}\left(\left[\frac{I_{in}(1-\gamma)}{\omega C_{j0} V_{bi}}(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t) + 1\right]^{\frac{1}{1-\gamma}} - 1\right) \tag{2}$$

Fig. 5 shows the relative voltage waveform of the power switch as a function of time and junction potential V_{bi} for a junction sensitivity of $\gamma = 0.5$.

The remaining components of the power stage have been investigated in [20] as well. Thereby most focus is on the inductors, as these are the most volume consuming parts, have the biggest weight and typically a big impact on the overall price of the converter. Therefore the inductors have been integrated as toroids into the printed circuit board (PCB). This process is described in [37] and Fig. 6 shows the principle.

A power stage has been designed to operate in suboptimal mode under consideration of the power switches nonlinear output capacitance. The converters efficiency is in the same area as the one presented in II-A and again limited by a high on-resistance, which is due to a low gate drive voltage.

While giving up on the single operating point operation in optimal operation mode, the suboptimal operating converters theoretically allows for different conduction angle operation on the cost of tighter timing to operate in ZVS.

C. Class-E based SEPIC converter

For dealing with the efficiency challenge, [38] compared a number of power switches both in simulation and experiment. Furthermore multiple air-core inductors where calculated, designed and implemented. An extraction is shown in Fig. 8. The prototypes reach Q-values beyond 100 and resonance frequencies up to 340 MHz. Fig. 9 shows a photograph of the implemented converters. On top of that an effective line- and load regulation scheme was realized in those. The designs where verified in a SEPIC converter (Fig. 7) [39], based on the topologies presented in [40], achieving a power density of

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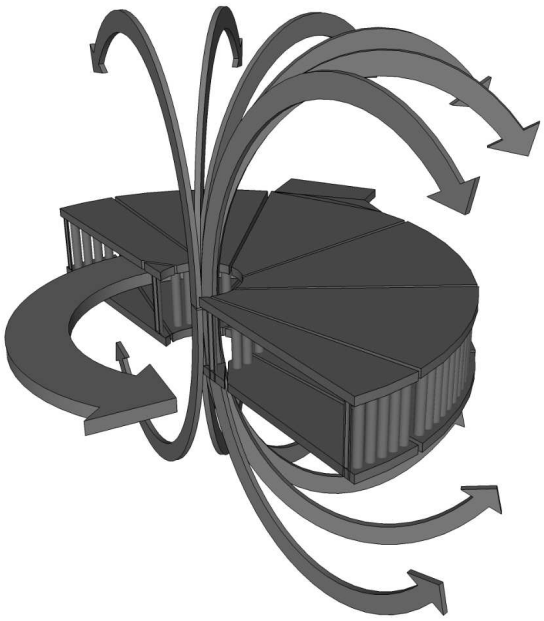

Fig. 6: PCB integrated inductor from [37]. The cross-section of the PCB toroid and the resulting flux arrows are shown.

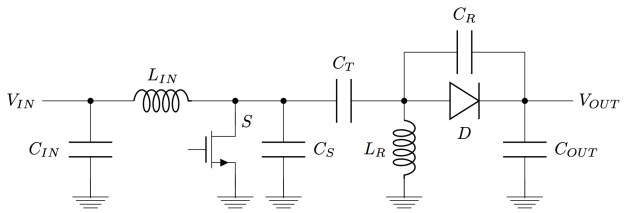

Fig. 7: Schematic of a class-E based SEPIC VHF converter [39].

Fig. 8: Photograph of various air core inductors [38].

$8.9\ \mathrm{W/cm^3}$ ($146\ \mathrm{W}/in^3$) by switching at $51\ \mathrm{MHz}$ for offline LED applications.

Fig. 10 shows the implementation of the final prototype with $70\ \mathrm{MHz}$ switching frequency. The voltage step-down ratio of the converters is 10 and the output power range is between 1 and $4\mathrm{W}$ at an efficiency within this range beyond $70\ \%$.

Compared to the above reported converters, the SEPIC converter is not based on an inverter that delivers a sinusoidal output. The later is crucial in telecommunication applications, when using the class-E inverter as a transmitter, but completely unnecessary demand as an intermediate VHF link within a DC/DC power converter. Relaxing this requirement removes the resonant tank inductor, and therefore the resonant tanks bandpass behavior. On the other hand the rectifier can no longer freely be chosen between several topologies, but has to be implemented with a diode, not referenced to ground, which is a disadvantage in some implementation technologies, such as integrated circuits.

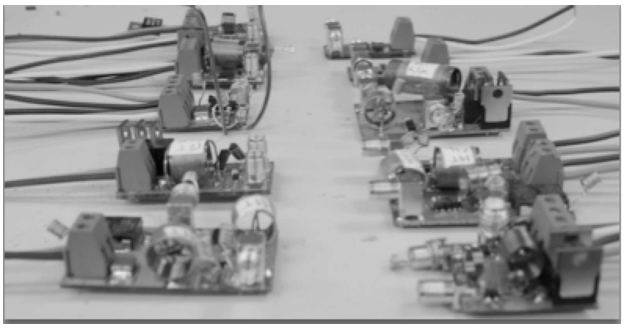

Fig. 9: Photograph of numerous prototypes for comparing measured efficiency with simulations [38].

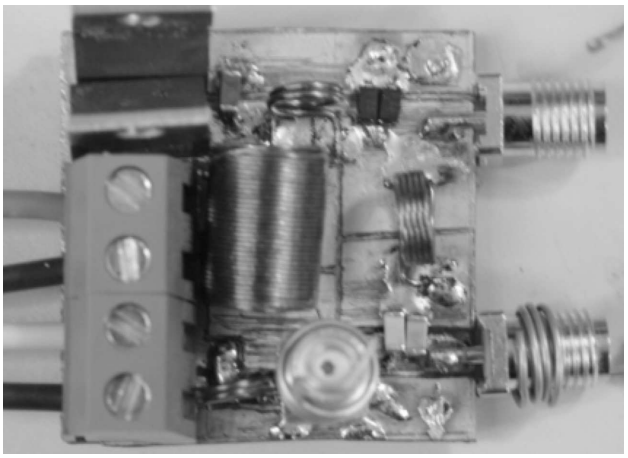

Fig. 10: Photograph of a closed loop low-power VHF converter with an efficiency beyond $70\ \%$ from [38]. The TO220 components in the upper left corner are the dummy load resistance.

D. Interleaved VHF converters

Additionally the self-oscillating principle from [19], [24] was combined with the interleave principle from [41], [42] in [43], resulting into a significant efficiency improvement. Interleaving two converter legs allows furthermore to use the ripple cancelation as described in [44] and applied in [41]. The complete schematic of the open loop implementation is shown in Fig. 11. The realized converter is switching at $120\ \mathrm{MHz}$, i.e. beyond the FM band, converts an input voltage between 6 and $9\ \mathrm{V}$ into an output current between 0.4 and $0.5\ \mathrm{A}$ and has an efficiency between 80 and $89\ \%$ within this operation range. The output power range is 3 to $9\ \mathrm{W}$, corresponding to an output voltage range between $7\ \mathrm{V}$ and $20\ \mathrm{V}$. The converter is designed to drive LEDs. Fig. 12 shows both a SPICE based simulation and a the measurement of the power switches voltage waveforms. Fig. 13 shows the efficiency graph of this converter.

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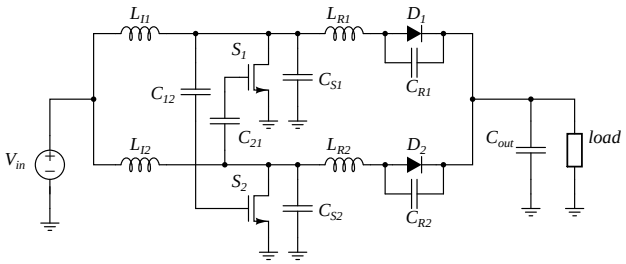
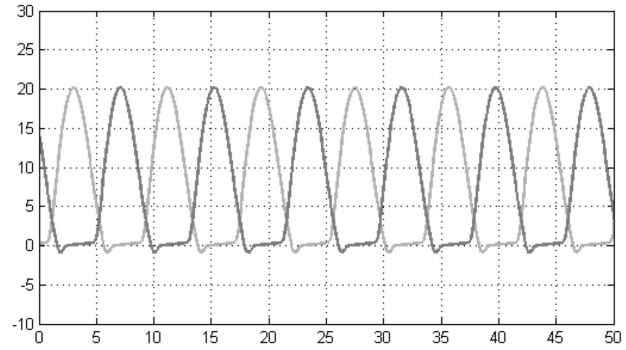
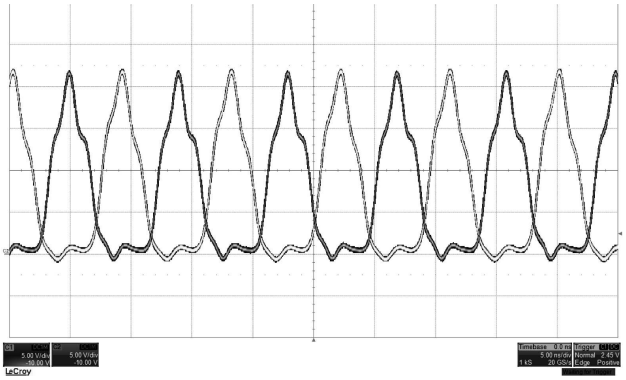


Fig. 11: Full schematic of the open-loop interleaved class-E converter from [43].



(a) simulated waveforms



(b) measured waveforms

Fig. 12: Drain-source waveforms of the two power switches in the interleaved converter from [43].

Interleaved converters allow for input and/or output ripple cancellation, segmented power stages, which enables higher power levels [45]. But those converters suffer from different optimal frequencies due to tolerances for each leg, which either might result in beat tones, when operating each of them at its own optimal resonant frequencies, or a non-optimal operation point with respect to efficiency for all legs, when operating all legs at the same frequency.

E. Bidirectional VHF converter

Replacing the diode in Fig. 1 with a transistor, the class-E amplifier and the class-E synchronous rectifier form a symmetric schematic as shown in Fig. 14. This was realized in [46] and resulted in a bidirectional converter with the same

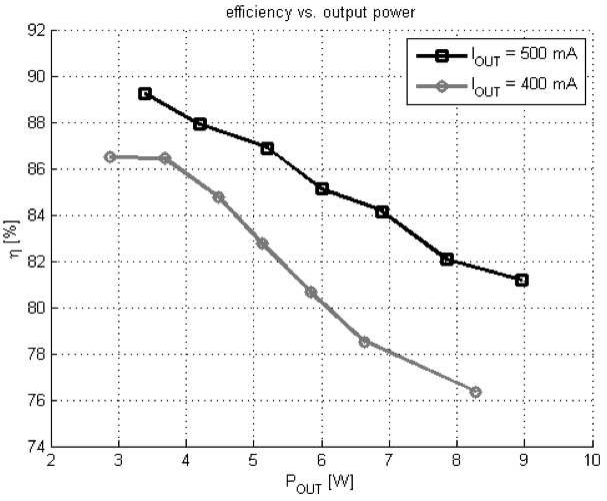


Fig. 13: Efficiency of a battery driven LED driver switching at 120 MHz [43].

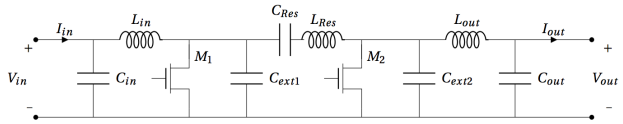


Fig. 14: Schematic of a VHF converter with class-E inverter and synchronous class-E rectifer [46].

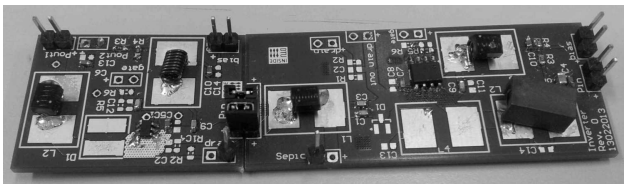


Fig. 15: Photograph of a bidirectional VHF converter [46].

conversion ration from both sides. Operating in the forward mode, the transistor M_1 is the power switch, operating in class-E mode, and M_2 is used as synchronous rectifier in class-E operation. In the reverse operating mode, the voltage designated V_{out} is acting as the input voltage and M_2 becomes the inverter switch, while M_1 turns into the synchronous rectifier. The maximum achieved efficiency with this topology was 70 % switching at 30 MHz. A photograph of the prototype and thermal pictures of the converter are shown in Fig. 15 and Fig. 16 respectively.

The bidirectional converter allows for lower conduction losses in the rectifier and allows for two-quadrant operation at the cost of an extra gate, which needs a control signal.

III. Challenges of VHF Converters

Lately remaining research challenges have been described in [47], [48] This section is summarizing the remaining challenges common in all above described converters with repect to implementation in products. It is dividing the major

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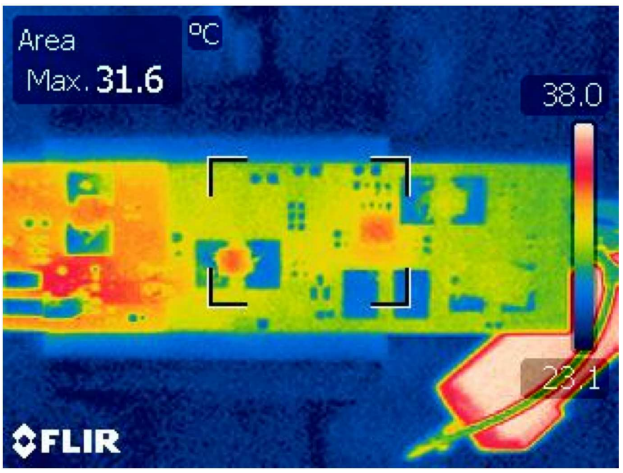
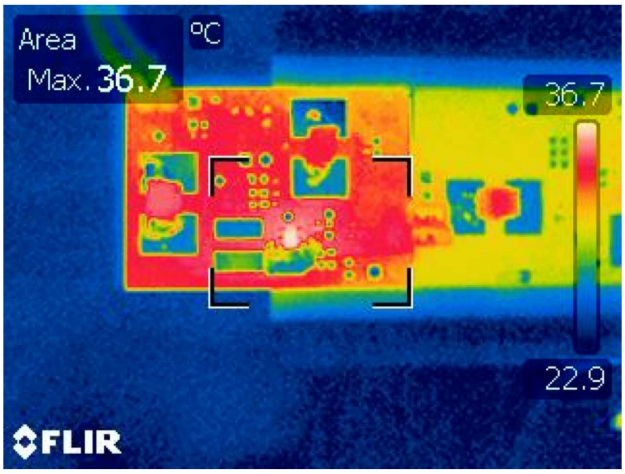


(a) class-E inverter



(b) class-E synchronous rectifier

Fig. 16: Thermal photographs of bidirectional VHF converter in thermal equilibrium [46].

remaining show stoppers into three categories and describes those afterwards with respect to existing products on the power supply market, with switching frequencies below the VHF range.

VHF operation of power supplies differs from sub-megahertz operated power supplies (here called traditional power converters) mainly by the following subjects:

- Electronic components, both active and passive,
- Circuit architectures for power stages and control parts,
- Adjacent behavior, such as electromagnetic compatibility (EMC), mechanics and other reliability tests.

A. Components

Especially inductive components are size, weight and cost optimization limitations in nowadays power circuits. Simultaneously VHF converters provide a major opportunity to overcome those.

Among the challenges are core losses, skin and proximity effect [27], [49]–[54]. For driving further miniaturization of VHF power supplies an obvious next step is to integrate the whole converter in a package (Power Supply in Package (PSiP)) or even on a single chip (Power Supply on Chip (PwrSoC)). The most challenging part for this goal is the integration of the inductors. Great progress has been made and summarized lately in [55], [56]. However realizations of integrated inductors with Q-values beyond 100 in the relevant frequency ranges remain to be seen. Hybrid concepts as shown in [57] might be applicable. Another challenge within passive components for VHF is the creation of a galvanic isolation barrier [58]–[60].

Despite passive components also active components, i.e. the power semiconductors, need to fulfill other requirements than in usual power supplies [61]–[63]. The parasitic components have a big influence on the design of the overall converter, as they are part of the design parameters. Unlike traditional power stages, the parasitic elements are therefore not considered undesired, but form an integral part of the stage. An example is the output capacitance C_{oss} of the power semiconductor in a class-E based power supply. According to [19] it is dependent on output power P_{out}, input voltage V_{in} and switching frequency f_{sw} as shown in (3).

$$P_{out} = 2\pi^2 f_{sw} C_{oss} V_{in}^2 \tag{3}$$

This means that the output capacitance C_{oss} is limiting the maximum switching frequency for a given application, which specifies P_{out} and V_{in}

B. Architectures

Where traditional power electronics circuits use square wave gate drive signals, the presented VHF converters so far utilized sinusoidal gate drive [18], [24], [64], [65]. This is mainly due to the input capacitance C_{iss} of VHF power semiconductors, which require a high peak current at extremely high speed. To consider the drive voltage trapezoidal its rise and fall times have to be less than 1 ns [65]. A trapezoidal or square wave drive would minimize the time of the power switch in linear operation and therefore decreases the losses.

The degrees of freedom in terms of modulation principles are less for VHF converters. Whereas power electronics circuits usually use pulse width modulation or phase modulation, the VHF converters efficiency is dependent on those parameters. Therefore they need to be adjusted statically to avoid losses by leaving the ZVS (or ZCS) range. A way to get around this is to apply burst mode control [17], [64], [66]. This method however introduces another low frequency component in the spectrum, which has to be buffered or filtered at both the in- and output of the converter. A requirement that enforces the use of bulky components and therefore is counterproductive to the intended advantages of VHF converters in the first place.

While the VHF converters offer good possibilities for fast transient regulations, their low frequency control performance is limited by intrinsic bandpass behaviors through serial capacitors. Even though some rectifiers are available with parallel capacitances and impedance transformation [19], [67], more suitable architectures are missing. Thereby it needs to be taken into account, that the original VHF power circuits are designed to match a defined load (typically the impedance of

the antenna) and therefore impedance transformation circuits can be realized in a passive way. Power converters however are connected to highly varying loads, i.e. load circuit in idle - drawing no energy from the supply - and full load - demanding the maximum output from the supply. Therefore active and lossless impedance matching circuits are required. Having such circuits at hand opens for utilization of the high gain bandwidth in VHF converters for line and load regulation.

C. Adjacencies

Lastly the interaction of VHF converters with its physical environment is different than the one of traditional power converters.

On one hand, the electromagnetic interaction between circuits increases, the higher the relevant frequencies are [68]–[71]. Fields are distributed easier both inside the converter and to its surroundings. The electrical behavior also becomes highly dependent on electromechanical interfaces, such as cooling and housing. However the harmonics of the resonant waveforms are falling faster, than the harmonics in hard switched traditional power converters [20]. Also the harmonics of the fundamental switching frequency are spaced wider. That means the distance can be used to place strategically important EMC bands, dependent on the application.

On the other hand, the carefully adjusted operating points of VHF converters (for efficiency purposes) are highly dependent on temperature [19], [20]. Adaptive mechanisms for ensuring optimal operation over industry standard temperature ranges are yet to come.

IV. Conclusion

The merge of techniques used in radio communication electronics and power electronics was pointed out. The development through the previous decades has been revisited and recent developments were summarized. Remaining challenges and the latest advances were described. The implementations of numerous VHF converters were presented. Among them are low-power, high-step-down converters with a switching frequency of $70\ \mathrm{MHz}$ and an efficiency beyond $70\ \%$ as well as a $120\ \mathrm{MHz}$, $9\ \mathrm{W}$ LED driver with an efficiency up to $89\ \%$. Both converters maintain high efficiencies over a wide load range.

The remaining challenges, that require solutions before VHF converters can be implemented in numerous industrial applications were found to be within the categorizes components, circuit architectures and reliability testing.

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Low Power Very High Frequency Resonant Converter with High Step Down Ratio

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***Abstract*—This paper presents the design of a resonant converter with a switching frequency in the very high frequency range (30-300MHz), a large step down ratio and low output power. This gives the designed converters specifications which are far from previous results. The class E inverter and rectifier have been selected for the prototype and the circuits are analyzed and simulated. Three different power stages are implemented based on different design parameters. The first prototype is with a switch with small capacitances, the second one is with a switch with low on resistance and the last one is with a large input inductor. The power stages are designed with the same specs and efficiencies from $60.7-82.9\%$ are achieved.**

I. Introduction

When designing power converters it is always a goal to reduce the price and the physical size, i.e. increase the power density. The development of Switch Mode Power Supplies (SMPS) has made it possible to increase the power density significantly, but it is limited by the size of the passive energy storing components (inductors and capacitors). The value and size of these is however dependent on the switching frequency. By increasing the switching frequency it will hence be possible to reduce the size of SMPSs further.

Traditional SMPS topologies like Buck and Boost are hard switching, this means the MOSFET is switching while energy is stored in the output capacitance. The result is that energy is dissipated in the MOSFET every time it turns on. Although this introduces losses in the converter, it is not critical for converters switching at $50-400kHz$. But when the frequency is increased to the Very High Frequency (VHF) range ($30-300MHz$) the dissipated power get almost 1000 times larger. This amount of energy would ruin the efficiency and require extreme cooling of the MOSFET. This leads to the development of resonant converters.

In order to avoid switching losses and be able to increase the frequency while keeping the efficiency high, new topologies have to be used. For the last two decades (since 1988 [1]) research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for DC/DC converters. With this type of converters it is possible to achieve Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS). In this case the MOSFET turns on when the voltage and/or current across/through it is zero. Theoretically this should eliminate switching losses if the switching is done instantaneously and at exactly the right time. This is not practically achievable, but even with slight deviations from the ideal case very high efficiencies can be achieved.

Increasing the switching frequency has several benefits beside reducing the size. As already mentioned the size of the passive components depends on the switching frequency. This gives a reduction in size, but also in cost as smaller components are generally cheaper. If the frequency is increased enough, some of the components can even be left out as they can be constituted by the parasitic parts of other components (this will be explained further in section II and III). An increase in switching frequency will also make it easier to comply with EMI requirements, as switching harmonics can easily be filtered out by small and cheap filters.

With a switching frequency in the VHF range, it will also be possible to achieve very fast responses. However in order to fully benefit from this, an efficient and fast control loop has to be implemented. This still seems to be a big challenge as some of the best results are still achieved using burst mode (or cell modulation) as in [2], [3]. Due to the high switching frequency the converter will reach steady state after just a few μs, this makes it possible to use an array of small converters and switch them on and off as needed. In this way each converter is designed to operate with a defined load/output. This makes the design much easier as resonant inverters are generally very load depended.

The fact that resonant inverters are load depended, makes it very hard to achieve good performance at varying loads. Furthermore resonant inverters need a large load impedance to operate in the ideal situation (having both ZVS and ZCS). This makes them well suited for boost type converters, but making a buck type is a bit more challenging. The most commonly used way to overcome this challenge is to add an autotransformer at the output, in that way the load impedance seen by the inverter is increased [2], [4], [5]. Another way to achieve low output voltage is to use an array of converters with the input in series and the output in parallel as in [6].

The most commonly used inverter is the class E, however several other topologies exist. Some of the research results are summed up in table I. From the table it is seen that very high efficiencies are achievable for the inverters, up to 97%. However for the complete converters the efficiency drops around 10%, with a maximum at 91%.

From table I it is also seen that the converters have limited

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TABLE I
RESULTS FROM PREVIOUS RESEARCH

Inverters

Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class DE	5.3	330	N/A	1154	89	1999 [7]
Class E	1	128	N/A	366	96.6	2006 [8]
Class ϕ_2	1	129	N/A	526	97.1	2006 [8]
Class ϕ_2	30	160	N/A	330	93.7	2007 [9]
Class E	1	129	N/A	322.7	97	2007 [10]
Class E	100	9	N/A	6.8	82	2011 [11]

Converters

Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class E	1	20	25	8.9	89	1989 [12]
Class ϕ_2	30	165	33	265	87	2006 [2]
Class E	100	11	12	10	75	2006 [13]
Class ϕ_2	30	150	33	180	84	2008 [4]
Class ϕ_2	10	170	75	250	91	2009 [5]
Class ϕ_2	30	165	33	225	87	2009 [5]
Class ϕ_2	30	330	50	900	79	2009 [6]
Class E	100	12	23.7	1.7	55	2010 [14]
Push-Pull ϕ_2	30	140	65.4	471.9	83.4	2010 [15]

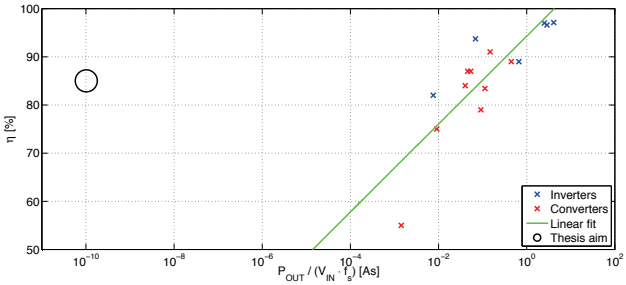

Fig. 1. Relation between $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$ and η.

gains, with a step down of 6.6 times and an step up of 2 being the largest. As already stated the large reductions are not produced solely by the converter, but with different ways to make the load impedance appear larger. By further inspection a connection between $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$ and η can be seen, this relation is shown in figure 1. It seems that it is problematic to have a high input voltage and switching frequency while having a low output power and still keep the efficiency high.

This paper will cover the design of a VHF power converter with a low voltage and power output. This will require a huge reduction in voltage and a combination of output power, input voltage and switching frequency unlike any of the previous results. This will put the converter in the area marked in figure 1, as it is seen this is very far from the results achieved by previous researchers (the specs for the converter is given in table II).

TABLE II
DESIGN SPECIFICATION FOR THE CONVERTER.

f_S	V_{IN}	V_{OUT}	P_{OUT}	R_L
$30-300MHz$	50V	5V	1W	25

As the load is given it is believed that the first step should be to design the rectifier and then design the inverter for the given input and load. It is also possible to design the inverter to a given load and then use different resistance compression networks to make the impedance of the rectifier match [16], [17], [18]. Though this is a solution often used, it is believed that it will increase the complexity of the converter unnecessarily and possibly reduce the achievable efficiency, size, and price.

Section II will cover the selection and design of a resonant rectifier for the given load and output power level. Then a resonant inverter will be designed for the input voltage and load impedance in section III. Experimental results from three different power stages will be shown in section IV. Finally section V summarises and concludes the paper.

II. RESONANT RECTIFIERS

The purpose of the rectifier is to convert the AC current from the inverter to a DC output. Just as the MOSFET has an output capacitance, the diode has a junction capacitance. In order not to burn this energy in the diode, it is important that the transition is made smoothly, so the capacitance is discharged before the diode turns on.

As stated in section I, it is difficult to achieve high efficiency if the input voltage and switching frequency are high and the output power low. The switching frequency is therefore set to 30MHz for the initial design. If good results are achieved with this frequency, it might be increased further in order to minimize the converter.

Though there are several ways to do this, only the most commonly used class E rectifier will be considered here. The class E rectifier is a rather simple circuit, consisting of a diode, two capacitors, and an inductor as shown in figure 2.

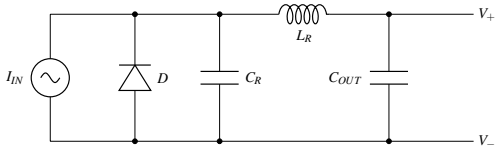

Fig. 2. Schematic of the class E rectifier.

For now it will be assumed that the output capacitance is infinite, so the output voltage is constant, and the diode is assumed to be ideal, i.e. no forward voltage drop, no junction capacitance and no reverse current.

In this case the rectifier will appear resistive at the switching frequency, if the resonance frequency of L_R and C_R are set to this frequency. This will make the design of the inverter a bit simpler, as most design formulas are for a resistive load.

The scaling of the two components will determine the duty cycle of the diode, D_D. As the forward voltage drop of a diode increases with the current running through it, it is desirable to keep D_D as high as possible. However as the diode is connected to the output through an inductor, the average

voltage across it has to be V_{OUT}. Hence a high D_D will lead to a high peak voltage across the diode.

In order to select D_D, and thereby the scaling of the resonating components, the values of real components has to be considered. All the considered inverters has a capacitor at the output insuring a pure AC path, without this there would be a direct DC path from input to output and it would be impossible to reduce the voltage. The average current through the diode, will therefore be the same as the output current.

With the forward voltage drop of a standard schottky diode being around $0.5V$ (10% of the output voltage), it is crucial to use a diode with low forward voltage drop. Fairchilds MBR0520L has one of the lowest forward voltages availible, max $385mV$, and can handle a reverse voltage of $20V$. With this diode, the diode loss will be up to $77mW$ or 7.7% of the output power. This clearly limits the maximum achievable efficiency and fits very well with the $\approx 10\%$ efficiency drop, seen in section I when going from an inverter to a complete converter.

A way to reduce the losses could be to use a synchronous rectifier, this will eliminate the forward voltage loss. This will however require an additional MOSFET, with the following need for gate drive and control.

If $D_D = 0.5\%$ is chosen, the peak diode voltage will be $3.562 \cdot 5V = 17.81V$ leaving a little margin up to the maximum. With this D_D the value of C_R should be $67.5pF$ and the value of L_R should be $417nH$ [19].

The inductor and output capacitor composes a 2nd order lowpass filter. In order to get maximum 1% (or $50mV$) ripple at the output, the 20V AC needs to be attenuated by $52dB$ which leads to a cut of frequency of $1.5MHz$ and a output capacitance of $27nF$.

The inductor has, as expected, a DC current of $0.2A$ (the output current with 1W and 5V) and on top of that an AC current with an amplitude of $120mA$. The DC resistance of the inductor is estimated to $25m$ and the AC resistance to $330m$ (these values are based on an air core inductor with a diameter of $6mm$ and 8 turns of $0.4mm$ wire). The loss caused by the inductor can then be calculated to $1mW$ due to DC losses and $2.4mW$ due to AC losses.

This is 0.34% of the output power and these resistances are based on a relatively large air core inductor. The Equivalent Series Resistance (ESR) of ceramic capacitor in the sizes used here, will be less than $200m$ [20] and the currents running through them are smaller than than the current in the inductor. The loss caused by them will thus not be significant. Furthermore the parasitic capacitance of the diode can account for C_R. Actually the parasitic capacitance of the chosen diode is $65pF$ at $5V$ reverse voltage fitting almost perfectly with the calculated value.

To sum up, the class E rectifier is a simple circuit which can be made of only 3 components. The selection of the diode is crucial in order to get a decent efficiency and even with the best diodes available, the diode losses will be significant. But as long as an inductor with low ESR is chosen, the total loss in the rectifier should be below $100mW$.

III. Resonant inverters

As mentioned in section I, a resonant inverter is used in order to eliminate switching losses. Either ZVS or ZCS can be achieved and in some special cases both. Generally ZVS will eliminate losses due to parasitic capacitances and ZCS will eliminate losses due to parasitic inductance. For MOSFETs and diodes in power applications the capacitances causes the dominating loss, ZVS will therefore be the main criteria.

However in some cases it is, as mentioned, possible to achieve both ZVS and ZCS switching (also called ZVS and zero slope switching, ZDS). If this can be achieved the exact timing of the switching is less important, as the voltage across the MOSFET will be zero for a small amount of time.

If only ZVS can be achieved, the MOSFET needs to turn on, at exactly the point where the voltage across it hits zero. If it switches just a little to early, there will be energy stored in the capacitor causing switching losses. If it switches a little too late, the drain source voltage will go below zero and the body diode will start to conduct which also gives losses.

The most commonly used resonant inverter is the class E, a schematic of it is shown in figure 3. It consists of a single MOSFET, two inductors, and two capacitors. In optimum operation L_{IN} is an infinite choke providing a pure DC input current. The resonant circuit (L_{RC} and C_{RC}) are inductive at the switching frequency and the inverter is designed to have both ZVS and ZDS.

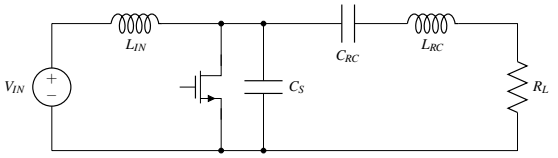

Fig. 3. Schematic of the class E inverter.

As already mentioned ZVS and ZDS switching can only be achieved in very specific situations. According to [22] and [23] this can only be achieved if:

$$R_L = \frac{8}{\pi^2 + 4} \cdot \frac{V_{IN}^2}{P_{OUT}}$$
$$f_{S,max} = \frac{P_{OUT}}{2 \cdot \pi \cdot C_S \cdot V_{IN}^2} \quad (1)$$

With $50V$ input, $1W$ output, and a switching frequency of $30MHz$, this would require a load impedance of $1.44k$ and an output capacitance of $2.1pF$. From equation 1 it is seen that there is a special combination of f_S, V_{IN} and P_{OUT} which makes it possible to operate in the optimum situation. Similar equations can be found for other topologies [22] and this is the reason for the dependence seen in figure 1.

A MOSFET with an output capacitance of $2.1pF$ for this voltage level and switching frequency is not available, they have minimum 10 times that. Furthermore the impedance is very far from the input impedance of the rectifier. It will therefore not be possible to achieve both ZVS and ZDS switching. However it is still possible to achieve ZVS and thereby

high efficiency as long as the transitions of the MOSFET is controlled well.

If the drain source voltage of the MOSFET is assumed to be a half sine wave when it is off and zero when it is on, the peak voltage across the MOSFET will be:

$$V_{IN} = \int V_{DS} = V_{DS,peak}\frac{2\cdot(D-1)}{\pi}$$
$$\Updownarrow$$
$$V_{DS,peak} = V_{IN}\frac{\pi}{2\cdot(D-1)} \quad (2)$$

The RMS value of a half wave rectified sine wave is:

$$V_{DS,rms} = V_{DS,peak}\sqrt{\frac{D}{2}} \quad (3)$$

And the RMS value of the output voltage is:

$$V_{OUT,rms} = \sqrt{P_{OUT}\cdot R_L} \quad (4)$$

According to [2] the reactance of the resonance circuit can now be determined by:

$$X_{RC} = R_L\cdot\sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1} \quad (5)$$

By combining equation 2, 3, 4, and 5, an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained:

$$X_{RC} = R_L\cdot\sqrt{\frac{V_{IN}^2\cdot\pi^2\cdot D}{2\cdot(2\cdot D-2)^2\cdot P_{OUT}\cdot R_L} - 1} \quad (6)$$

It is desirable to keep the duty cycle low in order to reduce the peak voltage across the MOSFET. However due to turn on and off times and delays, it is decided to keep it close to 50%. From equation 2 it is found that a duty cycle of 45% will give a peak voltage of $142.8V$, leaving a little headroom if a $150V$ MOSFET is used. Using this value along with the previous results the needed reactance is found to be 326 . If a capacitor of $680pF$ is used, the value of the inductor becomes $1.77\mu H$.

The next step is to determine the values of L_{IN} and C_S. In order to minimize losses it is preferable to keep L_{IN} large, thus large AC currents running in and out of the converter and thereby causing unnecessary losses are avoided. If the input choke is assumed infinite, the next step is to calculate the value of C_S. C_S and the resonance circuit should resonate at a frequency with a period of:

$$T_R = 2\cdot(1-D)\cdot T_S \Leftrightarrow f_R = \frac{f_S}{2\cdot(1-D)}$$

If the reactance of C_S is the same as the reactance of the resonant tank (with opposite operational sign) at f_R the circuit will resonate at this frequency. However as the capacitor is only used when the MOSFET is off, it has to be scaled by 1-D:

$$C_S = \frac{1-D}{2\cdot\pi\cdot f_R\cdot X_R} \quad (7)$$

With the specifications for this converter this would require a MOSFET with an output capacitance of maximum $10.9pF$. At the moment the MOSFETs with lowest output capacitances, C_{OSS}, which are able to switch in the MHz range and handle $150V$, has an output capacitance of $\approx 20pF$ at 50V. It is therefore necessary to reduce the input inductor in order to increase C_S. The effective capacitance of the output capacitor is $\frac{C_S}{1-D} = 36.4pF$, hence the total inductance of the resonance circuit and the input inductor should be $936nH$. Knowing the values of L_{RC} and C_{RC} the input inductance can be calculated to $2.91\mu H$.

From a simulation the RMS current through the inductors and the MOSFET is found to be; $I_{IN,rms} = 102mA$, $I_{FET,rms} = 165mA$ and $I_{OUT,rms} = 208mA$.

If the MOSFET has a $R_{ON,max} = 1.2$, this will give a conduction loss in the MOSFET of up to 33mW. The AC resistance of the inductors is estimated to $100m$, thus they will have a combined loss of 5.37mW. As for the rectifiers the losses in the capacitors are assumed to be negligible. Thus the total loss in the class E inverter is estimated to $\approx 38mW$.

The complete circuit with the class E inverter and class E rectifier can be seen in figure 4. With the loss calculated for the two parts the combined efficiency will be 88% excluding gate drive and gateing losses.

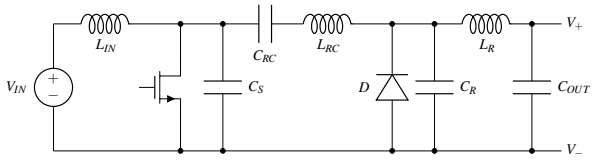

Fig. 4. Schematic of the class E inverter and class E rectifer.

IV. Experimental results

In section III the IRF5802 MOSFET were introduced and used for calculations and loss estimates. However several MOSFETs which can be used for this application exist, two of the best suited are compared in table III.

TABLE III
COMPARISON OF MOSFET CHARACTERISTICS
($R_{ds(on)}$ AT $V_{GS} = 10V$ AND CAPACITANCES AT $V_{DS} = 50V$).

Component	V_{DSS}	I_D	$R_{DS(on)}$	C_{ISS}	C_{OSS}
FDN86246	$150V$	$0.9A$	1.2	$85pF$	$18pF$
IRF5802	$150V$	$1.6A$	$359m$	$180pF$	$28pF$

In section III an output capacitance of $10.9pF$ was found ideal. As the voltage waveform across the MOSFET and C_S is given by V_{IN}, f_S and D, the currents (and thereby losses) in L_{IN}, C_S and the MOSFET scales with the value of C_S. It is therefore desirable to keep the value of C_S as close to this as possible in order to achieve high efficiency.

Comparing the two MOSFETs, the FDN86246 has much lower on resistance than the IRF5802. However the output

capacitance is higher and will as mentioned increase the currents and thus reduce the benefit of the low on resistance. Assuming the waveform across the MOSFET is the same using the two MOSFETs, the current using the FDN86246 will be $\frac{C_{FDN86246}-C_{IRF5802}}{C_{IRF5802}} = 142\%$ larger than using the IRF5802. The on resistance will be reduced by $\frac{R_{IRF5820}-R_{FDN86246}}{IRF5802} = 70.1\%$. Combining this gives a total loss reduction of 27.4%, using the estimated loss found in section III this correspond to $9mW$. Furthermore the increased current will also give losses in the input inductor, again using the estimate from section III the increased loss is found to $1.42 \cdot 5.37mW = 7.63mW$. Hence the total loss difference using the two MOSFET is estimated to be less than $2mW$. The increased capacitance will however also make the timing of the switching more important, as a larger amount of energy will be stored in the capacitor and burned in the MOSFET if the switching is just a little wrong.

Based on the analysis above, the MOSFET from IRF are found most suited. But as they are very close, prototypes using both will be made to compare them further.

This next subsections will cover the results obtained with three different power stages. The first power stage is the one which has been designed in the previous sections, the second power stage is with the MOSFET with lower $R_{DS(ON)}$ and the last power stage is with a large input inductor and higher output power, this should, as described in section III, give a higher efficiency.

A. MOSFET with low C_{OSS}

A power stage with the components selected in sections II and III was implemented. Just as the case were when going from calculated values to simulations, slight adjustments had to be made. The tuning procedure was, first to tune the inductor in the output filter to make it resistive at the switching frequency. Once that was done, the inverter was added to the design and a low voltage was applied. It was seen that the converter was not ZVS switching as the output capacitance of the MOSFET was not discharged when it switched on.

In order to get it to discharge faster the values of the input and resonant inductors had to be lowered. First the resonant inductor was lowered to give the desired output power and then the input inductor was adjusted to make the converter ZVS. As the output capacitance of the MOSFET is $20pF$, measuring with a probe with $10pF$ capacitance changes the switching a lot. This ruins the tuning and ZVS is thus not achieved, some waveforms have been measured and they are shown in figure 5. As it is seen the drain voltage has a small break when the MOSFET is switched on, this is due to the $10pF$ added by the probe.

So for the final fine tuning a thermal camera was used to measure the temperature of the MOSFET, it was then assumed that the MOSFET was ZVS when the temperature rise was lowest. Even though this is not a solid proof of ZVS, a low temperature rise comes from low power loss and thus the best tuned circuit. The efficiency was measured to 71.5% (see table IV).

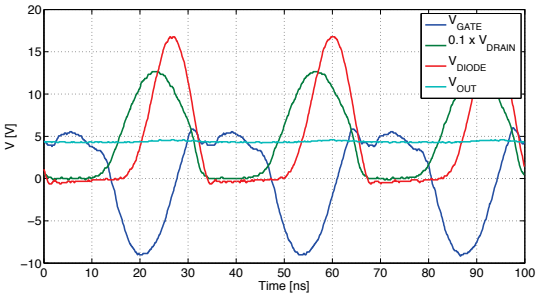

Fig. 5. Measurements on the prototype with low C_{OSS}.

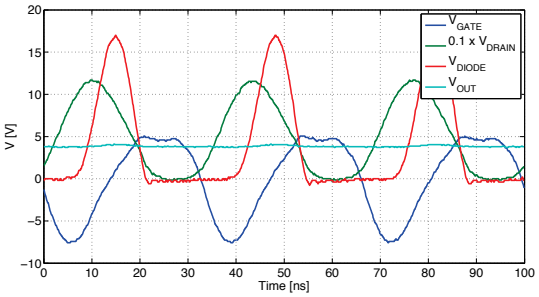

Fig. 6. Measurements on the prototype with large input inductor.

B. MOSFET with low R_{ON}

When the MOSFET was selected, the FDN86246 was found to be equally good to the IRF5802. The biggest difference between the two was on resistances and parasitic capacitances. A prototype was implemented using the FDN86246 in a circuit almost identical to the one used for the previous converter. A few turns was removed from the input inductor in order to make the converter ZVS with the increased output capacitance.

Due to the higher output capacitance more energy is stored and if the switch is switched at a few volts instead of zero, much more energy will be burned in the on resistance. Furthermore the AC current in the input inductor is larger which also increases the losses. The total efficiency of the converter was measured to 60.7%.

C. With large input inductor

As explained in section III, the highest efficiency should be achieved with a large input inductor (DC input current). To test this a prototype was made with the IRF5802, but this time with a $6.5\mu H$ input inductor. Then the resonance circuit and the load was adjusted in order to get ZVS and $5V$ output.

The increased output power makes the current through the MOSFET closer to that seen for the ideal class E inverter. Thereby the loss due to slight deviations in the timing of the switching becomes smaller.

The waveforms shown in figure 6 clearly shows that the converter is not ZVS when probes are placed at the gate and drain. Furthermore the voltage drops below $4V$, however removing the probes makes the output voltage increase to $5.0V$.

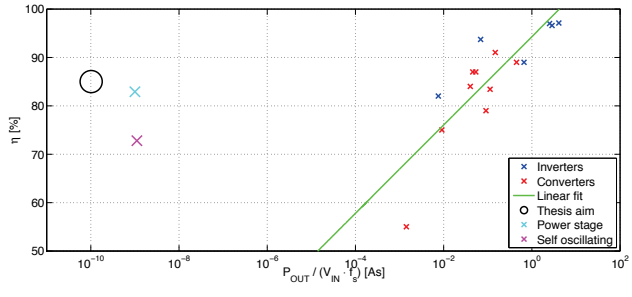

Fig. 7. The achieved $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$-factor and η next to previous results.

When tuned, the output power of the circuit became 1.53W and the efficiency was measured to 82.9%. This efficiency is without gate drive, but it is still among the best results achieved by previous researchers. Furthermore the $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$-factor explained in section I is much smaller than for any of the previous converters.

D. Summary of experimental results

The efficiency achieved for the three power stages is shown in table IV. From the three prototypes it is seen that good efficiencies can be achieved just by having ZVS. However the larger the current through the MOSFET is at the switching instant, the more important becomes the timing of the switching and losses increase.

TABLE IV
MEASUREMENTS ON POWER STAGES.

Converter	f_S [MHz]	I_{IN} [mA]	V_{OUT} [V]	R_L [ ]	η [%]	T_{Mos} [°C]	T_{Dio} [°C]
Low C_{OSS}	30	28	5.00	25	71.5	55.3	52.2
Low R_{ON}	29	32	4.93	25	60.7	65.1	53.2
Large L_{IN}	30	37	5.00	16.3	82.9	46.2	50.5

It has been shown that VHF converters with a very low $\frac{V_{IN}^2 \cdot f_S}{P_{OUT}}$-factor can be made with high efficiency, the best even had an efficiency of 82.9% which puts it among the best VHF converters. For comparison the results achieved for the power stages are shown i figure 7. The efficiency is not as high as wanted and the factor is a little lower than desired for one of the prototypes due to the higher output power. However seen next to previously achieved results they are very close.

V. CONCLUSION

The theoretical design of the resonant converter was considered in section II and III. Several different topologies were considered and based on complexity and efficiency estimates a class E inverter and rectifier was chosen.

Three different power stages were made; one with a MOSFET with the lowest available output capacitance, one with a MOSFET with low on resistance, and one with increased output power allowing a large input inductor. All the converters had 50V input and 5V output and the achieved efficiencies were between 60.7% and 82.9%. This shows that it is possible to make low power very high frequency converters with high step down ratio.

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Low Power Very High Frequency Switch-Mode Power Supply With 50 V Input and 5 V Output

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***Abstract*—This paper presents the design of a resonant converter with a switching frequency in the very high frequency range (30–300 MHz), a large step down ratio (ten times), and low output power (1 W). Several different inverters and rectifiers are analyzed and compared. The class E inverter and rectifier are selected based on complexity and efficiency estimates. Three different power stages are implemented; one with a large input inductor, one with a switch with small capacitances, and one with a switch with low on-resistance. The power stages are designed with the same specifications and efficiencies from 60.7–82.9% are achieved.**

***Index Terms*—DC-DC power conversion, inverters, rectifiers, resonant power conversion, switched mode power supplies, VHF circuits.**

I. Introduction

WHEN designing power converters it is always a goal to reduce the price and the physical size, i.e. increase the power density. The development of switch mode power supplies (SMPS) has made it possible to increase the power density significantly, but it is limited by the size of the passive energy storing components (inductors and capacitors). The value and size of these are however dependent on the switching frequency. By increasing the switching frequency it will hence be possible to reduce the size of SMPSs further.

Traditional SMPS topologies like Buck and Boost are hard switching, this means the MOSFET is switching while energy is stored in the output capacitance. The result is that energy is dissipated in the MOSFET every time it turns on. Although this introduces losses in the converter, it is not critical for converters switching at 50–400 kHz. But when the frequency is increased to the very high frequency (VHF) range (30–300 MHz) the dissipated power get almost 1000 times larger. This amount of energy would ruin the efficiency and require extreme cooling of the MOSFET. This leads to the development of resonant converters.

In order to avoid switching losses and be able to increase the frequency while keeping the efficiency high, new topologies have to be used. For the last two decades (since 1988 [1]), research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc/dc converters, see Fig. 1. With these type of converters, it is possible to achieve zero voltage switching (ZVS) and/or zero current switching (ZCS). In this case, the MOSFET turns ON when the voltage and/or current across/through it is zero. Theoretically, this should eliminate switching losses if the switching is done instantaneously and at exactly the right time. This is not practically achievable, but even with slight deviations from the ideal case very high efficiencies can be achieved.

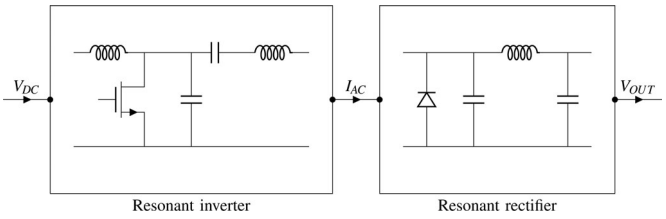

Fig. 1. Block diagram of the converter.

As already mentioned the value of the passive components depends on the switching frequency. Hence, an increase in frequency will lead to a reduction in size, as long as the size of the passive scales with the value. This assumption generally holds, but magnetic materials and packaging introduce some challenges. When the frequency is pushed far into the meghertz range, magnetic core losses increase rapidly and become unacceptably high for most core materials [2]. At this point, air core and PCB embedded inductors become a viable solutions, as the inductances needed at these frequencies can be made in a small physical size and the core losses avoided [3], [4].

Increasing the switching frequency also leads to capacitors with lower values. Electrolytic capacitors which often limit the overall lifetime [5], [6] can hence be avoided. The reduction in component values also leads to a cost reduction as smaller components are generally cheaper. If the frequency is increased enough, some of the components can even be left out as they can be constituted by the parasitic parts of other components (this will be explained further in Sections II and III). An increase in switching frequency will also make it easier to comply with EMI requirements, as switching harmonics can easily be filtered out by small and cheap filters.

With a switching frequency in the VHF range, it will also be possible to achieve very fast transient responses [7] which are highly demanded, e.g., for envelope tracking [8]. However, in order to fully benefit from this, an efficient and fast control loop has to be implemented. This is a big challenge and while some ways of achieving continuous regulation have been found [9], [10], the best results are still achieved using burst mode (or cell modulation) as in [11]–[13]. Due to the high switching

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TABLE I
RESULTS FROM PREVIOUS RESEARCH

Inverters

Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class DE	5.3	330	N/A	1154	89	1999 [17]
Class E	1	128	N/A	366	96.6	2006 [18]
Class ϕ_2	1	129	N/A	526	97.1	2006 [18]
Class ϕ_2	30	160	N/A	330	93.7	2007 [19]
Class E	1	129	N/A	322.7	97	2007 [20]
Class E	100	9	N/A	6.8	82	2011 [21]

Converters

Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class E	1	20	25	8.9	89	1989 [22]
Class ϕ_2	30	165	33	265	87	2006 [11]
Class E	100	11	12	10	75	2006 [23]
Class ϕ_2	30	150	33	180	84	2008 [14]
Class ϕ_2	10	170	75	250	91	2009 [15]
Class ϕ_2	30	165	33	225	87	2009 [15]
Class ϕ_2	30	330	50	900	79	2009 [16]
Class E	100	12	23.7	1.7	55	2010 [24]
Push-Pull ϕ_2	30	140	65.4	471.9	83.4	2010 [25]

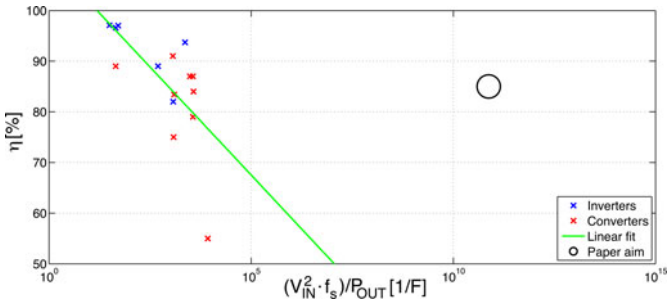

Fig. 2. Relation between $\frac{V_{\rm IN}^2 \cdot f_S}{P_{\rm OUT}}$ and η for the converters in Table I.

TABLE II
DESIGN SPECIFICATION FOR THE CONVERTER

f_S	V_{IN}	V_{OUT}	P_{OUT}	R_L
30-300 MHz	50 V	5 V	1 W	25 Ω

frequency the converter will reach steady state after just a few microseconds, this makes it possible to use an array of small converters and switch them on and off as needed. In this way, each converter is designed to operate with a defined load/output. This makes the design much easier as resonant inverters are generally very load dependent.

The fact that resonant inverters are load dependent, makes it very hard to achieve good performance at varying loads. Furthermore, resonant inverters need a large load impedance to operate in the ideal situation (having both ZVS and ZCS). This makes them well suited for boost-type converters, but making a buck type is a bit more challenging. The most commonly used way to overcome this challenge is to add an autotransformer at the output, in that way the load impedance seen by the inverter is increased [11], [14], [15]. Another way to achieve low output voltage is to use an array of converters with the input in series and the output in parallel in [16].

The most commonly used inverter is the class E, however several other topologies exist. Some of the research results are summed up in Table I. From the table it is seen that very high efficiencies are achievable for the inverters up to 97%. However, the efficiency drops around 10% for the complete dc/dc converters, i.e., when a rectifier is added.

From Table I, it is also seen that the converters have limited gains, with a step down of 6.6 times and a step up of 2 being the largest. As already stated the large reductions are not produced solely by the converter, but with different ways to make the load impedance appear larger. By further inspection, the connection given by (1) can be seen, this relation is shown in Fig. 2

$$\frac{V_{\rm IN}^2 \cdot f_S}{P_{\rm OUT}} \propto \frac{1}{\eta}. \tag{1}$$

Equation (1) shows that it is problematic to have a high input voltage and switching frequency while having a low output power and still keeping the efficiency high. The input voltage sets (together with $C_{\rm OSS}$) the energy stored in the output capacitance of the MOSFET each switching period and f_S sets how many times this has to be done each second. Combined these values are hence proportional to the circulating energy, that needs to run in the converter in order to ensure ZVS. The relation given in (1) hence states that it is difficult to achieve high efficiency, if the circulating energy that is needed for ZVS is high compared to the output power. The reason for this and the factor $V_{\rm IN}^2 \cdot f_S/P_{\rm OUT}$ will be described further in Section III.

This paper will cover the design of a VHF power converter with a low voltage and power output. This will require a large reduction in voltage and a combination of output power, input voltage, and switching frequency unlike any of the previous results. This will put the converter in the area marked in Fig. 2. As it is seen this is very far from the results achieved by previous researchers (the specifications for the converter is given in Table II).

As the load is given, the first step should be to design the rectifier and then design the inverter for the given input and load. It is also possible to design the inverter to a given load and then use different resistance compression networks to make the impedance of the rectifier match [26]–[28]. Though this is a solution often used, it will increase the complexity of the converter unnecessarily and possibly reduce the achievable efficiency, size, and price.

Section II covers the selection and design of a resonant rectifier for the given load and output power level. Then, a resonant inverter is designed for the input voltage and load impedance in Section III. Experimental results from three different power stages are shown in Section IV. Finally Section V summarizes and concludes the paper.

II. RESONANT RECTIFIERS

The purpose of the rectifier is to convert the ac current from the inverter to a dc output. Just as the MOSFET has an output capacitance, the diode has a junction capacitance. In order not to dissipate this energy in the diode, it is important that the transition is made smoothly, so the capacitance is discharged before the diode turns on.

As stated in Section I, it is difficult to achieve high efficiency if the input voltage and switching frequency are high and the output power low. The switching frequency is therefore set to 30 MHz for the initial design. If good results are achieved with this frequency, it might be increased further in order to minimize the size of the converter.

Though there are several ways to do this, only two will be considered here. The most commonly used class E rectifier and the equivalent to the class DE inverter, the class DE rectifier.

A. Class E

The class E rectifier is a rather simple circuit, consisting of a diode, two capacitors, and an inductor as shown in Fig. 3. Together these components constitutes a resonant rectifier capable of rectifying the ac input current to a dc output.

For now, it will be assumed that the output capacitance is infinite, so the output voltage is constant, and the diode is assumed to be ideal, i.e., no forward voltage drop, no junction capacitance, and no reverse current.

In this case, the rectifier will appear resistive at the switching frequency, if the resonance frequency of L_R and C_R are set to this frequency. This will simplify the design of the inverter as most design formulas are for a resistive load.

The scaling of the two components will determine the duty cycle of the diode, D_D. As the forward voltage drop of a diode increases with the current running through it, it is desirable to keep D_D as high as possible. However, as the diode is connected to the output through an inductor, the average voltage across it has to be V_{OUT}. Hence, a high D_D will lead to a high peak voltage across the diode.

In order to select D_D, and thereby the scaling of the resonant components, the values of real components have to be considered. All the considered inverters have a capacitor at the output ensuring a pure ac path, without this there would be a direct dc path from input to output and it would be impossible to reduce the voltage. The average current through the diode will therefore be the same as the output current.

With the forward voltage drop of a standard Schottky diode being around 0.5 V (10% of the output voltage), it is crucial to use a diode with low forward voltage drop. Fairchilds MBR0520L has one of the lowest forward voltages available, max 385 mV, and can handle a reverse voltage of 20 V. With this diode, the diode loss will be up to 77 mW or 7.7% of the output power. This clearly limits the maximum achievable efficiency and fits very well with the $\approx 10\%$ efficiency drop, seen in Section I when going from an inverter to a complete converter.

If $D_D = 50\%$ is chosen, the peak diode voltage will be $3.6 \cdot \mathrm{V}_{\mathrm{OUT}} = 17.8$ V leaving a little margin up to the maximum [29]. With this D_D the value of C_R should be [29]

$$C_R = \frac{1}{2 \cdot \pi^2 \cdot f_S \cdot R_L} = 67.5 \text{ pF}. \tag{2}$$

With this capacitance, the value of L_R can be calculated according to [29]

$$L_R = \frac{1}{(2 \cdot \pi \cdot f_S)^2 \cdot C_R} = 417 \text{ nH}. \tag{3}$$

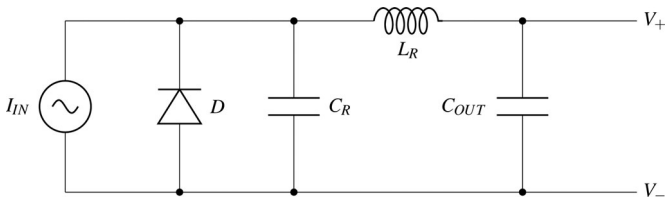

Fig. 3. Schematic of the class E rectifier.

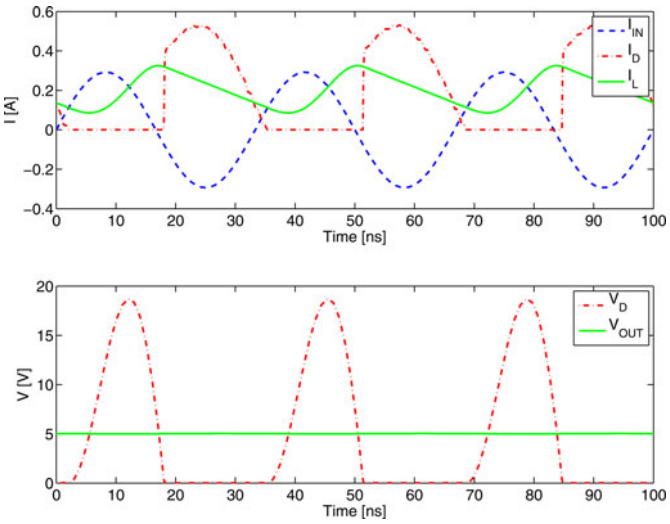

Fig. 4. Class E rectifier waveforms simulated with PLECS.

The inductor has, as expected, a dc current of 0.2 A (the output current with 1 W and 5 V) and on top of that an ac current with an amplitude of 120 mA (see Fig. 4). The dc resistance of the inductor is estimated to 25 mΩ and the ac resistance to 330 mΩ (these values are based on an air core inductor with a diameter of 6 mm and 8 turns of 0.4 mm wire). The loss caused by the inductor can then be calculated to 1 mW due to dc losses and 2.4 mW due to ac losses.

This is 0.34% of the output power and these resistances are based on a relatively large air core inductor. The equivalent series resistance (ESR) of a ceramic capacitor in the sizes used here will be less than 200 mΩ [30] and the currents running through them are smaller than the current in the inductor. The loss caused by them will thus not be significant. Furthermore, the parasitic capacitance of the diode can account for C_R. Actually, the parasitic capacitance of the chosen diode is, according to the datasheet, 65 pF at 5 V reverse voltage fitting almost perfectly with the calculated value.

B. Class DE

The class DE rectifier has an extra diode compared to the class E, but it does not have any inductors and the physical size and prize are expected to be more or less the same. As seen in the schematic in Fig. 5, the output capacitance is split in two. For now, they will both be assumed to be infinite making the output voltage pure DC. As the diodes are connected directly to the output, the total voltage across them will always be V_{OUT}. The diode duty cycle can therefore be chosen freely between 0 and

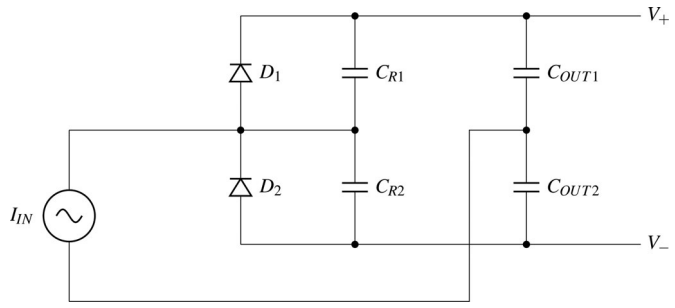

Fig. 5. Schematic of the class DE rectifier.

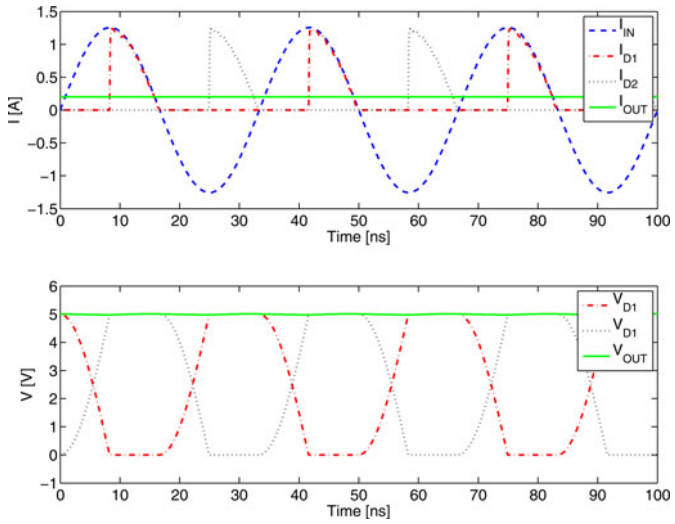

Fig. 6. Class DE rectifier waveforms simulated with PLECS.

0.5, a higher duty cycle would require both diodes to conduct at the same time.

From [31], (4)–(6) can be found. If $I_{\mathrm{IN,peak}}$ is isolated in (4) and ϕ is isolated in (6), the results can be substituted into (5). C_R can then be isolated in order to find the capacitances needed to get a desired diode duty cycle, (7). If a diode duty cycle of 25% is chosen, the needed capacitance can be calculated to 667 pF

$$V_{\mathrm{OUT}} = \frac{I_{\mathrm{IN,peak}} \cdot R_L}{\pi + \omega \cdot C_R \cdot R_L} \tag{4}$$

$$\cos(\phi) = 1 - \frac{2 \cdot \omega \cdot C_R \cdot V_{\mathrm{OUT}}}{I_{\mathrm{IN,peak}}} \tag{5}$$

$$D_D = \frac{\pi - \phi}{2 \cdot \pi} \tag{6}$$

$$C_R = \frac{\pi \cdot (1 - \cos(\pi - 2 \cdot D_D \cdot \pi))}{\omega \cdot R_L \cdot (1 + \cos(\pi - 2 \cdot D_D \cdot \pi))}. \tag{7}$$

As mentioned the diodes are coupled directly to the output, furthermore they provide the only dc path for the output current. The average current through each of the diodes will therefore be I_{OUT} (see Fig. 6), resulting in twice the diode loss as for the class E rectifier. This results in a total loss of more than 150 mW. Though several diodes could be put in parallel in order to reduce the forward voltage drop a bit, the diode losses will still be well above 100 mW, i.e., 10% of the output power.

TABLE III
PROS AND CONS OF THE INVESTIGATED RECTIFIER TOPOLOGIES

	Class E	Class DE
Pros	• Low complexity • Well documented and tested	• No inductors
Cons	• High semiconductor stress	• High loss • 2 semiconductors

C. Selection of Rectifier

Based on the analysis of the two rectifiers, the class E rectifier is found to be the best choice. The size and prize of the two rectifiers will be similar, but the loss of the class DE will be significantly higher than for the class E. Some of the pros and cons are shown in Table III.

For a high voltage output the DE might be better though, as the voltage across the diodes is lower and smaller diodes might be used. But for the low output needed for this converter, a class E rectifier is found to be the best choice.

The losses of the class E rectifier might even be unacceptable. A way to reduce the losses could be to use a synchronous rectifier, this will eliminate the forward voltage loss. This will however require an additional MOSFET, with the following need for gate drive and control.

III. RESONANT INVERTERS

As mentioned in Section I, a resonant inverter is used in order to eliminate switching losses. Either ZVS or ZCS can be achieved and in some special cases both. Generally, ZVS will eliminate losses due to parasitic capacitances and ZCS will eliminate losses due to parasitic inductance. For MOSFETs and diodes in power applications the capacitances causes the dominating loss, ZVS will therefore be the main criteria.

However in some cases it is, as mentioned, possible to achieve both ZVS and ZCS switchings (also called ZVS and zero derivative switching, ZDS). If this can be achieved the exact timing of the switching is less important, as the voltage across the MOSFET will be zero for a small amount of time.

If only ZVS can be achieved, the MOSFET needs to turn ON at exactly the point where the voltage across it hits zero. If it switches just a little too early, there will be energy stored in the capacitor causing switching losses. If it switches a little too late, the drain source voltage will go below zero and the body diode will start to conduct which also gives losses.

A. Class E

The most commonly used resonant inverter is the class E, a schematic of it is shown in Fig. 7. It consists of a single MOSFET, two inductors, and two capacitors. In optimum operation L_{IN} is an infinite choke providing a pure dc input current. The resonant circuit (L_R and C_R) is inductive at the switching frequency and the inverter is designed to have both ZVS and ZDS.

As already mentioned ZVS and ZDS switching can only be achieved in very specific situations. According to [32], [33] this

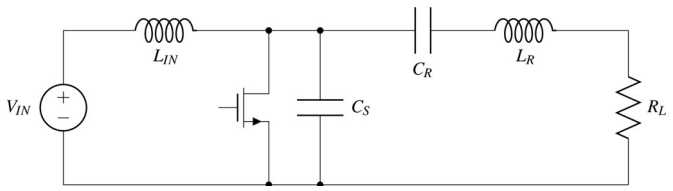

Fig. 7. Schematic of the class E inverter.

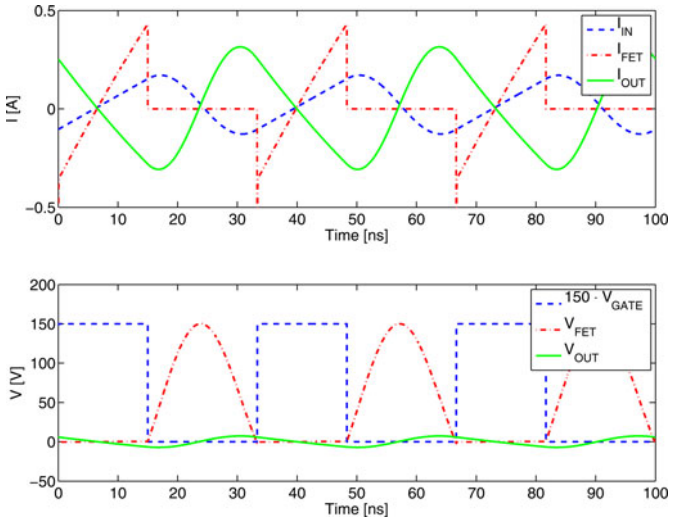

Fig. 8. Class E inverter waveforms with realistic C_{OSS} simulated with PLECS.

can only be achieved if

$$R_L = \frac{8}{\pi^2 + 4} \cdot \frac{V_{\mathrm{IN}}^2}{P_{\mathrm{OUT}}} \tag{8}$$

$$f_{S,\max} = \frac{P_{\mathrm{OUT}}}{2 \cdot \pi \cdot C_S \cdot V_{\mathrm{IN}}^2}. \tag{9}$$

With 50 V input, 1 W output, and a switching frequency of 30 MHz, this would require a load impedance of 1.44 kΩ and an output capacitance of 2.1 pF. From (9), it is seen that there is a special combination of f_S, V_{IN}, and P_{OUT} which makes it possible to operate in the optimum situation. Similar equations can be found for other topologies [32] and this is the reason for the dependence seen in Fig. 2.

A MOSFET with an output capacitance of 2.1 pF for this voltage level and switching frequency is not available, they have minimum 10 times that. Furthermore, the impedance is very far from the input impedance of the rectifier. It will therefore not be possible to achieve both ZVS and ZDS switchings. However, it is still possible to achieve ZVS and thereby high efficiency as long as the transitions of the MOSFET are controlled well. In this case, the components have to be selected carefully in order to ensure ZVS and the inverter will be running in a subnominal condition as described further in [34].

If the drain source voltage of the MOSFET is assumed to be a half sine wave when it is off and zero when it is on, the peak voltage across the MOSFET will be

$$V_{\mathrm{IN}} = \int V_{\mathrm{DS}} = V_{\mathrm{DS,peak}} \frac{2 \cdot (1 - D)}{\pi} \tag{10}$$

$$\Updownarrow$$

$$V_{\mathrm{DS,peak}} = V_{\mathrm{IN}} \frac{\pi}{2 \cdot (1 - D)}. \tag{11}$$

The rms value of a half wave rectified sine wave is

$$V_{\mathrm{DS,rms}} = V_{\mathrm{DS,peak}} \sqrt{\frac{D}{2}} \tag{12}$$

and the rms value of the output voltage is

$$V_{\mathrm{OUT,rms}} = \sqrt{P_{\mathrm{OUT}} \cdot R_L}. \tag{13}$$

According to [11], the reactance of the resonance circuit can now be determined by

$$X_{\mathrm{RC}} = R_L \cdot \sqrt{\left(\frac{V_{\mathrm{DS,rms}}}{V_{\mathrm{OUT,rms}}} \right)^2 - 1}. \tag{14}$$

By combining (11)–(14), an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained

$$X_{\mathrm{RC}} = R_L \cdot \sqrt{\frac{V_{\mathrm{IN}}^2 \cdot \pi^2 \cdot D}{2 \cdot (2 \cdot D - 2)^2 \cdot P_{\mathrm{OUT}} \cdot R_L} - 1}. \tag{15}$$

It is desirable to keep the duty cycle low in order to reduce the peak voltage across the MOSFET. However, due to turn on and off times and delays, it is decided to keep it close to 50%. From (11), it is found that a duty cycle of 45% will give a peak voltage of 142.8 V, leaving a little headroom if a 150 V MOSFET is used. Using this value along with the previous results, the needed reactance is found to be 326 Ω. If a capacitor of 680 pF is used, the value of the inductor can be calculated according to

$$L_R = \frac{C_R \cdot X_{\mathrm{RC}} \cdot \omega_S + 1}{C_R \cdot \omega_S^2} = 1.77\ \mu\mathrm{H}. \tag{16}$$

The next step is to determine the values of L_{IN} and C_S. In order to minimize losses, it is preferable to keep L_{IN} large, thus large ac currents running in and out of the converter and thereby causing unnecessary losses are avoided. If the input choke is assumed infinite, the next step is to calculate the value of C_S. In order to ensure ZVS, the voltage across C_S needs to rise to the peak and fall back down to zero within the period where the switch is open. This requires C_S and the resonance circuit to resonate at a frequency with a period equal to two times the period where the switch is open, i.e.,

$$T_R = 2 \cdot (1 - D) \cdot T_S \Leftrightarrow f_R = \frac{f_S}{2 \cdot (1 - D)}. \tag{17}$$

If the reactance of C_S is the same as the reactance of the resonant tank (with opposite operational sign) at f_R the circuit will resonate at this frequency. However, as the capacitor is only used when the MOSFET is off, it has to be scaled by $1-D$

$$C_S = \frac{1 - D}{2 \cdot \pi \cdot f_R \cdot X_{\mathrm{RC}}}. \tag{18}$$

With the specifications for this converter it would require a MOSFET with an output capacitance of maximum 10.9 pF. At the moment the MOSFETs with lowest output capacitances,

TABLE IV
CURRENTS (RMS) IN THE CLASS E INVERTER

IN	MOSFET	OUT
102 mA	165 mA	208 mA

C_{OSS}, which are able to handle 150 V, have an output capacitance of ≈20 pF at 50 V. It is therefore necessary to reduce the input inductor, in order to increase C_S while keeping the resonance frequency at the switch node equal to f_R. The output capacitance of the MOSFET is only contributing to the resonance in the part of the period where the MOSFET is OFF, hence it has to be scaled by $1-D$ in order to find the effective capacitance. The effective capacitance of the output capacitor is $C_{S,\mathrm{eff}} = \frac{C_S}{1-D} = 36.4$ pF, hence the total inductance of the resonance circuit and the input inductor should be

$$L_{\mathrm{total}} = \frac{1}{\omega_R^2 \cdot C_{S,\mathrm{eff}}} = 936\ \mathrm{nH}. \tag{19}$$

Knowing the values of X_{RC}, the input inductance can be calculated according to

$$L_{\mathrm{total}} = \frac{1}{\frac{1}{L_{\mathrm{IN}}} + \frac{\omega_R}{X_{\mathrm{RC}}}} \Leftrightarrow L_{\mathrm{IN}} = \frac{1}{\frac{1}{L_{\mathrm{total}}} - \frac{\omega_R}{X_{\mathrm{RC}}}} = 2.91\mu\mathrm{H}. \tag{20}$$

From a simulation, the rms current through the inductors and the MOSFET is found (see Fig. 8 and Table IV). The IRF5802 MOSFET has the lowest available output capacitance for a 150 V power MOSFET capable of switching in the VHF range. It has 20 pF output capacitance at 50 V and an on-resistance of 1.2 Ω, this will give a conduction loss in the MOSFET of up to 33 mW. The ac resistance of the inductors is estimated to be 100 mΩ, thus they will have a combined loss of 5.37 mW. As for the rectifiers, the losses in the capacitors are assumed to be negligible. Thus, the total loss in the class E inverter is estimated to ≈38 mW.

B. Class ϕ_2

As written in Section I, the large voltage peak across the MOSFET is a big problem when the input voltage is large. The class ϕ_2 (or EF_2) inverter, which is a hybrid between the class E and F_2 inverters, was developed in order to make the voltage across the MOSFET closer to a square wave. The voltage across the MOSFET should thereby become significantly smaller (ideally $2 \cdot V_{\mathrm{IN}}$ for $D = 50\%$). This is done by inserting a *LC* circuit in parallel with the MOSFET as shown in Fig. 9. This circuit is designed to have a resonance frequency at the second harmonic, which causes the voltage across the MOSFET to become a trapezoidal wave consisting of the first and third harmonics. The same benefits can be achieved with the flat-top class-E amplifier described in [35].

According to [14], the rms voltage across the MOSFET can be estimated by $V_{\mathrm{DS,rms}} = V_{\mathrm{IN}} \frac{4}{\pi \cdot \sqrt{2}}$; thus, the needed reactance of the resonant circuit is different (see (14)). The new values can be calculated to $L_R = 1.2\ \mu$H and $C_R = 522$ pF. No exact equations for the calculations of the added *LC* circuit or the input inductance are given in the literature; however, the following

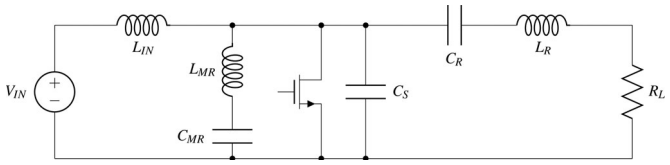

Fig. 9. Schematic of the class ϕ_2 inverter.

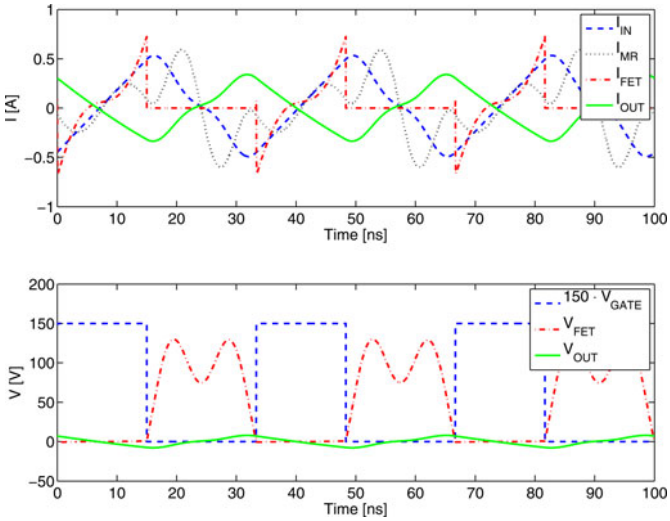

Fig. 10. Tuned class ϕ_2 inverter waveforms simulated with PLECS (the peak drain source voltage is reduced to 132 V).

TABLE V
CURRENTS (RMS) IN THE CLASS ϕ_2 INVERTER

IN	MR	MOSFET	OUT
311 mA	301 mA	207 mA	208 mA

gives results which are close [19]:

$$L_{\mathrm{IN}} = \frac{1}{9 \cdot \pi^2 \cdot f_S^2 \cdot C_S} = 625\ \mathrm{nH} \tag{21}$$

$$L_{\mathrm{MR}} = \frac{1}{15 \cdot \pi^2 \cdot f_S^2 \cdot C_S} = 375\ \mathrm{nH} \tag{22}$$

$$C_{\mathrm{MR}} = \frac{15}{16} \cdot C_S = 18.8\ \mathrm{pF}. \tag{23}$$

A PLECS simulation was used to tune the component to get exact ZVS (see Fig. 10), the final values are shown in Table VII. As for the class E inverter, the rms current through the inductors and the MOSFET was extracted, see Table V.

With the MOSFET used for the class E the conduction loss will be up to 51.4 mW. The current through L_R will be the same as for the class E and though the inductance is a bit lower, the ESR will still be estimated to 100 mΩ giving a loss of 4.3 mW. The input inductor and L_{MR} are noticeably smaller and their ESR will therefore be estimated to 50 mΩ and 25 mΩ, respectively. With these resistances and the listed rms currents, their loss will be 4.8 and 2.3 mW, respectively. The total loss of the class ϕ_2 inverter (again ignoring losses in the capacitors) is estimated to be 62.8 mW.

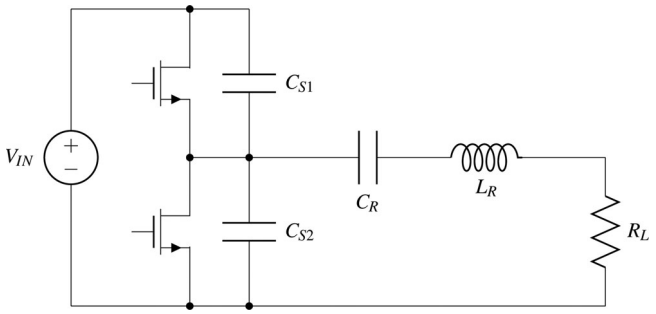

Fig. 11. Schematic of the class DE inverter.

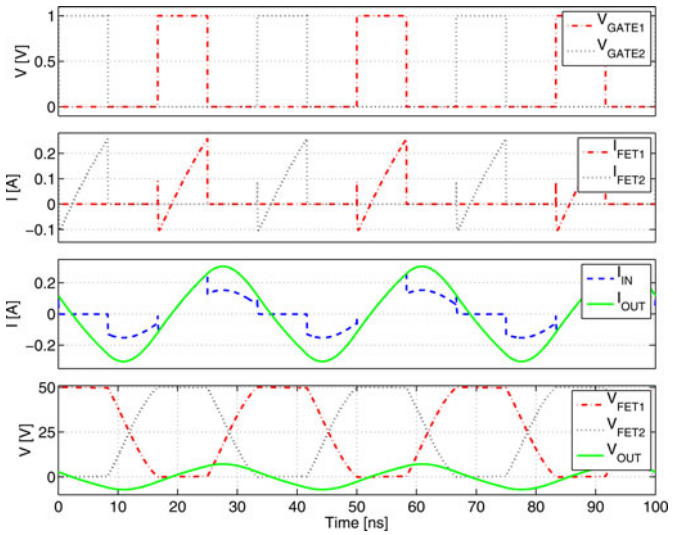

Fig. 12. Class DE inverter waveforms simulated with PLECS.

TABLE VI
CURRENTS (RMS) IN THE CLASS DE INVERTER

FET1	FET2	OUT
67.8 mA	67.8 mA	208 mA

C. Class DE

The class DE inverter has the same ZVS properties as the class E inverter and the low voltage stresses of the class D inverter. It is the counterpart of the class DE rectifier considered in Section II and, as seen in Fig. 11, the two circuits are very alike. As the DE rectifier, the DE inverter has two switches connected directly to the dc voltage, in this case MOSFETs connected to the input voltage. Both MOSFETs have capacitors across them which can be tuned to achieve ZVS. The only additional components are a resonant circuit at the output, just as seen for the previous inverters.

As for the class E inverter, ZVS and ZDS switching can be achieved in very specific situations. However, the values needed are different [32]

$$R_L = \frac{V_{\mathrm{IN}}^2}{2 \cdot \pi^2 \cdot P_{\mathrm{OUT}}} \tag{24}$$

$$f_{S,\max} = \frac{P_{\mathrm{OUT}}}{2 \cdot C_S \cdot V_{\mathrm{IN}}^2}. \tag{25}$$

With these equations, the demands for load impedance and output capacitance become $R_L = 126.7\ \Omega$ and $C_S = 6.67$ pF. Though this cannot be achieved either, these values are much closer to the design values. Increasing P_{OUT} to $\approx$5 W would actually make it possible to use this topology in the ideal situation. The design criteria is however 1 W and the converter will thus be designed to have ZVS.

If the voltage across C_{S1} and C_{S2} are assumed to rise linear when they are charged, the rms value of the voltage at the node between the MOSFETs will be trapezoidal. If the duty cycle of each MOSFET is set to 25%, the rms value can be calculated as $V_{\mathrm{IN}}\sqrt{\frac{5}{12}}$. As with the two other inverters, this value can be used to find the needed reactance of the resonant circuit. Using (14) and choosing $C_R = 680$ pF, the value of L_R is calculated to 859 nH. As for the class E inverter, the value of each of C_{S1} and C_{S2} can be found using the reactance of the resonance circuit and scaling them according to the duty cycle. This gives

$$C_S = \frac{1}{2 \cdot (1-D) \cdot 2 \cdot \pi \cdot f_S \cdot X_R} = 21.9\ \text{pF}. \tag{26}$$

As the total voltage across the two MOSFETs always will be V_{IN}, the average voltage across each of them is 25 V. The output capacitance of the MOSFET, used for the E and ϕ_2 inverters, almost fit the capacitance needed at this voltage and it will thus be used for the efficiency estimates. However, as the peak voltage across the MOSFETs is limited to the input voltage, several other MOSFETs could be used (or the input voltage could be increased).

Just as the case were for the two other inverters, it was necessary to adjust L_R a bit to give the desired output power. Adjusting the L_R to 550 nH and thus recalculating C_S to 21.4 pF gave the desired output power and the rms currents were extracted (see Fig. 12 and Table VI).

With these currents, the losses in the MOSFETs and the inductor are estimated to be $P_{L_R} = 2.2$ mW (using an ESR of 50 mΩ due to the small inductance) and $P_{\mathrm{FET1}} = P_{\mathrm{FET2}} = 5.5$ mW. If the losses in the capacitors are assumed negligible, the total loss will be 13.2 mW.

D. Selection of Inverter

During the analysis of the inverters, the values for all the passive components where found and they are summarized in Table VII.

All the inverters had some pros and cons, thus the same inverter will not be best for all applications. Some of the pros and cons are listed in Table VIII.

The class E inverter consists of only one MOSFET, two inductors, and a capacitor (if C_S is composed by the output capacitance of the MOSFET). It has however the largest voltage peak across the MOSFET which will limit the input voltage for a given MOSFET. Furthermore, the two inductors are both larger than any of the inductors used for the two other converters. This might limit the minimum size of the inverter as inductors are assumed to be the largest components. The total loss was estimated to be 38 mW or $\approx 4\%$ of the output power.

TABLE VII
COMPONENT VALUES FOR THE CLASS E, ϕ_2 AND DE INVERTERS

Component	Class E	Class ϕ_2	Class DE
L_{IN}	2.91 μH	794 nH	
L_{MR}		375 nH	
C_{MR}		18.8 pF	
C_S	20 pF	20 pF	$2 \cdot 21.4$ pF
C_R	680 pF	680 pF	680 pF
L_R	1.43 μH	1.23 μH	550 nH

TABLE VIII
PROS AND CONS OF THE INVESTIGATED INVERTER TOPOLOGIES

	Class E	Class ϕ_2	Class DE
Pros	• Low side switch • Easy tuning • Well documented	• Low side switch • Reduced stress	• One inductor • Low loss • Low stress
Cons	• Large stress • Large inductors	• Largest loss • Complex	• High side switch

TABLE IX
COMPARISON OF MOSFET CHARACTERISTICS

Component	V_{DSS}	I_D	$R_{DS(on)}$	C_{ISS}	C_{OSS}
IRF5802	150 V	0.9A	1.2 Ω	85 pF	18 pF
FDN86246	150 V	1.6A	359 $m\Omega$	180 pF	28 pF

($R_{ds(on)}$ at V_{GS} = 10 V and capacitances at V_{DS} = 50 V).

The class ϕ_2 inverter was a lot like the class E, the only difference being the added *LC* circuit put in to reduce the voltage across the MOSFET. While this is a good way of keeping the voltage down, the steep voltage curves require larger currents making the loss larger than seen for the class E inverter. Although it has two extra components, compared to the class E inverter, the physical size is expected to be more or less the same as the values (and thereby the size) of the inductors are smaller. The total loss was estimated to 62.8 mW which is a 65% increase compared to the class E inverter.

The class DE inverter was the only inverter with two switches. However, as C_{S1} and C_{S2} are composed by the parasitic capacitance of the MOSFETs, the total component count of the class DE inverter are the same as for the class E inverter. The peak voltage across the MOSFETs were by far the lowest seen in any of the inverters and the currents were also the lowest. These things combined gave the smallest output inductor (which also is the only inductor) and the lowest losses (13.2 mW).

From this analysis, the class DE inverter seems to be the best solution and the class E inverter comes in second. However, during this analysis the gate drive has not been considered. A good high side gate drive which is capable of operating in the VHF range has yet to be developed whereas a low side gate drive can be made with few components [24]. The complexity, price, and losses associated with the added high side gate drive will, at least, reduce the benefits of the DE inverter.

With the above considerations in mind, the class E inverter was chosen for the final design.

IV. EXPERIMENTAL RESULTS

In Section III, the IRF5802 MOSFET was introduced and used for calculations and loss estimates. Although commercial available MOSFETs are generally designed for either hard switching at a few megahertz or less or for use in RF applications [36], several MOSFETs which can be used for this application exist. Two of the best suited are compared in Table IX.

In Section III, an output capacitance of 10.9 pF was found ideal, but 18 pF was the closest achievable with commercially available MOSFETs. As the voltage waveform across the MOSFET and C_S is given by V_{IN}, f_S, and D, the currents (and thereby losses) in L_{IN}, C_S, and the MOSFET scale with the value of C_S. It is therefore desirable to keep the value of C_S as close to this as possible in order to achieve high efficiency.

Comparing the two MOSFETs, the IRF5802 (M_1) has much higher on-resistance than the FDN86246 (M_2). However, the output capacitance is lower and will as mentioned decrease the currents and thus reduce the drawback of the high on-resistance. Assuming the waveform of the voltage across the MOSFET is the same using the two MOSFETs, the current using M_2 will be $\frac{C_{M2}-C_{M1}}{C_{M1}} = 142\%$ larger than using M_1. The on resistance will be reduced by $\frac{R_{M1}-R_{M2}}{R_{M1}} = 70.1\%$. Combining this gives a total loss reduction of 27.4%, using the estimated loss found in Section III this correspond to 9 mW. Furthermore, the increased current will also give losses in the input inductor, again using the estimate from Section III the increased loss is found to $142\% \cdot 5.37$ mW $= 7.63$ mW. Hence, the total loss difference using the two MOSFETs is estimated to be less than 2 mW. The increased capacitance will however also make the timing of the switching more important, as a larger amount of energy will be stored in the capacitor and dissipated in the MOSFET if the switching is just a little wrong.

Based on the analysis above, the MOSFET from IRF are found most suited. But as they are very close, prototypes using both will be made to compare them further.

The next sections will cover the results obtained with three different power stages. The first power stage is the one which has been designed in the previous sections, the second power stage is with the MOSFET with lower $R_{\mathrm{DS(ON)}}$ and the last power stage is with a large input inductor and higher output power, this should, as described in Section III, give a higher efficiency.

A signal generator has been used to drive the MOSFETs and hence the design and efficiency of this is not included. The gate signal is however a sinewave which several researchers have shown how to generate efficiently using various types of resonant gate drives, e.g. [37]–[39]. The duty cycle is controlled by adjusting the dc offset of the sinewave, hence a dc offset equal to the threshold of the MOSFET will lead to a duty cycle of 50% and a lower offset lead to a lower duty cycle.

A. MOSFET With Low C_{OSS}

A power stage with the components selected in Sections II and III was implemented. Ceramic C0G capacitors were used for the resonating capacitors in order to ensure stable capacitance with varying voltages and ceramic X7R capacitors were used

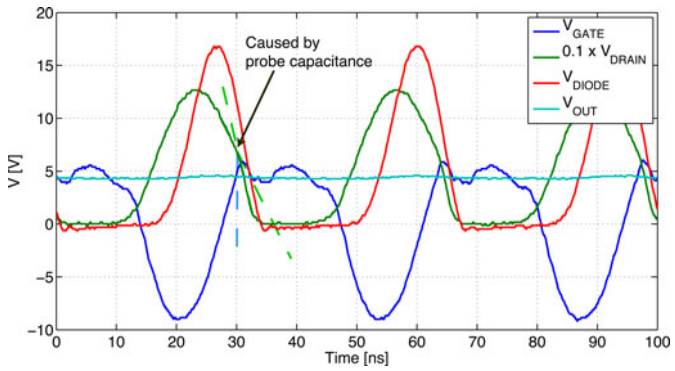

Fig. 13. Measurements on the prototype with low C_{OSS}.

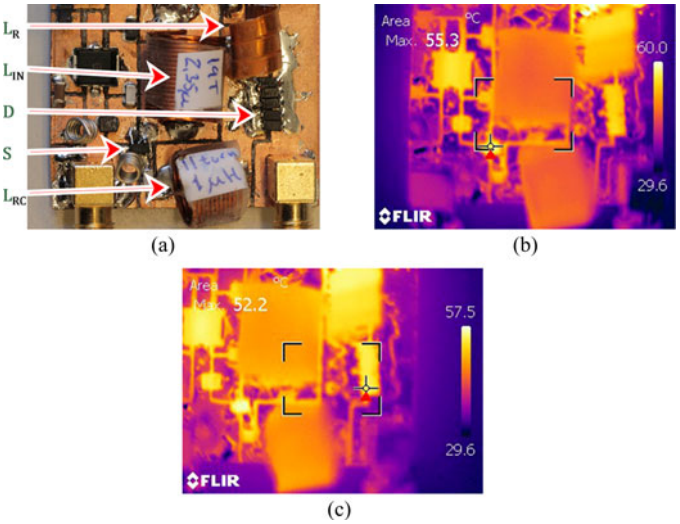

Fig. 14. Temperature measurements of the MOSFET and the diodes in the prototype with low C_{OSS} ($W_{\mathrm{board}} = 40$ mm). (a) Placement of the components. (b) The MOSFET is 55.3 °C. (c) The diodes are 52.2 °C.

TABLE X
MEASUREMENTS ON POWER STAGES

Converter	f_S [MHz]	I_{IN} [mA]	V_{OUT} [V]	R_L [Ω]	η [%]	T_{Mos} [°C]	T_{Dio} [°C]
Low C_{OSS}	30	28	5.00	25	71.5	55.3	52.2
Low R_{DS}	29	32	4.93	25	60.7	65.1	53.2
Large L_{IN}	30	37	5.00	16.3	82.9	46.2	50.5

as input and output capacitors. Custom made air core solenoids were used in order to enable exact tuning of the inductances and thereby achieve ZVS.

Just as the case were when going from calculated values to simulations, slight adjustments had to be made. The tuning procedure was first to tune the inductor in the output filter to make it resistive at the switching frequency. Once that was done, the inverter was added to the design and a low voltage was applied. It was seen that the converter was not ZVS switching as the output capacitance of the MOSFET was not discharged when switched ON.

In order to get it to discharge faster, the values of the input and resonant inductors had to be lowered. First, the resonant inductor was lowered to give the desired output power and then the input inductor was adjusted to make the converter ZVS. As the output capacitance of the MOSFET is 20 pF, measuring with a probe with 10 pF capacitance changes the circuit a lot. This ruins the tuning and ZVS is thus not achieved, some waveforms have been measured and they are shown in Fig. 13. As it is seen the drain voltage has a small break when the MOSFET is switched ON, this is due to the 10 pF added by the probe. The fact that the converter is not ZVS also introduces the miller plateau in the gate charge and causes the gate signal to deviate from a sinewave when the voltage reaches the miller voltage.

So for the final fine tuning a thermal camera was used to measure the temperature of the MOSFET, it was then assumed that the MOSFET was ZVS when the temperature rise was lowest. Even though this is not a solid proof of ZVS, a low temperature rise comes from low power loss and thus the best tuned circuit.

Fig. 14 shows thermal pictures of the converter in a steady state. From the pictures, it is seen that the diodes get almost as hot as the MOSFET. As the size of the components is almost equal this indicates that the total diode loss is almost five times the total MOSFET loss (there are five diodes in parallel). The efficiency was measured to be 71.5% (see Table X).

B. MOSFET With Low R_{ON}

When the MOSFET was selected, the FDN86246 was found to be equally good to the IRF5802. The biggest difference between the two was on-resistances and parasitic capacitances. A prototype was implemented using the FDN86246 in a circuit almost identical to the one used for the previous converter. A few turns were removed from the input inductor in order to make the converter ZVS with the increased output capacitance in the new MOSFET.

The MOSFET gets almost 10 °C warmer (see Fig. 15) clearly indicating a higher loss. Due to the higher output capacitance, more energy is stored and if the switch is switched at a few volts instead of zero, much more energy will be dissipated in the on-resistance. Furthermore, the ac current in the input inductor is larger which also increases the losses. The total efficiency of the converter was measured to 60.7%.

C. With Large Input Inductor

As explained in Section III, the highest efficiency should be achieved with a large input inductor (dc input current). To test this, a prototype was made with the IRF5802, but this time with a 6.5 μH input inductor. Then, the resonance circuit and the load were adjusted in order to get ZVS and 5 V output.

The increased output power makes the current through the MOSFET closer to that seen for the ideal class E inverter. Thereby, the loss due to slight deviations in the timing of the switching becomes smaller.

The waveforms shown in Fig. 16 clearly show that the converter is not ZVS when probes are placed at the gate and drain. Furthermore, the voltage drops below 4 V, however removing the probes makes the output voltage increase to 5.0 V.

When tuned, the output power of the circuit became 1.53 W and the efficiency was measured to 82.9%. This efficiency is without gate drive, but it is still among the best results achieved

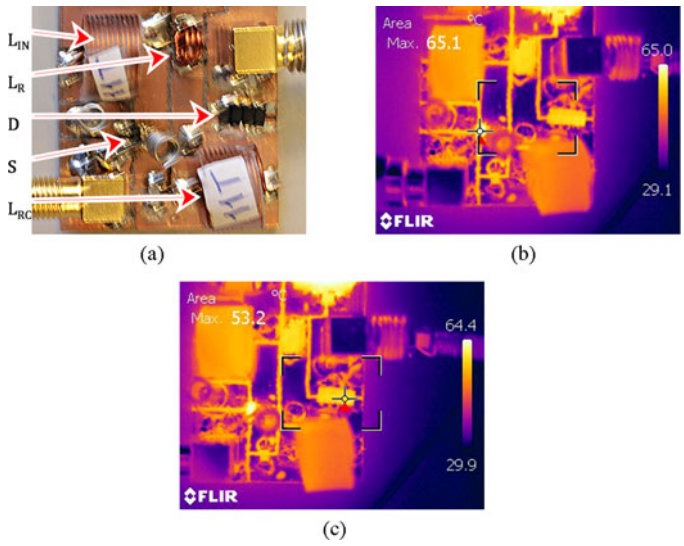

Fig. 15. Temperature measurements of the MOSFET and the diodes in the prototype with low $R_{\mathrm{DS(ON)}}$ ($W_{\mathrm{board}} = 32$ mm). (a) Placement of the components. (b) The MOSFET is 65.1 °C. The diodes are 53.2 °C.

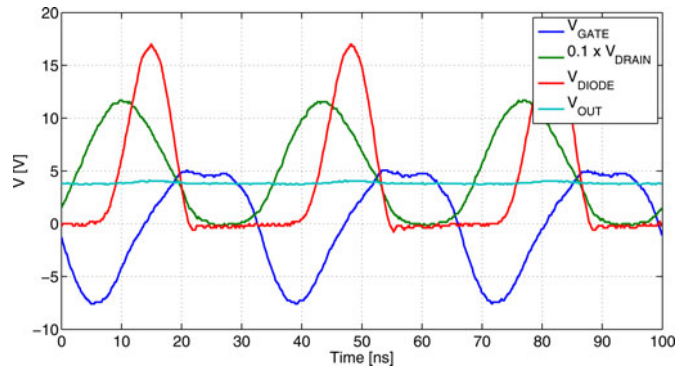

Fig. 16. Measurements on the 1.53W prototype with IRF5802.

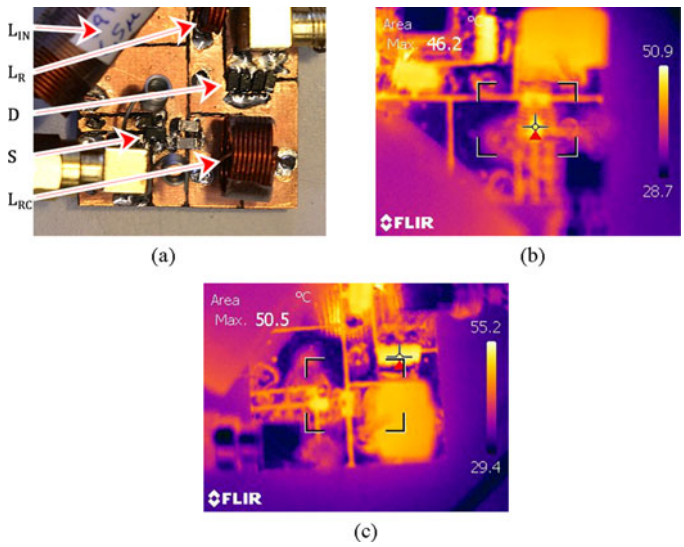

Fig. 17. Temperature measurements of the MOSFET and the diodes in the prototype with large input inductor. (a) Placement of the components. (b) The MOSFET is 46.2 °C. (c) The diodes are 50.5 °C.

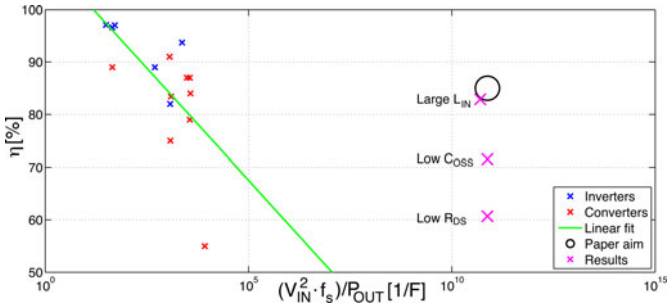

Fig. 18. The achieved $\frac{P_{\mathrm{OUT}}}{V_{\mathrm{IN}} \cdot f_S}$-factor and η next to previous results.

by previous researchers. Furthermore, the $\frac{V_{\mathrm{IN}}^2 \cdot f_S}{P_{\mathrm{OUT}}}$-factor explained in Section I is much smaller than for any of the converters shown in Table I.

D. Summary of Experimental Results

The efficiency achieved for the three power stages is shown in Table X. From the three prototypes, it is seen that good efficiencies can be achieved just by having ZVS. However, the larger the current through the MOSFET is at the switching instant, the more important becomes the timing of the switching and losses increase.

It has been shown that VHF converters with a very low $\frac{V_{\mathrm{IN}}^2 \cdot f_S}{P_{\mathrm{OUT}}}$-factor can be made with high efficiency, the best even had an efficiency of 82.9% which puts it among the best VHF converters. For comparison, the results achieved for the power stages are shown in Fig. 18. The efficiency is not as high as wanted and the factor is a little higher than desired for one of the prototypes due to the higher output power. However, seen next to previously achieved results they are very close.

V. Conclusion

The theoretical design of the resonant converter was considered in Sections II and III. Several different topologies were considered and based on complexity and efficiency estimates a class E inverter and rectifier were chosen.

The class E inverter was chosen based on complexity, efficiency, and the fact that it did not require a high side switch. With a simple and efficient high side gate drive the DE inverter is theoretically better, especially for converters with even higher input voltages. Such a gate drive was however yet to be invented and this topology was therefore not used for the practical implementation.

For the rectifier part it was again the class E topology that were chosen, this time due to the forward voltage drop of the diodes. With a low-voltage output, the forward voltage drop of the diode becomes a significant percentage of the output voltage and a single diode rectifier was found to be the best choice. For higher output voltages, the DE rectifier might be better as the loss due to forward voltage drop in the diodes becomes insignificant and the voltages stress of the devices the major concern.

Three different power stages were made; one with a MOSFET with the lowest available output capacitance, one with a

MOSFET with low on-resistance, and one with increased output power allowing a large input inductor. All the converters had 50 V input and 5 V output and the achieved efficiencies were between 60.7% and 82.9%. This shows that it is possible to make low power very high frequency converters with high step down ratio running at subnominal condition as long as the components are chosen carefully.

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A.5 M. Madsen, A. Knott, M. A.E. Andersen:
***"Very High Frequency Resonant DC/DC Converters for LED Lighting"*,**
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Very High Frequency Resonant DC/DC Converters for LED Lighting

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***Abstract*— This paper presents a very high frequency DC/DC converter for LED lighting. Several resonant topologies are compared and their usability discussed. At the end the resonant SEPIC converter is chosen based on the achievable power density and total bill of material. Simulations of a 51 MHz converter with 40 V input and 15 V output are made. The simulation shows possibility of achieving efficiency up to 87 % even with a HEXFET Power MOSFET. Three prototypes of the simulated converter are implemented showing good correlation with simulations. The prototypes have efficiencies up to 84 % and power densities up to 8.9 W/cm^3 (146 W/in^3).**

I. Introduction

During the last decade the focus on green and environment friendly energy usage has been constantly increasing. This has lead to a large increase in the use of Light-Emitting Diodes (LEDs) for lightning. These bulbs are still quite expensive due to both expensive LEDs and the power converter needed to supply these. Hence there is a strong demand for small, cheap and efficient power converters.

The power density of Switch-Mode Power Supplies (SMPS) is limited by their passive energy storing elements. As both the physical size and price of these scale with the switching frequency (f_S), increasing f_S into the Very High Frequency band (VHF, 30-300 MHz) will make it possible to achieve higher power density and lower cost. Increasing the switching frequency has several other advantages, which has been discussed in [4], [6], [15] and [16].

The high increase in f_S causes several new problems to arise. Some of these have been solved [4], [11] and [18], but many still need to be investigated. One of the main problems is the switching loss, which increases linearly with f_S. As f_S increases into the VHF band the switching losses becomes so severe that it will be impossible to cool the switching device and keep the efficiency high. Several researchers [2]- [5] and [7] have tried to use different types of resonant converters with Zero Voltage Switching (ZVS) and/or Zero Current Switching (ZCS) in order to reduce or ideally eliminate these losses.

Due to the resonating behaviour of these converters it is however very difficult to control these converters for varying loads efficiently. For now the most efficient way is to use burst mode control to simply Pulse Width Modulate (PWM) the converter in order to achieve the desired output [4], [9] and [21].

When working continuously in open loop these converters will have an almost constant current output for a given input voltage. This makes them very well suited for LED applications where it is the current that needs to be controlled. As the output current is constant for a given input voltage the current through the LED will be constant even as the forward voltage changes due to changes in temperature. The life time of LED bulbs are limited by the electrolytic capacitors needed, increasing the switching frequency will eliminated this need and hence increase the life time of the bulb.

This paper will give an example of the design of a VHF resonant DC/DC converter for LED lighting. First an appropriate topology is selected in section II, then the a simulation is made and component selected in section III. Section IV covers the implementation and measurements and finally section V concludes the paper.

II. Selection of topology

When designing resonant DC/DC converters it is very common to split the converter in to two parts; 1) a resonant inverter converting the DC input voltage to a sinusoidal output current 2) a resonant rectifier rectifying the AC current to a DC output [1], [8], and [14].

The most commonly used rectifier is the class E rectifier [8], [17] and [19]. Other alternatives exist [1], [7] and [10], but due to the very simple schematic with a single diode the class E rectifier is chosen for this converter.

For the inverter part several topologies has been used [2], [3] and [5], each with their own pros and cons.

The class DE inverter (used in [5], [10] and [11] and shown together with the selected rectifier in Figure 1) is the topology with the lowest stress on the switches due to the direct connection to the input, but it requires a high side driver. This is complex to design for these frequencies and it will increase both the complexity, size and price of the converter.

The class E inverter (used in [6] and [8]) shown in Figure 2 has only a low side switch and is therefore much simpler to drive, however it imposes a huge voltage stress on the switch. As the drain of the switch is connected to the input through an inductor, the average drain-source voltage (V_{DS}) of the switch has to be equal to the input voltage. Even if V_{DS} is assumed constant when the switch is closed, the peak voltage will be

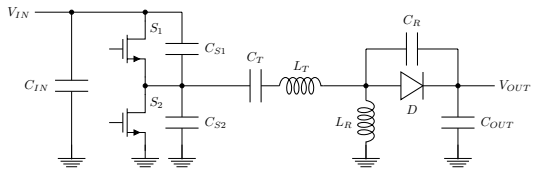


Fig. 1. Schematic of the class DE inverter and class E rectifier.

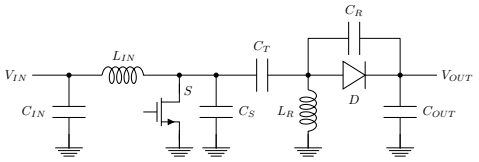


Fig. 4. Schematic of the SEPIC converter.

two times V_{IN} for a duty cycle of 50 %. In reality the voltage across the switch is more like a half wave rectified sine wave in order to achieve ZVS, which result in a peak voltage of 3.56 times V_{IN} [12].

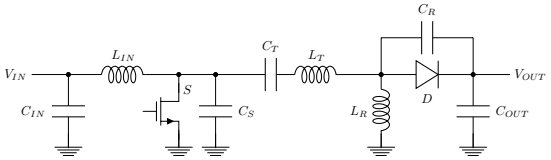


Fig. 2. Schematic of the class E inverter and rectifier.

In order to reduce this huge peak voltage the class EF_2 (or φ_2), which is a hybrid between the class E and class F_2, has been developed ([13] and [14]). It introduces an extra resonant circuit (C_{MR} and L_{MR} in Figure 3) across the drain and source of the switch with a zero at the second harmonic of f_S. If tuned correctly this adds the third harmonic of f_S on top of the sine wave seen with the class E. This results in a trapezoidal waveform across the switch. This reduces the peak voltage a bit, but increases complexity and results in additional losses due to large AC current at three times f_S.

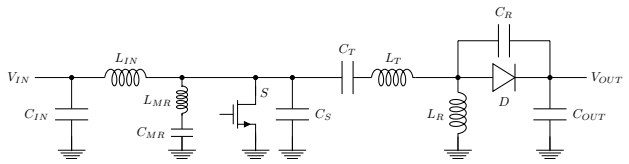


Fig. 3. Schematic of the class EF_2 inverter and class E rectifier.

The SEPIC converter [20] shown in Figure 4 is similar to the circuit in Figure 2 with L_T removed. However the waveforms are different, as this converter cannot be split into an inverter and a rectifier. The changed waveforms results in a much smaller input inductor than needed for the class E inverter, thus the achievable power density is higher due to fewer and smaller inductors.

Based on the analysis of the four converter topologies the SEPIC converter was chosen as it gives the highest power density and lowest cost.

III. Simulation and component selection

A model of a resonant SEPIC converter has been set up in spice based on the tuning procedure explained in [20]. The converter is designed to have the specifications given in table I. The converter will be used to supply a string of LEDs with a combined forward voltage drop of 12-15 V, depending on temperature and power level.

TABLE I
DESIGN SPECIFICATIONS

Specification	Symbol	Value
Input voltage	V_{IN}	40 V
Output power	P_{OUT}	5 W
Output Voltage	V_{OUT}	15 V
Switching frequency	f_S	51 MHz

From the simulations it is seen that the MOSFET should have a break down voltage of at least 100V (see Figure 6), however if the duty cycle is adjusted closer to 50 % the peak voltage will get close to 143 V (3.56 times the input voltage as for the class E). For this reason it was decided to build the prototype around an IRF5802 MOSFET from International Rectifier. The MOSFET has a break down voltage of 150 V and small parasitic capacitances compared to its competitors.

The peak voltage is slightly above 40 V (see Figure 6 where V_{AC} is anode-cathode voltage) and a MBR0540 40 V Schottky diode has therefore been selected. C_R needs to be 105 pF which is more than the parasitic capacitance of a single diode (35 pF), thus it is necessary either to add a 70 pF capacitor or use three diodes in parallel. The last solution have the benefit of sharing the current between the three devices. As the forward voltage drop of the diodes increases with the current running through them, this will lead to reduced losses and this solution was therefore selected.

The inductors are all square air core inductors (1515SQ-68N, 1515SQ-82N and 2222SQ-161) as they have a fairly high Q factor and are available off the shelf which ease implementation. The C_T capacitor is implemented with 4 parallel capacitors as it was found that this increased the efficiency of the converter with 1-2 % compared to using a single capacitor of the same value. For the input and output capacitors standard 1 μF X7R capacitors was selected.

IV. Implementation and measurements

A prototype of the simulated converter has been implemented and is shown in Figure 7. The prototype had an efficiency of 84 %, this is slightly lower than the simulated efficiency but still on level with other state of the art VHF converters. The output power was 5.7 W at 40 V input, which is significantly higher than the expected. The increase in output

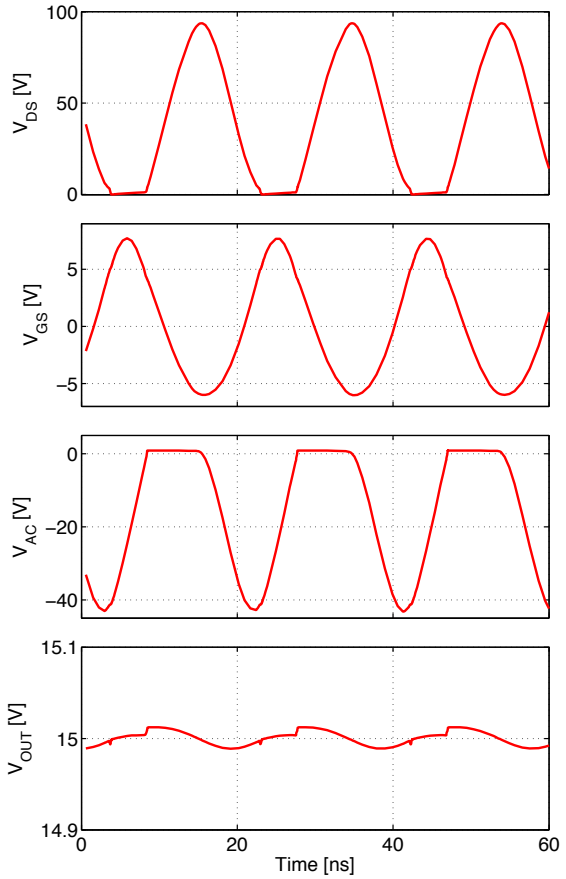


Fig. 5. Simulation results

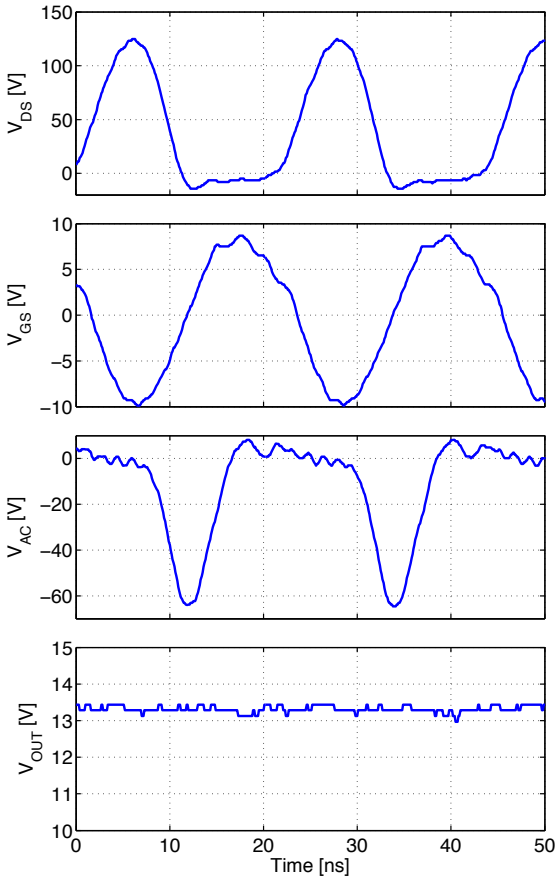


Fig. 6. Measured waveforms

TABLE II
BILL OF MATERIALS

Component	Simulated	Prototype	Type
C_{IN}	1 μF	1 μF	Capacitor (X7R)
L_{IN}	160 nH	160 nH	Inductor
S		IRF5802	n-channel MOSFET
C_S	22 pF	Parasitic	Capacitor
C_T	40 pF	4 · 10 pF	Capacitor (NPO)
L_R	82 nH	82 nH	Inductor
D		3 · MBR0540	Schottky diode
C_R	105 pF	Parasitic	Capacitor
C_{OUT}	1 μF	1 μF	Capacitor (X7R)

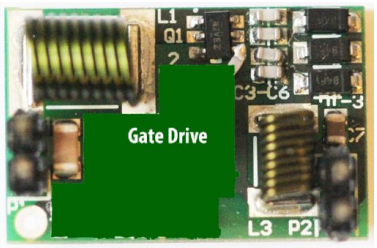
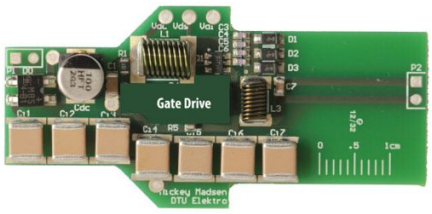


Fig. 7. Picture of the implemented prototype on a 15x22 mm PCB

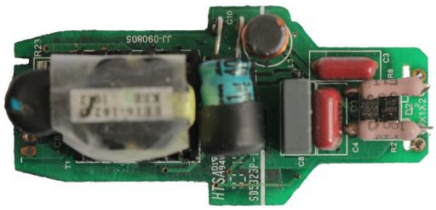
power was achieved by reducing the switching frequency to 46 MHz and increasing the duty cycle.

The gate and output voltages were measured with the standard probes for a Rohde & Schwartz RTO1024 digital oscilloscope. The capacitance of the probes are 10 pF, adding this between the drain and source of the MOSFET would change the resonance of the converter making it hard switch and thereby destroy the switch. To avoid this a voltage divider was made by adding a 1 pF capacitor in series with the probe, this reduces the effectively added capacitance to 0.9 pF. This still affect the behaviour of the converter, however as seen in Figure 6 the converter is still operating close to ZVS. In order to get the correct DC level a resistive voltage divider was added in parallel with the probe and the 1 pF capacitor. The same principle was used to measure the voltage at the anode of the diode, at this node 10pF would not be as crucial but it is still necessary to keep the converter close to ZVS.

From the measured waves it seems like the gate drive is a few nano second to slow when turning on the MOSFET. Whether this is actually happening or if it is due to a small delay caused by the resistive/capacitive voltage division made to measure the drain voltage is not certain. If the gate drive is actually turning on the MOSFET to late, it is partly saved

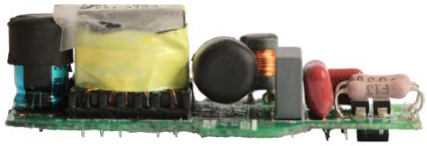


(a) Top of offline prototype

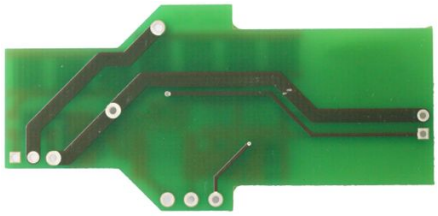


(b) Top of commercial supply

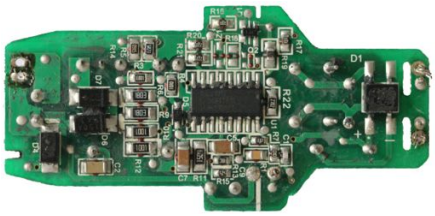
(c) Front of offline prototype



(d) Front of commercial supply



(e) Bottom of offline prototype



(f) Bottom of commercial supply

Fig. 8. Comparison of first VHF based prototype and commercial available 230 V power supply

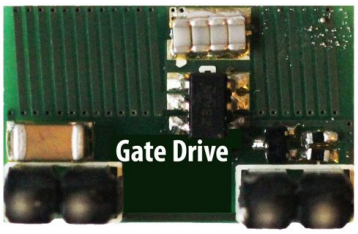


Fig. 9. Top side of prototype with PCB inductors (10x16mm PCB)

by the body diode of the MOSFET and the efficiency can therefore still be acceptable. However in this situation fine tuning of the gate drive could increase efficiency a few percent as the body diode is a quite lossy device.

The peak voltage across the diode is far above the rated limit. This is mainly caused by the reduced switching frequency which makes the impedance of the inductor decrease while the impedance of the parasitic capacitance increase, this increases the duty cycle of the diode and there by increases the peak voltage. The increased power is also contributing to an increased peak voltage, but this will only cause a slight increase.

The ripple seen at the output is clearly some digital noise cause by the oscilloscope and not something that can be used to determine the output ripple of the converter.

A. *Alternative implementations*

The main reason for the increasing the output power was to get the same amount of power as the commercial supply shown in Figure 8(b), 8(d) and 8(f). This supply is made for the european mains (230 V) and has an efficiency of 77 %, i.e. 7 % below the 40 V VHF converter with the same output in a much smaller footprint. In order to make a fair comparison a prototype was made with a mains rectifier and a capacitive voltage divider to reduce the input voltage of the VHF converter (the offline prototype is shown in Figure 8(a), 8(c) and 8(e)). The offline prototype has an efficiency of 78 % and a volume which is reduced by approximately 80 % compared to the commercial supply. Hence it offers slightly increased efficiency in a dramatically reduced volume.

It should however be noted that the power factor of the offline prototype is very poor (below 0.5) whereas the commercial has a power factor of 0.82. Furthermore the commercial supply is galvanic isolated which the offline prototype is not.

In order to push the power density even further, a prototype has been made were the inductors are implemented as PCB solenoids. The complete converter has a footprint of 16x10x4 mm (LxWxH) and can handle an output power of up to 5 W. This gives a power density of 7.8 W/cm^3 and if the connectors (2 times 2x5 mm on the PCB) are disregarded the power density is 8.9 W/cm^3 (146 W/inch^3). All the components used for this prototype are the same as for the one shown in Figure 7 (except for the inductors), but both sides of the PCB has been used. The series resistances of the PCB inductors are a

bit higher than their discrete counter parts and this causes the efficiency to drop to 80 %.

V. Conclusion

A very compact and cheap converter with state of the art efficiency for VHF converters has been implemented. It is shown that resonant VHF converters using standard MOSFETs can be implemented reducing price and making it possible to design for higher input voltages.

The paper has covered three different prototypes; 1) a basic design of a resonant SEPIC converter with a standard n-channel MOSFET and 84 % efficiency, 2) a offline (230 V_{AC}) prototype with a volume reduced by 80 % compared to a commercial supply and 3) a prototype with PCB inductors and a power density of 8.9 W/cm^3.

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A.6 M. Madsen, A. Knott, M. A.E. Andersen:
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Very High Frequency Half Bridge DC/DC Converter

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***Abstract*— This paper presents the first, off chip, class DE (resonant half bridge) converter working in the Very High Frequency (VHF) range. The benefits of using half bridge circuits both in the inverter and rectifier part of a VHF resonant dc/dc converter are analyzed and design equations for all components in the power stage are given. The circuit has been simulated to verify the accuracy of the presented equations and an efficiency of 89% has been shown.**

A prototype has been implemented with self-oscillating resonant gate drives driving the switches. The prototype has been used to drive an LED string and shows an efficiency of 85% at 29 MHz with 130 V input and 13.4 W output. The efficiency was above 82% in the range 110-150 V input with output power between 10.3 W and 16.5 W.

I. Introduction

In the early 70s the constant strive for small, cheap and efficient power supplies lead to the development of Switch-Mode Power Supplies (SMPS) [1]. As the size of modern power supplies are mainly governed by the passive energy storing elements, which scales inversely with the switching frequency, this strive has lead to constantly increasing switching frequencies ever since. Commercially available converters today switch at frequencies up to several megahertz and can have efficiencies of more than 95% (e.g. [2]).

The reason not to increase the switching frequency further and thereby reaching even higher power densities are the switching losses. In order to avoid switching losses and be able to increase the frequency while keeping the efficiency high, new topologies have to be used. For more than two decades (since 1988 [3]) research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc/dc converters. With this type of converters SMPS with switching frequencies in the Very High Frequency range (VHF, 30-300 MHz) have been designed with efficiencies up to approx. 90%, [4], [5].

Several of the benefits and challenges of the increased switching frequency are described in [6], [7]. One of the great benefits in terms of size and price is, that if the frequency is increased enough, some of the components can be left out as they can be constituted by the parasitic parts of other components or embedded in the PCB [8], [9]. One of the remaining challenges is the huge peak voltage across the MOSFET seen in most resonant circuits [10], [11]. The class DE inverter does not have this stress as the two MOSFETs act as each others clamps, but requires a high side gate drive which is another challenge.

In section II of this paper different resonant topologies suited for switching frequencies in the VHF range are compared. A new type of self-oscillating resonant gate drive suitable for high side gate drive at VHF is introduced in III. The design equations are verified in section IV and the theoretical efficiency is calculated. In section V experimental result are shown and finally section VI concludes the paper.

II. Comparison of Single and Two Switch Topologies

The converter analyzed and implemented in this paper is designed to meet the specifications listed in table I. The load could either be resistive or appear as a voltage source, e.g. a battery or an array of LEDs.

TABLE I
Design specification for the converter.

f_S	V_{IN}	V_{OUT}	P_{OUT}	R_L
30 MHz	100 V	40 V	10 W	160 Ω

Resonant converters are often designed in two parts, an inverter converting the dc input voltage to an ac current and a rectifier converting the ac current to a dc output voltage [12], [13]. The two parts are designed individually, but the design of the inverter is dependent on the input impedance of the rectifier.

It is possible to design the inverter to a load, which give optimal operating conditions for the inverter, and then use different resistance compression networks to make the impedance of the rectifier match [14]–[16]. Though this is a solution often used, it will increase the complexity of the converter unnecessarily and possibly reduce the achievable efficiency, size, and price. Therefore the design procedure will be firstly to design a rectifier for the given load and then design the inverter for the given input and rectifier impedance.

The rectifiers most commonly used in resonant converters switching in the VHF range are class E derived topologies [17], [18], consisting of a low pass filter with a cut of frequency at the switching frequency, a diode in parallel with the capacitor and an output capacitor to insure a constant output voltage. These all have a peak voltage across the diode of approx. 3.6 times the output voltage for a duty cycle of

50% [19], [20]. With an output voltage of 40 V this gives a peak diode voltage stress of almost 150 V, greatly limiting the number of suitable schottky diodes.

For this output voltage a half bridge solution (class DE [21]) is more suitable as the diodes are connected directly to the output and the voltage across them hence is limited to the output voltage (see Fig. 1). Furthermore the class DE rectifier is inductor less and hence offers a much higher power density, as the inductor is generally the biggest component.

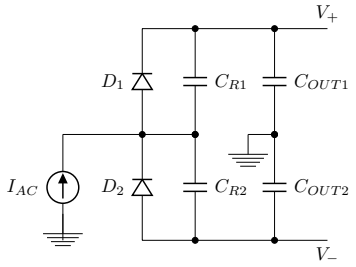

Fig. 1. Schematic of the class DE rectifier.

For the inverter part it is again the class E derived topologies that are most commonly used, this could be either a class E [22], [23], a class EF_2 (ϕ_2) [24], [25], a resonant SEPIC [26], [27] or a resonant boost converter [10], [28]. This is generally chosen due to complexity and losses connected with a high side gate drive for operation in the VHF range.

As for the rectifier, a class E derived inverter imposes huge voltage stress across the MOSFET. For the class E, the resonant SEPIC and resonant boost it is 3.6 the input voltage for a duty cycle of 50% [10], [11], for the class EF_2 this is reduced to approximately 2.3-3 times [13], [25]. As for the rectifier, the semiconductors in the class DE inverter are directly connected to the input and the voltage across them is limited to the input voltage (see Fig. 2). The class DE inverter has two other great advantages over the other topologies, it has only a single inductor and due to the lower peak voltage across the MOSFET the stored energy is approximately ten times lower (E = $\frac{1}{2} \cdot C_{OSS} \cdot V^2$), leading to much smaller resonating currents in a buck type converter [29].

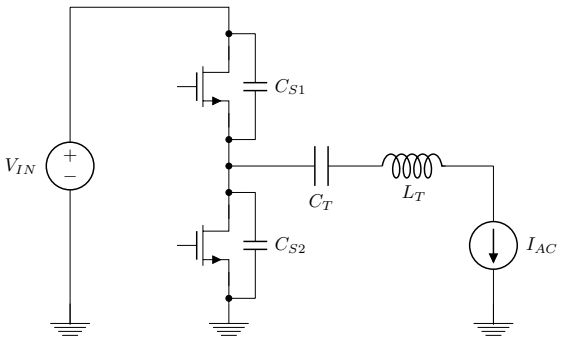

Fig. 2. Schematic of the class DE inverter.

If the maximum output voltage ripple is set to 1% (0.4 V) the values for C_{OUT1} and C_{OUT2} is calculated from eq. 1.

$$C_{OUT} = \frac{I_{OUT}}{V_{OUT,PP}} \cdot \frac{1 - D_D}{f_S} \tag{1}$$

The minimum diode duty cycle D_D is set by the parasitic capacitance of the diodes. Additional capacitance can be added to decrease the duty cycle, this will however increase the amount of resonating currents running in the converter and is hence not desired. The duty cycle for a given capacitance can be calculatec according to eq. 2 [30].

$$\begin{aligned} C_R &= \frac{\pi \cdot (1 - cos(\pi - 2 \cdot D_D \cdot \pi))}{\omega \cdot R_L \cdot (1 + cos(\pi - 2 \cdot D_D \cdot \pi))} \\ &\Updownarrow \\ D_D &= \frac{1}{2 \cdot \pi} \cdot arccos\left(\frac{C_R \cdot R_L \cdot \omega - \pi}{C_R \cdot R_L \cdot \omega + \pi}\right) \end{aligned} \tag{2}$$

The input resistance of the rectifier is calculated through equations from [30] combined to eq. 3.

$$R_{REC} = \frac{2 \cdot R_L}{\pi \cdot (C_R \cdot R_L \cdot \omega + \pi)} \tag{3}$$

If the voltages on both sides of the resonant circuit (C_T and L_T) are assumed to be trapezoidal, the rms voltages in those nodes can be calculated according to eq. 4 and 5.

$$V_{DS,rms} = V_{IN} \cdot \sqrt{\frac{D_M + 1}{3}} \tag{4}$$

$$V_{REC,rms} = V_{OUT} \cdot \sqrt{\frac{D_D + 1}{3}} \tag{5}$$

The reactance of the resonance circuit is calculated according to eq. 6 [31].

$$X_{RC} = R_{REC} \cdot \sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1} \tag{6}$$

Once the reactance of the resonant circuit is calculated, a suitable capacitance can be choosen and the inductance calculated. The capacitors C_{S1} and C_{S2} need to resonate with the resonant circuit at a frequency given by:

$$\omega_R = \frac{\omega}{2 \cdot (1/2 - D_M)} \tag{7}$$

Hence:

$$\omega_R^2 = \frac{1}{2 \cdot C_S \cdot \frac{X_{RC}}{\omega_R}} \tag{8}$$

Combining eq. 7 and 8 leads to the following expresion for the value of C_{S1} and C_{S2}:

$$C_S = \frac{1/2 - D_M}{\omega \cdot X_{RC}} \tag{9}$$

Finally the input capacitance is calculated in the same way as the output capacitance.

III. Self-oscillating resonant gate drive

The class DE inverter requires a high side gate drive and the design of this for VHF have not been presented in any previous publications. The circuits shown at the gates of the MOSFET in Fig. 3 constitutes self-oscillating resonant gate drives capable of making this high side gate signal.

The inductors L_{G1} and L_{G2} combined with the parasitic capacitances of the switches constitutes high pass filters from the drains to the gates of the MOSFETs [32]. If the high pass filters are designed to have the right gain and phase at the resonance frequency of the power stage, a sine wave will apear on the gates of the switches and the inverter will be self oscillating.

The sine wave will have an amplitude given by the gain of the high pass filter at the switching frequency and the peak voltage across the MOSFET. Hence the right gain with 100 V input and a desired gate signal of 12 V_{PP} is -18.4 dB. The phase shift should be as close to 180 ° in order to avoid conduction through the body diode.

In order to design the gate drive a MOSFET has to be chosen so that its parasitics can be taken into account. International Rectifiers IRF5802 HEXFET is chosen to be used due to its 150 V break down and low parasitic capacitances. The 150 V leaves plenty of headroom with 100 V input and the small capacitances leads small resonating currents in the converters. The most important specifications have been extracted from the datasheet and shown in table II.

TABLE II
PARASITIC COMPONENTS OF INTERNATIONAL RECTIFIERS MOSFET IRF5802. PARASITIC CAPACITANCES TAKEN FOR $V_{DS} = V_{IN}/2$.

C_{DS}	C_{GS}	C_{GD}	R_{ON}
13 pF	82 pF	6 pF	1.2 Ω

L_G should now be selected so that the resonance frequency of L_G and the parasitics of the MOSFET is well above the switching frequency, in order to insure close to 180 ° phase shift, but still close enough to ensure the desired gain from drain to source. This can be calculated analytically, but a simple simulation is a faster and more practical approach. Fig. 4 shows the gain and phase with to values of L_G and with and without 39 pF added between the gate and source of the MOSFET.

From the plot it can be seen that the desired response can be achieved either with a 200 nH inductor or with a combination of a 150 nH inductor and a 39 pF capacitor. The phase and gain of the two designs are more or less exactly the same at the switching frequency and the solution with the capacitor is chosen as it will consume least volume.

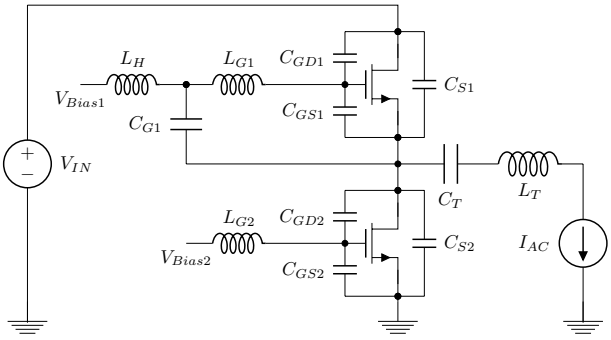

Fig. 3. Schematic of the class DE inverter with self oscillating gate drive.

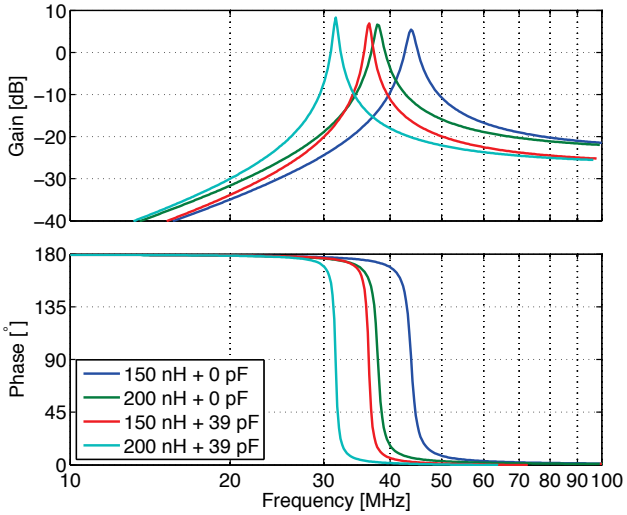

Fig. 4. Gain and phase of the filter from drain to source for different values of C_{GSext} and L_G.

The bias voltages V_{Bias1} and V_{Bias2} can be used to regulate the average of the sine wave and hence shift it up and down in order to control the duty cycle. The low side switch is connected to ground and the V_{Bias2} can therefore be connected directly to the inductor. For the high side switch an additional inductor and capacitor is required. C_{G1} insures that the node between L_H and L_{G1} has a fixed dc offset from source of the high side switch, just like V_{Bias2} for the low side gate drive. The value of C_{G1} should therefore be large enough to keep the voltage across is almost constant for a switching period. L_H is functioning as a choke only allowing dc current to run through it to set the dc voltage across C_{G1}. Setting this 20 times larger than L_G and C_{G1} to 100 nF works well in the VHF range.

IV. Simulation and Fine Tunning

The complete circuit with rectifier, inverter and self-oscillating gate drives are shown in Fig. 5. The MOSFETs for the inverter have already been selected in order to design the gate drive in section III.

In order to design and simulate the rest of the converter the diodes have to be chosen as well. The MBR0540 schottky diodes are chosen as they have low forward voltage drop. The breakdown voltage of these diodes are 40 V, hence there is no headroom to the 40 V output voltage. Two will be used in parallel to reduce the current through a single device. Due to the parasitic capacitance of these diodes C_R will be 40 pF resulting in a diode duty cycle of 32%.

Based on the equations from section II the values of all components have been calculated (see table III). The equations for resonant converters are all based on several assumptions, e.g. pure sine or trapezoidal waves, and the calculated values therefore often have to be fine-tuned [24], [33]. A Spice simulation has been used for this purpose and the simulated waveforms are shown in Fig. 6.

TABLE III
CALCULATED AND TUNED COMPONENT VALUES.

Component	Calculation	Simulation
C_{IN}	4.7 nF	4.7 nF
C_S	14 pF	14 pF
C_{GD}	6 pF	6 pF
C_{GS}	82 pF	82 pF
C_{GSext}	39 pF	39 pF
L_G	150 nH	150 nH
C_{G1}	100 nF	100 nF
L_H	3 uH	3.3 uH
C_T	500 pF	500 pF
L_T	338 nH	390 nH
C_R	40 pF	40 pF
C_{OUT}	14 nF	14 nF

As ceramic capacitors have very high Q factors (more than 1000 [33], [35]), the components causing the major parts of the losses are the MOSFETs, the inductor and the diodes. The losses in the MOSFETs and the inductor are ohmic, the RMS value of the current through these components are therefore measured and shown in table IV. In the diodes the losses are caused by a forward voltage drop and it is hence the average current which is important. The individual component losses and the total loss are listed in table IV and it is seen that an efficiency of 89% (excluding gating losses and drive) is achievable.

The converter is designed with two 150 V HEXFETs [36]. The MOSFET has an on resistance of up to 1.2 Ω at V_{GS} = 10 V and more than 2 Ω when the gate voltage drops below 6.5 V. This causes a significant amount of conduction loss in the MOSFETs, but the low parasitic capacitances loweres the resonating current.

V. IMPLEMENTATION AND VALIDATION

The inverter was designed for 100V input, 30 MHz switching frequency and 10W output power. The converter was implemented according to the simulated values and with square air core inductors from CoilCraft for the resonant tank and gate drive. The output power at 100 V input was 10.14 W,

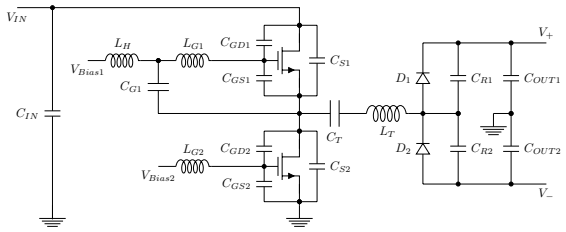

Fig. 5. Schematic of the class DE inverter with DE rectifier and self oscillating gate drive.

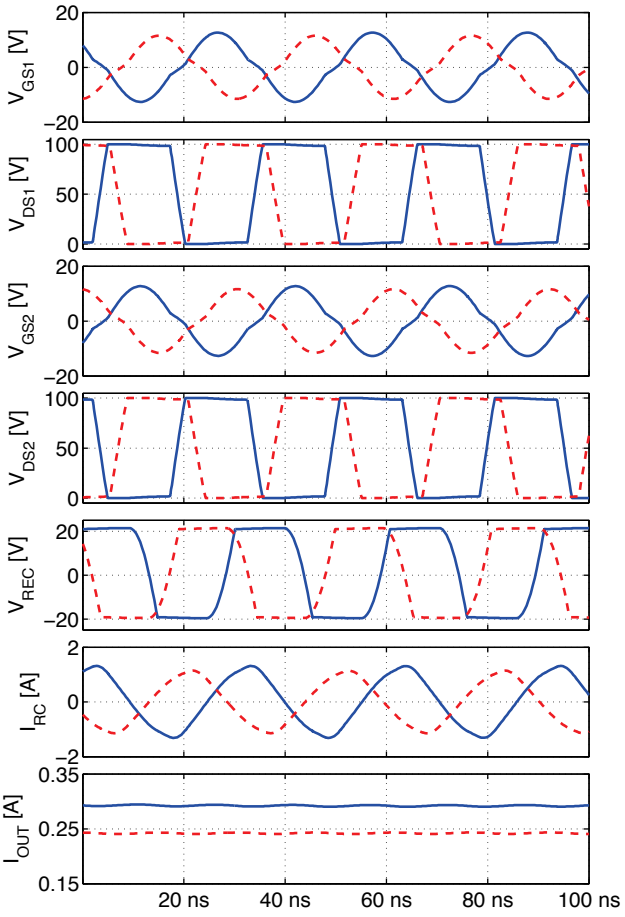

Fig. 6. Simulated waveforms of the class DE inverter and rectifier (solid = calculated values, dashed = tuned values).

TABLE IV
CURRENTS AND ASSOCIATED LOSSES IN THE COMPONENTS CAUSING THE MAIN LOSS.

Component	Current	R or V_F	Loss
S_1	430 mA	2 Ω	370 mW
L_T	777 mA	408 mΩ	246 mW
D_1	0.25 A	460 mV	115 mW
Total			1.22 W

hence very close to the design specifications. The switching frequency was however 29 MHz and the efficiency 77.1% both a bit lower than simulated. A picture of the prototype is shown in Fig. 7 and the thermal picture in Fig. 8 clearly shows the heat caused by the conduction loss in the MOSFETs.

By reducing the inductance in the inductor in the resonant tank to 300 nH, it was possible to increase the switching frequency to 30.5 MHz. This did however also lead to increased output power and changed the efficiency. The output power and efficiency for different values of L_{RC} can be seen in Fig. 9. As it can be seen the peak efficiency is almost 80%, but generally drops below 75% when the output power is increased above 12 W.

Another way to change the switching frequency is to adjust the gate drive. The output power and efficiency for three values of C_{GSext} can be seen in Fig. 10. The plot shows that it is possible to adjust the output power a little bit in this way, but the efficiency remains almost constant.

The implemented converter is technically galvanic isolated by C_T and C_{OUT}. It is therefore possible to stak the input of the converter on top of the output and increase the output power and input voltage in that way. This leads to the input voltage, output power and efficiency shown in Fig. 11. In this way the efficiency is increased to more than 85% and the output power above 15 W.

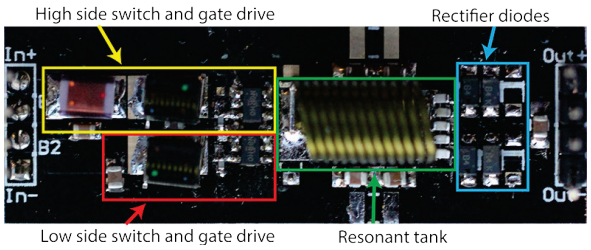

Fig. 7. Picture of the implemented converter on a 50x17 mm PCB.

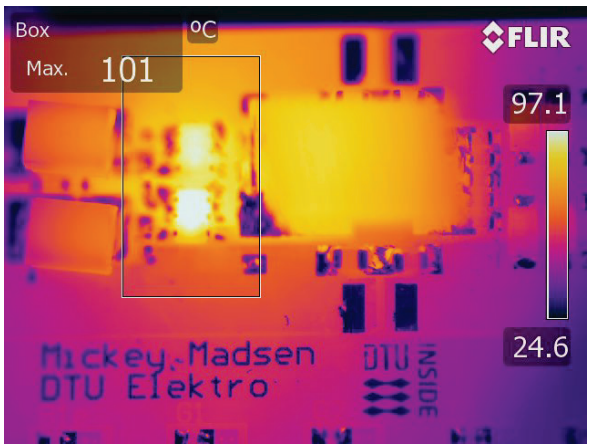

Fig. 8. Measured temperatures of the MOSFETs in the class DE inverter at 130 V input and 13.4 W output.

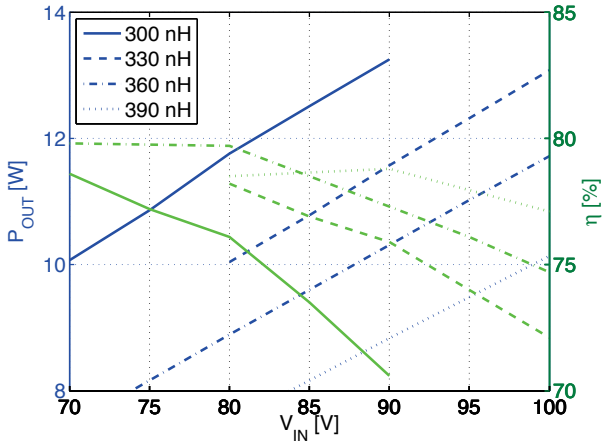

Fig. 9. Output power and efficiency for different values of L_T (C_{GSext} = 39 pF).

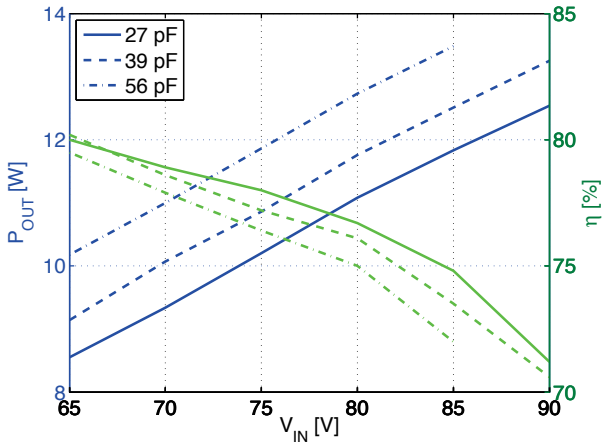

Fig. 10. Output power and efficiency for different values of C_{GSext} (L_T = 300 nH).

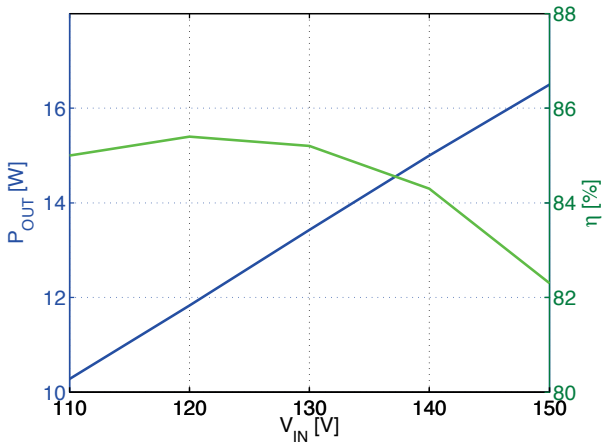

Fig. 11. Output power and efficiency when the input and output of the converter is connected in series.

VI. Conclusion

This paper has shown the design and implementation of the first (discrete) class DE converter working in the VHF range [37], [38]. Accurate equations, which almost eliminate the need for tuning of the resonant circuit, have been presented and demonstrated working.

A new type of self-oscillating gate drive which can be used to drive the high side switch has been presented and the design procedure explained.

Simulations have been presented which shows the accuracy of the formulas and the function of the gate drive. The simulation shows an efficiency of 89%, without gate drive and gating losses, when a HEXFET with high on resistance is used.

The implemented converter has a peak efficiency of 85% and above 82% for a wide input range when the input and output is connected in series across the supply. When used as an isolated converter the peak efficiency is almost 80%.

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A.7 **M. Madsen, M. Kovacevic, J. D. Mønster, J. A. Pedersen, A. Knott and M. A.E. Andersen:**
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Input-Output Rearrangement of Isolated Converters

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***Abstract*— This paper presents a new way of rearranging the input and output of isolated converters. The new arrangement posses several advantages, as increased voltage range, higher power handling capabilities, reduced voltage stress and improved efficiency, for applications where galvanic isolation is not a requirement. The proposed technique is particularly valuable in power conversion at very high frequencies, and may be combined with other stress reduction methods. Finally, the new arrangements are experimentally verified both on off the shelf converters and on a VHF resonant SEPIC converter. All results are in good agreement with the theory and twice the power handling capabilities and 5-10% higher efficiencies are shown.**

I. Introduction

Constant strive for cost and size reduction of power converters, as well as better performance, results in higher and higher switching frequencies. From the size and cost perspective, higher frequencies are desirable since energy storage requirements drop linearly with frequency, even though the components size and price do not typically scale at the same rate. An added benefit is cost and size reduction of filtering components. Recent advances in switching devices technology [1] and magnetic materials [2], [3] allowed converter operation in low-MHz range with high efficiencies [4]–[7]. If the switching frequency is pushed beyond 30 MHz, class E derived topologies - class E, resonant boost, resonant SEPIC, etc. - made it possible to use air-core magnetics, which eliminates core loss mechanism entirely [8], [9].

However, loss mechanisms in the switches start to dominate the total loss budget at higher frequencies. In low-MHz range, switching loss already gives incentive for use of resonant transition or quasi square-wave converter topologies (boost [10], inverted buck [6], flyback [11]). For operation above 30 MHz, switching losses impact converter efficiency so severely that only ZVS (zero voltage switching) topologies become practical. Even then, gating loss needs to be accounted for, regardless of the gating technique: hard-gating, single-resonant, or multi-resonant [12]. Needless to say, proper utilization of the switching components, especially in price-sensitive applications, is a must.

Class E derived converters exhibit voltage stress on the inverter switch of typically between 2.5 and 3.6 times input voltage, depending on the switch duty cycle [13]. As a consequence, devices with high voltage ratings are required. These devices typically perform worse compared to their lower voltage counterparts, as voltage rating comes at the expense of increase in $R_{DS,on}$ with all other parameters held the same. It is therefore of interest to reduce switch voltage blocking requirement in order to improve performance.

Voltage stress in these converters can be reduced by employing multi-resonant networks, either transmission line [14] or discrete with limited number of harmonics [15]–[17]. By implementing these techniques, switch voltage stress in VHF converters can be reduced to 2-2.5 times input voltage for the same duty cycle, but this technique requires extra resonant elements. Another approach infers single switch quasi square-wave converter topologies. The downside of quasi square-wave converters is limited converter transformation ratio (inverted buck, boost), or excessive ringing on the primary switch due to leakage inductance (flyback). In [18] a self-oscillating drive method was used to obtain a VHF self-oscillating DE inverter, in which the switch voltage stress is limited to input voltage. Finally, converter cell stacking [19], [20] reduces the switch voltage stress by N compared to a single cell case, where N is the number of converter cells. However, control becomes more complicated since it is required to balance voltages across the cells, and certain start-up issues may occur.

This paper presents a voltage stress reduction method, which may be used in either step-up or step-down applications where galvanic isolation is not a requirement. In addition to voltage stress reduction, it results in higher converter efficiency with minimum adjustments to the original circuit. Section II describes the method in detail. Section III shows experimental results when the principle is applied to conventional off-the-shelf design and a VHF prototype, respectively. Finally, Section IV concludes the paper.

II. The basic principle

Fig. 1 shows the conventional input-output configuration of an isolated dc/dc converter. If two isolated converters have their inputs connected in parallel and outputs connected in series, we obtain the structure in Fig. 2 (top). Similarly, if the inputs are connected in series and outputs in parallel, the structure in Fig. 3 (top) is obtained. Let us assume that one of the converters in each configuration is with 1:1 voltage transformation ratio. In such case, it is possible to connect its

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input to its output directly and remove 1:1 converter from the circuit, without effecting the rest of the system. In doing so, part of the delivered power flows directly from input to the output, and is not processed by the converter. As a consequence, higher converter efficiency is achieved. Moreover, compared to the single cell design, voltage and/or current stresses on the switches are reduced. The only difference is that the input is not galvanic isolated from the load. Fig. 2 and 3 (bottom) demonstrate the final connection rearrangement to obtain step-up and step-down configuration, respectively.

To quantify the benefits from the proposed configurations, we analyze the case where input voltage V_{in} and output voltage V_{out} are held constant across all configurations. Moreover, output current I_{out} and output power P_{out} are held constant as well. A distinction is made between the power processed by the converter P_C, and P_{out}.

Voltage transformation ratio of the conventional converter is

$$M = \frac{V_{out}}{V_{in}} \tag{1}$$

In step-up and step-down configurations, transformation ratio of the converter cell only becomes

$$M_{up} = \frac{V_{out} - V_{in}}{V_{in}} \tag{2}$$

$$M_{down} = \frac{V_{out}}{V_{in} - V_{out}} \tag{3}$$

In general, switch voltage stress is a function of both input and output voltages. In step-up configuration, output voltage stress contribution is reduced by a factor of $(1 - V_{in}/V_{out})$. In step-down configuration, input voltage stress contribution is reduced by $(1 - V_{out}/V_{in})$.

Output power of all three configurations is the same:

$$P_{out} = V_{out}\ I_{out} \tag{4}$$

The power processed by the converter P_C in the conventional structure is equal to P_{out}. In the step-up and step-down cases, this power is given as

$$P_{C,up} = P_{out}\left(1 - \frac{V_{in}}{V_{out}}\right) \tag{5}$$

$$P_{C,down} = P_{out}\left(1 - \frac{V_{out}}{V_{in}}\right) \tag{6}$$

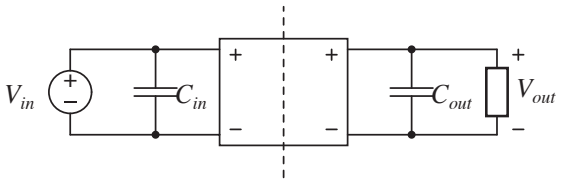


Fig. 1. Conventional isolated dc/dc converter topology. Dashed line represents galvanic isolation.

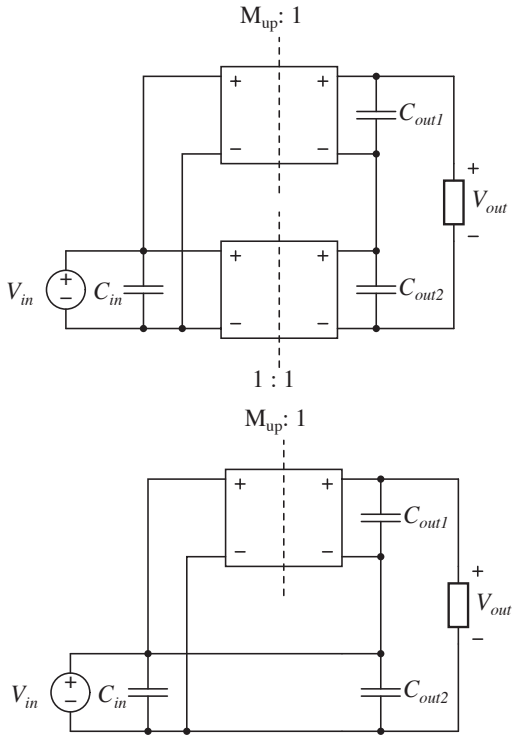


Fig. 2. Step-up configuration: two converter cells with inputs in parallel and outputs in series (top) and a single cell equivalent (bottom).

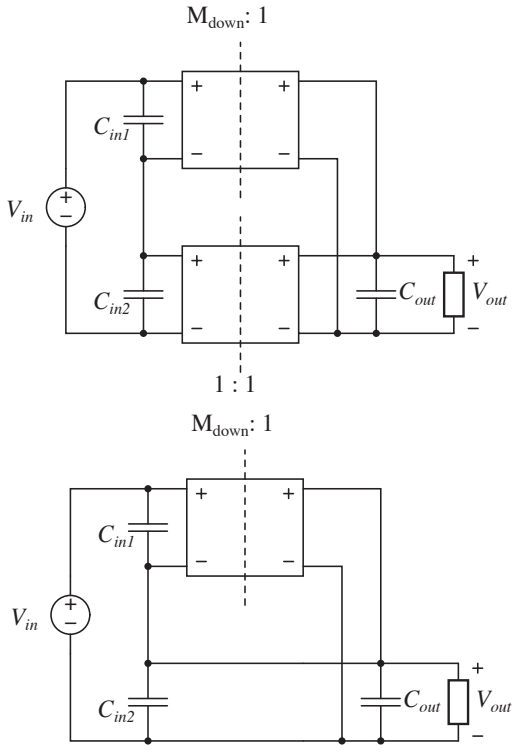


Fig. 3. Step-down configuration: two converter cells with inputs in series and outputs in parallel (top) and a single cell equivalent (bottom).

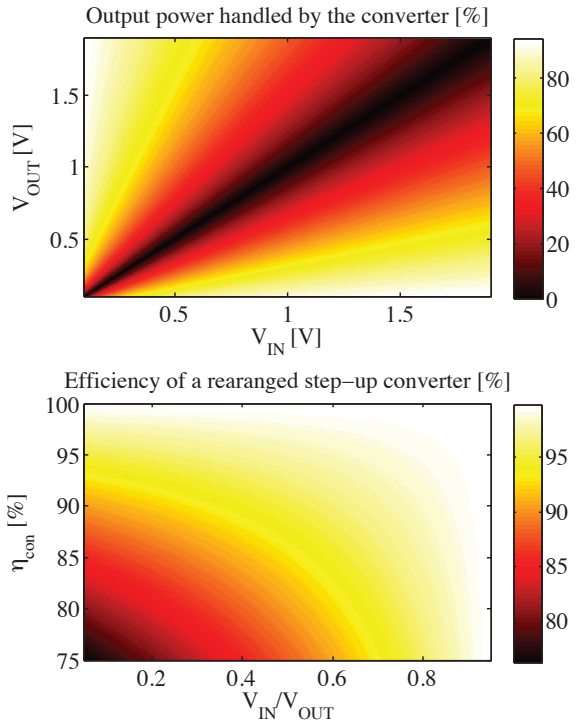


Fig. 4. Power processed by the converter and efficiency improvement by rearranging.

$P_{C,up}$ and $P_{C,down}$ are smaller than P_{out}, and the remaining power is delivered through the DC path. Efficiency of that power transfer is very close to 100%. Assuming that P_C, $P_{C,up}$, and $P_{C,down}$ are transfered with the same efficiency η, effective efficiencies of the step-up and step-down configurations can be expressed in terms of η, P_{out}, and $P_{C,up/down}$:

$$\eta_{up/down} = \eta \frac{P_{C,up/down}}{P_{out}} + \frac{P_{out} - P_{C,up/down}}{P_{out}} \qquad (7)$$

Equations 5-7 are illustrated in Fig. 4. The plot clearly shows that for limited step-up or step-down ratios, the percentage of the output power processed by the converter is small and hence the efficiency improvement becomes significant. For a step-up converter with 330V input and 400V output only 17.5% of the output power would be processed by the converter and if the converter efficiency were 80%, the rearranged efficiency would be 96.5%. The converter would in that case have to be designed as an galvanic isolated converter with 330V input, 70V output and a peak output power equal to 17.5% of the required power. Hence a high power boost converter with high efficiency could be replaced by a low power flyback or SEPIC converter with moderate efficiency while achieving the same overall system performance.

Adaptations shown in Fig. 2 and 3 can be used for any type of isolated converter, regardless of the isolation type (inductive or capacitive). In Fig. 5, a flyback converter is used in a step-up configuration, along with simulated waveforms. Fig. 6 presents

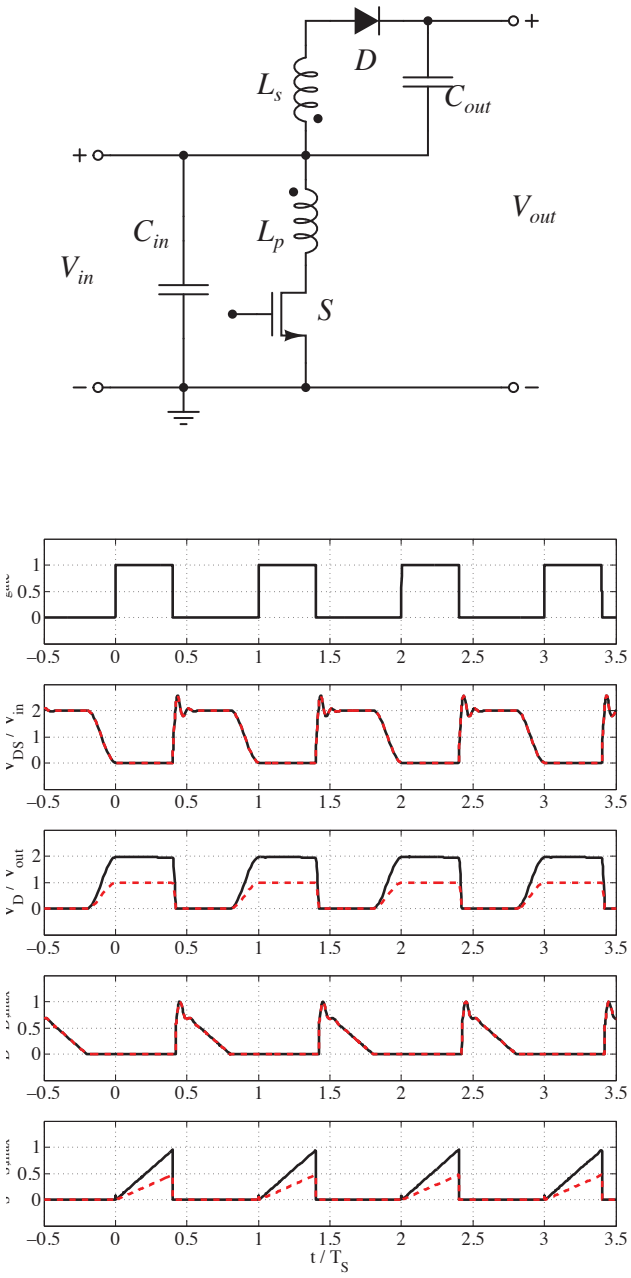


Fig. 5. Flyback converter in step-up configuration (top) and simulated waveforms of a quasi square-wave 1:2 flyback converter in conventional (solid black) and step-up (dashed red) configuration. Diode voltage and switch current stresses are reduced by a factor of 2. Output capacitance is formed by series connected C_{out} and C_{in}.

a class DE converter (DE inverter and DE rectifier) in step-down configuration.

The proposed technique may be used together with multi-cell stacked designs, as shown in Fig. 7. This also adds complexity to control circuitry since it needs to monitor and balance voltages across the cells.

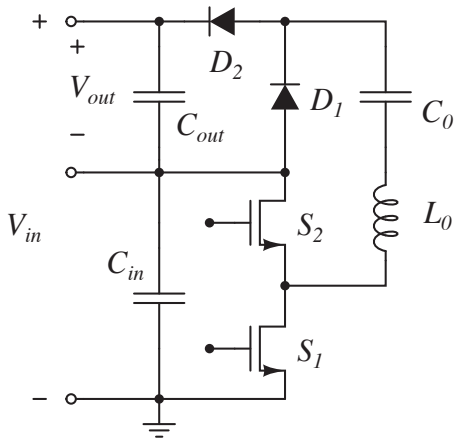


Fig. 6. Class DE converter in step-down configuration with output referenced to the inverter input. Parasitic capacitances of the switching devices are included implicitly.

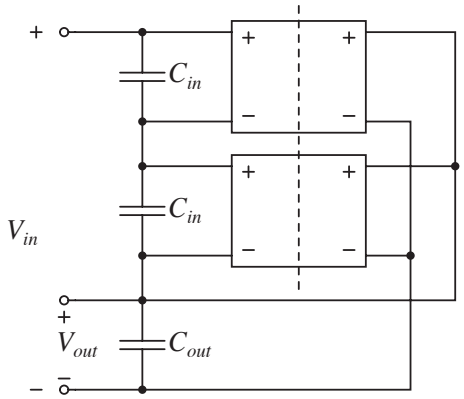
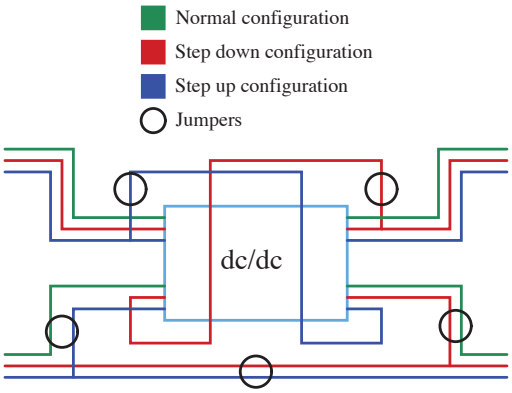
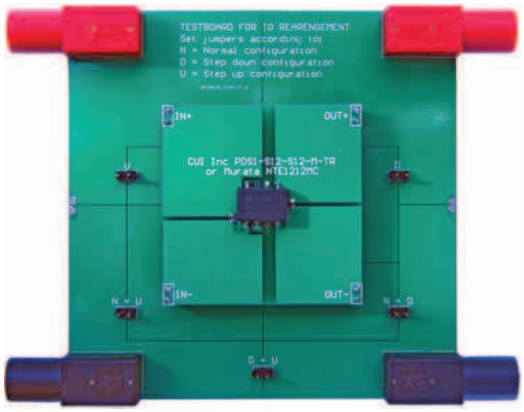


Fig. 7. Two stacked converters in step-down configuration.



(a) Schematic



(b) PCB

Fig. 8. Test board for evaluation of the principle.

III. Experimental Results

A. Off the shelf converter

In order to experimentally verify equation 5-7 a test setup with two isolated 12-12V DC/DC converters (Murata NTE1212MC and CUI Inc PDS1-S12-S12-S) has been made. The setup is made with five jumpers allowing the setup to be changed between normal configuration (12-12V), step down (24-12V) and step up (12-24V).

The measured efficiency as function of output power is shown in Fig. 9. The increased efficiency and power handling capability in the new configurations are clearly seen. With a 1-2 or 2-1 step ratio the converter only handles 50% of the output power (see equation 5-6). The power handling capability is hence doubled while the efficiency is increased across the entire load range with half the loss at full load.

B. Resonant SEPIC converter

As mentioned in Section I, the input and output voltage and the subsequent voltage stress on the semiconductors is of high importance in resonant converters. The availability of

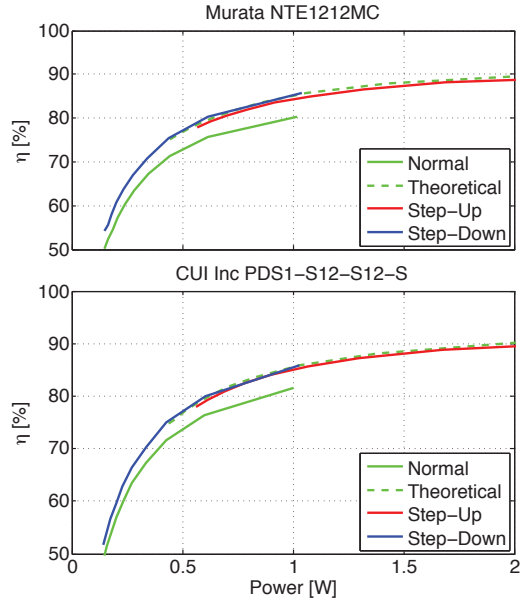


Fig. 9. Measured performance improvements of two rearranged converters.

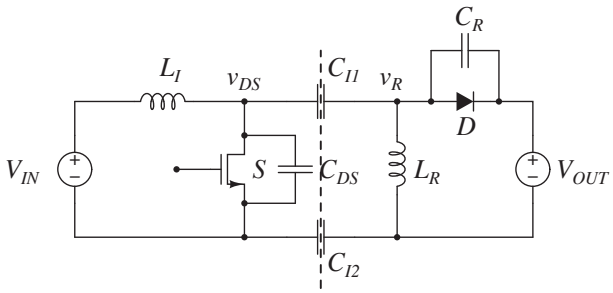


Fig. 10. Resonant SEPIC converter with capacitive galvanic isolation.

suitable semiconductors is reduced significantly as the break down voltage requirement gets above 100 V. Furthermore the amount of resonating current needed in order to achieve zero voltage switching scales with the voltage squared, hence a reduction in input and output voltage will lead to significantly lower currents and thereby also reduced losses due to ESR in the components.

As the switching loss in resonant converters with ZVS is reduced to a minimum, these converters are operable at several tens of MHz [12], [15]–[19], [21]–[32]. At these frequencies, galvanic isolation can be achieved simply by adding a small capacitor in the return path between the inverter and rectifier.

The proposed rearrangement is hence extremely well suited for non-isolated converters where very high frequency resonant converters can be used to achieve high power density, low cost and weight and still keep the efficiency high. In order to show the benefit in these type of converters a resonant SEPIC converter (see Fig. 10) switching at 50 MHz has been implemented and tested on the test board in Fig. 8.

Figure 11 shows the performance improvements measured with this setup. From the plot it is clearly seen that both the efficiency and the voltage and power handling capability are increased. The measurements and theoretical values for the step down version fits well as the loading conditions as well as the input voltage are the same. For the step-up version the output voltage from the converter changes quite dramatically as the input voltage is increased and becomes close to zero towards the end.

In [18] the same principle is shown for a capacitively isolated VHF class DE converter. Here the rearangement increases the efficiency by 5-10% across a wide input voltage range. At the same time the input voltage and output power is increased by approx 50%.

IV. Conclusion

The paper presents a voltage and/or current stress reduction technique for isolated dc-dc converters in applications where isolation is not a requirement. The technique provides higher efficiency compared to a conventional single cell design, and it can be combined with other methods of voltage stress reduction, as long as the initial converter provides capacitive or inductive isolation. Obtained benefits are considered very appealing for certain non-isolated applications, such as LED

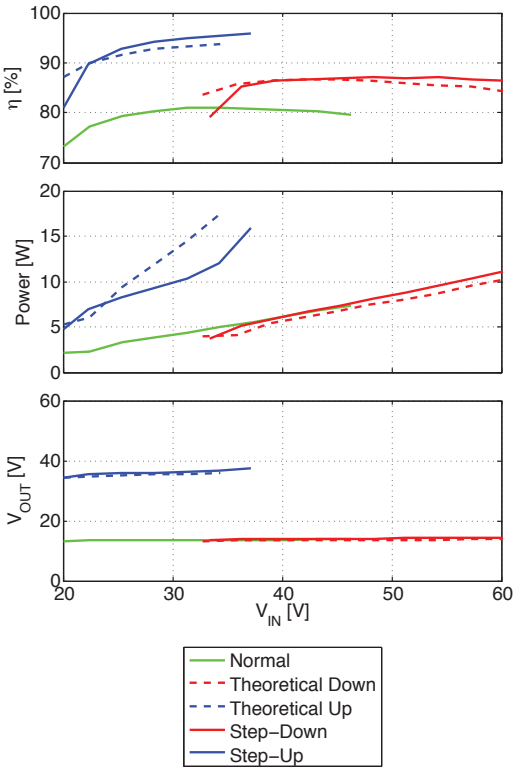


Fig. 11. Measured performance improvement of a VHF resonant SEPIC.

lighting. Theoretical analysis and experimental results are provided and are in good agreement. Twice the power handling capabilities and 5-10% higher efficiencies are shown for the tested converters.

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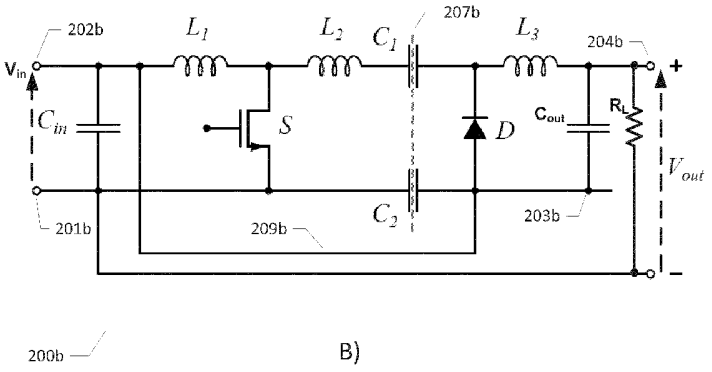

FIG 2

(57) **Abstract**: The present invention relates to a step-up DC-DC power converter which comprises a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier. The primary side circuit comprises a positive and a negative input terminal for receipt of an input voltage and an input capacitor coupled between the positive and negative input terminals and the secondary side circuit comprises an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode. A switched energy storage network is configured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce the converter output voltage. The step-up DC-DC power converter comprises an electrical short-circuit connection across the galvanic isolation barrier connecting, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connecting the second positive electrode of the output capacitor to the negative input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor. A load connection is established, in the first case, between the first positive electrode of the output capacitor and the negative input terminal or, in the second case, between the second negative electrode of the output capacitor and the positive input terminal.

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STEP-UP DC-DC POWER CONVERTER

The present invention relates to a step-up DC-DC power converter which comprises a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier. The primary side circuit comprises a positive and a negative input terminal for receipt of an input voltage and an input capacitor coupled between the positive and negative input terminals and the secondary side circuit comprises an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode. A switched energy storage network is configured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce the converter output voltage. The step-up DC-DC power converter comprises an electrical short-circuit connection across the galvanic isolation barrier connecting, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connecting the second positive electrode of the output capacitor to the negative input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor. A load connection is established, in the first case, between the first positive electrode of the output capacitor and the negative input terminal or, in the second case, between the second negative electrode of the output capacitor and the positive input terminal.

BACKGROUND OF THE INVENTION

Power density and component costs are key performance metrics of both isolated and non-isolated DC-DC power converters to provide the smallest possible physical size and/or lowest costs for a given output power requirement or specification. Resonant power converters are particularly useful for high switching frequencies such as frequencies above 1 MHz where switching losses of standard SMPS topologies (Buck, Boost etc.) tend to be unacceptable for conversion efficiency reasons. High switching frequencies are generally desirable because of the resulting decrease of the electrical and physical size of circuit components of the power converter like inductors and capacitors. The smaller components allow increase of the power density of the DC-DC power converter. In a resonant power converter an input "chopper" semiconductor switch (often MOSFET or IGBT) of the standard SMPS is replaced with a "resonant" semiconductor switch. The resonant semiconductor switch

relies on resonances of circuit capacitances and inductances to shape the waveform of either the current or the voltage across the semiconductor switch such that, when state switching takes place, there is no current through or no voltage across the semiconductor switch. Hence power dissipation is largely eliminated in at least some of the intrinsic capacitances or inductances of the input semiconductor switch such that a dramatic increase of the switching frequency becomes feasible for example to values above 10 MHz. This concept is known in the art under designations like zero voltage and/or zero current switching (ZVS and/or ZCS) operation. Commonly used switched mode power converters operating under ZVS and/or ZCS are often described as class E, class F or class DE inverters or power converters.

In view of the above, it remains a challenge to reduce the size and lower the component costs of both isolated and non-isolated DC-DC power converters. Hence, novel step-up DC-DC power converter topologies which reduce the required maximum voltage rating of active and passive components of the DC-DC converter are highly desirable. Likewise, novel step-up DC-DC power converter topologies which reduce the physical size or cost of active and passive components for example inductors, capacitors, transistors and diodes are highly desirable.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a step-up DC-DC power converter which comprises a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier. The primary side circuit comprises a positive and a negative input terminal for receipt of an input voltage and an input capacitor coupled between the positive and negative input terminals and the secondary side circuit comprises an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode. A switched energy storage network is configured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce the converter output voltage. The step-up DC-DC power converter comprises an electrical short-circuit connection across the galvanic isolation barrier connecting, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connecting the second positive electrode of the output capacitor to the nega-

tive input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor. A load connection is established, in the first case, between the first positive electrode of the output capacitor and the negative input terminal or, in the second case, between the second negative electrode of the output capacitor and the positive input terminal.

The present invention is described in detail in the following with reference to specific implementations in isolated resonant DC-DC power converters of Class E, DE and SEPIC topologies and a non-resonant flyback DC-DC converter topology. The skilled person will understand that the invention is equally applicable to other types of isolated resonant and non-resonant DC-DC power converter such as class π_2 inverters and rectifiers and resonant boost, buck, LCC converters etc.

The skilled person will understand that the electrical short-circuit connection across the galvanic isolation barrier eliminates the galvanic isolation between the primary and secondary side circuits of the step-up DC-DC converter by interconnecting the second electrode of the output capacitor and the negative input terminal. However, the electrical short-circuit connection provides numerous new benefits to the DC-DC converter as a whole and the lack of galvanic isolation is acceptable in numerous applications where the converter circuit is isolated from users such as retrofit LED bulbs and tubes. The series connection of the output and input capacitors established by the electrical short-circuit connection has the effect that the secondary side circuit only needs to supply the output voltage minus the input voltage of the present step-up DC-DC converter, instead of the entire converter output voltage as in ordinary isolated DC-DC power converters, to a converter load. The converter load is coupled between either the first positive electrode of the output capacitor and the negative input terminal or between the second negative electrode of the output capacitor and the positive input terminal depending on the connection points of the electrical short-circuit connection as explained in further detail below with reference to FIGS. 1A), 1B) and 1C). Consequently, since, the switched energy storage network only supplies a fraction of the converter output voltage it also supplies only a corresponding fraction of the total power to the converter load. The reduced voltage in the secondary side circuit of the step-up DC-DC power converter reduces the

required maximum voltage rating of active and passive components therein such as semiconductor switch or switches, inductor(s), capacitors, diode(s) etc. The reduced maximum voltage rating of the active and passive components leads to physically smaller and/or less costly active and passive components. In addition, the life span of the latter components may increase by the smaller voltage stress. Likewise, in the primary side circuit the smaller amount of power to be transferred through the step-up DC-DC converter for a given amount of output power delivered to the converter load leads to reduced power requirements for active semiconductors switches allowing less costly and physically smaller semiconductors to be applied.

The beneficial reduction of the amount of power to be transferred through the switched energy storage network is achieved because the residual fraction of the output power is transferred directly from the input voltage source and input capacitor to the output capacitor due to their series connection as explained in further detail below with reference to FIGS. 1A), 1B) and 1C).

The skilled person will appreciate that the switched energy storage network can comprise numerous types of ordinary switch topologies such as a single switch topology, a half-bridge switch topology or full-bridge switch topologies. The switched energy storage network preferably comprises at least one semiconductor switch such as a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) transistor. A control terminal, e.g. a gate or base, of the at least one semiconductor switch may be coupled to, and driven by, the switch control signal to alternatingly force the least one semiconductor switch between on-states and off-states. In the on-state an inductor of the switched energy storage network may be charged with energy from the input voltage source and in the following off-state release stored energy to the output capacitor to charge the latter. The secondary side circuit of the step-up DC-DC converter may comprise a rectifying element such as a diode or transistor inserted in front of the converter load.

The galvanic isolation barrier may comprise a transformer which comprises a pair of magnetically coupled inductors comprising a first inductor electrically connected to the primary side circuit and a second inductor electrically connected to the secondary side circuit. The first and second inductors could be discrete windings both

wound around a common magnetic permeable structure to form an isolation transformer. In an alternative embodiment, the first and second inductors are integrated in a printed circuit board without intervening magnetic material. The printed circuit board could have the entire step-up DC-DC power converter mounted thereon.

In yet another embodiment, the galvanic isolation barrier comprises a first capacitor coupled in series with the positive input terminal of the primary side circuit and the first positive electrode of the output capacitor and a second capacitor coupled in series with the negative input terminal of the primary side circuit and the second negative electrode of the output capacitor. Each of the first and second capacitors may possess particularly small physically dimensions in step-up resonant DC-DC power converters with a switching frequency, or frequency of the switch control signal, at or above 10 MHz. In the latter embodiments each of the first and second capacitors may comprise a ceramic capacitor and may possess a capacitance smaller than 10 nF such as smaller than 1 nF such as smaller than 100pF. Isolation capacitors with these capacitances may be SMD mounted ceramic capacitors with a very small footprint as discussed below.

The skilled person will appreciate that a practical electrical short circuit connection will possess a finite DC resistance and an upper limit of this finite DC resistance will vary depending on input/output voltage and/or current requirements of the step-up DC-DC power converter. The electrical short-circuit connection may possess a DC resistance of less than 1 kΩ, even more preferably less than 100 Ω, such as less than 10 Ω. In other embodiments, the electrical short circuit connection may have a unidirectional resistance such that the DC resistance only falls below the above-mentioned upper limits in one direction and exhibits a much larger DC resistance in the opposite direction, i.e. a diode characteristic

One embodiment of the step-up DC-DC power converter is based on a Class E converter and the switched energy storage network comprises first and second series connected inductors which are connected in series with the positive input terminal. A semiconductor switch is arranged with a first switch node connected between a mid-point node between the first and second series connected inductors and a second switch node connected to the negative input terminal of the primary side circuit. A

control terminal of the semiconductor switch is connected to the switch control terminal; and a third inductor has a first end connected to a second end of the second inductor through the first capacitor of a galvanic isolation barrier and a second node connected to the converter output voltage at the positive electrode of the output capacitor. A rectifier is connected between the first end of the third inductor and the negative electrode of the output capacitor.

Another embodiment of the step-up DC-DC power converter is based on a flyback converter topology wherein the first and second inductors of the isolation transformer are integrated in the switched energy storage network. The first inductor is arranged with a first inductor end connected to the positive input voltage terminal and a second inductor end connected to a first node of a semiconductor switch such as a drain terminal of a MOSFET switch. A second node of the semiconductor switch is connected to the negative input terminal of the primary side circuit. The second inductor of the isolation comprising a first inductor end connected to the first positive electrode of output capacitor and a second inductor end connected to the second negative electrode, respectively, of the output capacitor through a rectifier.

The step-up DC-DC power converter may comprise a resonant DC-DC power converter to facilitate zero voltage and/or zero current switching of the semiconductor switch or switches of the switched energy storage network as discussed in additional detail below. The resonant DC-DC power converter is particularly advantageous at high switching frequencies of the switch control signal such as above 10 MHz or above 20 MHz such as at or above 30 MHz as discussed below.

The step-up DC-DC power converter may comprise a mode selecting semiconductor switch which is configured to switch the step-up DC-DC power converter between two distinct modes of operation. According to this embodiment, the step-up DC-DC power converter comprises a rectifying element, such as a diode, coupled between the positive input terminal and second negative electrode of the output capacitor. The mode selecting semiconductor switch which is configured to selectively break and close the electrical short-circuit connection such that:
in a first mode of the step-up DC-DC power converter, establishing the series connection of the output capacitor and the input capacitor; and

in a second mode of the step-up DC-DC power converter, break the series coupling of the output capacitor and the input capacitor.

The mode selecting semiconductor switch may be switched between a conducting state and non-conducting state by a suitable control voltage applied on a control terminal of the mode selecting semiconductor switch such as a gate terminal of a MOSFET or FET semiconductor switch or base terminal of a BJT or IGBT semiconductor switch. A mode controlling circuit connected to, or integrated with, the step-up DC-DC power converter may be configured to supply this control voltage to the mode selecting semiconductor switch. The first mode of the step-up DC-DC power converter is selected in the conducting or ON state of the mode selecting semiconductor switch and the second mode of the step-up DC-DC power converter is selected in the non-conducting or OFF state of the mode selecting semiconductor switch. The rectifying element may comprise an ordinary diode or an active diode for example a semiconductor switch configured for diode operation by a suitable control signal applied to a control terminal of the semiconductor switch,

The mode switching feature of this embodiment of the step-up DC-DC power converter provides several advantages such as increasing the dynamic voltage operating range of the converter as discussed in additional detail below with reference to the appended drawings.

In a range of particularly advantageous embodiments of the present step-up DC-DC power converters the switch control signal of the switched energy storage network is placed in the so-called VHF range with a switching frequency at or above 10 MHz, or more preferably at or above 20 MHz such as at or above 30 MHz. These step-up DC-DC power converters preferably comprises resonant topologies as mentioned above to facilitate zero voltage and/or zero current switching of the semiconductor switch or switches of the switched energy storage network. The VHF operation of these step-up DC-DC power converters provides considerable decrease of the electrical and physical size of active and passive components such as the previously discussed inductors and capacitors. Hence the previously mentioned transformer or capacitors of the galvanic isolation barrier of the present step-up DC-DC power converter can be physically small and inexpensive. The capacitor based galvanic isola-

tion becomes particularly advantageous in the VHF frequency range as the capacitance of each of the isolation capacitors can be small, such as 10 nF or even smaller in some cases for example smaller than 1 nF such as about 100pF. Isolation capacitors with these capacitances may comprise SMD mounted ceramic capacitors with a very small footprint e.g. a footprint less than 1 cm^2 for example a footprint down to about 4 mm^2. In VHF frequency range operating embodiments of the step-up DC-DC power converter, such resonant step-up DC-DC power converters, each of the input capacitor and the output capacitor may have a capacitance smaller than 100 nF. The skilled person will understand that the input and output capacitors in certain embodiments of the invention may be formed exclusively by a parasitic capacitance associated with the primary side circuit and the secondary side circuit, respectively.

The skilled person will furthermore understand that each of the present step-up DC-DC power converters may be constructed by conversion of an isolated DC-DC power converter with a corresponding topology as described in additional detail below with reference to FIGS. 2A) - 2B) FIGS. 3A) - 3B), FIGS. 4A) - 4B) and FIGS. 5A) - 5B). Hence, a second aspect of the invention relates to a method of converting an isolated DC-DC power converter to a step-up DC-DC power converter with higher power conversion efficiency, said method comprising steps of:

providing a primary side circuit and a secondary side circuit of the isolated DC-DC power converter,

coupling an input capacitor between a positive and a negative input terminal of the primary side circuit,

coupling an output capacitor between a positive and a negative terminal of the secondary side circuit,

providing electrical coupling of the primary side circuit and the secondary side circuit through a galvanic isolation barrier,

providing a switched energy storage network configured for alternatingly being charged from an input voltage of the converter and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce a converter output voltage,

connecting, in a first case, an electrical short-circuit across the galvanic isolation barrier from the negative output terminal of the secondary side circuit to the positive

input terminal of the primary side circuit or connecting, in a second case, the positive output terminal of the secondary side circuit to the negative input terminal of the primary side circuit thereby establishing in both the first case and the second case a series coupling of the output capacitor and the input capacitor,

coupling, in a first case, a power converter load between the positive terminal of the secondary side circuit and the negative input terminal or coupling, in the second case, the power converter load between the negative terminal of the secondary side circuit and the positive input terminal of the primary side circuit.

A preferred embodiment of the above conversion methodology generates the previously discussed step-up DC-DC power converter with the mode switching feature. This is achieved by adding further method steps of:

connecting a rectifying element, such as a diode, between the positive input terminal and second negative electrode of the output capacitor; and

inserting a mode selecting semiconductor switch into the electrical short-circuit connection for selectively breaking and closing/making the short circuit connection such that:

establishing the series connection of the output capacitor and the input capacitor in a first mode of the step-up DC-DC power converter; and

breaking or disconnecting the series coupling of the output capacitor and the input capacitor in a second mode of the step-up DC-DC power converter.

The higher power conversion efficiency of the present step-up DC-DC power converter embodiments is achieved because a considerable amount of the power delivered to the converter load may be transferred directly from the input voltage source and input capacitor of the input side circuit to the output capacitor of the output side circuit due to the series connection of the input and output capacitors provided by the electrical short circuit connection as explained above. Hence, a smaller amount of power has to be transferred through the switched energy storage network and isolation barrier leading to lower power losses in the active and/or passive components thereof. The isolated DC-DC power converter may comprise a resonant DC-DC power converter, preferably a resonant DC-DC power converter where the frequency of the switch control signal of the switched energy storage network has a

frequency at or above 10 MHz such as at or above 20 MHz, more preferably at or above 30 MHz.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention will be described in more detail in connection with the appended drawings, in which:

FIGS. 1A) and 1B) are simplified electrical circuit diagrams illustrating a step-up DC-DC power converter in accordance with a first embodiment of the present invention,

FIG. 1C) is a simplified electrical circuit diagram of a step-up DC-DC power converter in accordance a second embodiment of the invention,

FIG. 1D) is a simplified electrical circuit diagram of a step-up DC-DC power converter in accordance a third embodiment of the invention,

FIG. 1E) is simplified electrical circuit diagram of a step-up DC-DC power converter in accordance a fourth embodiment of the invention,

FIG. 1F) is simplified electrical circuit diagram of a step-up DC-DC power converter in accordance a fifth embodiment of the invention,

FIG. 2A) is an electrical circuit diagram of a prior art isolated class E resonant DC-DC converter comprising a series resonant circuit,

FIG. 2B) is an electrical circuit diagram of a class E resonant step-up DC-DC power converter comprising a series resonant circuit in accordance with a sixth embodiment of the invention,

FIG. 3A) is an electrical circuit diagram of a prior art flyback DC-DC converter,

FIG. 3B) is an electrical circuit diagram of a flyback step-up DC-DC power converter in accordance with a 7^{th} embodiment of the invention,

FIG. 4A) is an electrical circuit diagram of a prior art isolated SEPIC converter,

FIG. 4B) is an electrical circuit diagram of a step-up SEPIC DC-DC converter in accordance with an 8^{th} embodiment of the invention,

FIG. 5A) is an electrical circuit diagram of a prior art isolated class DE resonant DC-DC converter comprising a series resonant circuit; and

FIG. 5B) is an electrical circuit diagram of a class DE resonant step-up DC-DC power converter in accordance with a 9^{th} embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIGS. 1A) and 1B) are simplified electrical circuit diagrams 100b illustrating basic operational principles of step-up DC-DC power converters in accordance with a first embodiment of the present invention. Two different variants of a generic converter circuit topology are illustrated on FIGS. 1A, 1B) and FIG. 1C), respectively. FIG. 1A) shows a step-up DC-DC power converter 100b comprising a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 107b. The primary side circuit comprises a positive input terminal 102b and a negative input terminal 101b for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 102b and a negative input terminal 101b to form an energy reservoir for the voltage source. The primary side circuit additionally comprises an input side 106b of a switched energy storage network arranged in front of the isolation barrier 107. The secondary side circuit comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at output terminal 104b. A second electrode of the output capacitor C_{out}, situated at a lower voltage potential than the first electrode, is connected to the positive input terminal 102b on the input side circuit via an electrical short-circuit connection or wire 109b extending across the isolation barrier 107b. The electrical short-circuit connection or wire 109b effectively places the output capacitor C_{out} and input capacitor C_{in} is series or cascade between the output voltage V_{out} at output terminal 104b and the negative input terminal 101b. An electrical load R_{load} of the step-up DC-DC converter 100b is coupled between the output terminal 104b and the negative input terminal 101b such that in effect the output and input capacitors C_{out}, C_{in} are coupled series to supply power or current to the electrical load. The primary side circuit comprises the previously discussed input side 106b of the switched energy storage network of the step-up DC-DC converter 100b and the secondary side circuit comprises an output side 108b of the switched energy storage network. The skilled person will appreciate that the switched energy storage network may include numerous circuit topologies depending on the particular type of DC-DC converter in question. The switched energy storage network preferably comprises at least one inductor for energy storage and release, but may alternatively exclusively comprise capacitors for energy storage. Generally, the switched energy storage network is configured for alternatingly being charged from the input voltage V_{in} and discharged to the output capacitor C_{out}

through the isolation barrier 107b in accordance with a switch control signal to produce the converter output voltage $V_{out.}$. The primary side circuit preferably comprises at least one semiconductor switch, for example a MOSFET, which is switched between on-states and off-states by the switch control signal such that the input voltage is modulated in accordance with a switch control signal. The frequency of the switch control signal of the switched energy storage network may be at or above 30 MHz to form a so-called VHF type of DC-DC power converter. The switch control signal may comprise a PWM modulated control signal. The primary side circuit may comprise an inductor that is charged with energy during an on-state of the least one semiconductor switch from the input capacitor C_{in} and/or the DC or AC input voltage V_{in}. The inductor of the primary side circuit may subsequently be discharged through the output side 108b of the switched energy storage network and the output capacitor C_{out} in an off-state of the least one semiconductor switch. The secondary side circuit may comprise a diode based rectifier or a synchronous rectifier in front of the output capacitor to produce the converter output voltage $V_{out.}$as a DC output voltage.

While the electrical short-circuit connection or wire 109b eliminates the galvanic isolation between the input and output side circuits of the step-up DC-DC converter 100b by interconnecting the second electrode of the output capacitor C_{out} and the negative input terminal 101b, it provides numerous new benefits to the DC-DC converter as a whole as illustrated with reference to FIG 1B). The series connection of the output and input capacitors C_{out}, C_{in} means that the secondary side circuit only needs to supply the converter output voltage minus the input voltage (i.e. V_{out} minus V_{in}) to the electrical load R_{load} instead of the entire output voltage which is the situation in prior art isolated DC-DC converter topologies. Since, the switched energy storage network, including the input and output sides 106b, 108b, only supplies a fraction of the converter output voltage V_{out} it also supplies a corresponding fraction of the total power only to the electrical load R_{load}. The reduced voltage across the output section 108b reduces the required maximum voltage rating of active and passive components therein leading to physically smaller and/or less costly active and passive components for example inductors, capacitors (including C_{out}), transistors and diodes etc. In addition, the life span of the latter components may increase by the smaller voltage stress. In the input section 106b, the smaller amount of power to be transferred through the DC-DC converter 100b for supplying a given converter

output power to the electrical load, leads to reduced power requirements for active semiconductors switches allowing less costly and physically smaller semiconductors to be applied.

These beneficial reductions of the amount of power to be transferred through the switched energy storage network 106b, 107b, 108b are achieved because the residual fraction of the output power supplied to the electrical load is transferred directly from the input voltage source V_{in} and input capacitor C_{in} to the output capacitor C_{out}. This power transfer mechanism is illustrated by the first output current path $I_{convert}$ which shows how secondary side current charges the output capacitor C_{out} when the current is drawn by the load and thereby delivers power that has passed through the switched energy storage network in a conventional manner. However, the present DC-DC converter also comprises a second output current path I_{direct} which illustrates how the output capacitor C_{out} is charged directly from the input voltage source V_{in} and input capacitor C_{in} when the current is drawn by the load without passing through input and output sides 106b, 108b and isolation barrier 107b of the switched energy storage network. The skilled person will appreciate that a practical electrical short circuit connection 109b will possess a certain DC resistance and an upper limit for this DC resistance will vary depending on input/output voltage and/or current requirements of the converter 100b. The electrical short-circuit connection may possess a DC resistance of less than 1 kΩ, even more preferably less than 100 Ω, such as less than 10 Ω. In other embodiments, the electrical short circuit connection 109b may have a unidirectional resistance such that the DC resistance only falls below the above-mentioned upper limits in one direction and exhibits a much larger DC resistance in the opposite direction, i.e. a diode characteristic.

FIG. 1C) is a simplified electrical circuit diagram 100c illustrating basic operational principles of step-up DC-DC power converters in accordance with a second embodiment of the present invention. The step-up DC-DC power converter 100c may be viewed as an alternative variant of the step-up DC-DC converter topology 100b in accordance with the first embodiment of the invention where the electrical short-circuit connection or wire 109c extending across the isolation barrier 107c is connecting the second positive electrode of the output capacitor C_{out} to the negative input terminal 102c of the primary side circuit. Thereby, a series coupling of the out-

put capacitor C_{out} and the input capacitor C_{in} from the converter output voltage V_{out} at the positive input terminal 104c to the negative electrode 101c of the output capacitor C_{out} is established. The negative electrode 101c of the output capacitor C_{out} is at a lower electric potential than the negative input terminal 102c. In this manner, the input voltage V_{in} is stacked on top of the voltage across the first and second electrodes of the output capacitor C_{out}. Otherwise, circuit functions, electrical component characteristics and component values of the second embodiment of the step-up DC-DC power converter 100c may be identical to those discussed above in connection with the first embodiment of the step-up DC-DC power converter 100b.

FIG. 1D) shows a step-up DC-DC power converter 100d in accordance with third embodiment of the invention. The converter core 105 of the step-up DC-DC power converter 100d may be identical to the core 105 of the step-up DC-DC power converter 100b discussed above in connection with FIGS. 1A) and 1B). Hence, corresponding features of these different step-up DC-DC power converter embodiments 100b, 100d have been provided with corresponding reference symbols to assist comparison. The third embodiment of the step-up DC-DC power converter 100d comprises a mode selecting controllable semiconductor switch SW1 inserted in a short-circuit connection or wire 109d. This short-circuit connection 109d effectively places the output capacitor C_{out} and input capacitor C_{in} is series between the output voltage V_{out} at output terminal 104d and the negative input terminal 101d as discussed above.

The mode selecting controllable semiconductor switch SW1 is configured to switch the step-up DC-DC power converter 110d between two distinct modes of operation as discussed below. The controllable semiconductor switch SW1 may comprise one or more BJT(s), FET(s) MOSFET(s) or IGBT(s) such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) transistor. SW1 may be switched between conducting/ON state and non-conducting/OFF state by a suitable control voltage applied on a gate or base terminal of the switch SW1. A mode controlling circuit of, or associated with, the step-up DC-DC power converter 100d may supply this control voltage to SW1.

SW1 is configured to break/disconnect or close/connect the short-circuit connection 109d depending on a state of SW1. The short-circuit connection 109d is established

in a conducting/ON state of SW1 and the short-circuit connection 109d is broken/disconnected in a non-conducting/OFF state of SW1. In the conducting state of SW1, the primary side circuit and the secondary side circuit of the converter core 105 are connected by the short-circuit connection 109d. The step-up DC-DC power converter 100d additionally comprises a diode 111d connected between the negative input terminal 101d and a negative electrode 115d of the output capacitor C_{out}. This diode 111d is reverse biased and hence non-conducting when SW1 is conducting/ON because the negative output electrode 115d is at a higher potential than the negative input terminal 101d. Consequently, when SW1 is ON or conducting the step-up DC-DC power converter 100d operates in a first distinct mode where the functionality of the power converter 100d is similar to the functionality of the previously discussed step-up DC-DC power converter 100b with the accompanying advantages.

A second distinct mode of the step-up DC-DC power converter 100d is reached or provided in the non-conducting/OFF state of SW1 where the short-circuit connection 109d is broken or opened. In this second distinct mode, the diode 111d will be forward biased and conducting such that the primary side circuit and the secondary side circuit are electrically connected both through galvanic isolation barrier 107d and through the diode 111d. Hence, the conducting diode 111d bypasses the galvanic isolation barrier 107d in the second mode of the step-up DC-DC power converter 100d. However, the overall functionality of the step-up DC-DC power converter 100d in the second mode of operation remains similar to the functionality of a corresponding ordinary (i.e. lacking the first mode of operation) step-up DC-DC power converter.

The mode switching feature of the present step-up DC-DC power converter 100d is accompanied with several advantages. The mode switching feature increases the dynamic voltage operating range of the power converter 100d. To illustrate these advantages consider an ordinary DC-DC power converter designed for a DC input voltage of 10 V and a DC output voltage range from 5 – 15 V. If this ordinary DC-DC power converter is converted or configured as the present step-up DC-DC power converter 100d, the DC output voltage range may be increased to 5 - 25 V by switching the re-configured power converter between the first and second modes of operation. This increase of DC output voltage range provided by the mode switching

feature of the present step-up DC-DC power converter 100d is particular advantageous for resonant power converters which generally suffer from a restricted or narrow DC output voltage range compared to non-resonant DC-DC power converters. However, exploiting the mode switching feature of the present step-up DC-DC power converter 100d requires that the intended application does not require galvanic isolation between the primary and secondary side circuits due to the electrical path through the diode 111d.

FIG. 1E) is simplified electrical circuit diagram of a first converter core 105e that may be utilized as converter core 105 in each of the step-up DC-DC power converter embodiments 100b, 100c, 100d, illustrated on FIGS. 1A), 1B), 1C) and 1D), respectively. The first converter core 105e comprises a plurality of separate resonant DC-DC power converter cores 110e. Each of the separate resonant DC-DC power converter cores 110e comprises an input side 111 of a switched energy storage network coupled to an output side 113 of the switched energy storage network through a galvanic isolation barrier 107e. The input sides 111 of the resonant DC-DC power converter cores 110e may be connected in parallel or series. The output sides 113 of the resonant DC-DC power converter cores 110e may likewise be connected in parallel or series. The parallelization of the plurality of input sides 111 and/or the parallelization of the one or more output sides 113 increases the power rating of a step-up DC-DC power converter utilizing the first converter core 105e. The skilled person will understand that each of the separate resonant DC-DC power converter cores 110e may comprise one of the prior art resonant DC-DC power converter cores discussed below with reference to FIGS. 2, 3, 4, 5 and 6.

FIG. 1F) is simplified electrical circuit diagram of a second converter core 105f of each of the step-up DC-DC power converter embodiments 100b, 100c, 100d, illustrated on FIGS. 1A), 1B), 1C) and 1D), respectively. The second converter core 105f comprises a plurality of separate resonant power inverters 114e. Each of the separate resonant power inverter cores 114e comprises an input side 115 of a switched energy storage network coupled to one or more rectifier(s) 117 of the resonant DC-DC power converter core 105f through a galvanic isolation barrier 107f. The separate resonant power inverter cores 114e may be connected in parallel or series. Likewise, the respective output side of the one or more rectifier(s) 117 may also be

connected in series or parallel. However, galvanic isolation may be inserted between the one or more rectifier(s) 117 if these are coupled in series.

FIG. 2A) shows an electrical circuit diagram of a prior art isolated class E resonant DC-DC converter 200 comprising a series resonant circuit including inductor L_2 and capacitor C_1. The prior art class E resonant converter comprises a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 207. The primary side circuit comprises a positive input terminal 202 and a negative input terminal 201 for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 202b and a negative input terminal 201 to form an energy reservoir for the voltage source. The primary side circuit additionally comprises a switched energy storage network which includes first and second series connected inductors L_1 and L_2 and a MOSFET switch S with a drain terminal connected to a midpoint node between the L_1 and L_2. The primary side circuit is arranged in front of an isolation barrier 207 formed by coupling capacitors C_1 and C_2. The secondary side circuit comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at output terminal 204. A second negative electrode of the output capacitor C_{out} is coupled to a negative terminal 203 of the converter output voltage. A load of the isolated class E resonant DC-DC converter 200 is schematically illustrated by load resistor R_L and coupled between the positive and negative output terminals 204, 203.

FIG. 2B) is an electrical circuit diagram of a class E resonant step-up DC-DC power converter 200b comprising a series resonant circuit in accordance with a sixth embodiment of the invention. The class E resonant step-up DC-DC power converter 200b may be obtained by conversion of the above-mentioned prior art isolated class E resonant DC-DC converter 200 by inserting or adding an electrical short circuit connection 209b extending across a galvanic isolation barrier 207b of the converter 200b in accordance with the principles discussed above in connection with the first embodiment of the invention discussed above in connection with FIGS. 1A) and 1B). The galvanic isolation barrier 207b comprises series capacitors C_1 and C_2.The electrical short circuit connection 209b connects the positive input terminal 202b and the second negative electrode 203b of the output capacitor C_{out}. As discussed in con-

nection with FIGS. 1A) and 1B), the electrical short-circuit connection or wire 209b effectively places the output capacitor C_{out} and input capacitor C_{in} is series or cascade between the output voltage V_{out} and the negative input terminal 201b. Hence, the electrical or power converter load, schematically illustrated by the load resistor R_L, is coupled between the converter output voltage at the output terminal 204b and the negative input terminal 201b. The skilled person will understand that the series capacitor C_2 of the galvanic isolation barrier 207b prevents DC current from flowing from the second negative electrode 203b of the output capacitor C_{out} and back to the negative input terminal 201b electrode of the input voltage source. In this manner, the DC current is directed or forced through the electrical short circuit connection 209b and back through the input capacitor C_{in}. In this manner, despite being electrically by-passed by the conversion, the isolation barrier 207 is important for the operation of the present class E resonant step-up DC-DC power converter 200b as node 201b, 203b and 202b would be directly electrically connected causing a short circuit at the converter input.

The class E resonant step-up DC-DC power converter 200b may comprise a capacitor (not shown) arranged across drain and source terminals of the MOSFET switch S to increase a resonant current and/or adjust/fine-tune a resonance frequency of the power converter 200b. Likewise, a yet further capacitor (not shown) may be arranged across the rectifying diode D to adjust a duty cycle of the secondary part of the power converter 200b, i.e. the class E rectifier.

FIG. 3A) is an electrical circuit diagram of a prior art flyback DC-DC converter 300. The prior art DC-DC converter 300 comprises a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 307. The primary side circuit comprises a positive input terminal 302 and a negative input terminal 301 for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 302 and a negative input terminal 301 to form an energy reservoir for the input voltage source. The primary side circuit additionally comprises a switched energy storage network which comprises a first inductor L_P having a first end coupled to the positive input terminal 302 and a second end to a drain terminal of a MOSFET switch S. A source terminal of the MOSFET switch S is coupled to the negative input

terminal 301. The first inductor L_P is a primary transformer winding of a transformer which provides a galvanic isolation barrier 307 of this prior art DC-DC converter 300. A secondary side circuit of the power converter 300 comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at output terminal 304. A second negative electrode of the output capacitor C_{out} is coupled to a negative terminal 303 of the converter output voltage. An electrical or power converter load is schematically illustrated by load resistor R_L and coupled between the positive and negative output terminals 304, 303 of the prior art DC-DC converter 300. The secondary side circuit furthermore comprises a second inductor L_S which is a secondary transformer winding of the above-mentioned transformer. The secondary transformer winding L_S has a first end coupled to a rectifying diode D and a second end coupled to the negative electrode of the output capacitor C_{out}. The rectifying diode D rectifies AC current generated by the secondary transformer winding L_S and generates a DC voltage as the converter output voltage between the positive and negative output terminals 304, 303. An electrical or power converter load is schematically illustrated by load resistor R_L coupled between the positive and negative output terminals 304, 303.

FIG. 3B) is an electrical circuit diagram of a flyback step-up DC-DC power converter 300b in accordance with a 7th embodiment of the invention. The flyback power converter 300b may be obtained by conversion of the above-mentioned prior art isolated flyback DC-DC converter 300 by inserting or adding an electrical short circuit connection 309b extending across a galvanic isolation barrier formed by the transformer comprising the magnetically coupled primary and secondary transformer windings L_P and L_S. The electrical short circuit connection 309b connects the positive input terminal 302b and the second negative electrode 303b of the output capacitor C_{out}. As discussed in connection with FIGS. 1A) and 1B), the electrical short-circuit connection or wire 309b effectively places the output capacitor C_{out} and input capacitor C_{in} is series or cascade between the output voltage V_{out} and the negative input terminal 301b. Hence, the electrical or power converter load, schematically illustrated by the load resistor R_L, is coupled between the converter output voltage at the output terminal 304b and the negative input terminal 301b. The skilled person will understand that the transformer coupling prevents DC current from flowing from the second negative electrode 303b of the output capacitor C_{out} and back to the

negative input terminal 301b electrode of the input voltage source. In this manner, the DC current is directed or forced through the electrical short circuit connection 309b and back through the input capacitor C_{in}.

FIG. 4A) is an electrical circuit diagram of a prior art isolated single-ended primary-inductor converter (SEPIC) 400. The prior art SEPIC 400 comprises a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 407. The primary side circuit comprises a positive input terminal 402 and a negative input terminal 401 for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 402 and a negative input terminal 401 to form an energy reservoir for the input voltage source. The primary side circuit additionally comprises a switched energy storage network which includes a first inductor L_1 having first node coupled to the DC or AC input voltage V_{in} and a second node coupled to a drain terminal of a MOSFET switch S. A source terminal of the MOSFET switch S is coupled to the negative input terminal 401. The primary side circuit is arranged in front of an isolation barrier 407 formed by coupling capacitors C_1 and C_2. The secondary side circuit comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at output terminal 404. A second negative electrode of the output capacitor C_{out} is coupled to a negative terminal 403 of the converter output voltage. A rectifying diode D rectifies AC current generated by a second inductor L_2 and generates a DC voltage as the converter output voltage V_{out} between the positive and negative output terminals 404, 403. A load of the SEPIC 400b, illustrated by load resistor $R_{L,}$ is coupled between the positive and negative output terminals 404, 403.

FIG. 4B) is an electrical circuit diagram of a SEPIC 400b in accordance with an 8th embodiment of the invention. The SEPIC 400b may be obtained by conversion of the above-mentioned prior art SEPIC 400 by inserting or adding an electrical short circuit connection 409b extending across a galvanic isolation barrier 407b of the SEPIC 400b. The galvanic isolation barrier 407b comprises series capacitors C_1 and C_2.The electrical short circuit connection 409b connects the positive input terminal 402b and the second negative electrode 403b of the output capacitor C_{out}. As discussed in connection with FIGS. 1A) and 1B), the electrical short-circuit connection

or wire 409b effectively places the output capacitor C_{out} and input capacitor C_{in} is series or cascade between the output voltage V_{out} and the negative input terminal 401b. Hence, the electrical or power converter load, schematically illustrated by the load resistor R_L, is coupled between the converter output voltage at the output terminal 404b and the negative input terminal 401b. The skilled person will understand that the series capacitor C_2 of the galvanic isolation barrier 407b prevents DC current from flowing from the second negative electrode 403b of the output capacitor C_{out} and back to the negative input terminal 401b electrode of the input voltage source as discussed previously.

The SEPIC 400b may comprise a capacitor (not shown) connected or arranged across drain and source terminals of the MOSFET switch S to increase a resonant current and/or adjust/fine-tune a resonance frequency of the SEPIC 400b. Likewise, a yet further capacitor (not shown) may be arranged across the rectifying diode D to adjust a duty cycle of the power converter 400b.

FIG. 5A) shows an electrical circuit diagram of a prior art isolated class DE resonant DC-DC converter 500 comprising a series resonant circuit including L_0 and C_0. The prior art class DE converter 500 comprises a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 507. The primary side circuit comprises a positive input terminal 502 and a negative input terminal 501 for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 502 and a negative input terminal 501 to form an energy reservoir for the input voltage source. The primary side circuit additionally comprises a switched energy storage network comprising a half-bridge circuit comprising cascaded MOSFET switches S_1 and S_2 arranged across the positive and negative input terminals 502, 501, respectively. An output 506 of the half-bridge circuit is coupled to a first inductor L_0 of the series resonant circuit and the latter is coupled in series with the capacitor C_0. This primary side circuit is arranged in front of the isolation barrier 507 formed by the coupling capacitor C_0 of the series resonant circuit and a second capacitor C_B inserted between the negative input terminal 501 and a negative output voltage terminal 503 to provide DC isolation between these in this prior art class DE converter 500. The secondary side circuit comprises an output capacitor C_{out} having a first

electrode electrically connected to the converter output voltage V_{out} at output terminal 504. A second negative electrode of the output capacitor C_{out} is coupled to the negative terminal 503 of the converter output voltage. A pair of rectifying diodes D_1 and D_2 rectifies AC current generated by excitation of the series resonant circuit and generates a DC voltage as the converter output voltage V_{out} between the positive and negative output terminals 504, 503. A load of the class DE converter 500, illustrated by load resistor $R_{L,}$ is coupled between the positive and negative output terminals 504, 503.

FIG. 5B) is an electrical circuit diagram of a class DE resonant DC-DC converter 500b in accordance with a 9th embodiment of the invention. The class DE converter 500b may be obtained by conversion of the above-mentioned prior art isolated class DE resonant DC-DC converter 500 by inserting or adding an electrical short circuit connection 509b extending across a galvanic isolation barrier 507b of the class DE converter 500b. The galvanic isolation barrier 507b comprises series capacitors C_1 and C_2. The electrical short circuit connection 509b connects the positive input terminal 502b and a second negative electrode 503b of the output capacitor C_{out}. As discussed in connection with FIGS. 1A) and 1B), the electrical short-circuit connection or wire 509b effectively places the output capacitor C_{out} and input capacitor C_{in} is series or cascade between the output voltage V_{out} and the negative input terminal 501b. Hence, the electrical or power converter load, schematically illustrated by the load resistor R_L, is coupled between the converter output voltage at the output terminal 504b and the negative input terminal 501b. The skilled person will understand that the series capacitor C_2 of the galvanic isolation barrier 507b prevents DC current from flowing from the second negative electrode 503b of the output capacitor C_{out} and back to the negative input terminal 501b electrode of the input voltage source as discussed previously. The series capacitor C_1 serves two purposes both forming part of the isolation barrier 507b and forming part of the series resonant circuit also including inductor L.

The class DE converter 500b may comprise a pair of capacitors (not shown) connected or arranged across the drain and source terminals of each of the MOSFET switches S_1 and S_2 to increase a resonant current and/or adjust/fine-tune a resonance frequency of the DE converter 500b. Likewise, a yet further pair of capacitors

(not shown) may be arranged across the rectifying diodes D_1 and D_2 to adjust a duty cycle of the secondary part of the power converter 500b, i.e. the class DE rectifier.

CLAIMS

1. A step-up DC-DC power converter comprising:
a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier,
the primary side circuit comprising a positive and a negative input terminal for receipt of an input voltage and an input capacitor coupled between the positive and negative input terminals,
the secondary side circuit comprising an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode,
a switched energy storage network configured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce the converter output voltage,
an electrical short-circuit connection across the galvanic isolation barrier connecting, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connecting the second positive electrode of the output capacitor to the negative input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor,
a load connection, in the first case, between the first positive electrode of the output capacitor and the negative input terminal or, in the second case, between the second negative electrode of the output capacitor and the positive input terminal.

2. A step-up DC-DC power converter according to claim 1, wherein the galvanic isolation barrier comprises:
a pair of magnetically coupled inductors comprising a first inductor electrically connected to the primary side circuit and a second inductor electrically connected to the secondary side circuit.

3. A step-up DC-DC power converter according to claim 2, wherein the first and second inductors are wound around a common magnetic permeable structure to form an isolation transformer.

4. A step-up DC-DC power converter according to claim 1, wherein the galvanic isolation barrier comprises:
a first capacitor coupled in series with the positive input terminal of the primary side circuit and the first positive electrode of the output capacitor; and
a second capacitor coupled in series with the negative input terminal of the primary side circuit and the second negative electrode of the output capacitor;

5. A step-up DC-DC power converter according to claim 1, wherein the electrical short-circuit connection has a DC resistance of less than 1 kΩ, even more preferably less than 100 Ω, such as less than 10 Ω.

6. A step-up DC-DC power converter according to claim 4 or 5, wherein the switched energy storage network comprises:
first and second series connected inductors and connected in series with the positive input voltage terminal,
a semiconductor switch having a first switch node connected between a mid-point node between the first and second series connected inductors, a second switch node connected to the negative input terminal of the primary side circuit and a control terminal connected to the switch control terminal; and
a third inductor having a first end connected to a second end of the second inductor through the first capacitor of the galvanic isolation barrier and a second end connected to the converter output voltage at the positive electrode of the output capacitor,
a rectifier connected between the first end of the third inductor and the negative electrode of the output capacitor.

7. A step-up DC-DC power converter according to claim 3, wherein the first and second inductors are integrated in the switched energy storage network;
the first inductor being arranged with a first inductor end connected to the positive input voltage terminal and a second inductor end connected to a first node of a semiconductor switch,
a second node of the semiconductor switch being connected to the negative input terminal of the primary side circuit; and

the second inductor comprising a first inductor end connected to the first positive electrode of output capacitor and a second inductor end connected to the second negative electrode, respectively, of the output capacitor through a rectifier.

8. A step-up DC-DC power converter according to any of the preceding claims, wherein the switched energy storage network comprises at least one semiconductor switch such as a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET.

9. A step-up DC-DC power converter according to any of the preceding claims, wherein a frequency of the switch control signal of the switched energy storage network has a frequency at or above 10 MHz, more preferably at or above 30 MHz.

10. A step-up DC-DC power converter according to any of the preceding claims, comprising a resonant DC-DC power converter.

11. A step-up DC-DC power converter according to any of the preceding claims, wherein each of the input capacitor and the output capacitor has a capacitance smaller than 100 nF.

12. A step-up DC-DC power converter according to any of the preceding claims, further comprising:
a rectifying element, such as a diode, coupled between the positive input terminal and second negative electrode of the output capacitor; and
a mode selecting semiconductor switch configured to selectively break and close the electrical short-circuit connection such that:
in a first mode of the step-up DC-DC power converter, establishing the series connection of the output capacitor and the input capacitor; and
in a second mode of the step-up DC-DC power converter, break the series coupling of the output capacitor and the input capacitor.

13. A method of converting an isolated DC-DC power converter to a step-up DC-DC power converter with higher power conversion efficiency, said method comprising steps of:

providing a primary side circuit and a secondary side circuit of the isolated DC-DC power converter,

coupling an input capacitor between a positive input terminal and a negative input terminal of the primary side circuit,

coupling an output capacitor between a positive and a negative terminal of the secondary side circuit,

providing electrical coupling of the primary side circuit and the secondary side circuit through a galvanic isolation barrier,

providing a switched energy storage network configured for alternatingly being charged from an input voltage of the converter and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce a converter output voltage,

connecting, in a first case, an electrical short-circuit across the galvanic isolation barrier from the negative output terminal of the secondary side circuit to the positive input terminal of the primary side circuit or connecting, in a second case, the positive output terminal of the secondary side circuit to the negative input terminal of the primary side circuit thereby establishing in both the first case and the second case a series coupling of the output capacitor and the input capacitor,

coupling, in a first case, a power converter load between the positive terminal of the secondary side circuit and the negative input terminal or coupling, in the second case, the power converter load between the negative terminal of the secondary side circuit and the positive input terminal of the primary side circuit.

14. A method of converting an isolated DC-DC power converter to a step-up DC-DC power converter according to claim 13, wherein the isolated DC-DC power converter comprises a resonant DC-DC power converter.

15. A method of converting an isolated DC-DC power converter to a step-up DC-DC power converter according to claim 13 or 14, comprising further steps of:

connecting a rectifying element, such as a diode, between the positive input terminal and second negative electrode of the output capacitor; and

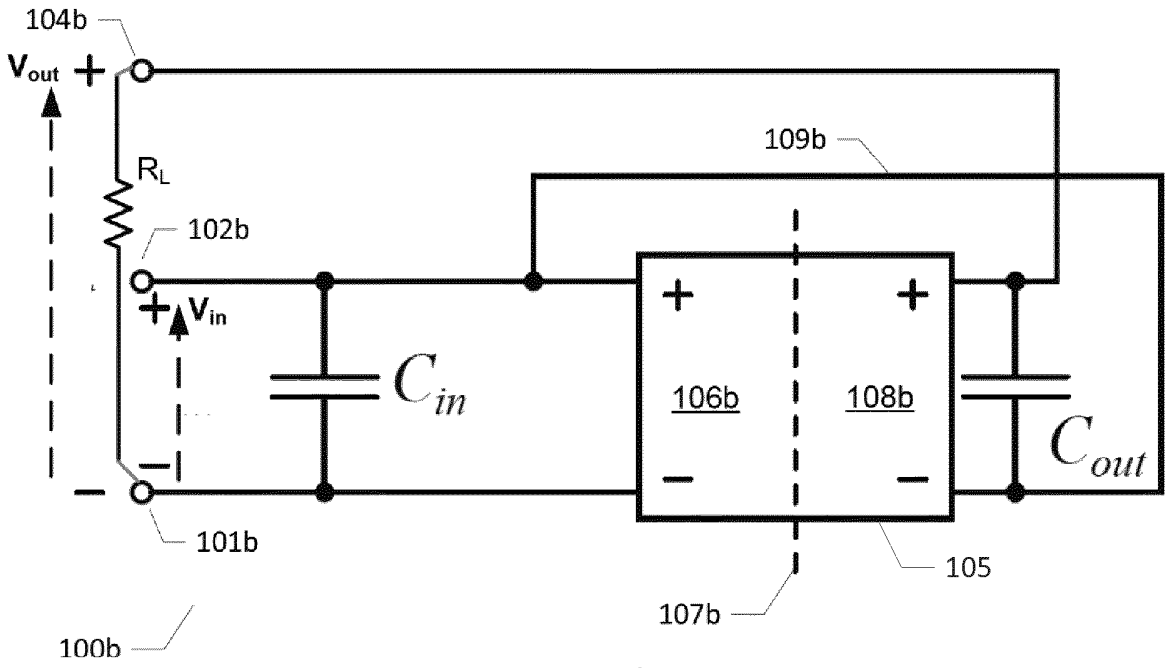
inserting a mode selecting semiconductor switch into the electrical short-circuit connection for selectively breaking and closing the short circuit connection such that:

establishing the series connection of the output capacitor and the input capacitor in

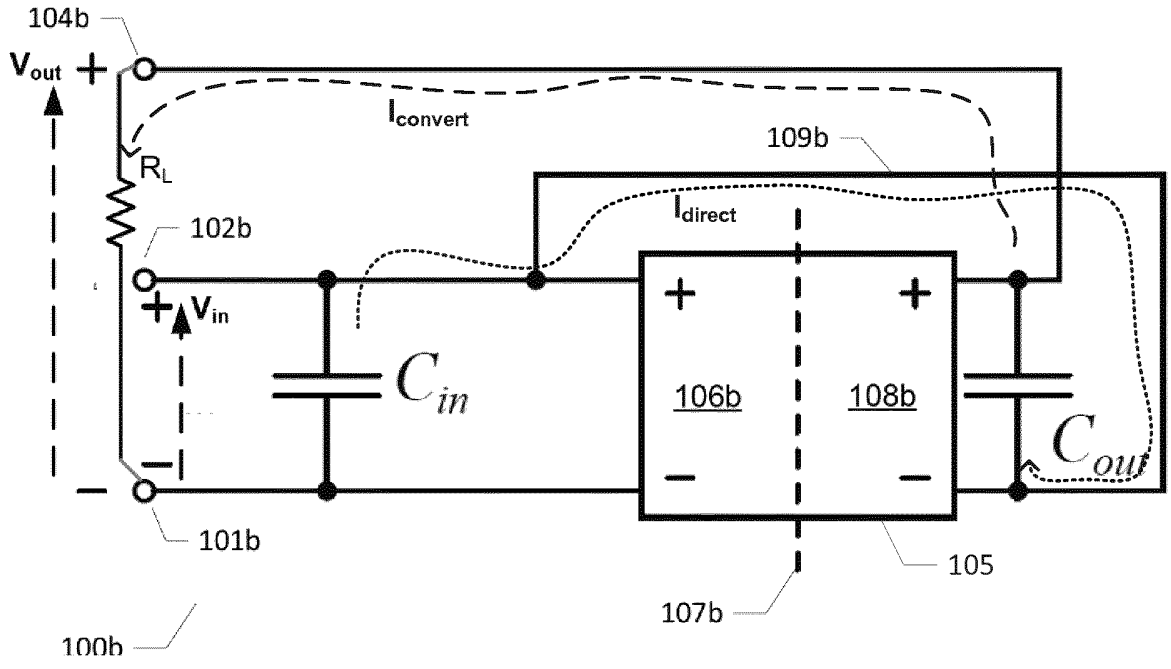
a first mode of the step-up DC-DC power converter; and

breaking or disconnecting the series coupling of the output capacitor and the input capacitor in a second mode of the step-up DC-DC power converter.

5


104b
V_{out}
R_L
102b
V_{in}
C_{in}
109b
106b
108b
C_{out}
101b
105
107b
100b

A)


104b
V_{out}
$I_{convert}$
R_L
109b
I_{direct}
102b
V_{in}
C_{in}
106b
108b
C_{out}
101b
105
107b
100b

B)

FIGS. 1A) – 1B)

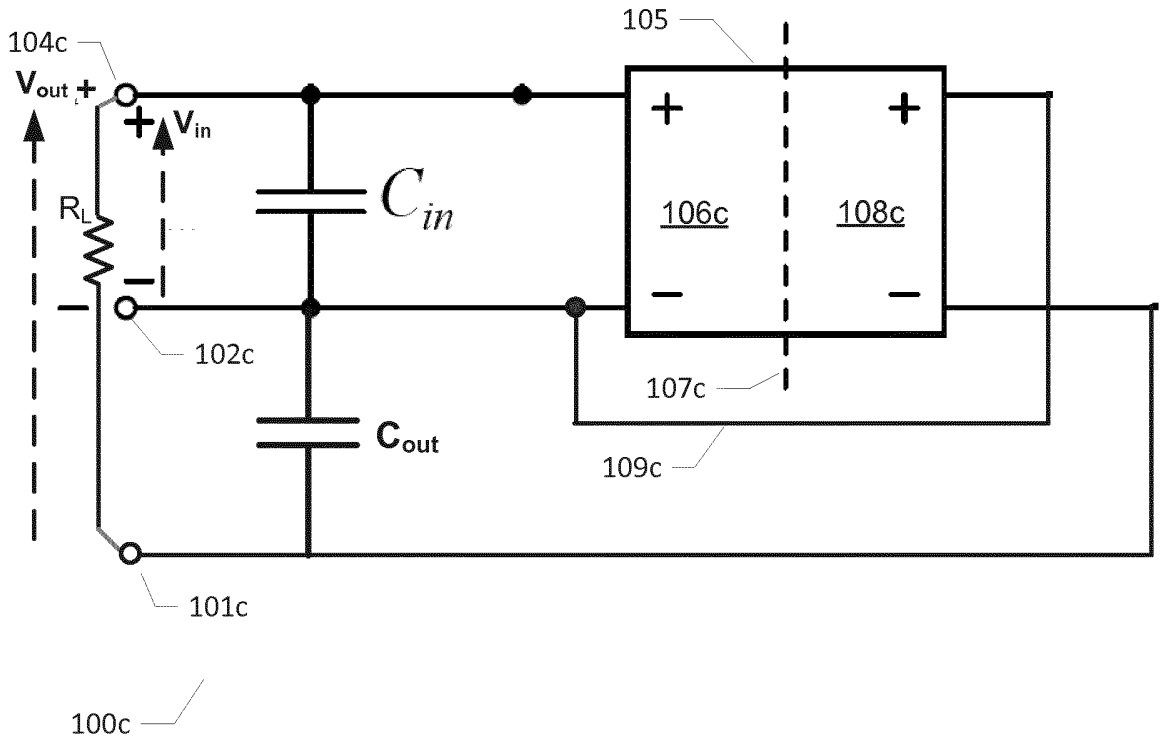
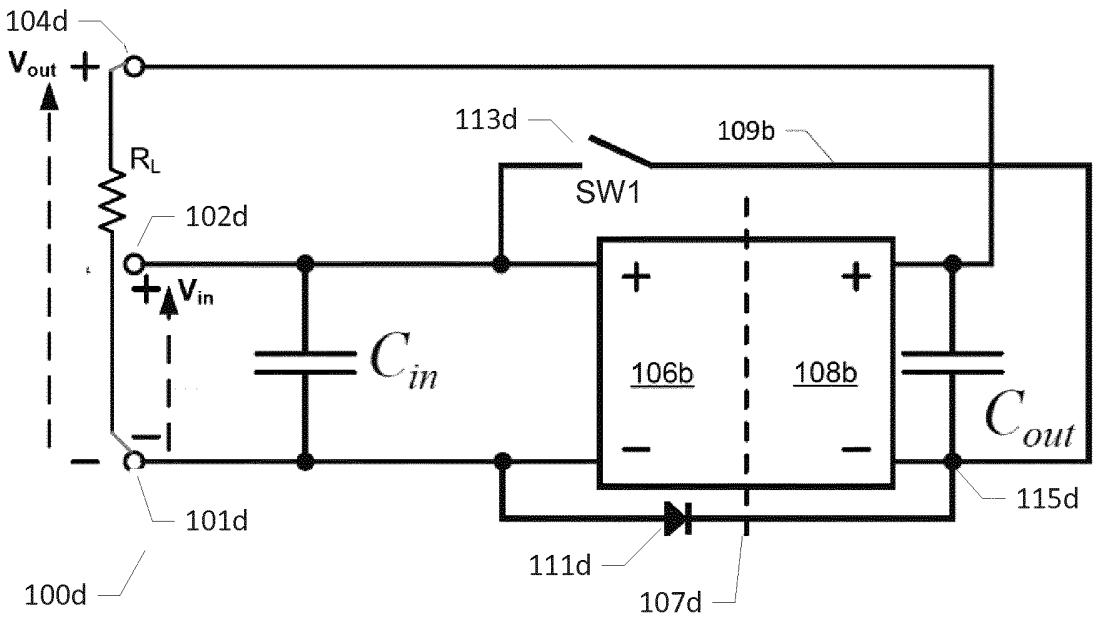

104c
Vout
+
Vin
RL
Cin
105
106c
108c
102c
107c
Cout
109c
101c
100c

FIG. 1C)


104d
V_{out}
+
R_L
102d
+
V_{in}
−
101d
100d
C_{in}
113d
SW1
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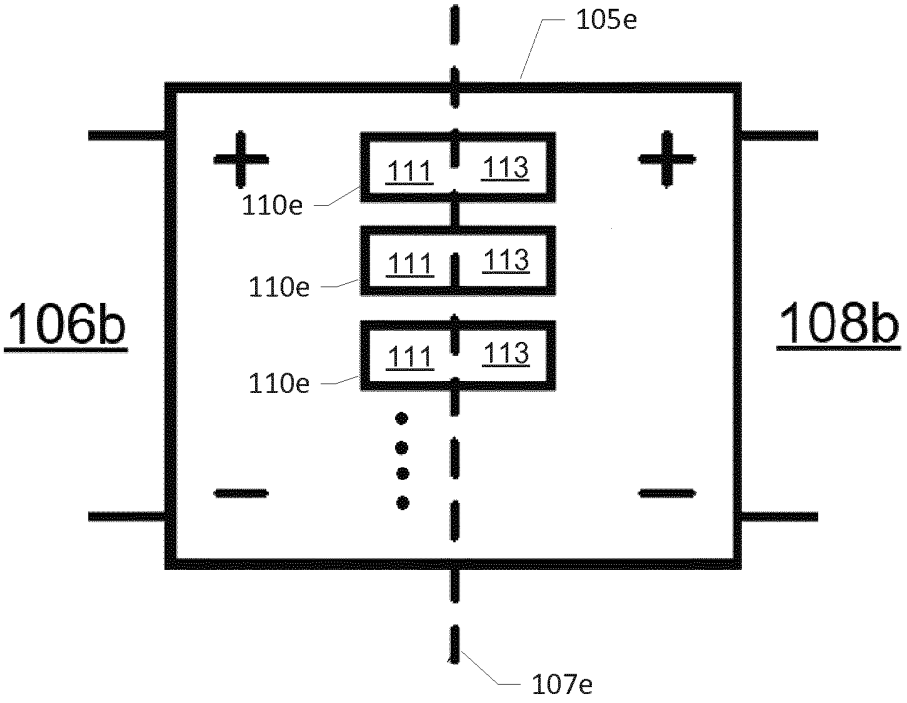
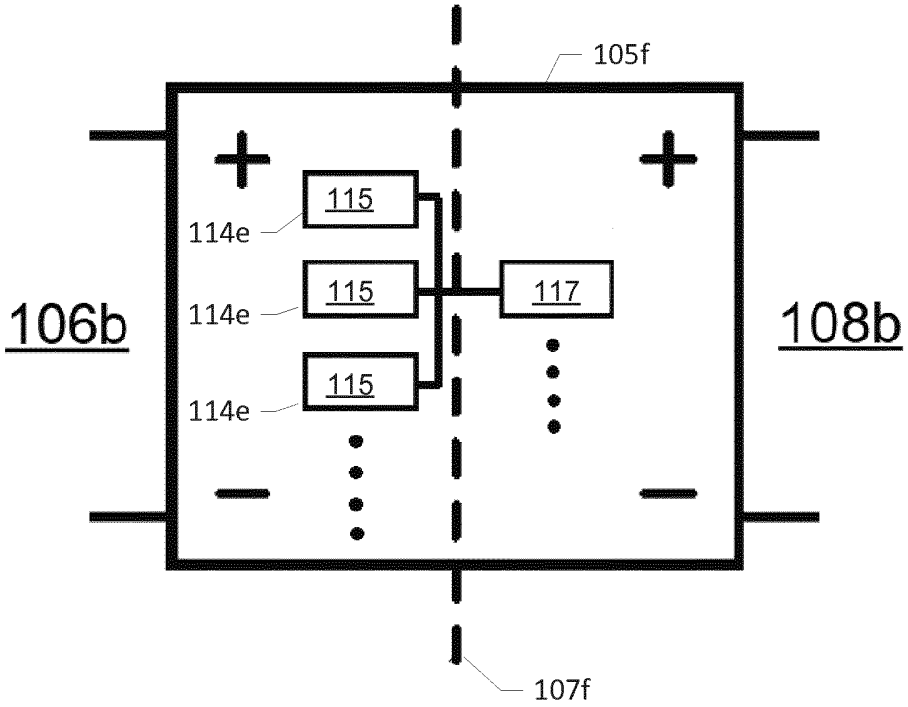
+
106b
−
+
108b
−
C_{out}
115d
111d
107d

FIG. 1D)

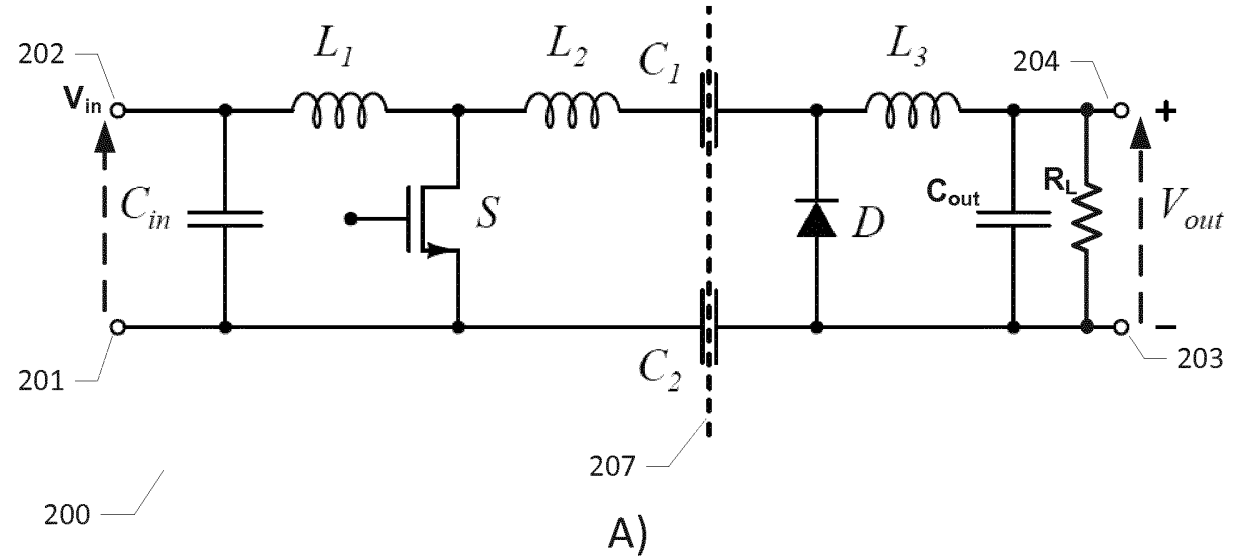

105e
111
113
110e
111
113
110e
111
113
110e
106b
108b
107e

E)

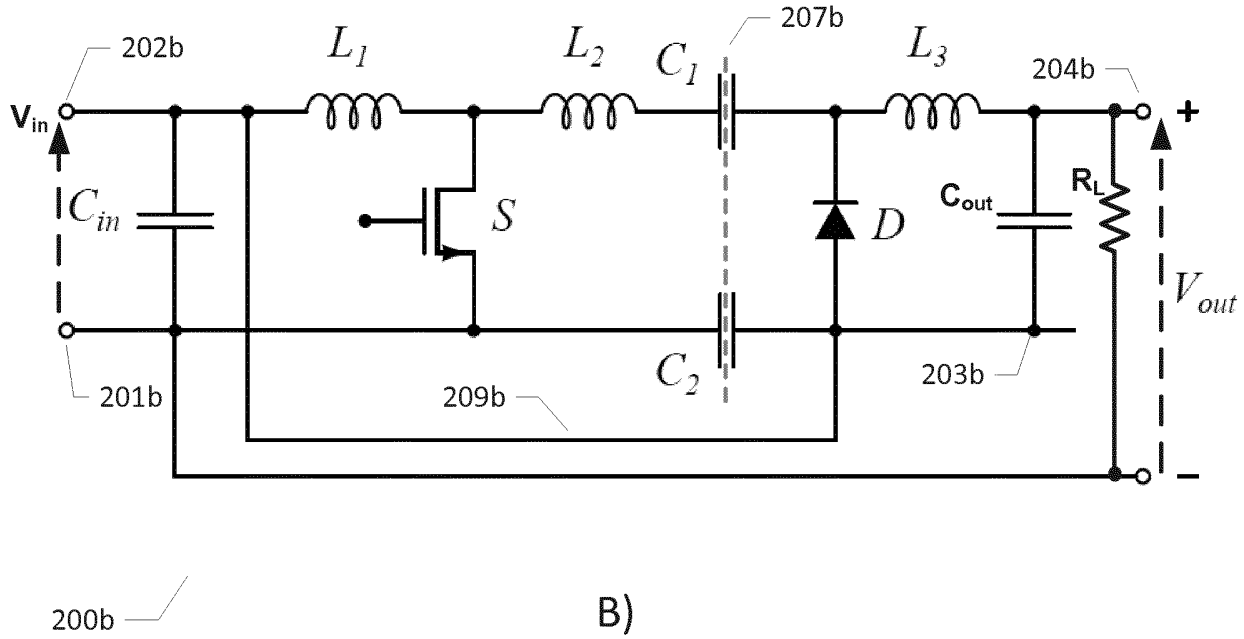

105f
115
114e
115
117
114e
115
114e
106b
108b
107f

F)

FIGS. 1E)-1F)


202
V_{in}
L_1
L_2
C_1
L_3
204
+
C_{in}
S
D
C_{out}
R_L
V_{out}
201
C_2
203
207
200

A)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+
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R_L
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C_2
201b
209b
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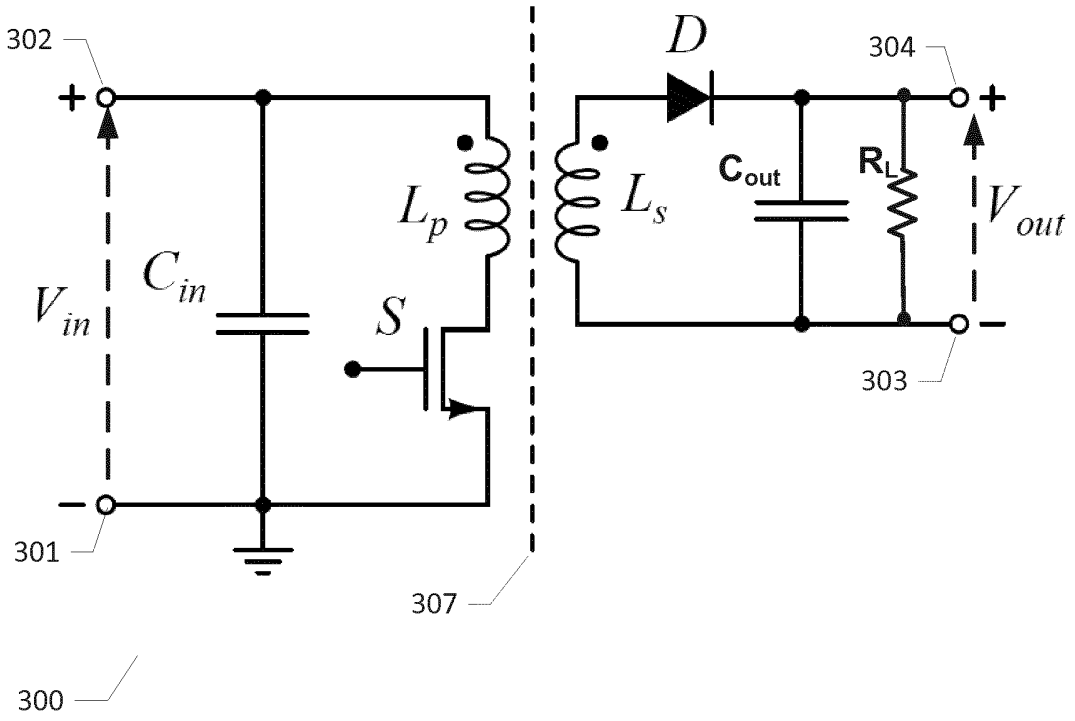
200b

B)

FIGS. 2A, B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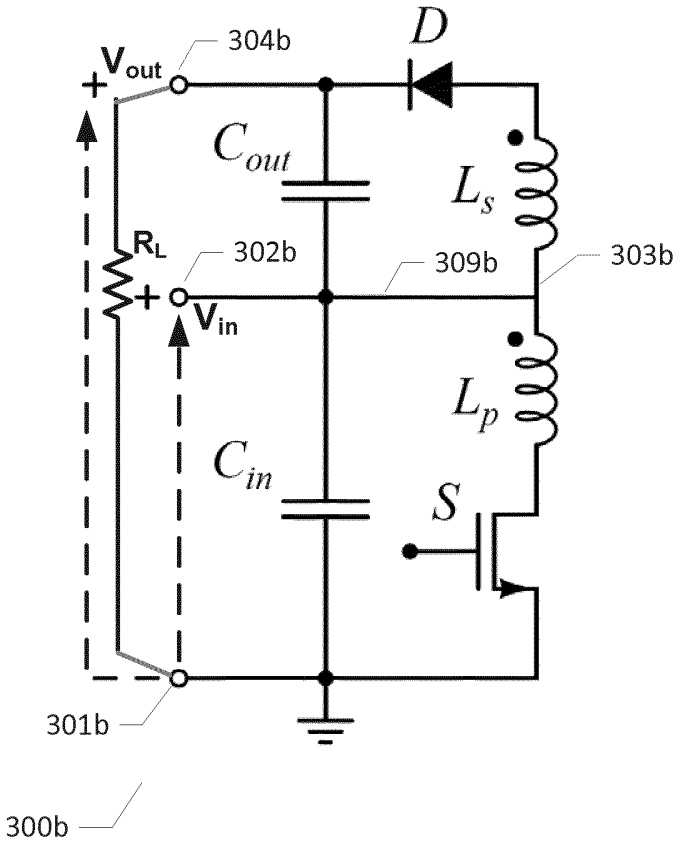
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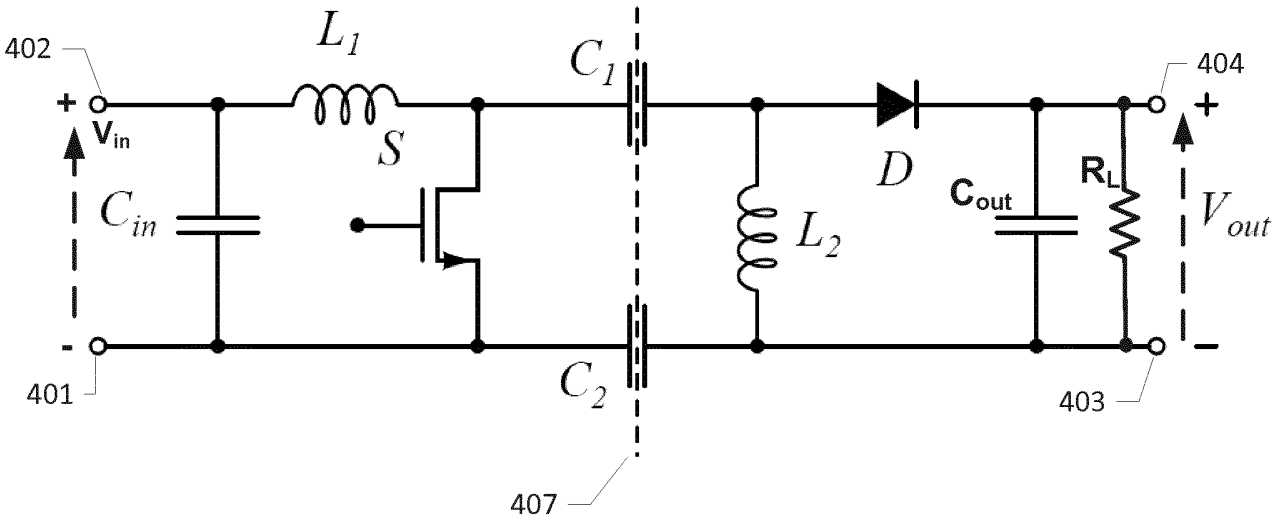
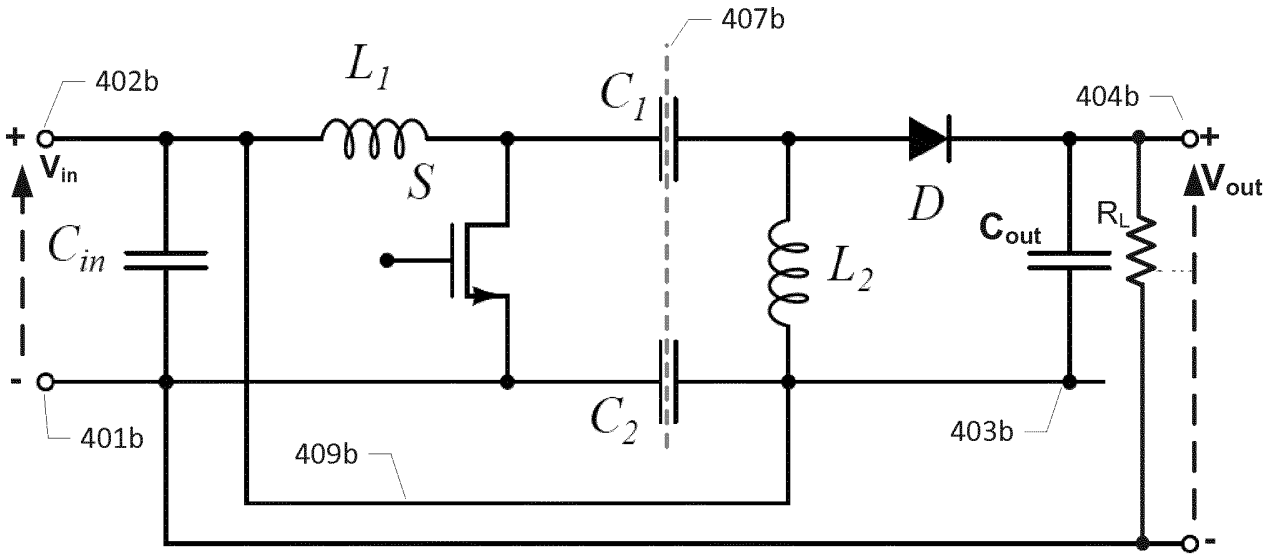
FIGS. 3A, B



A)

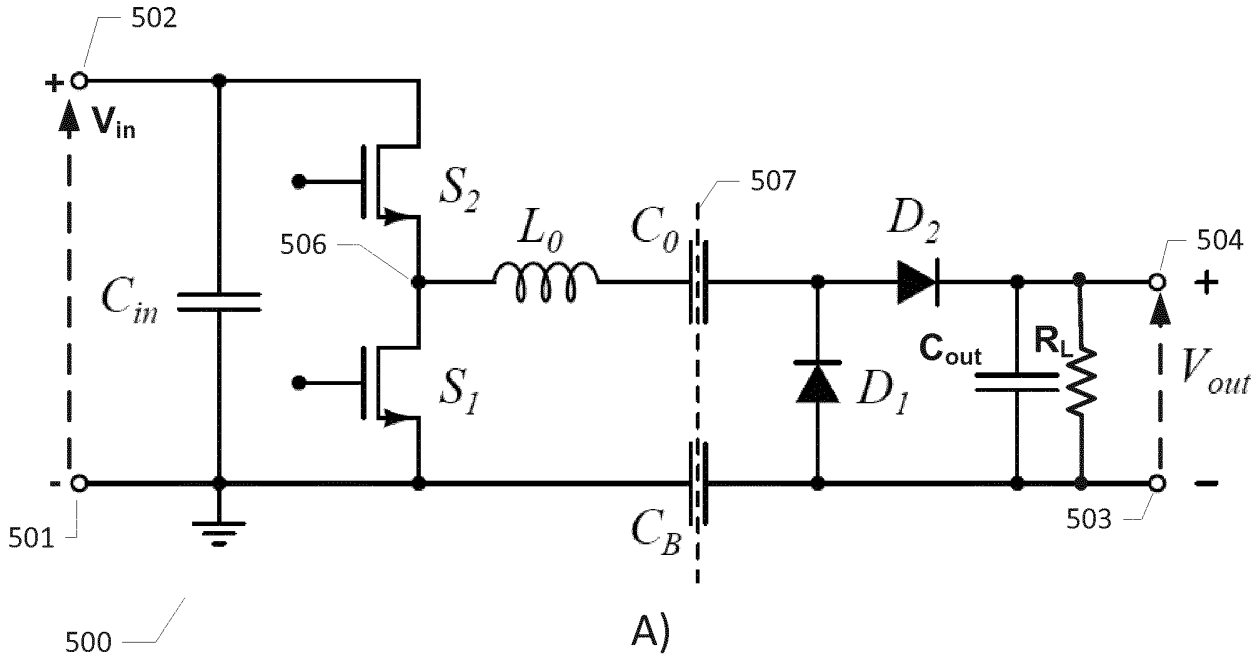
400



B)

400b

FIGS. 4A, B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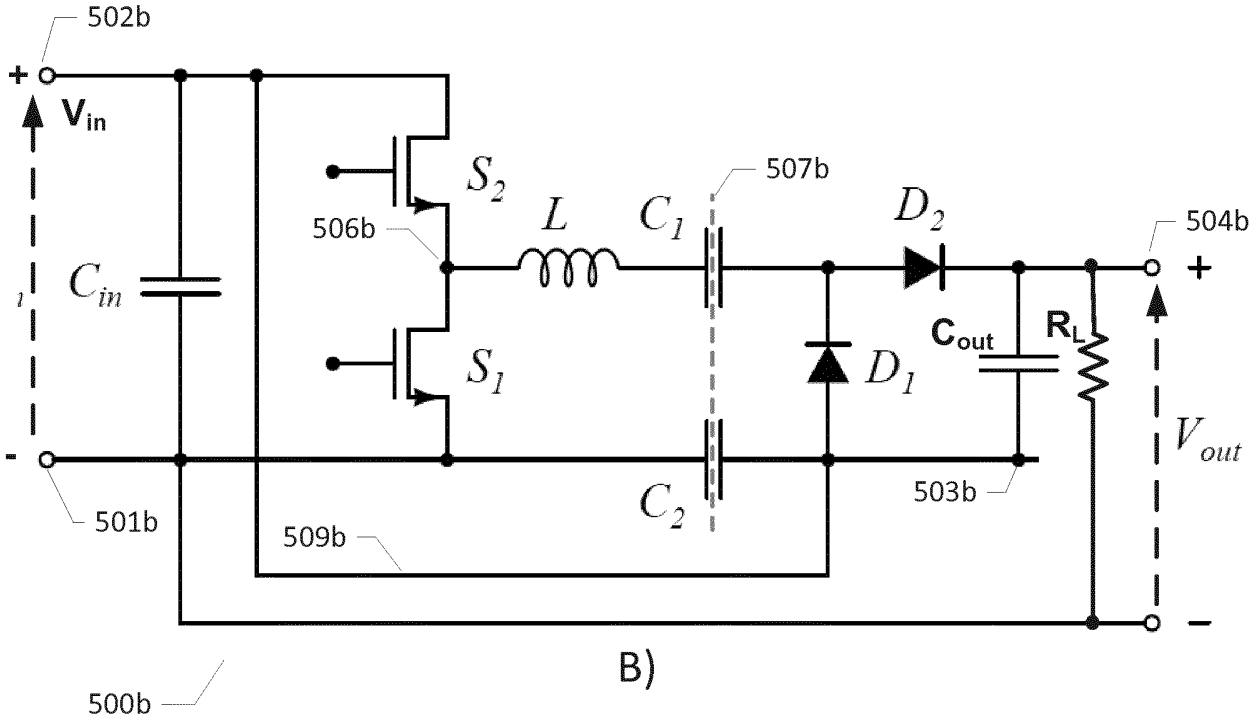
500

A)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R_L
V_{out}
-
501b
C_2
503b
509b
500b

B)

FIGS. 5A), B)

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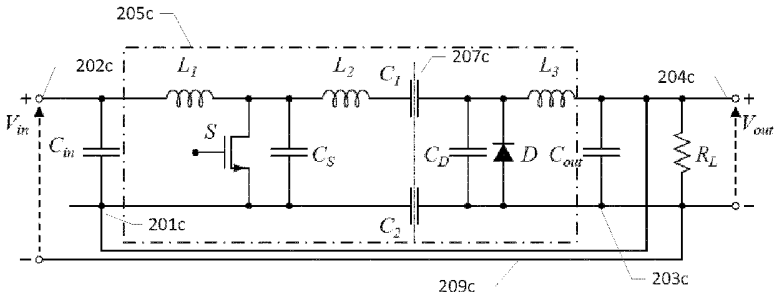

FIG .2B

(57) Abstract: The present invention relates to a resonant step-down DC-DC power converter which comprises a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier. The primary side circuit comprises a positive and a negative input terminal for receipt of an input voltage and an input capacitor coupled between the positive and negative input terminals and the secondary side circuit comprises an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode. A resonant network is con- figured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier by a semiconductor switch arrangement in accordance with a switch control signal to produce the converter output voltage. The resonant step-down DC-DC power converter comprises an electrical short-circuit connection across the galvanic isolation barrier connecting, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connecting the second positive electrode of the output capacitor to the negative input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor. A load connection is established, in the first case, between the first positive electrode of the output capacitor and the positive input terminal or, in the second case, between the second negative electrode of the output capacitor and the negative input terminal.

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RESONANT STEP-DOWN DC-DC POWER CONVERTERS

The present invention relates to a resonant step-down DC-DC power converter which comprises a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier. The primary side circuit comprises a positive and a negative input terminal for receipt of an input voltage and an input capacitor coupled between the positive and negative input terminals and the secondary side circuit comprises an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode. A resonant network is configured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier by a semiconductor switch arrangement in accordance with a switch control signal to produce the converter output voltage. The resonant step-down DC-DC power converter comprises an electrical short-circuit connection across the galvanic isolation barrier connecting, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connecting the second positive electrode of the output capacitor to the negative input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor. A load connection is established, in the first case, between the first positive electrode of the output capacitor and the positive input terminal or, in the second case, between the second negative electrode of the output capacitor and the negative input terminal.

BACKGROUND OF THE INVENTION

Power density and component costs are key performance metrics of both isolated and non-isolated DC-DC power converters to provide the smallest possible physical size and/or lowest costs for a given output power requirement or specification. Resonant power converters are particularly useful for high switching frequencies such as frequencies above 1 MHz where switching losses of standard SMPS topologies (Buck, Boost etc.) tend to be unacceptable for conversion efficiency reasons. High switching frequencies are generally desirable because of the resulting decrease of the electrical and physical size of circuit components of the power converter like inductors and capacitors. The smaller components allow increase of the power density of the DC-DC power converter. In a resonant power converter an input "chopper" semiconductor switch (often MOSFET or IGBT) of the standard SMPS is re-

placed with a "resonant" semiconductor switch. The resonant semiconductor switch relies on resonances of circuit capacitances and inductances to shape the waveform of either the current or the voltage across the semiconductor switch such that, when state switching occurs in the semiconductor switch, there is essentially no current through or essentially no voltage across the semiconductor switch. Hence power dissipation is largely eliminated in at least some of the intrinsic capacitances or inductances of the input semiconductor switch such that a marked increase of the switching frequency becomes feasible for example to values above 10 MHz. This concept is known in the art under designations like zero voltage and/or zero current switching (ZVS and/or ZCS) operation. Commonly used switched mode power converters operating under ZVS and/or ZCS are often described as class E, class F or class DE inverters or power converters.

In view of the above, it remains a challenge to reduce the size and lower the component costs of both isolated and non-isolated DC-DC power converters. Hence, novel resonant step-down DC-DC power converter topologies which reduce the required maximum voltage or power rating of active and passive components of the resonant DC-DC converter are highly desirable. Likewise, novel resonant step-down DC-DC power converter topologies which reduce the physical size or cost of active and passive components for example inductors, capacitors, transistors and diodes are highly desirable.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a resonant step-down DC-DC power converter comprising a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier; the primary side circuit comprises a positive input terminal and a negative input terminal for receipt of an input voltage. An input capacitor is coupled or connected between the positive and negative input terminals on the primary side circuit. The secondary side circuit comprising an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode of the output capacitor. The resonant step-down DC-DC power converter comprises a resonant network configured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier by a semiconductor switch arrangement in accordance with a switch

control signal to produce the converter output voltage, wherein a frequency of the switch control signal has a frequency at or above 20 MHz, more preferably at or above 30 MHz. An electrical short-circuit connection across the galvanic isolation barrier connects, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connects the second positive electrode of the output capacitor to the negative input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor. A load connection of the resonant step-down DC-DC power converter exists or is established, in the first case, between the first positive electrode of the output capacitor and the positive input terminal or, in the second case, between the second negative electrode of the output capacitor and the negative input terminal.

The present invention is described in detail in the following with reference to specific implementations derived from isolated resonant DC-DC power converters of class E, class DE and SEPIC topologies. The skilled person will understand that the invention is equally applicable to other types of isolated resonant DC-DC power converters such as class φ_2 (EF_2) inverters and rectifiers and resonant boost, buck, LCC converters etc. In this context the term DC can refer to a slowly varying input voltage where the term “DC” applies to variations of the input voltage level which are slow compared to a switching frequency, i.e. the above-mentioned frequency of the switch control signal, of the resonant step-down DC-DC power converter. The input voltage may accordingly comprise a substantially constant DC input voltage or a rectified AC voltage comprising a DC voltage component and an AC voltage component at a frequency significantly lower, for example more than 100 times lower, than the switching frequency of the resonant step-down DC-DC power converter. In the latter case, the input voltage may be supplied by an output of a 50/60 Hz mains voltage rectifier connected to the positive and negative input terminals of the resonant step-down DC-DC power converter.

The secondary side circuit of the resonant step-down DC-DC power converter may comprise a rectification circuit coupled between the resonant network and the output capacitor to convert a resonant AC voltage waveform of the resonant circuit into a DC converter output voltage.

The semiconductor switch arrangement preferably comprises one or more individual semiconductor switches configured for zero-voltage-switching and/or zero-current-switching. The present resonant step-down DC-DC power converters can be operated at very high switching frequencies, i.e. at or above the 20 MHz or 30 MHz, because the zero-voltage-switching and/or zero-current-switching of the one or more individual controllable semiconductor switches facilitated by the resonant network effectively reduces switching power losses of the semiconductor switch arrangement. A switching frequency at or above 30 MHz is normally considered as VHF operation of the resonant step-down DC-DC power converter.

The semiconductor switch arrangement may comprise various ordinary switch topologies such as single switch topologies, half-bridge switch topologies or full-bridge switch topologies. The one or more individual controllable semiconductor switches of the semiconductor switch arrangement may comprise a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) transistor. A control terminal, e.g. a gate or base, of each of the controllable semiconductor switches may be coupled to, and driven by, the switch control signal to alternatingly force each of the controllable semiconductor switches between on-states and off-states. In the on-state an inductor of the resonant network may be charged with energy from the input voltage source and in the following off-state release stored energy to the output capacitor to charge the latter. The resonant network preferably comprises at least one inductor and at least one capacitor where one or both of these components may comprise parasitic inductances or capacitances of active components or passive components of the resonant step-down DC-DC power converter. The secondary side circuit of the resonant step-down DC-DC converter may comprise one or more passive and/or active rectifying element(s) such as a diode or transistor inserted in front of the converter load.

The electrical connection of an input voltage or power source, e.g. a DC voltage generator, to the present resonant step-down DC-DC power converter is in the first case made between the negative input terminal of the primary side circuit and the positive electrode of the output capacitor such that the input and output capacitors of the converter are connected in series between the positive and negative terminals of the input voltage or power source. Likewise, in the second case the input voltage or

power source is connected between the negative electrode of the output capacitor and the positive input terminal of the primary side circuit such that the input and output capacitors of the converter once again are connected in series between the positive and negative terminals of the input voltage or power source.

The skilled person will understand that the electrical short-circuit connection across the galvanic isolation barrier eliminates the galvanic isolation between the primary and secondary side circuits of the resonant step-down DC-DC converter by interconnecting the second, negative, electrode of the output capacitor and the positive input terminal in the first case or the first, positive, electrode of the output capacitor and the negative input terminal in the second case. However, the electrical short-circuit connection provides numerous new benefits to the resonant step-down DC-DC converter as a whole and the lack of galvanic isolation is acceptable in numerous areas of applications where the converter circuit remains isolated from users such as retrofit LED bulbs and tubes. The series connection of the output and input capacitors between the input voltage/power source terminals established by the electrical short-circuit connection has several advantageous effects. Input current flowing through the input capacitor to charge this to the input voltage is also forced to flow through the output capacitor and charges the output capacitor such that energy or power is transferred directly from the input/primary side to the output/secondary side of the resonant step-down DC-DC converter. Hence, less power or energy needs to be transferred through the resonant network and the isolation barrier for a given output power of the converter as explained in further detail below with reference to the resonant step-down DC-DC converter embodiments of FIGS. 1A), 1B) and 1C). The reduced amount of power transferred to the secondary side circuitry through the resonant network and isolation barrier reduces power losses of or in the resonant step-down DC-DC converter. This advantage is obtained because the direct energy or power transfer between the input and output capacitors of the converter leads to a lower power loss than the ordinary transfer of energy or power through the resonant network.

Furthermore, the reduced amount of power which needs to be transferred through the resonant step-down DC-DC converter leads to reduced power handling requirements for both passive and active components, e.g. semiconductors switches, capacitors, diodes etc., allowing less costly and physically smaller components to be

applied. A yet further significant advantage of the present resonant step-down DC-DC converter is that the primary side circuit is only subjected to the input voltage between the positive and negative input terminals of the primary side circuit instead of the entire converter input voltage supplied by the external input voltage or power source as in ordinary isolated DC-DC power converters. As described above, the input voltage or power source is connected either between the negative input terminal and the positive electrode of the output capacitor or, in the second case, between the negative electrode of the output capacitor and the positive input terminal of the primary side circuit in the present resonant step-down DC-DC converter. The reduced voltage levels in the primary side circuit of the resonant step-down DC-DC power converter reduce the required maximum voltage ratings of active and passive components therein such as semiconductor switch or switches, inductor(s), capacitors, diode(s) etc. The reduced maximum voltage rating leads to physically smaller and/or less costly active and passive components with increased life span.

The galvanic isolation barrier may comprise a transformer which comprises a pair of electro-magnetically or magnetically coupled inductors comprising a first inductor electrically connected to the primary side circuit and a second inductor electrically connected to the secondary side circuit. The first and second inductors could be discrete windings both wound around a common magnetic permeable structure to form an isolation transformer. In one alternative embodiment, the first and second inductors are arranged to be electro-magnetically coupled without a common magnetically permeable structure to form a coreless isolation transformer. In such a coreless isolation transformer, the first and second inductors may be integrated in a printed circuit board without intervening magnetic material. The printed circuit board could have the entire resonant step-down DC-DC power converter mounted thereon. The first and second inductors are preferably arranged such that a magnetic coupling factor, k, between the first and second inductors is larger than 0.25. The first and second inductors of the coreless isolation transformer may for example comprise first and second embedded coils, respectively, formed in one or more conductive layers of the printed circuit board as disclosed in the applicant's co-pending application No. PCT/EP2014/079037.

In yet another embodiment, the galvanic isolation barrier comprises a first capacitor coupled in series with the positive input terminal of the primary side circuit and the first positive electrode of the output capacitor and a second capacitor coupled in series with the negative input terminal of the primary side circuit and the second negative electrode of the output capacitor. This embodiment is particularly advantageous in connection with the high switching frequency of the present resonant step-down DC-DC power converter where the power loss in the above-discussed common magnetic permeable structure of the transformer often will be unacceptable because of the accompanying decrease of power conversion efficiency of the resonant power converter. The capacitor based galvanic isolation barrier becomes particularly advantageous as the capacitance of each of the first and second (isolation) capacitors can be small, such as less than 100 nF for example smaller than 1 nF such as about 100pF. Such isolation capacitors may be formed by SMD mounted ceramic capacitors with a very small footprint e.g. a footprint less than 2 cm^2 for example a footprint down to or less than about 5 mm^2.

The high switching frequency of the present resonant step-down DC-DC power converter, i.e. at or above 20 MHz, also makes the capacitance of each of the input and output capacitors to be small compared to conventional non-resonant DC-DC power converters operating below 1 MHz. Hence, neither the input capacitor nor the output capacitor needs to be an electrolytic capacitor which generally is plagued by relatively low reliability and short-life span instead the first and second isolation capacitors and/or the input and output capacitors of the present resonant step-down DC-DC power converter can be reliable, physically small and inexpensive. The skilled person will understand that the input and output capacitors may be formed exclusively by parasitic capacitances associated with the primary side circuit and the secondary side circuit, respectively.

Another advantage of the high switching frequency of the present resonant step-down DC-DC power converter, as set by the switch control signal, is a marked size decrease of an EMI filter that may be placed in front of the positive and negative input terminals of present converter. The size decrease of the EMI filter is possible because ripple voltage components on the input voltage induced by the switching activity of the present resonant power converter are located around the switching

frequency of converter, i.e. around or above 20 MHz, where the necessary filter components of the EMI filter can be physically small.

The skilled person will appreciate that a practical embodiment of the electrical short circuit connection will possess a finite DC resistance. An upper limit of this finite DC resistance will vary depending on input/output voltage and/or current requirements of the resonant step-down DC-DC power converter. The electrical short-circuit connection may possess a DC resistance of less than 1 kΩ, even more preferably less than 100 Ω, such as less than 10 Ω. In other embodiments, the electrical short circuit connection may have a unidirectional resistance such that the DC resistance only falls below the above-mentioned upper limits in one direction and exhibits a much larger DC resistance in the opposite direction, i.e. a diode characteristic for example provided by a diode element or a controlled semiconductor switch such as a MOSFET.

One embodiment of the resonant step-down DC-DC power converter is based on a Class E converter and the resonant network comprises first and second series connected inductors which are connected in series with the positive input terminal. A semiconductor switch is arranged with a first switch node connected between a midpoint node between the first and second series connected inductors and a second switch node connected to the negative input terminal of the primary side circuit. A control terminal of the semiconductor switch is connected to the switch control terminal. A rectifying or rectification circuit of the resonant step-down DC-DC power is connected between the first and second capacitors of the galvanic isolation barrier and the first positive electrode and the second negative electrode of the output capacitor. The rectifying circuit may comprise a semiconductor diode or a synchronous semiconductor switch coupled, i.e. electrically connected, to a third inductor of the resonant step-down DC-DC power converter.

Another embodiment of the resonant step-down DC-DC power converter is based on a converter topology wherein the first and second inductors of the isolation transformer are integrated in the resonant network. The first inductor is arranged with a first inductor end connected to the positive input voltage terminal and a second inductor end connected to a first node of a semiconductor switch such as a drain ter-

minal of a MOSFET switch. A second node of the semiconductor switch is connected to the negative input terminal of the primary side circuit. The second inductor comprises a first inductor end connected to the first capacitor of the isolation barrier and a second inductor end connected to the second capacitor of the isolation barrier. A rectifying circuit is connected across the second inductor between the first and second capacitors of the galvanic isolation barrier and the first positive electrode and the second negative electrode of the output capacitor.

One embodiment of the resonant step-down DC-DC power converter comprises a mode switching feature that is accompanied with several advantages such as increases a dynamic voltage operating range and/or improving a power factor (PF) of the resonant power converter as discussed in additional detail below with reference to the appended drawings. This embodiment of the resonant step-down DC-DC power converter further comprises:

a rectifying element, such as a diode or or a controlled semiconductor switch such as a MOSFET, configured to:

in the first case conduct current from the positive input terminal to the second negative electrode of the output capacitor in the second case, conduct current from the negative input terminal to the first positive electrode of the output capacitor; and

a mode selecting semiconductor switch configured to selectively break and close an electrical connection between the negative input terminal and the second negative electrode of the output capacitor, such that:

in a first mode of the resonant step-down DC-DC power converter, establishing the series connection of the output capacitor and the input capacitor through the rectifying element and in a second mode of the resonant step-down DC-DC power converter, opening or breaking the series coupling of the output capacitor and the input capacitor.

The skilled person will appreciate that each of the present resonant step-down DC-DC power converters may be constructed by conversion of an isolated resonant DC-DC power converter with a corresponding topology as described in additional detail below with reference to FIGS. 2A) - 2B) FIGS. 3A) - 3B) and FIGS. 4A) - 4B). Hence, a second aspect of the invention relates to a method of converting a resonant DC-DC power converter to a non-isolated/uninsulated resonant step-down DC-

DC power converter possessing higher power conversion efficiency or smaller power loss. The method comprising steps of:

a) providing a primary side circuit and a secondary side circuit of the isolated DC-DC power converter,

b) optionally, coupling an input capacitor between a positive and a negative input terminal of the primary side circuit,

c) optionally, coupling a positive electrode of an output capacitor to a positive output terminal of the secondary side circuit and coupling a negative electrode of the output capacitor to a negative output terminal of the secondary side circuit,

d) providing electrical, e.g. electromagnetic, coupling of the primary side circuit and the secondary side circuit through a galvanic isolation barrier,

e) providing a resonant network configured for alternatingly being charged from an input voltage of the converter and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce a converter output voltage,

f) connecting, in a first case, an electrical short-circuit across the galvanic isolation barrier from the negative output terminal of the secondary side circuit to the positive input terminal of the primary side circuit or connecting, in a second case, the positive output terminal of the secondary side circuit to the negative input terminal of the primary side circuit thereby establishing in both the first case and the second case a series coupling of the output capacitor and the input capacitor,

g) coupling, in a first case, a power converter load between the positive terminal of the secondary side circuit and the positive input terminal or coupling, in the second case, the power converter load between the negative terminal of the secondary side circuit and the negative input terminal of the primary side circuit.

As mentioned above, the coupling of the input capacitor under step b) and the coupling of the output capacitor under step c) are both optional because one or both of the input and output capacitors may be formed exclusively by parasitic capacitances associated with the primary side circuit and the secondary side circuit, respectively.

The improved power conversion efficiency of the present resonant step-down DC-DC power converters is achieved because a smaller or larger amount of the output power delivered to the converter load may be transferred directly from the input volt-

age or power source and input capacitor of the input side circuit to the output capacitor of the secondary side circuit due to the series connection of the input and output capacitors between the input voltage or power source as explained above. Hence, a smaller amount of the output power has to be transferred through the resonant network and isolation barrier leading to lower power losses in the active and/or passive components thereof.

The method may comprise a further step of:

h) in the first case, electrically connecting an input voltage source between the negative input terminal of the primary side circuit and the positive output terminal of the secondary side circuit, or

i) in the second case, electrically connecting an input voltage source between the positive input terminal of the primary side circuit and the negative output terminal of the secondary side circuit.

The conversion of the resonant DC-DC power converter to the non-isolated resonant step-down DC-DC power converter may comprise certain further steps to add the previously discussed advantageous mode switching feature of the converted DC-DC power converter, i.e. the non-isolated resonant step-down DC-DC power converter. According to this embodiment of the conversion methodology the latter comprises further steps of:

j) inserting a rectifying element in the electrical short-circuit connection,

k) inserting a mode selecting semiconductor switch, in the first case, between the positive input terminal and the first positive electrode of the output capacitor and in second case between the negative input terminal and the second negative electrode of the output capacitor.

The skilled person will appreciate that each of the present resonant step-down DC-DC power converters may be constructed by conversion of a conventional or prior art isolated DC-DC power converter possessing a corresponding topology. The skilled person will appreciate that the conventional or prior art isolated DC-DC power converter may be step-up or boost converter delivering a higher output voltage than input voltage despite that the converted resonant step-down DC-DC power converter in accordance with the present invention delivers a lower output voltage than in-

put voltage due to the series connection of the input capacitor and output capacitor across the input voltage source.

A third aspect of the invention relates to a resonant step-down DC-DC power converter assembly comprising:
a resonant step-down DC-DC power converter according any of the above-described embodiments thereof,
a printed circuit board having at least the resonant network integrated thereon,
wherein the galvanic isolation barrier comprises a pair of magnetically coupled inductors comprising a first inductor electrically connected to the primary side circuit and a second inductor electrically connected to the secondary side circuit;
wherein the first and second inductors are formed by first and second electrical trace patterns, respectively, of the printed circuit board. The pair of magnetically coupled inductors may be coupled to each other without any magnetic permeable core material since the latter may be difficult to integrate on a printed circuit board in an efficient manner. The resonant step-down DC-DC power converter according to the latter embodiment of the invention preferably comprises a resonant converter such as class E, class DE or SEPIC converter in accordance with the present invention. The high frequency operation at or above 20 MHz makes the inductances of the first and second inductors sufficiently small to allow these to be integrally formed in the conductor pattern of the printed circuit board. Furthermore, the high switching frequency of the resonant VHF step-down DC-DC power converter as set by the frequency of the switch control signal provides a high magnetic coupling between the first and second inductors despite lack of the magnetic permeable core material. The high switching frequency of the resonant power converter provides a high magnetic coupling, as discussed above, between the pair of magnetically coupled inductors despite the lack of the magnetic permeable core material. The high magnetic coupling reduces the otherwise significant energy losses that would be incurred in the pair of magnetically coupled inductors of the galvanic isolation barrier if the resonant DC-DC power converter was operating at ordinary switching frequencies.
A fourth aspect of the invention relates to a LED light assembly, a charger assembly or a flat-screen display assembly, comprising:
a resonant step-down DC-DC power converter according any of the above-

described embodiments thereof mounted on a printed circuit board of the assembly, an AC mains voltage input connected to an input of a mains rectifier, an output of the mains rectifier connected, in the first case, between the first positive electrode of the output capacitor and the negative input terminal of the primary side circuit or connected, in the second case, between the negative input terminal of the primary side circuit and the negative electrode of the output capacitor to directly supply a rectified mains voltage to the resonant step-down DC-DC power converter in both cases.

The LED light assembly may be mounted in housing of a LED lamp or tube. The converter load may be formed by a plurality of LEDs coupled to the converter output voltage. The AC mains voltage may lie between 110 V and 240 V depending on the electricity system. The LED lamp application is helpful to illustrate the advantages of the present resonant step-down DC-DC power converter. In one exemplary embodiment, the plurality of LEDs may need a DC voltage of about 60 V and consume 10 W. A conventional isolated step-down DC-DC power converter in the LED light assembly connected directly to U.S. mains of 110 V would be required to handle a peak rectified input voltage of about 170 V on a primary side circuit. However, the primary side circuit of the present resonant step-down DC-DC power converter is only required to handle 170 V minus 60 V (i.e. the rectified input voltage minus the output voltage of converter) which is about 110 V. This reduction of DC voltage across the primary side circuit means that smaller and cheaper components such as semiconductor switches can be used. Furthermore, the conventional isolated step-down DC-DC power converter is required to transmit the required 10 W of power to the LEDs of the lamp while the present resonant step-down DC-DC power converter only needs to transmit or supply 110/200 * 10 W = 5.5 W. The residual 4.5 W of output power to the LED load is supplied directly from the 110 V AC mains source to the output of the converter through the mains rectifier and input capacitor.

The skilled person will appreciate that the electrical short-circuit connection across the galvanic isolation barrier provides noteworthy benefits to the present resonant step-down DC-DC power converter for example a reduction of the input voltage across the primary side circuit. These benefits are due to a marked reduction of peak AC voltage across the semiconductor switch or switches of the resonant power

converters. This peak AC voltage is often about 3 times larger than the input voltage of the primary side circuit due to the resonant waveforms inside the resonant network of the resonant power converter. Furthermore, since resonant power converters rely on a resonant current, securing ZVS/ZCS operation of the semiconductor switch or switches, which scales linearly with the input voltage, the resistive power losses in components of the resonant network incurred by this resonating current scale quadratically with the resonant current. Hence, the total power loss in the resonant network scales quadratically with the input voltage. The advantages, in particular the increase of power conversion efficiency, derived from the reduction of the input voltage to the primary side circuit provided by resonant step-down DC-DC power converters in accordance with the present invention are therefore particularly pronounced for resonant converter topologies.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention will be described in more detail in connection with the appended drawings, in which:

FIGS. 1A) and 1B) are simplified electrical circuit diagrams illustrating a resonant step-down DC-DC power converter in accordance with a first embodiment of the present the invention,

FIG. 1C) is a simplified electrical circuit diagram of a resonant step-down DC-DC power converter in accordance with a second embodiment of the present the invention,

FIG. 1D) is a simplified electrical circuit diagram of a resonant step-down DC-DC power converter in accordance with a 3rd embodiment of the present the invention,

FIG. 1E) is a simplified electrical circuit diagram of a resonant step-down DC-DC power converter in accordance with a 4th embodiment of the present the invention,

FIG. 1F) is simplified electrical circuit diagram of a first converter core that may be utilized in resonant step-down DC-DC power converter in accordance the present the invention,

FIG. 1G) is simplified electrical circuit diagram of a second converter core that may be utilized in resonant step-down DC-DC power converter in accordance the present the invention,

FIG. 2A) is an electrical circuit diagram of a prior art isolated class E resonant DC-DC converter comprising a series resonant circuit,

FIG. 2B) is an electrical circuit diagram of a class E resonant step-down resonant DC-DC power converter comprising a series resonant circuit in accordance with a 7th embodiment of the invention,

FIG. 3A) is an electrical circuit diagram of a prior art transformer coupled isolated class E resonant DC-DC converter comprising a series resonant circuit,

FIG. 3B) is an electrical circuit diagram of a transformer coupled class E resonant step-down DC-DC power converter comprising a series resonant circuit in accordance with an 8th embodiment of the invention,

FIG. 4A) is an electrical circuit diagram of a prior art isolated SEPIC converter; and

FIG. 4B) is an electrical circuit diagram of a step-down SEPIC resonant DC-DC converter in accordance with a 9th embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIGS. 1A), 1B) and 1C) are simplified electrical circuit diagrams 100a, 100b, 100c illustrating basic operational features of two different embodiments of resonant step-down DC-DC power converters in accordance with the present invention. The first embodiment is illustrated on FIGS. 1A) and 1B) while the second embodiment is illustrated on FIG. 1C).

FIG. 1A) shows a resonant step-down DC-DC power converter 100b comprising a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 107b. The primary side circuit comprises a positive input terminal 102b and a negative input terminal 101b for receipt of a DC or AC input voltage V_{in} from an input voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 102b and a negative input terminal 101b to form an energy reservoir for the input power or input voltage source. The primary side circuit additionally comprises an input side 106b of a resonant network arranged in front of a galvanic isolation barrier 107. The secondary side circuit comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at output terminal 104b. A second electrode of the output capacitor C_{out}, situated at a lower voltage potential than the first electrode, is connected to the positive input terminal 102b on the input side circuit via an electrical short-circuit connection or wire 109b extending across the galvanic isolation barrier 107b. The output capacitor C_{out} and input capacitor C_{in} are connected in series

or cascade between the DC or AC input voltage V_{in}, i.e. between positive and negative terminals of the input voltage or power source coupled to the output terminal 104b and the negative input terminal 101b, respectively. The skilled person will understand that the presence of the electrical short-circuit connection 109b provides the conversion from an ordinary resonant isolated DC-DC power converter to the present resonant step-down DC-DC power converter which lacks galvanic isolation between the input side circuit and the output side circuit. In this conversion process, the input voltage port of the original resonant isolated DC-DC power converter between the positive and negative terminals 102b, 101b (i.e. across C_{in}) is altered such that the input voltage port, for receipt of the DC or AC input voltage V_{in}, of the present, converted, resonant step-down DC-DC power converter 100b is arranged either between the output terminal 104b and the negative input terminal 101b in the first case or in the second case between the positive input terminal 102c and the negative electrode 103c of the output capacitor C_{out} as illustrated on FIG. 1A) and FIG. 1C), respectively. The resonant step-down DC-DC power converter embodiments 100b, 100c may comprise permanently connected electrical short-circuit connections or wires 109b, 109c to provide a single mode of operation of the resonant DC-DC power converter in question with fixed voltage step-down functionality. In alternative embodiments of the present DC-DC power converters, the coupling or interconnection of the primary and secondary circuits of the power converters 100b, 100c through the electrical short-circuit connections 109b, 109c may be selectable or programmable such that each of the power converters 100b, 100c may possess two distinct and selectable modes of operation as discussed below in further detail with reference to FIGS. 1D) and 1E). The skilled person will understand that the input and output capacitors C_{in} and C_{out} of the resonant step-down DC-DC power converter embodiments 100b, 100c may be formed exclusively by parasitic capacitances associated with the primary side circuit and the secondary side circuit, respectively.

An electrical load R_L of the step-down DC-DC converter 100b is coupled between the output terminal 104b and the positive input terminal 102b, which is across the output capacitor, such that these terminals form an output port of the DC-DC converter 100b. The primary side circuit comprises the previously discussed input side 106b of the resonant network of the step-down DC-DC converter 100b and the sec-

ondary side circuit comprises an output side 108b of the resonant network. The skilled person will appreciate that the resonant network may include numerous circuit topologies depending on the particular type of DC-DC converter in question. The resonant network preferably comprises at least one inductor for energy storage and release, but may alternatively exclusively comprise capacitors for energy storage. Generally, the resonant network is configured for alternatingly being charged from the input voltage V_{in} and discharged to the output capacitor C_{out} through the isolation barrier 107b in accordance with a switch control signal to produce the converter output voltage V_{out}. The primary side circuit preferably comprises at least one semiconductor switch, for example a MOSFET, which is switched between on-states and off-states by the switch control signal such that the input voltage is modulated in accordance with a switch control signal. The frequency of the switch control signal of the semiconductor switch arrangement which excites the resonant network may be at or above 30 MHz to form a so-called VHF type of step-down DC-DC power converter. The switch control signal may comprise a PWM modulated control signal. The primary side circuit may comprise an inductor that is charged with energy during an on-state of the least one semiconductor switch from the input capacitor C_{in} and/or the DC or AC input voltage V_{in}. The inductor of the primary side circuit may subsequently be discharged through the output side 108b of the resonant network and the output capacitor C_{out} in an off-state of the least one semiconductor switch. The secondary side circuit may comprise a diode based rectifier or a synchronous rectifier in front of the output capacitor to produce the converter output voltage V_{out} as a DC output voltage.

While the electrical short-circuit connection or wire 109b eliminates the galvanic isolation between the primary and secondary side circuits of the resonant step-down DC-DC converter 100b by interconnecting the second electrode of the output capacitor C_{out} and the positive input terminal 102b, it provides numerous new benefits to the DC-DC converter as a whole as illustrated with reference to FIG 1B). The series connection of the output and input capacitors C_{out}, C_{in} means that the primary side circuit only needs to withstand the converter output voltage V_{out} minus the input voltage across C_{in} instead of the entire DC or AC input voltage V_{in} delivered by the input voltage or power source which is the situation in the prior art isolated DC-DC converter topology. The reduced voltage across the primary side circuit reduces the

required maximum voltage rating of active and passive components therein leading to physically smaller and/or less costly active and passive components for example inductors, capacitors (including C_{in}), transistors and diodes etc. In addition, the life span of the latter components may increase by the smaller voltage stress. In the input section 106b and output section 108b, the smaller amount of power to be transferred through the DC-DC converter 100b for supplying a given amount of power to the load R_L of the converter leads to reduced power requirements for active semiconductors switches allowing less costly and physically smaller semiconductors to be applied.

These beneficial reductions of the amount of power transferred through the resonant network 106b, 107b, 108b are achieved because the residual fraction of the output power supplied to the load R_L is transferred directly from the DC or AC input voltage source V_{in} to the output capacitor C_{out} during charging of the input capacitor C_{in} This power transfer mechanism is illustrated on FIG. 1B) by the first output current path $I_{convert}$ which shows how secondary side current charges the output capacitor C_{out} and delivers output power to the load R_L of the converter. The secondary side current comprises an AC component 113a and a DC component 113b such that the latter is dissipated in the load R_L. Hence, the secondary side current delivers output power passing from the source of the DC or AC input voltage V_{in} and through the resonant network to the output side circuit in a conventional manner. However, the present DC-DC converter 100b also comprises a second output current path delivering current or power directly from the DC or AC input voltage source to the output capacitor C_{out} and the load R_L without passing through the power converter 100b. This direct current comprises an AC current component delivered to the output capacitor C_{out} as illustrated by AC input current path 111a and a DC current component delivered to the load R_L as illustrated by DC input current path 111b. The AC current component 111a and the DC current component 111b of the input current path passes through the short-circuit connection 109b and through the positive and negative inputs of the primary side circuit 106b such that the DC current component 111b of the direct current remains unprocessed by the converter. Hence, this DC current component is supplied directly to the load R_L without any noticeable power loss.

The skilled person will appreciate that a practical electrical short circuit connection

109b will possess a certain DC resistance and an upper limit for this DC resistance will vary depending on input/output voltage and/or current requirements of the converter 100b. The electrical short-circuit connection may possess a DC resistance of less than 1 kΩ, even more preferably less than 100 Ω, such as less than 10 Ω. In other embodiments, the electrical short circuit connection 109b may have a unidirectional resistance such that the DC resistance only falls below the above-mentioned upper limits in one direction and exhibits a much larger DC resistance in the opposite direction, i.e. a diode characteristic.

In the alternative embodiment of the resonant step-down DC-DC converter topology illustrated on FIG. 1), the electrical short-circuit connection or wire 109c extending across the isolation barrier 107c is connecting the first positive electrode of the output capacitor C_{out} to the negative input terminal 101c of the primary side circuit. Thereby, a series coupling of the output capacitor C_{out} and the input capacitor C_{in} from the input voltage V_{in} at the positive input terminal 102c to the negative electrode 103c of the output capacitor C_{out} is established. The negative electrode 101c of the output capacitor C_{out} is at a lower electric potential than the negative input terminal 101c. In this manner, the DC or AC input voltage V_{in} to the power converter 100c is once again applied across the series connected input and output capacitors C_{in} and C_{out}. The converter load R_L is coupled between the output terminal 104c and the terminal 103c which also is across the output capacitor. Otherwise, circuit functions, electrical component characteristics and component values of this second embodiment of resonant power converter 100c may be identical to those of the first embodiment of the resonant power converter 100b.

FIG. 1D) is a simplified electrical circuit diagram of a resonant step-down DC-DC power converter 100d in accordance with a third embodiment of the present the invention. A converter core 105d of the resonant power converter 100d may be identical to the core 105b of the resonant power converter 100c discussed above in connection with FIG. 1A) and 1B). Hence, corresponding features of these different power converter embodiments 100b, 100d have been provided with corresponding reference numerals/symbols to assist comparison. The present resonant power converter embodiment 100d comprises a mode selecting controllable semiconductor switch SW1 operating in conjunction with a rectifying element 111e such as a diode

or an active semiconductor diode such as a controllable semiconductor switch. The operation of the resonant step-down DC-DC power converter 100d corresponds to the operation of the resonant step-down DC-DC power converter 100e discussed in detail below.

FIG. 1E) shows a simplified electrical circuit diagram of a resonant step-down DC-DC power converter 100e in accordance with a 4th embodiment of the present the invention. A converter core 105e of the resonant power converter 100e may be identical to the core 105 of the resonant power converter 100c discussed above in connection with FIG. 1C). Hence, corresponding features of these different power converter embodiments 100c, 100e have been provided with corresponding reference numerals/symbols to assist comparison. The present resonant power converter embodiment 100e comprises a mode selecting controllable semiconductor switch SW1 operating in conjunction with a rectifying element 111e such as a diode or an active semiconductor diode such as a controllable semiconductor switch. The rectifying element 111e is inserted in a short-circuit connection or wire 109e which connects a negative input terminal 109e of the power converter to a first positive electrode of the output capacitor C_{out}. The latter short-circuit connection corresponds to the short circuit connection 109c of the previously discussed resonant power converter 100c. Hence, when the rectifying element 111e is forward biased the short-circuit wire 109e effectively places the output capacitor C_{out} and input capacitor C_{in} is series, albeit possibly with a minor diode voltage drop, between the input voltage V_{in} terminals 104e, 103e of the resonant power converter 100e. On the other hand, when the rectifying element 111e is reversely biased the series coupling of C_{out} and C_{in} through short-circuit wire 109e is broken or disconnected to break the electrical connection between the primary side circuit and the secondary side circuit of the resonant power converter 100e.

The mode selecting controllable semiconductor switch SW1 is coupled between the negative input terminal 101e and the second negative electrode of the output capacitor 103e and configured to selectively break and close the electrical connection between these terminals 101e, 103e. The switch SW1 may comprise one or more BJT(s), FET(s) MOSFET(s) or IGBT(s) such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) transistor. SW1 may be switched between a conducting or ON state

and non-conducting or OFF state to connect and break, respectively, the electrical connection between terminals 101e, 103e by a suitable control voltage applied on a gate or base terminal of the switch SW1. A mode controlling circuit (not shown) integrated with or coupled to the present resonant power converter 100e may supply this control voltage to SW1.

When the mode selecting controllable semiconductor switch SW1 is placed in the non-conducting or OFF state (as illustrated) the negative terminals of the C_{out} and C_{in} capacitors are disconnected and the rectifying element 111e forward biased. Hence, the input and output capacitors C_{out} and C_{in} are series connected through the rectifying element 111e. The rectifying element 111e is forward biased because the DC or AC input voltage V_{in} is larger than the output voltage V_{out} allowing the previously discussed input current of the power converter to flow directly through C_{in} and into C_{out} to charge the output capacitor. Hence, the resonant power converter 100e is placed in a first mode of operation where it largely functions as the resonant power converter 100c of FIG. 1C) discussed above, i.e. as a resonant step-down non-isolated DC-DC power converter. By placing the controllable semiconductor switch SW1 in the conducting or ON state, the present resonant power converter embodiment 100e is switched to the second mode of operation. In the second state of operation, the rectifying element 111e is reversely biased and hence non-conducting due to the electrical connection between the negative capacitor terminals 101e, 103e. Hence, the above-discussed series connection (through the rectifying element 111e) of the input and output capacitors C_{out} and C_{in} in the first mode is broken or opened. In this second mode of operation of the the resonant power converter 100e, it largely functions as an ordinary resonant DC-DC power converter albeit still without any galvanic isolation between the primary and secondary side circuits because of the presence of the rectifying element 111e.

The mode switching feature, i.e. from the first mode to the second mode or vice versa, of the present resonant power converter 100e is accompanied with several advantages. The mode switching feature may be used to dynamically switch the present resonant power converter 100e between the first and second modes during operation of the converter 100e by appropriate control of the control terminal of SW1.The dynamic mode switching feature increases the input voltage range of the

resonant power converter 100e. To illustrate these advantages consider an ordinary resonant DC-DC power converter designed for a DC input voltage range of 10 – 20 V and a DC output voltage range of 10 V. If this ordinary DC-DC power converter is converted or configured as the present resonant step-down DC-DC power converter, the DC input voltage range may be increased to 10 - 30 V by utilizing both the first mode and second mode of the resonant step-down DC-DC power converter during operation of the converter. Hence, the resonant step-down DC-DC power converter is switched dynamically between the first and second modes of operation in accordance with the input voltage waveform. The increase of DC input voltage range achieved by the dynamic mode switching feature is particular advantageous because resonant power converters generally suffer from a restricted or narrow DC input voltage range compared to non-resonant DC-DC power converters. Another advantage of the dynamic mode switching feature is an improved power factor (PF) of the resonant power converter 100e. The power factor of a switched mode power converter or supply is an important performance metric in numerous applications such as LED lamps where regulatory requirements for minimum power factor, such as larger than 0.9, may exist. The improved PF is achieved by the dynamic mode switching feature because this feature allows the converter to track AC variations of the input voltage to the converter such as the AC variations in the waveform of a rectified 50/60 Hz mains voltage.

The flow of input current in the resonant step-down DC-DC power converter 100e in the first and second modes of operation is illustrated by a first DC input current path 111b1 and a second DC input current path 111b2. When the first mode of operation of the converter 100e is selected, i.e. the step-down functionality, the input current flows through the first DC input current path 111b1 where DC input current flows through the diode 111e and through the converter load R_L. When the second mode of operation of the converter 100e is selected, i.e. SW1 is conducting and ordinary conversion functionality, the input current flows through the second DC input current path 111b2 where the diode 111e is blocking and the DC input current flows through SW1 to the negative rail or terminal 103d of the converter without passing through the converter load.

FIG. 1F) is a simplified electrical circuit diagram of a first converter core 105f that may be utilized as converter core 105b, 105c, 105d, 105e of each of the step-down DC-DC power converter embodiments 100b, 100c, 100d, 100e, illustrated on FIGS. 1A), 1B), 1C), 1D) and 1E), respectively. The first converter core 105f comprises a plurality of separate resonant DC-DC power converter cores 110f. Each of the separate resonant DC-DC power converter cores 110f comprises an input side 111 of a resonant network coupled to an output side 113 of the resonant network through a galvanic isolation barrier 107f. The input sides 111 of the resonant DC-DC power converter cores 110e may be connected in parallel or series. The output sides 113 of the resonant DC-DC power converter cores 110f may likewise be connected in parallel or series. The parallelization of the plurality of input sides 111 and/or the parallelization of the one or more output sides 113 increases the power rating of a step-up DC-DC power converter utilizing the first converter core 105f. The skilled person will understand that each of the separate resonant DC-DC power converter cores 110f may comprise one of the prior art resonant DC-DC power converter cores discussed below with reference to FIGS. 2, 3 and 4.

FIG. 1G) is simplified electrical circuit diagram of a second converter core 105g that may be utilized as converter core 105b, 105c, 105d, 105e of each of the step-down DC-DC power converter embodiments 100b, 100c, 100d, 100e illustrated on FIGS. 1A), 1B), 1C), 1D) and 1E), respectively. The second converter core 105g comprises a plurality of separate resonant power inverters 114g. Each of the separate resonant power inverter cores 114g comprises an input side 115 of a resonant network coupled to one or more rectifier(s) 117 of the resonant DC-DC power converter core 105g through a galvanic isolation barrier 107g. The separate resonant power inverter cores 114g may be connected in parallel or series. Likewise, the respective output side of the one or more rectifier(s) 117 may also be connected in series or parallel. However, galvanic isolation may be inserted between the one or more rectifier(s) 117 if these are coupled in series.

FIG. 2A) shows an electrical circuit diagram of a prior art isolated class E resonant DC-DC converter 200 comprising a series resonant network or circuit including inductor L_2 and capacitor C_1. The prior art class E resonant converter comprises a primary side circuit and a secondary side circuit connected through a galvanic isola-

tion barrier 207. The primary side circuit comprises a positive input terminal 202 and a negative input terminal 201 for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 202b and a negative input terminal 201 to form an energy reservoir for the voltage source. A converter core 205 comprises a resonant network which includes first and second series connected inductors L_1 and L_2 and a semiconductor switch arrangement comprising a MOSFET switch S (or another suitable type of semiconductor switch) with a drain terminal connected to a midpoint node between the L_1 and L_2. The primary side circuit is arranged in front of an isolation barrier 207 formed by coupling capacitors C_1 and C_2. The secondary side circuit comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at output terminal 204. A second negative electrode of the output capacitor C_{out} is coupled to a negative terminal 203 of the converter output voltage. A load of the isolated class E resonant DC-DC converter 200 is schematically illustrated by load resistor R_L and coupled between the positive and negative output terminals 204, 203.

FIG. 2B) is an electrical circuit diagram of a class E resonant step-down DC-DC power converter 200c comprising a series resonant circuit in accordance with a 7th embodiment of the invention. The class E resonant step-down DC-DC power converter 200b may be obtained by conversion of the above-mentioned prior art isolated class E resonant DC-DC converter 200 by inserting or adding an electrical short circuit connection 209c extending across a galvanic isolation barrier 207c of the converter 200c. The galvanic isolation barrier 207c comprises series capacitors C_1 and C_2.The electrical short circuit connection 209c electrically connects the negative input terminal 201c and the first positive electrode 204c of the output capacitor C_{out}. The first positive electrode 204c is also connected to the converter output voltage V_{out}. As discussed in connection with FIG. 1C), the electrical short-circuit connection or wire 209c effectively places the output capacitor C_{out} and input capacitor C_{in} in series or cascade across the DC or AC input voltage V_{in}. Hence, the converter load, schematically illustrated by the load resistor R_L, is coupled in parallel across the output capacitor C_{out}. The skilled person will understand that the series capacitor C_2 of the galvanic isolation barrier 207c prevents DC current from flowing from the second negative electrode 203b of the output capacitor C_{out} and back to the negative input

terminal 201c. In this manner, the DC current is directed or forced through the electrical short circuit connection 209b and back through the input capacitor C_{in}. In this manner, despite being electrically by-passed by the conversion, the isolation barrier 207c is important for the operation of the present class E resonant step-down DC-DC power converter 200c as otherwise would nodes 201c and 203c and 204c be directly electrically connected causing a short circuit at the converter input.

The series resonant network of the converter core 205c of the converter 200c may, in addition to the above-discussed first and second series connected inductors L_1 and L_2, comprise a capacitor (C_S) arranged across drain and source terminals of the MOSFET switch S to increase a resonant current and/or adjust/fine-tune a resonance frequency of the power converter 200c. Likewise, a yet further capacitor C_D may be arranged across the rectifying diode D to adjust a duty cycle of the secondary part of the power converter 200c, i.e. the class E rectifier. During operation of the converter 200c, the series resonant network is excited by the MOSFET switch S such that the series resonant network is alternatingly charged from the DC or AC input voltage V_{in} and discharged to the output capacitor C_{out} through the galvanic isolation barrier 207c and through a rectification circuit comprising inductance L_3 and diode D.

FIG. 3A) is an electrical circuit diagram of a prior art transformer isolated class E resonant DC-DC converter 300 comprising a series resonant circuit. A converter core 305 of the converter 300 comprises a series resonant circuit which at least inductors L_2, L_3 and capacitors C_S and C_1. The prior art DC-DC converter 300 comprises a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 307 provided by the transformer 308. The primary side circuit comprises a positive input terminal 302 and a negative input terminal 301 for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 302 and a negative input terminal 301 to form an energy reservoir for the input voltage source. The primary side circuit additionally comprises a portion of a series resonant network or circuit which at least comprises inductors L_2 and capacitors C_S and C_1. A first inductor L_1 has a first end coupled to the positive input terminal 302 and a second end to a drain terminal of a MOSFET switch S which forms a switch arrange-

ment of the present power converter 300. A secondary side circuit of the power converter 300 comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at output terminal 304. A second negative electrode of the output capacitor C_{out} is coupled to a negative terminal 303 of the converter output voltage. An electrical or power converter load is schematically illustrated by load resistor R_L and coupled between the positive and negative output terminals 304, 303 of the prior art DC-DC converter 300. The secondary side circuit furthermore comprises the third inductor L_3 connected across a secondary transformer winding of the above-mentioned transformer 308. The secondary transformer winding has a first end coupled to a cathode of rectifying diode D and a second end coupled to the positive electrode of the output capacitor C_{out}. The rectifying diode D rectifies AC current generated by the secondary transformer winding and generates a DC voltage as the converter output voltage between the positive and negative output terminals 304, 303. An electrical or power converter load is schematically illustrated by load resistor R_L coupled between the positive and negative output terminals 304, 303.

FIG. 3B) is an electrical circuit diagram of a transformer coupled class E resonant step-down DC-DC power converter 300c in accordance with an 8th embodiment of the invention. The step-down DC-DC power converter 300c may be obtained by conversion of the above-mentioned prior art resonant isolated DC-DC converter 300 by inserting or adding an electrical short circuit connection 309c extending across a galvanic isolation barrier formed by the transformer 308b. The transformer 308b comprises magnetically coupled primary and secondary transformer windings with the polarity inversion indicated by the black dots at the top of the windings. A converter core 305c of the converter 300 comprises a series resonant network or circuit which at least comprises inductors L_2, L_3 and capacitors C_S and C_1. During operation of the converter 300c, the series resonant network is excited by the MOSFET switch S such that the series resonant network is alternatingly charged from the DC or AC input voltage V_{in} and discharged to the output capacitor C_{out} through the galvanic isolation barrier 307c and through a rectification circuit comprising diode D.

The electrical short circuit connection 309c connects the negative input terminal 302b of the primary side circuit and the first positive electrode 304c of the output capacitor C_{out} where the latter electrode also supplies the converter output voltage. As discussed in connection with FIGS. 1C), the electrical short-circuit connection or wire 309c effectively places the output capacitor C_{out} and input capacitor C_{in} is series or cascade across the positive and negative connections to the DC or AC input voltage V_{in}. Hence, the converter load, schematically illustrated by the load resistor R_L, is coupled between the converter output voltage across the positive and negative electrodes of the output capacitor C_{out}. The skilled person will understand that the transformer coupling prevents DC current from flowing from the second negative electrode 303c of the output capacitor C_{out} and back to the negative input terminal 301c of the primary side circuit.

FIG. 4A) is an electrical circuit diagram of a prior art isolated single-ended primary-inductor converter (SEPIC) 400. The prior art SEPIC 400 comprises a primary side circuit and a secondary side circuit connected through a galvanic isolation barrier 407. The primary side circuit comprises a positive input terminal 402 and a negative input terminal 401 for receipt of a DC or AC input voltage V_{in} from a voltage or power source (not shown). An input capacitor C_{in} is electrically connected between the positive input terminal 402 and a negative input terminal 401 to form an energy reservoir for the input voltage source. A converter core 405 of the converter 400 comprises a series resonant circuit which includes a first inductor L_1 having first node coupled to the DC or AC input voltage V_{in} and a second node coupled to a drain terminal of a MOSFET switch S. A source terminal of a MOSFET switch S of a switch arrangement is coupled to the negative input terminal 401. The prior art SEPIC 400 is a resonant type of power converter wherein a resonance frequency of the converter is determined by the resonant network of the converter core 405 comprising the first and second inductors L_1, L_2 and the capacitors C_S and C_D. The primary side circuit is arranged in front of a galvanic isolation barrier 407 within the converter core 405 and formed by coupling capacitors C_1 and C_2. The secondary side circuit comprises an output capacitor C_{out} having a first electrode electrically connected to the converter output voltage V_{out} at a positive output terminal 404. A second negative electrode of the output capacitor C_{out} is coupled to a negative terminal 403 of the converter output voltage. A rectifying diode D rectifies AC current generated by a second inductor

L_2 and charges the output capacitor C_{out} such that the converter output voltage V_{out} between the positive and negative output terminals 404, 403 is a DC voltage. A converter load of the SEPIC 400, illustrated by load resistor $R_{L,}$ is coupled between the positive and negative output terminals 404, 403.

FIG. 4B) is an electrical circuit diagram of a SEPIC 400c in accordance with a 9th embodiment of the invention. The SEPIC 400c may be obtained by conversion of the above-mentioned prior art SEPIC 400 by inserting or adding an electrical short circuit connection 409c extending across a galvanic isolation barrier 407c of the SEPIC 400c. The galvanic isolation barrier 407c comprises series capacitors C_1 and C_2 which prevent the flow of DC current between the secondary side circuit and the primary side circuit in the isolated SEPIC 400 discussed above. In the present SEPIC 400c, the electrical short circuit connection 409c electrically connects the negative input terminal 401c and the positive electrode 404c of the output capacitor C_{out}. As discussed in connection with FIGS. 1A) and 1B), the electrical short-circuit connection or wire 409c effectively places the output capacitor C_{out} and input capacitor C_{in} is series or cascade across the positive and negative connections to the DC or AC input voltage V_{in} such that the galvanic isolation between the primary and secondary side circuits is bypassed or eliminated. The electrical or power converter load, schematically illustrated by the load resistor R_L, is coupled between the converter output voltage V_{out} at the output terminal 404c and the negative electrode 403c of the output capacitor. The skilled person will understand that the series capacitor C_2 of the galvanic isolation barrier 407b prevents DC current from flowing from the second negative electrode 403b of the output capacitor C_{out} and directly back to the negative input terminal 401b of the primary side circuit. The SEPIC 400c comprises a converter core 405c comprises a resonant network as discussed above comprising first and second inductors L_1, L_2 and capacitors C_S and C_D. During operation of the converter 400c, the series resonant network is excited by the MOSFET switch S such that the series resonant network is alternatingly charged from the DC or AC input voltage V_{in} and discharged to the output capacitor C_{out} through the galvanic isolation barrier 407c and through a rectification circuit comprising a rectifying diode D. The capacitor C_S connected or arranged across drain and source terminals of the MOSFET switch S is optional, but may be helpful to increase a resonant current and/or adjust/fine-tune a resonance frequency of the resonant network SEPIC

400c. In some embodiments of the SEPIC 400c the capacitor C_S may be formed exclusively by a parasitic capacitance of the MOSFET S. The optional capacitor C_D may be arranged across the rectifying diode D to adjust a duty cycle of the power converter 400c.

5

CLAIMS

1. A resonant step-down DC-DC power converter comprising:
a primary side circuit and a secondary side circuit coupled through a galvanic isolation barrier,
the primary side circuit comprising a positive input terminal and a negative input terminal for receipt of an input voltage and an input capacitor coupled between the positive and negative input terminals,
the secondary side circuit comprising an output capacitor chargeable to a converter output voltage between a first positive electrode and a second negative electrode of the output capacitor,
a resonant network configured for alternatingly being charged from the input voltage and discharged to the output capacitor through the galvanic isolation barrier by a semiconductor switch arrangement in accordance with a switch control signal to produce the converter output voltage, wherein a frequency of the switch control signal has a frequency at or above 20 MHz,
an electrical short-circuit connection across the galvanic isolation barrier connecting, in a first case, the second negative electrode of the output capacitor to the positive input terminal of the primary side circuit or, in a second case, connecting the second positive electrode of the output capacitor to the negative input terminal of the primary side circuit thereby establishing in both the first and second cases a series coupling of the output capacitor and the input capacitor,
a load connection, in the first case, between the first positive electrode of the output capacitor and the positive input terminal or, in the second case, between the second negative electrode of the output capacitor and the negative input terminal.

2. A resonant step-down DC-DC power converter according to claim 1, wherein the galvanic isolation barrier comprises:
a pair of magnetically coupled inductors comprising a first inductor electrically connected to the primary side circuit and a second inductor electrically connected to the secondary side circuit.

3. A resonant step-down DC-DC power converter according to claim 2, wherein the first and second inductors are wound around a common magnetically permeable structure to form an isolation transformer.

4. A resonant step-down DC-DC power converter according to claim 2, wherein the first and second inductors are arranged to be magnetically coupled without a common magnetically permeable structure to form a coreless isolation transformer.

5. A resonant step-down DC-DC power converter according to claim 4, wherein the first and second inductors comprises first and second embedded coils, respectively, formed in one or more conductive layers of a printed circuit board.

6. A resonant step-down DC-DC power converter according to claim 4 or 5, wherein a magnetic coupling factor, k, between the first and second inductors is larger than 0.25.

7. A resonant step-down DC-DC power converter according to claim 1, wherein the galvanic isolation barrier comprises:
a first capacitor coupled in series with the positive input terminal of the primary side circuit and the first positive electrode of the output capacitor; and
a second capacitor coupled in series with the negative input terminal of the primary side circuit and the second negative electrode of the output capacitor;

8. A resonant step-down DC-DC power converter according to claim 7, wherein a capacitance of each of the first and second capacitors is smaller than 100 nF.

9. A resonant step-down DC-DC power converter according to any of the preceding claims, wherein a DC resistance of the electrical short-circuit connection is less than 1 kΩ.

10. A resonant step-down DC-DC power converter according to any of the preceding claims, wherein the resonant network comprises:
first and second series connected inductors connected in series with the positive input voltage terminal,

a semiconductor switch having a first switch node connected between a mid-point node between the first and second series connected inductors, a second switch node connected to the negative input terminal of the primary side circuit and a control terminal connected to the switch control terminal; and

a rectifying circuit connected between the first and second capacitors of the galvanic isolation barrier and the first positive electrode and the second negative electrode of the output capacitor.

11. A resonant step-down DC-DC power converter according to any of the preceding claims, wherein the semiconductor switch arrangement comprises one or more controllable semiconductor switches.

12. A resonant step-down DC-DC power converter according to claim 11, wherein the one or more controllable semiconductor switches are configured for zero-voltage-switching and/or zero-current-switching.

13. A resonant step-down DC-DC power converter according to any of the preceding claims further comprising:

a rectifying element such as a diode configured to:

in the first case conduct current from the positive input terminal to the second negative electrode of the output capacitor in the second case, conduct current from the negative input terminal to the first positive electrode of the output capacitor; and

a mode selecting semiconductor switch configured to, in the first case, selectively break and close an electrical connection between the positive input terminal and the first positive electrode of the output capacitor and in second case selectively break and close an electrical connection between the negative input terminal and the second negative electrode of the output capacitor, such that:

in a first mode of the resonant step-down DC-DC power converter, establishing the series connection of the output capacitor and the input capacitor through the rectifying element; and

in a second mode of the resonant step-down DC-DC power converter, opening or breaking the series coupling of the output capacitor and the input capacitor.

14. A method of converting a resonant isolated DC-DC power converter having a switching frequency at or above 20 MHz to a resonant non-isolated step-down DC-DC power converter possessing higher power conversion efficiency, said method comprising steps of:

a) providing a primary side circuit and a secondary side circuit of the isolated DC-DC power converter,

b) optionally, coupling an input capacitor between a positive and a negative input terminal of the primary side circuit,

c) optionally, coupling a positive electrode of an output capacitor to a positive output terminal of the secondary side circuit and coupling a negative electrode of the output capacitor to a negative output terminal of the secondary side circuit,

d) providing electrical coupling of the primary side circuit and the secondary side circuit through a galvanic isolation barrier,

e) providing a resonant network configured for alternatingly being charged from an input voltage of the converter and discharged to the output capacitor through the galvanic isolation barrier in accordance with a switch control signal to produce a converter output voltage,

f) connecting, in a first case, an electrical short-circuit across the galvanic isolation barrier from the negative output terminal of the secondary side circuit to the positive input terminal of the primary side circuit or connecting, in a second case, the positive output terminal of the secondary side circuit to the negative input terminal of the primary side circuit thereby establishing in both the first case and the second case a series coupling of the output capacitor and the input capacitor,

g) coupling, in a first case, a power converter load between the positive terminal of the secondary side circuit and the positive input terminal or coupling, in the second case, the power converter load between the negative terminal of the secondary side circuit and the negative input terminal of the primary side circuit.

15. A method of converting an isolated DC-DC power converter according to claim 14, comprising a further step of:

h) in the first case, electrically connecting an input voltage source between the negative input terminal of the primary side circuit and the positive output terminal of the secondary side circuit, or

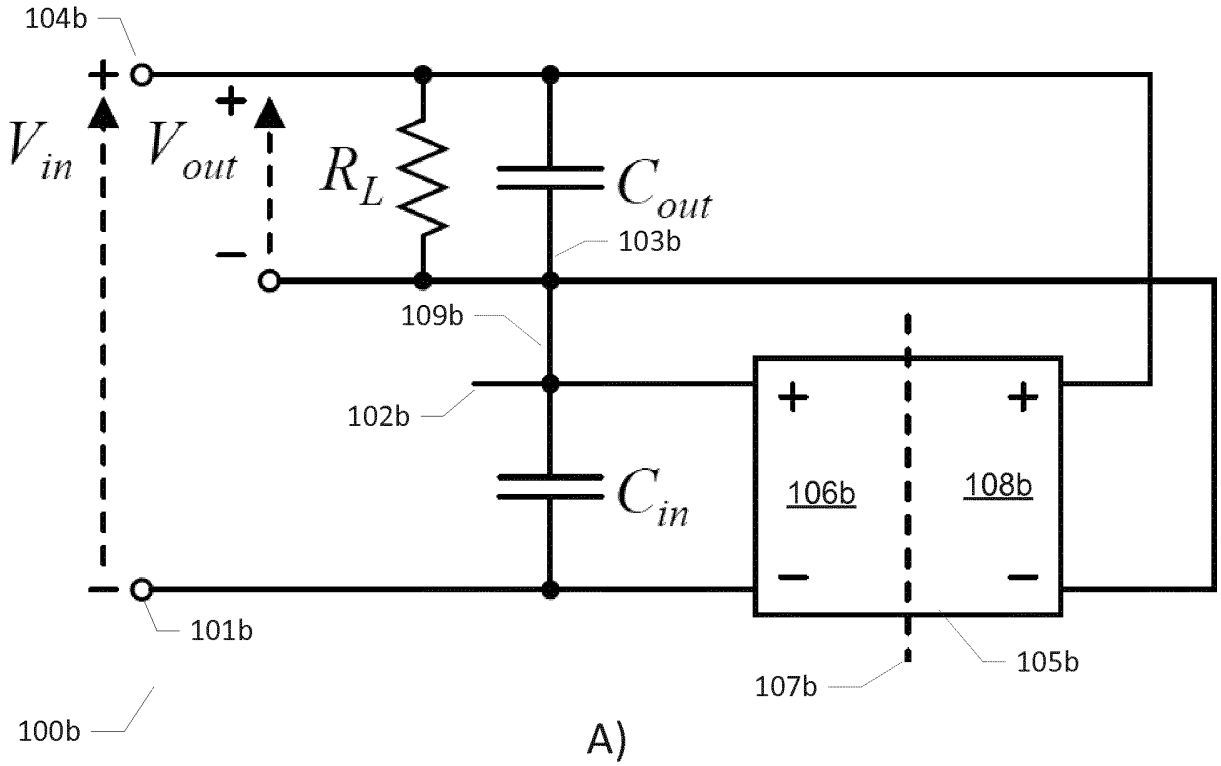
i) in the second case, electrically connecting an input voltage source between the positive input terminal of the primary side circuit and the negative output terminal of the secondary side circuit.

16. A method of converting an isolated DC-DC power converter according to claim 14 or 15, comprising further steps of:
j) inserting a rectifying element in the electrical short-circuit connection,
k) inserting a mode selecting semiconductor switch, in the first case, between the positive input terminal and the first positive electrode of the output capacitor and in second case between the negative input terminal and the second negative electrode of the output capacitor.

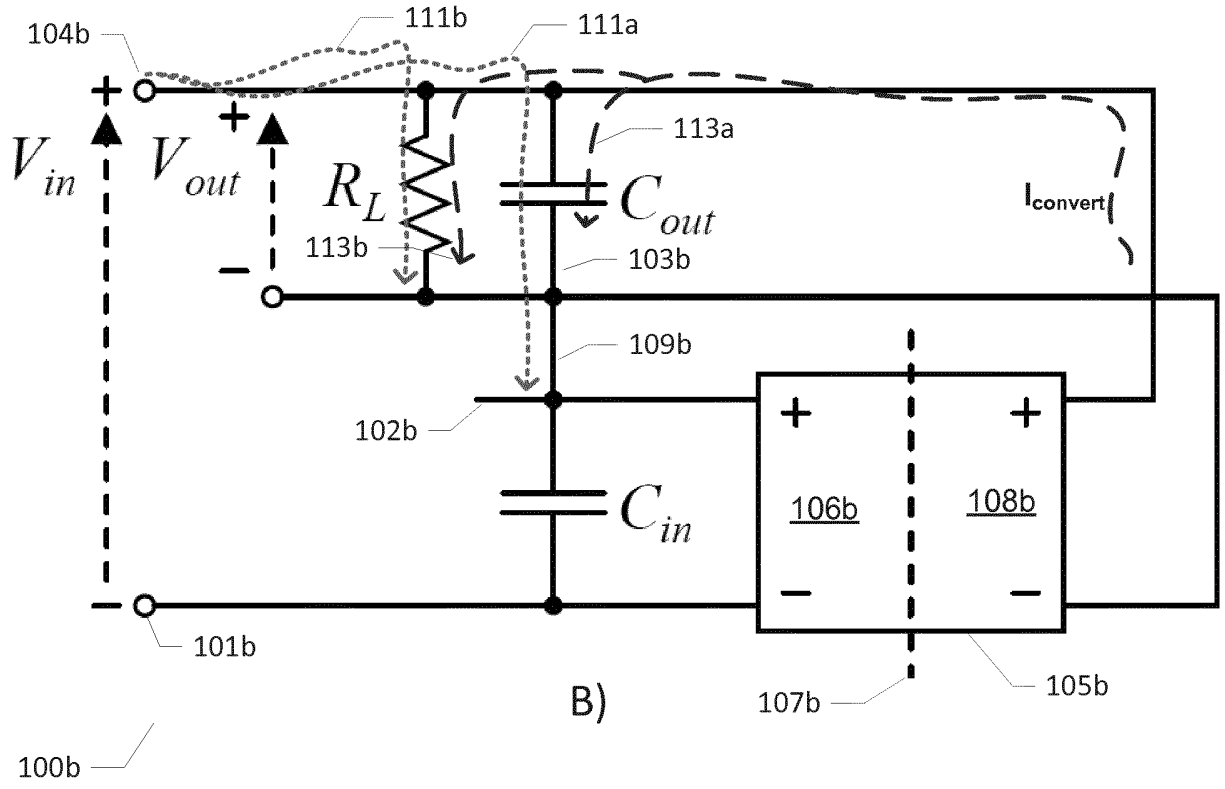
17. A step-down DC-DC power converter assembly comprising:
a resonant step-down DC-DC power converter according any of claims 1-13,
a printed circuit board having at least the resonant network mounted thereon,
a pair of magnetically coupled inductors comprising a first inductor electrically connected to the primary side circuit and a second inductor electrically connected to the secondary side circuit;
wherein the first and second inductors are formed by first and second electrical trace patterns, respectively, of the printed circuit board.

18. A LED light assembly comprising:
a resonant step-down DC-DC power converter according any of claims 1-13 mounted on a printed circuit board of the assembly,
an AC mains voltage input connected to an input of a mains rectifier,
an output of the mains rectifier connected, in the first case, between the first positive electrode of the output capacitor and the negative input terminal or connected, in the second case, between the negative input terminal and the negative electrode of the output capacitor to supply a rectified mains voltage to the resonant step-down DC-DC power converter in both cases.

19. A LED lamp comprising a LED light assembly according to claim 18.


104b
V_{in}
V_{out}
R_L
C_{out}
103b
109b
102b
C_{in}
106b
108b
101b
107b
105b
100b

A)


104b
111b
111a
V_{in}
V_{out}
R_L
113a
C_{out}
$I_{convert}$
113b
103b
109b
102b
C_{in}
106b
108b
101b
107b
105b
100b

B)

FIGS. 1A), 1B)

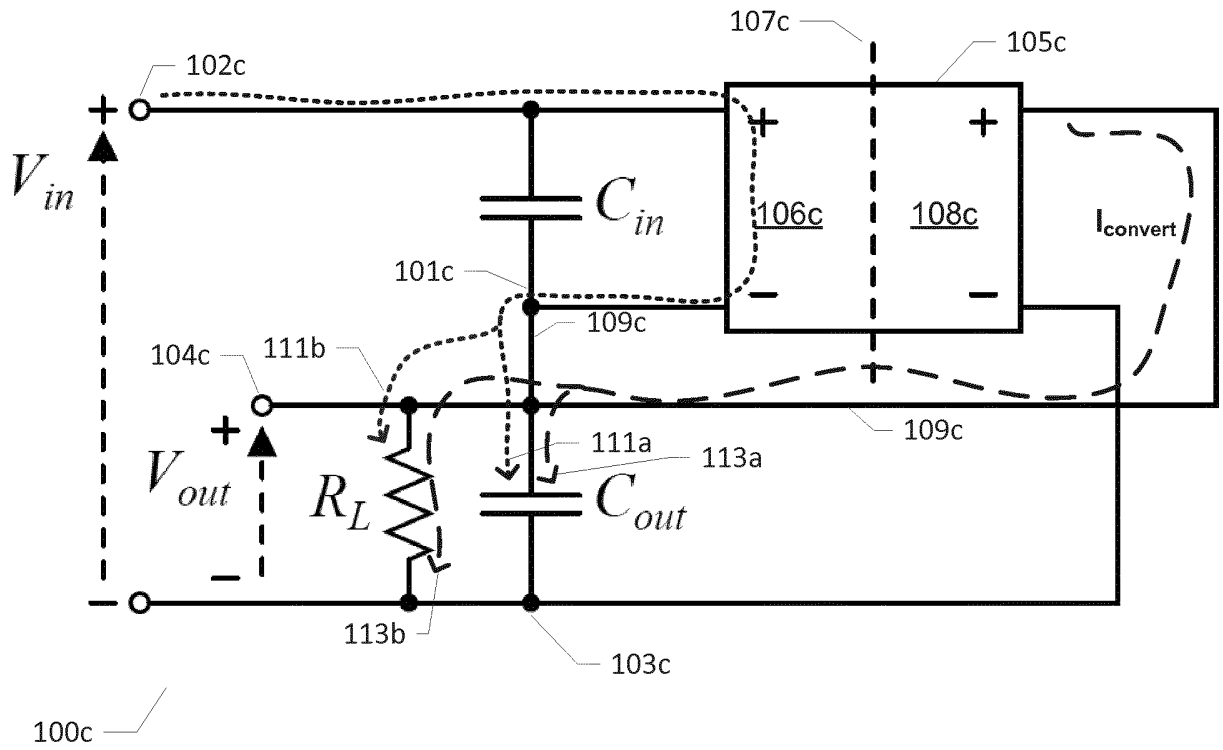
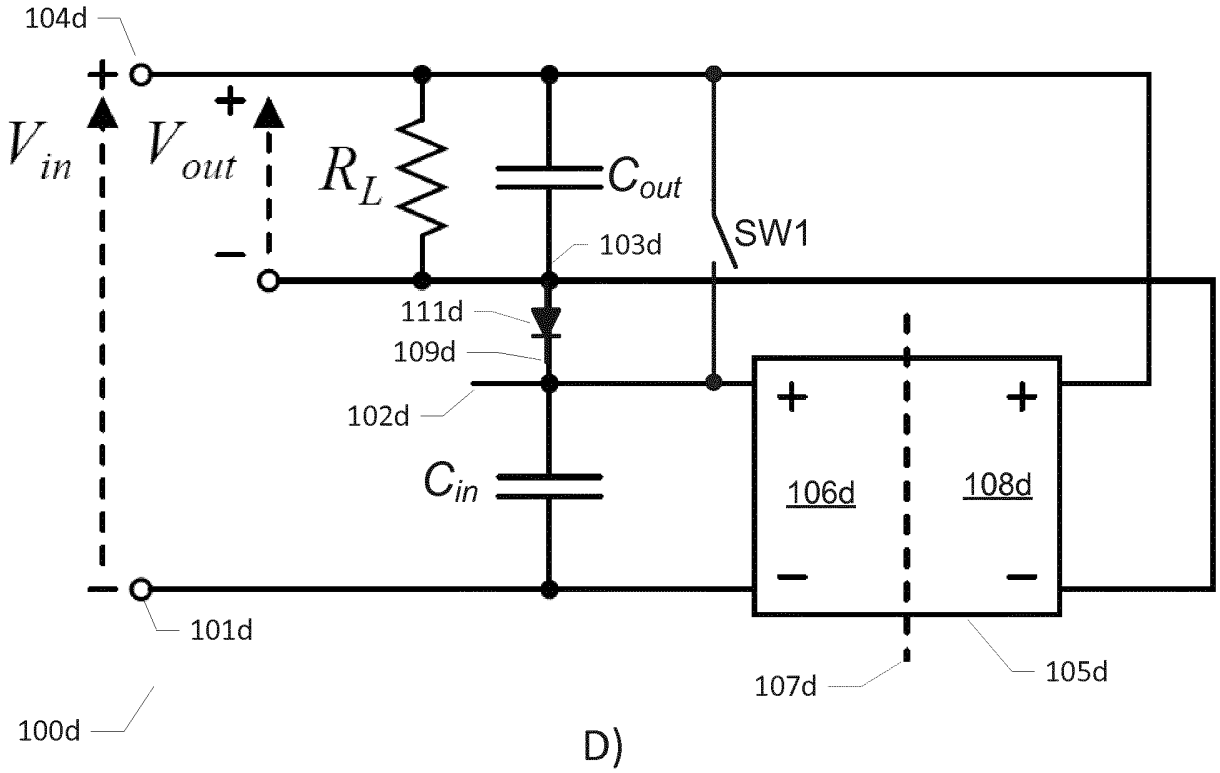
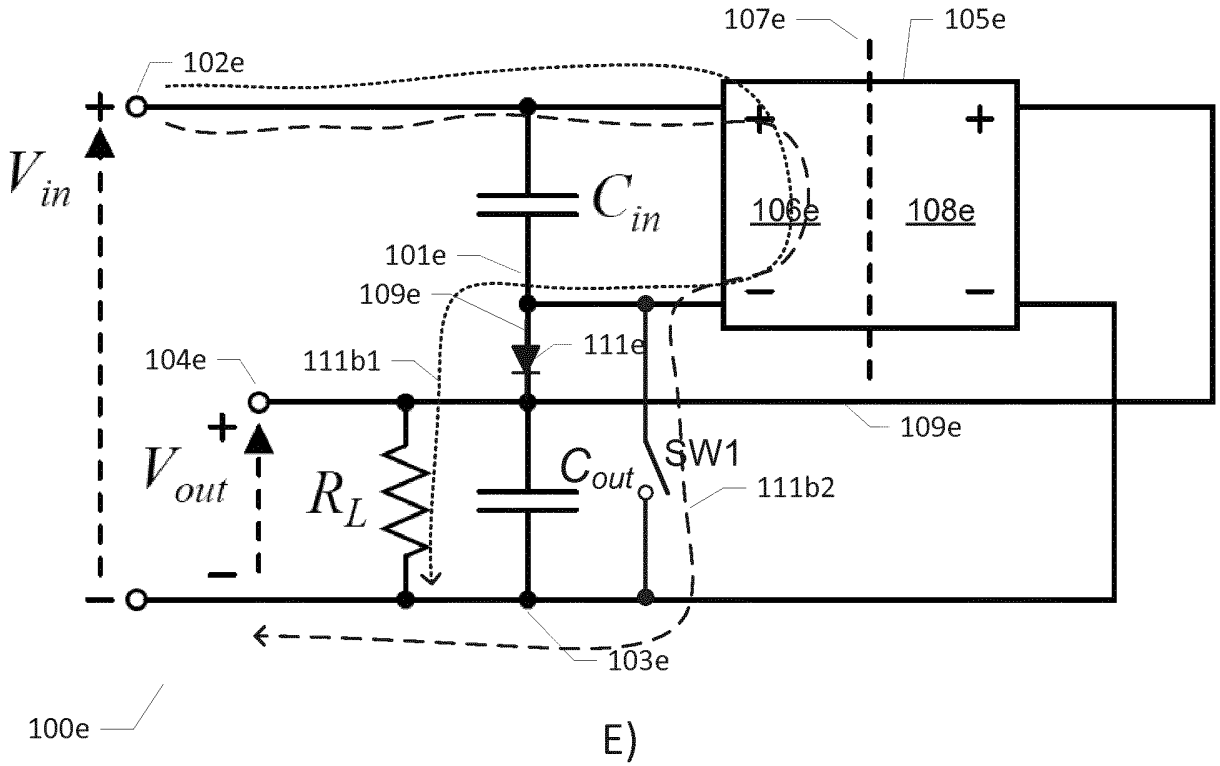

107c
105c
102c
V_{in}
C_{in}
106c
108c
$I_{convert}$
101c
109c
104c
111b
109c
111a
113a
V_{out}
R_L
C_{out}
113b
103c
100c

FIG. 1C)

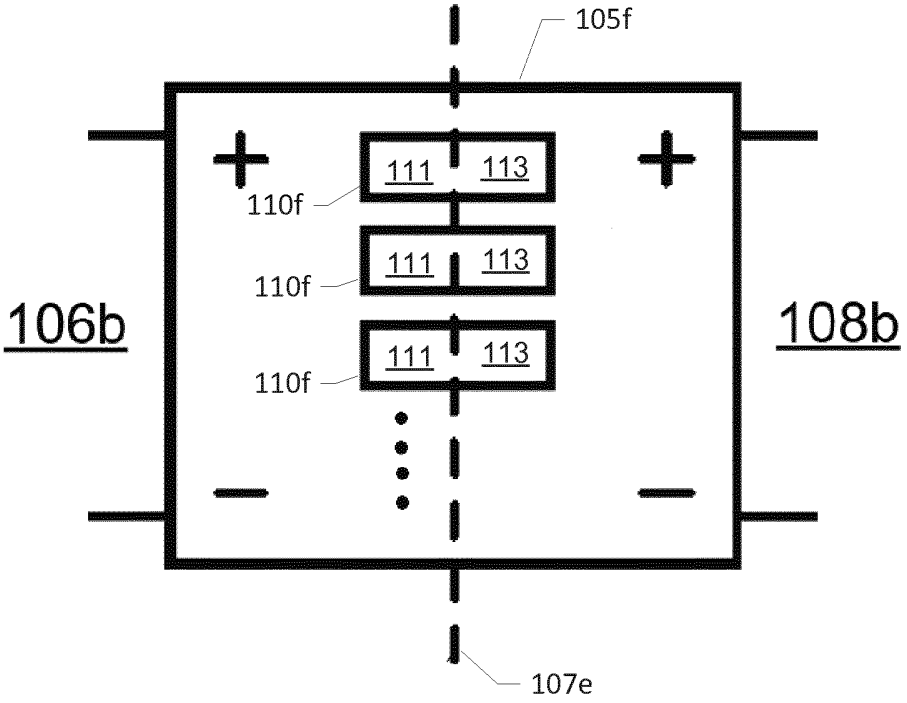

104d
V_{in}
V_{out}
R_L
C_{out}
SW1
103d
111d
109d
102d
C_{in}
106d
108d
101d
107d
105d
100d

D)

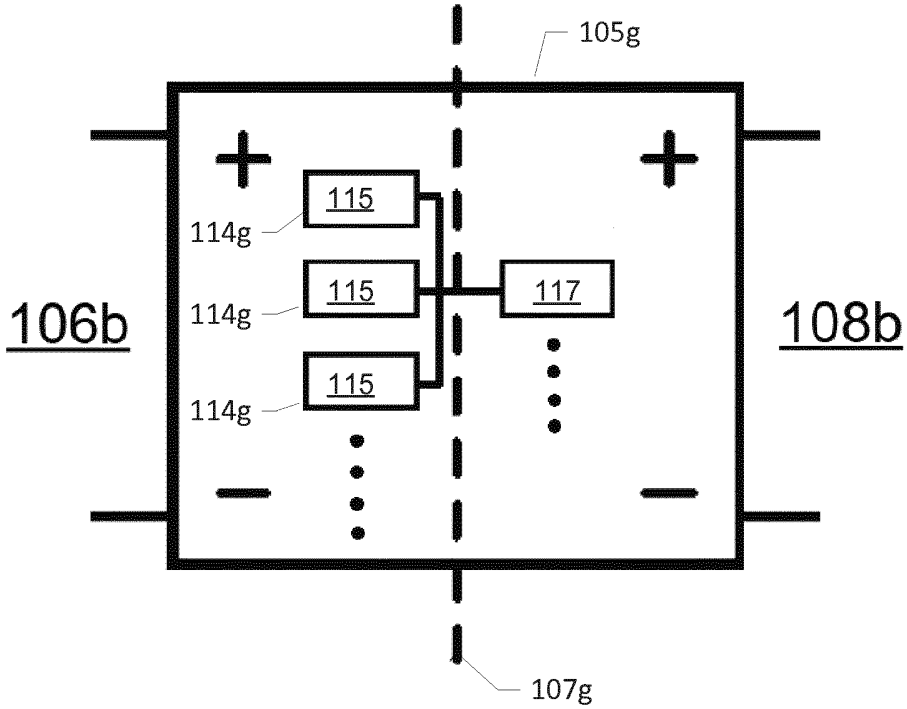

107e
105e
102e
V_{in}
C_{in}
106e
108e
101e
109e
111e
104e
111b1
109e
V_{out}
R_L
C_{out}
SW1
111b2
103e
100e

E)

FIGS. 1D)-1E)

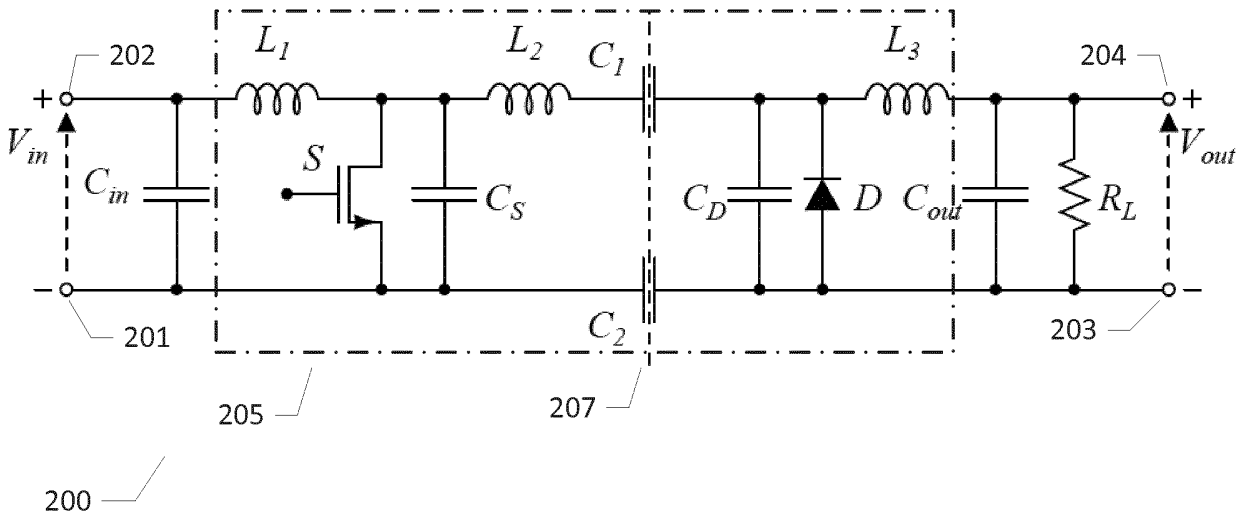

105f
111
113
110f
111
113
110f
111
113
110f
106b
108b
107e

F)

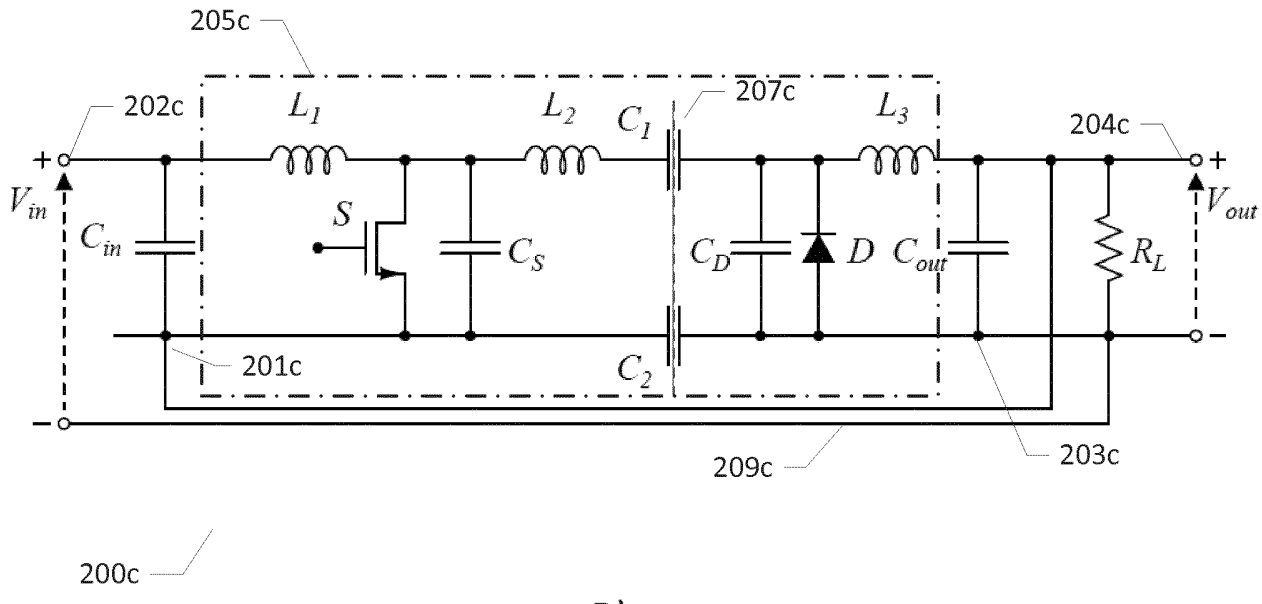

105g
115
114g
115
117
114g
115
114g
106b
108b
107g

G)

FIGS. 1F)-1G)

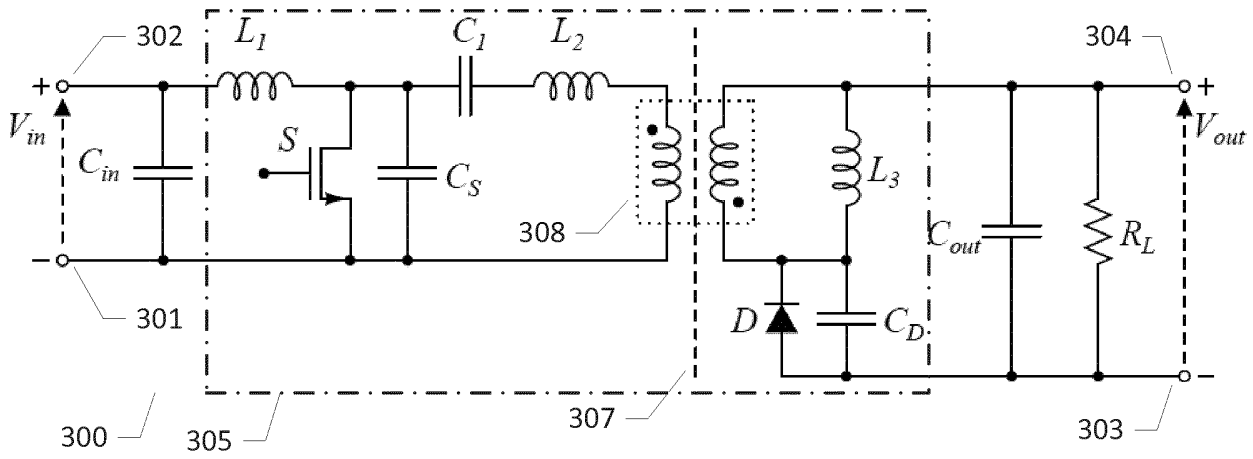

202
L_1
L_2
C_1
L_3
204
V_{in}
C_{in}
S
C_S
C_D
D
C_{out}
R_L
V_{out}
201
C_2
203
205
207
200

A)

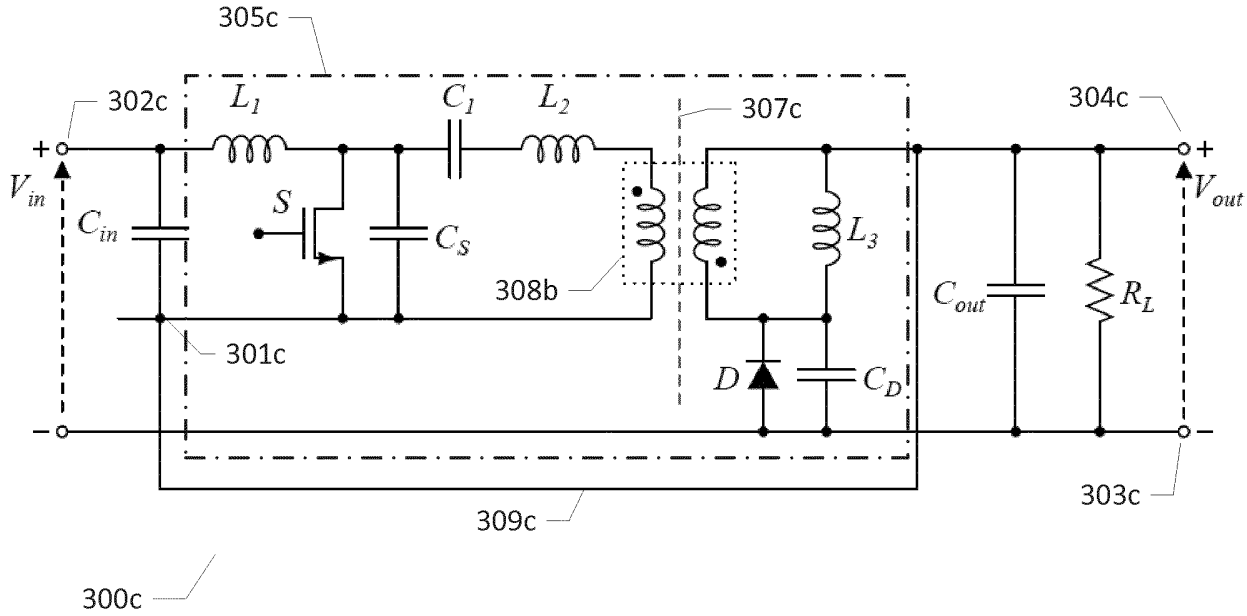

205c
202c
L_1
L_2
C_1
207c
L_3
204c
V_{in}
C_{in}
S
C_S
C_D
D
C_{out}
R_L
V_{out}
201c
C_2
209c
203c
200c

B)

FIGS. 2A), 2B)

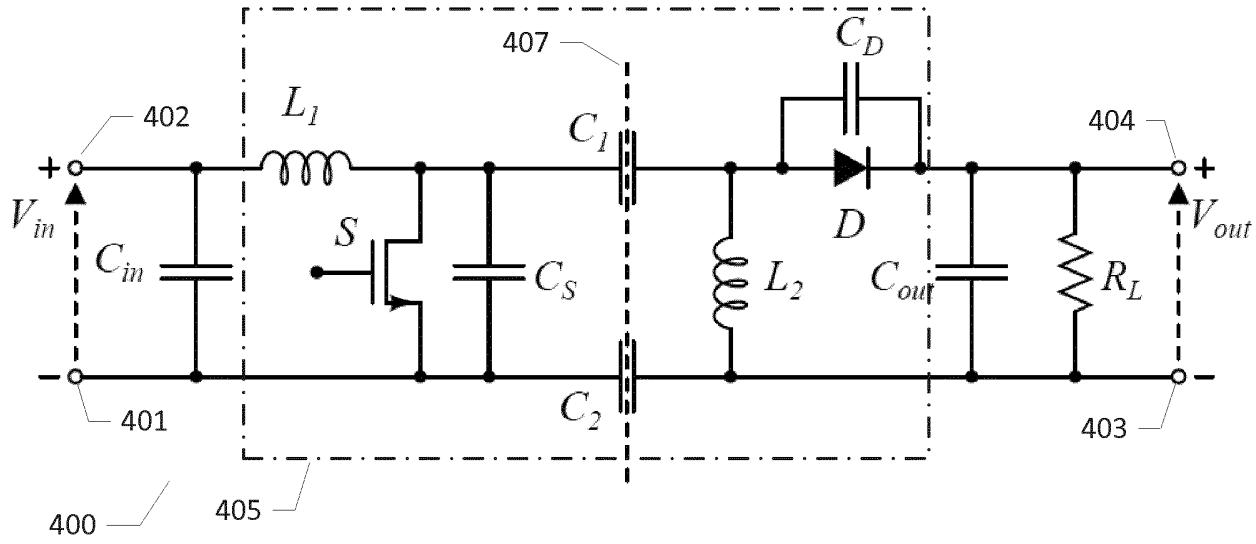

302
304
L_1
C_1
L_2
V_{in}
C_{in}
S
C_S
308
L_3
C_{out}
R_L
V_{out}
301
D
C_D
300
305
307
303

A)

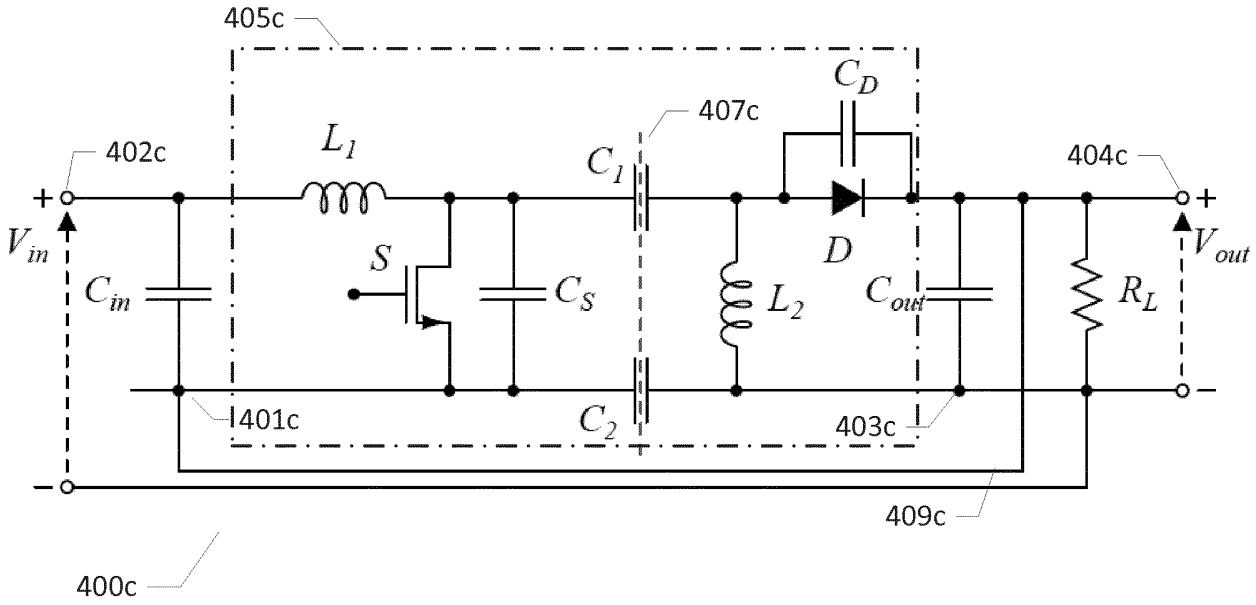

305c
302c
L_1
C_1
L_2
307c
304c
V_{in}
C_{in}
S
C_S
308b
L_3
C_{out}
R_L
V_{out}
301c
D
C_D
309c
303c
300c

B)

FIGS. 3A), 3B)


407
C_D
402
L_1
C_1
404
V_{in}
S
D
V_{out}
C_{in}
C_S
L_2
C_{out}
R_L
401
C_2
403
400
405

A)


405c
C_D
407c
402c
L_1
C_1
404c
V_{in}
S
D
V_{out}
C_{in}
C_S
L_2
C_{out}
R_L
401c
C_2
403c
409c
400c

B)

FIGS. 4A), 4B)

A.10 **M. Madsen, J. A. Pedersen, A. Knott, M. A.E. Andersen:**
***"Self-Oscillating Resonant Gate Drive for Resonant Inverters and Rectifiers Composed Solely of Passive Components"*,**
IEEE Applied Power Electronics Conference and Exposition, Fort Worth, TX, March 2014. Conference Proceedings p2029-2035.

Self-Oscillating Resonant Gate Drive for Resonant Inverters and Rectifiers Composed Solely of Passive Components

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***Abstract*— This paper presents a new self-oscillating resonant gate drive composed solely of passive components. The gate drive can be used in various resonant converters and inverters and can be used for both low and high side gate drive. The paper presents examples of how higher order harmonics can be used to improve the performance of the gate drive and how the gate drive can be implemented in a class E inverter, a class DE inverter and in class E inverter with a synchronous class E rectifier. The paper shows practical implementations of all the proposed inverters and converters operating in the Very High Frequency (VHF) range, all showing good results with peak efficiency up to 82% and output regulation from 70% to full load without bursting.**

I. Introduction

In the early 70s the constant strive for small, cheap and efficient power supplies lead to the development of Switch-Mode Power Supplies (SMPS) [1]. As the size of modern power supplies are mainly governed by the passive energy storing elements, which scales inversely with the switching frequency, this strive has lead to constantly increasing switching frequencies ever since. Commercially available converters today switch at frequencies up to several megahertz and can have efficiencies of more than 95% (e.g. [2]).

The reason not to increase the switching frequency further and thereby reaching even higher power densities is the switching losses. For the last two decades (since 1988 [3]) research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc/dc converters in order to avoid switching losses. With this type of converters SMPSs with switching frequencies in the Very High Frequency range (VHF, 30-300MHz) have been designed with efficiencies up to approx. 90%, [4], [5].

Several of the benefits and challenges of the increased switching frequency are described in [6], [7]. One of the big challenges is to drive the MOSFET without too high gating losses and so far resonant gate drives have shown to be the best solution for this [8], [9]. Control of these converters is also a challenge due to their resonant behavior and burst mode control has been used to overcome this challenge [10], [11], but it introduces spectral components at the bursting frequency.

The compact, low cost converters that can be designed with these resonant converters are very well suited for LED lighting. Price, efficiency and reliability are key parameters in this market and with the presented gate drive the price can be reduced to a minimum without compromising the reliability or efficiency.

In section II of this paper a new type of resonant gate drive and several ways of designing it will be shown. Section III shows how the gate drive can be implemented in a complete circuit, both as low and high side gate drivers and used for synchronous rectification and bidirectional power conversion. Section IV shows results from various prototypes utilizing this gate drive and finally section V concludes the paper.

II. Self-Oscillating Gate Drive

For a converter switching in the VHF range, hard gating leads to gating losses which are unacceptably high, at least for the semiconductors available today and for low to medium power levels [12], [13]. Several researchers have therefore used resonant gating to reduce the gating losses and drive the gate in an efficient way [14], [15]. All of these circuits need either a transformer, switching semiconductor, adjustable passives and/or feedback from other nodes in the circuit [16], [17].

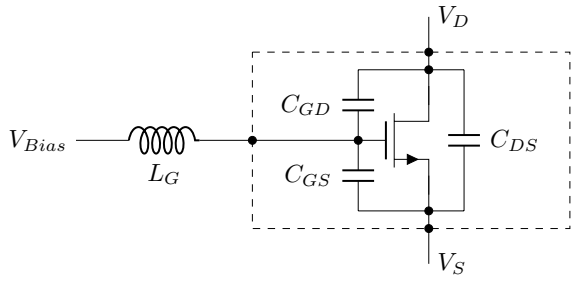


Fig. 1. Schematic of the basic self-oscillating gate drive. The gate resistance and the body diode has been left out for simplicity.

All these things adds to both price, size and complexity of the complete design.

This paper presents a new resonant gate drive solely constituted by passives around the main semiconductor. This leads to a robust and very simple and low cost gate drive.

The simplest implementation of the gate drive is shown in Fig. 1, the only thing added is an inductor at the gate of the semiconductor and a dc bias voltage. If the V_D is seen as input and V_G as output, the inductor and the parasitic capacitances composes a high pass filter with a capacitive load.

If this high pass filter is designed to have a gain, $G = V_{GS,pp}/V_{DS,pp}$, and have a phase shift close to $180\,^\circ$ at the resonance frequency of the power stage, it will create a sine wave at the gate with a peak to peak voltage swing of $V_{GS,pp}$ and a DC offset equal to V_{Bias}.

This dc offset can be used to control the switching frequency and the duty cycle of the power stage and thereby to regulate the output power. In some situations the parasitic capacitances of the MOSFET will lead to too high or too low gain at the desired frequency and additional capacitors, C_{GDext} and C_{GSext}, can be added to adjust this gain.

In order to improve the turn on speed of the MOSFET, and thereby lower the drain to source resistance, higher order harmonics can be added to the fundamental sine wave leading to a more trapezoidal gate signal. This can be achieved by adding small LC circuits between the gate and drain or source of the MOSFET (see Fig. 2). LC circuits connected to drain will cause the higher harmonics to be in phase with V_{DS} and LCs circuit connected to the source will cause the harmonics to be out of phase with V_{DS} (see Fig. 3).

The number of harmonics to include in a given design will depend on several parameters as price, complexity, efficiency etc. Adding higher order harmonics will in general increase the performance of the converter, but it is important to consider which harmonics to include and the magnitude of those harmonics compared to the fundamental. Fig. 4 shows the fundamental and the 3rd and 5th harmonics in and out of phase with the drain signal. It is clear that it is desirable to have the fundamental out of phase with the drain signal, but for the 3rd and 5th harmonic it depends on the duty cycle and the current waveform. From the figure it can be seen that it is desirable to have the 3rd harmonic out of phase for a duty cycle of 50%, but for a duty cycle of 25% it has to be in phase and will only add to the center part of the conducting period where the current usually is the smallest [18], [19]. The gate signals that can be achieved by adding harmonics are shown in Fig. 5.

III. Use in Resonant Circuits

As the resonant gate drive is only relying on the resonance of the power stage and is floating between the drain and source of the MOSFET, it can be used in all resonant circuits. It can for instance be used in the class E inverter [20], [21], a class EF_2 (ϕ_2) inverter [22], [23], a resonant SEPIC [24], [25], a resonant boost converter [26], [27] or a class DE inverter (including high side gate drive) [28], [29], but it can also

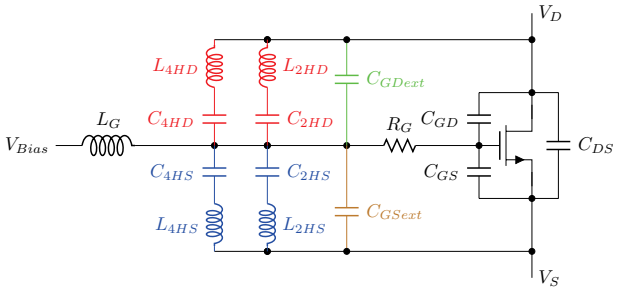


Fig. 2. Schematic of the self-oscillating gate drive with the 2nd and 4th harmonic to source and drain.

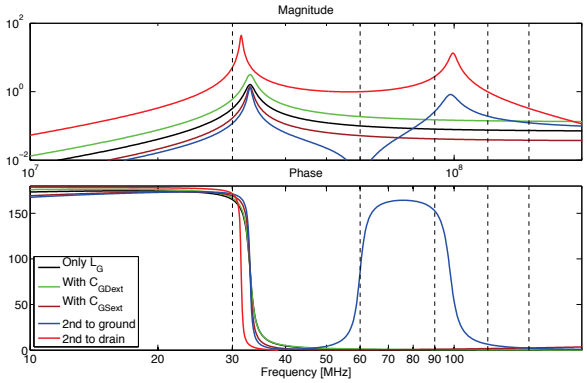


Fig. 3. Examples of transfer functions from drain to source for different implementations of the resonant gate drive.

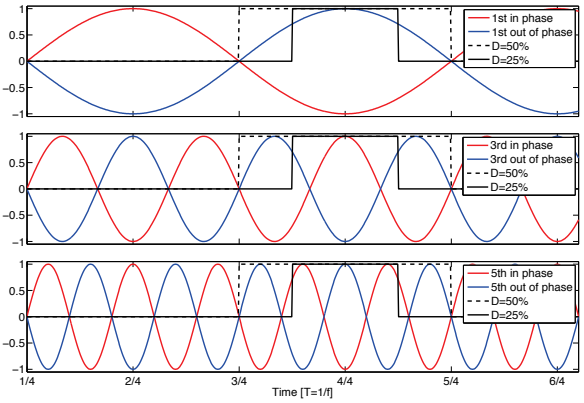


Fig. 4. The 1st, 3rd and 5th harmonics in and out of phase with the drain signal.

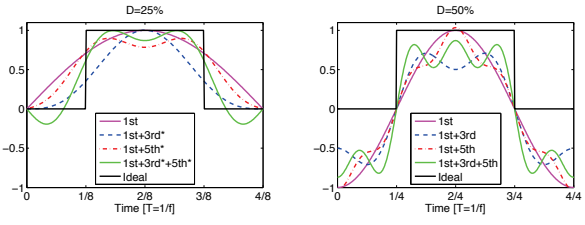


Fig. 5. Gate signals with higher order harmonics for 25% and 50% duty cycle (*=signal in phase with V_{DS}).

be used for synchronous rectification and bidirectional power flow.

A. In a class E inverter

The simple version of the gate drive implemented in a class E inverter is shown in Fig. 6. As the gate drive relies on the resonance of the inverter the switching frequency will automatically adjust for any tolerances in the passives, L_{IN}, L_R and C_R. Furthermore the dependency on the resonance of the power stage gives and inherent open load protection as an open load situation will remove the resonance of the circuit.

When designing a class E inverter with the proposed gate drive, the design procedure will be first to design the power stage according to the specifications for the inverter, then select a proper MOSFET and finally design the gate drive for the selected MOSFET. An inverter with the specifications in table I will be designed in the following to give an example.

TABLE I
DESIGN SPECIFICATION FOR THE CLASS E INVERTER

f_S	V_{IN}	P_{OUT}	R_L
50 MHz	45 V	5 W	25 Ω

The first step is to design the power stage and this can be done as described in [8]. The drain source voltage of the MOSFET is assumed to be a half wave rectified sine wave, hence the peak voltage is:

$$V_{IN} = \int V_{DS} = V_{DS,peak}\frac{2\cdot(1-D)}{\pi}$$
$$\Updownarrow$$
$$V_{DS,peak} = V_{IN}\frac{\pi}{2\cdot(1-D)} \quad (1)$$

The rms value of a half wave rectified sine wave is:

$$V_{DS,rms} = V_{DS,peak}\sqrt{\frac{D}{2}} \quad (2)$$

And the rms value of the output voltage is:

$$V_{OUT,rms} = \sqrt{P_{OUT}\cdot R_L} \quad (3)$$

According to [10] the reactance of the resonance circuit can now be determined by:

$$X_{RC} = R_L\cdot\sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}}\right)^2 - 1} \quad (4)$$

By combining equation 1, 2, 3, and 4, an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained:

$$X_{RC} = R_L\cdot\sqrt{\frac{V_{IN}^2\cdot\pi^2\cdot D}{2\cdot(2\cdot D-2)^2\cdot P_{OUT}\cdot R_L} - 1} \quad (5)$$

From equation 1 it is found that a duty cycle of 45% will give a peak voltage of 128 V, leaving approximately 20% headroom if a 150 V MOSFET is used. Substituting this and the values from table I into equation 5 gives a reactance of 134

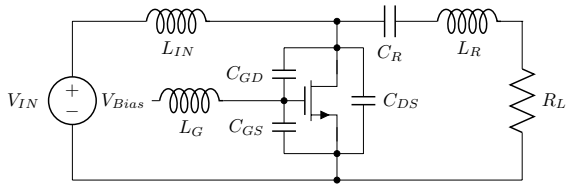


Fig. 6. Schematic of a class E inverter with self oscillating gate drive.

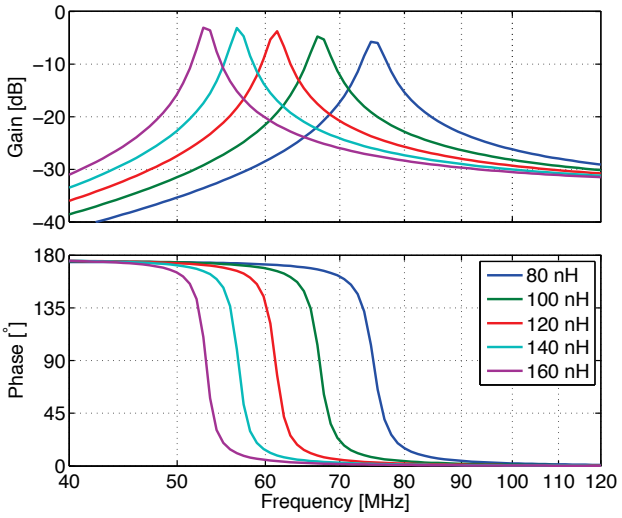


Fig. 7. Bodeplot of the transferfunction from drain to source for different gate inductors.

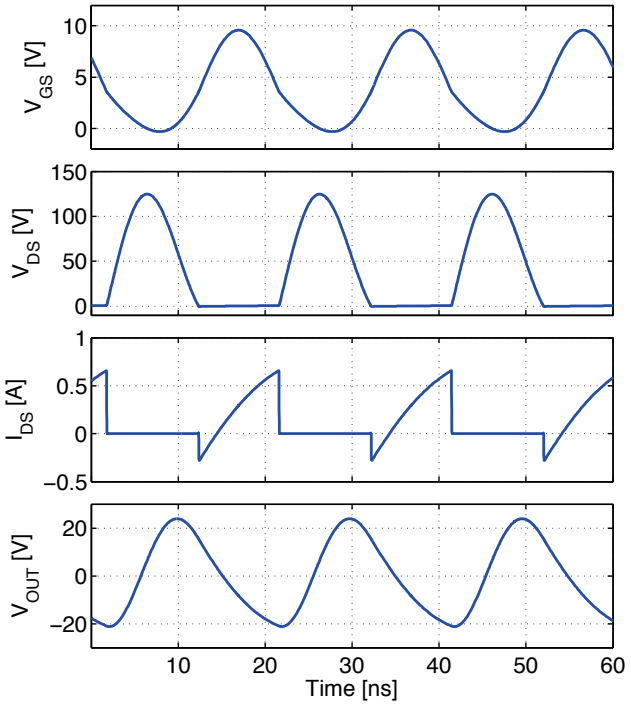


Fig. 8. Simulated class E inverter waveforms with the simple resonant gate drive.

Ω. If a capacitor of 100 pF is used, the value of the inductor becomes 528 nH.

When designing low power inverters switching at VHF it is important to select a MOSFET with low C_{OSS} [8]. For this reason Fairchilds FDT86256 is selected and the values in table II are extracted from the datasheet.

TABLE II
PARASITIC COMPONENTS OF FAIRCHILDS MOSFET FDT86256.
PARASITIC CAPACITANCES TAKEN FOR $V_{DS} = V_{IN}$.

C_{DS}	C_{GS}	C_{GD}	R_{ON}	R_G
15.3 pF	55 pF	1.2 pF	1 Ω	1.3 Ω

The effective output capacitance is $C_{DS,eff} = \frac{C_{DS}}{1-D} = 30$ pF, hence the total inductance of the resonance circuit and the input inductor should be:

$$L_{total} = \frac{1}{\omega_R^2 \cdot C_{S,eff}}$$

Where ω_R is given by:

$$\omega_R = \frac{\omega_S}{2 \cdot (1-D)}$$

Knowing the values of X_{RC}, the input inductance can be calculated according to:

$$L_{total} = \frac{1}{\frac{1}{L_{IN}} + \frac{\omega_R}{X_{RC}}}$$
$$\Updownarrow$$
$$L_{IN} = \frac{1}{\frac{1}{L_{total}} - \frac{\omega_R}{X_{RC}}} = 1.62\ \mu\text{H}$$

The values of all the components in the power stages have now been calculated and the only thing remaining is the gate inductor. The gate signal should have an amplitude of 10 V_{PP} and a phase shift as close to 180 ° as possible. The transferfunction from drain to source for different gate inductors is shown in Fig. 7.

From the plot it can be seen that the phase shift is around 175 ° for all the values of L_G at 40 MHz, but starts to decrease for the two largest inductors around the switching frequency. As the peak to peak voltage across the drain and source of the MOSFET is 128 V, a gain of $20 \cdot log(10V/128V)$ = -22 dB is needed to get a gate signal with an amplitude of 10 V_{PP}. This is almost exactly what is achieved with the 140 nH inductor and as the phase shift is still 170 ° at the switching frequency this value is chosen for this design. Simulated waveforms of the designed inverter can be seen in Fig. 8.

The class E inverter (as most resonant circuits) behaves as a voltage controlled current source in open-loop situations; hence the output power increases with the input voltage. As the amplitude of the gate signal is a fixed ratio of the input voltage, a change in input voltage will lead to a change in amplitude of the gate signal. Hence the gate signal will be small at low input voltages, giving low gating losses at low power levels, and be large at high power, levels leading to lower conduction losses in the MOSFET.

B. Used for synchronous rectification in a class E rectifier

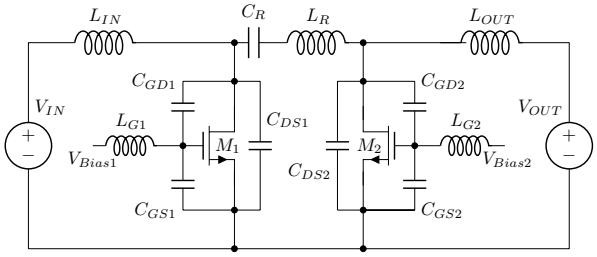


Fig. 9. Schematic of a class E dc/dc converter with synchronous rectification.

The self oscillating gate drive is very well suited for synchronous rectification as it doesn't require a control signal to control the phase between the two gate signals. The two gate signals will automaticly oscillate out of phase with the drain-source voltage of the MOSFET they are controling, hence the gate drive on the inverters side will act as a master drive and the rectifier drive act as a slave drive following the frequency set by the master drive. This principle automatically takes component tolerances and temperature variations of critical design parameters into account. If used in an isolated converter this will further more benefit from not having a control signal and hence no need for communication across the isolation barier. Fig. 8 shows how a dc/dc converter with synchronous rectification can be made with this gate drive. As it can be seen the converter is completely symmetric across the resonant tank, C_R and L_R, hence operation in both directions is possible allowing for bidirectional power flow.

C. Used for high side gate drive in a class DE inverter

An implementation of the self-oscillating resonant gate drive in a half bridge is shown in Fig. 7. Here the two MOSFETs have equally sized inductors at the gates, the only difference is that the other node of L_{G1} is connected to V_{bias} through L_H and to the switch node through C_{G1}. In this way the voltage at this node will follow the switch node but have a dc offset set by V_{Bias1}. As the phase of gate signals of the MOSFETs are directly coupled to drain source voltages, which are 180 °

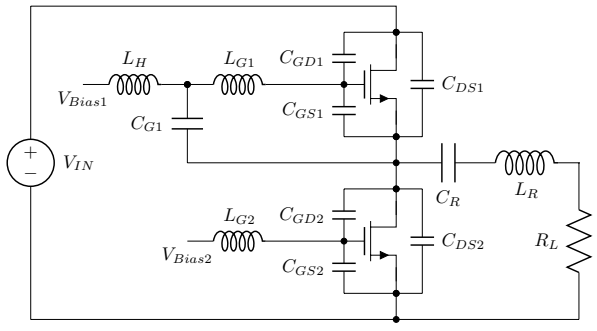


Fig. 10. Schematic of the class DE inverter with self oscillating gate drive.

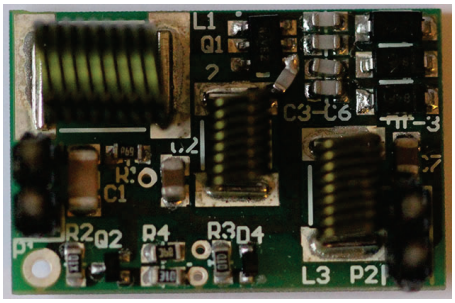


Fig. 11. Picture of a SEPIC converter with the simple version of the gate drive.

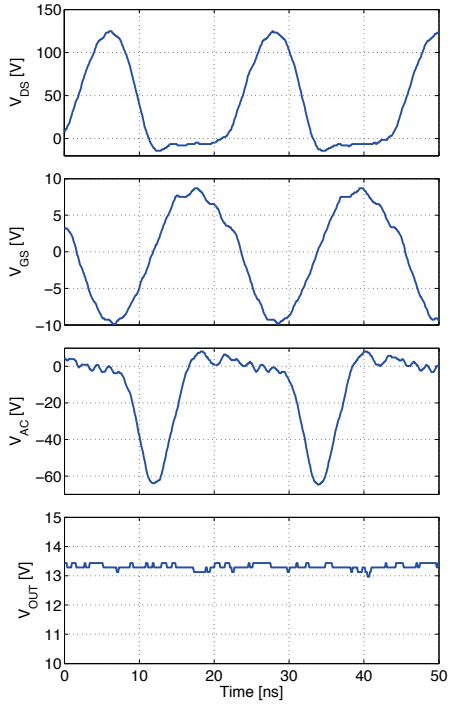


Fig. 12. Measured waveforms of the SEPIC converter with the simple gate drive.

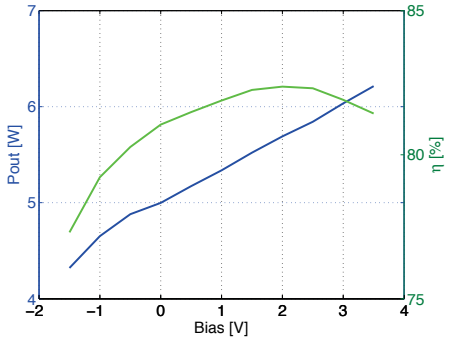
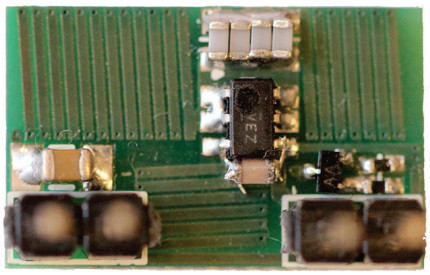
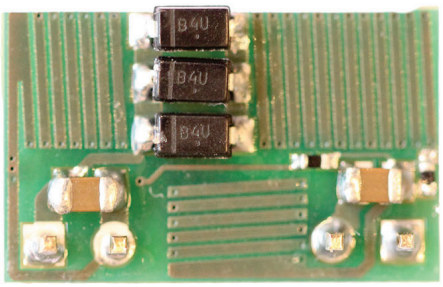


Fig. 13. Measured efficiency and output power for varying bias voltages.



(a) Top



(b) Bottom

Fig. 14. A SEPIC converter with the gate inductor embedded in the PCB.

shifted, the gate signals will automatically be phase shifted and shoot through is avoided.

The simple version of the gate drive has been used for simplicity, but all the implementations can be used.

IV. Practical Implementations

A resonant SEPIC converter switching at 51MHz showing efficiency of 84% with the simple version of the gate drive has been implemented. A picture of the prototype is shown in Fig. 11 and the measured waveforms are shown in Fig. 12. By varying the bias voltage it is possible to regulate the output power from 4.3 W to 6.2 W. The efficiency is above 80% in the range 5-6.2 W but drops to 77% at the lowest output power. A plot of the power and efficiency for varying bias voltages is shown in Fig. 13.

The three air core inductors takes up around half of the PCB footprint and they are the tallest components. In order to decrease the size further it is hence necessary to use another type of inductors. As the skin depth is very small and the maximum inductance 160 nH embedding the inductors in the PCB becomes a viable solution. A prototype of the same converter with the inductors embedded in the PCB has therefore been made [30] (see Fig. 14). Doing so the efficiency drops 2% but the power density increases approximately 4 times and the price becomes significantly lower.

The converter shown in Fig. 9 has also been implemented showing that the synchronous rectification works even without synchronization of M_1 and M_2 and allows for bidirectional power flow as well. The bidirectional converter is implemented as a class E inverter and a synchronous class E rectifier both using the simple self-oscillating gate drive.

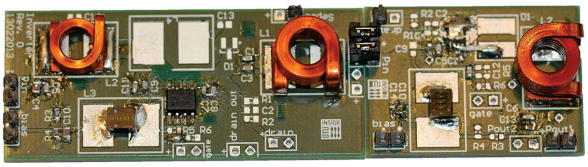


Fig. 15. Picture of a class E inverter and a synchronous class E rectifier both with the simple version of the gate drive.

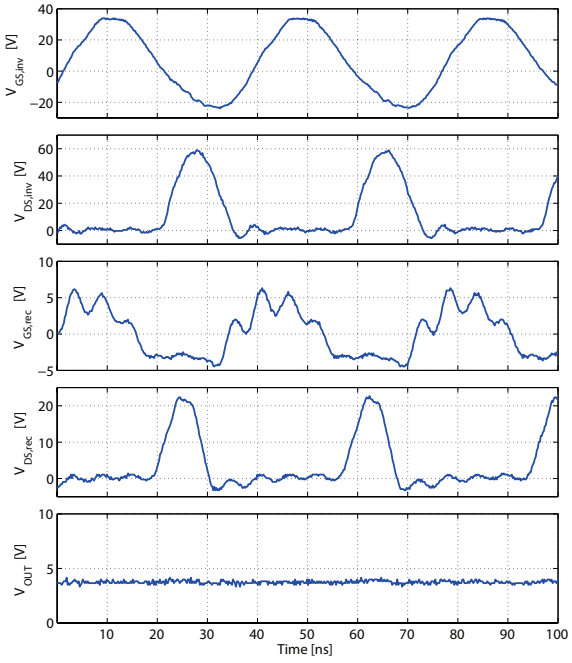


Fig. 16. Measured waveforms of the Class E converter with synchronous rectifier.

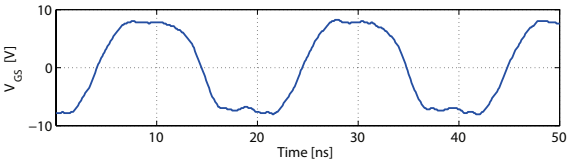


Fig. 17. Measured gate voltage of the SEPIC converter implemented with the gate drive with a 2.harmonic LC circuit connected to ground.

The reason for using a synchronous rectification is to minimize losses in the diode when dealing with low voltages and high currents; it also enables the converter to be used as a bidirectional converter. The converter with the synchronous rectifier is shown in Fig. 15. The converter reaches a maximum efficiency of 67% with the synchronous rectifier compared to 66.5% with a standard rectifier. The waveforms measured on the class E converter are shown in Fig. 16. It is evident that the inverter dictates the switching frequency. The simple gate drive in the rectifier is designed with an 180° phase shift from drain to gate at the switching frequency. This ensures that the rectifiers gate drive follows the same frequency as the inverter.

Since the converter is implemented with a synchronous rectifier it could be used as a bidirectional converter with a load connected to the input of the inverter and a power source connected to the output of the rectifier. The transfer ratio $\frac{V_{in}}{I_{out}}$ was roughly the same in both directions $\frac{14V}{2A} \approx \frac{5V}{730mA} \approx 7$. The efficiency was kept above 50% when driven in reverse direction. The switching frequency was in this case dictated by the rectifier and the inverter just followed. With this self-oscillating gate drive it is possible to implement a small and cheap bi-directional converter using only a few passive components for driving the MOSFETs.

One of the more advance self-oscillating gate dives described earlier with a 2. harmonic LC circuit connected to ground is used with the SEPIC converter shown in Fig. 11. The transfer function is showed in Fig 3 is designed to remove the 2. harmonic and adding a 3. harmonic in phase with the fundamental. To ensure that the two peaks of the gate drives transfer function is placed above the fundamental frequency and the 3. harmonic the value of L_G is reduced and a small value for L_{2HS} is used. The total value of the inductances is reduced compared to the simple gate drive, in this case the total inductance was reduced by 45% which will free up more space when using PCB inductors.

The waveform of the gate voltage are shown in Fig. 17, it is evident that the gate signal generated by the more advance self-oscillating gate drive is more like a square wave than in 12. The peak-peak voltage is however twice of the simple gate drive and these increases the gate losses and in this case resulting in the efficiency reduction of a few % compared to the simple gate drive.

A implementation of a class DE inverter showing the function of the high side gate drive is shown in [31]. This is the first implementation of an off chip high side gate drive for operation in the VHF range.

V. Conclusions

This paper has presented several ways of designing a new self-oscillating resonant gate drive along with several examples of implementations in complete circuits. The presented gate drive is a simple, compact, low cost and reliable solution composed only of passive components. The gate drive is floating between the drain and source of the MOSFET and is directly coupled to the resonance frequency of the power stage. Due to this the gate drive can be used in all resonant circuits, also for high side drive and synchronous rectification. The gate drive offers an inherent open load protection and allows for synchronous rectification in isolated converters without synchronization across the isolation barrier. Finally the gate drive allows for output control without the low frequency ripple seen when utilizing burst mode control.

The paper has shown practical implementations of a low side gate drive, a high side gate drive and synchronous rectification and efficiencies up to 84% has been achieved.

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A.11 **J. A. Pedersen, M. Madsen, A. Knott and M. A.E. Andersen: *"Self-oscillating Galvanic Isolated Bidirectional Very High Frequency DC-DC Converter"*, IEEE Applied Power Electronics Conference and Exposition, Charlotte, NC, March 2015. Conference Proceedings.**

Self-oscillating Galvanic Isolated Bidirectional Very High Frequency DC-DC Converter

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***Abstract*—This paper describes a galvanic isolated bidirectional Very High Frequency (VHF = 30 MHz - 300MHz) Class-E converter. The reason for increasing the switching frequency is to minimize the passive components in the converter. To make the converter topology bidirectional the rectifier has to be synchronous. This increases the complexity of the gate drives, which in this paper is solved by using a self-oscillating gate drive. A bidirectional converter has been implemented and is described in this paper; the converter reaches efficiencies above 80% in forward conduction mode and 73.5% in reverse conduction mode. The designed converter operates at a switching frequency of 35.6 MHz, which is well within the VHF range. The same converter is also implemented with PCB embedded inductors to minimize cost and the physical volume of the total converter.**

I. INTRODUCTION

In traditional Switch Mode Power Supplies (SMPS) small physical size is often a priority. The passive components usually take up most of the space and scale inversely with frequency and therefore increasing the switching frequency reduces the physical size of the overall converter. The switching frequency is typically limited to a few megahertz, this is where the switching losses become dominant as they increase linearly with frequency. Using resonant converters the switching losses can be significantly reduced, these types of converters are used in [1]–[5]. Increasing the switching frequency into the Very High Frequency (VHF = 30 MHz - 300 MHz) reduces the value as well as the physical size of passive components significantly, not just the energy storing components inside the converter also the EMI filter can be greatly reduced [6], [7]. The Class-E DC-DC converter topology, presented in [8] inspired by [9], is made with an inverter and a rectifier that both uses a resonant circuit to enable soft switching. This paper describes how the Class-E topology can be used for bidirectional VHF converters; this topology has two switching devises placed on each side of a resonant tank made with a capacitor in series with an inductor, to make this converter galvanic isolated the resonant capacitor is split into two capacitors where one is placed in series with the resonant inductor and one in the ground return path from the rectifier. Then an input and output filter which also helps to achieve soft switching in the inverter and rectifier. The symmetry around the resonant tank make the topology ideal for bidirectional operation. The schematic of the converter is seen in figure 1. The synchronous Class-E rectifier has been described in [10] and [11], and a bidirectional full-bridge class-E converter is implemented in [12] running at several hundred kilohertz. Bidirectional LLC converter have been used in different setups and shown that resonant converters are very suitable as bidirectional converter [13]–[15]. The bidirectional Class-E converter topology described in this paper could be suitable for many applications were size and price is a key consideration. One application for this converter is a single converter to charge a battery and then deliver the power from the battery to a load when it is not charging. This could be charging a battery from a PV panel during the day and delivering the power to an LED during the night. Another use of such a converter could be voltage sharing of batteries were two batteries need to have the same voltage. In future prospects this type of converter could also be integrated inside a chip, which can have two different transfer ratios depending on which way the chip is placed. This would cut the production cost for such a converter. Since this converter is galvanic isolated it is suitable for auxiliary supplies on the secondary side of an isolated converter. The converter is designed with a self-oscillating gate drive described in [10] that drives the MOSFET both in the inverter and the rectifier. This gate drive has shown great potential for normal VHF converters and in this paper it is used for driving a bidirectional converter.

II. THEORY

The converter is made as a standard Class-E converter in both directions, this is done by calculating the component values of the converter in forward direction, then afterward the reverse direction from the given resonant tank. To enable bidirectional power flow in a Class-E converter the rectifier needs to be implemented with a MOSFET and thereby becoming a synchronous rectifier as shown in figure 1. The use of VHF converters with synchronous rectification is a challenge due to the gate signals timing. The gate signals amplitude and duty cycle needs to be tightly controlled to ensure ZVS on the MOSFET in the rectifier and to keep the gate losses to a minimum. The design for the inverter is inspired from the method used in [16], made for a Class-ϕ_2 converter which is described in [17]. Where the impeadance of the circuit is matched to create a half sine on the drain of the MOSFET at the frequency needed to ensure ZVS in the inverter. The design method is changed to fit a Class-E inverter as described in [10]. This method is not ensuring a perfect sinusoidal current through the resonant tank but only that the ZVS of the MOSFET is achieved.

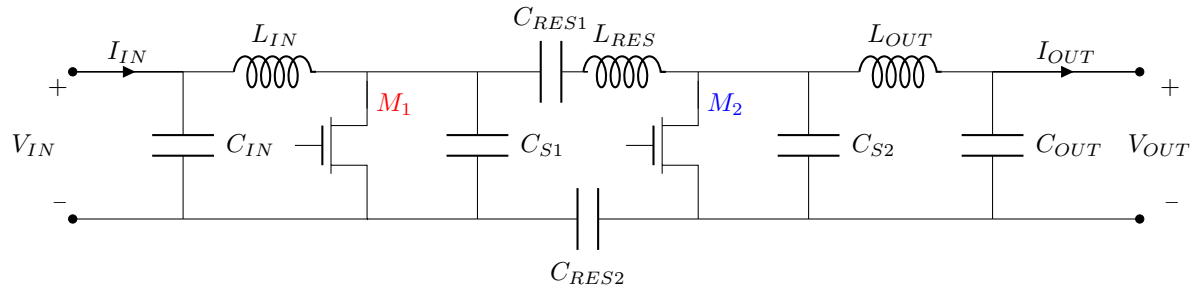


Fig. 1. Schematic of a bidirectional Class-E converter

A. Forward conduction mode

The forward conduction mode is when power is drawn from V_{IN} and delivered to V_{OUT} and the reverse conduction mode is the other way. The first step when designing the power stage is to make the rectifier. For a rectifier with a duty cycle $D = 50\%$, the inductor L_{OUT} and the capacitor C_{S2} is chosen so they resonate at the switching frequency, and the output capacitor C_{OUT} is chosen to be large enough to limit the output ripple. The input impedance of a Class-E rectifier at different duty cycles can be found in [18], for $D = 50\%$ the input impedance of the rectifier is:

$$Z_{IN} = 0.5760 \cdot R_L \tag{1}$$

When the rectifier and its input impedance is found the inverter can be calculated. First the drain source voltage of the MOSFET is assumed to be a half wave rectified sine, hence the peak voltage is:

$$\begin{aligned} V_{IN} = \int V_{DS} = V_{DS,peak} \frac{2 \cdot (1 - D)}{\pi} \\ \Updownarrow \\ V_{DS,peak} = V_{IN} \frac{\pi}{2 \cdot (1 - D)} \end{aligned} \tag{2}$$

The peak voltage is used to find the rms value of a half wave rectified sine:

$$V_{DS,rms} = V_{DS,peak} \sqrt{\frac{D}{2}} \tag{3}$$

The rms value of the output voltage is found from:

$$V_{OUT,rms} = \sqrt{P_{OUT} \cdot Z_{IN}} \tag{4}$$

The needed reactance of the resonance circuit can now be determined by [10]:

$$X_{RC} = Z_{IN} \cdot \sqrt{\left(\frac{V_{DS,rms}}{V_{OUT,rms}} \right)^2 - 1} \tag{5}$$

By combining equation 2, 3, 4, and 5, an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained:

$$X_{RC} = Z_{IN} \cdot \sqrt{\frac{V_{IN}^2 \cdot \pi^2 \cdot D}{2 \cdot (2 \cdot D - 2)^2 \cdot P_{OUT} \cdot Z_{IN}} - 1} \tag{6}$$

The reactance of the resonant tank has to match the calculated reactance for the given design, if the capacitor C_{RES2} is chosen to be much bigger than the C_{RES1} it can be neglected in the calculations, and hence the reactance of the resonant tank is:

$$X_{RC} = 2 \cdot \pi \cdot f_r \cdot L_{RES} - \frac{1}{2 \cdot \pi \cdot f_r \cdot C_{RES1}} \tag{7}$$

Where $f_r = \frac{f_s}{2 \cdot (1 - D)}$ is the frequency of the half wave sine. Last the input inductor is found this helps ensuring soft switching in the inverter, this is found by:

$$L_{IN} = \frac{1}{4 \cdot C_S \cdot f_r^2 \cdot \pi^2 - \frac{2 \cdot \pi \cdot f_r}{X_{RC}}} \tag{8}$$

Where $C_S = \frac{C_{S1}}{1 - D}$ is the effective capacitance of C_{S1}. When the converter is designed in the forward direction the component values is fixed this limits the possibilities of optimizing the circuit in reverse direction. However there is still some degree of freedom such as the choice of load impedance or change of switching frequency.

B. Reverse conduction mode

When designing the bidirectional converter in the reverse conduction mode the first thing is to calculate the resonance of L_{IN} and C_{S1}, this limits the frequencies of the converter in this direction, and if the same frequency is maintained as in forward operation the load options is limited. In this section the switching frequency is set to be the same as in forward direction to simplify the calculations. The values of L_{IN} and C_{S1} determines the duty cycle of the rectifier in reverse conduction mode and this affects the input impedance of the rectifier. When this is found the equations 6, 7 and 8 described in the forward conduction mode can be used to determining the duty cycle of the inverter. Most VHF converter have a resonant gate drive driving the MOSFETs with a sinusoidal current,

when using such a gate drive, the duty cycle can easily be changed by a varying DC offset. By doing this the duty cycle can be changed and there by also changing the output power of the converter.

III. Bidirectional converter

To test the circuit a bidirectional converter has been designed. The converter is operating at low voltages were the benefit of having a synchronous rectifier is highest. This circuit is intended to operate from 14 V to 7 V in the forward conduction mode and from 7 V to 3.5 V in the reverse conduction mode. All specifications are shown in table I. The switching frequency is set just inside the VHF range. The power level is intended for charging of a battery in the forward conduction mode and delivering power from the battery to an LED in the reverse conduction mode. The circuit can either be connected to the charger or the LED.

TABLE I. Design specification for the Class-E converter

Power flow	V_{IN}	V_{OUT}	f_s	P_{OUT}	R_L
Forward	14	7 V	37 MHz	5 W	10 Ω
Reverse	7	3.5 V	37 MHz	1.5 W	10 Ω

A. Gate drive

One of the main reasons to keep the switching frequency constant in both directions is to make the gate drive implementation easier. For the prototypes in this paper the gate drive is implemented with the self-oscillating passive gate drive described in [10]. The benefit of this gate drive is that it is controlled by the drain voltage so when the inverter starts sending power through the resonant tank the voltage across the MOSFET in the rectifier will rise and start the oscillation on the gate. For simplicity the gate drives for the MOSFETs are the same in the inverter and rectifier. the schematic is shown in figure 2.

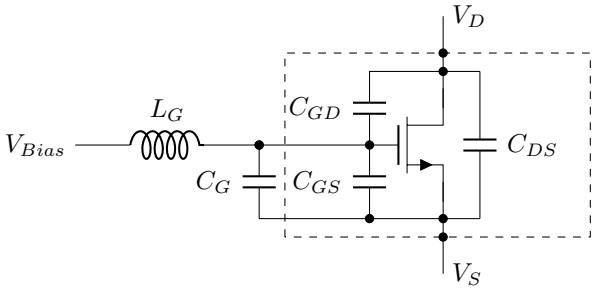


Fig. 2. Schematic of a basic self-oscillating gate drive were L_G and C_G is external components

To be able to simulate the converter the gate drive has to be found. Both MOSFETs (M_1 and M_2) are chosen to be the FDC8601 from Fairchild as they have relatively low parasitic capacitance. Because they are both the same MOSFETs the external components in the gate drive can be the same for simplicity. First the gate drive for the inverter in the forward direction are designed to have gain of -10 dB and a phase shift close to $180°$ from drain to gate. This ensures that the MOSFET is soft switching and that the gate signal is large enough to fully turn on the MOSFET. The gate drive in the rectifier is implemented with the same external components but here the gain of the gate dive are -4 dB as the parasitic capacitances are higher at lower drain-source voltages. The higher gain in the gate drive is beneficial since the drain voltage in the rectifier is smaller.

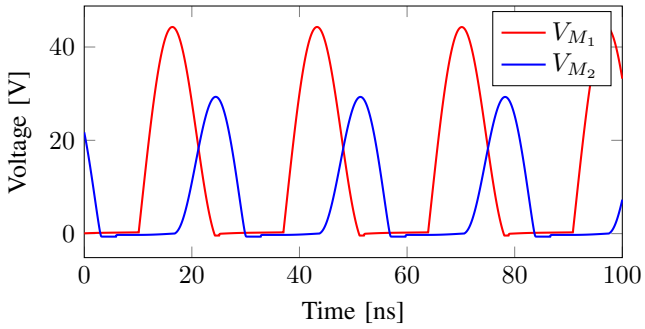


Fig. 3. Waveforms from simulation of the converter in forward conduction mode, V_{M1} and V_{M1} are the voltage across the MOSFETs

B. Simulation

With the gate drive, the converter was simulated in LTspice. The drain voltages of the two MOSFETs in forward conduction mode is shown in figure 3 and for the reverse conduction mode in figure 4. It is evident that the peak voltages are much higher than the in/output voltages, at 50% duty cycle the peak voltage across the MOSFET in a Class-E converter are 3.6 times the in/output for the inverter and rectifier respectively. The body diode is conduction a small period of time before the MOSFET turns on, this can be avoided by increasing the bias voltage seen in figure 2, the simulation are made with the components values stated in table II.

TABLE II. Component values used in the Class-E converter

Component	Value
C_{IN}	100nF
L_{IN}	350nH
C_{S1}	165pF
C_{RES1}	1nF
C_{RES2}	100nF
L_{RES}	110nH
C_{S2}	160pF
L_{OUT}	156nH
C_{OUT}	100nF
L_G	68µH
C_G	40pF

C. Implemented converter

The converter was implemented with discrete inductors from Coilcraft as shown in figure 5. The waveforms measured in the forward conduction mode resembles the simulations as shown in figure 6. The switching frequency of the converter is measured to be 35.6 MHz. This is close the desired 37 MHz, the shift in frequency is reasonable since the gate drive is self-oscillating and is not externally controlled. The converter has been measured in reverse conduction mode and the waveforms

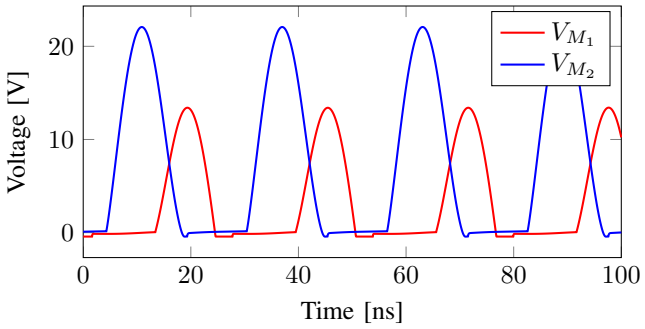


Fig. 4. Waveforms from simulation of the converter in reverse conduction mode

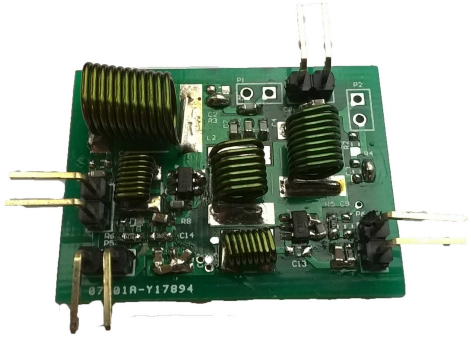


Fig. 5. Prototype with discrete inductors and synchronous rectifier

is shown in figure 7. The voltage across M_1 in reverse direction does not reach as high a voltage level as in the simulation, this could be due to the parasitics of the MOSFET which are more dominant at lower voltages. The efficiency of the converter in both directions is shown in figure 8, the efficiency is 80% for output powers above 1.5 W. In the forward conduction mode and above 70 %. The output power is changing over input voltage as shown in figure 9.

Implementing the magnetics as part of the PCB is widely used in traditional converters as described in [19], [20]. For VHF converters there is limited selection of magnetic materials since most materials does not operate well at these frequencies and therefore air core inductors are used. One form of air core inductors used for VHF converters is the PCB embedded inductors described in [21], [22]. A second identical prototype is made with PCB embedded inductors and compared to the

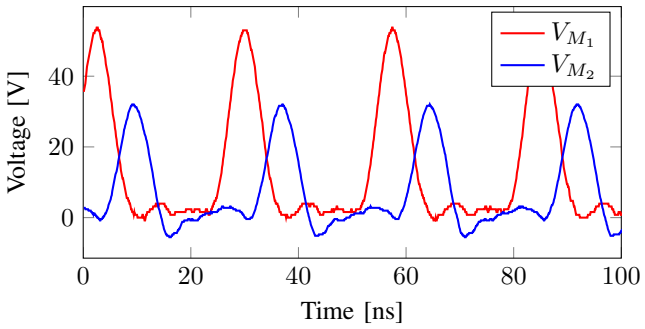


Fig. 6. Measured waveforms of the converter in forward direction

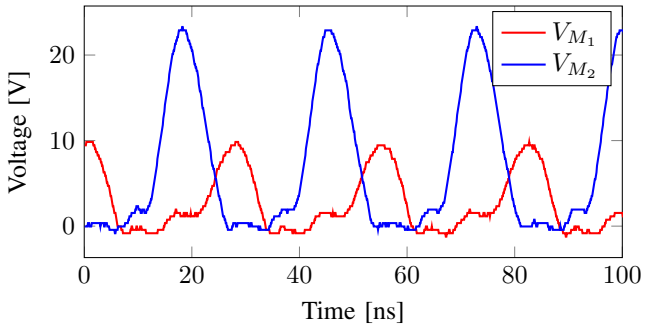


Fig. 7. Measured waveforms of the converter in reverse direction

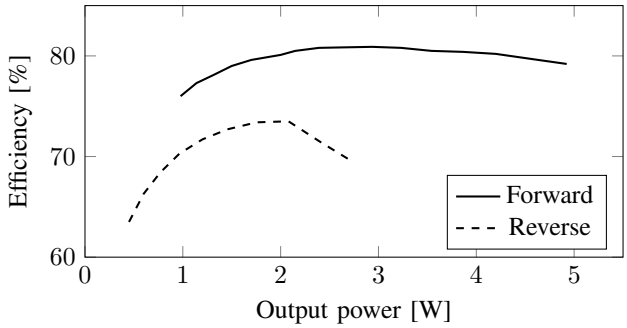


Fig. 8. Measured efficiency vs. output power

first converter. The converter with PCB embedded inductors, is seen in figure 10. It only reach 74% efficiency in the forward conduction mode and 65% in reverse conduction mode. The reason for the lower efficiency is the low Q values for the PCB embedded inductors. The Q values of the PCB embedded inductors varies from 80 to 110 which is lower than what can be achieved with larger air core inductors. The volume of this converter with PCB inductors is significantly reduced as the PCB area remains the same where as the hight of the converter is significantly reduced. This can be very useful in many applications were size is an issue. The PCB embedded inductors has the benefit of being cheap and has a low spread in production. Both the converter with discrete inductors and the one with PCB embedded inductors is implemented as unidirectional converter with a diode rectifier operating in the forward conduction mode see figure 11. In this configuration the efficiency is roughly 2.5% lower than with the synchronous

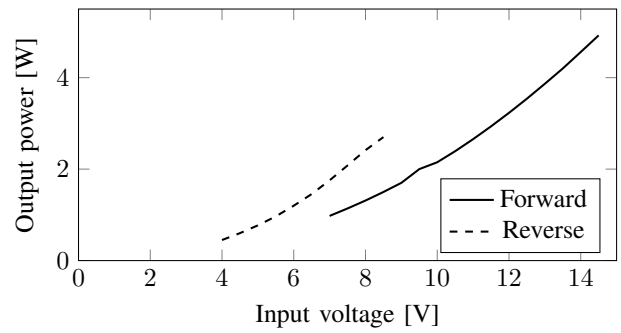


Fig. 9. Measured output power vs. input voltage

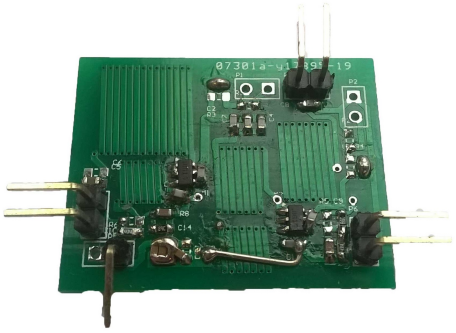
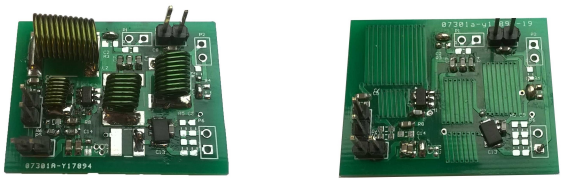


Fig. 10. Prototype with PCB inductors and synchronous rectifier



(a) (b)

Fig. 11. Unidirectional converter prototypes with diode rectifier, (a) with discreate inductors and (b) with PCB enbedded inductors

rectifier due to higher conduction losses in the diodes. This proves that the use synchronous rectifiers are very suitable for low voltage high current applications also in the VHF range.

IV. Conclusions and Future Work

In this paper a VHF bidirectional converter has been implemented and presented, it has been proven that the Class-E converter topology it is able to operate as a bidirectional converter in the VHF range. The implemented converter achieves high efficiency in both operating modes over varying input voltages and output powers. This type of converter can be used in various applications where a small bidirectional converter is needed. The price of this type of converter is relatively low since it only uses ceramic capacitors, air core inductors and two MOSFETs. By using PCB embedded inductors the price and the physical size of the converter can be reduced further however in this case it does decrease the efficiency.

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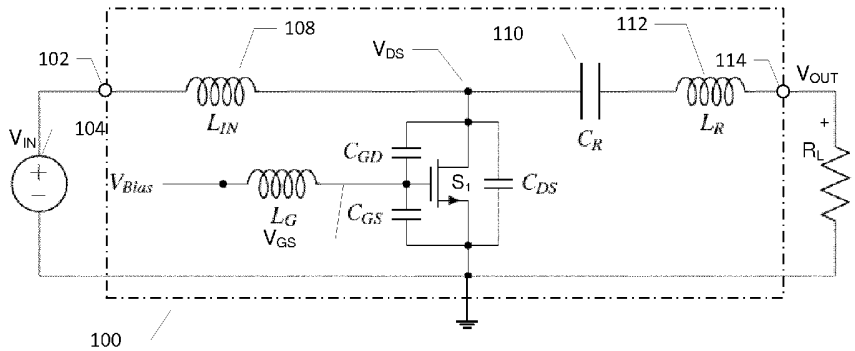

FIG 1A

(57) **Abstract**: The present invention relates to resonant power converters and inverters comprising a self-oscillating feedback loop coupled from a switch output to a control input of a switching network comprising one or more semiconductor switches. The self-oscillating feedback loop sets a switching frequency of the power converter and comprises a first intrinsic switch capacitance coupled between a switch output and a control input of the switching network and a first inductor. The first inductor is coupled in-between a first bias voltage source and the control input of the switching network and has a substantially fixed inductance. The first bias voltage source is configured to generate an adjustable bias voltage applied to the first inductor. The output voltage of the power converter is controlled in a flexible and rapid manner by controlling the adjustable bias voltage.

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SELF-OSCILLATING RESONANT POWER CONVERTER

The present invention relates to resonant power converters and inverters comprising a self-oscillating feedback loop coupled from a switch output to a control input of a switching network comprising one or more semiconductor switches. The self-oscillating feedback loop sets a switching frequency of the power converter and comprises a first intrinsic switch capacitance coupled between a switch output and a control input of the switching network and a first inductor. The first inductor is coupled in-between a first bias voltage source and the control input of the switching network and has a substantially fixed inductance. The first bias voltage source is configured to generate an adjustable bias voltage applied to the first inductor. The output voltage of the power converter is controlled in a flexible and rapid manner by controlling the adjustable bias voltage.

BACKGROUND OF THE INVENTION

Power density is always a key performance metric of a power supply circuit such as AC-DC, DC-AC and DC-DC power converters to provide the smallest possible physical size for a given output power specification. Resonant power converter topologies are well-known types of DC-DC/switched mode power supplies or converters (SMPS) in the art. Resonant power converters are particularly useful for high switching frequencies such as above 1 MHz where switching losses of standard SMPS topologies (Buck, Boost etc.) tend to be unacceptable for conversion efficiency reasons. High switching frequencies are generally desirable because of the resulting decrease of the electrical and physical size of circuit components of the power converter like inductors and capacitors. The smaller components allow increase of the power density of the SMPS. In a resonant power converter an input "chopper" semiconductor switch (often MOSFET or IGBT) of the standard SMPS is replaced with a "resonant" semiconductor switch. The resonant semiconductor switch relies on the resonances of circuit capacitances and inductances to shape the waveform of either the current or the voltage across the switching element such that, when switching takes place, there is no current through or voltage across the switching element. Hence power dissipation is largely eliminated in at least some of the intrinsic capacitances of the input switching element such that a dramatic increase of the switching frequency becomes feasible for example to values above 10 MHz. This concept is known in the art under designations like zero voltage and/or current switching (ZVS

and/or ZCS) operation. Commonly used switched mode power converters operating under ZVS and/or ZCS are often described as class E, class F or class DE inverters or power converters.

However, fast and accurate control of the output voltage of the resonant power converter remains a challenge. Prior art power converters described in the references below propose to utilize a self-oscillating feedback loop around the input switching element and driven by the intrinsic or inherent drain-to-source capacitance of a MOSFET switch in combination with a variable series inductance coupled to the gate terminal of the MOSFET switch.

U.S. 4,605,999 discloses a self-oscillating power converter comprising a self-oscillating inverter circuit build around a single MOSFET switch. The inherent drain-to-source capacitance of the MOSFET switch supplies a feedback path sufficient to sustain self-oscillation of the inverter circuit if the frequency of operation is sufficiently high. The power converter is voltage regulated by a feedback loop deriving the control signal from a DC output voltage of the converter and applying the control signal to a variable inductance network comprising an inductor and a pair of non-linear capacitances.

U.S. 5,430,632 discloses a self-oscillating power converter utilizing a pair of MOSFET transistor switches in a half bridge configuration wherein the junction of the two MOSFET transistors is coupled to a reactive network which in turn is connected to an output rectifier. Intrinsic gate-to-drain inter-electrode capacitances of the switching transistors serve as the sole means of sustaining oscillations. Oscillations are initiated at the gate-to-source terminals of the MOSFET transistor switches by a start-up circuit. The frequency of oscillation is determined by the gate-to-source capacitance of the MOSFET transistor switches and the inductance of an isolated gate drive transformer. The frequency of oscillation is controlled by varying inductance of the isolated gate drive transformer coupled to the gate terminals of the MOSFET transistor switches through a pair of control windings.

However, the possible regulation range of adjustable inductances and/or capacitances tend to be very narrow due to physical component limitations and the accu-

racy may also be limited. Furthermore, adjustable inductances and/or capacitances are difficult to integrate on semiconductor substrates or on ordinary circuit carriers like printed circuit boards. Finally, the maximum regulation speed of the inductance or capacitance may be limited due to the reactive nature of the component leading to an undesirable limitation of the speed of the regulation of the converter output voltage. This is of course particularly undesirable in view of the advantages of moving to higher converter switching frequencies for the reasons discussed above.

Consequently, it would be advantageous to provide a control mechanism for the oscillation frequency that eliminates the need of variable reactive components like inductors and capacitors such that the converter output voltage can be controlled by appropriately controlling a level of a circuit voltage or circuit current for example in the form of an adjustable bias voltage.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a resonant power converter or inverter comprising an input terminal for receipt of an input voltage and a switching network comprising one or more semiconductor switches controlled by respective control inputs. The switching network comprises a switch input operatively coupled to the input terminal for receipt of the input voltage and a switch output operatively coupled to an input of a resonant network of the resonant power converter. The resonant network comprises a predetermined resonance frequency (f_R) and an output operatively coupled to a converter output terminal. A self-oscillating feedback loop is coupled from the switch output to a control input of the switching network to set a switching frequency of the power converter. The self-oscillating feedback loop comprises a first intrinsic switch capacitance coupled between the switch output and the control input of the switching network,

a first bias voltage source configured to generate a first adjustable bias voltage,

a first inductor with substantially fixed inductance coupled in-between the first bias voltage source and the control input of the switching network. A voltage regulation loop of the resonant power converter is configured to control an output voltage of the power converter by controlling the first adjustable bias voltage applied to the first inductor.

The present resonant power converter allows flexible, rapid and accurate control of the converter output voltage by controlling the adjustable bias voltage applied to the first inductor coupled to the control input of the switching network. By adjusting a level of the adjustable bias voltage, an oscillation frequency of the self-oscillating feedback loop coupled around the switching network can be controlled so as to set a switching frequency of the resonant power converter. The adjustment of the oscillation frequency of the self-oscillating feedback loop is achieved without making any adjustment of the inductance of the first inductor which therefore has a substantially fixed inductance independent of the level of the adjustable bias voltage. The skilled person will understand that the term “substantially fixed” characterizing the inductance of the first inductor includes an inductance that vary slightly over temperature depending on electrical characteristics of a particular material of the selected inductor type. Furthermore, the application of the first adjustable bias voltage to the first inductor is preferably carried out without any adjustment of an inductive or capacitive reactance of a component coupled in series with the first inductor in the voltage regulation loop. Hence, the first adjustable bias voltage generated by the voltage regulation loop is preferably applied to the first inductor without any transformer, tuneable inductor or tuneable capacitor in series with the first inductor.

The ability of adjusting the switching frequency of the present resonant power converter by adjusting the level of the first adjustable bias voltage enables a wide and accurate control range of the switching frequency and eliminates or circumvents the previously discussed disadvantages of relying on adjustable inductances and/or capacitances to adjust the switching frequency of the resonant power converter. Power losses in intrinsic or parasitic capacitances such as the first intrinsic switch capacitance of the one or more semiconductor switches are furthermore reduced to a low level by the presence of first inductor because energy stored in these parasitic capacitances during charging is discharged to, and temporarily stored in, the first inductor. The stored energy in the first inductor is subsequently returned to parasitic or intrinsic capacitances of the one or more semiconductor switches. The parasitic or intrinsic capacitances may comprise gate-source, gate-drain and drain-source capacitances of a MOSFET switch.

While the present invention is described in detail in the following with reference to implementations in resonant power converters/inverters and corresponding DC-DC power converters of Class E or DE type or topology, the skilled person will understand that the invention is equally applicable to other types of resonant power inverters, rectifiers and converters such as class E, F, DE and π_2 inverters and rectifiers and resonant boost, buck, SEPIC, LCC, LLC converters etc.

The voltage regulation loop may comprise a reference voltage generator supplying a DC or AC reference voltage to a first input of a comparator or error amplifier. A second input of the comparator may be coupled to the converter output voltage and an output of the comparator may be operatively coupled to a control input of the first bias voltage source. In this manner, the comparator or error amplifier may be configured to generate a suitable error signal as control signal for the first bias voltage source by a comparison of the output voltage of the converter with the DC or AC reference voltage. The error signal or signals applied to the first bias voltage source increases or decreases the first adjustable bias voltage in an appropriate direction to adjust the converter output voltage to the target output voltage indicated by the DC or AC reference voltage as explained in additional detail below in connection with the accompanying drawings.

The skilled person will appreciate that the switching network can comprise numerous types of switch topologies such as single switch topology, half-bridge or full-bridge switch topologies. According to a preferred embodiment, the switching network comprises a first semiconductor switch with a control terminal coupled to the control input of the switching network and an output terminal coupled to the switch input and to the switch output. An input inductor is coupled between the input voltage and the switch input. This embodiment may comprise a basic class E power inverter or converter wherein the switching network comprises a single semiconductor switch with its output terminal, e.g. a drain terminal of a MOSFET, coupled both to the input and output of the switching network. The input inductor forms part of the resonant network to control the setting of the predetermined resonance frequency (f_R). The control terminal, e.g. a gate or base terminal, of the single semiconductor switch is coupled to the control input of the switching network.

The input inductor and the first inductor may be magnetically coupled with a predetermined magnetic coupling coefficient, preferably a magnetic coupling coefficient larger than 0.1 or even more preferably larger than 0.4. The magnetic coupling provides a number of advantages relative to the case of uncoupled input and first inductors such as improved phase response between the signal at the control input of the switching network and the switch output and larger and more constant gain. The magnetic coupling ensures that the inductor currents of the input inductor and first inductor are out of phase. Consequently, a phase shift between the control input signal, e.g. a gate voltage of the MOSFET switch, of the switching network and the switch output is very close to 180 degrees. Furthermore, the magnetic coupling is preferably substantially constant across a wide frequency range to provide a more constant level of the first adjustable bias voltage when the output voltage V_{OUT} of the power converter is regulated.

Another preferred embodiment of the present resonant power converter comprises a half-bridge based switching network. The switching network comprises a first semiconductor switch coupled between the switch output and a voltage supply rail of the resonant power converter and having a control terminal coupled to the control input of the switching network. The switching network additionally comprises a second semiconductor switch coupled between the switch output and the input terminal. A control terminal of the second semiconductor switch is coupled to a second bias voltage source through a cascade of a second inductor with substantially fixed inductance and a third inductor with substantially fixed inductance. A feedback capacitor of the switching network is coupled between the switch output and an intermediate node between the second and third inductors. This embodiment of the present resonant power converter may comprise a class DE power converter, inverter or form part of a class DE based DC-DC power converter.

The feedback capacitor serves as a bootstrap device which raises a voltage level supplied to the control terminal of the second semiconductor switch and thereby facilitates use of a N-channel MOSFET transistor as semiconductor switch device. The second inductor serves as a high impedance signal path at the oscillation frequency allowing passage of a relatively slowly varying bias voltage component gen-

erated by the second bias voltage source, but blocking passage of a relatively high frequency voltage component supplied through the feedback capacitor. Consequently, by combining bias voltage components supplied through the second inductor and the feedback capacitor, the control voltage at the second switch is level shifted and referred to the switch output instead of the voltage supply rail of the first semiconductor switch such as ground or a negative power supply voltage if the input voltage is a positive DC voltage. The self-oscillation loop may be configured to ensure that each of the semiconductor switches S_1 and S_2 is alternately switched between conducting and non-conducting states. The semiconductor switches S_1 and S_2 are also switched in opposite phase according to a non-overlapping scheme.

The first inductor and the third inductor may be magnetically coupled with a predetermined magnetic coupling coefficient, preferably a magnetic coupling coefficient larger than 0.1 or even more preferably larger than 0.4. The magnetic coupling will force a phase shift that is substantially 180 degrees between the control input signals, e.g. gate signals or voltages, of the first and second semiconductor switches. To provide a large magnetic coupling coefficient between the input inductor and the first inductor these may be wound around a common magnetically permeable member or core. For the same reason, the first inductor and the third inductor may be wound around a common magnetically permeable member or core.

The first bias voltage source may be configured in various ways. In one embodiment, the first bias voltage source may be coupled between a suitable DC bias or reference voltage of the resonant power converter and a ground potential or negative supply rail thereof. The first adjustable bias voltage may be derived from the DC bias or reference voltage by suitable voltage division or regulation circuitry. In one embodiment, the first bias voltage source comprises a capacitor coupled from the first adjustable bias voltage to a fixed electric potential of the resonant power converter such as ground. A first adjustable resistor is coupled between the first adjustable bias voltage and a first DC reference voltage and a second adjustable resistor is coupled between the first adjustable bias voltage and a second DC reference voltage. The first DC reference voltage may possess a DC voltage higher than a maximum peak voltage of the first adjustable bias voltage. The second DC reference voltage may possess a DC voltage lower than an expected minimum voltage

of the first adjustable bias voltage such that the first adjustable bias voltage can be varied through a suitable voltage regulation range by adjusting a resistance ratio between the first and second adjustable resistances. Each of the first and second adjustable resistors preferably comprises a MOS transistor allowing the respective resistances to be controlled from a high impedance gate terminal of the MOS transistor.

The first inductor may have an inductance between 1 nH and 10 µH such as between 1 nH and 50 nH. The latter inductance range makes it possible to form the first inductor as an electrical trace pattern of a printed circuit board or as an integrated passive semiconductor component leading to considerable size reduction and reliability advantages of the resonant power converter.

The substantially fixed inductance of the first inductor is preferably determined experimentally for example by adjusting its value until a suitable voltage swing is obtained at the control input of the switching network as explained below in additional detail. Preferably, the substantially fixed inductance is set such that a peak voltage at the control input of the switching network exceeds a threshold voltage of at least one of the semiconductor switches of the switching network. This threshold voltage may for example lie between 5 and 10 V for an N-channel power MOSFET, but the skilled person will appreciate that other types of semiconductor switches may have different threshold voltages depending on characteristics of the semiconductor technology in question.

In one embodiment, the substantially fixed inductance of the first inductor is selected such that a peak-peak voltage swing at the control input of the switching network is approximately equal to a numerical value of the threshold voltage of the at least one of the semiconductor switches of the switching network. In the above-mentioned example in respect of the N-channel power MOSFET, the peak-peak voltage swing would accordingly be adjusted to a value between 5 and 10 V in accordance with the threshold voltage.

In another embodiment, the self-oscillating feedback loop comprises a series resonant circuit coupled in-between the control input of the first semiconductor switch

and a fixed electric potential of the converter. The series resonant circuit preferably comprises a cascade of capacitor and an inductor connected between the control input of the semiconductor switch and a negative power supply rail e.g. ground. The series resonant circuit functions to introduce additional uneven frequency components, by attenuating one or more even harmonic frequency components, to a fundamental frequency component of the oscillating voltage waveform at the control input of the switching network, e.g. the gate of the first semiconductor switch. This leads to a trapezoidal waveform shape of the oscillating voltage waveform and results in faster switch turn-on and turn-off times.

A useful embodiment of the present resonant power converter comprises a DC-DC power converter. The DC-DC power converter is preferably constructed or derived by coupling a rectifier between the output of the resonant network and the inverter or converter output terminal to generate a rectified DC output voltage. The rectifier may comprise one or more diodes to provide passive rectification of the DC output voltage. The rectifier of an alternative embodiment of the resonant power converter comprises a synchronous rectifier which may comprise one or more semiconductor switches. According to one such embodiment the synchronous rectifier comprises: a rectification semiconductor switch configured to rectify an output voltage of the resonant network in accordance with a rectifier control input of the rectification semiconductor switch. A first rectification inductor with a substantially fixed inductance is coupled in-between a fixed or adjustable rectifier bias voltage and the rectifier control input. It is a significant advantage of this embodiment that the fixed or adjustable rectifier bias voltage of the rectifier may be left decoupled or unconnected to the first bias voltage source generating the first adjustable bias voltage for the switching network on the input side of the resonant power converter for the reasons discussed in detail below with reference to FIG. 8 of the appended drawings. The fixed or adjustable rectifier bias voltage may for example be coupled to a fixed DC bias voltage source of the resonance power converter or to the rectified DC output voltage through a resistive or capacitive voltage divider.

The skilled person will appreciate that numerous types of semiconductor transistors may be used to implement each of the first and second semiconductor switches depending on requirements such as threshold voltage, gate source break-down

voltage, drain source break-down voltage etc., imposed by any particular resonant power converter. Each of the first and second semiconductor switches may for example comprise a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET.

A second aspect of the invention relates to a resonant power converter assembly comprising a resonant power converter according to any of the above described embodiments thereof and a carrier substrate having at least the switching network and the resonant circuit integrated thereon wherein an electrical trace pattern of the carrier substrate is forming the first inductor. The carrier substrate may comprise a single-layer or multi-layer printed circuit board with integrally formed electrical wiring patterns interconnecting various electronic components of the resonant power converter. The relative small inductance required for the first inductance for achieving VHF switching frequencies of the power converter, e.g. in the order of tens of nH, facilitates an advantageous integration of the first inductor, and potentially other inductors of the power converter of suitable size, directly in the wiring pattern of carrier substrates like printed circuit boards. This type of integration leads to several advantages such as saving component costs, reducing assembly time and costs and possibly improving reliability of the power converter assembly.

A particularly advantageous embodiment of the carrier substrate comprises a semiconductor die, such as a CMOS based integrated circuit, integrating all active and passive components of the present resonant power converter thereon.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention will be described in more detail in connection with the appended drawings, in which:

FIG. 1A) is an electrical circuit diagram of a class E resonant power converter in accordance with a first embodiment of the invention,

FIG. 1B) is an electrical circuit diagram of a class E resonant power converter comprising a pair of magnetically inductors in accordance with a second embodiment of the invention,

FIG. 2A) is an electrical circuit diagram of a class E resonant power converter comprising a series resonant circuit in accordance with a third embodiment of the invention,

FIG. 2B) is an electrical circuit diagram of a class E resonant power converter comprising a series resonant circuit in accordance with a fourth embodiment of the invention,

FIG. 2C) is an electrical circuit diagram of a gate drive circuit for class E and DE resonant power converters comprising a plurality of series resonant circuits,

FIG. 2D) shows a plurality of magnitude and phase response curves of transfer functions of a MOSFET switch of the class E resonant power converter in accordance with the third embodiment of the invention,

FIG. 2E) shows a plurality of control input signal waveforms of the MOSFET switch of the class E resonant power converter in accordance with the third embodiment of the invention,

FIG. 3A) is an electrical circuit diagram of a class DE resonant power converter in accordance with a fifth embodiment of the invention,

FIG. 3B) is an electrical circuit diagram of a class DE resonant power converter comprising a pair of magnetically coupled inductors in accordance with a sixth embodiment of the invention,

FIG. 4 is an electrical circuit diagram of an exemplary DC-DC power converter based on the class E resonant power converter in accordance with the first embodiment of the invention,

FIG. 5 shows a series of graphs illustrating voltage waveforms at the output of a switching network of the class E resonant power converter of the first embodiment for different bias voltage levels applied to the control input of the switching network,

FIG. 6 is a circuit simulation model of a second exemplary DC-DC power converter based on the first embodiment of the class E resonant power converter,

FIG. 7 shows a series of graphs illustrating various simulated voltage waveforms of the second DC-DC power converter for four different DC bias voltage levels of an adjustable bias voltage; and

FIG. 8 is an electrical circuit diagram of a third DC-DC power converter with synchronous rectification on the output side based on the class E resonant power converter in accordance with the first embodiment of the invention

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1A) is a simplified electrical circuit diagram of a class E resonant power converter 100 in accordance with a first embodiment of the invention. The present class E resonant power converter is particularly well-adapted for operation in the VHF frequency range for example at switching frequencies above 10 MHz or even higher such as between 30 and 300 MHz due to, amongst other factors, low switching losses in connection with the operation of a self-oscillating feedback loop connected around a transistor switch element S_1 as explained in further detail below.

The class E resonant power inverter or converter 100 comprises an input pad or terminal 102 for receipt of a DC input voltage V_{IN} from a DC power supply 104. The DC voltage level may vary considerably according to requirements of any particular conversion application such as lying between 1 V and 500 V for example between 10 V and 230 V. A switching network comprises a single switch transistor S_1. The skilled person will understand that the switch transistor S_1 can comprise different types of semiconductor transistors such as MOSFETs and IGBTs. The skilled person will likewise understand that the switch transistor S_1 in practice can be formed by a plurality of parallel separate transistors e.g. to distribute operational currents between multiple devices. In one embodiment of the invention, S_1 is formed by an IRF5802 power MOSFET available from the manufacturer International Rectifier. A gate terminal V_{GS} of the switch transistor S_1 forms a control input of the switching network allowing S_1 to be switched between a conducting state or on-state with low resistance between the drain and source terminals and a non-conducting state or off-state with very large resistance between the drain and source terminals. A drain terminal V_{DS} of the switch transistor S_1 forms both a switch input and a switch output of the switching network in the present embodiment based on a single switch transistor. The drain terminal V_{DS} is at one side coupled to the DC input voltage through an input inductor L_{IN} (108). The drain terminal V_{DS} is also coupled to a first side of a series resonant network comprising resonant capacitor C_R and resonant inductor L_R. The input inductor $L_{IN,}$ resonant capacitor C_R, an intrinsic drain-source capacitance C_{DS} of the MOSFET S_1 and the resonant inductor L_R (112) form in conjunction a resonant network of the power converter 100. A second and opposite side of the series resonant network is operatively coupled to an output terminal 114 or node of the class E resonant power converter 100 either directly as illustrated or through a suitable rectification circuit as illustrated in detail below. An inverter load is schematical-

ly indicated by a load resistor R_{LOAD} connected to the converter at the output terminal 114 and may generally exhibit inductive, capacitive or resistive impedance. The resonant network is designed with a resonance frequency (f_R) of about 50 MHz in the present implementation, but the resonance frequency may vary depending on requirements of the application in question. In practice, the respective values of the resonant capacitor C_R and resonant inductor L_R may be selected such that a target output power at the converter output is reached for a particular load impedance. Thereafter, the value of the input inductor L_{IN} is selected such that a desired or target value of the predetermined resonance frequency (f_R) is reached in view of the intrinsic drain-source capacitance C_{DS} for the selected switch transistor.

The present class E resonant power converter 100 comprises a self-oscillating feedback loop arranged around the transistor switch S_1 such that the oscillation frequency of the loop sets the switching or operational frequency of the power converter 100 as briefly mentioned above. The self-oscillating feedback loop comprises an intrinsic gate-drain capacitance C_{GD} of the transistor switch S_1 which transmits a 180 degree phase shifted portion of the switch output signal at the drain terminal V_{DS} back to the gate terminal of the transistor switch S_1. Additional loop phase shift is introduced by the gate inductor L_G which preferably comprises a substantially fixed inductance. The gate inductor L_G is coupled in-between a variable bias voltage V_{Bias} and the gate terminal of the transistor switch S_1. The variable bias voltage V_{Bias} is generated by a bias voltage generator or source with a design explained in further detail below in connection with FIG. 4. However, the adjustable bias voltage V_{Bias} applied to the gate terminal of transistor switch S_1 through the gate inductor L_G provides an advantageous mechanism for controlling the converter output voltage V_{OUT}. This mechanism exploits that the time period of the cycle time, the cycle time being the reciprocal of the oscillation frequency of the feedback loop, during which S_1 remains in a non-conducting state is controlled by the previously mentioned components of the resonant network defining the resonance frequency (f_R). The latter frequency controls when the voltage at the switch output at V_{DS} reaches ground or zero volts, being the lower power supply rail of the converter in the present embodiment, and thereby allowing S_1 to be turned on again without introducing switching losses to discharge the intrinsic drain-source capacitance C_{DS}. This operation mechanism where the resonant circuit is used to discharge the intrinsic semiconductor switch

capacitance until the voltage across the semiconductor switch reaches approximately zero is normally denoted zero voltage switching (ZVS) operation.

Conversely, the time period of the cycle time during which S_1 remains conducting, or in its on-state, can be controlled by the level of the adjustable bias voltage. This property allows a duty cycle, and hence the oscillation frequency of the self-oscillating loop, to be adjusted. This is explained in further detail in connection with FIG. 5 below. Since the switch output at V_{DS} is coupled directly to the DC input voltage through the input inductor L_{IN} the average voltage at the switch output V_{DS} is forced to equal the DC input voltage. The integral of a half-period sine waveform of frequency (f_R) equals the sine amplitude divided by pi times the resonance frequency (f_R). Furthermore, when S_1 is conducting the voltage across S_1 is essentially zero such that the voltage at the switch output V_{DS} becomes substantially zero. These circumstances lead to the following equation for a peak voltage, $V_{DS,PEAK}$, across S_1:

$$V_{DS,PEAK} = \frac{V_{IN}*\pi*f_R}{f_S} \qquad (1);$$

wherein f_S = The oscillation frequency of the self-oscillation loop which equals the switching frequency of the power converter.

Equation (1) reveals that a decreasing oscillation frequency leads to increasing switch output voltage V_{DS} as illustrated below by switch output voltages V_{DS} of FIG. 5.

The voltage waveforms, duty cycle control and oscillation frequency control discussed above are illustrated on the graphs 500, 510 and 520 of FIG. 5 for three different levels of the adjustable bias voltage V_{Bias} applied to the substantially fixed inductance gate inductor L_G. The scale on the y-axis of all graphs indicates voltage in volts while the x-axis scale indicates time in steps of 10 ns such that the entire x-axis spans over about 100 ns. As mentioned above, L_G is coupled to the control input or gate V_{GS} of the transistor switch S_1. In graph 500, the adjustable bias voltage V_{Bias} has been adjusted to a level which results in a duty cycle of approximately 0.5 in the switch output voltage V_{DS}. Waveform 501 shows the switch output voltage V_{DS}

while waveform 503 shows the corresponding gate-source voltage applied to the gate V_{GS} of S_1. It is evident that the cycle time of the switch output voltage V_{DS} is about 10 s corresponding to an oscillation frequency of about 100 MHz.

In practice, the substantially fixed inductance of the gate inductor L_G may be selected such that a desired voltage amplitude of the (oscillating) gate-source voltage waveform is achieved. The voltage amplitude is preferably adjusted such that a suitable peak voltage at the gate terminal of MOSFET switch S_1 is reached in view of its threshold voltage and its gate break-down voltage. This means that the peak voltage at the gate terminal should be sufficiently large to exceed the threshold voltage of the chosen semiconductor switch, e.g. V_{TH} of MOSFET switch S_1. The oscillation frequency f_S of the self-oscillation loop will inherently lie close to the resonance frequency (f_R) of the resonant network if the bias voltage is adjusted approximately to the threshold voltage of the MOSFET switch S_1. If the adjustable bias voltage V_{Bias} is increased above the threshold voltage, the on-period of the MOSFET switch S_1 increases and leads to increase of the duty cycle of the oscillating switch output voltage waveform. This leads to a decreasing oscillation frequency or switching frequency of the power converter. The decrease of the oscillation frequency leads to an increase of the peak voltage $V_{DS,PEAK}$ at the switch output as explained above in connection with equation (1), and a corresponding increase of the peak voltage across the series resonant network comprising resonant capacitor C_R and resonant inductor L_R due to its coupling to the switch output voltage V_{DS}. Furthermore, because the series resonant network exhibits inductive impedance, the decreasing oscillation frequency of the switch output voltage waveform leads to a decrease of the impedance of the series resonant network. The decrease of impedance leads in turn to increasing current and power through the series resonant network and through the load resistor R_{LOAD} - in effect increasing the converter output voltage V_{OUT}.

Consequently, the converter output voltage V_{OUT} can be controlled by appropriately controlling the adjustable bias voltage V_{Bias} applied to the substantially fixed inductance gate inductor L_G. This feature provides a highly flexible and fast way of controlling the converter output voltage V_{OUT} compared to prior art mechanism based on adjustable inductances and/or capacitances. In particular, the range of

adjustment of the adjustable bias voltage V_{Bias} can be very wide compared to the possible regulation range of the adjustable inductances and/or capacitances.

In graph 510, the adjustable bias voltage V_{Bias} has been increased to a level which results in a duty cycle of approximately 0.7 in the switch output voltage $V_{DS.}$ Waveform 511 shows the switch output voltage V_{DS} while waveform 513 shows the corresponding gate-source voltage applied to the gate V_{GS} of S_1. As illustrated, the switch output voltage V_{DS} has increased from a peak level of approximately 30 volt for the 0.5 duty cycle condition depicted above to approximately 50 volt. It is evident that the cycle time of the switch output voltage V_{DS} has decreased to about 18 ns corresponding to an oscillation frequency of about 55 MHz. Finally, in graph 520, the adjustable bias voltage V_{Bias} has been further increased to a level which results in a duty cycle of approximately 0.9 in the switch output voltage $V_{DS.}$ Waveform 521 shows the switch output voltage V_{DS} while waveform 523 shows the corresponding gate-source voltage applied to the gate V_{GS} of S_1. As illustrated, the switch output voltage V_{DS} has further increased from a peak level of approximately 50 volt for the 0.7 duty cycle condition depicted above to approximately 150 volt. It is evident that the cycle time of the switch output voltage V_{DS} has further decreased to about 50 ns corresponding to an oscillation frequency of about 20 MHz.

FIG. 1B) is an electrical circuit diagram of a class E resonant power converter 100b comprising a pair of magnetically coupled inductors in accordance with a second embodiment of the invention. The skilled person will appreciate that the above discussed features, functions and components of the first embodiment of the class E resonant power converter 100 may apply to the present embodiment as well. Likewise, corresponding components in the first and second embodiments of the present class E resonant power converter have been provided with corresponding reference numerals to ease comparison. The main difference between the first and second embodiments is that the previously discussed separate and substantially uncoupled input inductor L_{IN} and gate inductor L_G have been replaced by the pair of magnetically coupled inductors L_{In} and L_G where the respective functions in the present class E resonant power converter 100b are similar to those of the first embodiment. The skilled person will appreciate that magnetic coupling between the input inductor L_{in} and gate inductor L_G may be achieved in numerous ways for example by a close-

ly spaced arrangement of the inductors e.g. coaxially arranged. The magnetic coupling provides a number of advantages over the first embodiment such as improved phase response between the control input and switch output of the MOSFET switch S_1 and larger and more constant gain. The magnetic coupling ensures that the respective inductor currents of the input inductor L_{in} and gate inductor L_G are out of phase. Consequently, the phase shift between control input of the switch S_1 and the switch output is very close to 180 degrees. Furthermore, the magnetically coupled input inductor L_{in} and gate inductor L_G may be configured such that the magnetic coupling is substantially constant across a wide frequency range to provide a more constant level of the first adjustable bias voltage when the output voltage V_{OUT} of the power converter is regulated.

The magnetic coupling between the magnetically coupled input inductor L_{in} and gate inductor L_G may also be accomplished by a transformer structure as schematically indicated on FIG. 1B). The input inductor L_{in} and gate inductor L_G may for example be wound around a common magnetically permeable member or core. The latter embodiment has the advantage of a stronger coupling of magnetic fields between the input inductor L_{in} and gate inductor L_G. This forces a phase shift even closer to 180 degrees between the control input of the switch S_1 (i.e. gate voltage of switch S_1) and the switch output (i.e. drain voltage of the switch S_1).

The magnetically coupled input inductor L_{in} and gate inductor L_G may be configured to possess a magnetic coupling which is sufficient to ensure that inductor current forced in L_G by L_{IN} is sufficiently large to drive the control input of the switch S_1. In this case the gate drive can also be used to drive cascode coupled transistors where the intrinsic capacitance C_{GD} is small or non-existent.

FIG. 2A) is a simplified electrical circuit diagram of a class E resonant power converter 200 in accordance with a third embodiment of the invention. The present power converter is of similar topology to the above discussed power converter based on a single switch transistor S_1. The skilled person will appreciate that the above discussed features, functions and components of the first embodiment may apply to the present embodiment as well. Likewise, corresponding components in the first and second embodiments of the present class E resonant power converter

have been provided with corresponding reference numerals to ease comparison. The main difference between the first and second embodiments lies in an addition of a series resonant circuit, comprising a cascade of capacitor C_{MR} and inductor L_{MR}, connected between the gate node or terminal V_{GS} of switch transistor S_1 and the negative supply rail e.g. ground. The function of the series resonant circuit is to introduce additional uneven frequency components, by attenuating one or more even harmonic frequency components, to the fundamental frequency component of the oscillating gate voltage waveform of the switch transistor S_1. This leads to a trapezoidal waveform shape of the gate voltage of switch transistor S_1 leading to faster switch turn-on and turn-off times. This is beneficial because it reduces the conduction losses, as the switch MOSFET S_1 will have relatively high resistance when the gate voltage is just above the threshold voltage. FIG. 2C) shows generally applicable embodiments of a series resonant network 201a coupled to the control input, e.g. a gate terminal, of a switch transistor or a switching network of a class E or DE resonant power converter such as the class E and DE resonant power converters depicted on FIGS. 1A)-1B), FIG. 2A), FIGS. 3A)-3B), FIG. 4 and FIG. 8. The series resonant network 201 comprises a plurality of series resonant circuits of which one or more may be included in particular design of the class E or DE resonant power converter.

If a transistor switch like a MOSFET is driven by a sine wave the gate signal will be right above the threshold voltage of the MOSFET in a beginning and end of a conduction period of the MOSFET. This causes the on resistance to be very high in these periods as the MOSFET is only fully turned on when the gate signal is larger than around twice the threshold voltage. In many resonant power converters these time periods are also where the largest currents are running through the MOSFET. Hence a lot of power is dissipated in these time periods. In order to improve the turn on speed of the MOSFET, higher order harmonics can be added to the fundamental sine wave leading to a more trapezoidal gate signal as mentioned above. This can be achieved by adding one or more series resonant circuits, each preferably comprising an LC circuit, between the control input, i.e. the gate of the present MOSFET switch, and a drain or source of the MOSFET as illustrated on FIG. 2C). Here the capacitor, C_{GDext}, is optional and may be used to increase overall gain of the gate signal as shown in FIG. 2D). In the same way capacitor, C_{GSext}, can optionally be

used to lower the gain. The first and second LC based series resonant circuits C_{4HI} and L_{4HI} and C_{2HI} and L_{2HI}, respectively, are both connected to drain of MOSSFET switch S_1 and will cause higher harmonics to be in phase with the switch output voltage at the switch output, V_{DS}. The third and fourth LC based series resonant circuits C_{4HO} and L_{4HO} and C_{2HO} and L_{2HO}, respectively, connected to the ground will cause the harmonics to be out of phase with V_{DS} as illustrated in FIG. 2D). The magnitude response curve 250 of graph 245 of FIG. 2D) illustrates how a LC circuit with a resonance at the second harmonic of the switching frequency of the power converter causes a peak in the gain at the third harmonic and that it is in phase with the switch output V_{DS}. It can be shown that a 3rd harmonic in phase will be desirable for a duty cycle of 25%, but for a duty cycle of 50% it would be more desirable to have the signal out of phase as this would increase the signal right after and turn on of the MOSFET and just before turn off of the MOSFET. This feature can be achieved by setting a LC series resonant circuit with resonant frequency at the 2nd harmonic to ground instead as indicated by the third and fourth series resonant circuits C_{4HO} and L_{4HO} and C_{2HO} and L_{2HO}, respectively, of FIG. 2C). By this connection, the magnitude response curve 252 of FIG. 2D) is achieved. Here a zero is seen at the 2nd harmonic of the switching frequency and again a peak at the 3rd harmonic, but this time with a phase shift of nearly 180 degrees (please refer to curve 252 of the phase graph 246). The skilled person will understand that the number of harmonics to include in a given power converter design will depend on several parameters as price, complexity, efficiency etc. Adding higher order harmonics will in general increase the performance of the power converter, but it is important to consider which harmonics to include and the magnitude of those harmonics compared to the fundamental. Graphs 247 and 248 of FIG. 2E) show the fundamental and the 3rd and 5th harmonics of the switching frequency are in and out of phase with the switch output signal for the duty cycle D set to 25 % and 50 %. Note that the symbol * indicates that the depicted signal is in phase with the switch output signal V_{DS}. By comparing, the gate drive signal waveforms with the indicated ideal (rectangular) waveform shape of the same, it is clear that it is desirable to place the fundamental out of phase with the switch output signal, but for the 3rd and 5th harmonic it depends on the duty cycle and the current waveform. Exemplary gate drive waveforms that can be achieved by adding harmonics by the above-described series resonant networks are shown in the graphs 247 and 248 of FIG. 2E).

FIG. 2B) is an electrical circuit diagram of a class E resonant power converter 200b comprising a series resonant circuit in accordance with a fourth embodiment of the invention. The skilled person will appreciate that the above discussed features, functions and components of the third embodiment of the class E resonant power converter 200 may apply to the present embodiment as well. Likewise, corresponding components in the third and fourth embodiments of the present class E resonant power converter have been provided with corresponding reference numerals to ease comparison. The main difference between the third and fourth embodiments is that the previously discussed a series resonant circuit, comprising the cascade of capacitor C_{MR} and inductor L_{MR}, connected between the gate node or terminal V_{GS} of switch transistor S_1 and ground have been replaced by another type of resonant circuit comprising the parallelly coupled capacitor C_{MR} and inductor L_{MR}. The parallelly coupled capacitor C_{MR} and inductor L_{MR} are connected between the adjustable bias voltage V_{Bias} and the gate inductor L_g. This connection with the parallelly coupled capacitor C_{MR} and inductor L_{MR} provides the same advantages as the series resonant circuit employed in the third embodiment, but with much smaller inductances of inductors L_g and L_{MR} leading to a significant reduction in costs and size.

FIG. 3A) is a simplified electrical circuit diagram of a class DE resonant power converter or inverter 300 in accordance with a fifth embodiment of the invention. The present resonant power inverter 300 is based on a switching network which comprises a half-bridge semiconductor topology. The present DE resonant power converter 300 provides several important advantages. One of the biggest challenges when designing resonant power converters is a huge voltage stress imposed on the switch element in the single switch power converter topology described above in connection with the first, second, third and fourth embodiments of the invention. This voltage stress may reach 3-4 times the level of the DC input voltage. Using a half bridge switch topology instead limits a peak voltage across the each of the semiconductor switches S_1 and S_2 to a level of the input voltage. However, this requires a fast and efficient high side driver which can pose a significant advantage if an operating frequency or switching frequency above approximately 5 MHz is desired. The present generation of the first adjustable bias voltage solves this problem as it can also be used as a high side drive (V_{Bias1}) at several tens of megahertz. The half-

bridge comprises a cascade of the first semiconductor switch S_1 coupled between a switch output terminal 311 and ground and a second semiconductor switch S_2 coupled between the switch output terminal 311 and a DC input voltage rail supplied through power input terminal 302 from an external DC voltage source or generator 304. A coupling or mid-point node interconnecting the first and second semiconductor switches S_1 and S_2 form the switch output terminal 311. This switch output terminal 311 is the drain terminal of the first semiconductor switch S1. This switch output terminal or node 311 is coupled to a first side of a series resonant network comprising resonant capacitor C_R and resonant inductor L_R. A drain node of the transistor switch S_2, coupled to the DC input voltage, comprises the switch input terminal of the present half-bridge switch. Each of semiconductor switches S_1 and S_2 may comprise a NMOS power transistor as illustrated by the switch symbol. Intrinsic drain-gate, gate-source and drain-source capacitances of the first NMOS transistor switch S_1 are depicted as C_{GD2}, C_{GS2} and C_{DS2} and likewise as C_{GD1}, C_{GS1} and C_{DS1} for NMOS transistor switch S_2.

The, resonant capacitor C_R, intrinsic drain-source capacitances of switches S_1 and S_2, C_{DS1} and C_{DS2}, respectively, and the resonant inductor L_R in conjunction form a resonant network of the power converter 300. A second and opposite side of the series resonant network is coupled to an output terminal 314 or node of the power converter 300. A converter load is schematically illustrated by a load resistor R_{LOAD} connected to the converter at the output terminal 314 and may generally exhibit inductive, capacitive or resistive impedance. The class DE resonant power inverter 300 furthermore includes a self-oscillating feedback loop arranged around the transistor switch S_1 such that an oscillation frequency of the loop sets the switching or operational frequency of the power converter in a manner similar to the one discussed in detail above in connection with the first embodiment of the invention. The self-oscillating feedback loop comprises an intrinsic gate-drain capacitance C_{GD2} of the transistor switch S_1 and a first gate inductor L_{G2} which preferably comprises a substantially fixed inductance as discussed above. The gate inductor L_{G2} is coupled in-between a variable bias voltage V_{Bias2} and the gate terminal V_{GS2} of the transistor switch S_1. The variable bias voltage V_{Bias2} may be generated in numerous ways by a suitably configured bias voltage generator or source for example as explained in further detail below in connection with FIG. 4. In addition to the circuitry forming the

self-oscillating feedback loop arranged around transistor switch S_1, the current power inverter 300 comprises a second or high side adjustable bias voltage V_{Bias1} that is coupled to the gate terminal of the second semiconductor switch S_2 through a cascade of a second substantially fixed inductance L_H and a third substantially fixed inductance L_{G1}. The inductances of the gate inductors L_{G2} and L_{G1} may be substantially identical. A feedback capacitor C_{G1} is coupled between the switch output node 311 and an intermediate node between the second and third substantially fixed inductances L_H and L_{G1}. The feedback capacitor C_{G1} serves as a bootstrap device which raises the voltage level supplied to the upper transistor switch S_2 and facilitates use of a N-channel MOSFET transistor as switch device. The inductor L_H serves as a high impedance signal path at the oscillation frequency allowing passage of a relatively slowly varying bias voltage component generated by the second adjustable bias voltage V_{Bias1}, but blocking passage of a relatively high frequency voltage component supplied through the bootstrap capacitor or feedback capacitor C_{G1}. Consequently, combining the bias voltage components from L_H and C_{G1}, the gate control voltage at the gate terminal of the second switch S_2 is level shifted. In this manner, the gate control voltage is referred to the switch output node 311 instead of ground. The self-oscillation loop ensures that each of the semiconductor switches S_1 and S_2 is alternately switched between conducting and non-conducting states in opposite phase in a non-overlapping manner. Thereby, the switch output node 311 becomes alternatingly clamped to the DC input voltage V_{IN} and ground through the semiconductor switches S_1 and S_2 at a frequency defined by the oscillation frequency of the self-oscillating loop.

The duty cycle of the switch output voltage waveforms and hence the converter output voltage at V_{out} can once again be controlled by synchronously controlling the respective bias voltages supplied by the first and second adjustable bias voltages V_{Bias2} and V_{Bias1}.

FIG. 3B) is an electrical circuit diagram of a class DE resonant power converter 300b comprising a pair of magnetically coupled inductors L_{G1} and L_{G2} in accordance with a sixth embodiment of the invention. The skilled person will appreciate that the above discussed features, functions and components of the first embodiment of the class DE resonant power converter 300 may apply to the present embodiment as

well. Likewise, corresponding components in the fifth and sixth embodiments of the present resonant power converters have been provided with corresponding reference numerals to ease comparison. The main difference between the fifth and sixth embodiments is that the previously discussed separate and substantially uncoupled gate inductors L_{G1} and L_{G2} have been replaced by the pair of magnetically coupled inductors L_{G1} and L_{G2} where their respective functions in the present class E resonant power converter 300b are similar to those of the first embodiment. The skilled person will appreciate that magnetic coupling between the gate inductors L_{G1} and L_{G2} may be achieved in numerous ways for example by a closely spaced arrangement of the inductors e.g. coaxially arranged. The magnetic coupling provides a number of advantages over the above-described first embodiment of the class DE resonant power converter 300 such as improved phase response between the respective gate signals at the gate terminals, or control inputs, of the inductors L_{G1} and L_{G2} and larger gain. The magnetic coupling ensures that the respective inductor currents in the inductors L_{G1} and L_{G2} are out of phase. Hence, forcing a phase shift that is substantially 180 degrees between the gate signals of the inductors L_{G1} and L_{G2}.

The magnetic coupling between the inductors may also be accomplished by a transformer structure as schematically indicated on FIG. 3B) wherein the inductors L_{G1} and L_{G2} are wound around a common magnetically permeable core. The latter embodiment has the advantage that a larger magnetic coupling between the inductors L_{G1} and L_{G2} can be achieved and the relative phase shift of substantially 180 degrees between the respective gate signals or voltages of the MOSFET switches S_1 and S_2 is enforced even stronger.

FIG. 4 is a schematic electrical circuit diagram of a DC-DC or switched mode power converter/supply (SMPS) 400 which is based on the class E resonant power converter or inverter 100 disclosed above in a first embodiment of the invention. The DC-DC power converter 400 comprises, in addition to the circuitry of the class E resonant power converter 100, a voltage control loop controlling the level of a DC output voltage V_{OUT} of the DC-DC converter and a rectifier 413 schematically illustrated by a storage capacitor and a diode. The rectifier 413 preferably includes a series inductor coupled between the illustrated diode and the output voltage terminal V_{OUT}. The skilled person will appreciate that the illustrated diode(s) based rectifier

413 may be replaced by a synchronous rectifier based on one or more actively controlled semiconductor switches rather than diodes as described in additional detail below with reference to FIG. 8. The voltage control loop regulates respective resistances of a pair of pull-up and pull-down MOSFET resistors M_1 and M_2 forming part of bias voltage source or generator supplying the adjustable bias voltage V_{Bias}. The adjustable bias voltage V_{Bias} is applied to the gate terminal of transistor switch S_1 through the gate inductor L_G as explained in connection with FIG. 1A) above. The voltage control loop comprises a comparator or error amplifier 414 which has a first input coupled to a DC or AC reference voltage V_{REF} and a second input coupled to the DC output voltage V_{OUT} of the converter. A resulting error signal V_{ERR} reflecting whether the output voltage is lower or higher than the reference voltage is fed to an optional level converter 414. The level converter 414 is configured to provide appropriate gate control signals V_{C1} and V_{C2} for the pair of pull-up and pull-down MOSFET resistors M_1 and M_2 to either increase or decrease the adjustable bias voltage V_{Bias}. The bias voltage source or generator comprises the MOSFET resistors M_1 and M_2 coupled between the DC input voltage and ground. Hence, the adjustable bias voltage V_{Bias} can either be pulled towards the DC input voltage or ground depending on the adjustable on-resistances of the MOSFET resistors M_1 and M_2. The skilled person will appreciate that the voltage control loop can be configured in numerous ways to provide appropriate control signals to the MOSFET resistors M_1 and M_2 for example by proportional voltage control or by purely binary voltage control, i.e. up/down.

FIG. 6 is a circuit simulation model of a second DC-DC power converter based on the first embodiment of the class E resonant power converter. The DC-DC converter comprises a rectifier coupled between an output of the series resonant circuit, including C1 and L4, and a load resistance R6 coupled to an output voltage of the converter. The rectifier comprises components C3, D, L2 and C5. Inductor and capacitor component values of the second DC-DC power converter are listed on the figure in Henry and Farad, respectively. Accordingly, the inductance of the gate inductor Lg is set to a substantially fixed value of 68 nH. The semiconductor switch is modelled by an ideal switch ISW with the listed parameters, i.e. an on-state resistance of 1.0 Ω off-state resistance of 1MΩ and threshold voltage of 4.5 V.

FIG. 7 shows a series of graphs 600, 610, 620, 630 and 640 illustrating various simulated voltage waveforms of the simulation model of the second DC-DC power converter for four different fixed DC bias voltage levels of the adjustable bias voltage V_{bias}. V_{bias} is stepped through fixed DC voltage levels of -7.0, -2.0, 3.0 and 8.0 volt as illustrated by waveforms 607, 605, 603, 601, respectively, of graph 600 showing the DC bias voltage level. The DC input voltage V2 (Vin) is kept constant at 50 volts for all simulations.

The scale on the y-axis of all graphs indicates voltage in volts while the x-axis scale indicates time in steps of 0.01 µs such that the entire x-axis spans over about 0.05 µs.

Graph 610 illustrates the corresponding oscillating control input voltage waveforms 617, 615, 613, 611 at the indicated gate node (refer to FIG. 6) for the four different levels of the DC bias voltage. The higher average level of the oscillating control input voltage waveforms for the highest DC bias voltage of 8.0 V is evident. Graph 620 illustrates the corresponding switch output voltage waveforms 627, 625, 623, 621 at the switch output node i.e. at the indicated drain node (refer to FIG. 6). The longer conducting states or on-states of the switch ISW for the highest DC bias voltage of 8.0 V is evident leading to a lower oscillation frequency or switching frequency of the converter.

Graph 640 illustrates the corresponding load power waveforms 627, 625, 623, 621 for the power delivered the load resistor R6 through the converter output. The gradually increasing load power from about 1.5 W at the lowest DC bias voltage of -7.0 V to about 3.5 W at the highest DC bias voltage of 8.0 V is evident. Hence, converter output power and therefore converter output voltage can be controlled by adjusting the voltage supplied by the adjustable bias voltage V_{bias}.

FIG. 8 is a schematic electrical circuit diagram of a DC-DC or switched mode power converter/supply (SMPS) 800 based on the class E resonant power converter or inverter 100 according to the first embodiment of the invention discussed above. The DC-DC power converter 800 comprises, in addition to the circuitry of the class E resonant power converter 100, a synchronous rectifier building around transistor

switch S_{R1} and comprising additional passive components L_{G2} and L_{OUT}. The skilled person will understand that the DC-DC power converter 800 may comprise an output capacitor coupled from V_{OUT} to the negative supply rail (e.g. ground) and a voltage control loop similar to the one discussed above in connection with FIG. 4 in the fourth embodiment of the invention. The voltage control loop being configured to control the output voltage at V_{OUT} of the power converter 800 as defined by a DC or AC reference voltage. The transistor switch element S_{R1} and inductors L_{G2} and L_{OUT} provide a synchronous rectifier in the DC-DC power converter 800 and replaces the diode based asynchronous rectifier circuit 413 discussed above. Since the control input, e.g. the gate drive signal, of the switching network of the present class E and DE resonant power converters does not need a traditional PWM or PDM type of control signal (but only the two adjustable bias voltage V_{Bias1} and V_{Bias2}), the resonant power converters in accordance with the present embodiments are generally very well suited for synchronous rectification as illustrated on FIG. 8 for this particular embodiment. The traditional PWM or PDM type of control signals are not required because is not necessary to control a phase between the respective control input signals of the first transistor switch S_1 and the rectification transistor switch S_{R1}. The rectification transistor switch S_{R1} may for example be coupled to a suitable fixed rectifier DC bias voltage V_{Bias2} applied to the inductor L_{G2} coupled to the gate (i.e. control input) of S_{R1}. For rectification purposes, the gate terminal of S_{R1} is driven by an oscillation output voltage, i.e. the drain voltage V_{DS}, of the first semiconductor switch S_1 to automatically maintain synchronous operation between S_1 and SR1. This absence of the traditional PWM or PDM type of control signals on the respective gate terminals of the first transistor switch S_1 and rectification transistor switch S_{R1} is a significant advantage leading to simplified power converter design and smaller component count. In isolated power converter applications, the present diode based asynchronous rectifier circuit 413 possess an additional advantage because it eliminates the need for transmitting or communicating the traditional PWM or PDM type control signal or signals across a voltage isolation barrier of the resonant power converter. This type of voltage isolation barrier will typically require expensive and space consuming components like optocouplers or fast transformers in traditional power converter topologies. As illustrated by FIG. 8, the present DC-DC power converter with synchronous rectification may be completely symmetrical in terms of circuit topology across a series resonant network comprising resonant ca-

pacitor C_R and resonant inductor L_R allowing for bidirectional power flow between the DC input power source V_{IN} 804 and the output voltage at V_{OUT}. The skilled person will appreciate that the input transistor switch S_1 and rectifier transistor switch S_{R1} may be substantially identical or different components and the same applies to the fixed inductance inductors L_{G2} and L_{G1} depending on factors such as the voltage conversion ratio of the resonant power converter.

The skilled person will appreciate that the above-described synchronous rectifier may be added to each of the above discussed class E and DE resonant power converter embodiments depicted above on FIG. 1B), FIGS. 2A)-2B) and FIGS. 3A)-3B).

CLAIMS

1. A resonant power converter comprising:
an input terminal for receipt of an input voltage,
a switching network comprising one or more semiconductor switches controlled by respective control inputs,
the switching network comprising a switch input operatively coupled to the input terminal for receipt of the input voltage and a switch output operatively coupled to an input of a resonant network of the resonant power converter,
the resonant network comprising a predetermined resonance frequency (f_R) and an output operatively coupled to a converter output terminal,
a self-oscillating feedback loop coupled from the switch output to a control input of the switching network to set a switching frequency of the power converter;
the self-oscillating feedback loop comprising:
a first intrinsic switch capacitance coupled between the switch output and the control input of the switching network,
a first bias voltage source configured to generate a first adjustable bias voltage,
a first inductor with substantially fixed inductance coupled in-between the first bias voltage source and the control input of the switching network,
a voltage regulation loop configured to control an output voltage of the power converter by controlling the first adjustable bias voltage applied to the first inductor.

2. A resonant power converter according to claim 1, comprising:
an input inductor coupled between the input terminal and the switch input,
the switching network comprising a first semiconductor switch with a control terminal coupled to the control input of the switching network and an output terminal coupled to the switch input and to the switch output.

3. A resonant power converter according to claim 2, wherein the input inductor and the first inductor are magnetically coupled with a predetermined magnetic coupling coefficient, preferably a magnetic coupling coefficient larger than 0.1 or even more preferably larger than 0.4.

4. A resonant power converter according to claim 1, wherein the switching network comprises:
a first semiconductor switch coupled between the switch output and a voltage supply rail of the resonant power converter and having a control terminal coupled to the control input of the switching network,
a second semiconductor switch coupled between the switch output and the input terminal; and
wherein a control terminal of the second semiconductor switch is coupled to a second bias voltage source through a cascade of a second inductor with substantially fixed inductance and a third inductor with substantially fixed inductance,
and wherein a feedback capacitor is coupled between the switch output and an intermediate node between the second and third inductors.

5. A resonant power converter according to claim 4, wherein the first inductor and the third inductor are magnetically coupled with a predetermined magnetic coupling coefficient, preferably a magnetic coupling coefficient larger than 0.1 or even more preferably larger than 0.4.

6. A resonant power converter according to claim 3 or 5, wherein the input inductor and the first inductor are wound around a common magnetically permeable member of core; or
the first inductor and the third inductor are wound around a common magnetically permeable member or core.

7. A resonant power converter according to any of the preceding claims, wherein the first bias voltage source comprises:
a capacitor coupled from the first adjustable bias voltage and a fixed electric potential of the resonant power converter such as ground,
a first adjustable resistor coupled between the first adjustable bias voltage and a first DC reference voltage,
a second adjustable resistor coupled between the first adjustable bias voltage and a second DC reference voltage.

8. A resonant power converter according to any of the preceding claims, wherein the voltage regulation loop comprises:
a reference voltage generator supplying a reference DC or AC voltage to a first input of a comparator,
a second input of the comparator being coupled to the converter output voltage,
an output of the of the comparator operatively coupled to a control input of the first bias voltage source.

9. A resonant power converter according to any of the preceding claims, wherein the first inductor has an inductance between 1 nH and 10 µH such as between 1 nH and 50 nH.

10. A resonant power converter according to any of the preceding claims, wherein the substantially fixed inductance of the first inductor is set such that a peak voltage at the control input of the switching network exceeds a threshold voltage of at a semiconductor switch of the switching network.

11. A resonant power converter according to claim 10, wherein the substantially fixed inductance of the first inductor is selected such that a peak-peak voltage swing at the control input of the switching network is approximately equal to a numerical value of the threshold voltage of the at least one of the semiconductor switches of the switching network.

12. A resonant power converter according to any of the preceding claims, wherein the self-oscillating feedback loop further comprises:
a series resonant circuit coupled in-between the control input of the switching network and a fixed electric potential of the power converter.

13. A resonant power converter according to claim 12, wherein the self-oscillating feedback loop further comprises:
a first series resonant circuit coupled in-between the control input of the first semiconductor switch and fixed electric potential of the converter such as a positive or negative DC supply voltage or a ground voltage,

a second series resonant circuit coupled in-between the control input of the first semiconductor switch and the switch output.

14. A resonant power converter according to any of the claims 1-11, wherein the self-oscillating feedback loop further comprises:
a parallel resonant circuit coupled in series with the first inductor in-between the first adjustable bias voltage and the first inductor.

15. A resonant power converter according to any of the preceding claims, further comprising:
a rectifier coupled between the output of the resonant network and the converter output terminal to provide a rectified DC output voltage.

16. A resonant power converter according to claim 15, wherein the rectifier comprises a synchronous rectifier.

17. A resonant power converter according to claim 16, wherein the synchronous rectifier comprises:
a rectification semiconductor switch configured to rectify an output voltage of the resonant network in accordance with a rectifier control input of the rectification semiconductor switch,
a first rectification inductor with a substantially fixed inductance coupled in-between a fixed or adjustable rectifier bias voltage and the rectifier control input.

18. A resonant power converter according to claim 17, wherein the fixed or adjustable rectifier bias voltage is coupled to a fixed DC bias voltage source or to the rectified DC output voltage through a resistive or capacitive voltage divider.

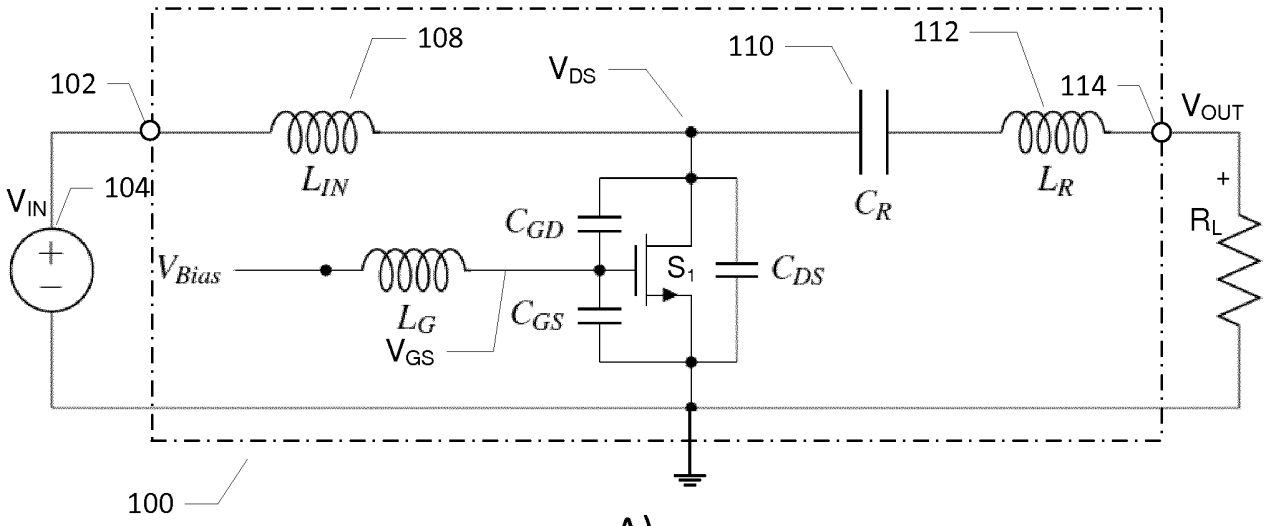
19. A resonant power converter according to any of claims 2-18, wherein one of the first and second semiconductor switches comprises a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET.

20. A resonant power converter assembly comprising:
a resonant power converter according to any of the preceding claims,

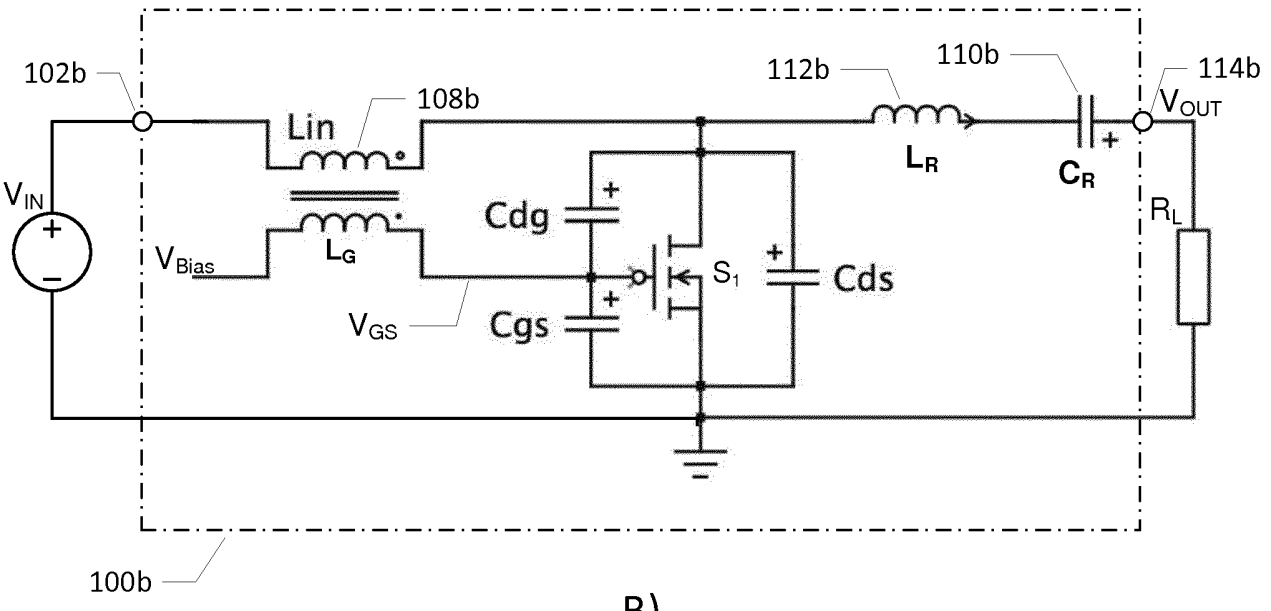
a carrier substrate having at least the switching network and the resonant circuit integrated thereon,

an electrical trace pattern of the carrier substrate forming the first inductor.

21. A resonant power converter assembly according to claim 16, wherein the carrier substrate comprises a semiconductor die.

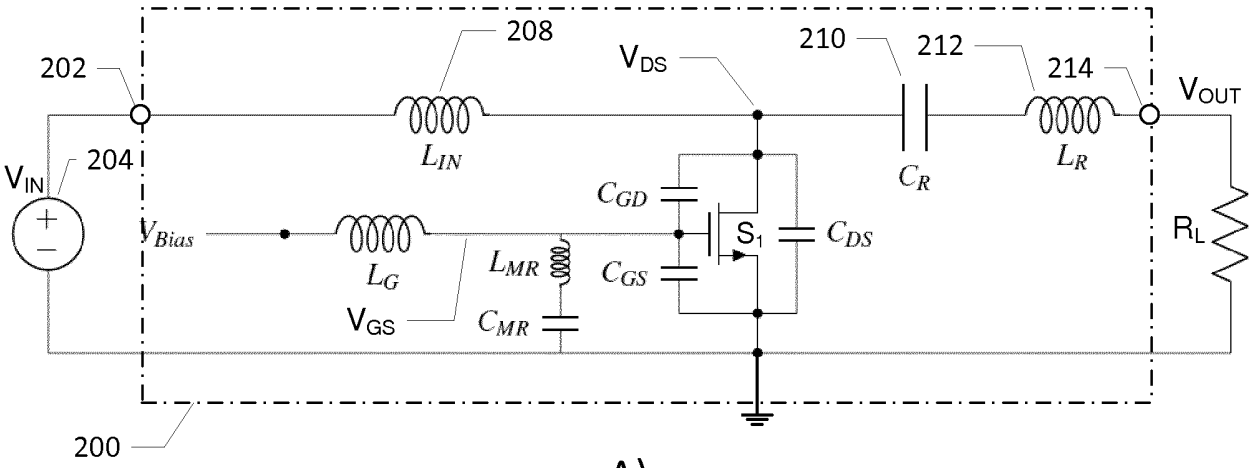

102
108
V_{DS}
110
112
114
V_{OUT}
V_{IN}
104
L_{IN}
C_{GD}
C_R
L_R
R_L
V_{Bias}
S_1
C_{DS}
L_G
C_{GS}
V_{GS}
100

A)

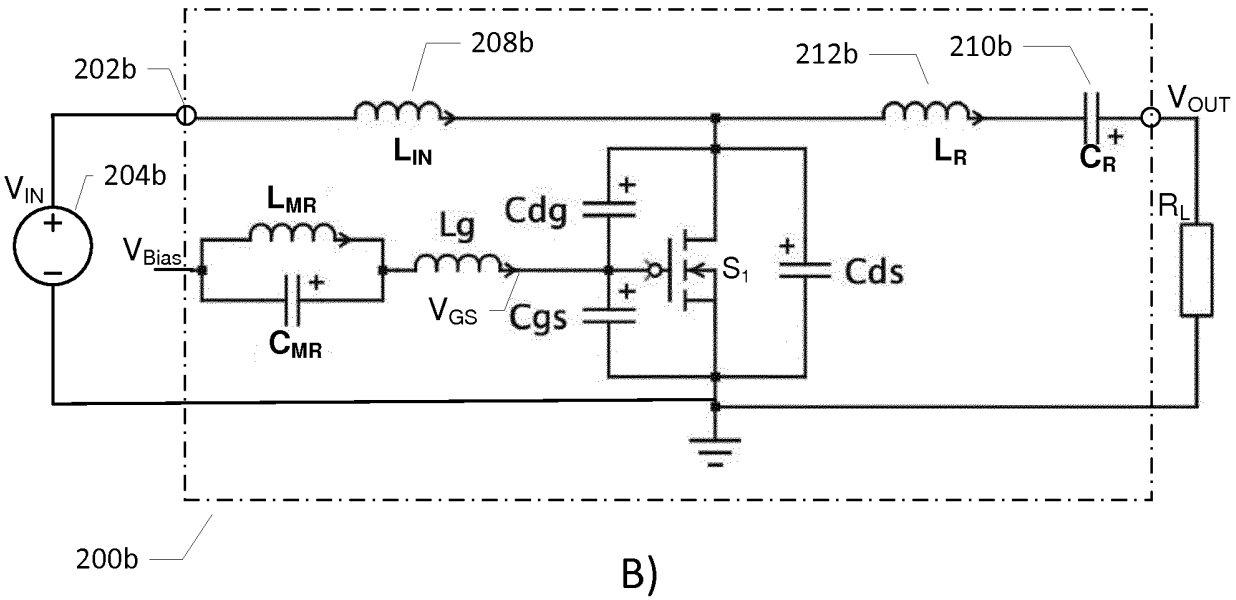

102b
112b
110b
114b
V_{OUT}
Lin
108b
L_R
C_R
V_{IN}
R_L
Cdg
V_{Bias}
L_G
S_1
Cds
V_{GS}
Cgs
100b

B)

FIGS. 1A, B

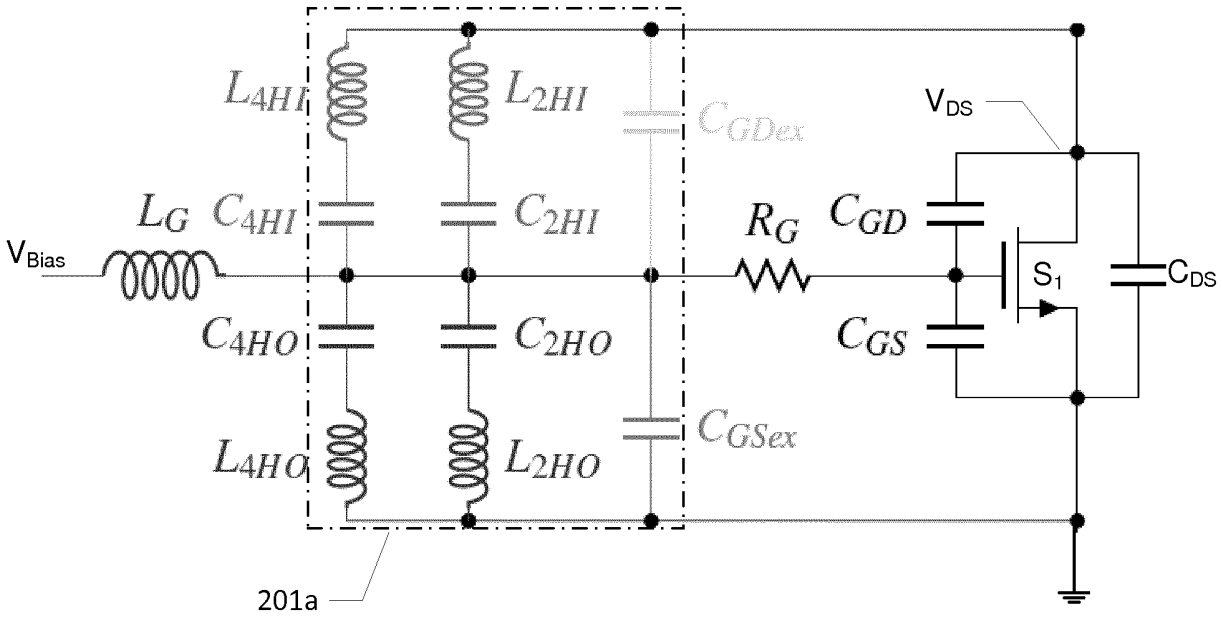

202
208
V_{DS}
210
212
214
V_{OUT}
V_{IN}
204
L_{IN}
C_R
L_R
C_{GD}
V_{Bias}
L_G
L_{MR}
C_{GS}
S_1
C_{DS}
R_L
V_{GS}
C_{MR}
200

A)


202b
208b
212b
210b
V_{OUT}
V_{IN}
204b
L_{IN}
L_R
C_R
L_{MR}
Lg
Cdg
R_L
V_{Bias}
S_1
Cds
V_{GS}
Cgs
C_{MR}
200b

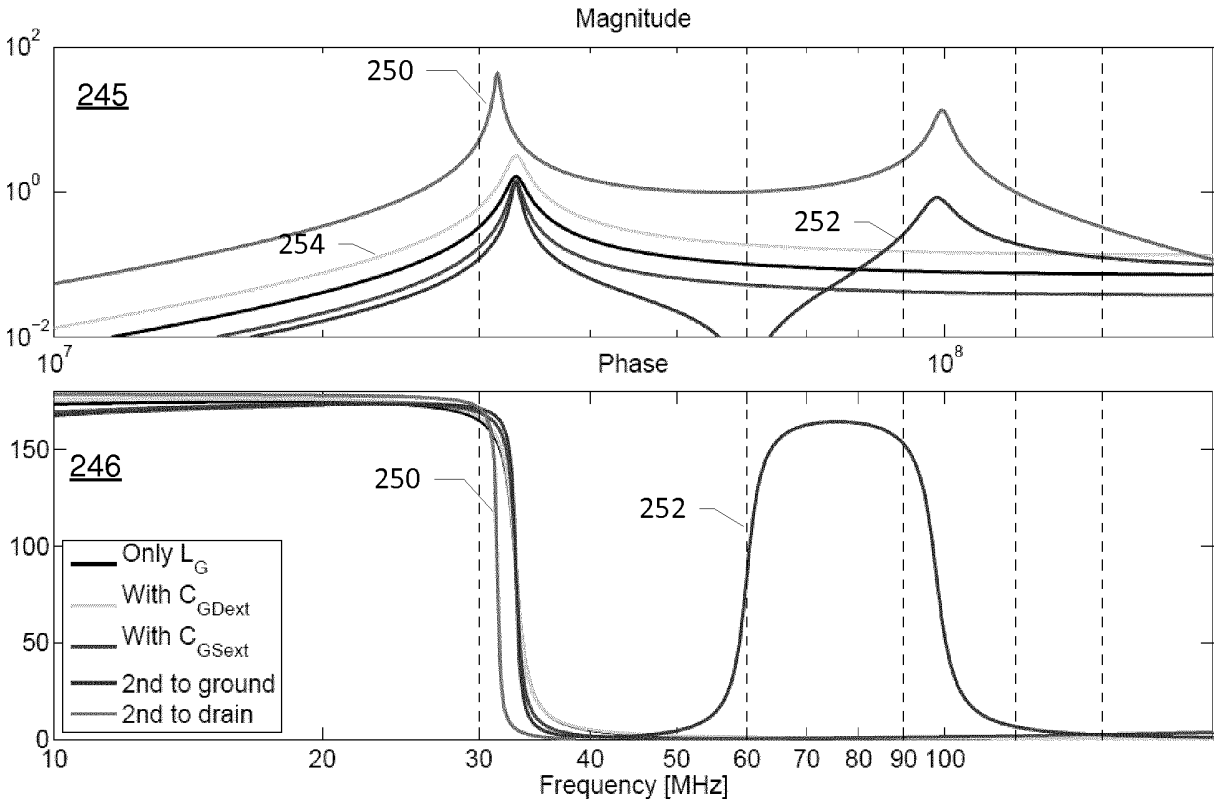
B)

FIGS. 2A, B

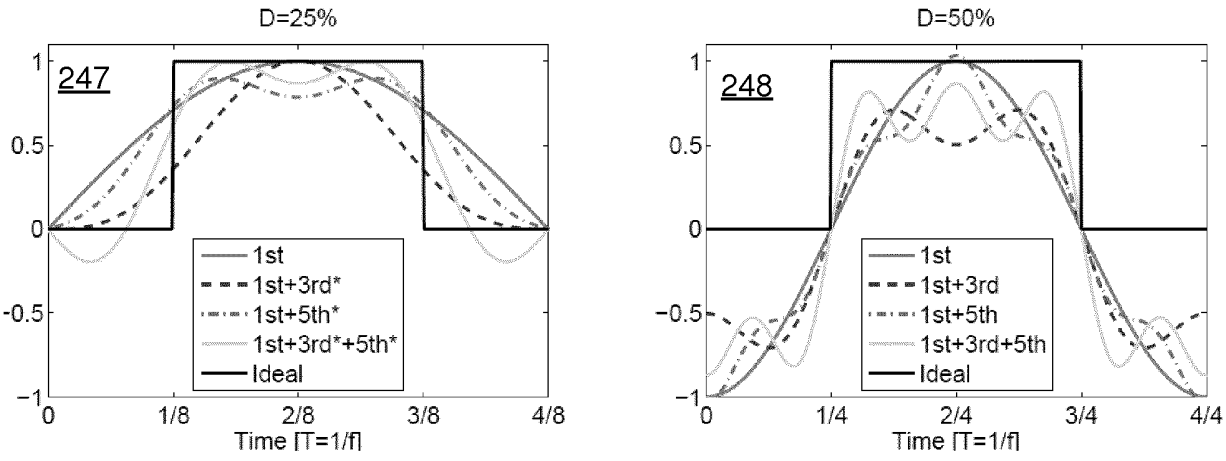

L_{4HI}
L_{2HI}
C_{GDex}
V_{DS}
L_G
C_{4HI}
C_{2HI}
R_G
C_{GD}
V_{Bias}
S_1
C_{DS}
C_{4HO}
C_{2HO}
C_{GS}
C_{GSex}
L_{4HO}
L_{2HO}
201a

C)

FIG. 2C

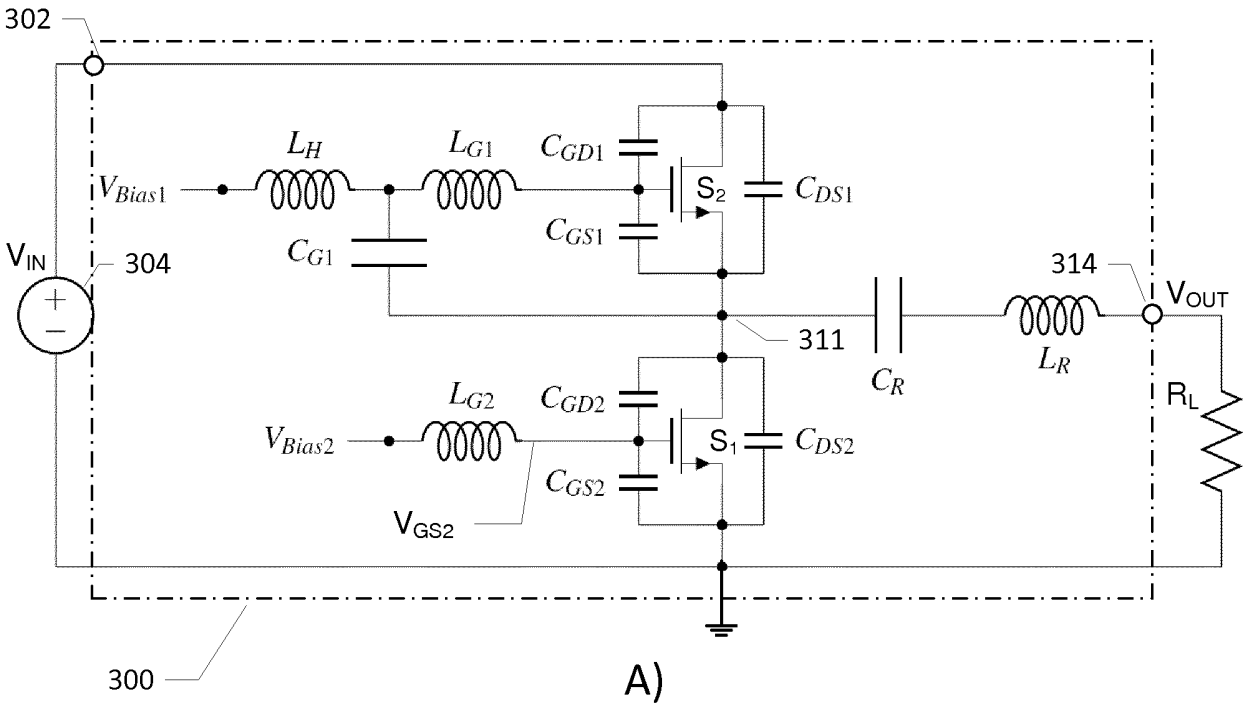

Magnitude
245
250
254
252
Phase
246
250
252
Only L_G
With C_{GDext}
With C_{GSext}
2nd to ground
2nd to drain
Frequency [MHz]

D)

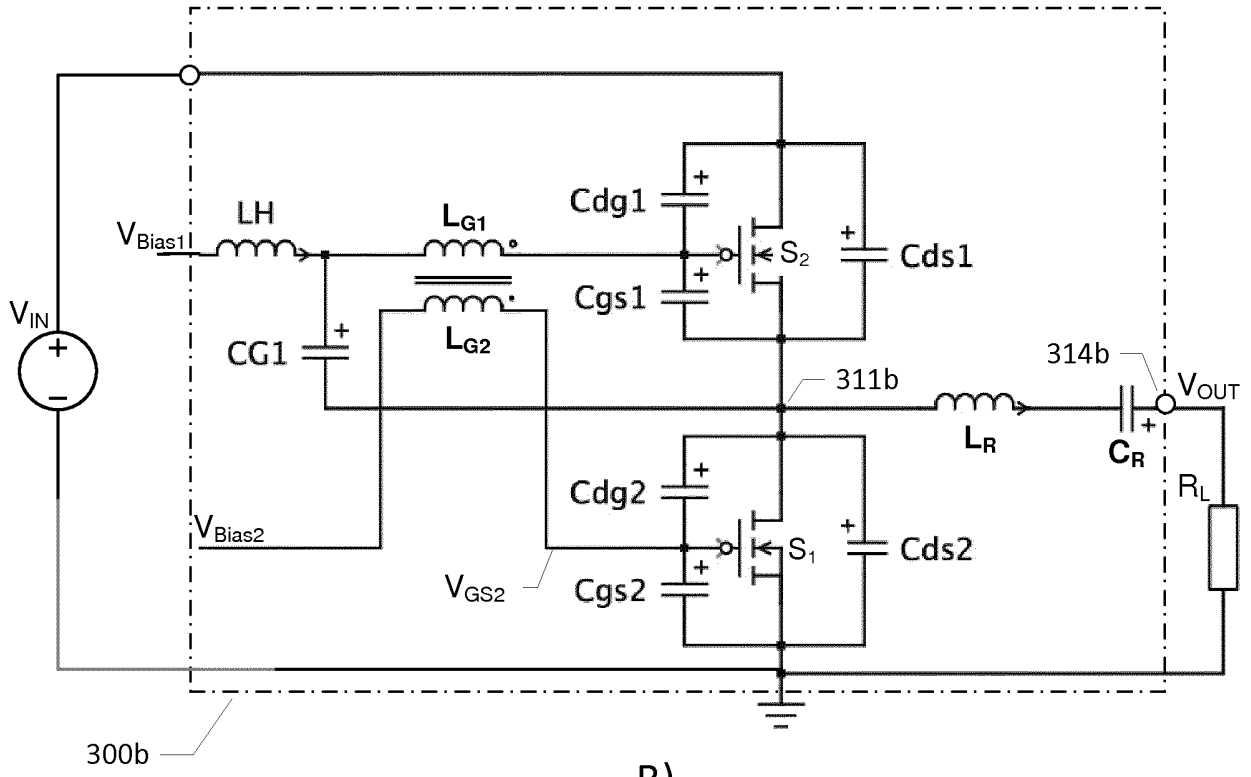

D=25%
247
1st
1st+3rd*
1st+5th*
1st+3rd*+5th*
Ideal
Time [T=1/f]
D=50%
248
1st
1st+3rd
1st+5th
1st+3rd+5th
Ideal
Time [T=1/f]

E)

FIGS. 2D, E


302
L_H
L_{G1}
C_{GD1}
V_{Bias1}
S_2
C_{DS1}
C_{GS1}
C_{G1}
V_{IN}
304
314
V_{OUT}
311
C_R
L_R
L_{G2}
C_{GD2}
R_L
V_{Bias2}
S_1
C_{DS2}
C_{GS2}
V_{GS2}
300

A)


LH
L_{G1}
Cdg1
V_{Bias1}
S_2
Cds1
Cgs1
V_{IN}
CG1
L_{G2}
311b
314b
V_{OUT}
L_R
C_R
Cdg2
R_L
V_{Bias2}
S_1
Cds2
V_{GS2}
Cgs2
300b

B)

FIGS. 3A, B

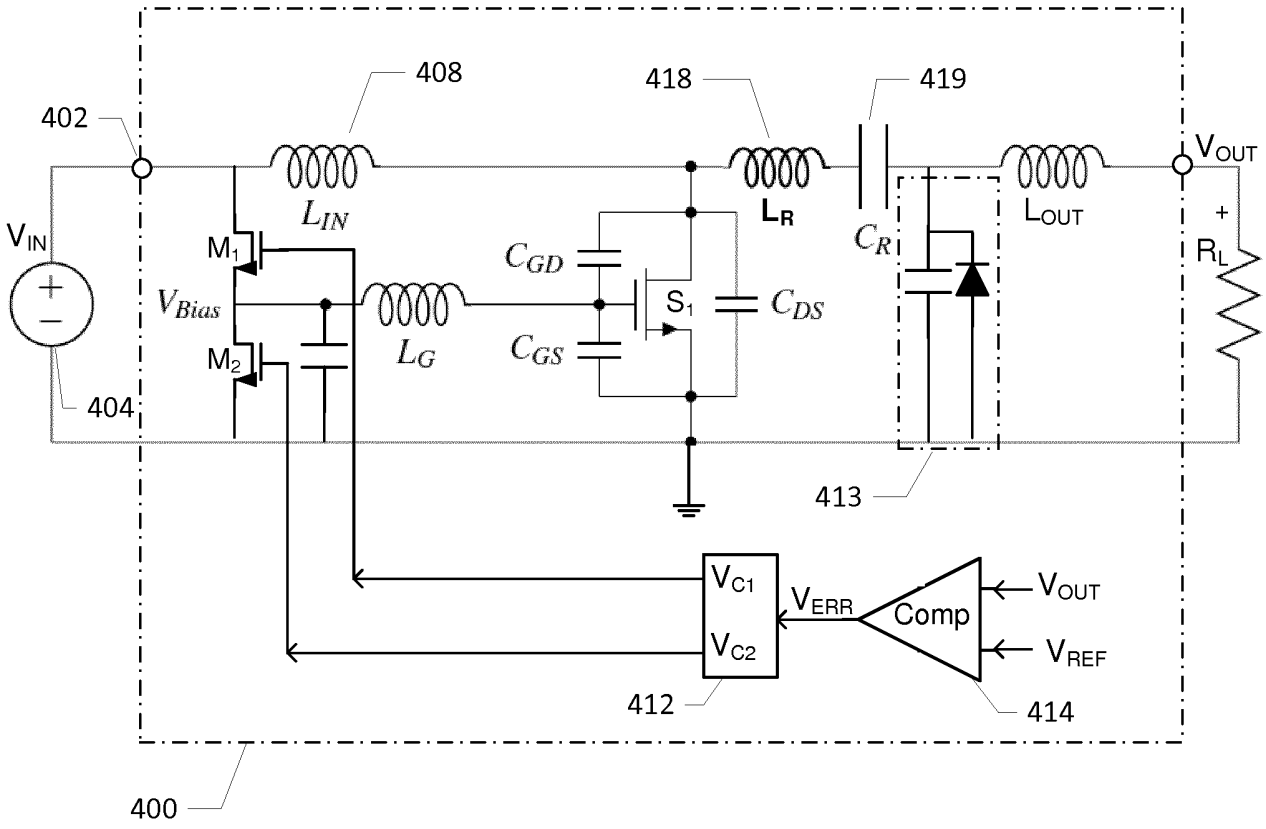

408
418
419
402
V_{OUT}
L_{IN}
L_R
C_R
L_{OUT}
V_{IN}
M_1
C_{GD}
S_1
C_{DS}
V_{Bias}
L_G
C_{GS}
M_2
R_L
404
413
V_{C1}
V_{ERR}
Comp
V_{OUT}
V_{C2}
V_{REF}
412
414
400

FIG. 4

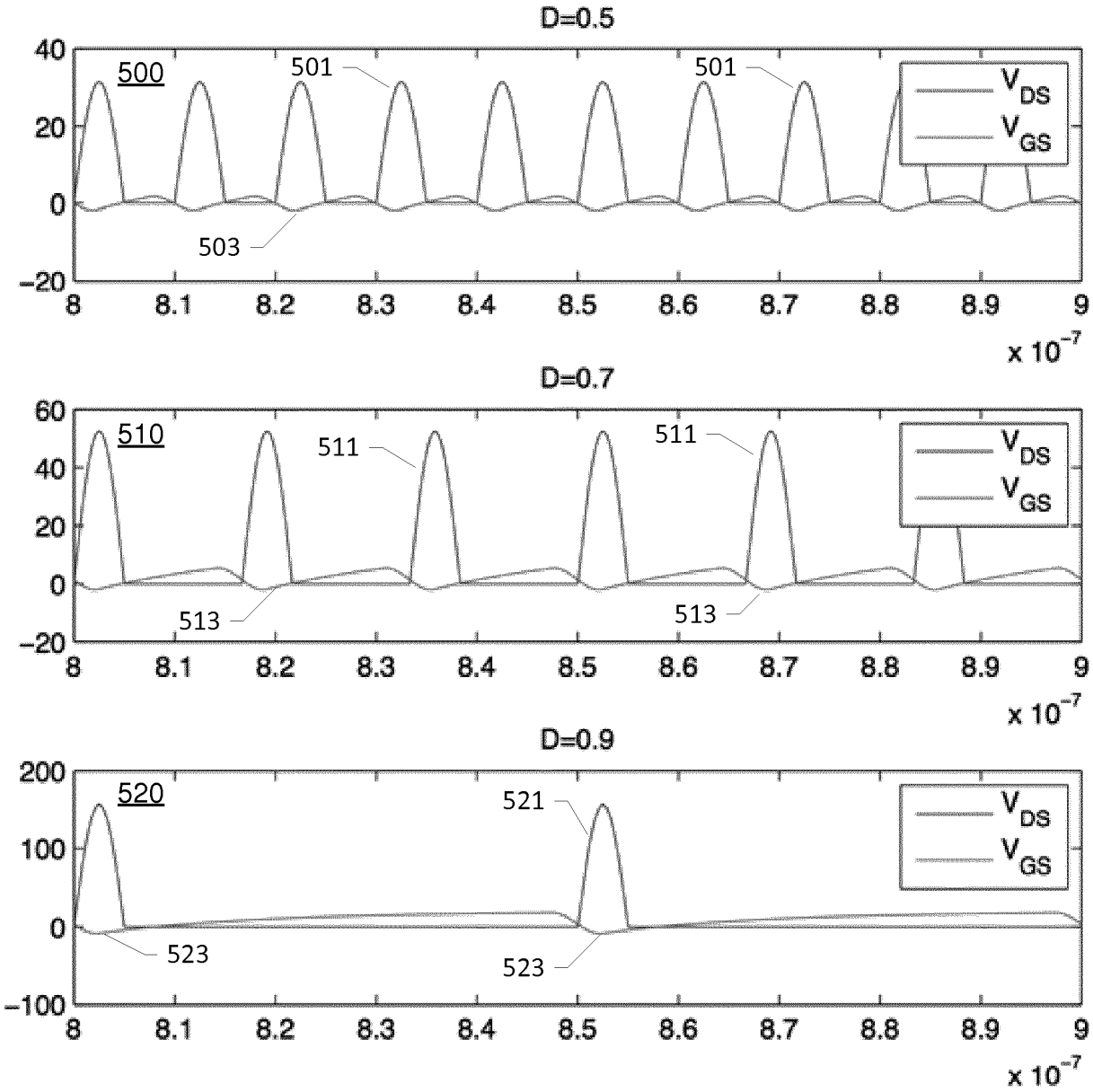
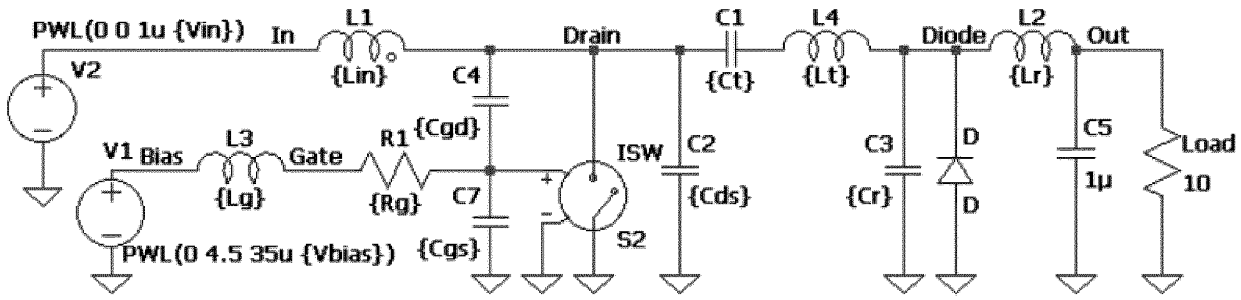

D=0.5
500
501
501
503
V_{DS}
V_{GS}
40
20
0
−20
8
8.1
8.2
8.3
8.4
8.5
8.6
8.7
8.8
8.9
9
x 10^{-7}
D=0.7
510
511
511
513
513
60
40
20
0
−20
D=0.9
520
521
523
523
200
100
0
−100

FIG. 5




```
.param Vin=50
.param Lin 1u
.param Cds 26p
.param Cgd 10p
.param Cgs 80p
.param Rg 1.5
.param Ct 1n
.param Lt 250n
.param Lg 68n
.param Lr 30n
.param Cr 80p
```

```
.tran 0 50u
.step param Vbias LIST -7 -2 3 8

.model ISW SW(Ron=1 Roff=1Meg Vt=4.5 Vh=-0.5)


    .model D D
```

FIG. 6

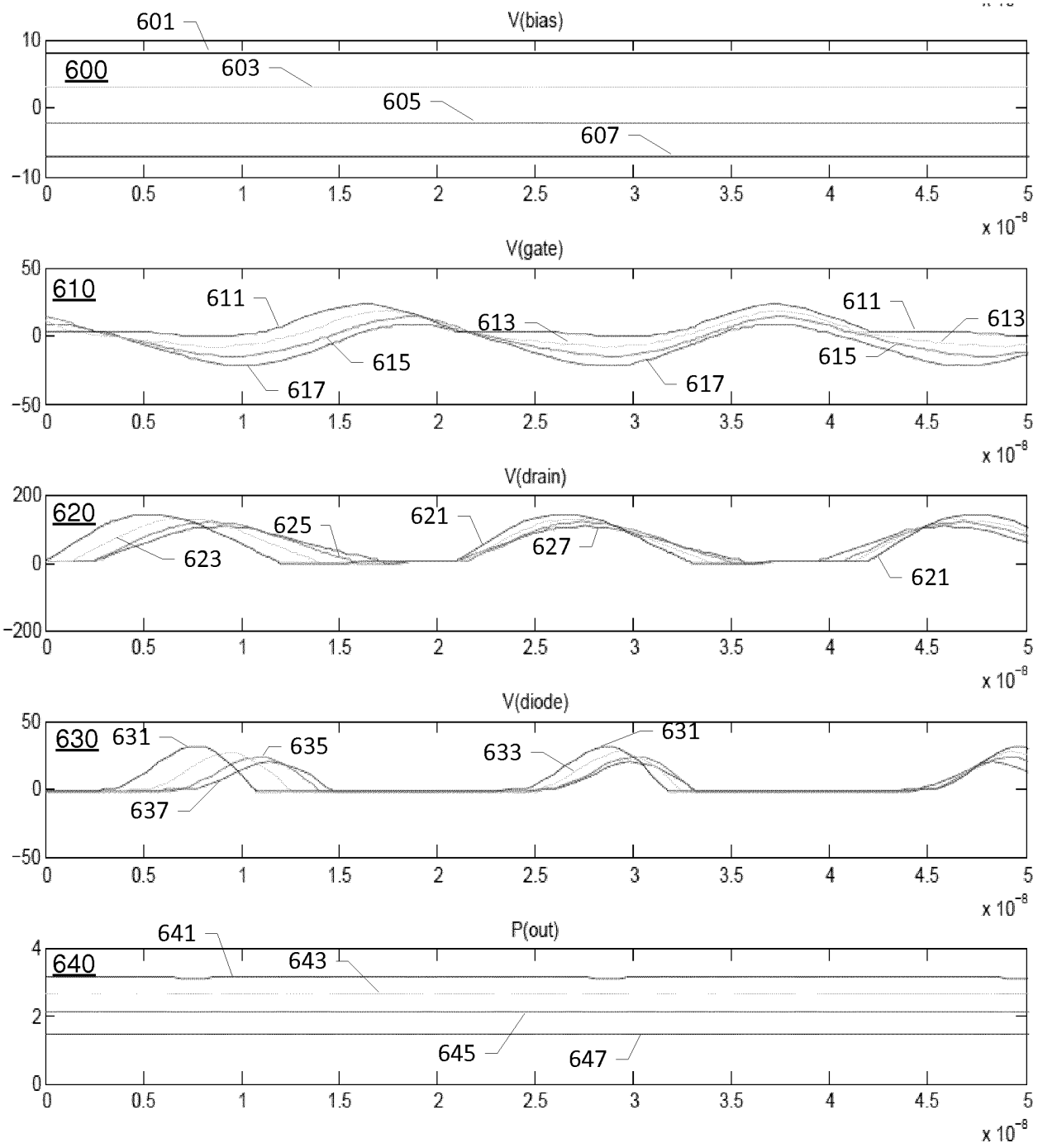

V(bias)
601
600
603
605
607
V(gate)
610
611
613
615
617
V(drain)
620
623
625
621
627
V(diode)
630
631
635
637
633
P(out)
641
640
643
645
647
x 10^-8

FIG. 7

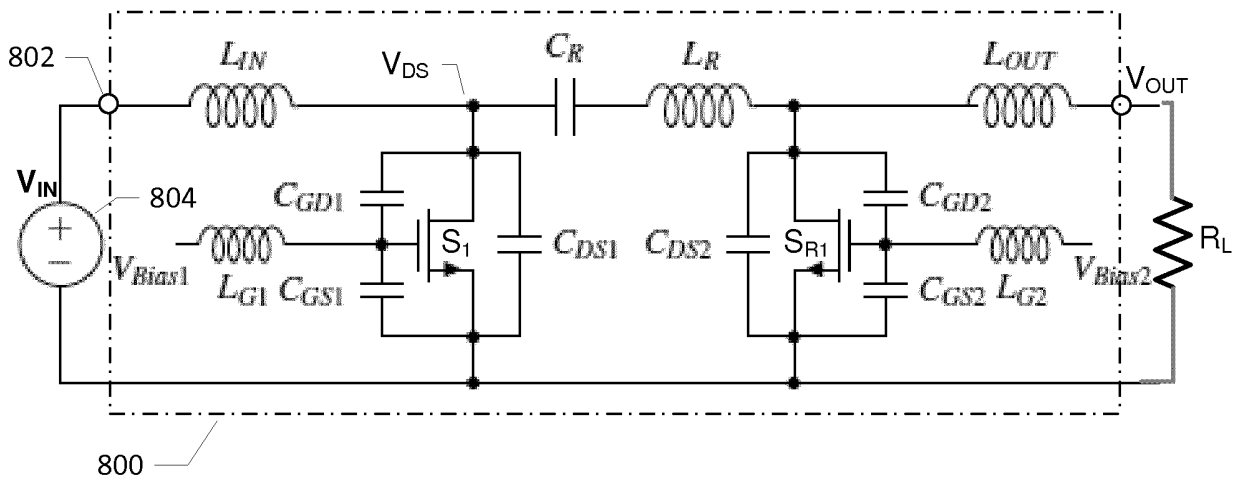

802
L_{IN}
V_{DS}
C_R
L_R
L_{OUT}
V_{OUT}
V_{IN}
804
C_{GD1}
C_{GD2}
S_1
C_{DS1}
C_{DS2}
S_{R1}
R_L
V_{Bias1}
L_{G1} C_{GS1}
C_{GS2} L_{G2}
V_{Bias2}
800

FIG. 8

A.13 **M. Madsen, A. Knott, M. A.E. Andersen, A. P. Mynster:**
***"Printed Circuit Board Embedded Inductors for Very High Frequency Switch-Mode Power Supplies"*,**
IEEE Energy Conversion Congress and Exhibition Asia DownUnder, Melbourne, Australia, June 2013. Conference Proceedings p1071-1078.

Printed Circuit Board Embedded Inductors for Very High Frequency Switch-Mode Power Supplies

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Email: apm@delta.dk

***Abstract*—The paper describes the design of three different structures for printed circuit board embedded inductors. Direct comparison of spirals, solenoids and toroids are made with regard to inductance, dc and ac resistance, electromagnetic field and design flexibility.**

First the equations for the impedances are given and an example of the achievable impedances are given. Prototypes are then made and measured. The differences between the three structures and the accuracy of the formulas are evaluated.

Finite element simulations are used to investigate the magnetic field around the structure, in order to take possible electromagnetic interference problems into account, when the structures are compared. The simulated fields are verified through near field measurements performed on the prototypes.

Finally deign flexibility are considered, both regarding scalability and design of the individual inductors and implementation in a complete design. At the end of the paper a summary of pros and cons of the three structures are listed.

I. Introduction

The constant strive for small, cheap and efficient power supplies firstly lead to the development of Switch-Mode Power Supplies (SMPS) in the early 70s [1]. Since this strive has lead to constantly increasing switching frequencies, as the size of modern power supplies are mainly governed by the passive energy storing elements, which scales inversely with the switching frequency.

Commercially available converters today switch at frequencies up to several mega hertz and can have efficiencies of more than 95% (e.g. [2]).

The reason not to increasing the switching frequency even higher and thereby reaching even higher power densities is the switching losses. However with the use a soft switching techniques and resonant converters, SMPSs with switching frequencies in the Very High Frequency range (VHF, 30-300MHz) have been designed with efficiencies up to approx. 90%, [3] and [4].

This highly increased switching frequency has several pros and cons which has been discussed in various publication, e.g. [5]. One of the challenges is to design high-Q inductors, as most magnetic materials are limited to operation up to a few megahertz. With the high frequency, the inductance needed is however also lowered significantly and it is hence possible to use relatively small air core inductors. So far the type of inductor most commonly used is an air core solenoid.

Given the small inductance, the inductors can however also be designed as Printed Circuit Board (PCB) embedded inductors. Several structures for the design of these inductors exist and many of them have been described several times in previous publication, e.g. [6], [7] and [8]. Spiral inductors are commonly used in Integrated Circuits (ICs) and hence several publications with design guides for these exists ([9], [10] and [11]). Though discrete air core solenoid are commonly used, solenoids are not as common for embedded inductors. Some publications are however available showing inductors with Q values of up to more than 300 ([12] and [13]).

Both spirals and solenoids have strong external magnetics fields. This make them likely to cause Electromagnetic Interference (EMI) problems, either by direct radiation or by coupling to nearby metallic structures such as cables and other circuit boards. The fields have been described for spirals in [6] and for solenoids and toroids in [7]. The external field from the toroid is much weaker than for the two other structures. For this reason the design of this structure has been investigated in [6], [14] and [15].

Though the three structures have been described in several publications, no direct comparison have been made. In this paper this comparison will be made, the paper hence describes the three different structures for PCB embedded inductors; solenoids, spirals and toroids (see Fig 1). In section two, formulas for calculating the inductance and Equivalent Series Resistance (ESR) are given. The formulas are then verified through impedance measurements in section four. Finite Element (FEM) simulations are described in section three and used to investigate the magnetic fields. These are verified via near field measurements in section five. Section six list pros and cons of the different structures and finally section seven concludes the paper.

II. Parameter Calculations

Equations for the inductance and ESR of the three types of inductors are given in the following subsections. Equations for the capacitance and resonance frequency are not given, as accurate formulas are not available and derivation of these is outside the scope of this paper.

The inductors are evaluated for use in VHF SMPS and for this purpose the inductance will usually not be more than

maximum a few hundred mega hertz, the size small and the frequency up to around 100MHz. In this case the capacitance is relatively small, hence the self-resonance frequency becomes high and exact knowledge of these are hence not crucial.

A. Spirals

The spirals are designed as archimedean spirals, i.e. with constant trace width and a constant distance between the traces. The length of the trace in an arcimedean spiral can be calculated according to eq. 1 with the assumption that $1+2+3+...+N = N \cdot \frac{N+1}{2}$

$$l_{TRACE} = \pi \cdot N_{TURNS} \frac{D+d}{2} = \pi \frac{D^2 - d^2}{4 \cdot T_{TRACE}} \quad (1)$$

Here N_{TURNS} is the number of turns, T_{TRACE} is the thickness of the copper and D and d is the outer and inner diameter, respectively. MATLAB has been used to design the inductors, here the function pdist2 can be used to get a more accurate length when the coordinates for the trace are known.

Now that trace length is know the dc resistance is simply calculated from eq. 2. If a two layer spiral is made, the resistance of course has to be doubled and the resistance of the via has to be added. The ac resistance, caused by the skin effect, of a planar inductor can, according to [16], be approximated by eq. 3.

$$R_{DC} = \frac{\rho \cdot l_{TRACE}}{W_{TRACE} \cdot T_{TRACE}} \quad (2)$$

$$R_{AC} = \frac{\rho \cdot l_{TRACE}}{W_{TRACE} \cdot \delta(1 - e^{T_{TRACE}/\delta})} \quad (3)$$

Here ρ is the electrical resistivity of copper, W_{TRACE} is the width of a trace and δ is the skin depth.

The inductance of a spiral can be calculated by eq. 4 [17]. Here c_1 and c_2 are constants of 2.46 and 0.20, respectively, and p is a fill ratio defined as $p = \frac{D-d}{D+d}$.

$$L = \frac{\mu \cdot N_{TURNS}^2 \frac{D+d}{2}}{2} \left(ln\left(\frac{c_1}{p}\right) + c_2 \cdot p^2 \right) \quad (4)$$

B. Solenoids

In order to calculate the resistance of a solenoid, the structure is split in two; the vias and the traces. The dc resistance of a single via and a single trace, can now be calculated according to eq. 5 and 6, respectively.

$$R_{DC,VIA} = \frac{\rho \cdot T_{PCB}}{A_{VIA}} = \frac{\rho \cdot T_{PCB}}{\pi \cdot T_{VIA}(D_{VIA} - T_{VIA})} \quad (5)$$

$$R_{DC,TRACE} = \frac{\rho \cdot W_L}{W_{TRACE} \cdot T_{TRACE}} \quad (6)$$

Here T_{PCB} is the thickness of the PCB, A_{VIA} is the area of a cross section of a via, D_{VIA} is the via diameter, T_{VIA} is the thickness of the copper in a via and W_L is the width of the inductor.

The total dc resistance can then be calculated as the sum of all the vias and traces. Using multiple vias in parallel for each turn will lower the total resistance. If this is done the total resistance can be calculated according to eq. 7. Here N_{VIAS} is the number of parallel vias in a single turn.

$$R_{DC} = 2 \cdot N_{TURNS} \left(\frac{R_{DC,VIA}}{N_{VIAS}} + R_{DC,TRACE} \right) \quad (7)$$

The ac resistance is calculated as a first order approximation of the skin effect, hence neglecting the proximity effect. This will not give exact results, but it ease the comparison of the three structures and is sufficient for evaluation of pros and cons of each structure.

It is assumed that the ac current will run along the inner edge of the solenoid, hence along the inner edge of the traces and the inner edge of the inner half of the vias. This assumption will be verified through FEM simulations. Using this assumption and the skin depth, the ac resistance is calculated according to eq. 8.

$$R_{AC} = 2 \cdot N_{TURNS} \left(\frac{R_{AC,VIA}}{N_{VIAS}} + R_{AC,TRACE} \right) \quad (8)$$

Where:

$$R_{AC,VIA} = \frac{\rho \cdot T_{PCB}}{A_{VIA}} = \frac{2 \cdot \rho \cdot T_{PCB}}{\pi \cdot \delta(D_{VIA} - \delta)}$$

$$R_{AC,TRACE} = \frac{\rho \cdot W_L}{W_{TRACE} \cdot \delta}$$

The inductance of the solenoid can be calculated according to Niwas formula [18]. In eq. 9, L_L is the length of the inductor and g is the square of the hypotenuse of a cross section of the inductor given by; $g^2 = W_L^2 + T_{PCB}^2$

$$\begin{aligned} L = {} & 8e^{-9} \cdot N_{TURNS}^2 \frac{W_L \cdot T_{PCB}}{L_L} \Bigg[\frac{1}{2} \frac{L_L}{T_{PCB}} sinh^{-1} \frac{T_{PCB}}{L_L} \\ & + \frac{1}{2} \frac{L_L}{W_L} sinh^{-1} \frac{T_{PCB}}{L_L} \\ & - \frac{1}{2} \left(1 - \frac{T_{PCB}^2}{L_L^2}\right) \frac{L_L}{T_{PCB}} sinh^{-1} \frac{W_L}{L_L \sqrt{1 + T_{PCB}^2/L_L^2}} \\ & - \frac{1}{2} \left(1 - \frac{W_L^2}{L_L^2}\right) \frac{L_L}{W_L} sinh^{-1} \frac{T_{PCB}}{L_L \sqrt{1 + W_L^2/L_L^2}} \\ & - \frac{1}{2} \frac{T_{PCB}}{L_L} sinh^{-1} \frac{W_L}{T_{PCB}} - \frac{1}{2} \frac{W_L}{L_L} sinh^{-1} \frac{T_{PCB}}{W_L} \\ & + \frac{\pi}{2} - tan^{-1} \frac{W_L \cdot T_{PCB}}{L_L^2 \sqrt{1 + g^2/L_L^2}} \\ & + \frac{1}{3} \frac{L_L^2}{W_L \cdot T_{PCB}} \sqrt{1 + \frac{g^2}{L_L^2}} \left(1 - \frac{1}{2} \frac{g^2}{L_L^2}\right) + \frac{1}{3} \frac{L_L^2}{W_L \cdot T_{PCB}} \\ & - \frac{1}{3} \frac{L_L^2}{W_L \cdot T_{PCB}} \sqrt{1 + \frac{W_L^2}{L_L^2}} \left(1 - \frac{1}{2} \frac{W_L^2}{L_L^2}\right) \\ & - \frac{1}{3} \frac{L_L^2}{W_L \cdot T_{PCB}} \sqrt{1 + \frac{T_{PCB}^2}{L_L^2}} \left(1 - \frac{1}{2} \frac{T_{PCB}^2}{L_L^2}\right) \\ & + \frac{1}{6} \frac{L_L^2}{W_L \cdot T_{PCB}} \left(\frac{g^2 - W_L^2 - T_{PCB}^2}{L_L^2} \right) \Bigg] \end{aligned} \quad (9)$$

C. Toroids

A toroid is simply a solenoid bend in a circle, hence the same procedure and some of the assumption can be used again. It is thus assumed that the current run along the inner edges and the toroid is split into slabs and vias to get the resistance. The dc resistance of a slab is determined by integration from the inner radius to the outer radius [14].

$$R_{DC,SLAB} = \int_{r_I}^{r_O} \frac{\rho}{T_{TRACE}\left(\frac{2\cdot\pi\cdot r}{N_{TURNS}} - C_{TRACE}\right)}$$

$$= \frac{\rho \cdot N_{TURNS}}{2\cdot\pi\cdot T_{TRACE}} ln\left(\frac{2\cdot\pi\cdot r_O - C_{TRACE}\cdot N_{TURNS}}{2\cdot\pi\cdot r_I - C_{TRACE}\cdot N_{TURNS}}\right) \quad (10)$$

Here C_{TRACE} is the clearance between to slabs and r_I and r_O are the inner and outer radius, respectively. As for the solenoid a first order approximation of the skin effect is used for the ac resistance, hence this simply becomes:

$$R_{AC,SLAB} = \int_{r_I}^{r_O} \frac{\rho}{\delta\left(\frac{2\cdot\pi\cdot r}{N_{TURNS}} - C_{TRACE}\right)}$$

$$= \frac{\rho \cdot N_{TURNS}}{2\cdot\pi\cdot\delta} ln\left(\frac{2\cdot\pi\cdot r_O - C_{TRACE}\cdot N_{TURNS}}{2\cdot\pi\cdot r_I - C_{TRACE}\cdot N_{TURNS}}\right) \quad (11)$$

The resistance of the vias are the same as for the solenoid and the total resistance becomes:

$$R_{DC} = N_{TURNS}\left(2\cdot R_{DC,SLAB} + \frac{R_{DC,VIA}}{N_{INNER}} + \frac{R_{DC,VIA}}{N_{OUTER}}\right) \quad (12)$$

$$R_{AC} = N_{TURNS}\left(2\cdot R_{AC,SLAB} + \frac{R_{AC,VIA}}{N_{INNER}} + \frac{R_{AC,VIA}}{N_{OUTER}}\right) \quad (13)$$

Here N_{INNER} and N_{OUTER} are the number of inner and outer vias, respectively. The inductance of a toroid is derived in [15] and repeated in eq. 14.

$$L = \frac{\mu\cdot N_{TURNS}^2\cdot T_{PCB}}{2\cdot\pi} ln\left(\frac{r_O}{r_I}\right) \ldots + \frac{r_O + r_I}{2}\mu\left[ln\left(8\frac{r_O + r_I}{r_O - r_I}\right) - 2\right] \quad (14)$$

An example of the calculated impedances of the three structures is given in table I. The table shows that the solenoid has almost twice the ac resistance of the spiral and 20% more than the toroid. It should however be noted that a quadratic solenoid is far from optimal and higher Q could be obtained if a more narrow solenoid was designed. A 6mm wide solenoid with 8 turns can have 86nH and a Q factor of 92 in $48mm^2$.

From the formulas for the inductance of each of the three structures, it can be seen that each of the three structures has a limited number of parameters which can be adjusted if the PCB parameters are given. The number of turns is the only common parameter for the three structures.

The only parameter left for the spiral, is the width of the trace (and the number of layers or inductors in series).

TABLE I
PARAMETERS FOR THREE INDUCTORS WITH APPROX. 82NH INDUCTANCE IN 8X8MM

Structure	Spiral	Solenoid	Toroid
N_{TURNS}	3.2	6	16
L	81 nH	81 nH	85 nH
R_{DC}	65 $m\Omega$	72 $m\Omega$	100 $m\Omega$
R_{AC} @ 50MHz	253 $m\Omega$	495 $m\Omega$	392 $m\Omega$
Q @ 50MHz	100	51	68

For the solenoid both the length and width can be adjusted and though it is generally best to avoid the extremes, i.e. long and narrow or short and wide, this gives a larger amount of design flexibility.

For the toroid it is possible to adjust both the inner and outer radius. For a small structure, the minimum inner radius will however be limited by the size of a via (incl. annular ring) and the number of turns. If the inner radius is increased, it is possible to ad more vias in parallel to reduce the resistance. The core of the inductor is then decreased and more turns are needed to keep the same inductance, thus the gain of doing so is limited.

III. FINITE ELEMENT SIMULATIONS

FEM simulations has been used for several reasons. First of all it is a good way to investigate, if the assumptions made about the current distribution in order to calculate the ac resistance holds. Secondly the inductance and resistance can be extracted and thereby be used to confirm the accuracy of the formulas. Lastly the simulations can be used to investigate the magnetic field from each of the three structures, so possible EMI problems can be included in the comparison.

When the formulas for the ac resistance of the spiral was derived, it was assumed that the current would run along the surface of the spiral and the resistance caused by proximity effect was neglected. A FEM simulation of a four turns spiral has been made and the current distribution is shown in figure 5 and the magnetic flux density is shown in figure 2(a). The simulation shows how the increasing strength of the magnetic

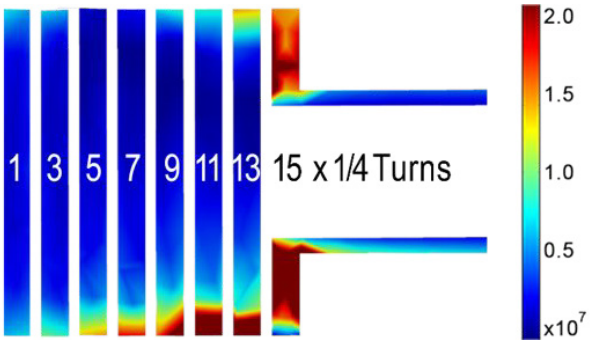
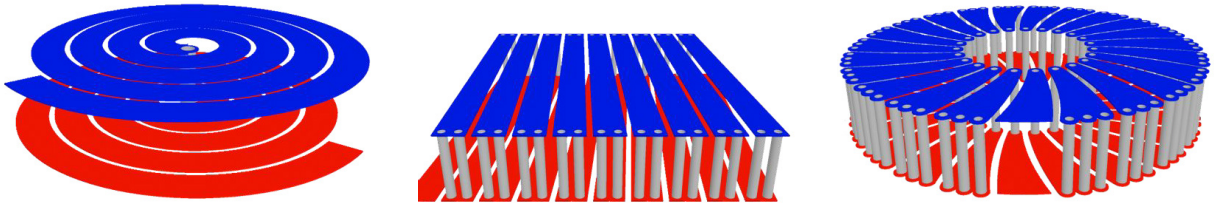
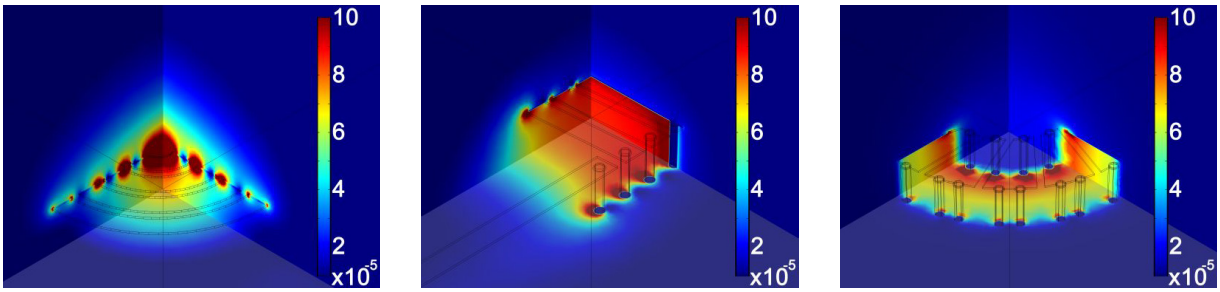


Fig. 5. Cross sections of a four turns spiral inductor showing how the current distribution (A/m^2) changes as the centre is approached



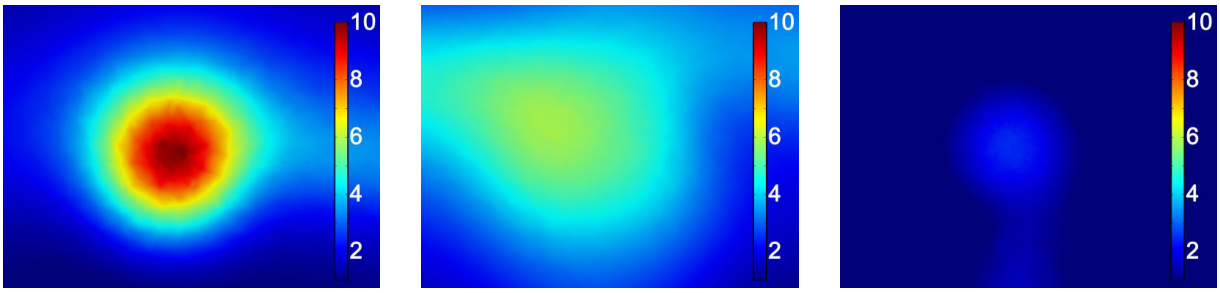
(a) Spiral (b) Solenoid (c) Toroid

Fig. 1. Three types of PCB embedded inductors



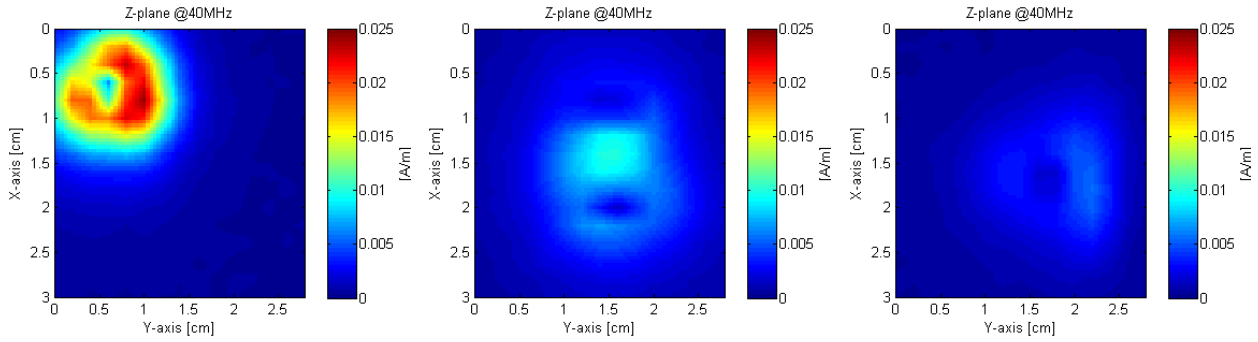
(a) Spiral (b) Solenoid (c) Toroid

Fig. 2. Finite element simulations of the magnetic flux density (B-field [T]) inside the three types of PCB embedded inductors



(a) Spiral (b) Solenoid (c) Toroid

Fig. 3. Finite element simulations of the magnetic field (H-field [A/m]) 2mm above the three types of PCB embedded inductors



(a) Spiral (b) Solenoid (c) Toroid

Fig. 4. Tangential near-field scans on three types of PCB embedded inductors. The color indicates the field strength of the combined x and y component, i.e. not including the z component as in the simulation

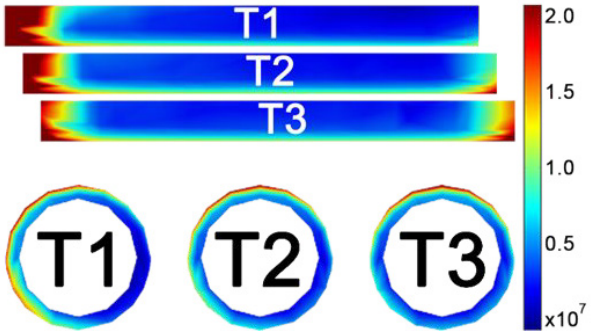


Fig. 6. The current distribution (A/m^2) of turn 1-3 of a six turns solenoid, the bottom of the traces and the top of the vias face the centre of the structure

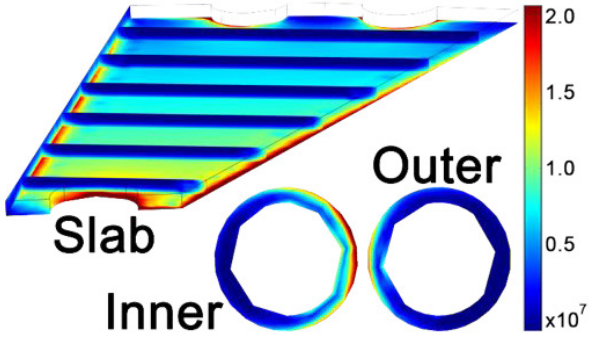


Fig. 7. Current distribution (A/m^2) in a turn of a toroid inductor

field towards the centre causes the current to crowd along the edges, this leads to higher resistance than given by eq. 3.

From the simulation it is also seen that the magnetic flux is concentrated at the centre and not shielded by the structure in any way. The fact that the field is not shielded is clear in figure 3(a) where the magnetic field 2mm above the structure is plotted. It can be seen how there is a strong field just above the structure, but also that the field decreases fast away from the centre.

Similar simulations has been made for a six turns solenoid (figure 6, 2(b) and 3(b)) and a 16 turns toroid (figure 7, 2(c) and 3(c)). The three simulated inductors has been to designed to have equal inductances in equal areas, hence the varying number of turns.

From the simulations of the solenoid, it is seen that the assumption that the current would be running along the outer surface of the inner half of the vias holds. The angle between the centre of the current and the centre of the structure is changed a bit due to the magnetic flux around the ends of the solenoid, but the area conducting the current is still the same.

On the traces the simulation shows that current is running along the surface towards the centre as expected, but also along the edges due to the magnetic field.

As the solenoid and toroid are very similar, the current distribution found in the simulation of the toroid is very similar to those found for the solenoid. The major difference is that the toroid has a even magnetic field around each turn and hence there is no change in the distribution of current between the turns.

The simulated toroid had a single via on the inner side of a turn and two parallel vias on the outer side. Figure 7 shows that the assumption about the current distribution in the vias still holds, as the current is still running in the inner surface of the via.

Contrary to the spiral, both the solenoid and the toroid structure incapsulates the magnetic field. In the solenoid all the magnetic flux goes through the centre of the structure and returns along the outer edges of the structure. This results in a much weaker field outside the structure than seen for the spiral, however the return path outside the structure can be long and hence a weak but wide field is seen in figure 3(b).

The toroid has a much weaker external magnetic field as the field caused by the turns will be fully incapsulated by the structure. Only the small single turn field (which resembles the shape of the field of the spiral) is outside the structure. This leads to a very weak and narrow external field as seen in figure 3(c).

IV. Measurements

More than 50 different inductors with each structure have been made and measured, in order to evaluate the accuracy of the formulas for resistance and inductance. As the impedance of these inductors are very small and the frequencies at which they need to be measured are very high, the measurements has to be done with very high accuracy [15].

Initial measurement of the inductance and ac resistance at 50MHz where made with a HP 4195A. The measured values fit for most of the inductors with around 10-20% deviation. However especially for the small inductors the measured values are up to 50% lower than the calculated.

An Agilent 4294A, which has an error of less than 3% for the desired measurements, has been used for the final measurements in order to get more accurate results. The measured values fit very well with the calculated values and the results for several of the prototypes is shown in figure 8.

The measured inductance and ac resistance of the largest spirals is higher than calculated. This is not surprising as the inductance of the spiral width a thin trace becomes very large in the last measurements, hence the resonance frequency starts to approach 50MHz even though the parasitic capacitance is small (see figure 9). For the spirals with thicker traces, the parasitic capacitance is larger and the resonance frequency is therefore lower.

The measurements of the solenoid impedance fits very well for both the inductance and ac resistance. The dc resistance however deviates a lot, surprisingly the inductors with a low number of turns has too high resistance whereas the inductors with high number of turns has too low resistance. The reason for the big jump between the inductor with less than 9 and more than 13 turns, can be due to the fact that they are from two different production panels. Both orders were placed for $35\mu m$ copper, but if $18\mu m$ is used for the calculation

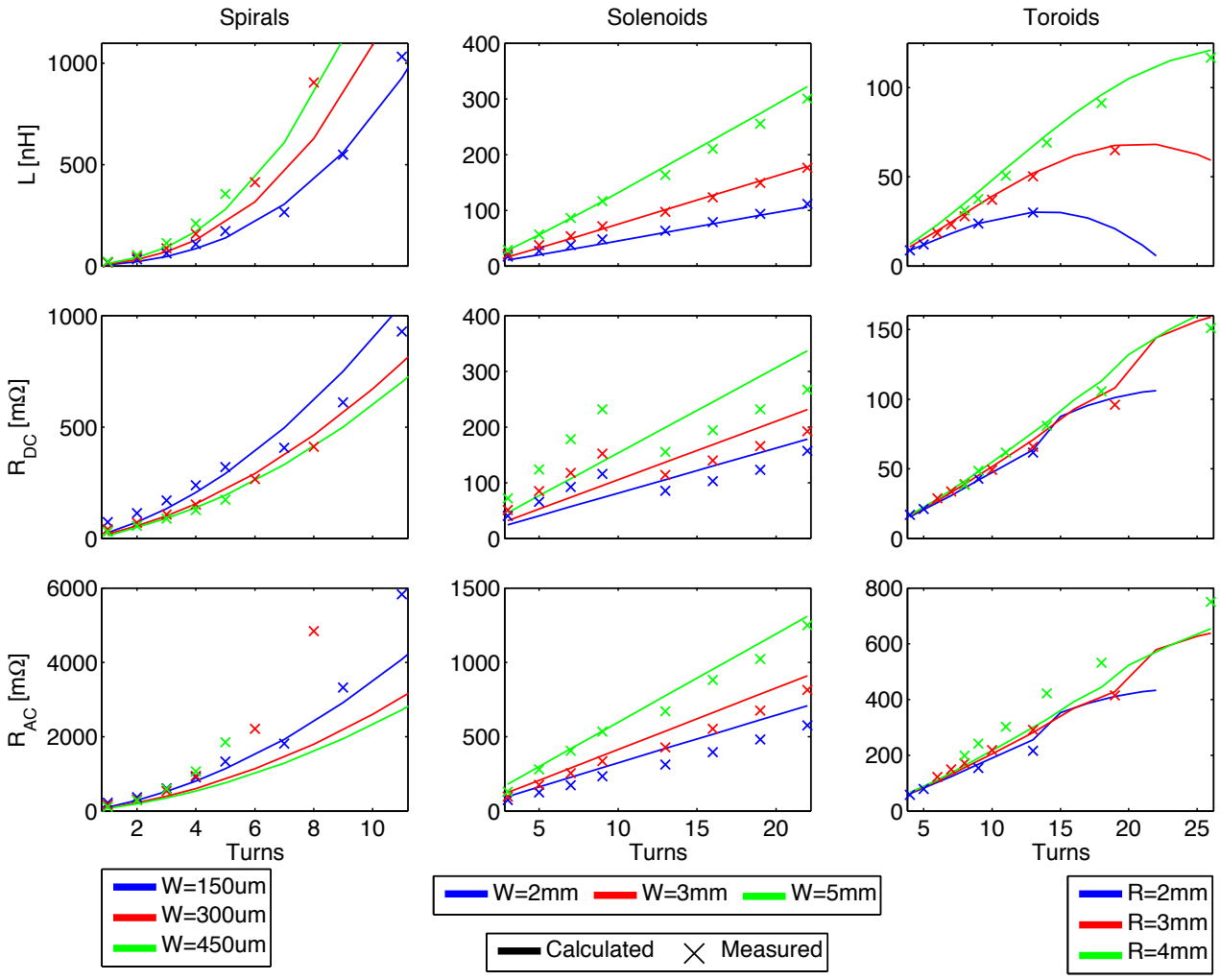


Fig. 8. Measurements of the inductance and dc and ac resistance of some of the experimental prototypes

of the ones with low number of turns and $50\mu m$ is used for the rest the deviation from the measurements are less than 1%. This shows that the tolerances of the manufacturing process is crucial to get exact results for the dc resistance, but the inductance and ac resistance are much less sensitive. As the inductance and ac resistance will be the most important parameters for use in VHF SMPS, this should not cause problems in implementations.

The calculated values of the inductance and resistance of the toroids generally fits very well with measurements. There is a small deviation in the dc resistance for the toroid with a radius of 3mm and 19 turns, but the deviation is still within 10%. The measured ac resistance of the big toroids is up to 20% higher than the calculated values. The reason for this is not clear, but it could be due to an uneven distribution of the current in the vias when there are many in parallel.

Figure 9 shows a frequency sweep of the three structures, both of prototypes with a low number of turns and of ones with a high number of turns. The inductance is very close to constant across the entire frequency range, except for the big spiral which is close to the resonance at the higher frequencies.

From the figure it can be seen that the resistance of the spiral starts to increase due to the skin effect much earlier than the two other structures. This is because the resistance of the spiral is almost entirely due to the resistance of the trace and here the skin effect starts at 1-5MHz ($\delta = 65 - 30\mu m$). The resistance of the solenoid and the toroid only start to increase at approx. 10MHz where the skin depth equals the thickness of the vias ($20\mu m$). At 50MHz, where the ac resistance used for figure 8 has been measured, the skin depth is approx. $10\mu m$ and all the structures are clearly affected by the skin depth.

V. Near Field

The importance of controlling the magnetic near-fields cannot be understated. Since one of the greatest advantages of switching in the VHF frequency range is the size of the

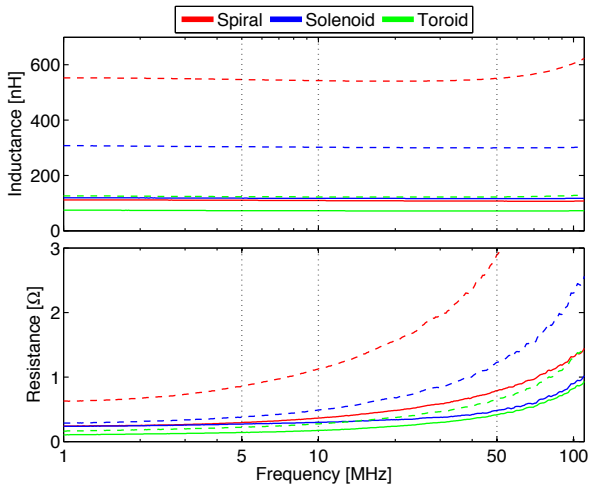


Fig. 9. Inductance and series resistance of prototypes with a low number of turns (solid) and high number of turns (dashed)

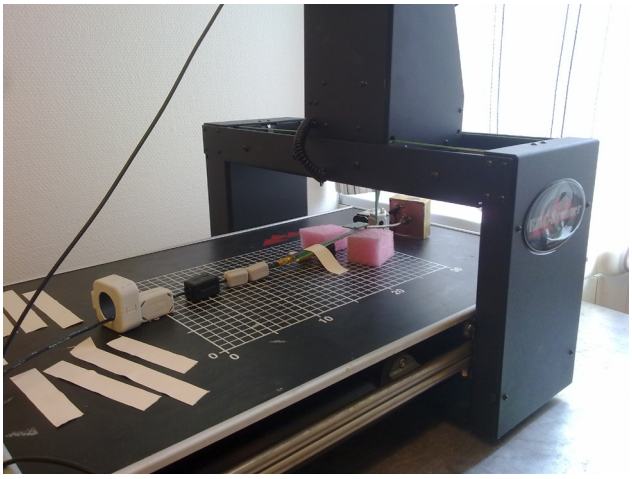


Fig. 10. The experimental setup for the near field scans

SMPS, it will in most cases be integrated in products with tight space requirements. Thus other metallic structures will be nearby. If the magnetic near-field is too strong or too widely spread it will couple to the structure and generate a current on this, which will then be re-radiated. This would make it almost impossible for the product to pass EMC requirements.

Therefore the magnetic near-fields have also been measured with a setup as described in [19]. The setup can measure both amplitude and phase of the magnetic near-field. It consist of an oscilloscope measuring the time domain response from a reference probe and a scan probe. The reference probe is placed below the circuit in a stationary position. The scan probe is positioned in each measurement point on a x-y grid surface over the structure. In the measurements the probe measures the field in 2 mm distance above the structure and with a grid step size in both the x and y direction of 2 mm.

When comparing the simulated and measured magnetic near-field, it is important to note that the z component of the fields has not been measured. From the simulations we expect that the strongest external field from both the spiral and the toroid, will be a vertical field through the centre of the structure (i.e. the z component). In the measurements it therefore seems like the field have a local minimum in the centre of the spiral and toroid and at the ends of the solenoid, but this is not the case.

The shape of the measured magnetic fields is the same as seen in the FEM simulations. The spiral has the strongest external field of the three structures and the toroid the weakest. Both the spiral and toroid has their external fields located right above the structure, whereas the solonoids field extends far outside the structure.

VI. Comparison

The paper has evaluated the impedances and the field of the structures. A very important parameter is however the flexibility or design freedom, both when scaling the inductor and laying out the complete PCB.

The spiral is by far superior in this perspective. It can be made in a single layer, the width of the trace can be scaled to get the desired relation between size and Q factor and finally it does not need and integer number of turns, which makes it possible to get the terminals placed in a way that fits into the rest of the circuit.

The solenoid also has some benefits over the two other structures. It has a rectangular shape and it has both the terminals on the same layer. The rectangular shape is much easier to align together with other rectangular components on a board which most often also is rectangular. The ability to adjust the width and length and thereby design it to fit perfectly into the circuit is also very convenient.

The toroid is clearly the least flexible as the connectors are fixed to be right above each other. Furthermore it is the structure that can achieve the lowest inductance pr area and both of the two other structures can be design with lower dc and ac resistances for a given inductance in the same area.

The only real advantage of the toroid is the small external field. As the possible EMI problems of VHF SMPS are yet to be investigated in detail, it is not clear if the compensate for this larger area and/or lower Q factor.

Several aspects of the three PCB inductors have now been evaluated and the pros and cons has been summed up in table II.

The three converters in figure 11 has been designed to give and idea of how the complete circuit with PCB embedded inductors will behave. Embedding the inductors in the PCB clearly gives some benefits, i.e. a much lower profile and a higher power density [21]. However the design still has to be optimised in order to compete with discrete air core solenoids which can have Q factors of more than 200 [20].

TABLE II
PROS AND CONS OF THE THREE STRUCTURES

Structure	Pros	Cons
Toroid	Smallest external field	Least flexible Lowest Q and L pr area
Solenoid	Rectangular shape High Q	Wide external field
Spiral	Highest Q Most flexible	Strong external field

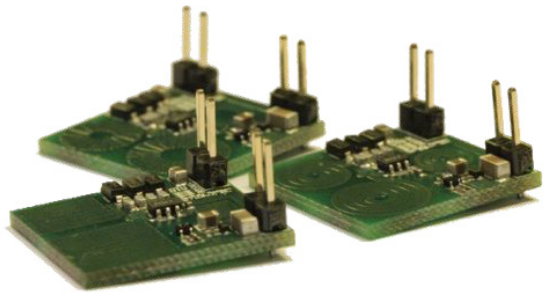


Fig. 11. Resonant converters with the different structures for PCB embedded inductors

VII. CONCLUSION

This paper has given the first direct comparison between three different structures for PCB embedded inductors. The inductors have been compared with regard to resistance, inductance, magnetic field and design flexibility, both theoretically and experimentally.

The results show that there are huge differences in what can be achieved with the different structure and that a single structure cannot be selected as the superior for all applications. The spiral can achieve the highest inductance pr area and is the only structure that can be made in a single layer; the solenoid is easy to scale and can be designed to fit perfectly into a complete design and the toroid is by far superior with regard to the external magnetic field.

Future research within PCB embedded inductors should include derivation of formulas to calculate the parasitic capacitance and thereby also the resonance frequency, as these will become important for designs where a large structure is needed in order to get a higher Q factor.

Another way to increase the Q factor is to investigate how the design of each structure can be optimised to reduce the resistance without increasing the size.

Detailed investigation of the EMI from VHF SMPS is also needed. If it turns out that this is a problem, structures surrounding the inductor to encapsulate the field could be a solution.

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A.14 M. Madsen, J. D. Mønster, A. Knott, M. A.E. Andersen:
***"Design Optimization of Printed Circuit Board Embedded Inductors through Genetic Algorithms with verification by COMSOL"*,**
COMSOL conference 2013, Boston, MA, October 2013. Conference Proceedings.

Design Optimization of Printed Circuit Board Embedded Inductors through Genetic Algorithms with Verification by COMSOL

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Abstract: This paper describes the implementation of a complete design tool for design, analysis, optimization and production of PCB embedded inductors.

The papers shows how the LiveLink between MATLAB and COMSOL makes it possible to combine the scripting and calculation power of MATLAB with the simulation power of COMSOL in order to get an extremely efficient tool for inductor design.

The tool has been used to investigate PCB embedded spiral, solenoid and toroidal inductors. Due to the fact that the spirals are axisymmetric they can be simulated in 2D, which speeds up the simulation significantly. This is not possible for the solenoid and toroid, hence complete 3D structure has been made and simulated for these structures.

Keywords: Inductor, Resistance, Optimization, LiveLink to MATLAB, axisymmetric.

1. Introduction

Passive energy storing elements constitute the major part of modern switch-mode power supplies (SMPS), both regarding size and price. The physical and numerical size of these, scales directly with the inverse of the switching frequency. The constant strive for smaller and cheaper power supplies has therefore let to constantly increasing switching frequencies ever since the development of the SMPS in the early 70's.

Recent research combines radio frequency (RF) circuits and power electronics to design SMPSs with switching frequencies in the Very High Frequency range (VHF, 30-300MHz) [1]-[2]. This is a dramatic increase from the .1-5 MHz which traditional SMPS topologies are limited to due to switching losses.

Several benefits arise from the increased switching frequency; higher power density, decreased cost, reduced weight and faster transient response [3]-[4]. The increased frequency however also leads to some new challenges [5]-[6]. One of these challenges is the magnetic components.

The core materials that are normally used to get high coupling in transformers and high inductance in inductors have high core losses at these frequencies. New core materials or ways of designing the magnetic components therefore has to be developed.

The inductance needed at these frequencies are very low (~10-200nH) and the skin depth is 4-12 μm. Hence embedding these as air core inductors in the Printed Circuit Board (PCB), and thereby reduce the size and price of these even further, becomes a viable solution [7]-[8].

In order to keep the efficiency high at these highly elevated frequencies soft switching is essential, as hard switching would lead to breakdown of the semiconductors. A key parameter to achieve this is accurate inductance value. Formulas for these are all based on approximations leading to small deviations. As the inductance cannot be fine tuned once the PCB has been manufactured, Finite Element Analysis (FEA) becomes a very attractive way to insure that the circuit is correctly designed the first time.

2. System level

In order to design and produce the inductors a MATLAB program with a GUI has been designed, see figure 1. The program takes the production parameters and the desired inductance and size as input and uses a genetic algorithm and formulas to find parameters for the initial design.

Then COMSOL is used to investigate the current distribution and magnetic fields and to verify the inductance and resistance.

Once the design has been verified in COMSOL and any error has been corrected, a PCB file is generated directly from the same interface.

3. MATLAB optimization

The optimization routine is used to find the best inductor, within a given area. Best is defined

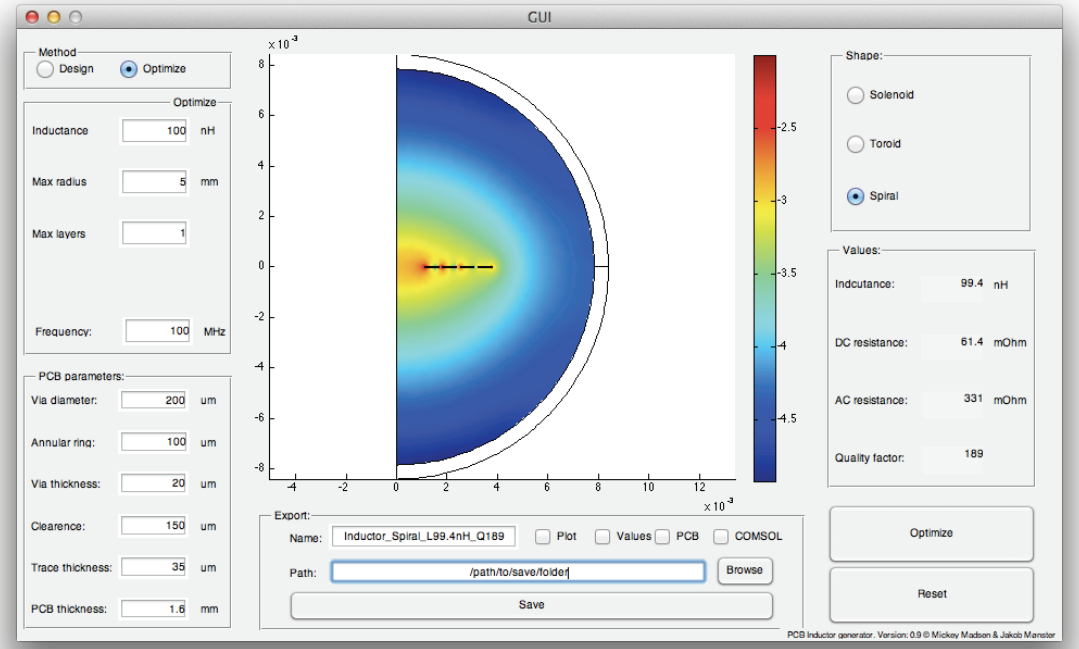

Figure 1. GUI of the MATLAB program, with the extracted simulation results from COMSOL via LiveLink for MATLAB.

as the required inductance the user needs, with the highest Q factor and with the lowest area, in that preferred order. The optimization routine is based on a genetic algorithm already implemented in MATLAB. The optimization parameters are the desired inductance, a maximum area and the Q factor. The Q factor is the relationship between the inductance and resistance, given by:

$$Q = \frac{\omega L}{R}$$

The inductor should have the highest possible Q factor and the desired inductance. This is achieved by having a cost function that the genetic algorithm minimizes. The genetic algorithm takes any number of inputs, with possibility to define the variable as an integer. Each variable is setup so a closer value to the desired will lower the cost function, and each variable is weighted according to the importance of that specific parameter. The cost function used is:

$$Cost = a \cdot \left| \frac{L}{L_{desired}} - 1 \right| + b \cdot \frac{1}{Q} + c \cdot A$$

where $L_{desired}$ is the desired inductance and A is the area of the inductor. The weight factors used are shown in Table 1.

Table 1. The weight factors used for the cost function.

a	b	c
100	10,000	1

The overall MATLAB program with the optimization routine is described by the flowchart shown in Figure 2.

4. COMSOL:

To verify that the calculations used to derive the optimum structure and evaluate that the formulas in overall are usable the MATLAB program is used to interface to COMSOL via COMSOL LiveLink for MATLAB [9].

The AC/DC module in COMSOL is used to simulate the three possible inductor structures. The AC/DC module gives possibility for extracting the inductance and resistance, which

are the desired parameters [10]. A precondition for using the AC/DC module is that the length of the structure l, is much less than the wavelength of the frequency at which the system is simulated. That is:

$$l < {}^{1}/_{10} \cdot \lambda$$

At VHF frequencies the wavelength is still in the range of a few meters, why the AC/DC module is a viable approximation to the system, as the structures are very small.

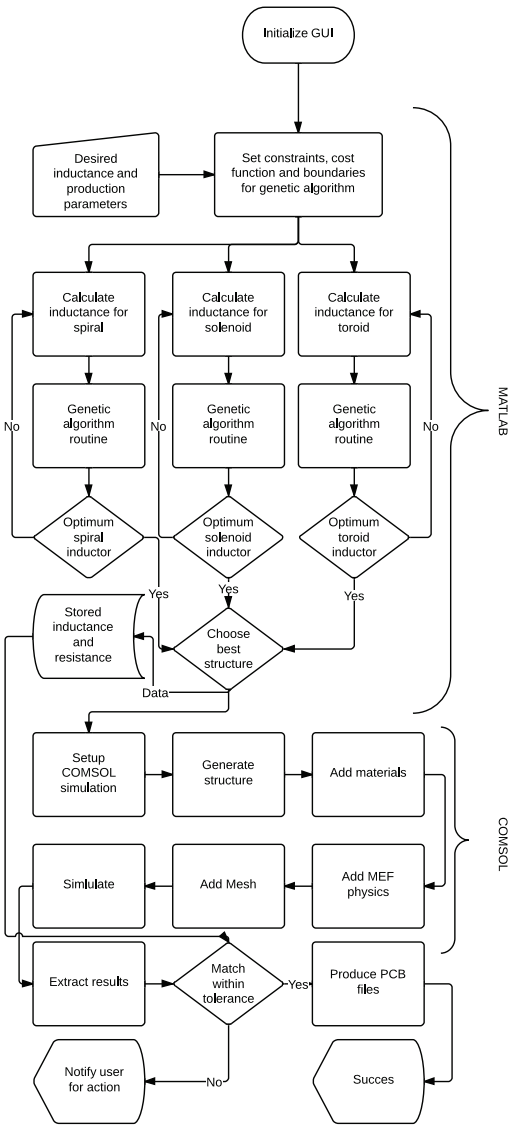

Figure 2. Flowchart of the MATLAB program, with the optimization routine and the COMSOL routine

4.1 Design steps

The COMSOL model is set up in five steps. Each are described here in detail. The program can simulate three different structures: A solenoid, a toroid and a spiral. The spiral is simulated in 2D to achieve faster simulation time. Examples of the three different structures are shown in Figure 3-5.

LiveLink for MATLAB gives access to all the normal features of COMSOL with the scripting capabilities of MATLAB. In general five steps are used in the interface.

4.2 Step 1 – Generating the structure

The structures are made by implementing the layers of the PCB in a z-shifted plane, and then extruding them. Cylinders are added as vias, and then subtracting smaller cylinders inside the other for the holes in the vias. This gives a very exact representation of the full 3D inductor structures [11]. There is a short loop for the 2 connectors in the inductors, and between is made a gap. This is used when setting up the physics. At last the entire inductor is made into a union. During the generation of the structure, several selections are made, both with boxes and explicit. These are automatically updated if more structures are added in the process.

The spiral is only modeled in an axisymmetric 2D model with infinite elements [12] to lower the simulation time. The two other structures are (unfortunately) not possible to split into an symmetry.

The PCB's dielectric material is not added to the model, as it does not influence the inductances and resistance of structure, and only will increase simulation time. If the parasitic capacitance or resonance frequency of the inductors is to be extracted from the simulation, this has to be added as it do influences the capacitance.

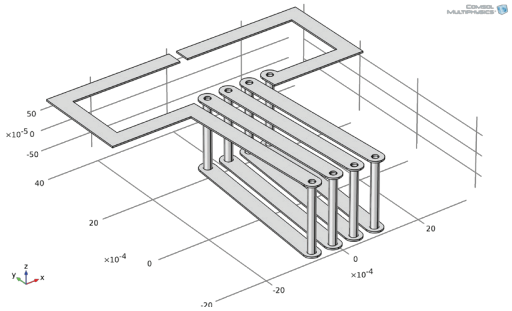

Figure 3. Example of a solenoid inductor in 3D.

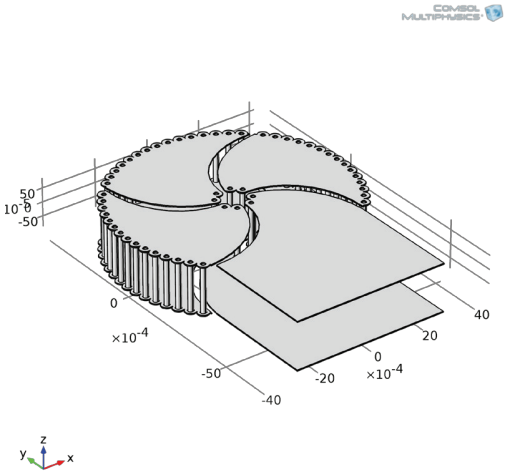

Figure 4. Example of a toroid inductor in 3D.

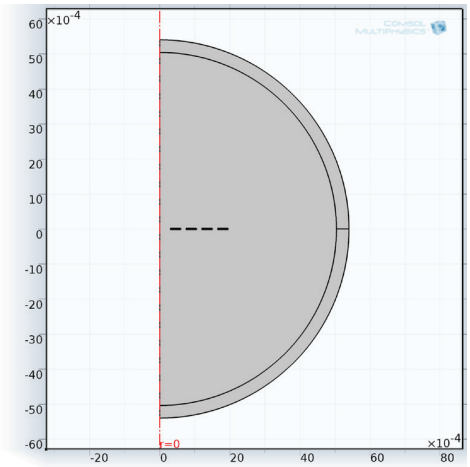

Figure 5. Example of a spiral inductor in 2D.

4.3 Step 2 – Setting up the physics

The physics is based on the Magnetic Fields (MF) with a frequency domain study. The physic is set to work at the entire system expect the gap created between the terminals. This will introduce a small error but smaller than if the connectors were taken to the exterior of the bounding box. The surroundings are modeled as air, and the structure as copper. As the magnetic field is not guided by a core, there is added an infinite element to ensure the entire field is simulated within the bounding box's boundaries.

For exciting the inductor a "Single-turn coil" is used [13], with a voltage input. Furthermore the physics is set to linear, as this decreases the simulation time dramatically, and does not change the results.

4.4 Step 3 - Meshing

As there is great difference between the overall size of the structure and the holes in the vias and the height of the copper traces, which have an even smaller skin-depth, the mesh must be customized to the structure. The structure is split in three. The inductor structure uses "Free Tetrahedrals" with the size set to "Extra fine". Boundary layers is used to get the correct current density in the copper tracks,. The air is also meshed with "Free Tetrahedrals", but with the size set to "Fine". The infinity domain is swept with a simple distribution of 3 elements. This configuration gives a mesh quality of approximately 0.7.

4.5 Step 4 – Study setup

The study is set up to use a frequency domain. The standard stationary solver is changed to use a SOR solver instead of the Multigrid, as the system is set to linear.

4.6 Step 5 – Extracting parameters

The inductance and ac-resistance are added to a table from a global evaluation. The table is then imported into MATLAB together with a plot of the magnetic field with the LiveLink for MATLAB functions "mphtable" and "mphplot".

5. Verification

In order to verify the formulas used to calculate the inductance and resistance and to ensure that the implementation of the models in COMSOL is a good approximation a comparison of calculated, simulated and measured values are

performed. The extensive comparison is only made for spirals, as the simulation time if done for solenoids and toroids would accumulate to weeks.

The simulations are shown for two set of spiral structures: one with one layer and a 150um trace shown in Figure 6 and one set with a 2 layer structure and 300um trace in Figure 7. The number of turns is swept from 1 to 15 and 1 to 10 respectively.

The comparison shows that there in general is a good agreement between calculated, simulated and measured inductances, but with higher accuracy for the simulated values.

The same is the case for the ac-resistance. In both sets there is a large increase in the measured resistance when the structures become large. This is the start of the first resonance, and this isn't part of neither the simulation nor the calculation.

In Figure 8 and 9 is shown a cutout of the magnetic field of a solenoid and a toroid. The simulation shows that solenoid and toroid structures encapsulate the magnetic field, resulting in a much weaker external field than seen for spirals. In the solenoid all the magnetic flux goes through the center of the structure and returns along the outer edges of the structure. For the toroid the major part of the field is running inside the toroidal structure and only a small part of the field (caused by the single turn) runs outside.

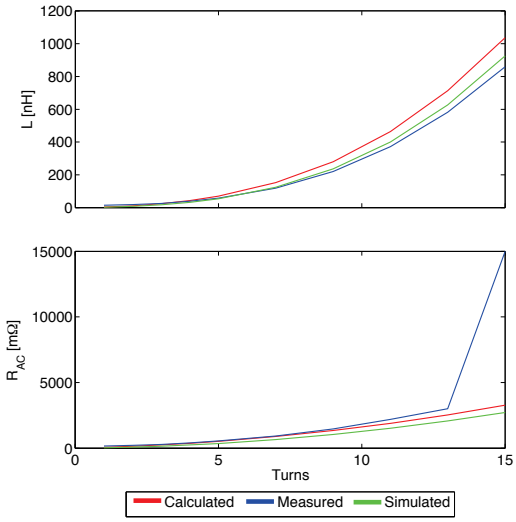

Figure 6. Inductance and resistance of single layer spirals with 150µm trace width.

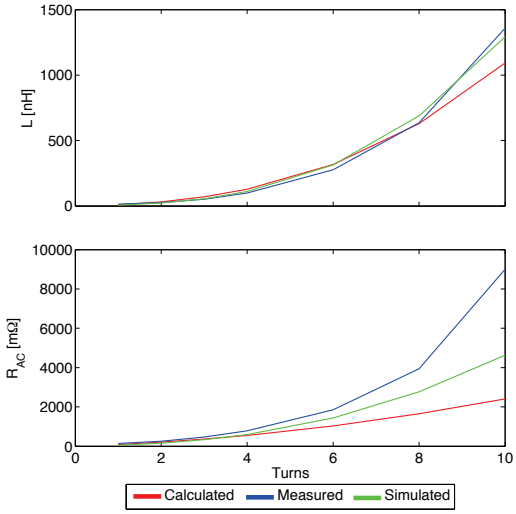

Figure 7. Inductance and resistance of two layer spirals with 300µm trace width.

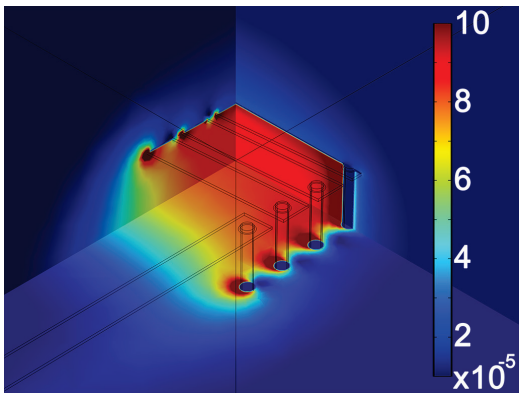

Figure 8. Magnitude of the B-field in a solenoid inductor (Multislice).

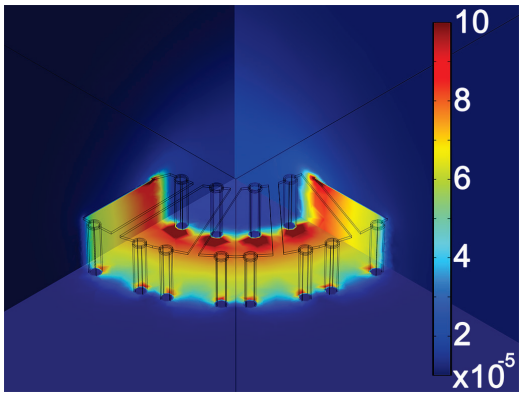

Figure 9. Magnitude of the B-field in a toroid inductor (Multislice).

6. Conclusion

It has been demonstrated how the LiveLink between COMSOL and MATLAB can be used to design, analyze and optimize PCB embedded inductors. The scripting and calculation power of MATLAB combined with the simulation power of COMSOL can serve as an extremely efficient tool for inductor design.

A genetic algorithm has been used to design the optimal inductors based on the available equations. Then COMSOL has been used to verify the calculated inductance and resistance and investigate the current distribution and the magnetic fields. This analysis is very useful for finding new ways to design inductors in order to make new shapes with even better performance.

Ones the inductor has been investigated and verified to give the desired impedances the PCB files can be generated directly from the same MATLAB GUI giving a very simple and yet accurate design tool.

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A.15 H. Schneider, J. D. Mønster, M. Madsen, T. Andersen, A. Knott, M. A.E. Andersen:
***"Investigation of a Hybrid Winding Concept for Toroidal Inductors using 3D Finite Element Modeling"*,**
COMSOL conference 2013, Boston, MA, October 2013. Conference Proceedings.

Investigation of a Hybrid Winding Concept for Toroidal Inductors using 3D Finite Element Modeling

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Abstract: This paper investigates a hybrid winding concept for a toroidal inductor by simulating the winding resistance as a function of frequency. The problem of predicting the resistance of a non-uniform and complex winding shape is solved using 3D Finite Element Modeling. A prototype is built and tested experimentally to verify the simulation results. Finally COMSOL LiveLink to CAD is utilized to highlight a bottleneck for this kind of winding scheme.

Keywords: Inductor, Resistance, Mesh, Boundary layers, LiveLink.

1. Introduction

The conventional wire wound toroid shown in Figure 1 is used extensively in switch mode power supplies in EMC filters and as inductors and transformers. However the space between the windings increases gradually from the inner diameter towards the outer diameter of the core which limits the utilization of the available winding space. This effect can increases the resistance and thus the conduction loss of the component [1,2].

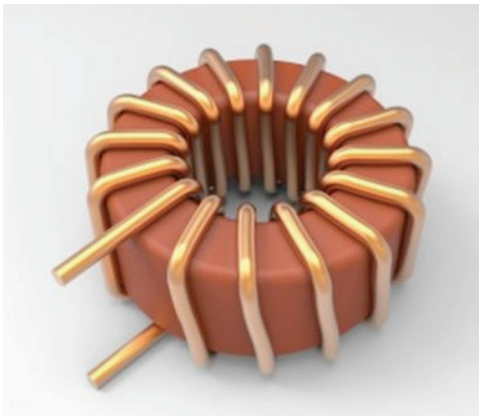

Figure 1. Conventional toroidal inductor

Furthermore, in the manufacturing process of a toroidal inductor with a large diameter wire and a small core a hook/pull type winding machine must be utilized. Under manufacturing a tool pass through the center of the toroidal core to grab and pull the wire which is manually feed to the hook for each turn.

To overcome these disadvantages a hybrid winding scheme may be used [3]. The basic idea of the hybrid winding scheme is to cut and bend copper foils into "U" shaped pieces that fit around the toroidal core as shown in Figure 2. To complete the winding the foil pieces are connected through the traces in a printed circuit board (PCB). In a final product the foil pieces would be pre-attached to a former for easy handling and alignment on the PCB.

Figure 2. Exploded view of the hybrid winding concept for a toroidal inductor.

The hybrid winding concept has the following benefits compared to the conventional single layer wire wound inductor:

- Large scale production and distributed stock of foil assemblies reduce cost and delivery time.
- Fully automated manufacturing process. Foil pieces are stamped, bended and attached to a plastic former. The core and the foil assembly can be placed by a pick and place machine.
- Better utilization of winding space. Constant resistance with increased number of turns or constant number of turns with decreased resistance for the same core size
- Low AC resistance due to increased surface area using foil.
- Configurable winding structure. The connections of the foil pieces through the PCB can be freely defined by the design engineer. The number of turns can be decreased by paralleling the foil pieces. It enables the same foil assembly to be used for inductors, common mode EMC chokes, transformers etc.
- Different core materials can be used with the same foil assembly.

The disadvantages may be as follows:

- Commercial available PCB layer thickness and interconnections between the foil cutouts and the PCB tracks is a bottleneck for high power applications.
- The assembly of the foil cutouts is limited to a specific core size.

2. Use of COMSOL Multiphysics

The challenge of predicting the resistance as a function of the frequency of such a complex 3D winding geometry is solved using the COMSOL AC/DC module[4]. The greatest challenge was to create the mesh since eddy currents need to be considered and the thickness of the foil to the PCB traces in this work vary from 0.5mm to 70µm. A boundary layer mesh with 4 layers and a stretch factor of 2.5 was used. The first layer fitness was set manually to 5µm. A free tetrahedral mesh was used for the DC resistance simulation.

3. Results

In Figure 3 the current density at 100kHz in the foil cutouts and the PCB traces are shown. The 3D model of the hybrid inductor is shown from beneath in order to inspect the PCB traces. Some of the windings and the core are hidden in order to look at the inner part of the winding. From the colors it is easy to see that the current density is highest closest to the core where the current path is shortest and in the places where the width of the foil cutout is lowest. This suggests that the foil cutouts should be angled instead of the PCB traces in order to reduce the resistance.

The implemented prototype is shown in figure 4. The PCB were milled with a router and the foil pieces were cut with a scissor and soldered manually. It is clear that the prototype has rounded corners and unequal spacing compared to the 3D drawing shown in figure 3.

In Figure 5 the simulated and measured resistance as a function of the frequency is shown. An offset is added to the simulation result to compensate for any static error sources such as imprecise cuts and clearance of the bent foils, all of which is not included in the 3D model. The simulation with offset fits the measured results from 10 Hz to 100 kHz which is the common operating frequency range. It is eddy currents in the core that causes the increase in the measured AC-resistance beyond the 100 kHz which is not accounted for in the simulation model.

A LiveLink to a computer aided design (CAD) program [5] was also implemented and several simulations were performed in order to investigate the DC-resistance versus the PCB Thickness. The result shown in figure 6 indicates that the DC-resistance could be halfed by using 220 um thick PCB traces compared to the common 70 um PCB trace thickness. The simulation prove that the PCB trace thickness is a bottleneck for high power applications.

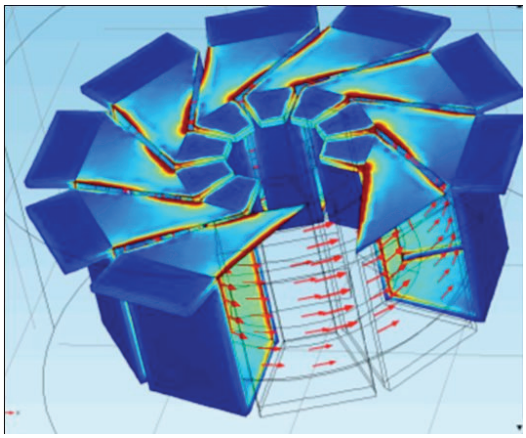

Figure 3. Simulated current density and magnetic flux density

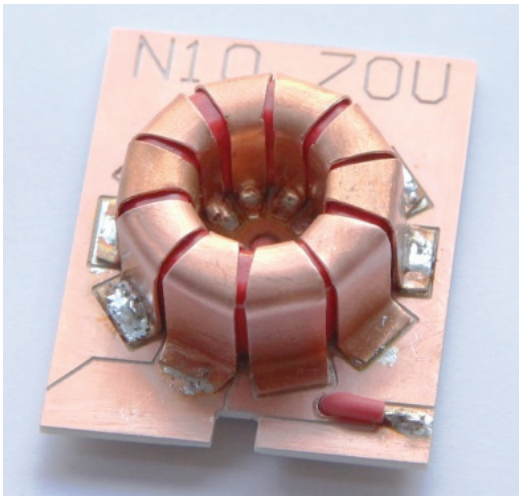

Figure 4. Prototype used for validation of the simulation results

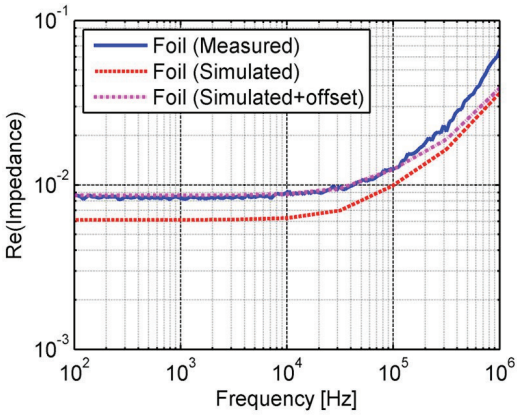

Figure 5. Resistance as a function of the frequency

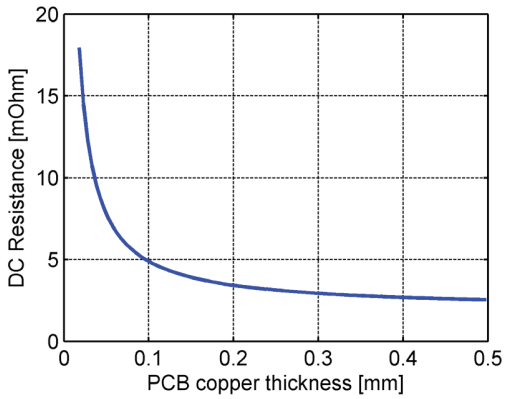

Figure 6. Simulated DC-resistance as a function of PCB copper thickness. Foil thickness is fixed at 500 µm.

4. Conclusion

A hybrid winding concept for toroids using the traces in a printed circuit board to make connection to bent copper foil cutouts has been evaluated in terms of AC-resistance and the DC-resistance as a function of PCB trace thickness.

A FEM analyses have been carried out and the model have been experimentally validated.

It is found that the commercially available layer thickness in a PCB is a bottleneck for high power applications. Finally a plot of the simulated current density in the winding reveals that the winding configuration can be optimized which is crucial for performance.

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A.16 H. Schneider, J. D. Mønster, M. Madsen, T. Andersen, A. Knott, M. A.E. Andersen:
***"Optimizing Inductor Winding Geometry for Lowest DC-Resistance using LiveLink between COMSOL and MATLAB"*,**
COMSOL conference 2013, Boston, MA, October 2013. Conference Proceedings.

Optimizing Inductor Winding Geometry for Lowest DC-Resistance using LiveLink between COMSOL and MATLAB

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Abstract: An optimization routine is presented to optimize a hybrid winding geometry for a toroid inductor in terms of the DC resistance. The hybrid winding geometry consist of bended foil pieces connected through traces in a printed circuit board. MATLAB is used to create a graphical user interface that visually plots the winding using input parameters such as core dimensions, number of turns, clearance between windings, and the winding angle of each segment of the winding. COMSOL LiveLink is used to import the winding geometry from MATLAB and create a 2D finite element model to simulate the DC reisistance. Finally the winding configuration with the lowest DC resistance is found by sweeping the parameters of the winding geometry and simulate and save the result in each step. An improvement of more than 30% compared to previous work where achieved in this way

Keywords: Inductor, Resistance, Mesh, Boundary layers, LiveLink.

1. Introduction

The conventional wire wound toroid is used in many power electronic applications such as EMC filters, power inductors, transformers and so on. However it has the following disadvantages regarding the winding scheme and the manufacturing/production process [1, 2]:

- The spacing between the windings increases gradually from the inner diameter towards the outer diameter of the core limiting the utilization of the winding area.
- For large wire diameters a hook/pull type manufacturing machine is used. The space required for the hook and the wire being pulled through the center of the core further decrease the utilized winding area.
- For large wire diameters manual work is required for feeding the hook with the wire leading to increased cost.
- Complex manufacturing machines are needed for winding due to non-separable core.
- Manufacturer lead time and price strongly depends on the purchase history and number of ordered magnetic components.
- The leaded toroid may be placed and soldered manually in a production increasing time to market and cost.

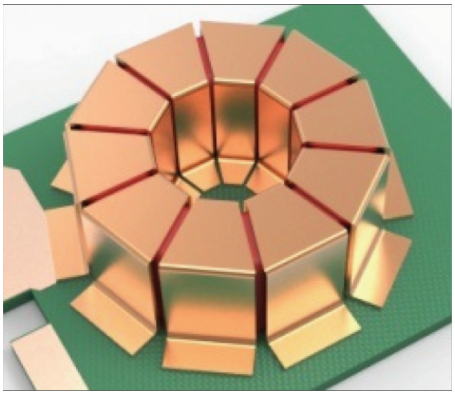

Figure 1. Surface mounted hybrid toroidal inductor.

This work focus on a hybrid foil combined with printed circuit board (PCB) trace winding scheme in an attempt to improve both the utilized winding space and improve the time to market by creating more freedom in the manufacturing and production process.

The basic idea is to cut and bend copper foils into "U" shaped pieces that fit around the toroidal core. The number of bended foil pieces determines the number of turns and in a final product all the foil pieces would be pre-attached to a plastic former for easy handling and alignment on the PCB.

In previous work [4] a hybrid inductor with 15 turns, a foil thickness of 500um and a single layer PCB with a layer thickness of 70um was implemented as a prototype. The measurements were used to evaluate a 3D Finite element model (FEM) created in COMSOL with good agreement. The results showed that typical available PCB layer thicknesses (18um – 210um)

are a bottle neck for the DC resistance in a hybrid inductor.

In the implemented model the bended copper pieces went straight over the core and the traces in the PCB was angled to complete the winding. It is easy to imagine how the DC resistance would be improved if the thin traces in the PCB were straight and short and the thicker copper pieces were angled over the core connecting the winding. It is however hard to predict the optimum angles of each segment in a turn and to predict the impact on the DC resistance. It is necessary to find an answer to these questions in order to take full advantage of the hybrid inductor.

2. Use of COMSOL Multiphysics

COMSOL is used to simulate and find the DC resitance of the windings in the inductor. The system is set up as a 2D simulation to improve simulation time, which is needed for the optimization algortihm solution time not to get extremely long.

The 3D model is based on four segments per turn, labeled F1-F4 as shown in Figure 2. The optimization algortihms input parameters is the coil dimensions, number of turns, minimum clearance between turns, the starting position of the winding following the tangent of the core, the angle of each segment and the thickness of each segment.

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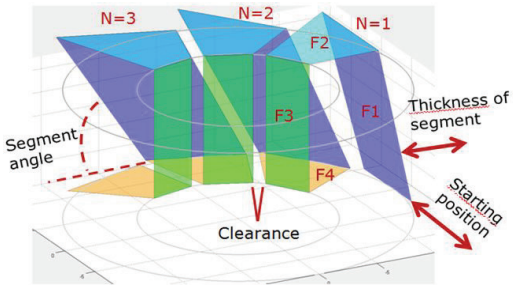

Figure 2. Geometry of the winding and the related parameters.

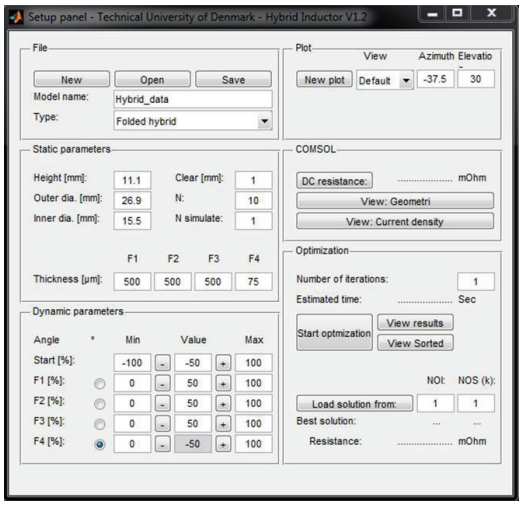

Figure 3. The designed MATLAB GUI with LiveLink to COMSOL.

To control the optimization rutine a MATLAB program was developed, that can take all the inputs, and set the different constraints, and in general control the optimization. For setting up the 2D structure in COMSOL the LiveLink for MATLAB [5] was used. The following steps were implemented in the MATLAB code in order to automate the calculation of the DC resistance with changing winding geometry:

- Creating a MATLAB GUI – See Figure 3
- Creating the winding geometry
  - The geometry of a single turn is created based on the parameters set by the GUI for the winding such as size of the core, clearance, thickness of the foil and the angle of each segment in a turn. The coordinates positions are translated from 3D to 2D by unfolding the each turn.
  - A for loop creates the desired turns by copying the coordinates of the single turn by rotating them in a polar coordinate system. Every section of a turn is created as a polygon and the coordinates is saved for later selection of domains and boundaries. Each segmet is shifted so they lay in layers. This is done to ensure that the windings will not

cross each other, as shown in Figure 4.

- Selecting the boundaries. As the specific boundaries are not number as the are generated, it is nessary to find them in order to set up the rest of the simulation. This is done by using the LiveLink method “mphselectbox”. The saved positions used to generate the turns are used and the boundary are stored for later use.

- The material setup is defined for each segment in the simulation, instead of using the standard Copper material, this is done since the different segments can (and usaully have) different thickness of the copper. The differrence is used to define an electrical conductivity for each segment modelling the thickness.

- The physics is set up as an “Electrical Currents” model, with a stationary study, and the discretixation of the electric potential to (the standard) quadratic. To enforce a voltage over the entire structure a Terminal is added on the first structure (bottom structure, red boundary). Here a voltage of 1V is set. On the last (top) structure a Ground node is added. To ensure the connection betweeen each turns structure the Periodic Condition is used, between the boundaries of the end of one structure and the input of the next, as indicated by the arrows in Figure 4.

- The geometry is meshed using the standard mesh Free Triangular, with the seize set to “Normal”. This gives an simple, yet accurate enough approximation.

- The study is set as a stationary standard study, with direct solving.

- The results are taken in two parts

  - A global variable is used to calculate the DC resistance seen from the terminals. The conductance G is available directly from the solution and the DC resistance is then calculated as The current density was evaluated in the

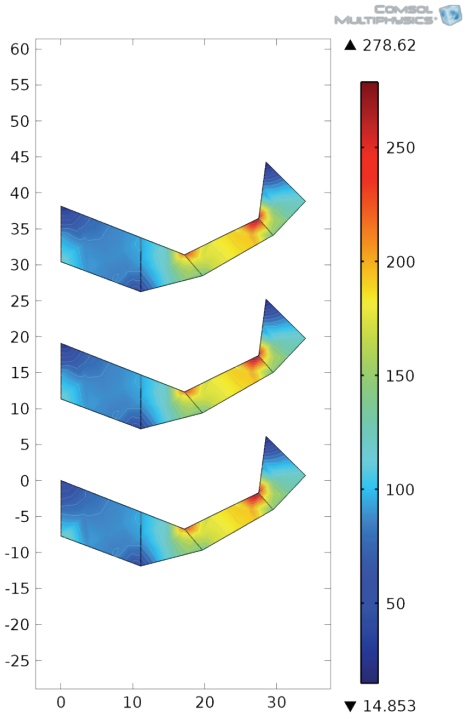

Figure 1 Current density plot of each of the turns structures.

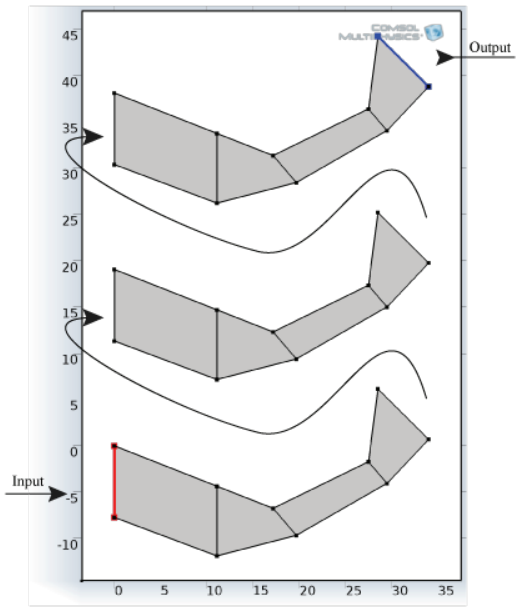

Figure 2 Ilustration of an unfold winding which is copied and connected in series via “Periodic Condition”

$$R_{DC} = \frac{1}{G}$$

same way but as a surface maximum and minimum, as well as plotted using in COMSO, see Figure and shown in a MATLAB figure using the function "mphplot".

3. Results

The result of the optimization routine is shown in Figure 5. The plot shows the simulated resistance for a given number of solutions where the previously mentioned parameters of the winding were altered. In this specific case the resistance don't change much as a function of the winding parameters as in other cases. In this work the following 3 cases were examined:

- **Case 1**: Few turns,
  PCB layer thickness << Foil thickness
- **Case 2**: Many turns,
  PCB layer thickness << Foil thickness
- **Case 3**: Few turns,
  PCB layer thickness = Foil thickness

In table 1-3 the parameters and result for each of the 3 cases are summarized. In each case 3 winding configurations are compared. One where only the PCB trace is angled called "Bottom", one where the lowest DC-resistance were found called "Opt." for optimized and one where only the top segment of the bended foil was angled called "Top".

In Case 1 the optimized solution resulted in an improvement of 32 % compared with only angling the PCB trace. However an 31 % improvement was achieved by only angling the top segment of the bonded foil piece. If few turns and a big difference in foil and PCB trace is utilized the "Top" solution may be sufficient since it will result in a low DC-resistance and may be easier to fabricate.

In Case 2 a very small improvement of 0.8 % for both the "Opt." and the "Top" compared to the "Bottom" is achieved. The limited space due to many turns reduce the influence of angling the segments in the winding and obviate the optimization.

In Case 3 the "Opt." and "Top" configuration resulted in 11 % and 6 % improvement respectively. For few turns and equal winding thickness the optimized solution is therefore attractive. This could be an important conclusion since this configuration is highly suitable for high frequency operation which is in high demand. However this must be confirmed in a 3D simulation of the AC-resistance which is out of the scope in this work.

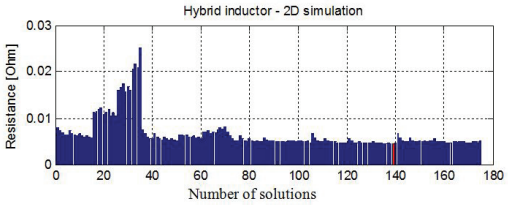

Figure 5. Illustration of optimizing routine for a single integration. The x-axis is the combination number for the given angle span and the y-axis is corresponded DC resistance.

Table 1: Case 1 (Few turns, PCB layer thickness << Foil thickness)

Number of turns: 10, Segment thickness: F1, F2, F3 = 500 µm, F4 = 70um, Clearance = 1mm			
Winding angle configuration	***Bottom***	***Opt.***	***Top***
Starting point SP [%]	0	20	0
Outer Foil Segment F1 [%]	0	63	0
Top Foil Segment F2 [%]	0	37	100
Inner Segment F3 [%]	0	0	0
Bottom Segment F4 [%]	100	0	0
DC resistance [mΩ]	6.78	4.64	4.71
Improvement [%]	Ref.	32	31

Table 2: Case 2 (Many turns, PCB layer thickness << Foil thickness)

Number of turns: 100, Segment thickness: F1, F2, F3 = 500 µm, F4 = 70um, Clearance = 1mm			
Winding angle configuration	***Bottom***	***Opt.***	***Top***
Starting point SP [%]	0	0	0
Outer Foil Segment F1 [%]	0	75	0
Top Foil Segment F2 [%]	0	25	100
Inner Segment F3 [%]	0	0	0
Bottom Segment F4 [%]	100	0	0
DC resistance [mΩ]	435	432	432
Improvement [%]	Ref.	0.8	0.8

Table 3: Case 3 (Few turns, PCB layer thickness = Foil thickness)

Number of turns: 10, Segment thickness: F1, F2, F3, F4 = 500 µm, Clearance = 1mm			
Winding angle configuration	***Bottom***	***Opt.***	***Top***
Starting point SP [%]	0	100	0
Outer Foil Segment F1 [%]	0	38	0
Top Foil Segment F2 [%]	0	21	100
Inner Segment F3 [%]	0	0.5	0
Bottom Segment F4 [%]	100	40.5	0
DC resistance [mΩ]	2.6	2.3	2.5
Improvement [%]	Ref.	11	6

4. Conclusion

A MATLAB program for optimizing the structure of an inductor in order to minimize the DC resistance have been created. The program sets up the 2D simulation of the structure dividide into turns, again dividede into 4 segments, each with different thickness. The system is simlated and the numerical as well as grapical results are extracted. The program shows that it is capacble of finding the optimum winding geometry, leading to an improved DC-resistance. The findings are in general:

- Few turns and large difference in foil and PCB trace thickness
  - Angeling the top segment (F2) is a suitable solution
- Many turns
  - Less degree of freedom to alter the shape of the winding
- Same thickness of all the segments in a turn
  - An optimized solution is preferred

5. References

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***"Investigation, development and verification of printed circuit board embedded air-core solenoid transformers"*,**
IEEE Applied Power Electronics Conference and Exposition, Charlotte, NC, March 2015. Conference Proceedings.

Investigation, development and verification of printed circuit board embedded air-core solenoid transformers

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***Abstract*— A new printed circuit board embedded air-core transformer/coupled inductor is proposed and presented. The transformer is intended for use in power converter applications operating at very high frequency between 30 MHz to 300 MHz. The transformer is based on two or more solenoid structures in different configurations. The different configurations are compared for usefulness as a transformer solution, and an analytical model of the inductive parameters for the most suitable configuration is derived for design purpose. The analytical model is verified by comparing calculations and measurements of prototypes. The analytical model shows good agreement with the measured results. The model can predict the inductive parameters of the transformer with a deviation range of approximately 3 % to 22 %. Lastly a prototype is used in a VHF converter to achieve a rise of 2.2% points in efficiency.**

I. Introduction

The increasing demand from consumers and industry for high power density converters is leading to continuous work on resonant switch-mode power supplies (SMPS) switching in the very high frequency (VHF) range between 30 MHz to 300 MHz [1], with designs achieving efficiencies up to approximately 90% [2], [3]. VHF power converters reduces the requirements for inductance and capacitance for a desired output power as the need for energy storing per switching cycle is inversely coupled to the frequency [4]. Galvanic isolation in traditional high-frequency SMPS is usually implemented with an isolation transformer, that utilize a magnetic core. This approach is not suitable for VHF-SMPS as the core-losses will be significant at VHF [5]. Air-core magnetics with the lack of magnetic core removes the core-losses and the possibility of saturation, making them a suitable solution for VHF operation with the converters low inductance requirements. Air-core magnetic design can be implemented into a printed circuit board (PCB) [6]–[14], and can be implemented with different structures. This paper propose an implementation and analytic inductance model of a PCB embedded rectangular solenoid air-core transformer. First the concept of PCB embedded solenoid transformers is introduced, followed by an evaluation of different winding configurations. An analytic model of the inductive parameters is developed for the most promising configuration and finally the model is verified by measurement of implemented prototypes, together with the use of a coupled inductor in a VHF resonant converter, showing improved efficiency.

II. Transformers

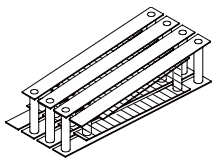
Transformers in general exist in a vast number of designs, most focused on versions with a core to guide the flux to achieve a good coupling between the primary and secondary side. Air-core transformers can also be made in many designs, but are for practical purposes limited to structures that in it self will guide the flux through a common winding area, since there is no core to help guiding the flux. Spiral and toroid PCB embedded air-core transformer structures have previously been proposed [10], [13]. In this paper the solenoid PCB embedded air-core transformer is proposed.

A. Printed circuit board embedded air-core transformers

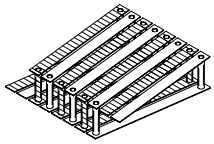
The idea behind PCB embedded air-core transformers is to utilize the easy, cheap and consistent production method of PCBs with air-core magnetics. In general air-core magnetics are considered a viable solution for magnetic components in converters operating in the VHF range since they do not have any core losses, which in a normal core based transformer would be very high [5]. The disadvantages are the low inductance, coupling and typically a larger external magnetic field, due to the missing magnetic material [8] . The 3D transformer structures are created in the PCB by using areas of copper in a two or more layer PCB as horizontal wires and by using vias as vertical wires.

1) Solenoid transformers: The PCB embedded rectangular air-core solenoid transformer can be designed in different configurations, where two main configurations are investigated here. The solenoid transformer is either built up by having a solenoid winding structure nested inside a slightly larger solenoid structure, embedded in a minimum

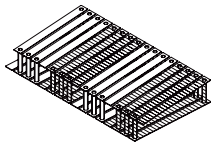
four layer PCB, giving the transformer a rectangular cross section as seen in Figure 1a, or built up by having two or more windings in an interleaved pattern on the same layers. The interleaved configurations ranges from the bifilar configuration to the end-to-end configuration as seen in Figures 1b to 1d. The interleaved configurations can be implemented in a two layer PCB.



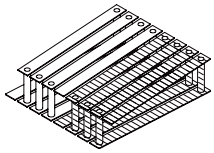
(a) Nested



(b) Bifilar



(c) Sections (4:4)



(d) End-to-end

Fig. 1. Different winding configurations of rectangular PCB embedded air-core solenoid transformers

III. Comparison

In this section different configurations similar to each of the configurations shown in Figure 1 is evaluated for their inductive parameters and coupling. A good transformer will have a high coupling to efficiently transfer energy from the primary side to the secondary.

A. Transformer parameters

The inductive model of a transformer can be defined as a two-port passive device and is described by the inductance matrix [15] in (1). The inductance matrix consists of the self-inductance for each winding L_{pp} and L_{ss}. L_{ps} and L_{sp} are the mutual inductance, and is determined by the flux that flows through the mutual area of the transformer. Note that L_{ps} and L_{sp} are equal since the transformer is a passive device.

$$\begin{bmatrix} v_p(t) \\ v_s(t) \end{bmatrix} = \begin{bmatrix} L_{pp} & L_{ps} \\ L_{sp} & L_{ss} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_p(t) \\ i_s(t) \end{bmatrix} \tag{1}$$

The coupling ratio is defined as (2), and is a ratio of how much flux couples between the primary and secondary windings. In regular transformers wound around a core, the coupling is in the range of $k = 0.99$ for the best [15].

$$k = \frac{L_{ps}}{\sqrt{L_{pp} L_{ss}}} \tag{2}$$

The measurement of the inductance matrix defined in (1) was carried out by measuring the S-parameters [13] on a Agilent 4396B, set up as a vector network analyzer. The S-parameter measurements are converted to Z-parameters [16] and then inductances by (3).

$$L = \frac{\Im(Z)}{\omega} \tag{3}$$

B. Evaluation of configurations

Prototypes in each of the configurations similar to the ones shown in Figure 1 were produced and measured. The prototypes are shown in Figure 2. The resulting inductances, in Table I, used for comparison are mean values from 1 MHz to 10 MHz, to remove any small measurement noise. The impedances measurements of the prototype transformers, are shown in Figure 3.

TABLE I
Inductances of different configurations of PCB embedded solenoid transformers

Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	67.40	17.62	9.58	0.70

(a) Nested configuration

Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	42.25	18.95	41.87	0.45

(b) Bifilar

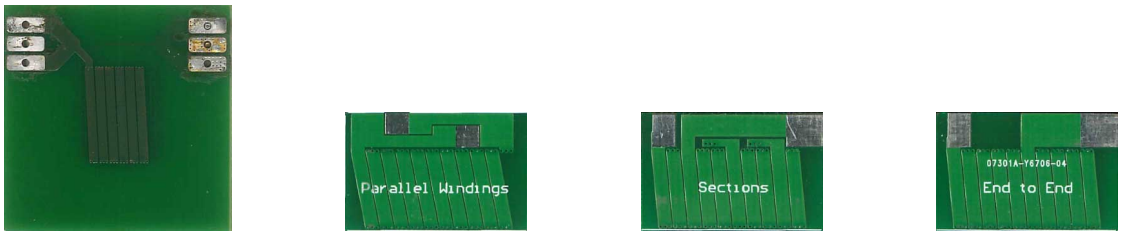
Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	40.95	10.52	38.81	0.26

(c) Interleaved in sections (2:2)

Variable	L_{pp}	L_{ps}	L_{ss}	k
Measured [nH]	41.00	3.22	39.45	0.08

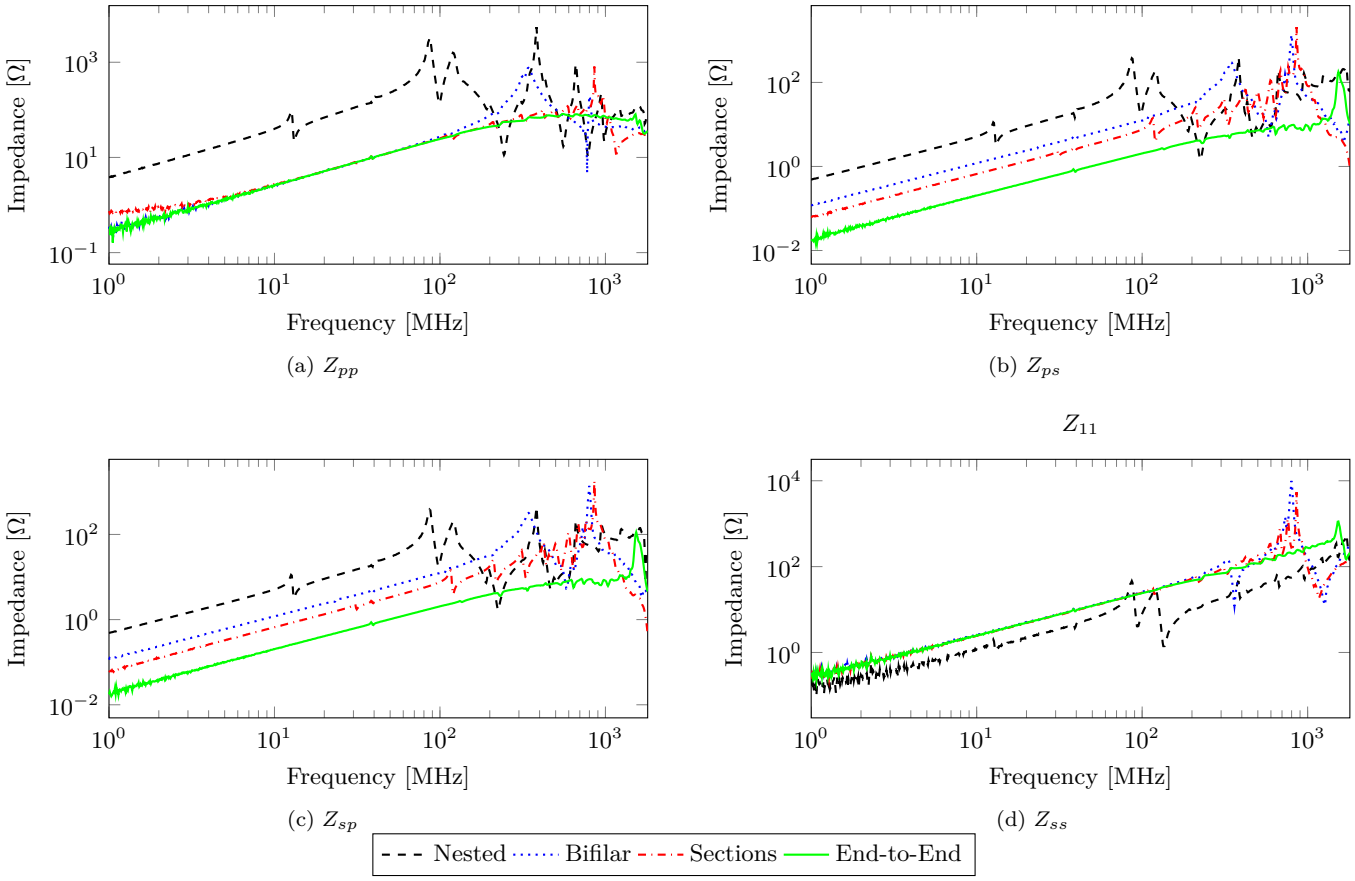
(d) End-to-end

The interleaved configurations shows coupling in the range from $k = 0.08$ to $k = 0.45$. The more intertwined the primary and secondary side is, the higher the coupling. The coupling is in general limited by the clearance between the traces / sections on the PCB, leaving the end-to-end configuration with very bad coupling for a transformer. The sections configuration shows better properties with the bifilar configuration as the optimum of the interleaved with a coupling of $k = 0.45$. Compared to the nested configuration, the interleaved configurations are inferior, as the coupling is $k = 0.7$ for the nested configuration. This coupling coefficient is suitable for a VHF converter as the leakage inductance can be used in the design of the converter. As the nested configuration is the most promising, the inductance formulas for inductance matrix will be derived and evaluated.



(a) Nested (b) Bifilar (c) Sections (d) End-to-end

Fig. 2. Examples of PCB embedded air-core solenoid transformers with different winding configurations. Scale 1:1



(a) Z_{pp} (b) Z_{ps}

(c) Z_{sp} (d) Z_{ss}

Fig. 3. Impedances of different winding configurations of the PCB embedded air-core solenoid transformer

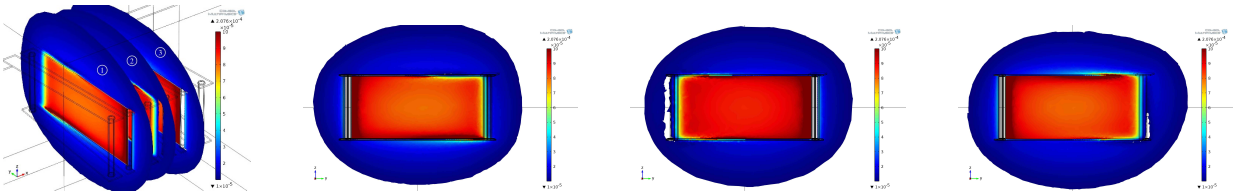
IV. Analytic model

In this section the nested configuration is analytically analyzed. The cylindrical solenoid transformer is a classic textbook example in the magnetic literature, with relatively simple equations [17]. The general equations for a solenoid inductor with a rectangular cross section was derived in [18], the short version given in [19]. The formula is valid as long as the width is greater than the height of the inductor, which, for all practical purposes, is the case for PCB embedded solenoids. There are no equations in the literature for solenoid transformers with rectangular cross sections, so the model will be deduced here. The following assumptions are made to simplify the model expression:

- The lengths of each solenoid structure are equal
- The flux is evenly distributed inside the solenoid.

The assumption that the flux is evenly distributed inside the the solenoid is an approximation, and will be a source of error. The approximation is made on basis of 3D finite element simulations made in COMSOL of a single inductor. An example of the strength of the magnetic field is shown in Figure 4. The flux is slightly concentrated where there is a wire or a via, but is on average close to an evenly distribution.

1) Inductance formula: For the self-inductance L_{pp} and L_{ss} the equation is given in (5) [19], with the respective



(a) Overview (b) Sample 1 (c) Sample 2 (d) Sample 3

Fig. 4. Flux distribution in a PCB solenoid inductor

heights h, widths w and numbers of turns N for the primary and secondary side respectively. The dimensions can be seen in Figure 5. For reference the inner structure of windings is denoted the primary side and the outer the secondary. g is given by (4).

$$g^2 = w^2 + h^2 \tag{4}$$

The mutual inductance, L_{ps} or L_{ps}, is determined by the shared flux, which will pass through the windings mutual area inside the transformer. The mutual inductance must therefore be the same inductance formula (5) as the inner solenoid with respect to the width and height but with the number of turns as $N^2 = N_p N_s$.

$$\begin{aligned} L = {} & 8 \cdot 10^{-9} N^2 \frac{hw}{l} \\ & \left[\frac{1}{2}\frac{l}{h} \sinh^{-1}\left(\frac{w}{l}\right) + \frac{1}{2}\frac{l}{w} \sinh^{-1}\left(\frac{h}{l}\right) \right. \\ & - \frac{1}{2}\left(1 - \frac{h^2}{l^2}\right)\frac{l}{h} \sinh^{-1}\left(\frac{w}{l\sqrt{1+\frac{h^2}{l^2}}}\right) \\ & - \frac{1}{2}\left(1 - \frac{w^2}{l^2}\right)\frac{l}{w} \sinh^{-1}\left(\frac{h}{l\sqrt{1+\frac{w^2}{l^2}}}\right) \\ & - \frac{1}{2}\frac{h}{l} \sinh\left(\frac{w}{h}\right) \quad - \frac{1}{2}\frac{w}{l} \sinh^{-1}\left(\frac{h}{l}\right) \\ & \left. + \left(\frac{\pi}{2} - \tan^{-1}\left(\frac{wh}{l^2\sqrt{1+\frac{g^2}{l^2}}}\right)\right) \right. \\ & + \frac{1}{3}\frac{l^2}{wh}\sqrt{1+\frac{g^2}{l^2}}\left(1 - \frac{1}{2}\frac{g^2}{l^2}\right) + \frac{1}{3}\frac{l^2}{wh} \\ & - \frac{1}{3}\frac{l^2}{wh}\sqrt{1+\frac{w^2}{l^2}}\left(1 - \frac{1}{2}\frac{w^2}{l^2}\right) \\ & - \frac{1}{3}\frac{l^2}{wh}\sqrt{1+\frac{h^2}{l^2}}\left(1 - \frac{1}{2}\frac{h^2}{l^2}\right) \\ & \left. + \frac{1}{6}\frac{l}{wh}\left(\frac{g^3 - w^3 - h^3}{l^2}\right)\right] \end{aligned} \tag{5}$$

A. Verification

The nested configuration is produced in different windings ratios, sizes, and coupling ratios to validate the formulas. The transformers are produced in a standard 4 layer PCB configuration. The full configuration of the prototypes is listed in Table II. A prototype transformer is shown in Figure 2a.

TABLE II

Parameters of the nested configuration solenoids

	Dimensions [mm]					**Turns**	
Prototype	w_p	h_p	w_s	h_s	l	N_p	N_s
1	23.2	1.24	25	1.6	10.3	19	19
2	6.6	1.24	8.2	1.6	6.5	7	2
3	16.1	1.24	17.7	1.6	7.4	15	2
4	5.2	1.24	6.8	1.6	5.7	7	2

The measured inductances shown in Table III fit closely to the calculated with the highest deviation between calculated and measured being 18.7%. The coupling has a higher deviation than the inductances, since it is a combination of the deviations of the inductances, but still with a maximum deviation of 21.8%, which is comparable to formulas for other structures [20]. The inductance equations is in general good enough to use for design of transformers or coupled inductors.

TABLE III

Comparison of analytic model and measurements

Variable	L_{pp}	L_{ps}	L_{ss}	k
Calculated [nH]	1119.17	1119.17	1499.16	0.86
Measured [nH]	1154.33	1104.82	1506.57	0.84
Δ [%]	3.05	1.30	0.49	2.89

(a) Solenoid transformer

Variable	L_{pp}	L_{ps}	L_{ss}	k
Calculated [nH]	65.98	20.91	9.17	0.85
Measured [nH]	67.40	17.62	9.58	0.70
Δ [%]	2.11	18.71	4.21	21.78

(b) Solenoid transformer - 2

Variable	L_{pp}	L_{ps}	L_{ss}	k
Calculated [nH]	596.30	86.45	15.77	0.89
Measured [nH]	592.14	76.84	18.54	0.74
Δ [%]	0.70	12.50	14.95	20.54

(c) Solenoid transformer - 3

Variable	L_{pp}	L_{ps}	L_{ss}	k
Calculated [nH]	52.47	16.64	7.68	0.83
Measured [nH]	53.40	14.17	8.22	0.68
Δ [%]	1.75	17.42	6.63	21.83

(d) Solenoid transformer - 4

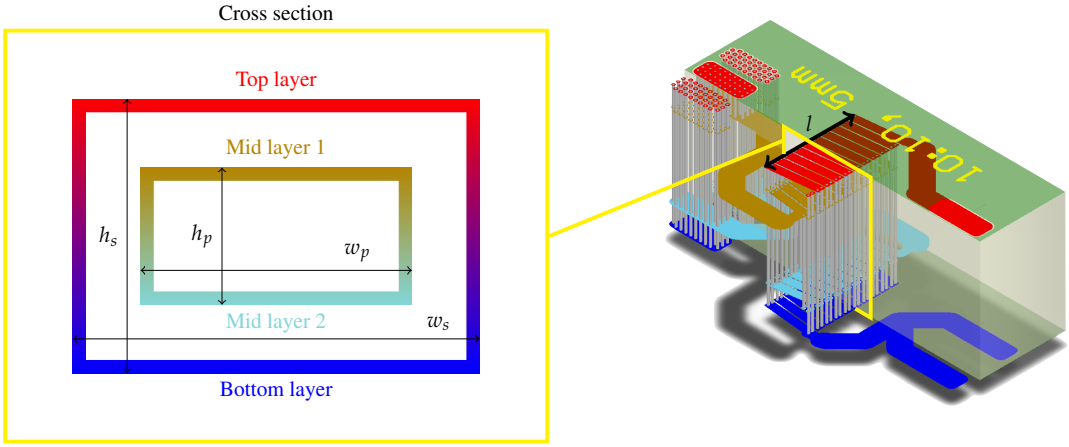


Fig. 5. Dimensions of the PCB embedded solenoid transformer (nested configuration)

V. Applied design

The nested configuration is used in an half-bridge VHF resonant power converter presented in [21]. The converter is a class-DE type, with a passive gate drive [22] for both the high-side and low-side. Each gate drive circuit has an inductor $L_{G(1,2)}$ in series with the MOSFETs gate. For the class-DE converter to work properly in the VHF area, the switch timing between the high-side and low-side is critical. The two separate inductors can be made by a coupled inductor instead, which will force the gate currents to be 180°phase-shifted, and ensure a better timing, resulting in higher efficiency. As the gate drive circuit should see the same inductance as when the gate inductors are not coupled, the primary L_{pp} and secondary inductances L_{ss} values should be chosen so the leakage inductance corresponds to the original L_G, leading to (6). If the coupling is close to one, the inductances would go to infinity, hence large couplings are for any applied purpose unpractical, as the coupled inductor will be very large. A coupling of $k = 0.6$ is chosen as a good compromise, leading to an inductance matrix of (7).

$$L_{pp,ss} = \frac{L_G}{1-k} \tag{6}$$

$$\begin{bmatrix} L_{pp} & L_{ps} \\ L_{sp} & L_{ss} \end{bmatrix} = \begin{bmatrix} 375\text{nH} & 225\text{nH} \\ 225\text{nH} & 375\text{nH} \end{bmatrix} \tag{7}$$

A. Coupled inductor design

The coupled inductor is designed with the formulas presented in Section IV, with the simplifications implemented. The length of the inductors are matched (as close as possible) and the widths w_p and w_h are set as close as possible. The PCB production sets certain limits on the inductors, e.g. as the width of each trace can be no smaller than the minimum via hole size, the clearance between the traces, as well as the width of the inner inductor must have a minimum clearance to the outer inductor, etc.

All the restrictions does that not all combination of L_{pp}, L_{ss} and L_{ps} can be obtained. The specific design is found using a genetic algorithm to optimize the transformer to the given inductance matrix. The algorithm has been set to favorite the leakage inductance to ensure the high-side and low-side gate-drive are matched.

B. Experimental

The class-DE converter from [21] is used as base performance. The schematic is shown in Figure 6, with the corresponding component values in Table IV.

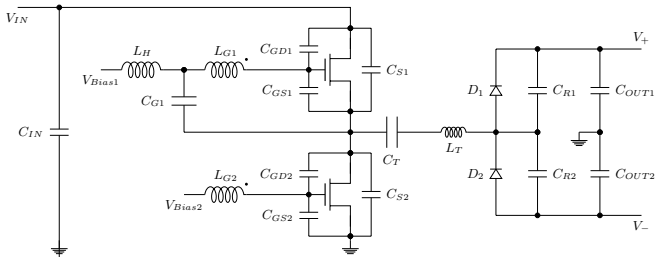


Fig. 6. Converter schematic of the class-DE inverter with coupled inductors in the self-oscillating gate drive

TABLE IV
Component values for class-DE converter

Component	Value
C_{in}	4.7nF
C_s	14pF
C_{GD}	6pF
C_{GS}	82pF
C_{GDext}	39pF
L_G	150nH
C_{G1}	100nF
L_H	3.3µH
C_T	500pF
L_T	360nH
C_R	40pF
C_{OUT}	14nF

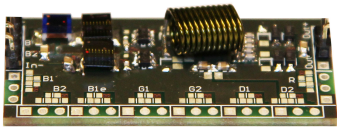
TABLE V
COMPARISON OF THE CLASS-DE CONVERTER WITH DIFFERENT GATE DRIVE INDUCTORS

Converter	L_{pp}	L_{ps}	L_{ss}	k	$L_{pp,leak}$	$L_{ss,leak}$	P_{in}	P_{out}	n
Base configuration	150nH	-	150nH	-	-	-	12.21W	9.57W	78.87%
Leakage based	120nH	-	100nH	-	-	-	10.25W	6.44W	63.1%
Coupled inductor	238.5nH	165nH	333.5nH	0.58	120.5	102.8	11.32W	9.12W	81.09%

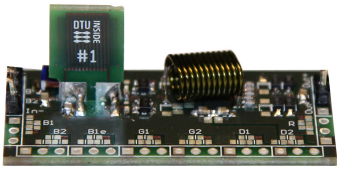
The converter performance is tested at 80V input, and the efficiency is measured with a Yokogawa WT1600. The converter, shown in Figure 7, is tested with three different L_G configurations:

1) The original inductors
2) Inductors with the value of the leakage inductance
3) The coupled inductor

The leakage inductor value, are two separate inductors with the value of the leakage inductance of the coupled inductor. This is to check whether it is the coupling or the slight change in inductance that causes any effect in the circuit. The inductor measurement and efficiencies are shown in Table V. The base efficiency is 78.87%, and with the leakage-valued inductors the efficiency is at 63.1%. The coupled inductor increase the efficiency by 2.2% points from the base value to 81.09%.



(a) Non-coupled gate inductors



(b) Coupled PCB embedded gate driver inductors

Fig. 7. Class-DE converters used for efficiency comparison

VI. CONCLUSION

New structures for PCB embedded air-core transformers was proposed based on the rectangular solenoid structure, for use in VHF converters. The structures were evaluated for the use as a transformer, by comparing the coupling of the transformers. The structure of two solenoids nested inside each other, was found to be the most promising. An analytic two-port model for the structure was developed and verified by measurements on prototypes of the configuration. The formula shows a good consistency between the calculated and measured inductances, with a deviation range of approximately 3 % to 22 %. The proposed analytical model is suitable to predict the inductive parameters of the nested configuration of the PCB embedded air-core solenoid transformers.

The use of a coupled inductor in the self-oscillating gate drive in a class-DE converter shows that PCB embedded air-core solenoid inductor are suitable for using in VHF converters.

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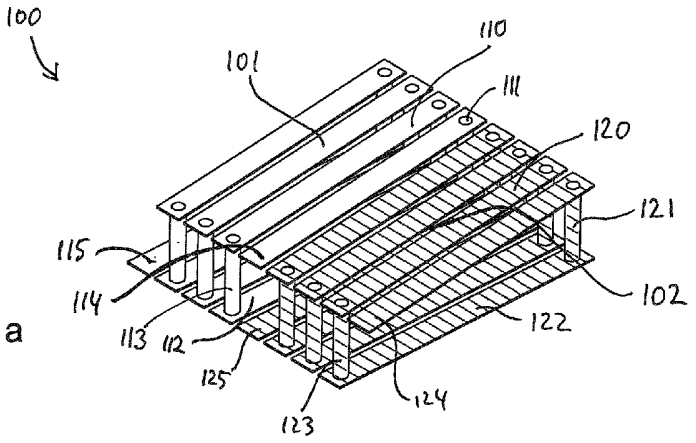

Fig.1a

(57) **Abstract**: A resonant power converter for operation in the radio frequency range, preferably in the VHF, comprises at least one PCB-embedded transformer. The transformer is configured for radio frequency operation and comprises a printed circuit board defining a horizontal plane, the printed circuit board comprising at least two horizontal conductive layers separated by an isolating layer, a first embedded solenoid forming a primary winding of the transformer and a second embedded solenoid being arranged parallel to the first solenoid and forming a secondary winding of the transformer, wherein the first and second embedded solenoids are formed in the conductive layers of the printed circuit board, wherein each full turn of an embedded solenoid has a horizontal top portion formed in an upper conductive layer, a horizontal bottom portion formed in a lower conductive layer, and two vertical side portions formed by vias extending between the upper and the lower conducting layers.

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EMBEDDED SOLENOID TRANSFORMER FOR POWER CONVERSION

The present invention relates in one aspect to a transformer for radio frequency operation comprising a printed circuit board defining a horizontal plane, the printed circuit board comprising at least two horizontal conductive layers separated by an isolating layer, a first solenoid forming a primary winding of the transformer and a second solenoid being arranged parallel to the first solenoid and forming a secondary winding of the transformer.

According to a further aspect, the invention relates to a power converter operating at radio frequencies and comprising a transformer of the above-mentioned kind. More particularly, the invention relates to a resonant DC-DC converter operating at radio frequencies and comprising a transformer of the above-mentioned kind.

BACKGROUND OF THE INVENTION

Over many years there has been a constant need for small, cheap and efficient power supplies. This has led to the development of Switch-Mode Power Supplies (SMPS). The size of modern power supplies are mainly governed by the passive energy storing elements, which scales inversely with the switching frequency. Therefore, much development has been devoted to increasing switching frequencies. Commercially available converters today switch at frequencies up to several megahertz and can have efficiencies of more than 95%. The reason for not increasing the switching frequency further and thereby reaching even higher power densities are switching losses. One way of addressing this issue has been the use of resonant Radio Frequency (RF) amplifiers (inverters) combined with a rectifier for DC-DC converters. With this type of converters, SMPSs with switching frequencies in the Very High Frequency range (VHF, 30- 300MHz) have been designed with efficiencies up to approx. 90%. By operating the DC-DC converters at radio frequencies, or even at VHF frequencies, it is possible to reduce the size, and thereby also price, of the passive energy storing elements significantly. However, the inductive components, and in particular the power transformers, are still the largest components in the circuits. Therefore, there is a need for small and highly efficient transformers.

Object of the present invention is therefore to provide a transformer for radio frequency operation, with a small and efficient design that can be reliably produced at low cost.

DEFINITIONS

Throughout the present text, the term “conductive” refers to electrically conductive. The term “isolating” refers to electrically isolating. The term “coupled” is to be understood as a galvanically separated electromagnetic coupling, which is to be distinguished from electrically “connected” referring to a galvanic connection through a conductive material.

Depending on the particular use, a transformer may sometimes also be referred to as coupled inductors. The term “transformer” usually refers to devices adapted for power transfer. Transformers require a high level of coupling to avoid inhibitive losses. The term “coupled inductors” is usually employed when referring to devices adapted for signal transfer, where a lower level of coupling may still be useful or maybe even desirable for a particular application. However, the topologies of a transformer and of coupled inductors cannot be distinguished in practice. Therefore, throughout the present application, the terms transformer and “coupled inductors” are treated as interchangeable.

When arranged in a circuit, a transformer may be operated in different configurations depending on the way the transformer is connected into the circuit. When referring to an “isolating transformer”, it is to be understood that a given transformer is connected in an isolating configuration. Accordingly, when referring to an “autotransformer” it is to be understood that the transformer is connected in an autotransformer configuration.

When referring to power converters, this includes any of a DC-DC converter, an AC-DC converter, an AC-AC converter, and a DC-AC converter.

The term “horizontal” refers to directions parallel to the plane of the printed circuit board (PCB). The term “vertical” refers to directions perpendicular to the horizontal plane defined by the printed circuit board, wherein a first vertical direction points in

an upward direction, and a second vertical direction opposite to the first vertical direction points in a downward direction, wherein a vector pointing from a "lower" element to an "upper" element has an upward pointing vertical component.

The term "parallel" covers geometries with a lateral offset as well as coinciding geometries without offset, i.e. when referring to parallel axes coinciding axes are also covered. In this context, the orientation of a solenoid is determined by the direction of its longitudinal axis. Any angle between solenoids including the angle zero, i.e. a configuration with parallel solenoids, is thus to be understood as the angle between the respective longitudinal axes of the solenoids.

SUMMARY OF THE INVENTION

According to a first aspect, the object of the invention is achieved by a resonant power converter for operation in the radio frequency range, preferably in the VHF, the power converter comprising at least one transformer, wherein the at least one transformer comprises

- a printed circuit board defining a horizontal plane, the printed circuit board comprising at least two horizontal conductive layers separated by an isolating layer,
- a first embedded solenoid forming a primary winding of the transformer and
- a second embedded solenoid being arranged parallel to the first solenoid and forming a secondary winding of the transformer,

wherein the first and second embedded solenoids are formed in the conductive layers of the printed circuit board, wherein each full turn of an embedded solenoid has a horizontal top portion formed in an upper conductive layer, a horizontal bottom portion formed in a lower conductive layer, and two vertical side portions formed by vias extending between the upper and the lower conducting layers. In general, a single winding formed in this way may already be considered as a PCB-embedded solenoid.

Thereby an efficient power converter is achieved with a small size, which can be produced in an automated manner with high reproducibility and at low cost. The power converter may be any of a DC-DC converter, an AC-DC converter, an AC-AC converter, and a DC-AC converter.

Further according to one embodiment of the power converter, at least one of the transformers is arranged as an isolating transformer between an input side and an output side. In such a configuration, the power passed through the converter is transferred from an input side of the converter through the isolating transformer to the output side of the converter. Therefore, a good coupling between the first and second solenoids is required to avoid excessive losses, such as a coupling factor k above 0,6 or preferably above 0,8.

Further according to one embodiment, the power converter is a resonant DC-DC converter. In this context the term DC can refer to a slowly varying voltage. In the context of a switch mode power converter, the term “DC” may thus be considered fulfilled as long as the variation of the DC-voltage level is slow as compared to the switching frequency of the power converter. When building a resonant DC-DC converter, a good coupling between the first and second solenoids is desired in order to achieve an efficient resonant operation of the power converter. This is achieved by using a PCB-embedded transformer of the solenoid type as disclosed in the present application. Advantageously, this may be such a PCB-embedded transformer with bifilar interleaved first and second solenoids, wherein single turns of the first solenoid alternate with single turns of the second solenoid. Alternatively, this may advantageously also be a PCB-embedded transformer formed in a multilayer PCB, such as a four-layer PCB, wherein the second solenoid is arranged inside the first solenoid as seen in a cross-sectional plane perpendicular to a longitudinal axis of the solenoids (or vice versa).

Furthermore, by using a PCB-embedded transformer of the solenoid type as disclosed in the present application for coupling first and second solenoids in a resonant DC-DC power converter, a particularly small form factor, low profile (i.e. a low vertical dimension), low weight, and low production cost is achievable. Furthermore, using a PCB-embedded transformer in a power converter as described in the present invention has the advantage that the foot-print of the transformer may be shaped as desired by the circuit designer. This freedom of design gives a considerable flexibility to the circuit designer and is particularly relevant when the available space is a critical parameter.

The above-mentioned advantages are particularly useful, for example when integrating a power converter into LED-lighting devices or flat-screen displays, due to the very stringent spatial limitations in such lighting applications. In particular the limitations on the vertical dimensions (low profile) of the converters are very demanding in these applications. These challenges can be met by a power converter including PCB-embedded transformer as disclosed by the present invention. The above-mentioned advantages are also useful, for example when building charging devices as e.g. used in many mobile consumer devices, due to the reduced weight and an enhanced mechanical stability that may be achieved thereby.

Further according to one embodiment of the power converter, a switching frequency on the input side is at least 10 MHz, preferably at least 20 MHz, more preferably at least 30 MHz. This operation range of the power converter is particularly advantageous for the resonant DC-DC converter.

Operating in this frequency range facilitates the use of embedded transformers in a particularly advantageous way for designing efficient power converters. The choice of operating at frequencies of at least 10MHz, at least 20Mhz, or even at least 30MHz synergistically adds to the above-mentioned advantages of a low overall form factor, low profile, low weight, freedom of design, etc. For example, the possibility of an efficient coreless transformer design of the embedded PCB-transformer configured for operation in the VHF as discussed in this application avoids losses in a core material; the low capacitance needed when operating at these frequencies makes it possible to use ceramic capacitors which have a much longer lifespan than electrolytic capacitors; at these frequencies a rapid transient response and a small component form factor can be achieved; the smaller size of the components required leads to a reduced cost of components and a cheaper assembly, thereby reducing the overall production cost for the power converter. In particular, designing the power converter as a resonant power converter facilitates a particularly efficient operation at the above recited switching frequencies.

Further according to some embodiments of the resonant power converter, the transformer is provided according to one of the advantageous embodiments as detailed in the following.

According to a broader aspect, the object of the invention is achieved by a transformer for radio frequency operation, the transformer comprising

- a printed circuit board defining a horizontal plane, the printed circuit board comprising at least two horizontal conductive layers separated by an isolating layer,
- a first embedded solenoid forming a primary winding of the transformer and
- a second embedded solenoid being arranged parallel to the first solenoid and forming a secondary winding of the transformer,

wherein the embedded solenoids are formed in the conductive layers of the printed circuit board, wherein each full turn of an embedded solenoid has a horizontal top portion formed in an upper conductive layer, a horizontal bottom portion formed in a lower conductive layer, and two vertical side portions formed by conductive vias extending between the upper and the lower conducting layers.

By using solenoids embedded in a PCB in a transformer arrangement, an embedded solenoid transformer is obtained. An embedded solenoid transformer has several advantages over other configurations as further detailed in the following.

The printed circuit board is stratified with a vertical stacking direction, i.e. different layers of the printed circuit board are oriented horizontal and parallel to each other. At least one isolating layer usually also forms the carrier layer. In a multilayer PCB, the stacked layers may in combination form a carrier layer.

The embedded solenoids are helical coils wound around a horizontal axis that defines a longitudinal direction of the solenoid. In a preferred embodiment, each coil is formed by a series of traces of conductive material patterned into the horizontal conductive layers of the PCB. The traces are electrically connected in series by means of vias penetrating the isolating layer in a vertical direction to form a horizontal coil embedded in the PCB. Top portions of the coil that are formed by traces in an upper conductive layer alternate with bottom portions that are formed by traces in a lower conductive layer. Starting with a top portion, a full turn of a coil is thus formed, by the top portion, followed by a downward via, a bottom portion, and an upward via. Each of the upward and downward vias may also be formed by multiple vias that are coupled in parallel, thereby lowering the total resistance of the turn.

The embedded solenoid transformer is easy to scale by merely adjusting the layout of the traces forming the top and bottom portions and the positions of the vias.

The embedded solenoids have an essentially rectangular cross-section as seen in a cross-sectional plane perpendicular to the longitudinal axis. Typically, the rectangular cross-section has a slab-like shape with a flat aspect ratio where the vertical dimension is smaller than the horizontal dimension.

The first and second solenoids are placed next to each other, with partial overlap, or with full overlap, and are inductively coupled. The coupling may be external, i.e. through the external field of the solenoids, and/or internal, i.e. through the internal field of the solenoids.

Advantageously according to a preferred embodiment, the transformer is “coreless”, i.e. the solenoids are not coupled through a magnetically conducting material. The term “coreless” is thus to be understood as to also include embodiments where the transformer is coupled through a magnetically non-permeable material, such as a typical substrate material used for producing printed circuit board. For example, the embedded solenoids may be wound about, and thus filled with, such magnetically non-permeable material. Such coreless embodiments are in the following also referred to as “air-core”. Such coreless transformer arrangements have the advantage that they are easier to produce than an embedded transformer with core-based coupling. Furthermore, such coreless embodiments have the advantage that they are not subject to dissipation due to losses in a core material.

Advantageously according to a preferred embodiment, the first and second solenoids are embedded on the same PCB. Thereby, additional assembly steps can be avoided, which may carry the inherent risk of misalignment and reduced precision. As a consequence, reliable and reproducible high-volume production of the embedded transformer can be achieved.

In the most general configuration, the longitudinal axes of the first and second solenoids may have an arbitrary angle with respect to each other. However, in order to achieve an appropriate coupling, in particular in an air-core configuration, the longi-

tudinal axes of the first and second solenoids are arranged parallel to each other. Furthermore, the first and second solenoids may have an essentially rectangular footprint on the PCB as seen in projection in a horizontal plane. Owing to that rectangular footprint, the embedded transformer built from the first and second solenoids can be designed to fit easily into a complete circuit design which most frequently also has rectangular layout geometry.

According to one embodiment, an embedded transformer relies on external coupling through a horizontal side-by-side arrangement, or a vertical arrangement of two solenoids stacked on top of each other. This structure is easy to implement and it is very easy to make more than one primary or secondary winding. Each winding will give the best possible inductor in terms of inductance divided by the series resistance of the inductor, but at the price of a considerably lower coupling between the first and second solenoids than for other arrangements.

As mentioned above, the use of embedded solenoids for the embedded transformer has a number of advantages over other coil geometries. For example, as compared to spiral windings solenoids have the benefit that the current is more evenly distributed over the full width of the traces, whereas the current density of spirals tends to concentrate at one edge of the traces. Therefore the solenoid geometry can achieve a lower series resistance of the coil, in particular for large structures. Furthermore, as mentioned above, solenoids have a rectangular footprint with connectors that are typically arranged at the corners of the structure. From a design flexibility point of view this is preferable over the round structure of a spiral with one connector in the center of the structure. Furthermore the external magnetic field from the solenoid geometry is much weaker than for the spiral geometry, thereby reducing the risk of failing electromagnetic interference requirements. In a further example, as compared to toroidal coil geometries, solenoids have lower series resistance as the viases in the solenoid geometry are distributed equally on both sides of the traces, whereas in the toroidal structure would result in a concentration of the current density in the vertical viases at the inner edge of the toroid. Furthermore, the rectangular footprint of the solenoid geometry is again to be considered an advantage from a circuit designer's point of view as compared to the round shape of toroids, amongst others due to a higher inductance per area, better usage of footprint, and better de-

sign compatibility with rectangular geometry circuit layouts. Furthermore, a surprisingly good coupling efficiency can be achieved as compared to e.g. toroidal structures.

Further according to one embodiment of the transformer, the first and second solenoids are wound around a common axis. Thereby an improved coupling between the first and second solenoids is achieved as compared to e.g. a horizontal side-by-side arrangement, or a vertical arrangement of two solenoids stacked on top of each other.

Further according to one embodiment of the transformer, the first and second solenoids at least partially overlap in a longitudinal direction. In the region of the overlap, the coupling between the first and second solenoids is achieved via the internal magnetic field in the region of the overlap. Thereby an improved coupling is achieved as compared to geometries relying on an external coupling. The overlap may be partial or, preferably, over the full lengths of the first and/or second solenoids. The overlap may be achieved in different geometries as further detailed below.

Further according to one embodiment of the transformer, top portions of the first and second solenoids are formed in a common upper conductive layer, and/or bottom portions of the first and second solenoids are formed in a common lower conductive layer. This embodiment has the advantage that it only requires two conductive layers. This is advantageous for a cheap and reliable production of the embedded solenoid transformer, for example in a dual layer PCB.

Advantageously according to one embodiment, the PCB of the transformer is a dual layer PCB.

Further according to one embodiment of the transformer, the first and second solenoids are section-wise interleaved. This embodiment may be considered a hybrid of external and internal coupling between the first and second solenoids, wherein each of the sections are tightly packed coils with an optimum inductance divided by the series resistance. The sections of the first and second solenoids are all aligned on a

common axis, thereby sharing a common magnetic path with a good coupling efficiency. This embodiment has the advantage that it allows for providing more than one primary and/or secondary winding in a simple layout.

Further according to one embodiment of the transformer, first sections of the first solenoid alternate with second sections of the second solenoid. The first and second sections share a common magnetic path with a good coupling efficiency.

Further according to one embodiment of the transformer, first sections are single turns and/or second sections are single turns. Thereby, in the region of the overlap, the solenoids are fully interleaved turn by turn. To make space for this interleaving, the axial pitch (distance between adjacent turns in an axial direction) of the respective solenoids needs to be increased. This has the disadvantage that the series resistance for a given inductance of the respective solenoids increases. However, the embodiment has the advantage that a highly efficient coupling between the interleaved solenoids is achieved for a two-layer embedded structure.

Further according to one embodiment of the transformer, the PCB has at least four-layers. This embodiment allows for more complex transformer geometries.

Further according to one embodiment of the transformer, when seen in a cross-sectional plane perpendicular to a longitudinal axis of the solenoids, the second solenoid is arranged inside the first solenoid or, alternatively the first solenoid is arranged inside the second solenoid. This embodiment needs to be implemented in at least a four layer PCB. Despite the inherent reduction of the overlap in cross-sectional area shared by the first and second solenoids (the inside solenoid has inherently a smaller cross-section than the outside/enclosing solenoid), a surprisingly high coupling efficiency is achieved in this embodiment as compared to embodiments implemented in a two-layer PCB configuration, such as even the fully interleaved configuration with alternating single turns.

Furthermore, for a given application this embodiment has a smaller footprint than the above-mentioned embodiments, and magnetic flux is encapsulated better than in e.g. the interleaved structure as the turns of each of the windings is placed as

close as possible. This structure can also be preferable for galvanic isolation applications as the isolation is achieved through the layers of the PCB, which typically requires much shorter separation distances than isolation along the surface within the same layer. Preferably, the first solenoid forming the primary side is the inner solenoid, and the second solenoid forming the secondary winding is the outer solenoid enclosing the inner solenoid.

Most preferably, first and second solenoids are arranged concentrically. Thereby an optimum coupling efficiency is achieved.

Further according to some embodiments, the power converter comprises further solenoids coupled to the first solenoid and/or the second solenoid. By adding further windings/solenoids a transformer with multiple input and/or output windings can be formed.

Further according to one embodiment of the invention, the transformer is adapted for operation at a radio frequency in the range 1MHz – 1 GHz; alternatively 10 MHz – 500 MHz; further alternatively 30 MHz – 300 MHz. The typical dimensions of PCB structures are particularly suited for viable operation of power electronics in the radio frequency range, in particular around and above 1 MHz, and more particular in the VHF-ranges given above. Since at these frequencies the skin depth is around 10µm (micrometer), the penetration of the current into the conductor is comparable to and even less than the thickness of the conductive layers of a typical PCB. Typical PCBs have conductive layer thicknesses in the range from about 0.1mm down to about 15µm. For example, a so-called “1oz Cu” PCB layer is specified to a copper amount of 1 ounce per sqft, resulting in a copper layer thickness between 30µm-40µm, typically about 35µm. The thickness scales linearly with the copper amount, wherein typical specifications copper layers in a PCB are 1/2oz, 0.75oz, 1oz, 2oz, and 3oz. Due to the small skin depth at high frequencies, the resistance of the solenoid inductors is not significantly affected by the small thickness of typical PCB conductive layers.

Further according to one embodiment of the invention, the transformer has a coupling factor k of above 0,1, preferably above 0,2, preferably above 0,3, preferably

above 0,4, preferably above 0,5, more preferably above 0,6, even more preferably above 0,7, and most preferably above 0,8. Transformers intended for transferring power, e.g. an isolating transformer arranged between an input side and an output side, should have a high coupling factor k, such as above 0,6 or preferably above 0,8 . On the other hand, coupled inductors intended for synchronizing parallel stages in an AC-circuit may already benefit from much lower coupling factors. In fact, it may be beneficial to provide a circuit with coupled inductors having a specified coupling factor that may be chosen within a broad range of coupling factors. The coupling factor may be chosen e.g. by selecting a layout type and/or tailoring the parameters of a given layout, such as illustrated by the examples in the detailed description below.

Further according to one embodiment, at least one transformer is arranged as an isolating transformer between an input side and an output side.

Further according to one embodiment, at least one transformer is arranged as an autotransformer between an input side and an output side.

Further according to one embodiment, at least one transformer is arranged such that the first solenoid is used as a power carrying inductor in the power converter and the second solenoid is used as a sensing inductor to measure the current through the first inductor. The measured current signal may be for display, presentation at a current monitoring output port, and/or for use as a control signal in the power converter itself, or as a control signal in a system including a power converter according to the present invention. The PCB-embedded transformer configuration allows for a simple, space-saving and cost-effective integration of the current sensing arrangement in the power converter.

Further according to particularly preferred embodiments, the power converter is a resonant DC-DC converter.

Further according to preferred embodiments of the power converter, the switching frequency on the input side is at least 10MHz, preferably at least 20MHz, more preferably at least 30MHz.

According to a further aspect, an inverter is adapted for operation at radio frequencies, preferably in the VHF, and comprises a transformer according to any of the above cited embodiments. The transformer structure may be used as coupled inductors for coupling two complementary gate drive signal of first and second semiconductor switches. Thereby an efficient power inverter is achieved with a small size, which can be produced in an automated manner with high reproducibility and at low cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention will be described in more detail in connection with the appended drawings, which show schematically in

FIG. 1a-c an embedded solenoid transformer according to a first embodiment,

FIG. 2a-c an embedded solenoid transformer according to a second embodiment,

FIG. 3a-c an embedded solenoid transformer according to a third embodiment,

FIG. 4a-c an embedded solenoid transformer according to a fourth embodiment,

FIG. 5 a DC-DC converter circuit comprising an embedded transformer according to a first embodiment,

FIG. 6 a class-DE power inverter comprising coupled inductors according to another embodiment,

FIG. 7 a DC-DC converter circuit comprising an embedded transformer according to a second embodiment,

FIG. 8 a DC-DC converter circuit comprising an embedded transformer according to a third embodiment,

FIG. 9 a DC-DC converter circuit comprising an embedded transformer according to a fourth embodiment,

FIG. 10 a DC-DC converter circuit comprising an embedded transformer according to a fifth embodiment, and in

FIG. 11 a DC-DC converter circuit comprising an embedded transformer according to a sixth embodiment.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figs. 1-4 show different layouts for the implementation of a transformer (x00) embedded in a printed circuit board (PCB), wherein in all the shown embodiments the first solenoids (x01) and the second solenoids (x02) are arranged on a common longitudinal axis Z. In the shown embodiments, the conductive paths of each of the solenoids (x01, x02, 203, 204) is made up of slab-shaped horizontal traces (x10, x12, x20, x22, 230, 232, 240, 242) formed in the conductive layers of a printed circuit board having at least two conductive layers, and vertical vias (x11, x13, x21, x23, 231, 233, 241, 243) made of a conductive material connecting the horizontal traces (x10, x12, x20, x22, 230, 232, 240, 242) in series to form a coil. Figs.1 – 3 show embodiments of PCB embedded solenoid transformers that require a PCB with two conductive layers separated by an isolating layer, such as a dual layer PCB. Fig.4 shows an embodiment requiring a multilayer PCB with at least four vertically stacked conductive layers separated from each other by isolating layers. Only the conductive paths forming the solenoids are drawn, whereas isolating layers are omitted in the drawings. Respective sub-figures (a) show perspective views of the conductive paths for both the first and second solenoids (x01, x02), sub-figures (b) show an end view as seen in the direction of the longitudinal axis Z, and sub-figures (c) show a top elevation view of the solenoid arrangements (x00).

Fig.1 shows a first embodiment of a PCB embedded transformer 100 in an end-to-end configuration with a first solenoid 101 having four turns wound around a longitudinal axis Z, each turn having a top portion 110, followed by a downward via 111, a bottom portion 112, and an upward via 113. The first solenoid 101 has first connection terminals 114, 115 for connection to further circuitry. In direct extension to the

first solenoid 101, a second solenoid 102 is formed by four turns wound around the same longitudinal axis Z, each turn having a top portion 120, followed by a downward via 121, a bottom portion 122, and an upward via 123. The second solenoid 102 has connection terminals 124, 125. The end-to end configuration is essentially a solenoid, which has been broken up in two solenoids by omitting the vertical connection between the contact terminals 114 and 125.

Fig.2 shows a second embodiment of a PCB embedded transformer 200 in a section-wise interleaved configuration. The arrangement comprises four identical sections 210, 220, 230, 240 of four turns each, wherein the four sections 210, 220, 230, 240 are aligned along a common longitudinal axis Z. The turns of the solenoid sections 210, 220, 230, 240 are formed in the same way by respective horizontal top and bottom portions connected in series through vertical vias as described above, and each of the sections 210, 220, 230, 240 has respective connection terminals 214, 215, 224, 225, 234, 235, 244, 245. The first and third sections 210, 230 form a primary side of the transformer 200. The first and third sections 210, 230 may be operated as separate first solenoids with four turns each or they may be connected in series for operation as one first solenoid with eight turns. Accordingly, the second and fourth sections 220, 240 form the secondary side of the transformer 200 and may be operated as separate second solenoids or as one second solenoid.

Fig.3 shows a third embodiment of a PCB embedded transformer 300 with two solenoids in a 1:1 interleaved configuration. The transformer 300 has a first solenoid 301 with turns formed by top portions 310, bottom portions 312, and vertical viases 311, 313 connecting alternating top and bottom portions 310, 312 in series to provide a coil as described above. The first solenoid 301 has first connection terminals 314, 315 for connection to further circuitry. A second solenoid 302 is formed accordingly from top portions 320, bottom portions 322, and vertical viases 321, 323. The second solenoid 302 has second connection terminals 324, 325 for connection to further circuitry. Both solenoids 301, 302 are wound around a common longitudinal axis Z. However, in contrast to the above-described embodiments, the pitch of the first and second solenoids (i.e. the distance between adjacent turns within the same solenoid) is doubled to allow for an alternating arrangement of single turns from the first solenoid 301 and from the second solenoid 302. The increased pitch tends to

produce a more leaky solenoid, and somewhat increases the length and thus the resistance of the solenoids with the same number of turns. However, the 1:1 interleaved configuration has the benefit of a considerably increased coupling between the first and second solenoids as compared to other two-layer designs, such as the embodiments mentioned above.

Fig.4 shows a fourth embodiment of a PCB embedded transformer 400, wherein a first solenoid 401 encloses a second solenoid 402. In the shown embodiment, the first and second solenoids are wound around the same longitudinal axis Z in a preferred concentric arrangement. The transformer 400 requires a multilayer PCB with four conductive layers as best seen in Fig.4b. The turns of the outer first solenoid 401 are formed by top portions 410 in an uppermost conductive layer, bottom portions 412 in a lowermost conductive layer and vertical vias 411, 413 connecting alternating top and bottom portions 410, 412 in series. The turns of the inner, second solenoid are formed by top portions 420 in an upper inner conductive layer of the multilayer PCB, bottom portions 422 in a lower inner conductive layer of the multilayer PCB, and vertical vias 421, 423 connecting the top and bottom portions 420, 422 in series. The transformer has primary side connection terminals 414, 415 for connecting the outer, first solenoid 401 to further circuitry, and secondary side connection terminals 424, 425 for connecting the inner, second solenoid 402 to further circuitry. Note, that the role of the inner and outer solenoids may be interchanged, such that the inner solenoid forms the primary side of the transformer 400, and the outer solenoid forms the secondary side of the transformer 400.

Figs.5 and 6 give examples of advantageous uses of PCB embedded solenoid transformers in power converters operating at radio frequencies, preferably in the VHF range.

Fig. 5 shows a class-E isolated resonant DC-DC converter 50, which may be adapted for radio frequency operation, preferably in the VHF. The converter 50 receives a DC-input voltage Vin on an input side 51, and provides a DC-output voltage to a load on an output side 52. The input side 51 may comprise a semiconductor switch, such as a MOSFET, with a control terminal Q1 that may be driven by an external oscillator or e.g. a self-oscillating gate drive circuit as described in the co-

pending International Patent Application PCT/EP2013/072548, and a resonant tank formed by capacitance C2 and L2. The output side 52 may comprise a class-E rectifier, here represented schematically by diode D1, capacitance C3, and inductance L3. Input side 51 and output side are coupled by an isolating transformer T1. Advantageously, the transformer T1 is a PCB embedded solenoid transformer 500 with a primary winding 501 and a secondary winding 502 inductively coupled to the primary winding 501, wherein the coupling designated by the double line may be a coreless coupling.

Fig.6 shows a self-oscillating class-DE power inverter 60 adapted for radio frequency operation, preferably in the VHF. The inverter 60 receives a DC-input voltage Vin at input terminals of an input stage 61, and provides an AC-output voltage in the radio frequency range, e.g. in the VHF, to a load at output terminals of an output stage 62. The input stage 61 may comprise semiconductor switches with control terminals Q1, Q2 and respective drain-source capacitors C2, C3 in a half-bridge configuration, wherein the semiconductor switches are controlled to oscillate with opposite phase. As shown schematically in Fig.6, the oscillation may be driven by a self-oscillating circuit as described in the co-pending International Patent Application PCT/EP2013/072548, here illustrated by inductance L1 and C1, in combination with coupled inductors M1 locking the control signals acting on the semiconductor switches Q1, Q2 to opposite phase. Advantageously, the coupled inductors M1 are a PCB embedded solenoid structure 600 with a first winding 601 and a second winding 602 inductively coupled to the first winding 601, wherein the coupling designated by the Z-shaped thick line may be a coreless coupling.

Figs.7-11 show further embodiments of resonant DC-DC converters comprising an embedded solenoid transformer coupling an input side of the converter to an output side. In all embodiments, the embedded transformers are made up of embedded PCB solenoid inductors that are coupled to form an embedded solenoid transformer as described above. In figs. 7–11 coupling is indicated by a double line, wherein the coupling may be a coreless coupling.

Fig.7 shows a generic schematic of a resonant DC-DC converter 70 with an input side (inverter) 71 coupled to an output side (rectifier) 72 through an embedded iso-

lating transformer 700, wherein the embedded printed circuit board solenoid inductors 701, 702 are coupled to be used as the transformer 700 between the input side inverter 71 and the output side rectifier 72.

Fig.8 shows a generic schematic of a resonant DC-DC converter 80 with an input side inverter 81 coupled to an output side rectifier 82 through an embedded autotransformer 800. The autotransformer 800 is formed by coupled embedded printed circuit board solenoid inductors 801, 802. In applications where a high step ratio is required, but isolation is not, this configuration gives several advantages. The autotransformer 800 can be used to transform the impedance of the output side rectifier 82 to the desired output impedance for the input side inverter 81. This is particularly desirable in resonant converters as they are very dependent on the input and output impedances.

Fig.9 shows schematically an embodiment of a resonant DC-DC converter 90 with an input side inverter 91 coupled to an output side rectifier 92 through an embedded autotransformer 900. The resonant DC-DC converter 90 of Fig.9 differs from the resonant DC-DC converter 80 of Fig.8 in that the input side inverter 91 comprises a plurality of smaller inverters Inv1, Inv2. In the particular embodiment shown, the input side inverter 91 has two smaller inverters Inv1, Inv2 coupled with serial input and parallel output, a configuration also referred to as “SIPO”. The input side inverter 91 can also comprise an even higher number of smaller inverters. Furthermore, the plurality of smaller inverters may also be arranged with other combinations of parallel and serial input and output. The output side rectifier 92 may comprise multiple smaller rectifiers in the same way (not shown). Galvanic isolation in the sub-block (i.e. the smaller inverters and/or the smaller rectifiers) is a requirement if serial input or output is to be used. Generally, serial connection is desirable for high voltages and parallel connection is desirable for high currents.

Fig.10 shows schematically an embodiment of a resonant DC-DC converter 100 with an input side inverter 101 and an output side rectifier 102 coupled together through an embedded isolating transformer 1000. The isolating transformer is formed by coupled embedded printed circuit board solenoid inductors 1001, 1002. In this particular embodiment of the resonant DC-DC converter 100, the input side in-

verter 101 comprises a class DE inverter and the output side comprises a class E rectifier 102. This topology is especially suitable for applications with high input voltage and low output voltages. This is due to the half bridge configuration on the input side 101, which limits the peak voltage across the two switches S1, S2 to the input voltage, and the single diode rectifier on the output side 102, which minimizes the loss in the rectifier due to forward conduction loss in the diode. For example, this may be useful for a USB charging device, which needs to convert an input with a voltage of 110V/230V from a rectified mains input to an output of 5V, and which has to be galvanic isolated to properly protect a user of the charging device.

Fig.11 shows schematically an embodiment of a resonant DC-DC converter 110 with an input side inverter 111 and an output side rectifier 112. As in the embodiment of Fig.10, the input side inverter 111 comprises a class DE inverter and the output side rectifier comprises a class E rectifier. The embodiment 110 of Fig.11 differs from the embodiment 100 of Fig.10 in that the input side inverter 111 and the output side rectifier 112 are coupled together through an embedded autotransformer 1100. The autotransformer 1100 is formed by coupled embedded printed circuit board solenoid inductors 1101, 1102 as also shown in Fig.8 and Fig.9.

In applications where galvanic isolation is not a requirement it is generally more desirable to use the coupled inductors in an autotransformer configuration. Furthermore, for applications with low input voltages, inverters with just a low side switch, like switch Q1 in the input side inverter 51 shown in Fig.5, are typically more desirable, for example in battery driven applications like automotive, portable devices, etc. Furthermore, for applications with high output voltage, an output side rectifier comprising a half bridge rectifier is preferable.

EXAMPLES

A transformer can be described by an inductance matrix.

$$\begin{bmatrix} v_p(t) \\ v_s(t) \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_p(t) \\ i_s(t) \end{bmatrix},$$

wherein v(t) and i(t) refer to time-dependent voltage and current, respectively, and indices p and s refer to primary-side and secondary-side, respectively.

An interpretation of the inductance matrix yields transformer parameters for characterizing a given transformer. The diagonal elements *L*11 and *L*22 of the inductance matrix are the self-inductances for each winding, and the off-diagonal elements *L*12 and *L*21 are the mutual inductances as determined by the mutual flux. Since the transformer is a passive device *L*12 and *L*21 are equal. The coupling factor k is given by

$$k = \frac{L_{12}}{\sqrt{L_{11} L_{22}}} \quad .$$

In the following, examples are given for different types of layouts of PCB embedded transformers as described above with reference to Figs.1 – 4, wherein the number of turns of the transformers of the below examples may vary with respect to the transformers shown in the figures. The actual numbers of turns and corresponding geometry data of the measured transformers are given in each of the examples below. The geometry data comprise values for the width w of the transformer and/or first and second solenoids. These widths w are given as the distance between the respective vertical centers of the vias in a horizontal direction transverse to the longitudinal direction. The geometry data further comprise the overall lengths l of the transformers and/or the first and second solenoids in the longitudinal direction. The respective heights h of the transformers and/or first and second solenoids are determined by the PCB layer stack used for producing the respective embedded solenoid transformer. Depending on the transformer layout, the structures have been implemented in dual-layer PCB or in a four-layer PCB as also indicated in the examples below. The dual-layer PCB stack comprises an isolating core layer with a thickness of about 1600µm carrying an upper conductive layer made of copper with a thickness of 35µm on one side, and a corresponding lower conductive layer made of copper with a thickness of 35µm on the opposite side. The four-layer PCB stack has a total thickness of about 1600µm and comprises an isolating inner layer with a

thickness of 710µm carrying inner upper and lower copper layers on either side. The inner copper layers have a thickness of 35µm each. Each of the inner copper layers is covered by a respective outer isolating layer of 7628 prepreg with a thickness of 360µm each. Finally, each of the outer isolating layers carries an outer conductive layer made of copper foil with a thickness of 18µm.

The examples are transformers designed for operation in the VHF frequency range, and the different transformers are characterized by measured values for the above-mentioned transformer parameters L11, L22, L12, L21, k. Measurements of the transformer parameters L11, L22, L12, L21, k have been obtained using a network analyzer, wherein all measurements have been made in the frequency range 1MHz – 1.8GHz. Based on the measurement results a frequency range of operation is specified, for which the obtained transformer values are considered valid. Since the transformer is a passive device, L12 equals L21. Therefore only values for L12 are given below.

Example 1

Example 1 refers to an end-to-end layout embedded in a dual layer PCB as illustrated above with respect to Figs.1a-c and in the following implementation:

	1st solenoid	**2nd solenoid**	**transformer**
Number of turns	5	5	
Width w / mm	10	10	10
Length l / mm	10	10	20
Height h / mm	1,6	1,6	1,6
Trace width t / mm	1,8	1,8	1,8

The following transformer parameters have been measured for this implementation:

L11 / nH	**L12 / nH**	**L22 / nH**	**K**
41,00	3,22	39,45	0,08

The values of the transformer parameters are valid for operation in the frequency range from 100MHz – 850MHz.

Example 2

Example 2 refers to section-wise interleaved layout embedded in a dual layer PCB as illustrated above with respect to Figs.2a-c and in the following implementation with one first solenoid and one second solenoid arranged on a common longitudinal axis. Both solenoids have five turns distributed over two sections, with two and three turns, respectively. When seen along the longitudinal direction, starting from one end of the transformer, two turns of the first solenoid are followed by three turns of the second solenoid, which is followed by three turns of the first solenoid, which is again followed by two turns of the second solenoid.

	1st solenoid	**2nd solenoid**	**transformer**
Number of turns	5	5	
Number of sections	2	2	
Number of turns per section	2/3	2/3	
Width w / mm	10	10	10
Length l / mm			20
Height h / mm	1,6	1,6	1,6
Trace width t / mm	1,8	1,8	1,8

The following transformer parameters have been measured for this implementation:

L11 / nH	**L12 / nH**	**L22 / nH**	**k**
40,95	10,52	38,81	0,26

The values of the transformer parameters are valid for operation in the frequency range from 1MHz – 900MHz.

Example 3

Example 3 refers to an interleaved layout, wherein single turns of a first solenoid alternate with single turns of a second solenoid. The layout is embedded in a dual

layer PCB as illustrated above with respect to Figs.3a-c and in the following implementation:

	1st solenoid	2nd solenoid	transformer
Number of turns	10	10	
Width w / mm	10	10	10
Length l / mm			16,4
Height h / mm	1,6	1,6	1,6
Trace width t / mm	0,6	0,6	0,6

The following transformer parameters have been measured for this implementation:

L11 / nH	L12 / nH	L22 / nH	k
159,07	94,03	162,89	0,59

The values of the transformer parameters are valid for operation in the frequency range from 1MHz – 650MHz.

Example 4

Example 4 refers to a layout, wherein a first solenoid is enclosed inside a second solenoid. The layout is embedded in a four-layer PCB as illustrated above with respect to Figs.4a-c and in the following implementation:

	1st solenoid	2nd solenoid	transformer
Number of turns	19	19	
Width w / mm	23,4	25	25
Length l / mm	11	11	11
Height h / mm	0,71	1,6	1,6
Trace width t / mm	0,4	0,4	0,4

The following transformer parameters have been measured for this implementation:

L11 / nH	L12 / nH	L22 / nH	k
1154,33	1104,82	1506,57	0,84

The values of the transformer parameters are valid for operation in the frequency range from 1MHz – 25MHz.

CLAIMS

1. Resonant power converter for operation in the radio frequency range, preferably in the VHF, the power converter comprising at least one transformer, wherein the at least one transformer comprises
   - a printed circuit board defining a horizontal plane, the printed circuit board comprising at least two horizontal conductive layers separated by an isolating layer,
   - a first embedded solenoid forming a primary winding of the transformer and
   - a second embedded solenoid being arranged parallel to the first solenoid and forming a secondary winding of the transformer,

   wherein the first and second embedded solenoids are formed in the conductive layers of the printed circuit board, wherein each full turn of an embedded solenoid has a horizontal top portion formed in an upper conductive layer, a horizontal bottom portion formed in a lower conductive layer, and two vertical side portions formed by vias extending between the upper and the lower conducting layers.

2. Power converter according to claim 1, wherein the transformer is a coreless transformer.

3. Power converter according to any of the preceding claims, wherein the first and second solenoids are embedded on the same PCB.

4. Power converter according to any of the preceding claims, wherein the first and second solenoids are wound around a common axis.

5. Power converter according to claim 4, wherein the first and second solenoids at least partially overlap in a longitudinal direction.

6. Power converter according to any of the preceding claims, wherein top portions of the first and second solenoids are formed in a common upper conductive layer, and/or bottom portions of the first and second solenoids are formed in a common lower conductive layer.

7. Power converter according to claim 6, wherein the first and second solenoids are section-wise interleaved.

8. Power converter according to claim 7, wherein first sections of the first solenoid alternate with second sections of the second solenoid.

9. Power converter according to claim 6 or claim 7, wherein first sections are single turns and/or second sections are single turns.

10. Power converter according to any of the preceding claims, wherein the PCB has at least four-layers.

11. Power converter according to claim10, wherein when seen in a cross-sectional plane perpendicular to a longitudinal axis of the solenoids, the second solenoid is arranged inside the first solenoid or, alternatively the first solenoid is arranged inside the second solenoid.

12. Power converter according to any of the preceding claims, wherein the transformer comprises further solenoids coupled to the first solenoid and/or the second solenoid.

13. Power converter according to any of the preceding claims, wherein the transformer is adapted for operation at a radio frequency in the range 1MHz – 1 GHz, alternatively 10 MHz – 500 MHz, further alternatively 30 MHz – 300 MHz.

14. Power converter according to any of the preceding claims, wherein the transformer has a coupling factor k of above 0,1, preferably above 0,3, preferably above 0,4, preferably above 0,5, more preferably above 0,6, and most preferably above 0,8.

15. Power converter according to any of the preceding claims, wherein at least one transformer is arranged as an isolating transformer between an input side and an output side.

16. Power converter according to any of the preceding claims, wherein at least one transformer is arranged as an autotransformer between an input side and an output side.

17. Power converter according to any of the preceding claims, wherein at least one transformer is arranged such that the the first solenoid is used as a power carrying inductor in the power converter and the second solenoid is used as a sensing inductor to measure the current through the first inductor.

18. Power converter according to any of the preceding claims, wherein the power converter is a resonant DC-DC converter.

19. Power converter according to any of the preceding claims, wherein a switching frequency on the input side is at least 10 MHz, preferably at least 20 MHz, more preferably at least 30 MHz.

20. Power converter according to any of the preceding claims, wherein the power converter is an inverter.

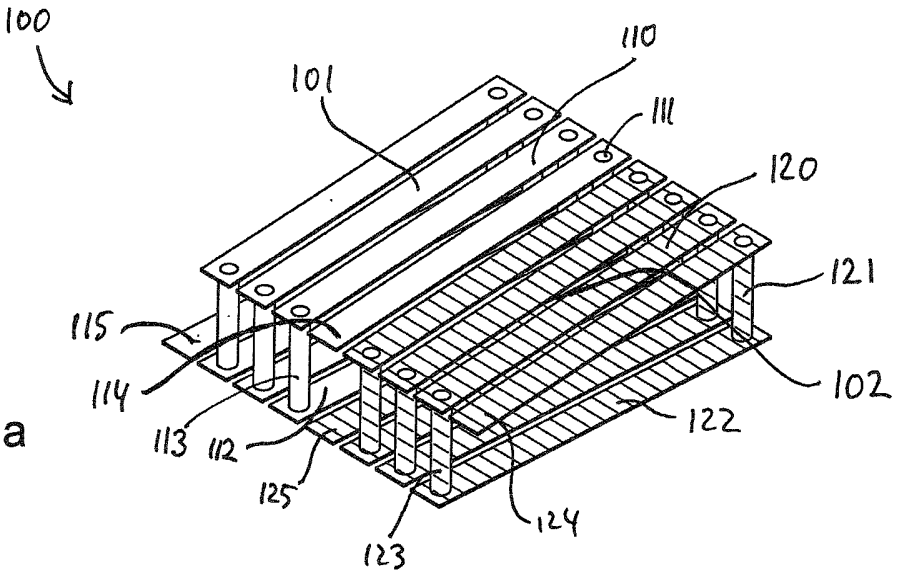
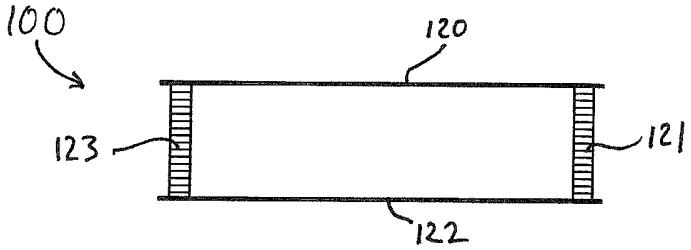


Fig.1a



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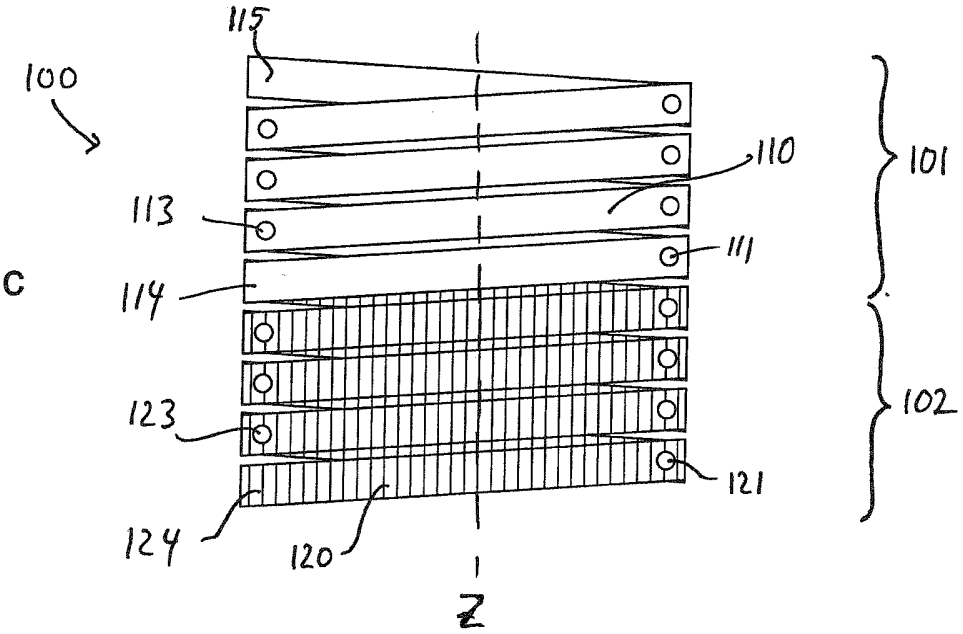


Fig.1c

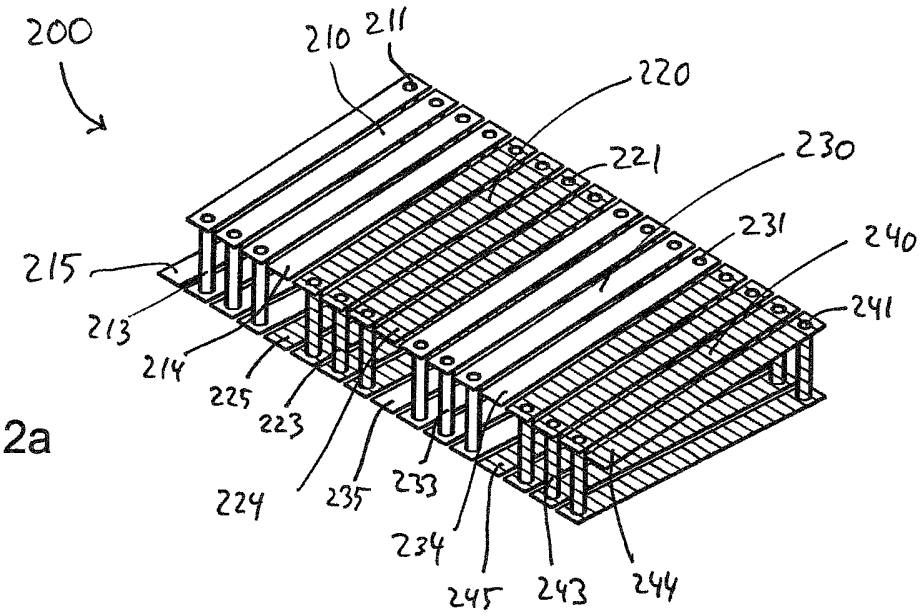
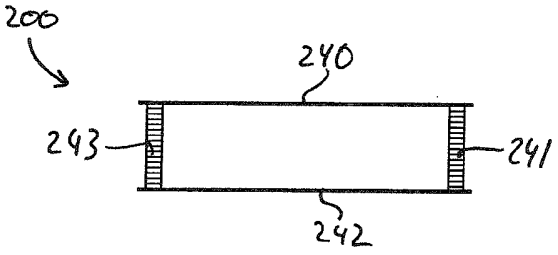


Fig.2a



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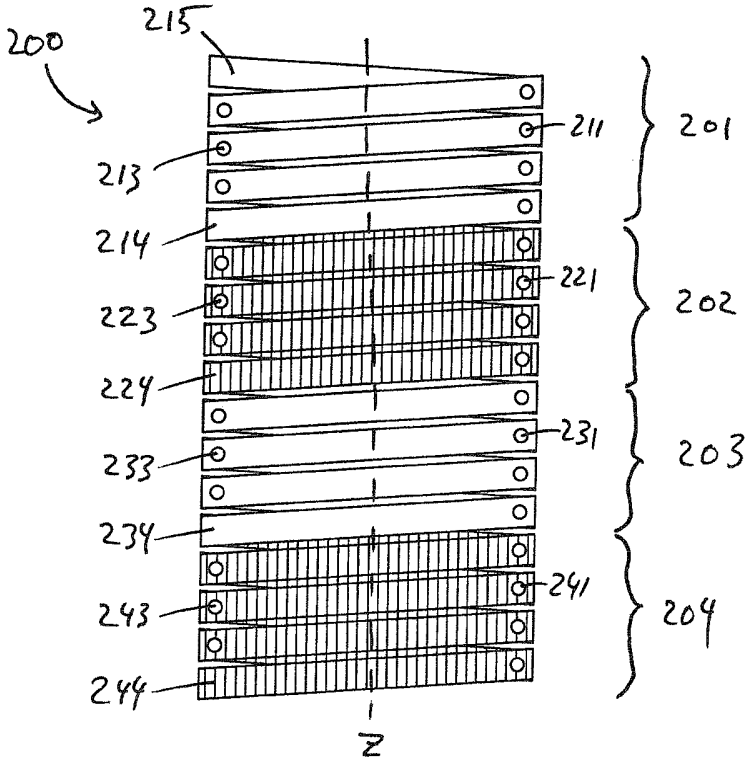
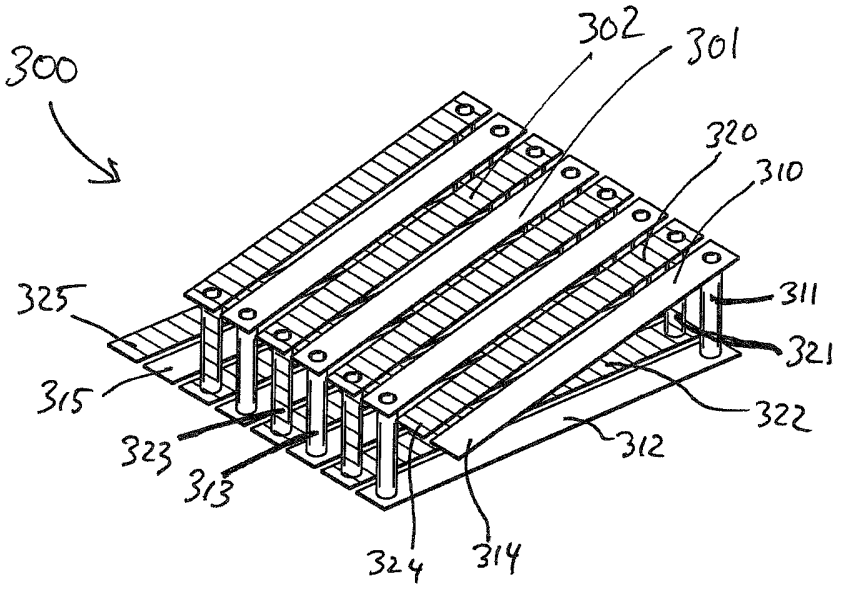


Fig.2c



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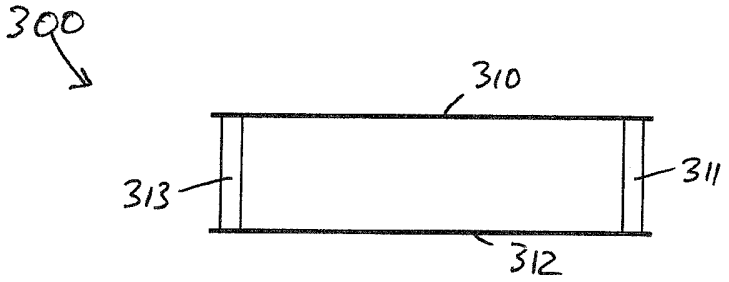


Fig.3b

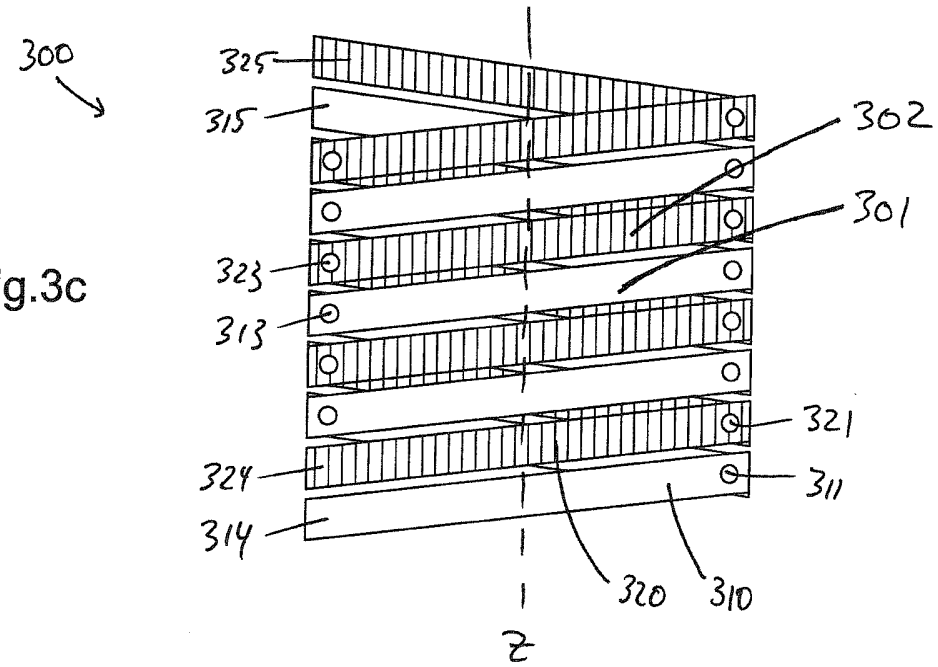


Fig.3c

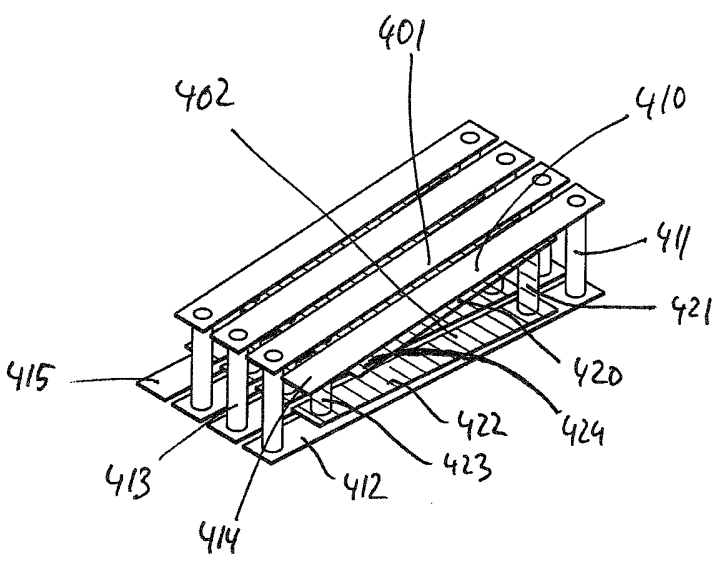


Fig.4a

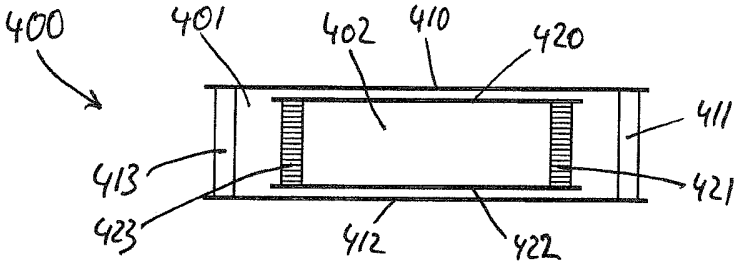
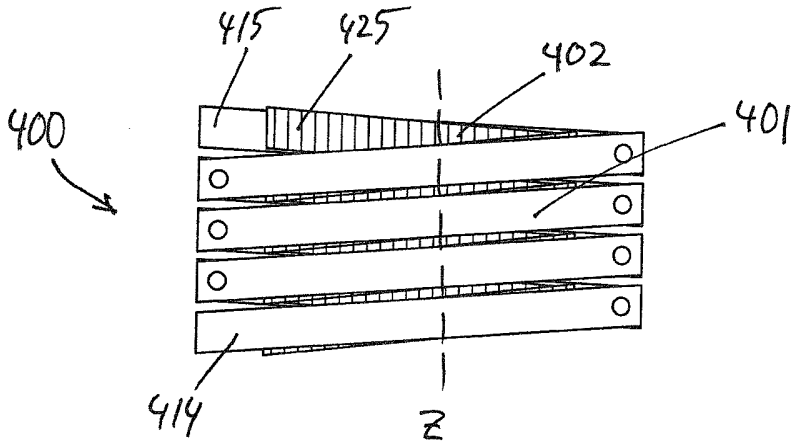


Fig.4b



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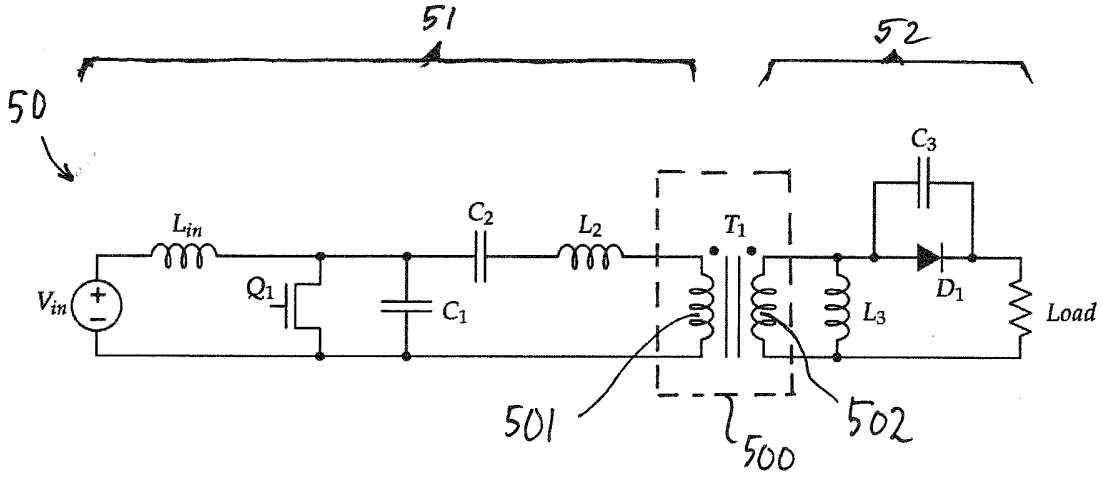
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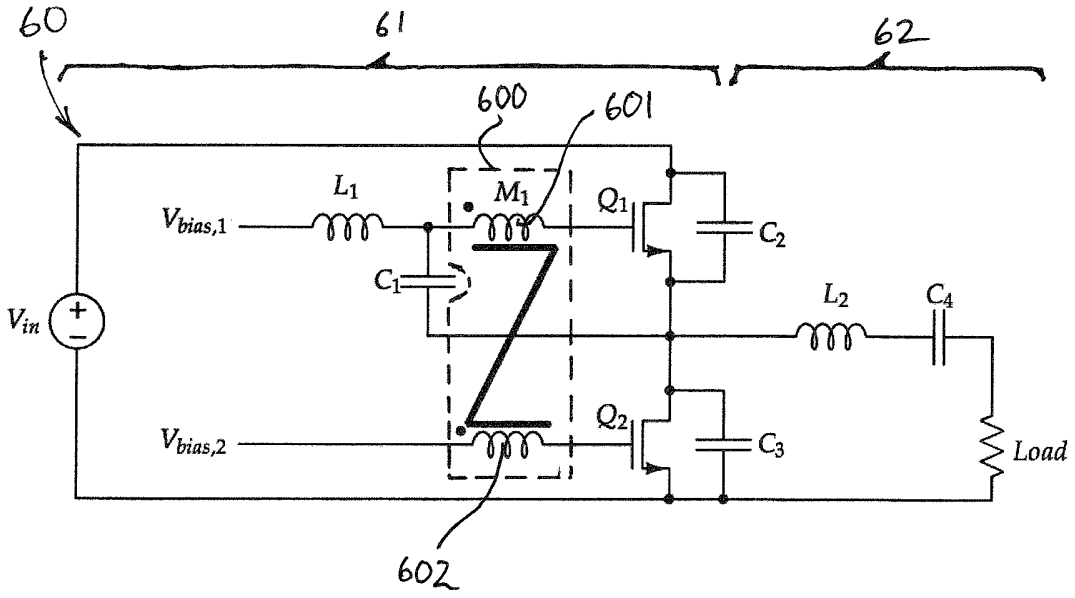
52
50
C_3
L_{in}
C_2
L_2
T_1
V_{in}
Q_1
C_1
L_3
D_1
Load
501
500
502

Fig.5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601
L_1
M_1
Q_1
C_2
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C_1
L_2
C_4
V_{in}
Q_2
C_3
$V_{bias,2}$
Load
602

Fig.6

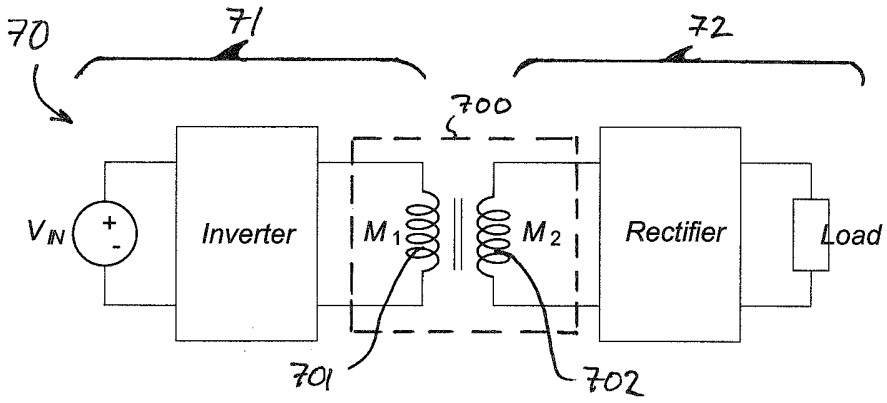


Fig.7

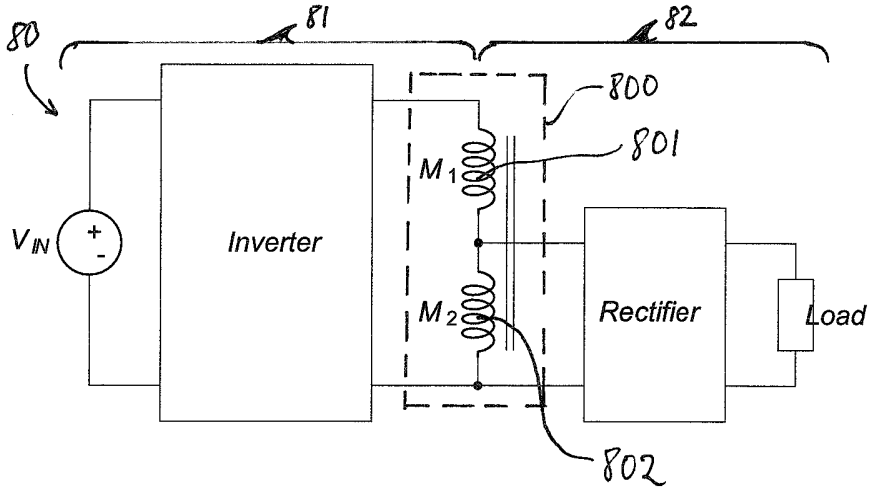


Fig.8

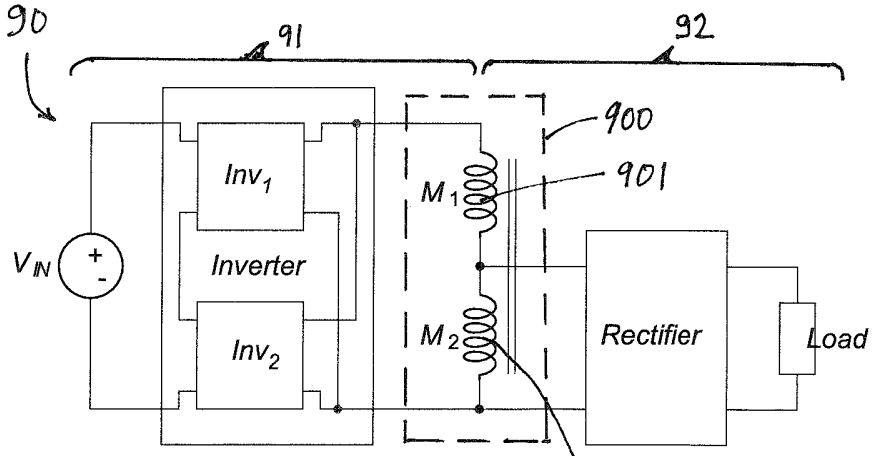
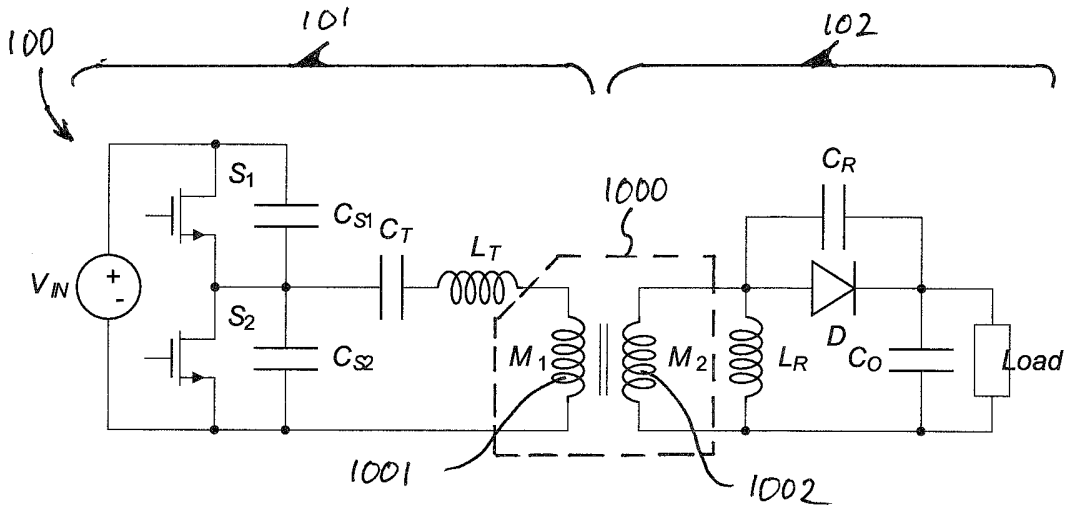


Fig.9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C_T
L_T
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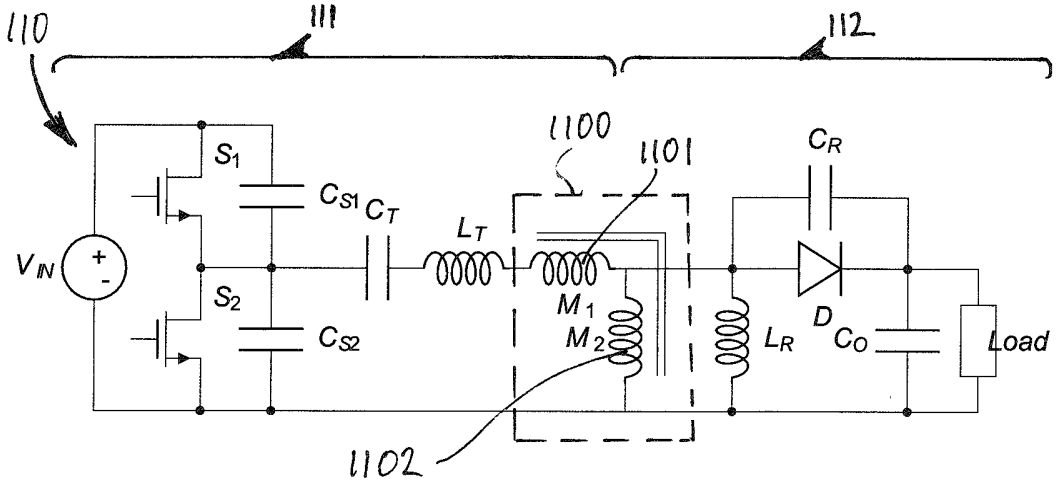
C_R
V_{IN}
S_2
C_{S2}
M_1
M_2
L_R
D
C_O
Load
1001
1002

Fig.10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C_T
L_T
C_R
V_{IN}
S_2
C_{S2}
M_1
M_2
L_R
D
C_O
Load
1102

Fig.11

A.19 M. Madsen, D. J. Perreault, A. Knott and M. A.E. Andersen: *"Self-oscillating Galvanic Isolated Bidirectional Very High Frequency DC-DC Converter"*, Accepted for presentation at IEEE COMPEL 2015 with subsequent publishing in the conference procedings.

Outphasing Control of Gallium Nitride based Very High Frequency Resonant Converters

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***Abstract* — In this paper an outphasing modulation control method suitable for line regulation of very high frequency resonant converters is described.**

The pros and cons of several control methods suitable for very high frequency resonant converters are described and compared to outphasing modulation. Then the modulation technique is described and the design equations given.

Finally a design example is given for a converter consisting of two class E inverters with a lossless combiner and a common half bridge rectifier. It is shown how outphasing modulation can be used for line regulation while insuring equal and purely resistive loading of the inverters. Combined with a proper design of the inverters that, insures they can achieve zero voltage switching across a wide load range, and gallium nitride FETs for the switching devices, this makes it possible to achieve more than 90% efficiency across most of the input voltage range with good line regulation.

***Keywords* — Gallium nitride, Phase control, Power control, VHF circuits, Zero voltage switching.**

I. Introduction

The development of Switch-Mode Power Supplies (SMPS) has made it possible to increase the power density of power converters significantly. Modern power supplies are however limited by the passive energy storing elements, which is needed to store energy between each switching period. The size of these components scale inversely with the switching frequency, and there have therefore been a constant strive for higher switching frequencies ever since. Commercially available converters today switch at frequencies up to several megahertz and can have efficiencies of more than 95% (e.g. [1]).

The reason not to increase the switching frequency further, and thereby reaching even higher power densities, is the switching losses. For more than two decades (since 1988 [2]) research has been done, in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc/dc converters, in order to avoid switching losses. With this type of converters, SMPSs with switching frequencies in the Very High Frequency range (VHF, 30-300MHz) have been designed with efficiencies up to approx. 90% [3], [4].

Several of the benefits and challenges of the increased switching frequency are described in [5], [6]. Among the benefits are higher power densities, lower weight and removed need for electrolytic capacitors and magnetic core materials [7]. The increased frequency also enables the possibility of very fast transient responses, to achieve this a fast and efficient control scheme is needed. This together with the fact that resonant converters are very load dependent remains two of the major challenges for very high frequency resonant converters.

In section II of this paper different control schemes for resonant converters are investigated and compared. Section III describes a method for efficient outphasing control of resonant converters. Section IV covers the design and simulation of a converter with the described control and finally section V concludes the paper.

II. Control of Resonant Converters

Resonant converters are dependent on precise timing between the resonances in the power stage and the switching of the power semiconductors. The resonances in the power stage are used to shape the voltages and currents, so that the voltage across or the current through the power semiconductors are zero at the switching instant, known as zero-voltage-switching (ZVS) and zero-current-switching (ZCS).

In power applications the energy stored in the parasitic capacitance of the switching device is generally the dominating contributor to switching losses, hence ZVS is crucial to insure high efficiency when the switching frequency is pushed into the VHF range.

Pulse width modulation (PWM) is the most commonly used control scheme for power converters, but if a resonant converter is controlled in this way, ZVS is lost as soon as the duty cycle moves away from one optimal value.

Pulse frequency modulation (PFM) is another option, but it requires a very wide frequency operation range to insure even a limited controllability of the converter. Combinations of PWM and PFM have shown good results [8], but the control circuit becomes quite complex and still requires a wide frequency operation range.

A. Burst mode control

So far the most commonly used control method for VHF converters has been burst mode control (also called cell modulation, on-off or bang-bang control) [4], [9]-[12]. Here the entire converter is switched on and off in order to control the output. The benefit of controlling the converter in this way is that the converter will either be on and working in its optimal operating point or off with only small standby losses. The result is a wide control range with an almost flat efficiency curve [4], [10]. Further the converter can be optimized for high

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peak efficiency in this specific operation point instead of compromising the peak efficiency for higher average efficiency.

One down side of burst mode control is that low frequency harmonics is introduced, which increase the size of the needed input and output filters. Another is added circuitry that adds both to complexity and to the losses, which reduces the efficiency at full load. Further burst mode requires the converter to be able to start and reach steady state quickly, most implementations use a burst frequency approximately two decades below the switching frequency in order to insure that the converter has time to reach steady state and operate efficiently for some time before it is shut down again [4], [9]-[12].

Several control schemes for burst mode control are available with hysteresis [4], [9]-[10] and PWM [11] being the most commonly used, phase shift [12] and constant on time are two other alternatives.

Hysteresis control has the best transient response, as the transitions between the on and off states are defined by the hysteresis window, instead of a fixed frequency or times as in the other schemes. Another advantages is very good efficiency at light loads due to a very low burst frequency. These advantages come at the expense of widely varying burst frequencies increases the complexity and potentially size of the needed input/EMI filter.

The design of the input filter is more straightforward with PWM where a fixed burst frequency is used, but the transient response and light load efficiency degrades. The performance of a VHF converter controlled by PWM burst mode, is in many aspects similar to a conventional hard switched converter operating at the burst frequency.

Phase shift control has the same pros and cons as hysteresis control, but the delay in the control circuitry is utilized in the design which makes it possible to use slower components than would have been needed with hysteresis control.

Constant on time control can be compared to PWM control, but with the on time fixed instead of the frequency. This gives a more stable frequency than seen for hysteresis and phase shift control, but still with good light load efficiency.

B. Outphasing

Outphasing, also referred to as Linear Amplification with Nonlinear Components (LINC), was introduced for RF amplifiers in the 1930's [13]. This control method has however only been used a few times in previous publication [14]-[15] and posses several advantages compared to burst mode.

Outphasing control utilizes a phase shift between two or more inverters to control the combined output through a common rectifier, as illustrated with two inverters in Fig. 1. In this way the individual inverters run continuously at a fixed frequency while the total output to the load is regulated.

With this control method all the benefits of the high switching frequency can be achieved, both fast transient response, wide control range and small input and output filters.

The main drawback of outphasing is that the losses in the inverters are almost constant at light and full load, which decrease the light load efficiency significantly. Further the varying load and the inverters impact on each other is a challenge, this will be investigated further in section III.

III. Proposed Outphasing System

Selecting the right combiner is crucial to achieve a good result with outphasing. Several approaches have been suggested [16]-[19], but the lossless combiner proposed in [20] (shown in Fig. 2) posses several benefits for use in resonant converters. The combiner only consists of an inductor and capacitor, if these are assumed ideal the combiner is lossless. Further the admittance seen by the two inverters can be made zero, insuring purely resistive loading of the inverters. As resonant converters are very load dependent and quickly looses ZVS when load reactively this is crucial in order to insure high efficiency.

The input impedance of the rectifier, R_{REC}, can be assumed purely resistive at the switching frequency. Further the output voltage of the two inverters, V_{INV1} and V_{INV2}, can be assumed equal to:

$$V_{INV1} = V_{IN} \cdot G_{INV} \cdot e^{-I \cdot \varphi} \quad (1)$$

$$V_{INV2} = V_{IN} \cdot G_{INV} \cdot e^{I \cdot \varphi} \quad (2)$$

Where V_{IN} is the input voltage, G_{INV} is a fixed gain between the input voltage to the converters and the peak output voltage.

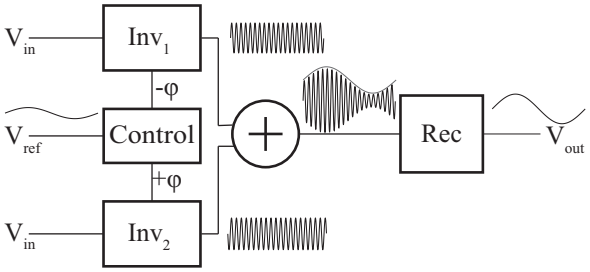

Fig. 1. System view of a converter using outphasing modulation.

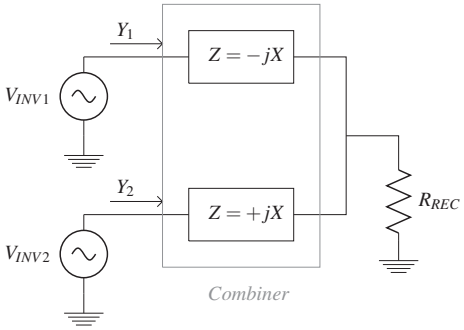

Fig. 2. Schematic of the lossless combiner for outphasing modulation.

The admittance seen by the two inverters is now written as:

$$Y_1 = \frac{1}{X} - \frac{I \cdot e^{I\cdot\varphi} \cdot V_{OUT}}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \quad (3)$$

$$Y_2 = \frac{1}{X} - \frac{I \cdot V_{OUT}}{X \cdot e^{I\cdot\varphi} \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \quad (4)$$

Where G_{REC} is a fixed voltage gain from the peak input voltage of the rectifier to the output voltage, V_{OUT}. The imaginary part of the admittance is:

$$\Im(Y_1) = \frac{1}{X} - \frac{V_{OUT} \cdot \cos(\varphi)}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \quad (5)$$

$$\Im(Y_2) = -\frac{1}{X} + \frac{V_{OUT} \cdot \cos(\varphi)}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \quad (6)$$

Setting this to zero and solving for the phase, φ, gives:

$$\varphi = \arccos\left(\frac{V_{IN} \cdot G_{INV} \cdot G_{REC}}{V_{OUT}}\right) \quad (7)$$

If the phase is controlled according to this equation, the loading of the inverters will be purely resistive. The real part of the admittance is:

$$\Re(Y_1) = \Re(Y_2) = \frac{V_{OUT} \cdot \sin(\varphi)}{X \cdot V_{IN} \cdot G_{INV} \cdot G_{REC}} \quad (8)$$

From this the output power, P_{OUT}, can be calculated for a given value of the combiner reactance, X, and input and output voltage by:

$$P_{OUT} = \frac{G_{INV} \cdot V_{IN} \sqrt{V_{OUT}{}^2 - V_{IN}{}^2 \cdot G_{INV}{}^2 \cdot G_{REC}{}^2}}{X \cdot G_{REC}} \quad (9)$$

From (8) it is seen that it is not possible to control the power, if the loading of the converters needs to be purely resistive. If the output voltage is kept fixed, the output power will however be a quadratic function of the input voltage that can be offset by the chosen reactance for the combiner.

IV. Design and Simulation

The outphasing modulation will be evaluated for use as line control of a resonant converter with the specifications given in table 1. The aim is to use outphasing to achieve max +/- 20% output power variation for a input variation of +/- 33%.

TABLE I. SPECIFICATIONS FOR THE CONVERTER.

Input voltage	Output voltage	Frequency	Output power
12-24 V	54 V	30 MHz	10-15 W

Equation (7) shows that it is only possible to adjust the phase to give a purely resistive loading of the inverters, if the input voltage multiplied by the combined gain of the inverter and rectifier is less than or equal to the output voltage. This is because outphasing modulation can only be used to reduce the output power, from the power that would be delivered if the two inverters where operating in phase.

Due to the high switching frequency class E inverters with only low side switches are chosen. Other suitable topologies, such as the class Φ_2 [4] or class DE [21], could have been chosen, but the class E inverter is chosen due to the low input voltage and its simplicity.

A half bridge rectifier with a gain of exactly $4/\pi$ is selected due to the high output voltage. The gain of a class E inverter is $\pi/2$. With these gains the phase, output power, load resistance and reactance can be calculated, results shown in Fig 3-6.

The value of the combiner reactances is set to 56 Ω, corresponding to a 300 nH inductor and 94 pF capacitor, in order to achieve a output power which is 14 W in average. The 14 W is based on the assumption that the total system efficiency will be around 90% and that 1.4 W hence will be lost in the converter. Fig. 5-6 clearly shows the purely resistive loading of the converter with a value between 28 and 110 Ω across the input voltage range. The complete circuit is shown in Fig. 7.

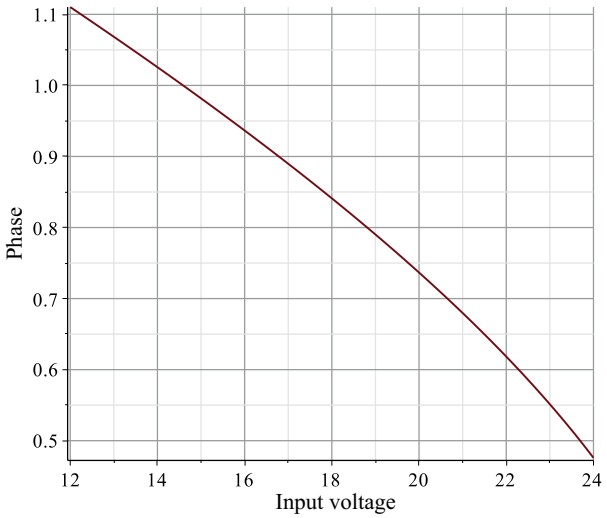

Fig. 3. The phase shift needed across the input voltage range for purely resistive loading of the inverters (in radians).

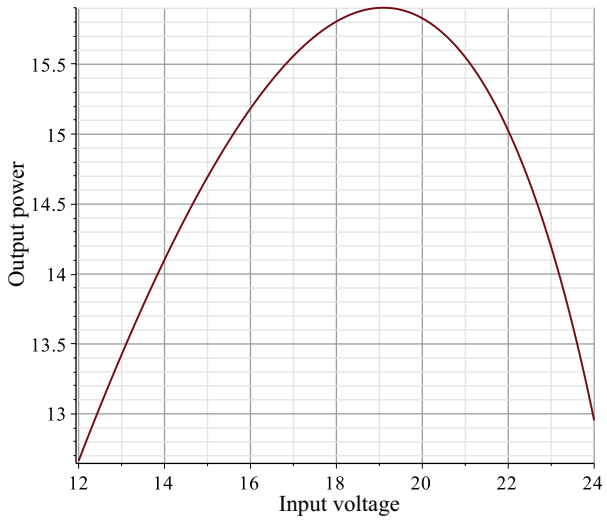

Fig. 4. The achieved output power across the input voltage range. The reactance of the combiner is set to 56 Ω to achieve the desired output power plus 10% that is expected to be losses.

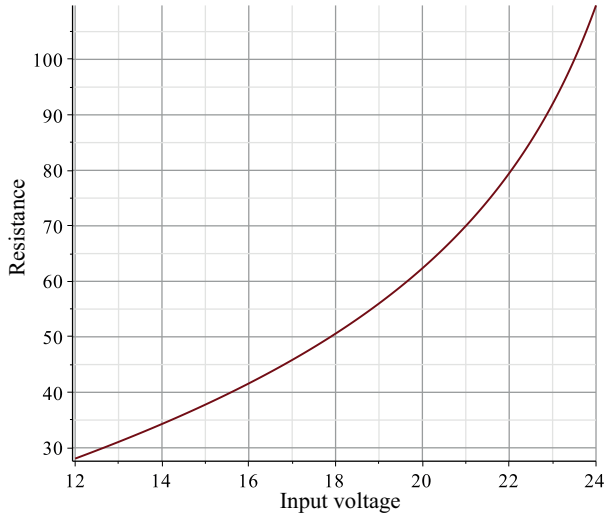

Fig. 5. The load resistance seen by the inverters across the input voltage range.

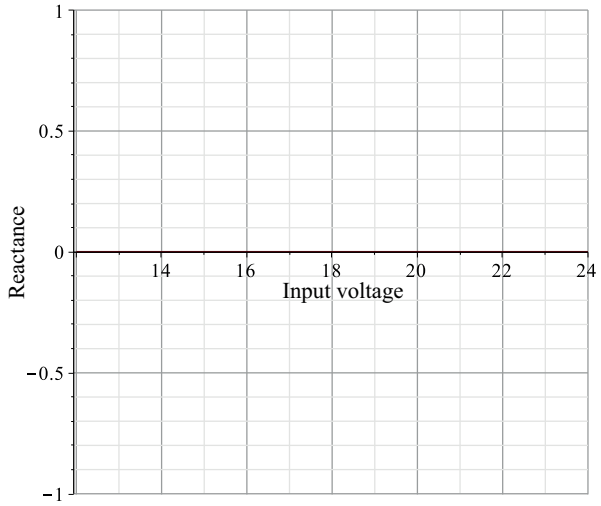

Fig. 6. The load reactance seen by the inverters across the input voltage range, it is zero across the range as it should be.

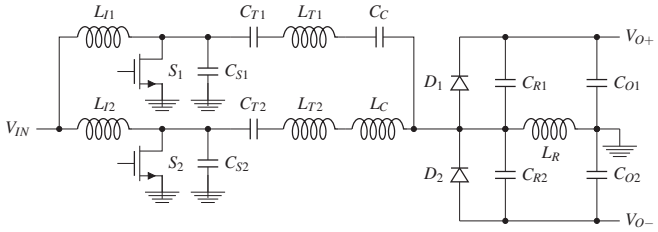

Fig. 7. Schematic of the two inverters, the combiner and the half bridge rectifier.

The two inverters are designed to be identical and based on the methodology described in [22], but without the parallel resonant tank. The values of the input inductors, L_{I1} and L_{I2}, and the switch capacitances, C_{S1} and C_{S2}, are given by the equations:

$$L_{I1} = L_{I2} = \frac{Q_S \cdot R_{\min}}{k \cdot 2 \cdot \pi \cdot f_s} \tag{10}$$

$$C_{S1} = C_{S2} = \frac{1}{Q_S \cdot R_{\min} \cdot k \cdot 2 \cdot \pi \cdot f_s} \tag{11}$$

Where R_{min} = 28 Ω, f_s = 30 MHz and Q_S and k are set to 0.7 and √2, respectively. This gives inductor values of 832 nH and capacitances of 192 pF. EPCs 8010 GaN FETs are selected for the switches and their parasitic output capacitance combined with additional 140 pF composes C_{S1} and C_{S2}. The values of the resonant tanks components, C_{T1}, C_{T2}, L_{T1} and L_{T2}, are also calculated based on (10) and (11), but here Q_S is set to 3.4 in order to insure that the currents running into the combiner is close to sine waves. MBR0560 schottky diodes are selected for the rectifier and their parasitic capacitance of 15 pF composes C_{R1} and C_{R2}. The inductor in the rectifier, L_R, is used to tune the rectifier to appear resistive at the switching frequency. Through a spice simulation the required value is found to be 350 nH. 2 µF capacitors are selected for C_{O1} and C_{O2}. A complete bill-of-material is shown in table II.

TABLE II. BILL OF MATERIAL FOR THE CONVERTER.

Component	Value
L_{I1} and L_{I2}	832 nH
C_{S1} and C_{S2}	140 pF
S_1 and S_2	EPC 8010
C_{T1} and C_{T2}	40 pF
L_{T1} and L_{T2}	355 nH
L_C	300 nH
C_C	94 pF
D_1 and D_2	MBR0560
C_{R1} and C_{R2}	(parasitic)
L_R	350 nH
C_{O1} and C_{O2}	2 µF

A spice simulation of the deigned converter has been made and the waveforms are shown in Fig. 8. From the waveforms it can be seen that the two inverters is indeed loaded equally and that ZVS is achieved across the entire input voltage range. Further more the efficiency is high and only drops below 90% for 24 V input. The reason for the reduced efficiency at this point is that the resonating currents in the inverters increase with the input voltage and hence the losses increase, at the same time the output power drops as expected from Fig. 4. The output power is kept well within the desired range with a minimum at 10 W and a peak of 14 W.

V. Conclusion

This paper have covered a short description of the most commonly used control methods for resonant converters operating in the very high frequency range, followed by the design and evaluation of a converter where outphasing of two inverters is used to achieve line regulation.

The designed converter achieves very good performance with equally and purely resistive loading of the two inverters across the entire input voltage range. This combined with a design of the inverters that insures that they can operate with ZVS across a wide load range, insures efficient operation of the converter across the entire input voltage range. The aim was to achieve efficient line regulation with less than +/- 20% output power variation for an input variation of +/- 30%. This is achieved as the converters keeps within +/- 16.5% output power variation. Furthermore the design exhibits very high efficiency across the entire input voltage range and only drops below 90% at the maximum input voltage.

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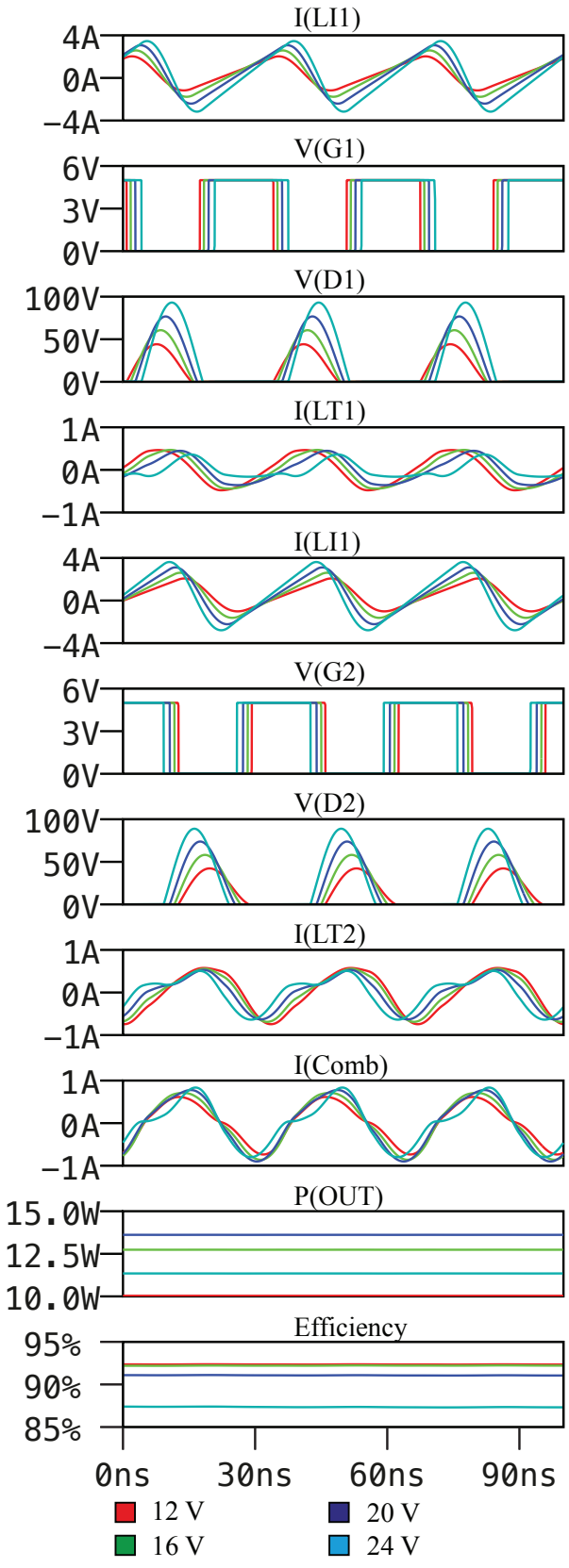

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(54) **Title**: BURST MODE CONTROL

(57) **Abstract**: The present invention relates to a new method of power converter regulation, in particular regulation of very high frequency (VHF) power converters operating at frequencies in the MHz range, wherein accurate output regulation utilises inherent delays in the regulation loop, whereby, contrary to hysteresis on/off control, the new method does not require immediate responses to comparisons of a sense voltage to two reference voltages; rather, according to the new method, only one reference voltage is used, and delays in the feedback loop are allowed to cause some variation of an output of the power converter.

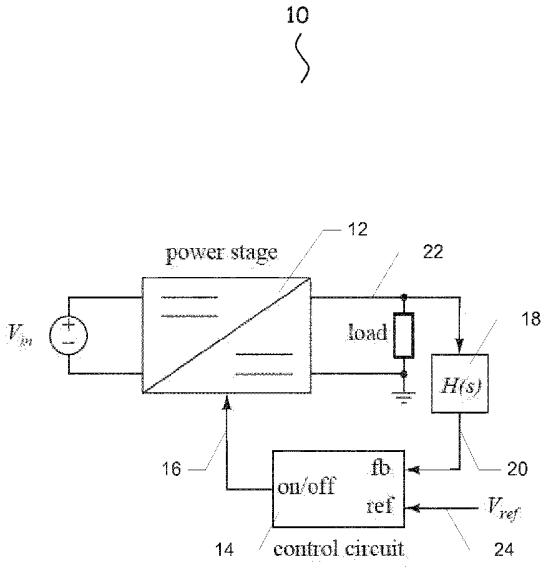

Fig. 1

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BURST MODE CONTROL

The present invention relates to a new method of power converter regulation, in particular regulation of very high frequency (VHF) power converters operating at frequencies in the MHz range.

BACKGROUND OF THE INVENTION

Reducing the physical size of electronic equipment in power applications is desired in order to add more features into existing products, integrate power converters in places normally unfit for such equipment, and reduce system cost. Increasing the operating frequency of the converter is a direct way of reducing the size of energy storage elements such as bulky capacitors and inductors, which usually dominate the overall converter volume. Due to reduction in energy storage requirements the transient response is dramatically increased. LED lighting applications and point-of-load (PoL) converters particularly benefit from very high frequency (VHF) converters due to size, price, and weight reduction, and faster transient response.

Conventionally, burst mode control is used to control the output voltage or current of resonant power converters. Burst mode control allows the converter designer to optimize resonant power converters for operation in one operating point. The output voltage or current is controlled by turning the resonant power converters on or off as necessary to maintain constant output voltage or current. A disadvantage of burst mode control is that the EMI performance is the same or worse compared to hard switched converters at the same modulation frequency. Typically, the modulation frequency ranges from 20 kHz to 1 Mhz.

Typically, prior art burst mode control is either hysteresis based, or pulse width modulation (PWM) based with constant switching frequency.

With hysteresis and PWM control, fast responses – ideally zero time delays - of the components of the regulation loop are required so that low cost components cannot be used.

The converter start-up circuit must also provide very little delay. As a consequence, passive start-up circuits (which have lower cost) are usually not an option.

Hysteresis based control results in tight output regulation, but requires a high cost, high performance comparator with very small propagation delays.

A conventional hysteretic burst mode control method of controlling a power converter, comprises the steps of

turning the power converter on when an absolute value of a sense voltage is less than or equal to an absolute value of a first reference voltage, and

turning the power converter off when the absolute value of the sense voltage is larger than or equal to an absolute value of a second reference voltage that is larger than the absolute value of the first reference voltage.

Typically, the difference between the first and second reference voltages is a predetermined fixed value.

SUMMARY OF THE INVENTION

The present invention provides a modulation method for obtaining accurate output regulation of a power converter while exploiting inherent delays in the feedback loop. Contrary to hysteresis on/off control, i.e. hysteretic burst mode control, the new method does not require immediate responses to comparisons of a sense voltage to two reference voltages. Rather, according to the new method, only one reference voltage is used, and delays in the feedback loop are allowed to cause some variation of an output of the power converter. The variation can be predicted and accounted for during the converter design process.

Thus, a new method of controlling a power converter is provided, comprising the steps of

turning the power converter on when an absolute value of a sense voltage is less than or equal to an absolute value of a reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

turning the power converter off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a second time period has elapsed since a previous turn-on of the power converter.

In the following, the new method is termed phase-shift burst mode control due to the phase shift caused by the first and second time periods. According to the new method, hysteresis is provided in the time domain.

A power converter operating in accordance with the new method is also provided.

Thus, a new power converter is provided, comprising a control circuit coupled to compare a sense voltage with a reference voltage, and having a control output that is coupled to control turn-on and turn-off of the power converter in such a way that

the power converter is turned-on when the absolute value of the sense voltage is less than or equal to the absolute value of the reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

the power converter is turned-off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a second time period has elapsed since a previous turn-on of the power converter.

The first time period may include a third time period of a predetermined duration that has to elapse from the point in time when the absolute value of the sense voltage drops below the absolute value of the reference voltage until the power converter is turned-on.

The second time period may include a fourth time period of a predetermined duration that has to elapse from the point in time when the absolute value of the sense voltage raises above the absolute value of the reference voltage until the power converter is turned-off.

The predetermined durations of the third and fourth time periods may be different.

Throughout the following disclosure, the process of alternatingly turning a power converter on and off, is termed "modulation" of the power converter, and the time between two consecutive turn-on events is termed a "modulation period", and the rate of turn-on is termed the "modulation frequency".

The sense voltage may correspond to an output voltage of the power converter; or an output current of the power converter; or another desired characteristic of the power converter.

An output current of the power converter is a current consumed by a load connected to an output of the power converter.

The control circuit may perform turn-off of the power converter by turning at least one switch of the power converter off, e.g. by short-circuiting the gate of a Field-Effect-Transistor (FET) to its source; or, the base of a bipolar transistor to its emitter, and turn-on of the power converter by allowing the at least one switch of the power converter to turn-on again, e.g. by opening the short-circuit.

The control circuit may also perform turn-on and turn-off of a resonant power converter by changing the impedance or the loop-gain of the resonant part of the power circuit, whereby the resonant power converter is turned-off by changing the impedance or loop-gain to a first value at which the resonant part of the power circuit does not oscillate, and whereby the resonant power converter is turned-on by changing the impedance or loop-gain to a second value at which the resonant part of the power circuit oscillates.

The control circuit may comprise one or more delays configured to provide at least part of one or more of the respective first and second time periods. Propagation delays in circuit components, such as propagation delays in a comparator, filtering elements, the power circuit, etc., may advantageously be incorporated into the appropriate time period.

The control circuit may comprise a comparator coupled to compare the sense voltage with the reference voltage, and an output of the comparator may constitute the control output that is coupled to control turn-on and turn-off of the power converter, and thus, the delays with which the comparator changes state of its output from high to low and vice versa, in response to changed input(s), constitute part of the respective first and second time periods.

The delays with which the comparator changes state of its output from high to low and vice versa, in response to changed input(s), may provide at least part of the third and fourth time periods.

The output voltage of the power converter may be coupled to signal conditioning circuit, such as a low-pass filter, etc., configured to output the sense voltage.

The power converter may be of any known type of power converters, and in particular any type of VHF power converters, such as square wave power converters, quasi-square wave power converters, resonant transition power converters, resonant power converters, etc.

The power converter may have a plurality of power circuits operating in series and/or in parallel and/or interleaved, e.g. with inputs in series and/or parallel and/or with outputs in series and/or parallel. All or some of the plurality of power circuits may be controlled with a single control circuit.

A resonant power converter may be of any known type of resonant power converters, such as converters comprising: a class E inverter and a class E rectifier, a class DE inverter and a class DE rectifier, a class DE inverter and a class E rectifier, etc.; or, class EF2 (or class Φ) converters, resonant Single-Ended Primary-Inductor Converters (SEPIC), etc.

The power converter may be driven by an oscillator, or the converter may be self-oscillating. Further, the power converter may be interleaved.

Basing control of the output of the power converter on a single reference voltage and time periods during which the power converter does not change state from a turned-on state to a turned-off state, or vice-versa, leads to lowered performance requirements for control circuit components as compared to components of conventional control circuits, e.g. utilizing PWM-control or hysteresis control. E.g., low cost components and passive start-up circuits may be used in the new control circuit.

Furthermore, it is possible to include low-pass filtering, or other signal conditioning, of the output voltage for provision of the sense voltage, thus improving signal integrity.

Increasing at least one of the first and second time periods provided by the control circuit lowers modulation frequency of the control output signal controlling the on/off states of the

power converter. This in turn increases variation of the output voltage; however, output voltage variations may be lowered by provision of a suitable output filter at the output of the power converter.

Due to the time periods provided by the control circuit, the response time of the control circuit is longer than the response time of hysteresis control. Still, desired regulation is achieved within one modulation cycle.

Conventional control circuits, such as PWM-control or hysteresis control, rely on high-end components and on minimizing time delays in the control circuit, leading to higher cost and lower component availability than for the corresponding components of the new control circuit.

For example, a comparator used in the new control circuit may be 9-10 times slower than a comparator used in a conventional control circuit, e.g. 4.5 ns vs 40 ns.

As further explained below, at least one of, or both of, the first and second time periods may be equal to, or substantially equal to, one fourth the modulation period, e.g. at 50 % duty cycle, for example at least one of, or both of, the third and fourth time periods may be equal to, or substantially equal to, one fourth the modulation period, e.g. at 50 % duty cycle.

The sense voltage may be a function of the output voltage supplied to a load connected to an output of the power converter; or, the sense voltage may be a function of the output current supplied to a load connected to an output of the power converter; or, the sense voltage may be a function of power, i.e. output voltage times output current, supplied to a load connected to an output of the power converter; etc.

An output capacitor connected to an output of the power converter stabilizes the output voltage supplied by the power converter. The output capacitor is charged during turn-on of the power converter and discharged during turn-off of the power converter. During turn-on, the capacitor is charged with the current supplied by the power stage of the power converter minus the current supplied to the load connected to the output of the power converter. During turn-off, the capacitor is discharged with the load current. Thus, the slope of the voltage ripple ΔV_{out} developed across the output capacitor as a result of the charging and discharging of the output capacitor depends on the output current. If the output current is low, the slope of the voltage ripple is steep during turn-on of the power converter and low during turn-off of the power converter, and vice versa if the output current is high. This together with the first and second time periods causes the output voltage ripple to vary with varying output current and also causes the mean value of the output voltage V_{out} to vary with varying output current. Correspondingly, the ripple of the output current I_{out} and

output power P_{out}, and the mean value of output power P_{out} may also vary with varying output current.

This variation may be compensated in various ways in order to lower the amount of variation and making the desired output value more constant and independent of the output current at least within a predetermined output current range.

For example, the control circuit may be configured to compensate a dependence of the sense voltage, and thereby a dependence of the output voltage; or, the output current; or the output power; etc., on the output current, for example by varying the reference voltage in dependence on the output current in such a way that the dependence of the sense voltage on the output current is compensated. For example, an increase in output voltage may be compensated by lowering the reference voltage so that the power converter is turned-on at a lower voltage thereby lowering the resulting output voltage. The change in reference voltage takes place over a plurality of modulation periods. When the load is constant, the reference voltage does not change unless an adjustment of the output, such as the output voltage or current, is performed.

Additionally; or, alternatively, the control circuit may be configured to vary at least one of the first and second time periods in dependence of the output current, whereby the dependence of the sense voltage on the output current is compensated. For example, an increase in output voltage may be compensated by lowering the second time period so that the power converter is turned-on during a shorter time period thereby lowering the resulting output voltage. When the load is constant, the first and second time periods do not change.

BRIEF DESCRIPTION OF THE DRAWINGS

Below, the new method and the new power converter are explained in more detail with reference to the drawings in which various resonant examples of the new power converter are shown. In the drawings:

Fig. 1 shows a schematic diagram of a resonant power converter with the new control circuit,

Fig. 2 shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 3 shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 4 shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 5 shows a schematic circuit diagram of an exemplary new resonant power converter,

Fig. 6 shows exemplary signal conditioning circuits,

Fig. 7 shows exemplary switch drivers,

Fig. 8 shows a schematic circuit diagram of an exemplary new resonant power converter with a stop circuit,

Fig. 9 shows a switch driver with oscillator turn-off,

Fig. 10 shows a power circuit diagram of a VHF interleaved self-oscillating resonant SEPIC converter,

Fig. 11 is a plot of simulated waveforms of the power circuit shown in Fig. 10,

Fig. 12 shows a schematic circuit diagram of a model of a new resonant power converter used for calculation of component values,

Fig. 13 shows a circuit diagram of a control circuit used to control the power circuit shown in Fig. 10,

Fig. 14 is a plot of characteristic waveforms of the model shown in Fig. 12,

Fig. 15 is a plot of experimental waveforms of the control circuit shown in Fig. 13,

Fig. 16 is a plot of experimental waveforms of the power circuit shown in Fig. 10,

Fig. 17 (a) shows a plot of converter efficiency as a function of output power and (b) shows a plot of output voltage offset as a function of the load,

Fig. 18 is a flowchart of the new method,

Fig. 19 shows (a) a schematic circuit diagram of a model of the new resonant power converter together with (b) a conventional hysteretic control circuit and (c) a phase-shift burst mode control circuit,

Fig. 20 shows a plot of simulated waveforms of the model converter current and voltages controlled by the hysteretic control circuit,

Fig. 21 shows a plot of simulated waveforms of the model converter current and voltages controlled by the phase-shift burst mode control circuit, and

Fig. 22 shows schematic circuit diagrams of control circuits with varying sense voltage.

DETAILED DESCRIPTION OF EMBODIMENTS

The accompanying drawings are schematic and simplified for clarity, and they merely show details which are essential to the understanding of the new resonant power converter, while other details have been left out. The new resonant power converter according to the appended claims may be embodied in different forms not shown in the accompanying drawings and should not be construed as limited to the examples set forth herein.

Like reference numerals refer to like elements throughout. Like elements may, thus, not be described in detail with respect to the description of each figure.

Fig. 1 shows a schematic block diagram of a resonant power converter 10 controlled in accordance with the new method. The illustrated resonant power converter 10 comprises a VHF power circuit 12, a control circuit 14 with a control output 16, and a signal conditioning circuit 18 providing a sense voltage 20 based on and corresponding to the output voltage 22.

The control circuit 14 is coupled to compare the sense voltage 20 with a reference voltage 24.

Alternatively, the sense voltage 20 may be provided by a current sensor, such as a resistor, a hall element, etc., coupled so that the sense voltage corresponds to an output current of the resonant power converter 10.

The control circuit 14 has a control output 16 that is coupled to control turn-on and turn-off of the VHF power circuit 12 of the resonant power converter.

In the illustrated examples, the output voltage and the sense voltage have positive values, so that the absolute value of the sense voltage or the output voltage is equal to the value itself.

The VHF power circuit 12 of the resonant power converter 10 is turned-on when the sense voltage 20 is less than or equal to the reference voltage 24 and a first time period has elapsed since a previous turn-off of the VHF power circuit 12. The VHF power circuit 12 of the resonant power converter 10 is turned-off when the sense voltage 20 is larger than or equal to the reference voltage 24 and a second time period has elapsed since a previous turn-on of the VHF power circuit 12.

The VHF power circuit 12 may be of any known resonant power converter topology with a frequency of operation in the MHz range, such as at or above 20 MHz, such as at or above 30 MHz, such as in the 30 MHz – 300 MHz range, such as converters comprising: a class E inverter and a class E rectifier, a class DE inverter and a class DE rectifier, a class DE inverter and a class E rectifier, etc.; or, class EF2 (or class Φ) converters, resonant SEPIC converters, etc.

The resonant power converter may be driven by an oscillator, or the converter may be self-oscillating. Further, the resonant power converter may be interleaved.

Inherent signal propagation delays of the components of the control circuit 14 forms parts of the first and second time periods, and the inherent signal propagation delays may form the entire first and second time periods. Additionally, one or more delay circuits may

provide part of the first time period and/or part of the second time period, namely part of the third time period and/or part of the fourth time period.

The control circuit 14 may comprise a comparator that is coupled to compare the sense voltage 20 with the reference voltage 24, and having a comparator output that is the control output 16.

The delays with which the comparator changes state of its output from high to low and vice versa, in response to changed input(s), constitute part of the respective first and second time periods, namely part of the third time period and/or part of the fourth time period.

The signal conditioning circuit 18 may be a low-pass filter configured to output the sense voltage.

The control output 16 may be coupled to control turn-off of at least one power switch (not shown) of the resonant power converter 10 thereby turning the resonant power converter off.

This is illustrated in the class E inverter based resonant power converters shown in Figs. 2 and 3. The only difference between the resonant power converter of Fig. 2 and the resonant power converter of Fig. 3 is that inductor L_3 of Fig. 2 has been substituted by rectifier D_1 in Fig. 3.

Alternatively, or additionally, the control output 16 may be coupled to control other parts of the resonant power converter circuit than the power switches, e.g. by enabling and disabling energy transfer from the input to the output of the resonant power converter 10, e.g. by turning the resonant power converter on and off by changing the impedance or the loop-gain of the resonant part of the power circuit, whereby the resonant power converter is turned-off by changing the impedance to a first value at which the power circuit does not oscillate, and whereby the resonant power converter is turned-on by changing the impedance to a second value at which the power circuit oscillates.

This is illustrated in Figs. 4 and 5 showing a class E inverter based resonant power converter similar to the class E inverter based resonant power converters shown in Fig. 3 except for the fact that the control output 16 turns S_2 on and off.

In Fig. 4, the resonant part of the resonant power converter 10 does not oscillate when switch S_2 is turned-on, and the resonant part of the resonant power converter 10 oscillates and operates like the resonant power converter 10 of Fig. 3 when switch S_2 is turned-off.

In Fig. 5, the functions of rectifier D2 and switch S2 of Fig. 4 are combined in switch S2 functioning as a synchronous rectifier in Fig. 5 when the second self-oscillating gate driver is enabled so that the resonant power converter is turned on.

Fig. 6 shows circuit diagrams of two examples of low-pass filters that may constitute the signal conditioner 18.

The signal conditioners shown in Figs. 6 (a) and (b) may be substituted with any suitable signal conditioner chosen from other signal conditioner designs available to the person skilled in the art.

Examples of self-oscillating gate drivers are shown in Fig. 7.

In Fig. 7(a), a low enable signal keeps the gate of the power switch at zero voltage, whereby oscillation of the power circuit is inhibited, while a high enable signal allows propagation of the VHF oscillator signal driving the gate of the power switch causing the power circuit to oscillate.

In Fig. 7(b), a low enable signal switches switch transistor S_{aux} off and keeps the gate of the power switch at a constant voltage, whereby oscillation of the power circuit is inhibited, while a high enable signal allows propagation of the VHF oscillator signal driving the switch transistor S_{aux} on and off thereby driving the power switch on and off causing the power circuit to oscillate.

The gate drivers shown in Figs. 7 (a) and (b) may be substituted with any suitable gate driver chosen from other gate driver designs available to the person skilled in the art.

Fig. 8 shows a schematic circuit diagram of an exemplary new resonant power converter with a stop circuit,

Fig. 9 shows a switch driver with oscillator turn-off,

Fig. 10 is a circuit diagram of a power circuit 12 of an interleaved self-oscillating resonant SEPIC converter, wherein two power circuits 12a, 12b drive each other via capacitive coupling C_{X1} and C_{X2} between the switches S_1 and S_2 and operate in interleaved mode.

The power circuits are substantially identical, i.e.:

$$L_{I1} = L_{I2} = L_I$$

$$C_{I1} = C_{I2} = C_I$$

$$C_{X1} = C_{X2} = C_X$$

$$C_{S1} = C_{S2} = C_S$$

The values of the most important parasitic components of the semiconductor devices, namely diode junction capacitors and parasitic capacitors of the semiconductor switches, are included in determination of operating frequency of the resonant power converter. The

oscillation frequency f_S is determined mainly by the inductance L_I and the total capacitance seen from the drain when the rectifiers are shorted, $C_{DS,tot}$

$$f_s = \frac{1}{2\pi\sqrt{L_I C_{DS,tot}}}$$

where

$$C_{DS,tot} = C_I + C_{OSS} + C_S + C_X||C_{ISS}$$

$$C_{OSS} = C_{DS} + C_{DG}$$

$$C_{ISS} = C_{GS} + C_{DG}$$

Oscillations start once the gate voltages of the MOSFET switches S_1 and S_2 become slightly higher than the MOSFET threshold voltage. Simulated waveforms of the resonant power circuit of Fig. 10 are shown in Fig. 11. Ideally, respective waveforms of the two interleaved power converters are identical and shifted 180° with relation to each other.

If VHF ripple is neglected, the converter output can be modeled as a current source with the current value of I_0. When an on/off modulation is applied on the converter, the current supplied by the converter i_{conv} to C_{out} and the load may be approximately modeled as a current square wave:

$$i_{conv} = \begin{cases} I_0, \ when\ the\ converter\ is\ ON \\ 0, when\ the\ converter\ is\ OFF \end{cases}$$

Output current I_{out} is equal to average value of i_{conv} over one modulation cycle. The resulting current going into C_{out} is i_{conv} - I_{out}, which has no DC component in steady state. If parasitics of C_{out} are negligible, the resulting V_{out} voltage waveform is a triangular wave. Assuming that turn-on and turn-off delays are independent of the output voltage rate of change, the output voltage ripple is

$$\Delta V_{out} = \frac{I_{out}}{C_{out}} t_{D,on} + \frac{I_0 - I_{out}}{C_{out}} t_{D,off}$$

where $t_{D,on}$ is the fourth time period and $t_{D,off}$ is the third time period, i.e. $t_{D,on}$ and $t_{D,off}$ are the control loop turn-on and turn-off delays, respectively, from the sense voltage crossing the reference voltage and to turn-on or turn-off, respectively, of the power converter. If the control circuit's delays are constant, the equation shows that V_{out} is a linear function of I_{out}, and the longer delay defines $V_{out,max}$. In the special case of $t_{D,on}$ and $t_{D,off}$ being equal, V_{out} is independent of I_{out}. At any given load, the offset of V_{out}: $\Delta V_{out,off}$, and f_M are determined from the values of C_{out} and the delays $t_{D,on}$ and $t_{D,off}$ by:

$$\Delta V_{out,off} = \frac{\Delta V_{out}}{2} \frac{t_{D,on} - t_{D,off}}{t_{D,off} + t_{D,on}}$$

and

$$f_M = \frac{I_0}{C_{out}\,\Delta V_{out}} \frac{I_{out}}{I_0} \left(1 - \frac{I_{out}}{I_0}\right)$$

Modulation frequency is highest at 50% duty cycle, i.e. the power converter is turned on half the time:

$$f_{M,max} = \frac{1}{2\,(t_{D,on} + t_{D,off})}$$

I_0 is not known from values of circuit components. An approximate value of I_0 can be determined from Spice simulations. Once I_0 is obtained, the output filter and the feedback circuit need to be designed to provide a desired modulation frequency f_M at a specified load.

Fig. 12 shows a block diagram of such a low frequency model of a resonant power. The VHF power circuit 12 is modelled as an on-off controllable DC current source.

The conditioning circuit 18 at the input of the control circuit 14, see Fig. 13, has a simple transfer function:

$$H(s) = \frac{A_{FB}}{1 + s\tau_{FB}}$$

Where

$$A_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

$$\tau_{FB} = \frac{R_{FB1}R_{FB2}}{R_{FB1} + R_{FB2}}\, C_{FB}$$

The comparator 26 of the control circuit 14 model is ideal; the propagation delay of the real comparator is added into the delay block. The delay block is represented by two different time delays, since the shutdown of the power circuit is significantly faster than the start-up sequence. This is because shutdown is performed by the auxiliary switches S_{aux1} and S_{aux2}, while during start-up C_{ISS} is passively charged from the bias voltage V_B through the biasing resistors.

Fig. 13 shows the control circuit 14. The sense voltage 20 is low-pass filtered in *H(s)*, a voltage divider/low pass filter 18 formed by R_{FB1}, R_{FB2}, and C_{FB}, and input to the comparator 26. The comparator output 16 turns the switches S_{aux1} and S_{aux2} on and off in response to

the voltage difference at the comparator inputs. When S_{aux1} and S_{aux2} are on, v_{GS1} and v_{GS2} are zero and the power circuit oscillations are inhibited. Once S_{aux1} and S_{aux2} are off, C_{ISS1} and C_{ISS2} are charged through R_{B1} and R_{B2}, whereby v_{GS1} and v_{GS2} start to increase from 0 to V_B. After the first time period, when v_{GS1} and v_{GS2} exceed the power MOSFET threshold voltage V_{th}, switches S_1 and S_2 enter saturation and initiate oscillations in the power circuit. $H(s)$ has two primary purposes: to filter high frequency noise and adjust the feedback voltage level. It also contributes to propagation delay in the feedback loop.

In Fig. 14, characteristic voltage and current levels from a numerical example of the model are shown, where

- C_{out} = 3.3 µF
- I_0 = 1.04 A, I_{out} = 0.52 A
- R_{FB2} = 2 kΩ, R_{FB1} = 8.2 kΩ
- C_{FB} = 220 pF
- $t_{d,on}$ = 700 ns + 170 ns = 870 ns
- $t_{d,off}$ = 170 ns

The parameters are chosen to approximate the experimental setup described below. $v_{gate}(t)$ represents the gate voltages of S_1 and S_2 with removed VHF component. $V_{out}(t)$ passes through the single pole transfer function $H(s)$ and results in a distorted triangular waveform $v_{FB}(t)$. Average value of $v_{FB}(t)$ is slightly lower than the reference V_{ref} voltage, which is due to $t_{d,on} > t_{d,off}$. This is also the cause of the duty cycle of the comparator output $v_{cmp}(t)$ to be lower than 50%. Since the referent output voltage is 10 V, a small offset can be observed in $V_{out}(t)$. This offset is dependent on the duty cycle of the power circuit, the time difference $t_{d,on} - t_{d,off}$, and C_{out}. $t_{d,on}$ depends on the voltage difference between V_B and V_{th}. Obtained modulation frequency is very close to 300 kHz.

In order to verify the analysis explained above, a 10.5 W prototype converter with regulation of the output voltage was produced and the measurements for the prototype converter is disclosed below.

Plots of drain, gate, and rectifier voltages in the power circuit are shown in Fig. 15. The drain and rectifier voltages were measured with capacitance of 2.2 pF in series with an oscilloscope probe, in order to reduce influence of the probe to the power circuit. This introduces attenuation of A = 0.19 in the measurement and removes the DC component of the measured voltages. Component values of the power circuit are listed in Table I. Switching frequency of the power circuit is f_S =49 MHz. Open loop output voltage and output voltage and current are V_{out} = 10.2 V and I_0 = 1.04 A, respectively.

When the duty cycle of 50% is obtained, I_{out} =0.5 I_0 = 0.52 A. Plots of the waveforms of the relevant voltages in the converter for this case are shown in Fig 9. Modulation frequency f_M is at its maximum value of 300 KHz at 50% duty cycle, and drops as the duty cycle moves away from 50%. In addition, under these conditions output voltage ripple $\Delta V_{out,pp}$ is at its maximum as well.

The comparator used in the circuit is AD8468 from Analog Devices. The component datasheet specifies 40 ns propagation delay. For comparison, a high speed TLV3501 comparator has a 4.5 ns propagation delay, which is a reduction by a factor of 9. This is by no means a limit since there are other significant contributors as well (conditioning and power circuit on-off circuit). This delay may be increased even further at a cost of a lower modulation frequency f_M and higher output voltage ripple for a given C_{out}.

Figs. 15 and 16 illustrate relationships between the signals in time domain, v_{cmp+}, v_{cmp-}, v_{GS}, v_{DS}, and v_{out} (upper waveforms) with respect to the comparator output (lower waveforms). High output voltage ripple is caused by a small output filtering capacitance (C_{out} = 3.3 μF).

Efficiency of the converter is shown in Fig. 17(a) as a function of output power. Since f_M is allowed to drop significantly under light load conditions, efficiency is maintained high over wide load range (η>75%above 20% load) with peak efficiency above 81%.

Since the control is based on phase shift, a small DC error is introduced in the value of v_{out}, which varies with the load. If the output voltage ripple is assumed triangular (which is reasonable since i_{conv} is a current square wave), the peak values of v_{out} are determined as:

$$V_{out+} = V_{out,ref} + \frac{I_0 - I_{out}}{C_{out}} \Delta t_+$$

$$V_{out-} = V_{out,ref} + \frac{-I_{out}}{C_{out}} \Delta t_-$$

So that the offset of V_{out} is determined by

$$V_{out,offset} = V_{out,ref} - \frac{\Delta V_{out+} + \Delta V_{out-}}{C_{out}} \Delta t_-$$

$v_{out,ref}$ is a target value for the output voltage set by V_{ref} and $R_{FB1} - R_{FB2}$ voltage divider. Δt_+ and Δt_- are the time delays from a point when v_{out} crosses $v_{out,ref}$ to a point where v_{out} reaches its maximum and minimum value, respectively. Depending on the variables in these equations, $v_{out,offset}$ may be either positive or negative, and decreases with I_{out}. Measured dependence of Δv_{out} is shown in the lower plot of Fig. 17. Both the offset and the output ripple are reduced with increase in C_{out}, while the switching frequency will be reduced.

A comparison between the model disclosed above and experimental results show close, but not perfect matching. The reasons for this are subjects of further investigation; it is

assumed that imperfections in the active components and tolerances of the passive components are the main contributors. Still, the model gives significant insight into the system operation, and can be used as a good estimate during the converter design.

Compared to hysteresis based burst mode control, the new method of controlling the resonant power converter allows use of a significantly slower and less expensive components in the control circuit, which is of importance for cost sensitive applications such as LED lighting and PoL converters. The illustrated power circuits and control circuits were implemented using only low cost commercially available components, with peak efficiency above 81% and high efficiency over wide load range.

Fig. 18 is a flowchart 100 of the new method of controlling a resonant power converter. The method starts with method step 110 wherein the resonant power converter is turned on.

When the resonant power converter is turned on, the output voltage and/or output current increases. A sense voltage is provided in the resonant power converter that corresponds to the output voltage or output current, and a reference voltage is provided in the resonant power converter that corresponds to a desired resulting output voltage or output current of the resonant power converter.

According to method step 120, the output voltage and/or output current continue to increase until the corresponding sense voltage V_{sense} is equal to or larger than the reference voltage V_{ref}, and

according to method step 130, the output voltage and/or output current continue to increase until also a second time period t_2 has elapsed since a previous turn-on of the resonant power converter.

Thus, when the sense voltage V_{sense} is equal to or larger than the reference voltage V_{ref}, and a second time period t_2 has elapsed since a previous turn-on of the resonant power converter, the resonant power converter is turned-off in method step 140.

When the resonant power converter is turned on, the output voltage and/or output current decreases.

According to method step 150, the output voltage and/or output current continue to decrease until the corresponding sense voltage V_{sense} is equal to or less than the reference voltage V_{ref}, and

according to method step 160, the output voltage and/or output current continue to decrease until also a first time period t_1 has elapsed since a previous turn-off of the resonant power converter.

Thus, when the sense voltage V_{sense} is equal to or less than the reference voltage V_{ref}, and a first time period t_1 has elapsed since a previous turn-off of the resonant power converter, the resonant power converter is turned-off in method step 110.

In the following, properties of the phase-shift burst mode control method for very high frequency (VHF) DC-DC converters are compared with a conventional control method with hysteresis based on comparison of a sense voltage with two threshold values. Again, an on-off controllable current source is used to model the low-frequency behaviour of VHF converters. Large output capacitance is used for output voltage filtering. The model is shown in Fig. 19(a).

Fig. 19(b) shows the model of Fig. 19(a) controlled with a conventional hysteretic control circuit and Fig. 19(c) shows the model of Fig. 19(a) controlled with a phase-shift burst mode control circuit.

For both circuits, the VHF power converter is operating (turned-on) when V_{ctrl} is high, e.g. 2 Volt, delivering an average current of I_0 = 2 A. The VHF power converter is turned-off when V_{ctrl} is low, e.g. 0 Volt. In the present example, capacitor C_{out} and load R_{load} are set to 10 µF and 10 Ω, respectively. Reference voltage V_{ref} equals 1 V, high impedance signal conditioning network $H(s)$ has ratio of V_{sense}/V_{out} = 1 : N, e.g. 1 : 10, independent of frequency. The circuit configurations and component values are selected so that the target output V_{out} is equal to 10 V and at nominal load, the VHF power converter operates at a 50 % duty cycle. It is assumed that gate drivers do not introduce any delay in any of the circuits of Figs. 19 (a) – (c) so that $V_{ctrl} = V_{cmp}$.

In the control circuit with hysteresis shown in Fig. 19(b), instantaneous response of the comparator is assumed so that the comparator does not add a delay in the control loop. In the present example, the hysteresis window is V_H = 20 mV. The comparator turns the converter on when $V_{sense} < V_{ref}$ and turns it off otherwise. Simulated waveforms of the converter voltages of the converter with hysteresis control are shown in Fig. 20.

Modulation frequency f_M, i.e. the frequency at which the converter turns on and off, is given by:

$$f_M = \frac{I_0/2}{2\,\Delta V_{out}\,C_{out}} = \frac{I_0/2}{2\,N\,V_H\,C_{out}}$$

This equation is derived under the assumption that propagation delay t_D of the comparator, the gate driver, and the power stage of the converter is zero, and the equation is a good approximation when $t_D \ll 1/f_M$. Expensive components, e.g. comparators, gate drivers, etc., have to be used in VHF designs to realize small propagation delays in the feedback loop.

Time difference ΔT from $V_{sense} = V_{ref}$ until $V_{sense} = V_{ref} + V_H$ in Fig. 20 equals $1/(4\ f_M)$. If V_H -> 0 and t_D -> $1/(4\ f_M)$, the waveforms shown in Fig. 20 turn into the waveforms shown in Fig. 21 showing simulated waveforms of the converter voltages of the converter with phase shift burst mode control. The waveforms in Figs. 20 and 21 are aligned so that V_{sense} voltages cross the respective V_{ref} voltages at the same time, e.g. 2 µs, 4 µs, 6 µs, etc. The output voltage ripples are identical in Figs. 20 and 21, however the signal propagation delay through the feedback loop is $1/(4\ f_M)$, see the time difference between converter currents $I_{conv,H/PS}$, comparator output voltages $V_{cmp,H/PS}$, etc.

With the component values mentioned above, the modulation frequency is 250 kHz.

In Fig. 21, the power converter is turned-on at 3 µs, 7 µs, 11 µs, and 15 µs, and the power converter is turned-off at 1 µs, 5 µs, 9 µs, and 13 µs, and the first time period is equal to the second time period that is equal to 2 µs and the fourth time period, i.e. the turn-on delay $t_{D,on}$, is equal to the third time period, i.e. the turn-off delay $t_{D,off}$, that is equal to 1 µs.

The converter with phase shift burst mode control provides the same output voltage ripple (i.e. $\Delta V_{out,H} = \Delta V_{out,PS}$) as the converter with conventional hysteresis control, while using one or more components in the feedback loop with significantly larger respective delays. The resulting delay may be distributed arbitrarily between the power stage, the comparator, and the gate driver(s). This is very important for VHF converters, since numerous start-up and shutdown techniques (self-oscillating gate drivers and converters) with small, but finite delays may be utilized in a VHF converter with phase shift burst mode control.

Turn-on and turn-off delay ($t_{D,on}$ and $t_{D,off}$) do not need to be equal, either. Any one of the components in the feedback loop in any combination may contribute to the values of the turn-on and turn-off delays, with the restraint that:

$$t_{D,on} + t_{D,off} = \frac{1}{2\ f_M}$$

Output voltage of a converter with hysteresis control resides within the range from $H(s)^{-1}(V_{ref,H} - V_H)$ to $H(s)^{-1}(V_{ref,H} + V_H)$, resulting in a voltage ripple of $\Delta V_{out,H}$.

This is different of a converter with phase shift burst mode control as illustrate in Fig, 19 (c) in which the output voltage V_o is load dependent. The output voltage V_o decreases with increased load. If output voltage ripple at I_{out} = 1A is $\Delta V_{out,PS}$ and under assumptions of constant delay in the comparator (and otherwise ideal components), average value of $V_{out,PS}$ ranges from $\Delta V_{out,PS}/2$ at I_{out} = 0 to $-\Delta V_{out,PS}$ at $I_{out} = I_0$ linearly with I_{out}.

The variation of the output voltage V_o as a function of output current may be decreased in various ways. One way is to allow the reference voltage to change as a function of the output voltage V_o to compensate for the change in the output voltage V_o.

Fig. 22(a) shows a control circuit in which the sense voltage 20 is compared to a reference voltage 28 that is adjusted as a function of the mean output voltage V_o. $H_1(s)$ is an ordinary low-pass filter. In the illustrated circuit $V_{ref1} = V_{ref} - (V_{ref,mean} - V_{ref})$, where $V_{ref,mean}$ is the output of the low-pass filter $H_1(s)$. Thus, $V_{ref1} = V_{ref}$ when $V_{ref,mean} = V_{ref}$ and V_{ref1} decreases when the mean output voltage V_o increases and vice versa whereby the variation of the mean output voltage V_o as a function of output current is counteracted.

Fig. 22(b) shows another control circuit in which the sense voltage 20 is compared to a reference voltage 28 that is adjusted as a function of the mean of the comparator output voltage $V_{cmp,PS}$ 16. The operation of the illustrated control circuit is based on the fact that the average value of $V_{cmp,PS}$ varies linearly with the output current I_{out}.

Reference voltage V_{ref1} is formed by superposition of $V_{ref,PS}$ and low-pass filtered $V_{cmp,PS}$. The resistor and capacitor values in the compensation network need to be chosen to provide sufficient attenuation of the ac component of $V_{cmp,PS}$.

In the illustrated control circuit, when the converter operates at 50% modulation, the average of $V_{cmp,PS}$ equals V_{ref}. If the output current I_{out} is reduced, the average value of $V_{cmp,PS}$ is reduced, thus decreasing reference voltage V_{ref1} 28 thereby counteracting the increase of the output voltage V_o that would otherwise result for the reduced output current I_{out}. If the output current I_{out} is increased, the average value of $V_{cmp,PS}$ is increased, thus increasing reference voltage V_{ref1} 28 thereby counteracting the decrease of the output voltage V_o that would otherwise result from the increased output current I_{out}. V_{ref1} is calculated with the following formulae:

$$V_{ref1} = V_{ref,PS}\frac{R_1||(R_2+R_3)}{R_1} + V_{cmp,PS,high}\frac{I_{out}}{I_0}\frac{R_1||(R_2+R_3)}{R_1}$$

.

CLAIMS

1. A power converter comprising a control circuit coupled to compare a sense voltage with a reference voltage, and having a control output that is coupled to control turn-on and turn-off of the power converter in such a way that

the power converter is turned-on when an absolute value of the sense voltage is less than or equal to an absolute value of the reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

the power converter is turned-off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a second time period has elapsed since a previous turn-on of the power converter.

2. A power converter according to claim 1, wherein the control circuit comprises a comparator that is coupled to compare the sense voltage with the reference voltage, and having a comparator output that is the control output.

3. A power converter according to claim 1 or 2, wherein the power converter is configured for operation at a frequency above 1 MHz.

4. A power converter according to any of the previous claims, comprising a delay circuit configured for providing at least part of at least one of the respective time periods.

5. A power converter according to any of the previous claims, wherein an output voltage of the power converter is coupled to a signal conditioning circuit configured to output the sense voltage.

6. A power converter according to any of the previous claims, wherein the control output is coupled to control turn-off of at least one power switch of the power converter.

7. A power converter according to any of claims 1 - 6, wherein the control output is coupled to control disconnection of energy transfer from the input to the output of the power converter.

8. A power converter according to any of claims 1 - 6, wherein the control output is coupled to control connection of energy transfer from the input to the output of the power converter.

9. A power converter according to any of the previous claims, wherein the power converter is a SEPIC converter.

10. A power converter according to claim 9, wherein the SEPIC converter is a self-oscillating SEPIC converter.

11. A power converter according to claim 9 or 10, wherein the power converter is an interleaved SEPIC converter.

12. A power converter according to any of the previous claims, wherein the control circuit is configured to compensate a dependence of the sense voltage on an output current.

13. A power converter according to claim 12, wherein the control circuit is configured to vary the reference voltage in dependence on the output current, whereby the dependence of the sense voltage on the output current is compensated.

14. A power converter according to claim 12, wherein the control circuit is configured to vary at least one of the first and second time periods in dependence of the output current, whereby the dependence of the sense voltage on the output current is compensated.

15. A method of controlling a power converter, comprising the steps of

turning the power converter on when an absolute value of a sense voltage is less than or equal to an absolute value of a reference voltage and a first time period has elapsed since a previous turn-off of the power converter, and

turning the power converter off when the absolute value of the sense voltage is larger than or equal to the absolute value of the reference voltage and a second time period has elapsed since a previous turn-on of the power converter.

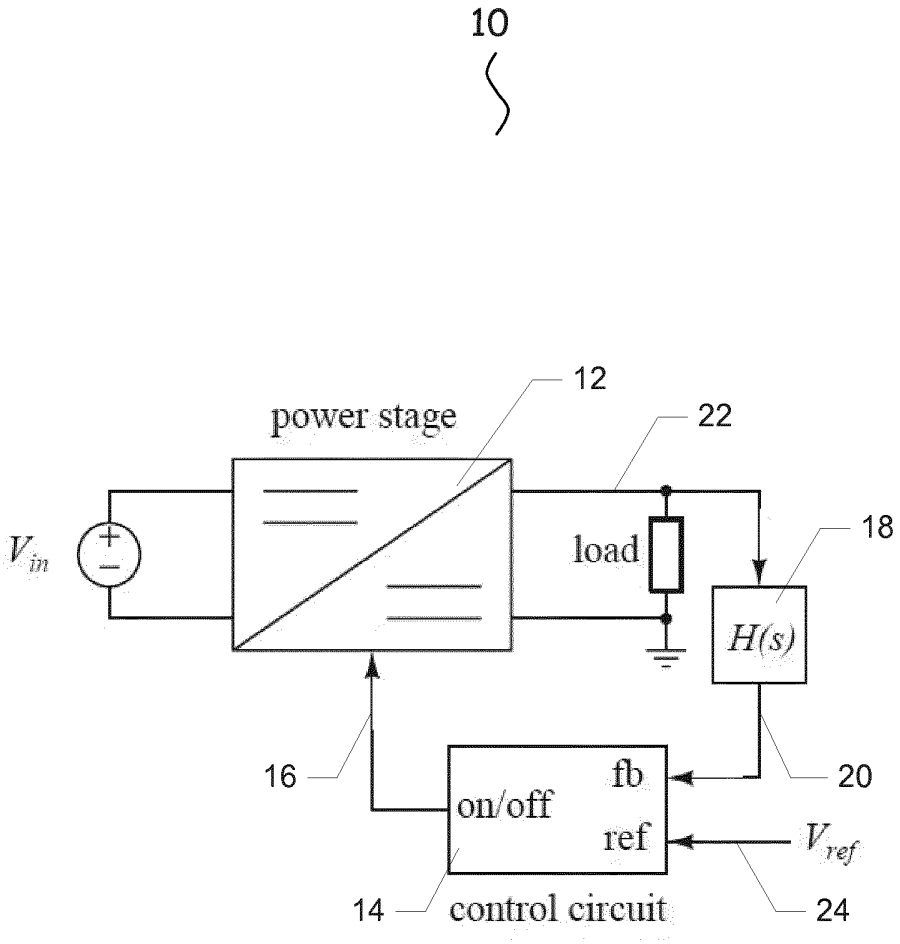

10
12
power stage
22
18
V_{in}
load
H(s)
16
fb
on/off
ref
V_{ref}
20
14
control circuit
24

Fig. 1

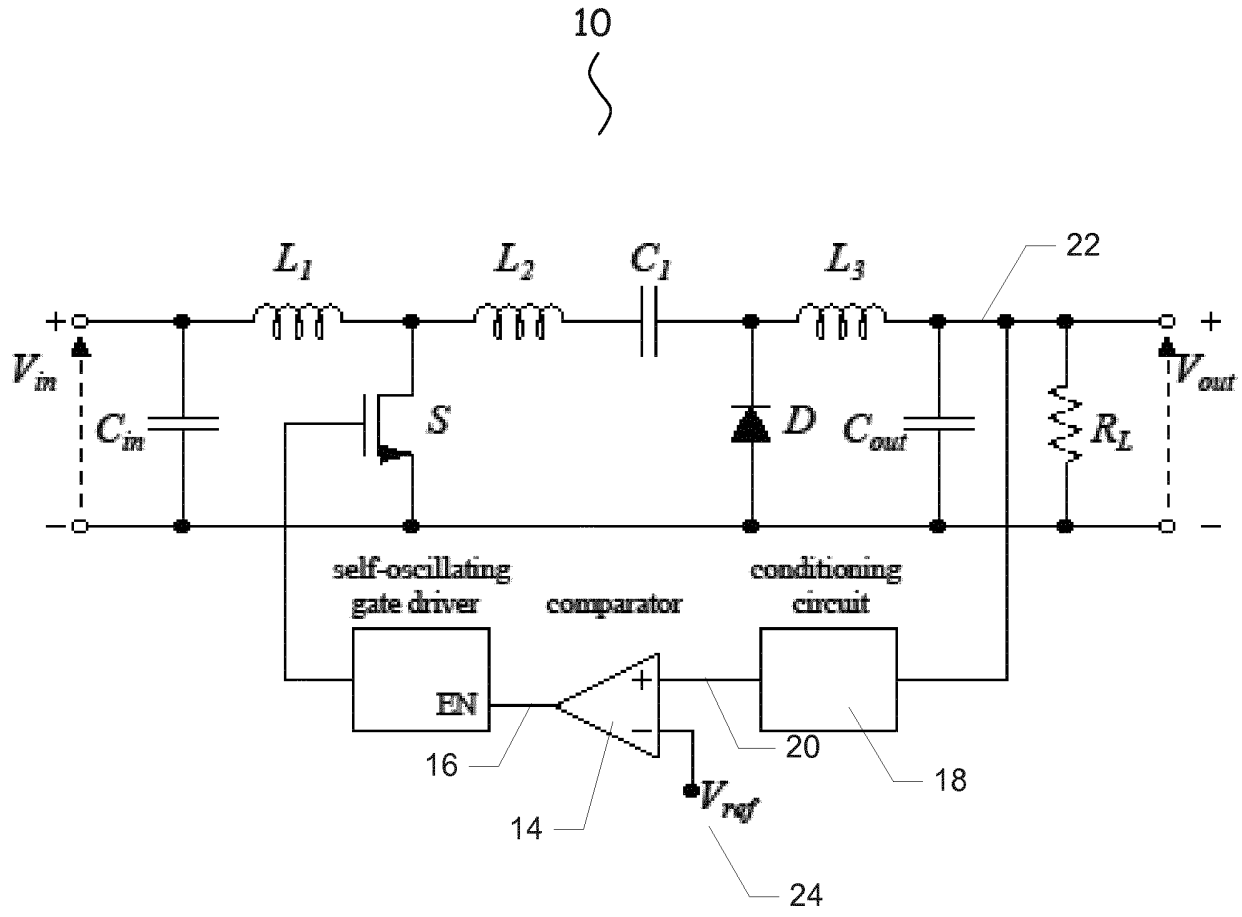

10
L_1
L_2
C_1
L_3
22
V_{in}
C_{in}
S
D
C_{out}
R_L
V_{out}
self-oscillating gate driver
comparator
conditioning circuit
EN
16
14
V_{ref}
20
18
24

Fig. 2

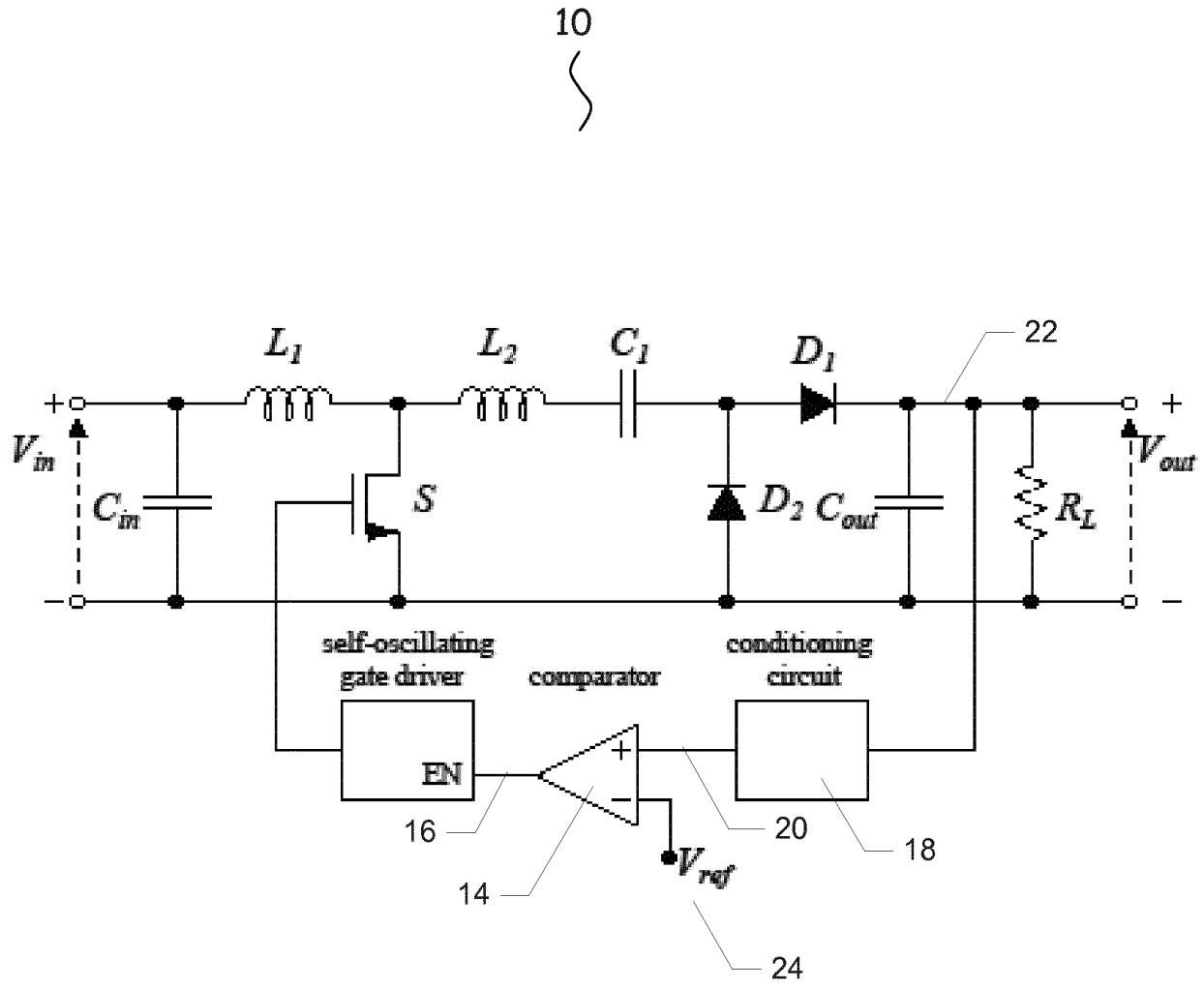

10
L_1
L_2
C_1
D_1
22
V_{in}
C_{in}
S
D_2 C_{out}
R_L
V_{out}
self-oscillating gate driver
comparator
conditioning circuit
EN
16
14
V_{ref}
20
18
24

Fig. 3

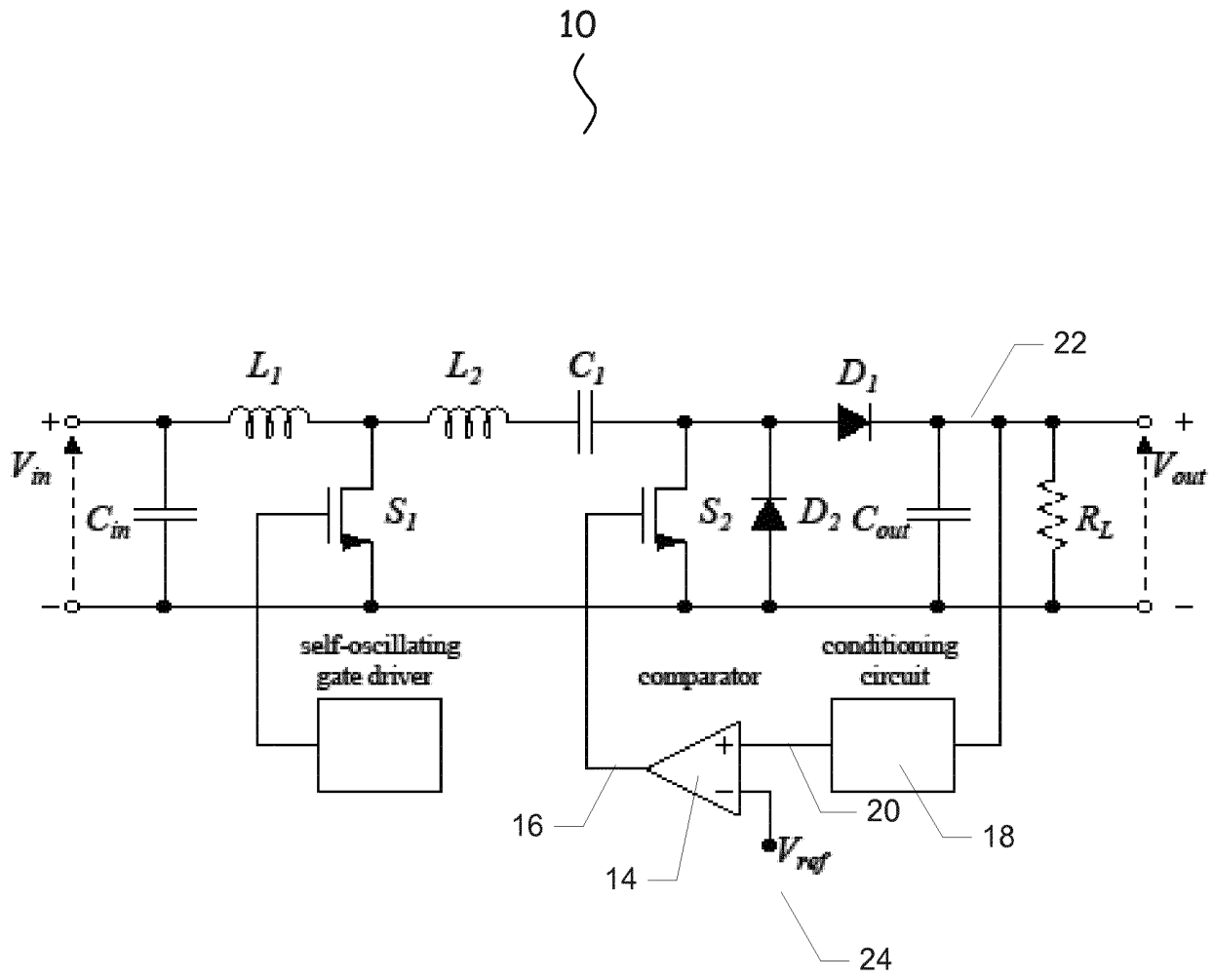

10
22
L_1
L_2
C_1
D_1
V_{in}
C_{in}
S_1
S_2
D_2
C_{out}
R_L
V_{out}
self-oscillating gate driver
comparator
conditioning circuit
16
14
V_{ref}
20
18
24

Fig. 4

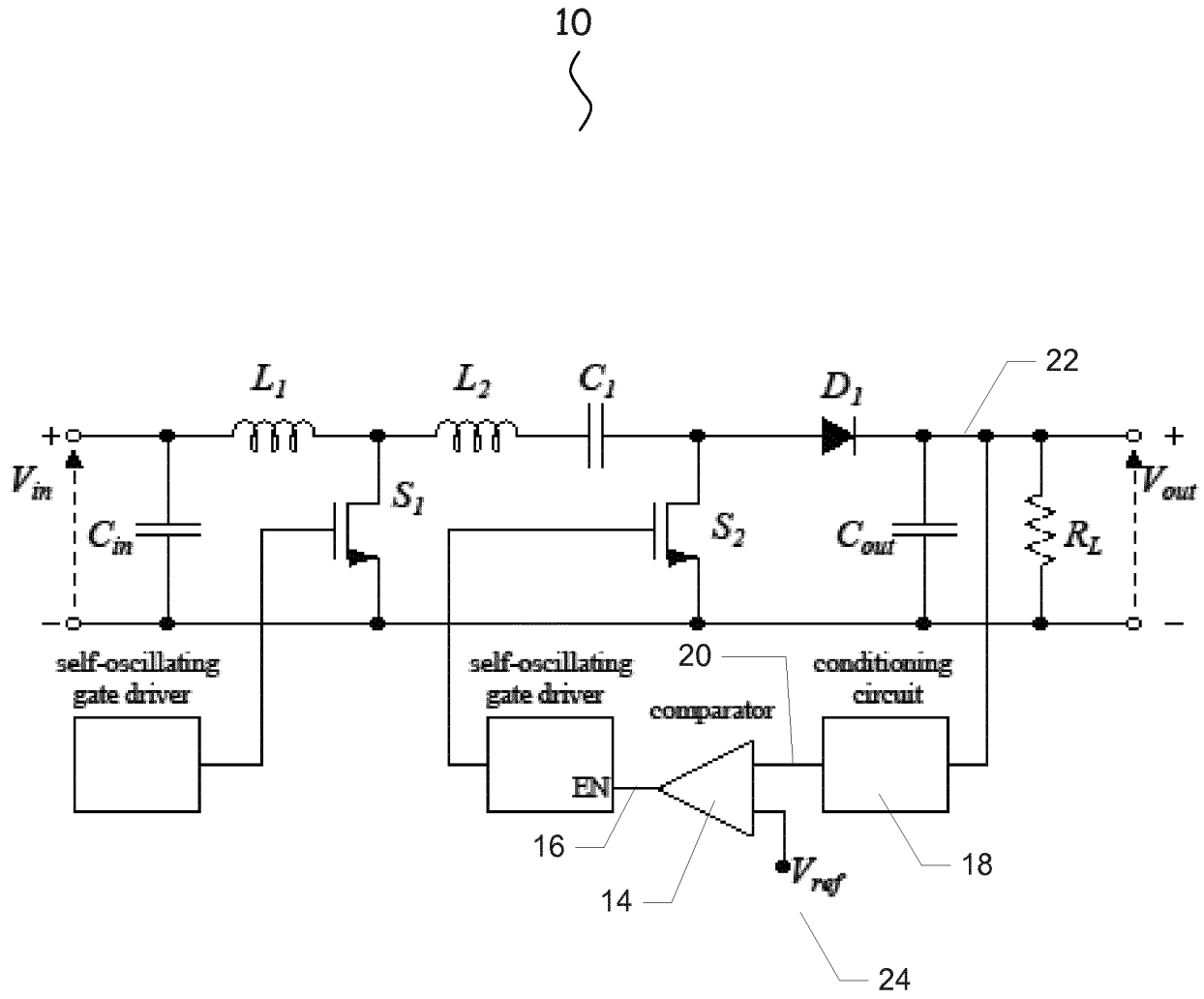
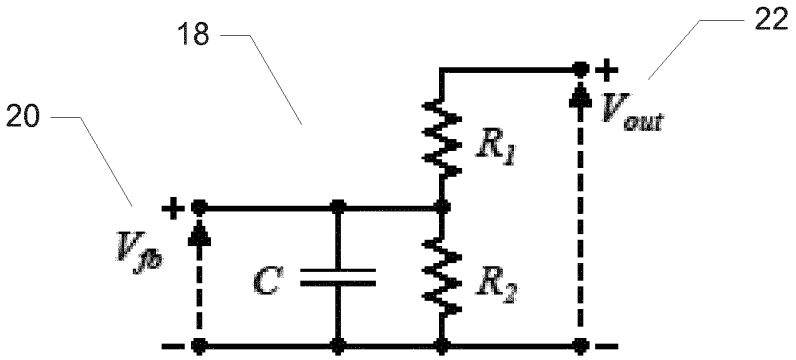
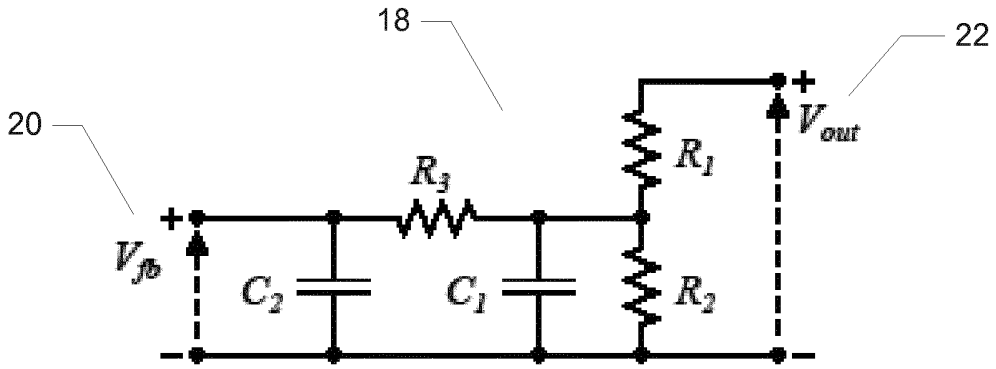

10
L_1
L_2
C_1
D_1
22
V_{in}
C_{in}
S_1
S_2
C_{out}
R_L
V_{out}
self-oscillating gate driver
self-oscillating gate driver
20
comparator
conditioning circuit
EN
16
14
V_{ref}
18
24

Fig. 5

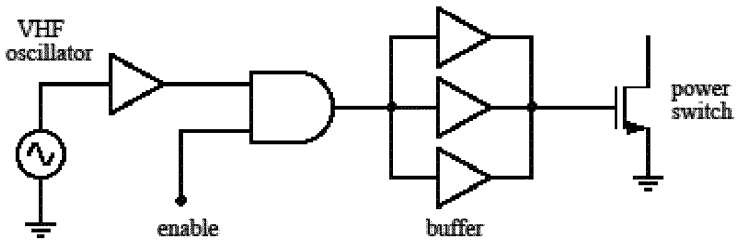


(a)

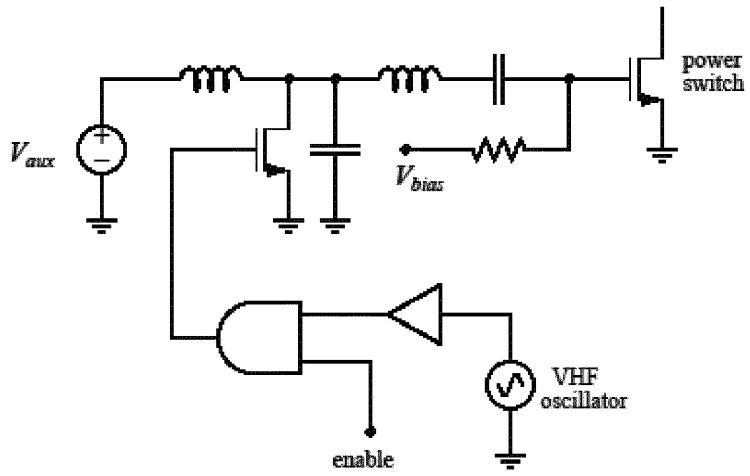


(b)

Fig. 6


VHF
oscillator
enable
buffer
power
switch

(a)


power
switch
V_{aux}
V_{bias}
VHF
oscillator
enable

(b)

Fig. 7

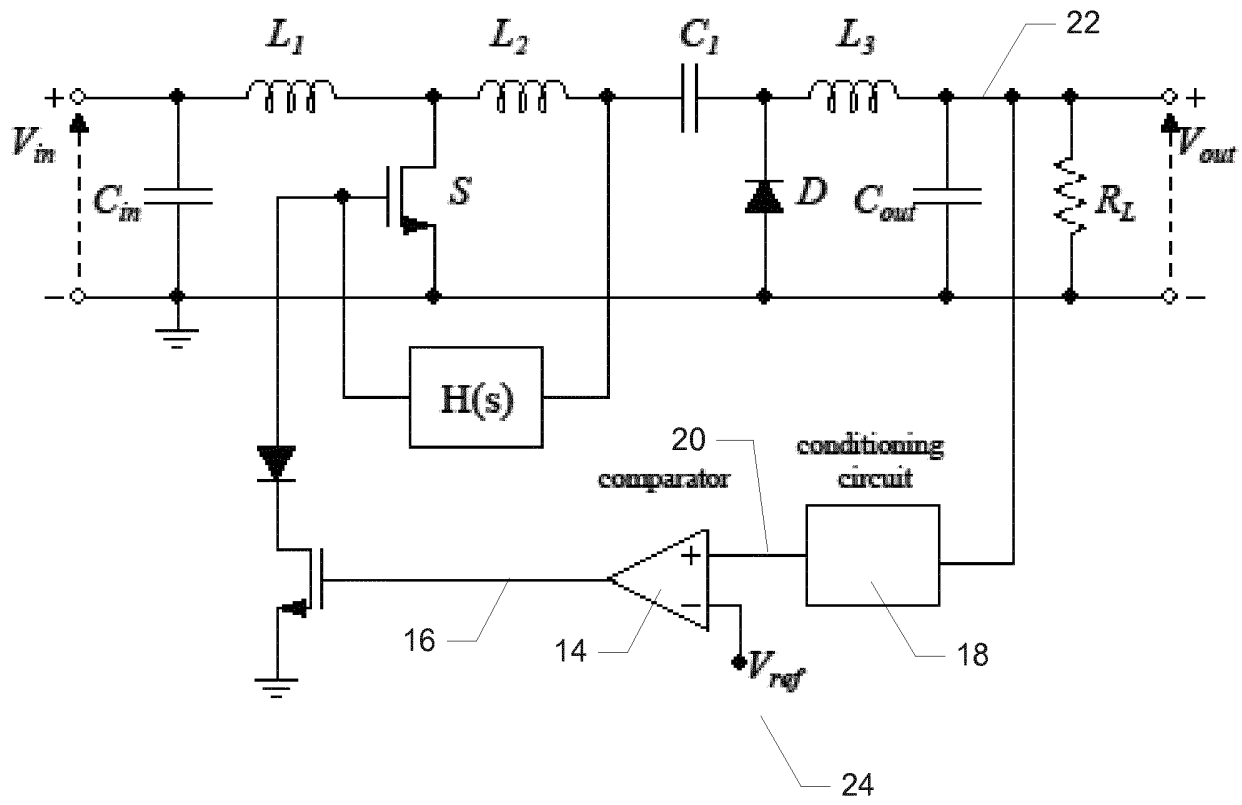

L_1
L_2
C_1
L_3
22
V_{in}
C_{in}
S
D
C_{out}
R_L
V_{out}
H(s)
20
comparator
conditioning circuit
16
14
V_{ref}
18
24

Fig. 8

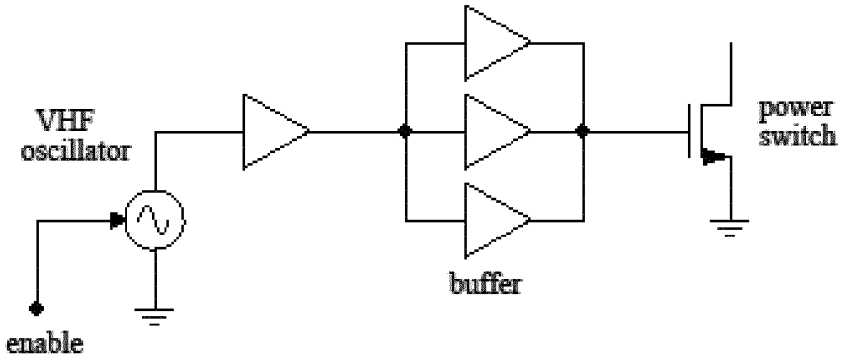


Fig. 9

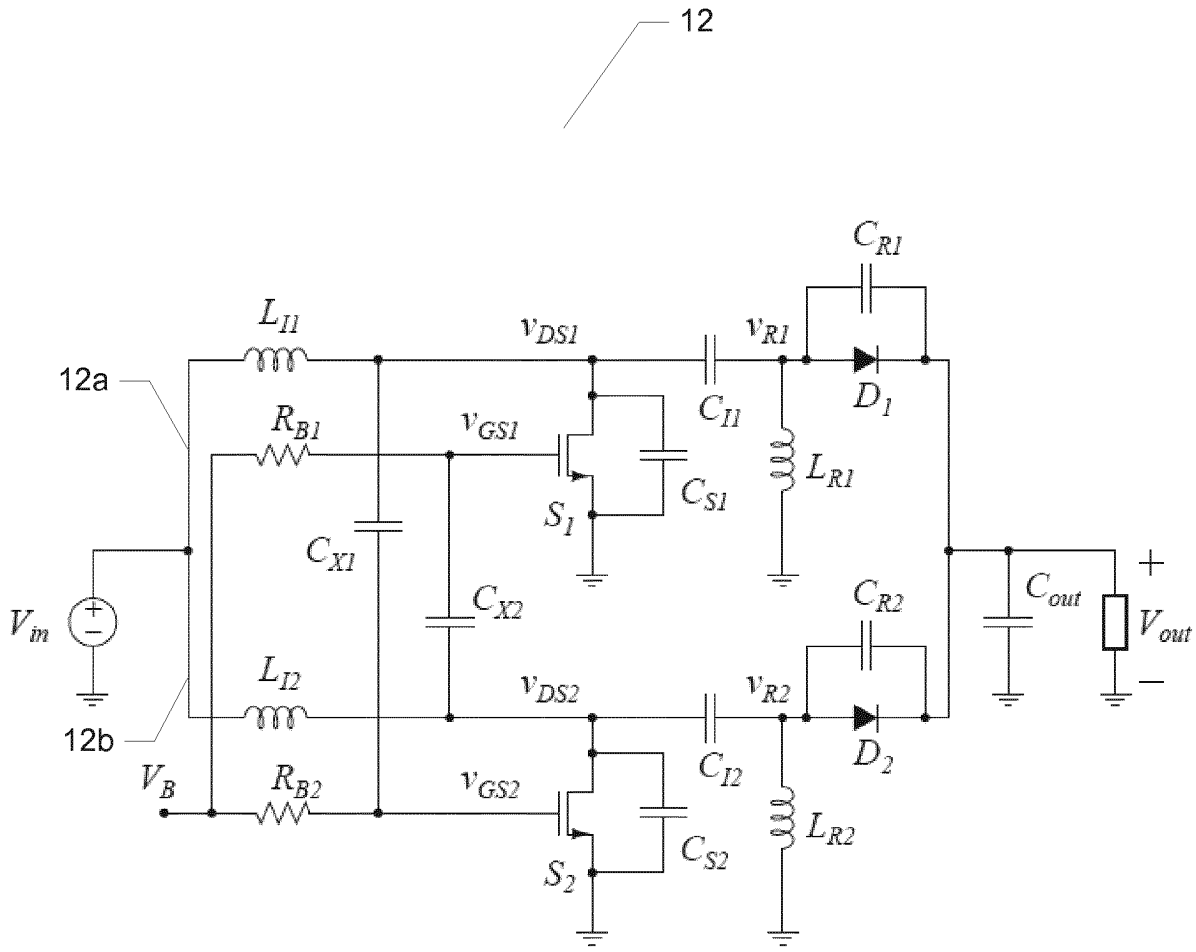

12
12a
12b
L_{I1}
v_{DS1}
v_{R1}
C_{R1}
D_1
C_{I1}
L_{R1}
R_{B1}
v_{GS1}
S_1
C_{S1}
C_{X1}
C_{X2}
V_{in}
L_{I2}
v_{DS2}
v_{R2}
C_{R2}
D_2
C_{I2}
L_{R2}
V_B
R_{B2}
v_{GS2}
S_2
C_{S2}
C_{out}
V_{out}
+
−

Fig. 10

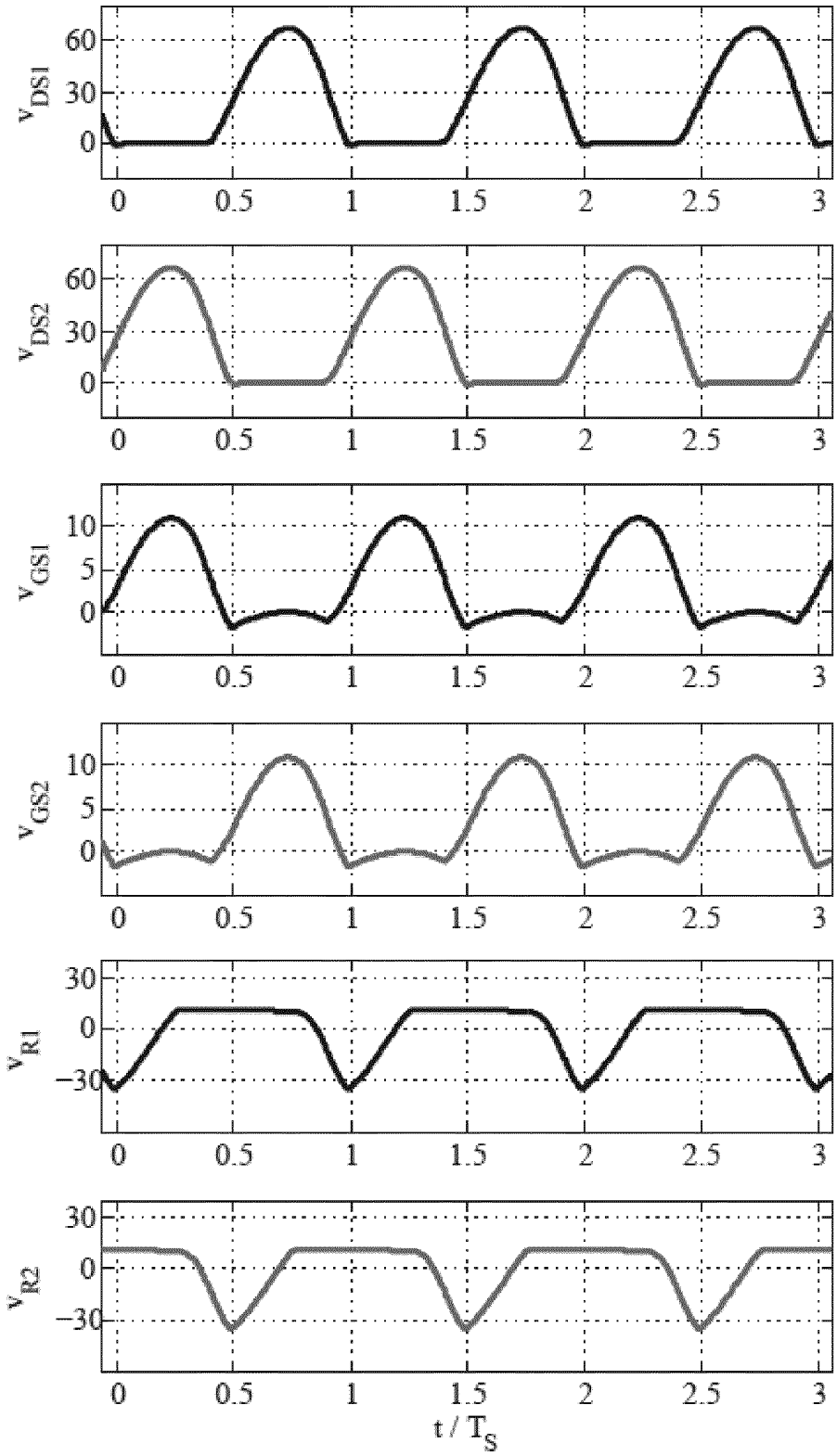

v_{DS1}
60
30
0
v_{DS2}
60
30
0
v_{GS1}
10
5
0
v_{GS2}
10
5
0
v_{R1}
30
0
−30
v_{R2}
30
0
−30
0
0.5
1
1.5
2
2.5
3
t / T_S

Fig. 11

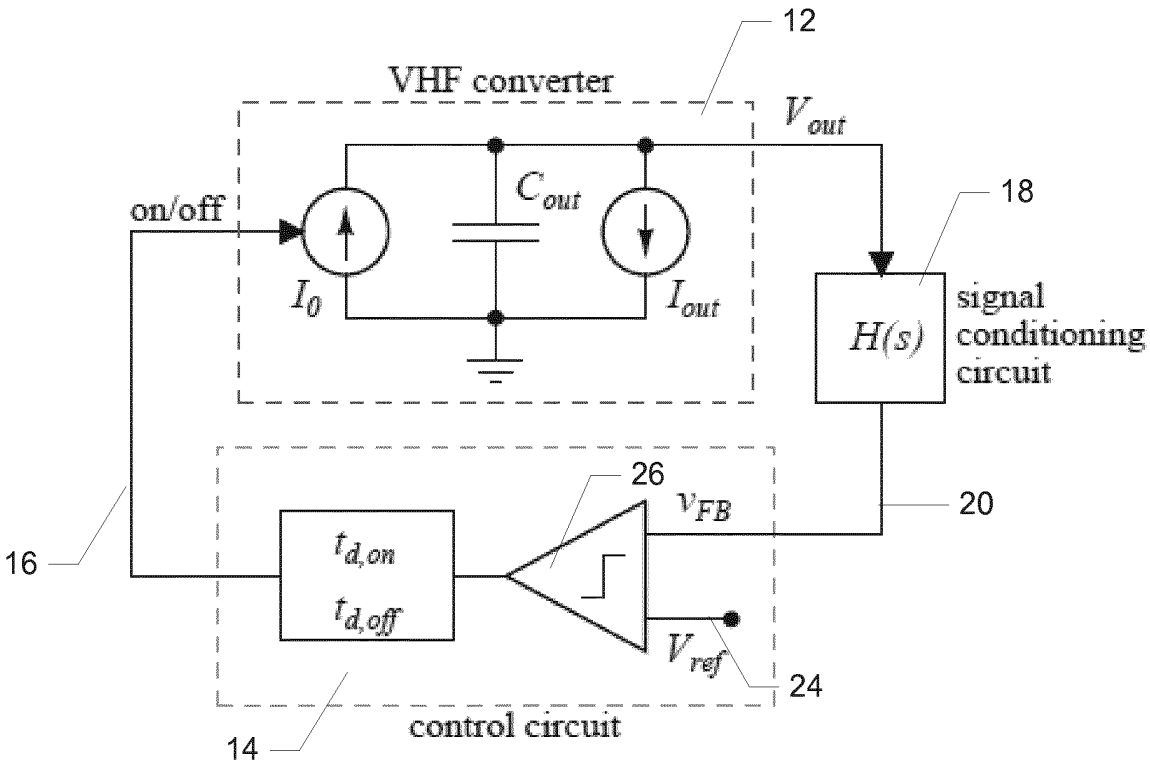

12
VHF converter
V_{out}
C_{out}
on/off
I_0
I_{out}
18
$H(s)$
signal conditioning circuit
26
v_{FB}
20
16
$t_{d,on}$
$t_{d,off}$
V_{ref}
24
14
control circuit

Fig. 12

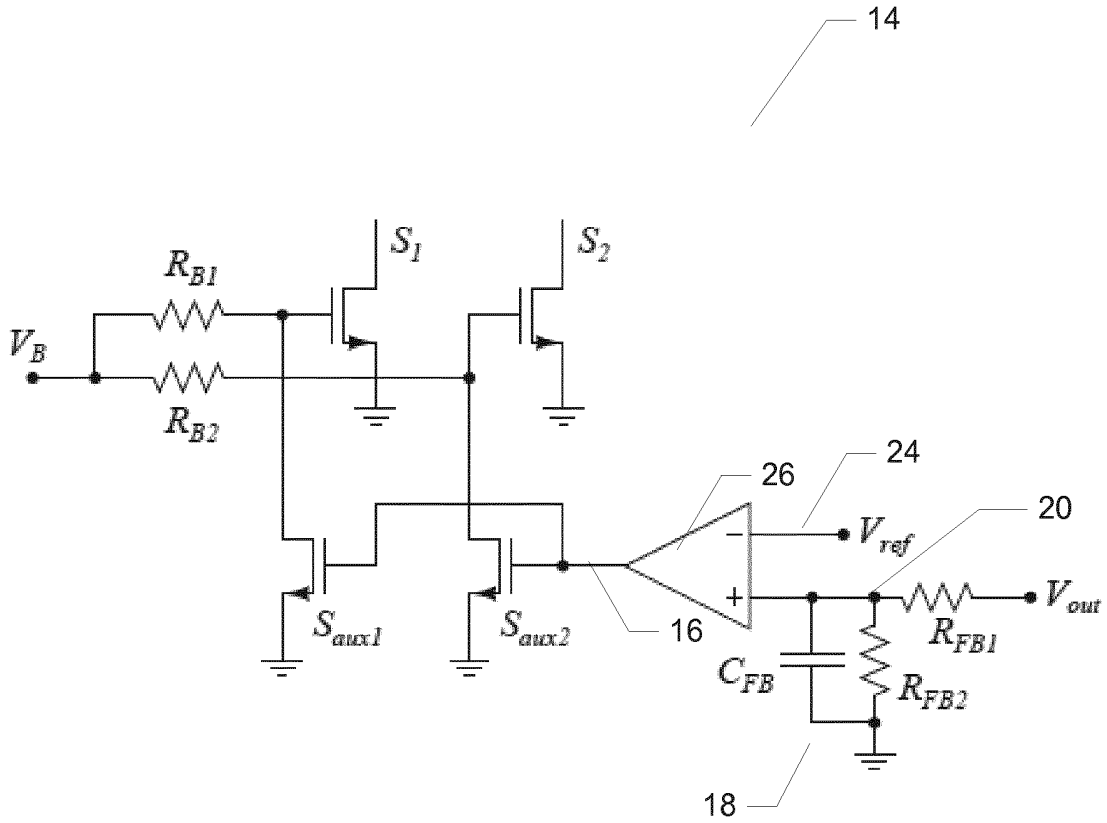

14
S_1
S_2
R_{B1}
V_B
R_{B2}
26
24
20
V_{ref}
V_{out}
S_{aux1}
S_{aux2}
16
R_{FB1}
C_{FB}
R_{FB2}
18

Fig. 13

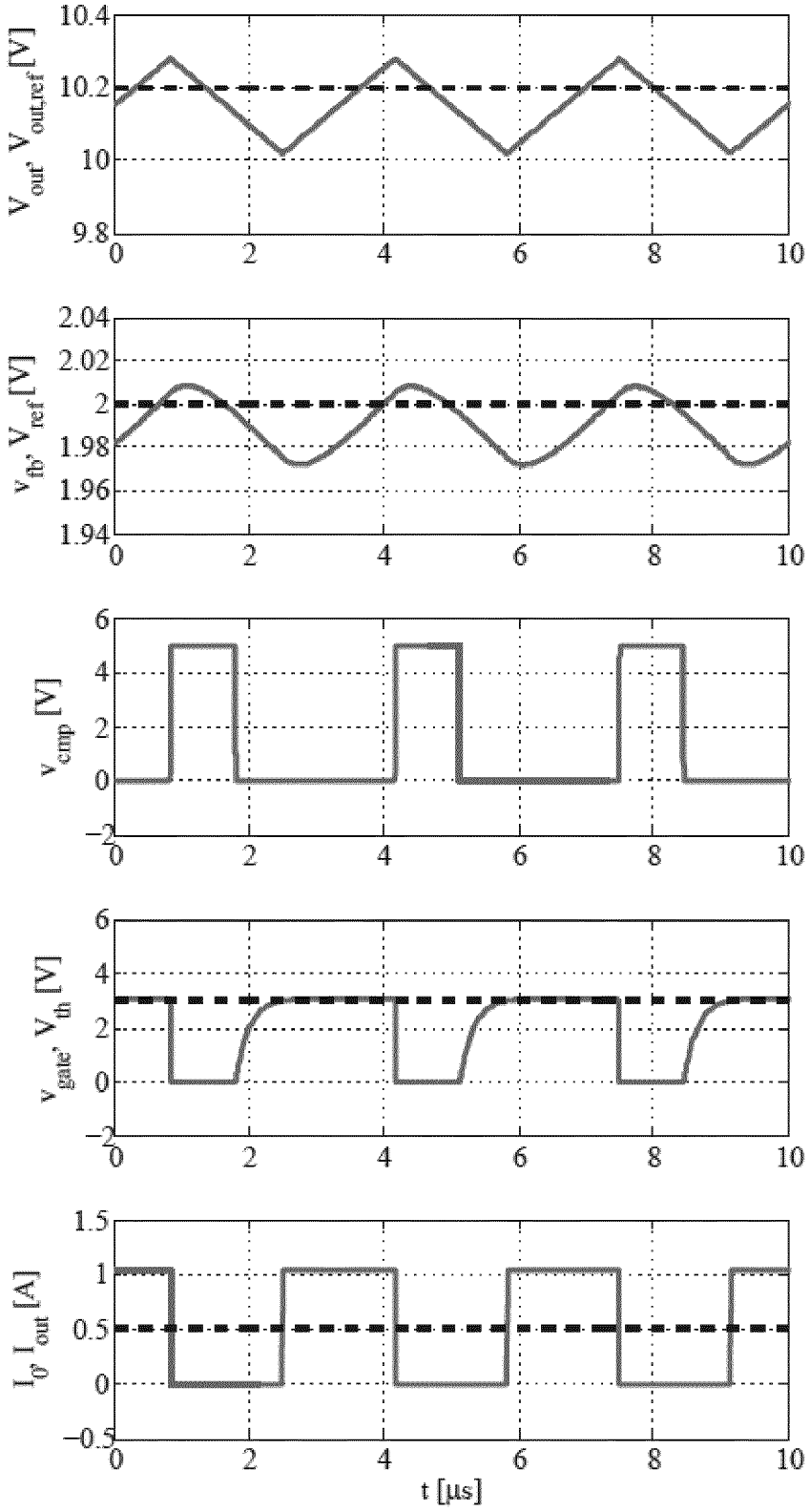
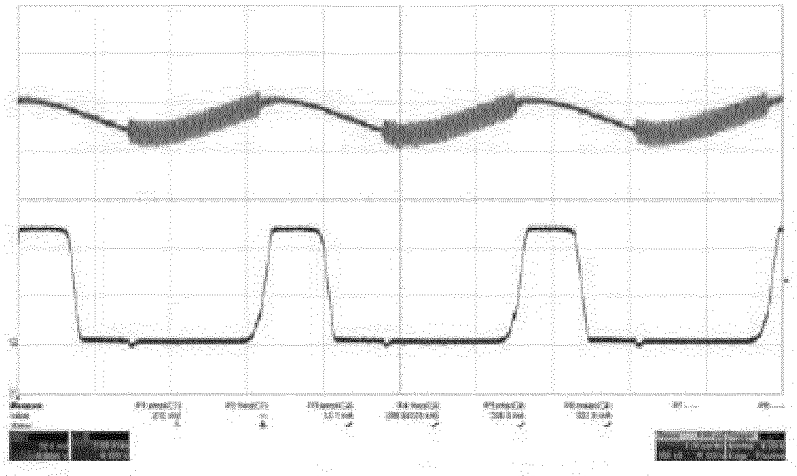
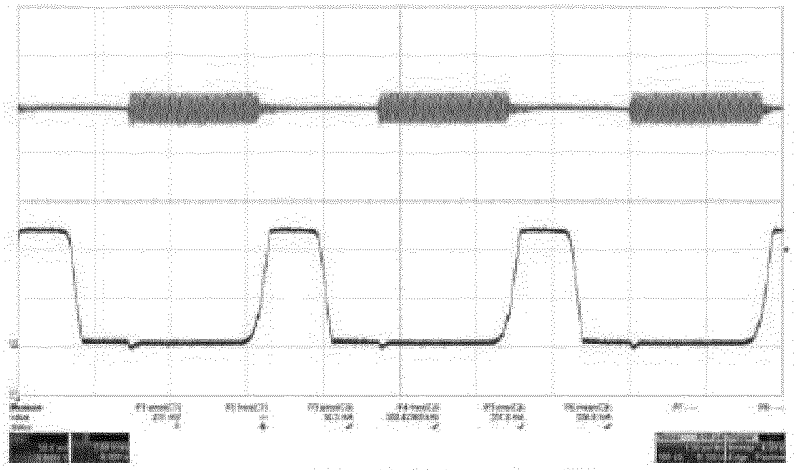

V_{out}, $V_{out,ref}$ [V]
10.4
10.2
10
9.8
v_{fb}, V_{ref} [V]
2.04
2.02
2
1.98
1.96
1.94
v_{cmp} [V]
v_{gate}, V_{th} [V]
I_0, I_{out} [A]
1.5
1
0.5
0
−0.5
0
2
4
6
8
10
t [µs]

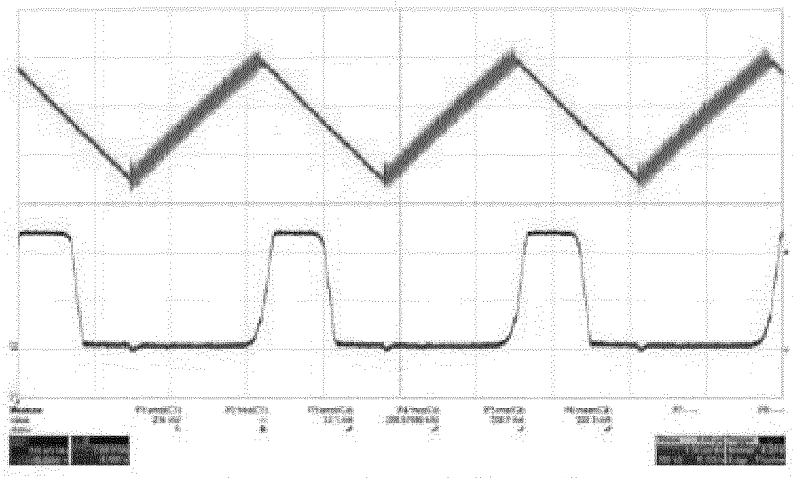
Fig. 14



(a) $v_{cmp+}(t)$: 50 mV/div, 1 µs/div

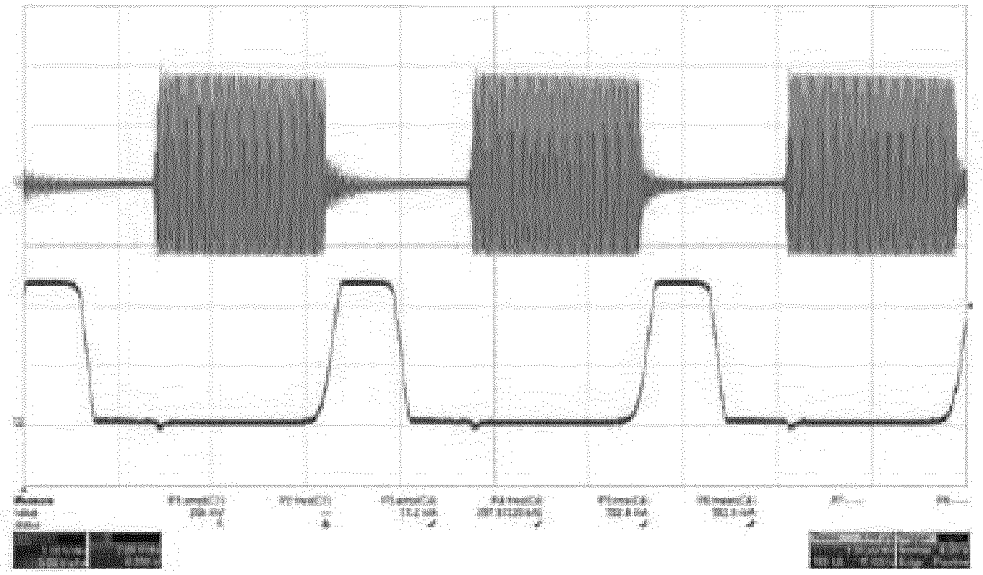


(b) $v_{cmp-}(t)$: 50 mV/div, 1 µs/div

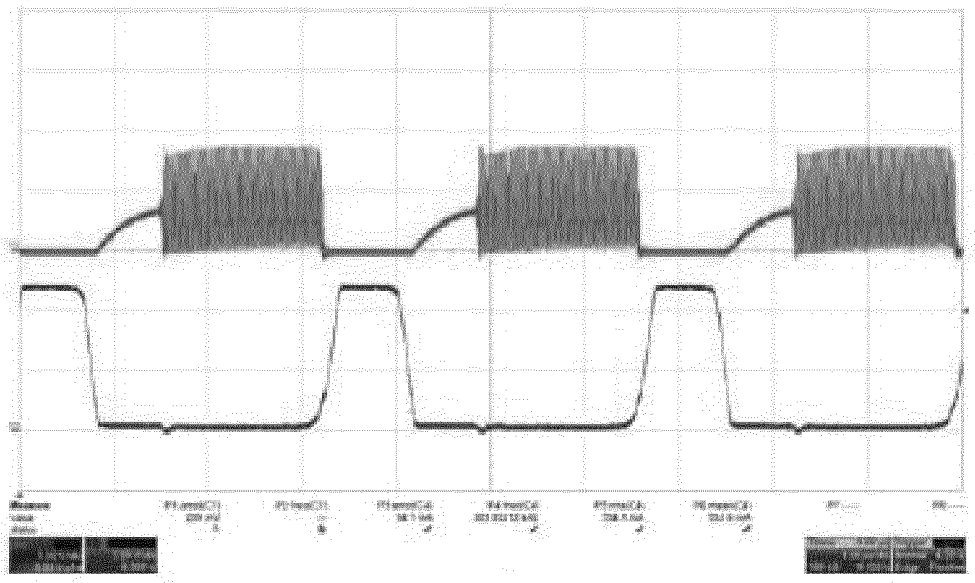


(c) $v_{out}(t)$: 100 mV/div, 1 µs/div

Fig. 15

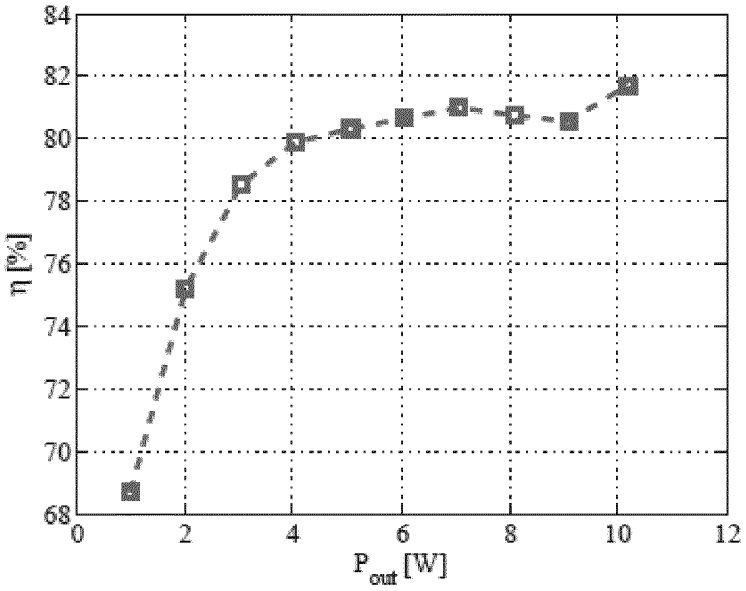


(a) $A\ v_{DS,AC}(t)$ (scaled, no DC): 5 V/div, 1 µs/div

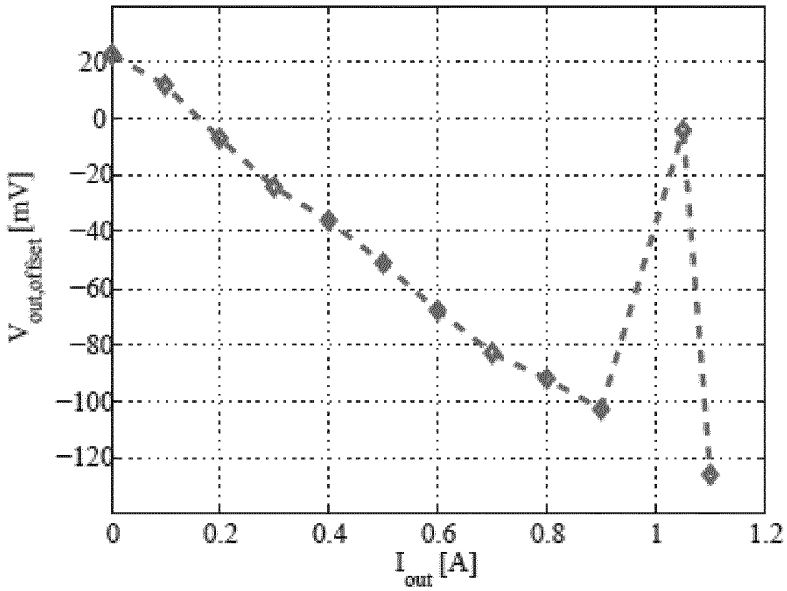


(b) $v_{GS}(t)$: 5 V/div, 1 µs/div

Fig. 16


84
82
80
78
76
74
72
70
68
η [%]
0
2
4
6
8
10
12
P out [W]

(a)


20
0
−20
−40
−60
−80
−100
−120
V out,offset [mV]
0
0.2
0.4
0.6
0.8
1
1.2
I out [A]

(b)

Fig. 17

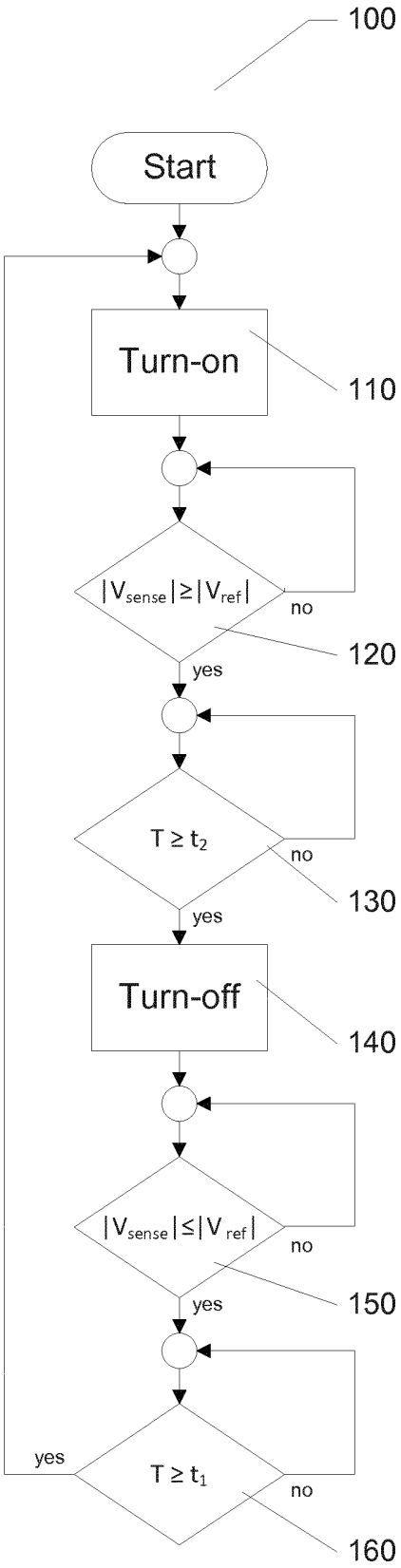
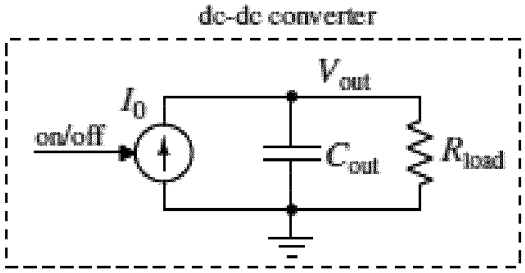
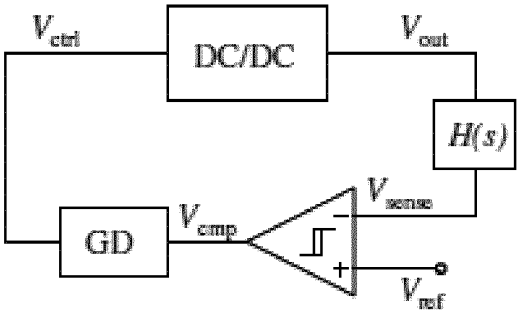

100
Start
Turn-on
110
|Vsense| ≥ |Vref|
no
120
yes
T ≥ t2
no
130
yes
Turn-off
140
|Vsense| ≤ |Vref|
no
150
yes
T ≥ t1
yes
no
160

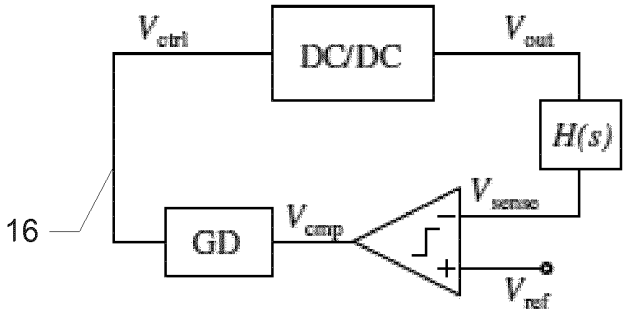
Fig. 18


dc-dc converter
V_{out}
I_0
on/off
C_{out}
R_{load}

(a)


V_{ctrl}
DC/DC
V_{out}
$H(s)$
V_{sense}
GD
V_{cmp}
V_{ref}

(b)


V_{ctrl}
DC/DC
V_{out}
$H(s)$
V_{sense}
16
GD
V_{cmp}
V_{ref}

(c)

Fig. 19

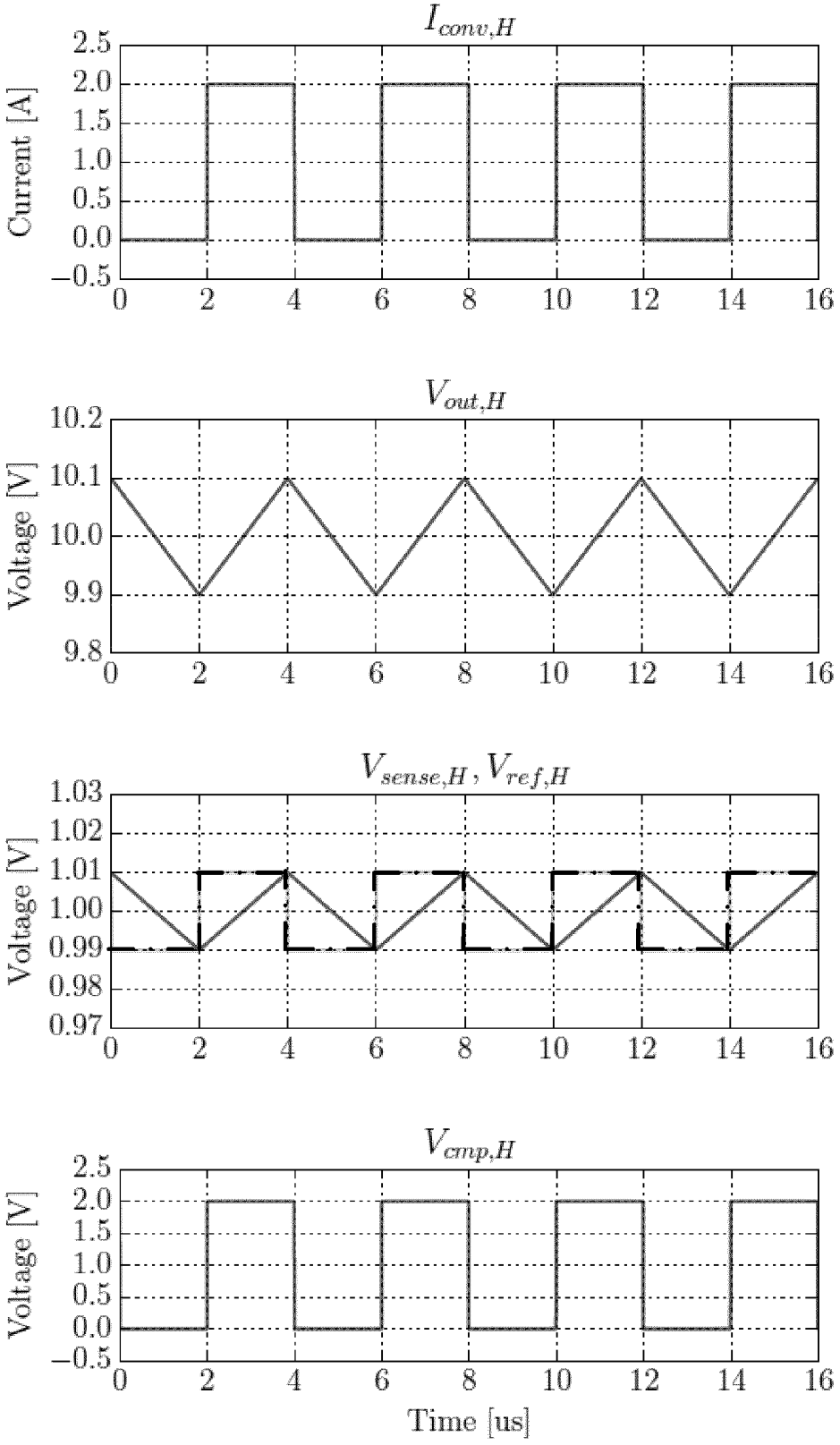

$I_{conv,H}$
Current [A]
2.5
2.0
1.5
1.0
0.5
0.0
−0.5
0
2
4
6
8
10
12
14
16
$V_{out,H}$
Voltage [V]
10.2
10.1
10.0
9.9
9.8
$V_{sense,H}$, $V_{ref,H}$
1.03
1.02
1.01
1.00
0.99
0.98
0.97
$V_{cmp,H}$
Time [us]

Fig. 20

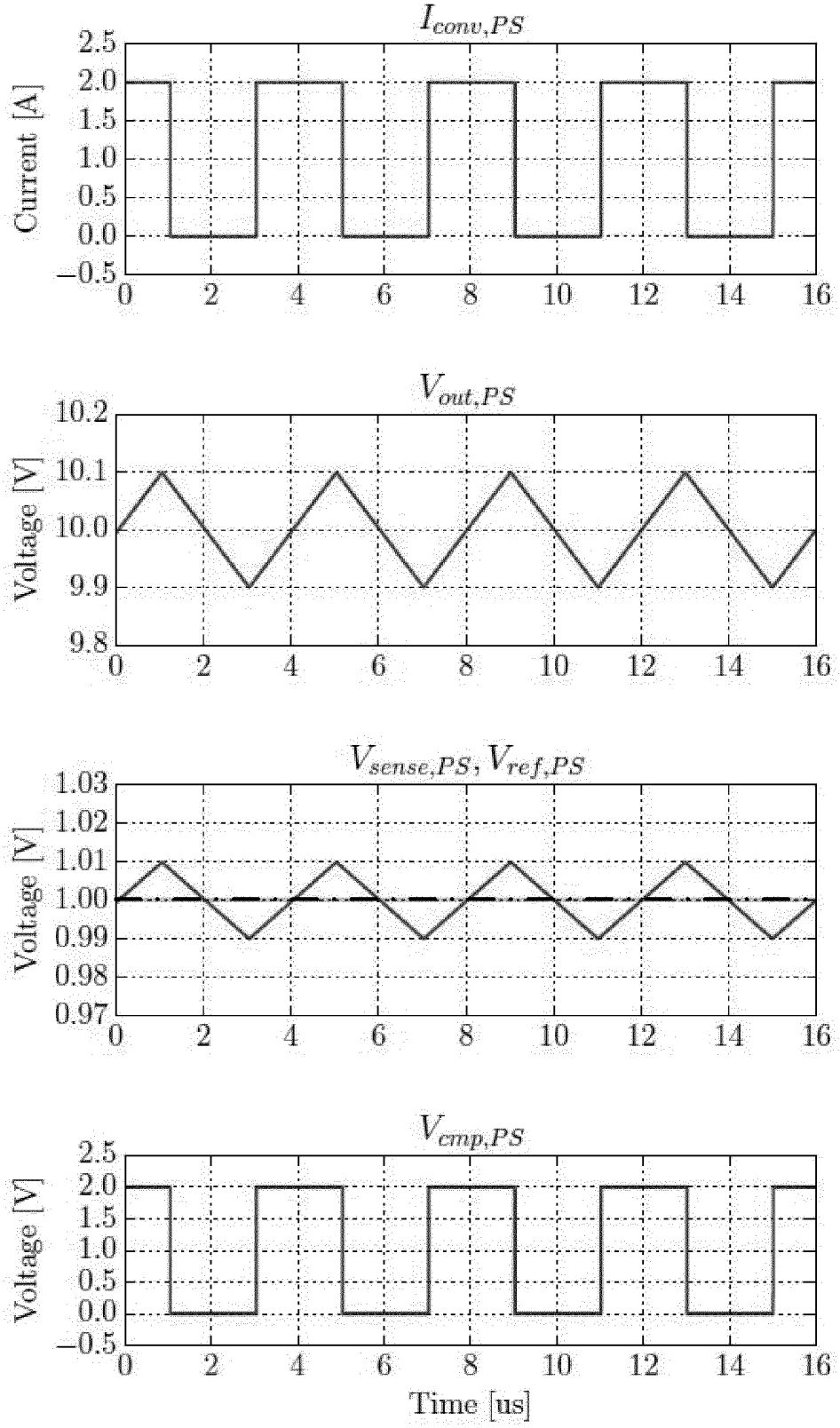
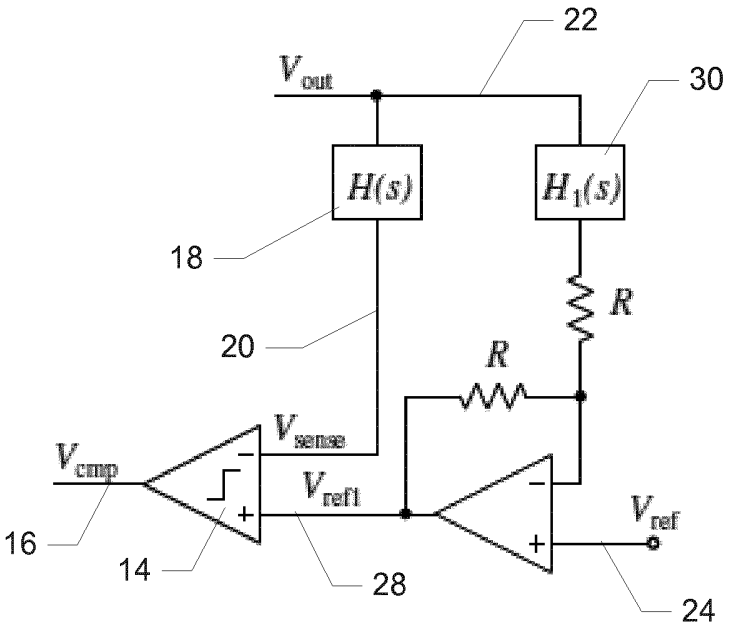
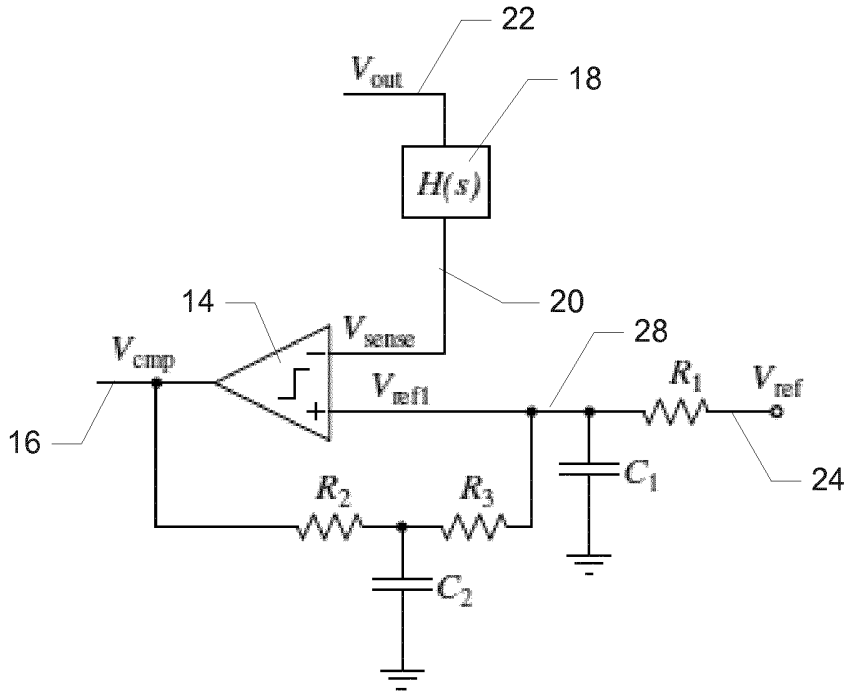

$I_{conv,PS}$
Current [A]
2.5
2.0
1.5
1.0
0.5
0.0
−0.5
0
2
4
6
8
10
12
14
16
$V_{out,PS}$
Voltage [V]
10.2
10.1
10.0
9.9
9.8
$V_{sense,PS}, V_{ref,PS}$
1.03
1.02
1.01
1.00
0.99
0.98
0.97
$V_{cmp,PS}$
Time [us]

Fig. 21

22/22



(a)



(b)

Fig. 22

A.21 M. Madsen and M. Kovacevik: *"On and Off Controlled Resonant dc-dc Power Converter"*, WO2015128397 A1, September 3rd 2015

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Published:

— *with international search report (Art. 21(3))*

(54) **Title**: ON AND OFF CONTROLLED RESONANT DC-DC POWER CONVERTER

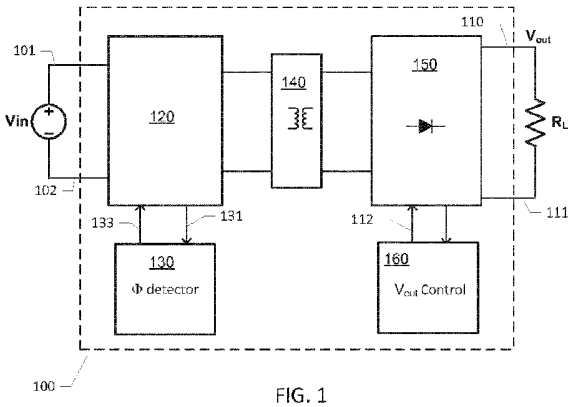


FIG. 1

(57) **Abstract**: The present invention relates to a resonant DC-DC power converter comprising an input side circuit comprising a positive and a negative input terminal for receipt of an input voltage or current and an output side circuit comprising positive and negative output terminals for supply of a converter output voltage and connection to a converter load. The resonant DC-DC power converter further comprises a rectification circuit connected between an output of a resonant network and the output side circuit. The resonant network is configured for alternatingly being charged from the input voltage or current and discharged through the rectification circuit by a first controllable switch arrangement in accordance with a first switch control signal. A second controllable switch arrangement of the resonant DC-DC power converter is configured to select a first impedance characteristic of the resonant network in a first switch state and select a second impedance characteristic of the resonant network in a second switch state. An output voltage or current control circuit is configured to adjust the converter output voltage and/or current by activating and interrupting the first switch control signal in accordance with the switch state of the second controllable switch arrangement.

WO 2015/128397 A1

ON AND OFF CONTROLLED RESONANT DC-DC POWER CONVERTER

The present invention relates to a resonant DC-DC power converter comprising an input side circuit comprising a positive and a negative input terminal for receipt of an input voltage or current and an output side circuit comprising positive and negative output terminals for supply of a converter output power, voltage or current and connection to a converter load. The resonant DC-DC power converter further comprises a rectification circuit connected between an output of a resonant network and the output side circuit. The resonant network is configured for alternatingly being charged from the input voltage or current and discharged through the rectification circuit by a first controllable switch arrangement in accordance with a first switch control signal. A second controllable switch arrangement of the resonant DC-DC power converter is configured to select a first impedance characteristic of the resonant network in a first switch state and select a second impedance characteristic of the resonant network in a second switch state. An output voltage or current control circuit is configured to adjust the converter output voltage and/or current by activating and interrupting the first switch control signal in accordance with the switch state of the second controllable switch arrangement.

BACKGROUND OF THE INVENTION

Power density and component costs are key performance metrics of both isolated and non-isolated DC-DC power converters to provide the smallest possible physical size and/or lowest costs for a given output power requirement or specification. Resonant power converters are particularly useful for high switching frequencies such as frequencies above 1 MHz where switching losses of standard SMPS topologies (Buck, Boost etc.) tend to be unacceptable for conversion efficiency reasons. High switching frequencies are generally desirable because of the resulting decrease of the electrical and physical size of circuit components of the power converter like inductors and capacitors. The smaller components allow increase of the power density of the DC-DC power converter. In a resonant power converter an input "chopper" semiconductor switch (often MOSFET or IGBT) of the standard SMPS is replaced with a "resonant" semiconductor switch. The resonant semiconductor switch relies on resonances of a resonant network typically involving various circuit capacitances and inductances to shape the waveform of either the current or the voltage across the semiconductor switch such that, when state switching takes place, there

is no current through or no voltage across the semiconductor switch. Hence power dissipation is largely eliminated in at least some of the intrinsic capacitances or inductances of the input semiconductor switch such that a dramatic increase of the switching frequency into the VHF range becomes feasible for example to values above 30 MHz. This concept is known in the art under designations like zero voltage and/or zero current switching (ZVS and/or ZCS) operation. Commonly used switched mode power converters operating under ZVS and/or ZCS are often described as class E, class F or class DE inverters or power converters.

However, it remains a significant challenge to adjust or control the output power/voltage/current of resonant DC-DC power converters in an efficient way. If the resonant power converter is controlled by Pulse Width Modulation (PWM) of the "resonant" semiconductor switch, the ZVS ability is lost and power conversion efficiency will drop significantly. Varying the switching frequency of the resonant power converter has also been applied in prior art power converters to control the output voltage/current of the resonant power converter, but this control methodology suffers from a limited range of output voltage regulation and increasing power conversion losses. Controlling the output voltage/current of the resonant power converter by a control scheme which is a combination of variable switching frequency and PWM has also been applied in existing resonant power converters and generally proved to work well. This control methodology or scheme unfortunately leads to highly complex control circuitry.

Another more simple yet efficient way of controlling or adjusting the output power/voltage/current of resonant DC-DC power converters has been to turn on and off the entire resonant power converter in an intermittent manner. This control scheme is designated “burst mode control” or “on/off control”. Burst mode control allows the resonant power converter to operate at a fixed switching frequency where the conversion efficiency is high or optimal during on or activate time periods. During time periods where the power converter is off or deactivated, power losses are essentially eliminated because of the lack of switching activity of the resonant transistor which drives the resonant power converter. Ideally burst mode control of resonant power converter leads to full load regulation and constant efficiency from zero to full load on the converter.

On/off control of prior art resonant power converters has been achieved by controlling the signal voltage on the control terminal of a "resonant" semiconductor switch, e.g. a MOSFET gate terminal. This scheme may work in a satisfactory manner in some applications, but in order to regulate or adjust the converter output voltage and current a feedback control signal from the output/secondary side of the converter to the control terminal of the resonant" semiconductor switch is required. This presents a significant problem in isolated resonant power converters because the feedback control signal must cross a galvanic isolation barrier between the primary side circuitry and the secondary side circuitry. Traditionally, to maintain the galvanic isolation between input side circuitry and output side circuitry of the resonant power converter, the control signal to the resonant semiconductor switch has been transmitted through a relatively slow and expensive optocoupler or through a bulky and slow transformer. The time delay through the optocoupler or transformer presents, however, a serious obstacle to on/off control of resonant power converters where a fast transient response is highly desirable to provide adequate control of the converter output voltage and current. The time delay problem is particularly pronounced for high frequency resonant power converters operating with switching frequencies at or above 20 MHz.

TSO-SHENG CHAN ET AL: "A Primary Side Control Method for Wireless Energy Transmission System", IEEE Transactions on Circuits and Systems i: regular papers, IEEE, Vol. 59, No. 8 discloses a wireless energy transmission system (WETS) transferring power from a primary side circuit to a secondary side circuit through a skin barrier. The IEEE paper discloses a resonant class E based DC-DC power converter with an inductive power transformer connecting the input side circuit and output side circuit through the skin barrier. A charging protection circuit comprise a controllable secondary side switch (Ms) which selectively connects and disconnects a battery (Vb) load from the output of the power converter. A primary side controller operates by detecting variations of the input current and phase of the input reactance to determine the state of the secondary side switch (Ms). The proposed range of switching frequencies of the class E based DC-DC power converter is between 83-175 kHz.

In view of these problems and challenges associated with prior art resonant power converters, it would be advantageous to provide a novel control mechanism for on/off control of resonant power converter eliminating the need to transmit the feedback control signal from an output voltage control circuit across a galvanic isolation barrier to the control terminal of the resonant semiconductor switch. The elimination of the feedback control signal would also be advantageous in non-isolated resonant power converters because of the time delay and occupation of board or carrier area associated with wiring of the feedback control signal to the resonant transistor.

In view of the above, it remains a challenge to reduce the size and lower component costs of both isolated and non-isolated resonant DC-DC power converters. It also remains a challenge to provide an output voltage control mechanism with fast transient response to provide good regulation of the converter output voltage even for high frequency resonant power converters. Hence, a novel control mechanism for resonant power converters which simplifies the control of the converter output voltage and reduces the number of electronic components required to perform the output voltage regulation is highly desirable.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a resonant DC-DC power converter comprising an input side circuit comprising a positive and a negative input terminal for receipt of an input voltage or current and an output side circuit comprising positive and negative output terminals for supply of a converter output power, voltage or current and connection to a converter load. The resonant DC-DC power converter further comprises a rectification circuit connected between an output of a resonant network and the output side circuit. The resonant network is configured for alternatingly being charged from the input voltage or current and discharged through the rectification circuit by a first controllable switch arrangement in accordance with a first switch control signal, wherein a frequency of the switch control signal lies at or above 20 MHz, more preferably at or above 30 MHz. A second controllable switch arrangement of the resonant DC-DC power converter is configured to select a first impedance characteristic of the resonant network in a first switch state and select a second impedance characteristic of the resonant network in a second switch state. An output voltage or current control circuit is configured to adjust or regulate the con-

verter output voltage and/or current by activating and interrupting the first switch control signal in accordance with a switch state of the second controllable switch arrangement.

The first and second impedance characteristics of the resonant network may exhibit different resonance frequencies and/or different Q values at the resonance frequency as explained in additional detail below. A switching frequency of the first switch control signal is preferably located approximately at the resonance frequency of the resonant network when the resonant DC-DC power converter is operational or turned on to ensure high power conversion efficiency.

The output voltage and/or current control circuit is capable of regulating the converter output voltage or current by controlling the state, i.e. conducting state or non-conducting state, of the second controllable switch arrangement and thereby turn off or turn on operation of the present resonant DC-DC power converter. Since the second controllable switch arrangement may conveniently be arranged in the output side circuit of the resonant DC-DC power converter, the output voltage of the converter may be adjusted by a voltage or current control loop arranged entirely on the output side of the converter. Hence, output voltage and/current regulation of isolated variants of the resonant DC-DC power converter can be achieved via control of components placed in the secondary side circuit only. The need of feeding an output control signal, such as an output voltage signal or output current signal, back to the input side or primary side of such isolated resonant DC-DC power converters has been eliminated. As mentioned above, this elimination of the need to transmit a feedback control signal back to the input side or primary side circuit, in particular to the control terminal of the first switch arrangement, is advantageous in both non-isolated and isolated variants of the present resonant DC-DC power converters. In connection with the isolated resonant DC-DC power converters, the elimination of the feedback control signal to the first switch arrangement of the input side circuit removes the need for expensive, bulky and costly isolation devices such as opto-couplers or transformers to transmit the feedback control signal across the galvanic isolation barrier.

In connection with the non-isolated resonant DC-DC power converters, the ability to carry out the output voltage and/or current regulation in the output side circuit eliminates the time delay and board space occupation associated with the wiring of the feedback control signal to the first switch arrangement of the input side circuit. This improves the transient response of the non-isolated resonant DC-DC power converter so as to provide better regulation of the converter output voltage and/or current to the load. This feature is particularly advantageous for resonant DC-DC power converter operating at VHF switching frequencies at or above 30 MHz where short delay times in turning on and turning off the power converter improves regulation performance.

The second controllable switch arrangement may be inserted at various locations of the output side circuitry of the resonant DC-DC power converter to select between the first and second impedance characteristics of the resonant network. The second controllable switch arrangement is preferably coupled to an output of the resonant network. According to one embodiment, the second controllable switch arrangement is coupled in series between an output of the rectification circuit and the positive or the negative output terminal to connect the converter load in a conducting switch state and disconnect the converter load in a non-conducting switch state. In this manner the positive or negative output terminal and converter load may be electrically disconnected from the residual portion of the resonant DC-DC power converter in the off state of the converter.

The rectification circuit is preferably designed to exhibit substantially resistive impedance at a resonance frequency of the resonant network with the connected converter load. In this situation, the first impedance characteristic, including the resonance frequency, of the resonant network may be determined by one or more interconnected inductors and capacitors of the resonant network with negligible influence from components of the rectification circuit. On the other hand, when the converter load is disconnected from the output of the rectification circuit by the second controllable switch arrangement, the rectification circuit may exhibit a different and non-resistive input impedance which loads the resonant network. This non-resistive loading leads to a change of the impedance characteristics of the resonant network so as to select the second impedance characteristic of the resonant network. This sec-

ond impedance characteristic of the resonant network may exhibit a lower resonance frequency Q value than the Q value at the resonance frequency of the first impedance characteristic. The second impedance characteristic of the resonant network may possess a lower or higher, i.e. different, resonance frequency than the resonance frequency of the first impedance characteristic of the resonant network for example because an inductor and/or a capacitor of the rectification circuit has/have influence on the resonance frequency of the resonant network. These types of differences between the first and second impedance characteristics of the resonant network may be exploited to enable and disable oscillation of a feedback loop around the first controllable switch arrangement as described in further detail below. According to another embodiment, the second controllable switch arrangement is coupled across the output of the resonant network to select the first impedance characteristic of the resonant network in a non-conducing state and the second impedance characteristic of the resonant network in in a conducing state.

In another embodiment, the impedance characteristics of the resonant network are changed from the first impedance characteristic to the second impedance characteristic of the resonant network by connecting one or more auxiliary capacitances and/or connecting one or more auxiliary inductances to existing capacitances and inductances, respectively, of the resonant network by the second controllable switch arrangement.

In a preferred embodiment of the resonant DC-DC power converter, the rectification circuit comprises the second controllable switch arrangement; and a control circuit is configured for generating a control signal for the second controllable switch arrangement synchronously to the first switch control signal. In this embodiment, the respective functions of the rectification circuit and second controllable switch arrangement are integrated. In this manner, the second controllable switch arrangement may, in addition to connecting and disconnecting the converter load, operate as a synchronous full-wave or half-wave rectifier and replace functions of one or more ordinary rectifier diodes of the rectification circuit.

The output voltage or current control circuit of the resonant DC-DC power converter may comprise a self-oscillation feedback loop coupled between an output terminal

and a control terminal of the first controllable switch arrangement. In this embodiment, the first impedance characteristic of the resonant network is configured to enable oscillation of the self-oscillation feedback loop and the second impedance characteristic of the resonant network is configured to disable oscillation of the self-oscillation feedback loop. Hence, the state switching of the second controllable switch arrangement can be used to activate and interrupt the operation of the power converter by enabling and disabling, respectively, the oscillation or switching of the first controllable switch arrangement. The latter may for example comprise a transistor such as a MOSFET where the self-oscillation feedback loop is connected between a drain and gate terminal of the MOSFET. The skilled person will understand that the self-oscillation feedback loop preferably is arranged entirely in the input side circuit of the resonant DC-DC power converter to avoid transmission of feedback signals of the self-oscillation feedback loop from the output side circuit.

The self-oscillation feedback loop may comprise a first intrinsic switch capacitance coupled between the output and control terminals of the first controllable switch arrangement. The self-oscillation feedback loop further comprises a first bias voltage source configured to generate a first adjustable bias voltage and a first inductor, preferably with substantially fixed inductance, coupled in-between the first bias voltage source and the control terminal of the first controllable switch arrangement. The self-oscillation feedback loop may in addition to the first intrinsic switch capacitance include an external capacitor connected between the output and control terminals of the first controllable switch. The skilled person will appreciate that the first intrinsic switch capacitance may comprises a drain-gate capacitance of a MOSFET transistor contained in the first controllable switch arrangement. Several resonant DC-DC power converter designs based on self-oscillation feedback loops around the input side switch arrangement are disclosed in the applicant's co-pending application PCT/EP2013/072548. The skilled person will understand that these self-oscillation feedback loops may be utilized in the present resonant DC-DC power converters.

The first and second impedance characteristics of the resonant network which enable and disable, respectively, the oscillation of the first controllable switch arrangement may differ in various ways. In one embodiment the Q value of the first impedance characteristic is larger than 5 at the resonance frequency of the first imped-

ance characteristic; and the Q factor of the second impedance characteristic is smaller than 2 at the resonance frequency of the second impedance characteristic. In another embodiment the resonance frequency of the first impedance characteristic is at least 1.4 times larger than the resonance frequency of the second impedance characteristic.

In a range of advantageous embodiments of the resonant DC-DC power converter, the frequency of the first switch control signal is placed at or above 20 MHz such as above at or above 30 MHz in the so-called VHF range. In these embodiments, the above-discussed resonance frequency of the first impedance characteristic of the resonant network is situated at or above 20 MHz, or at or above 30 MHz. The resonance frequency of the first impedance characteristic of the resonant network is preferably situated approximately at the frequency of the first switch control signal. The resonant DC-DC power converters preferably facilitate zero voltage and/or zero current switching of the semiconductor switch or switches driving or exciting the resonant network.

The output voltage or current control circuit may comprise a regulation loop, e.g. a voltage, current or power regulation loop, connected between the converter output voltage/current and a control terminal of the second controllable switch arrangement to adjust the converter output voltage and/or current in accordance with one or more DC reference voltage(s) or current(s). The voltage or current regulation loop may for example comprise a DC reference voltage generator configured to supply the one or more DC reference voltage(s),
one or more comparator(s) configured for comparing the converter output voltage to at least a first DC reference voltage and select the conducting state or the non-conducting state of the second controllable switch arrangement depending on a result of the comparison.

In this embodiment, the voltage regulation loop may use a single DC reference voltage to adjust the converter output voltage. The resonant DC-DC power converter may be turned off when the converter output voltage exceeds the single DC reference voltage by selecting an appropriate state of the second controllable switch arrangement. Likewise, the DC-DC power converter may be turned on when the con-

verter output voltage is smaller than the single DC reference voltage by selecting the opposite state of the second controllable switch arrangement.

In an alternative embodiment of the resonant DC-DC power converter the voltage or current regulation loop comprises at least two different DC reference voltages or currents which are utilized as references for controlling output regulation. In this embodiment, the DC reference voltage generator is configured to supply at first DC reference voltage and a second DC reference voltage where the first DC reference voltage is higher than the second DC reference voltage; The one or more comparator(s) is configured to:
comparing the converter output voltage to the first and second DC reference voltages; and
selecting one of the conducting and non-conducting states of the second controllable switch arrangement in response to the converter output voltage exceeding the first DC reference voltage,
selecting the opposite state of the second controllable switch arrangement in response to the converter output voltage falls below the second DC reference voltage.

As previously mentioned, the resonant DC-DC power converter may comprise a galvanic isolation barrier. The galvanic isolation barrier is preferably arranged between the input side circuit and the output side circuit to provide galvanic isolation between the converter output voltage and the input side circuit. This galvanic isolation barrier may comprise a pair of magnetically coupled inductors comprising a first inductor electrically connected to the input side circuit and a second inductor electrically connected to the input of the rectification circuit. The pair of magnetically coupled inductors may comprise a transformer. In another embodiment, the galvanic isolation barrier comprises first and second coupling capacitors. The first coupling capacitor may be arranged in a signal carrying line of the resonant power converter for example in series between the output of the resonant network and the rectification circuit. The second coupling capacitor may be arranged in a negative voltage wire or ground wire of the resonant power converter between the input and output side circuits. The coupling capacitor based galvanic isolation barrier is particularly useful in resonant DC-DC power converters operating at or above 20 MHz because of the relatively small capacitances required of the first and second capacitors at

such high frequencies. The small capacitance allows each of the first and second capacitors to be physically small and be implemented as non-electrolytic SMD capacitors for example ceramic capacitors with a capacitance below 100 nF.

The skilled person will understand that all resonant DC-DC power converter topologies may be used in the present invention for example SEPIC, class E, class F, class DE or converter topologies derived from these. Several exemplary isolated and non-isolated resonant DC-DC power converters of Class E topology are described in detail below in connection with the appended drawings.

The first controllable switch arrangement may comprise one or more semiconductor switches and the second controllable switch arrangement may comprise one or more semiconductor switches. Each of the semiconductor switches of the first and second controllable switch arrangements may comprise a semiconductor transistor such as a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET. The control terminals or terminals of the first controllable switch arrangement may accordingly comprise gate terminal(s) or base terminal(s) of the one or more semiconductor switches. The control terminal of each of the semiconductor switches may be driven by the first switch control signal to alternatingly force the semiconductor switches between on-states and off-states. The control terminals or terminals of the second controllable switch arrangement may comprise gate terminal(s) or base terminal(s) of the one or more semiconductor switches.

One embodiment of the resonant DC-DC power converter comprises a wireless data receiver for receipt of remote data commands to control the switch state of the second controllable switch arrangement. The remote data command may be used to interrupt or activate operation of the resonant DC-DC power converter by commands received via a wireless home automation network. The remote data command may be inputted to the output voltage or current control circuit that controls the state switching of the second controllable switch arrangement. In this manner, the resonant DC-DC power converter can be switched ON or OFF or regulated via remote control. The wireless data receiver may be compliant with various industry standard wireless data communication protocols such as the ZigBee communication protocols or wired data communication protocols such as the Digital Addressable Lighting Interface (DALI) and protocol.

The skilled person will appreciate that the first controllable switch arrangement may be formed by a single transistor, for example a NMOS device, or several interconnected transistors depending on the selected topology of the resonant DC-DC power converter. In some embodiments, the first controllable switch arrangement may comprise a half-bridge switch topology or a full-bridge switch topology.

The galvanic isolation barrier may comprise a transformer which comprises a pair of magnetically coupled inductors comprising a first inductor electrically connected to the primary side circuit and a second inductor electrically connected to the output side circuit. The first and second inductors could be discrete windings both wound around a common magnetic permeable structure to form an isolation transformer. In an alternative embodiment, the first and second inductors are integrated in a printed circuit board without intervening magnetic material. The printed circuit board could have the entire DC-DC power converter mounted thereon.

One embodiment of the resonant DC-DC power converter is arranged on a single substantially flat carrier substrate to form a compact, low cost and single unit power converter assembly that is well-suited for integration in various kind of consumer equipment such as LED lamps and battery chargers. The latter embodiment of the resonant DC-DC power converter comprises a single substantially flat carrier substrate comprising a first surface and a second, opposing, surface, wherein the input side circuit, the output side circuit, the rectification circuit, the resonant network, the first controllable switch arrangement, the second controllable switch arrangement and the output voltage or current control circuit are arranged on the first surface and/or the second surface. The flat carrier substrate may comprise a single sided or double-sided printed circuit board, which may comprise additional layers between a top layer comprising the first surface and a bottom layer comprising the second surface. The skilled person will appreciate that respective passive and active electronic components of the input side circuit, the output side circuit, the rectification circuit, the resonant network, the first controllable switch arrangement, the second controllable switch arrangement and the output voltage or current control circuit may be attached to the upper and/lower carrier surfaces by soldering or gluing.

A second aspect of the invention relates to a method of operating a resonant DC-DC power converter to generate a converter output voltage or current, said method comprising steps of:

a) alternatingly charging and discharging a resonant network of the resonant converter from an input voltage or current source by a first controllable switch arrangement in accordance with a first switch control signal,

b) rectifying a resonant current of the resonant network,

c) discharging a rectified resonant current to a rectification circuit to produce a rectified output voltage,

d) switching between a first impedance characteristic or a second impedance characteristic of the resonant network by selecting a first or a second switch state of a second controllable switch arrangement,

e) adjusting a converter output voltage or current by alternatingly activating and interrupting the first switch control signal in accordance with first and second switch states of the second controllable switch arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention will be described in more detail in connection with the appended drawings, in which:

FIG. 1 is a top-level schematic block diagram of resonant DC-DC power converters in accordance with preferred embodiments of the invention,

FIG. 1A) is a schematic block diagram of a power converter assembly comprising resonant DC-DC power converters in accordance with preferred embodiments of the invention,

FIG. 2 is a simplified electrical circuit diagram of an isolated class E type of DC-DC power converter in accordance with a first embodiment of the invention,

FIG. 3 is a simplified electrical circuit diagram of isolated class E type of DC-DC power converter in accordance with a second embodiment of the invention,

FIG. 4 is a simplified electrical circuit diagram of a self-oscillating isolated class E DC-DC power converter in accordance with a third embodiment of the invention; and

FIG. 5 is a simplified electrical circuit diagram of a non-isolated class E DC-DC power converter in accordance with a fourth embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1 shows a simplified schematic block diagram of a resonant DC-DC power converter 100 in accordance with preferred embodiments of the present invention. Detailed schematic circuit diagrams of exemplary embodiments of the present resonant DC-DC power converters are described below with reference to FIGS. 2, 3, 4 and 5. The resonant DC-DC power converter 100 comprises an input block 120 and an output block 150 connected through an optional galvanic isolation barrier 140. The galvanic isolation barrier 140 may comprise various types of electrical insulation elements or components such as a pair coupling capacitors or a pair of magnetically coupled inductors such as a transformer. The input block 120 comprises an input side circuit which comprises a positive input terminal 101 and a negative input terminal 102 for receipt of a DC or AC input voltage V_{in} from a voltage or power source. The input side circuit may comprise an input capacitor (not shown) electrically connected between the positive and negative input terminals 101, 102 to form an energy reservoir for the input voltage source and suppress ac ripple voltage components and/or noise components of the DC or AC input voltage V_{in}. The output block 150 comprises an output side circuit comprising positive and negative output terminals 110, 111, respectively, for supplying a converter DC output voltage V_{out} and connection to a converter load. The converter load is schematically represented by load resistor R_L. The output block 150 further comprise a rectification circuit, schematically represented by the diode symbol, connected between an output of a resonant network (not shown) of the resonant DC-DC power converter 100 and the output side circuit. The input block 120 comprises a first controllable switch arrangement, comprising at least one controllable semiconductor switch, operable in accordance with a switch control signal. The controllable semiconductor switch or switches may comprise a transistor such as a BJT, MOSFET or IGBT where the base or gate terminal(s) are coupled to the switch control signal. The controllable switch arrangement is coupled to the resonant network such that the latter is alternatingly charged from the DC or AC input voltage and discharged the rectification circuit to produce the DC output voltage V_{out}. A frequency of the switch control signal of the first controllable switch arrangement accordingly sets the switching frequency of the resonant DC-DC power converter 100. The resonant network may be exclusively arranged in the input block 120 in some embodiments of the invention while the resonant network in other embodiments may include certain passive components of the

galvanic isolation barrier 140 and/or rectification circuit. The resonant network preferably comprises at least one capacitor and at least one inductance connected to each other. The resonant DC-DC power converter 100 further comprises an output voltage or current control circuit 160 which is configured to adjust the DC output voltage V_{out} by activating and interrupting the previously discussed switch control signal of the first controllable switch arrangement in accordance with a switch state of a second controllable switch arrangement (not shown). The switch state of a second controllable switch arrangement is controlled via control line or wire 112 which may be connected to a suitable control terminal of the second controllable switch arrangement as discussed in additional detail below. When the switch control signal of the first controllable switch arrangement is interrupted or stopped, i.e. not switching, the resonant network is no longer charged or excited and the DC output voltage V_{out} gradually decreases due to the current drawn by the converter load. When the switch control signal of the first controllable switch arrangement is activated the resonant network is again charged or excited by the first controllable switch arrangement and supplies resonant current to the rectification circuit and output side circuit such that the DC output voltage V_{out} gradually increases.

Different types of control mechanisms are utilized in different embodiments of the present resonant DC-DC power converter to control the activation and interruption of the switch control signal of the first controllable switch arrangement. In one embodiment, the second controllable switch arrangement is configured to connect and disconnect the converter load R_L such that impedance characteristics of the resonant network are altered. In another embodiment, the impedance characteristics of the resonant network are changed by switching the second controllable switch arrangement between a conducting state and a non-conducting state for example adding one or more auxiliary capacitances or inductances to the resonant network. This change of the impedance characteristics of the resonant network may in certain embodiments be detected by a resonant phase detector 130. The resonant phase detector 130 may be configured to monitor, via monitor line of signal 131, a resonant voltage and a resonant current of the resonant network. The resonant phase detector 130 may configured to measure a change of phase or amplitude between the resonant current and resonant voltage at a nominal resonance frequency of the network caused by the change of the impedance characteristics of the resonant

network caused by the state switching of the second controllable switch arrangement.

The resonant phase detector 130 may generate the switch control signal for the first switch arrangement and supply this control signal 133 to the control terminal or terminals of the resonant network such as a base or gate terminal as discussed above. In one advantageous embodiment of the present resonant DC-DC power converter 100, the resonant phase detector 130 is integrated into a self-oscillation feedback loop formed around the first controllable switch arrangement. In this manner, oscillation of the self-oscillation feedback loop is either enabled or disabled according to the switch state of the second controllable switch arrangement as discussed in additional detail below with reference to FIGS. 4 & 5.

FIG. 1A) illustrates schematically how the resonant DC-DC power converters 100 in accordance with preferred embodiments of the present invention may be arranged on a single substantially flat carrier substrate 180 such as a printed circuit board (PCB). The resonant DC-DC power converter mounted on such a single carrier substrate 180 forms a compact, low cost and single unit power converter assembly that is well-suited for integration in various kind of consumer equipment such as LED lamps and battery chargers. Furthermore, the mounting of the input block 120, the galvanic isolation barrier 140 and the output block 150 on a common carrier substrate allows high power conversion efficiency because the input and output side circuits of the resonant DC-DC power converter are placed proximate to each other. The single substantially flat carrier substrate 180 may comprise an upper or first surface 182 and a second, opposing, surface (not shown). The skilled person will appreciate that passive and active electronic components of the resonant DC-DC power converter embodiment in question may be attached to the upper and/lower carrier surfaces for example by soldering or gluing. These passive and active electronic components may comprise the respective semiconductor switches, capacitors, inductors, terminals, comparators etc. of the resonant DC-DC power converter embodiments 200, 300, 400 and 500 discussed in detail below and illustrated on FIGS. 2, 3, 4 and 5. Likewise, suitable electrical wire traces may be formed on the upper and/lower carrier surfaces of the single flat carrier substrate 180 to interconnect the circuit blocks 120, 130, 140, 150, 160 in a desired manner. The upper or

under surface 182 of the substantially flat carrier substrate 180 also comprises the positive input terminal 101 and the negative input terminal 102 for receipt of the DC or AC input voltage V_{in} from the voltage or power source of the converter. The upper or under surface 182 of the substantially flat carrier substrate 180 comprises the positive and negative output terminals 110, 111, respectively, for supplying the DC output voltage V_{out}, together with the accompanying output power and current, generated by converter to the intended load for example LED devices of a LED lamp.

The resonant DC-DC power converters 100 in accordance with preferred embodiments of the present invention may comprise an optional wireless or wired data receiver 190 for receipt of remote data commands to the output voltage or current control circuit 160. The remote data command may be used to interrupt, activate or adjust operation of the resonant DC-DC power converter via the output voltage or current control circuit 160. The remote data command may be subjected to a logical OR operation with the switch control signal otherwise provided by the output voltage or current control circuit 160 via signal wire or line 112. In this manner, the resonant DC-DC power converter can be switched ON or OFF or regulated via remote control and be integrated with a wireless or wired home automation network. The optional data receiver 190 may be compliant with various industry standard wireless data communication protocols such as the ZigBee communication protocols or wired data communication protocols such as the Digital Addressable Lighting Interface (DALI) interface and protocol.

FIG. 2 shows an electrical circuit diagram of an isolated class E DC-DC power converter 200. The power converter 200 comprises an input block 220 and an output block 250 connected through an optional galvanic isolation barrier 240 formed by series or coupling capacitors C2 and C3. The input side circuit 220 comprises a positive input terminal 202 and a negative input terminal 201 for receipt of a DC or AC input voltage V_{in} from a voltage or power source. An input capacitor (not shown) may in addition be electrically connected between the positive and negative input terminals 201, 202 to form an energy reservoir for the input voltage source and suppress ac ripple voltage components and/or noise components of the DC or AC input voltage V_{in}. The input side circuit 220 additionally comprises a resonant network as discussed below which is alternatingly charged from the DC or AC input voltage V_{in}

and discharged through a class E rectification circuit 250 by a first controllable switch arrangement S1. The latter comprises a single controllable semiconductor transistor or switch S1 in the present embodiment. The skilled person will understand that the first controllable switch arrangement S1 may comprise a plurality of controllable semiconductor transistors or switches in other embodiments of the invention. The first controllable switch arrangement S1 may for example comprise a half-bridge arrangement with a pair of stacked semiconductor transistors or switches in a corresponding class DE embodiment of the resonant DC-DC power converter. The single controllable semiconductor switch S1 may comprise a transistor such as a MOSFET or IGBT, for example a Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET.

The resonant network comprises at least a first inductor L1, a first capacitor C1, which may be a parasitic capacitance of part of S1, and second inductor L2 and the coupling capacitors C2 and C3 of the galvanic isolation barrier 240. The capacitance of the coupling capacitor C3 may be much larger than the capacitance of C2, e.g. more than 10 times larger, such that the effect of the capacitance of C3 may be neglected in setting of the resonance frequency of the resonant network. The charging and discharging, or excitation, of the resonant network follows the first switch control signal applied to a control or gate terminal 204 of semiconductor switch S1 such that the switch S1 alternates between an conducting/on-state and a non-conducting/off-state at the frequency of the first switch control signal when the resonant power converter 200 is active or ON. The power converter 200 is preferably designed or configured such that a frequency of the first switch control signal is situated in close proximity to the resonance frequency of the resonant network when an on-state or conducting state of a second controllable semiconductor switch S2 is selected as explained in detail below. Hence, the switching frequency of the resonant power converter 200 corresponds to the frequency of the first switch control signal when the converter is ON or active. The state switching of semiconductor switch S1 generates a resonant current in the resonant network flowing from an output of the resonant network through a class E rectification circuit of the output block 250 to produce a rectified DC output voltage V_{out} across a rectification capacitance. The class E rectification circuit comprises inductor L3, rectifier diode D1 and capacitor C4. The skilled person will understand that the inductor L3 and capacitor C4 may influence

the setting of resonance frequency of the resonant network depending on how the converter is dimensioned, However, the influence of the rectification components L3 and C4 may be minimal in power converter embodiments where the rectification circuit is configured to exhibit an essentially resistive input impedance at the resonance frequency of the resonant network when the switch S2 is in its conducting state or on-state. The capacitors C5 and C6 ensure a stable converter output voltage or current.

The output block furthermore comprises a positive and a negative output terminal 210, 211, respectively, which supply the converter DC output voltage V_{out} to a converter load R_L of the class E power converter 200. The converter load is schematically illustrated by load resistor R_L on the drawing, but may in practice include different types of electric loads for example a set of LED diodes or a rechargeable battery etc. The second controllable semiconductor switch S2 is placed in-between a positive output node 209 of the rectification circuit and the converter load R_L. Hence, S2 is placed in series with the converter load such that the latter is disconnected from the class E power converter 200 when switch S2 is switched to its off-state or non-conducting state. In this off-state of S2, the capacitor C6 is electrically isolated from the converter rectification circuit, but may supply power to the converter load momentarily while the DC output voltage of the power converter declines due to current drawn by the converter load R_L. In the opposite situation, where S2 is placed in its on-state or conducting state, the positive output node 209 of the rectification circuit is connected to the converter load R_L and the rectification capacitors C5 and C6 are placed in parallel so as to form a joint output capacitor of the power converter 200. The skilled person will understand that the second controllable semiconductor switch S2 preferably is designed or selected such that its on-resistance is markedly smaller than an equivalent load resistance, e.g. at least 10 times smaller, to minimize the on-state power loss in S2 and a voltage drop across S2.

The second controllable semiconductor switch S2 preferably comprises at least one MOSFET transistor such as a NMOS transistor. The second controllable semiconductor switch S2 may of course be formed by a plurality of parallelly connected individual semiconductor switches such as a plurality of parallelly connected MOSFETs.

The skilled person will understand that the arrangement of the second controllable semiconductor switch S2 operates to connect the converter load R_L to the output of the rectifier in the conducting state of switch S2 and disconnect the converter load R_L from the output node 209 of the rectifier in the non-conducting state of the switch S2. This in effect changes the loading at the output of the resonant network presented by the rectification circuit because the equivalent input impedance of the rectification circuit increases markedly when the converter load R_L is disconnected by the switch S2. This change of loading on the output of the resonant network caused by the state switching of switch S2 changes the impedance response characteristics of the resonant network such that the latter exhibits a second and different impedance response characteristic in the non-conducting state of switch S2 (where the converter load is disconnected). This change of the impedance characteristics over frequency of the resonant network may for example comprise a change of Q value and/or a change of the resonance frequency. The impedance response characteristics of the resonant network may be represented by its impedance characteristics as seen from the output of the switch transistor S1, i.e. the drain terminal of S1 in the present embodiment. The Q of the impedance characteristics of the resonant network may for example change from a value between 5 and 20 in the conducting state of switch S2 down to a value between 0.5 and 2 in the non-conducting state of switch S2. The resonance frequency of the resonant network may for example decrease with a factor somewhere between 1.4 and 3 such as about 1.41 from the conducting state to the non-conducting state of switch S2 for example from about 30 MHz to about 21 MHz. The class E power converter 200 further comprises an output voltage control circuit 260 which is configured to adjust the DC output voltage V_{out} by enabling/activating or disabling/interrupting the first switch control signal on the gate terminal 204 of the first switch S1 in accordance with the selection of the first impedance characteristic or the second impedance characteristic of the resonant network. The output voltage control circuit comprises a comparator 208 and DC reference voltage generator (not shown) supplying a DC reference voltage V_{ref} to a first input of the comparator 208. A comparator output is connected to a gate terminal 212 of the switch S2 to such that the comparator output selects one of the conducting state and non-conducting state of the switch S2 depending on the logic level of the comparator output. The control mechanism of the output voltage control circuit, which enables or disables the gate control signal on

the switch S1, may respond to the selected impedance characteristics of the resonant network, as controlled by the state of switch S2, via different control and detection mechanisms. In one embodiment, a resonant phase detector 230 is configured to monitor, via monitor line of signal 231, a resonant voltage and a resonant current of the resonant network as described above in connection with the resonant phase detector 130. The resonant phase detector 230 produces in response supply a control signal 233 to the gate terminal 204 of the first switch S1 to selectively activate or interrupt the state switching of S1.

Another embodiment of the control mechanism of the output voltage control circuit comprises a self-oscillation feedback loop coupled between a drain, i.e. output terminal, and the gate terminal 204 of the switch S1. The first impedance characteristic of the resonant network is configured to enable oscillation of the self-oscillation feedback loop by design of a suitable loop gain. Hence, the gate signal of switch S1 will be active or enabled and switching at the oscillation frequency defined by the magnitude and phase characteristic of the loop of gain of the self-oscillation feedback loop. This oscillation frequency is the switching frequency of the class E power converter 200 during active or ON operation and will typically be situated close to an impedance maximum of the resonant network where the loop gain has the largest magnitude. The second impedance characteristic of the resonant network is conversely configured to disable or interrupt the oscillation of the self-oscillation feedback loop by changing the loop gain of the self-oscillation feedback loop in a suitable manner. When the oscillation of the self-oscillation feedback loop is interrupted, the gate control signal on the gate 204 of switch S1 is disabled or interrupted for example clamped to a constant voltage level below a threshold voltage of S1 if the latter is a MOSFET. As explained above the output voltage control circuit activates or interrupts/deactivates the class E converter 200 by controlling the state of the second switch S2 which switch state in turn enables or disables the self-oscillation of the feedback loop around switch S1. The latter determines the switching frequency of the class E power converter 200. Consequently, the on-state or conducting state of switch S2 where the converter load is connected enables normal or ON operation of the class E power converter 200. The class E power converter 200 is furthermore switched OFF or to a non-operational state by selecting the off-state of the second switch S2 where the converter load is disconnected via a suitable gate sig-

nal on the gate terminal 212 of S2. In this manner, the output voltage control circuit 260 provides on/off control of the class E power converter 200 to adjust the DC output voltage via state switching of switch S2 in a highly efficient and convenient manner. In particular, the on/off control is carried out by the changing the state of the switch S2, placed on a secondary or output side of the class E power converter 200, from a control signal derived from the secondary side circuit. Therefore, the adjustment of the DC output voltage is achieved without transmitting any control signal across the galvanic isolation barrier, formed by series capacitors C2 and C3 in the present embodiment, to the switch S1 on the input side circuit as explained in further detail below with reference to the self-oscillation based DC-DC power converter embodiments depicted on FIG. 4 and FIG. 5.

The frequency of the switch control signal on the gate 204 of switch S1 is preferably at or above 20 MHz or even above 30 MHz to provide the so-called VHF type of resonant DC-DC power converter 200. The switch control signal may comprise a PWM modulated control signal. The rectification circuit may comprise a diode based rectifier or a synchronous rectifier in front of the rectification capacitor to produce the converter output voltage $V_{out.}$as a DC output voltage. The class E power converter 200 may comprise a capacitor C1 connected or arranged across drain and source terminals of the switch S1 to increase a resonant current and/or adjust/fine-tune a resonance frequency of the class E converter 200. Likewise, a yet further capacitor C4 may be arranged across the rectifying diode D1 to adjust a duty cycle of the resonant power converter 200.

FIG. 3 is a simplified electrical circuit diagram of an isolated resonant class E type of DC-DC power converter 300 in accordance with a second embodiment of the invention. The main difference between the present class E converter 300 and the previous class E embodiment 200 lies in the integration of the functions of the separate rectifying diode D1 and the second controllable semiconductor switch S2 of the class E converter 200 in a single component S2 of the present class E power converter 300. The skilled person will appreciate that the above discussed features, functions and components of the first embodiment of the class E power converter 200 may apply to the present embodiment of the class E power converter 300 as well. Likewise, corresponding features and components of the first and second em-

bodiments of the class E power converters 200, 300 have been provided with corresponding reference numerals to ease comparison.

The skilled person will understand that the arrangement and control of the second controllable semiconductor switch S2 in the class E power converter 300 serve two different functions. The first function is similar to the functionality of the switch S2 of the class E converter 200 discussed above, i.e. to connect the converter load R_L to the output of the rectifier in the conducting state of switch S2 and disconnect the converter load R_L from the output of the rectifier in the non-conducting state of the switch S2. The loading on the output of the resonant network applied by the rectification circuit is altered between the conducting and non-conducting states of switch S2 as discussed above because the equivalent input impedance of the rectification circuit increases markedly when the converter load R_L is disconnected by switch S2. This change of loading on the output of the resonant network caused by the state switching of switch S2 changes the impedance characteristics of the resonant network such that it exhibits a second and different impedance characteristic in the non-conducting state of switch S2 (where the converter load is disconnected). This state switching is controlled by a voltage control loop comprising a comparator 308 and gate enable or drive circuit 305. An output of the gate drive circuit 305 is connected to a gate terminal 312 of the switch S2 and operable to determine the state of switch S2, i.e. conducting or non-conducting. A control circuit (not shown) is connected to the gate enable circuit 305 such that when switch S2 is in a conducting state during normal or ON operation of the class E power converter 300, the gate control signal on gate 312 is switched synchronously to the gate control signal of switch S1 on the input block 320. In this manner, the switch S2 operates as a synchronous half-wave rectifier and replaces the operation of rectifier diode D1 of the class E power converter 200. The rectification action of switch S2 generates the DC output voltage V_{out} of the converter across a rectification capacitor C5 coupled across the negative and positive output terminals, 310, 311 of the class E power converter 300. The class E power converter 300 may comprise a capacitor C1 as illustrated connected or arranged across drain and source terminals of the switch S1 to increase a resonant current and/or adjust/fine-tune a resonance frequency of the class E power converter 300. Likewise, a yet further capacitor C4 may be arranged across the integrated rectifying switch and converter load switch S2 to adjust a duty

cycle of the power converter 300. Also a self-oscillating gate drive may be used to drive the controllable switch S2 for synchronous rectification, in this way communication across the isolation barrier can be avoided.

FIG. 4 is a simplified electrical circuit diagram of a self-oscillating isolated class E DC-DC power converter 400 in accordance with a third embodiment of the invention. The main difference between the present class E power converter 400 and the previous class E converter 200 discussed in connection with FIG. 2 lies in the arrangement of a self-oscillation feedback loop coupled between an output or drain terminal of a first controllable semiconductor switch S1 and a control terminal 404 of switch S1. The self-oscillation feedback loop comprises a feedback capacitor C7 coupled between the drain and gate terminals of switch S1 and a series inductor L4 placed in-between the gate terminal 404 and a bias voltage source V_{bias}. The self-oscillation of the controllable semiconductor switch or transistor S1 is achieved by an appropriate phase shift induced by the combination of the feedback capacitor C7 and the gate inductor L4 in combination with an appropriate voltage gain provided by the first impedance characteristic of the resonant network. Hence, when the second controllable semiconductor switch S2 is placed in a conducting state, i.e. with the converter load R_L connected to the output of the converter, the self-oscillation of the switch or transistor S1 is enabled. When the transistor S1 is self-oscillating the power converter 400 is ON or operational to supply a DC output voltage and current to the converter load R_L. In the opposite state, i.e. off-state, of switch S2, the resonant network, comprising at least L1, L2, C1 and C2, exhibits a markedly different, impedance characteristic from the first impedance characteristic due to the disconnection of the converter load R_L from the output of the rectification circuit. The second impedance characteristic of the resonant network is configured to disable oscillation of the self-oscillation feedback loop around transistor switch S1. This may be achieved by designing the second impedance characteristic of the resonant network with a reduced Q factor and/or a changed resonance frequency compared to the first impedance characteristic. The Q factor at the resonance frequency of the first impedance characteristic may for example be larger than 5 or 10 while the Q factor at the resonance frequency of the second impedance characteristic may be smaller than 2 or 1. In addition, the resonance frequency of the first impedance characteristic may be arranged at a desired/target switching frequency of the DC-DC power

converter 400 for example at or above 20 MHz or at or above 30 MHz while the resonance frequency of the second impedance characteristic may example at least 1.4 times lower than the resonance frequency of the first impedance characteristic. The skilled person will understand that the functionality of the previously discussed resonant phase detectors 130, 230, 330 is integrated into the self-oscillation feedback loop formed around the transistor S1. In this manner, oscillation of the self-oscillation feedback loop is either enabled or disabled according to the switch state of the second controllable switch S2.

The skilled person will understand that the each of the illustrated capacitors C7, C8 and C1 in practice may represent intrinsic device capacitances only of the transistor switch S1 for example drain-gate, gate-source and drain-source capacitances of a MOSFET transistor embodiment of switch S1. In the alternative, one or more of these intrinsic device capacitances may be supplemented by a parallelly connected external capacitor to provide a desired capacitance. The skilled person will appreciate that the above discussed features, functions and components of the output voltage control loop, rectification circuit and galvanic isolation barrier of first embodiment of the class E power converter 200 may apply to the corresponding components and circuits of present embodiment of the power converter 400 as well. Hence, corresponding components of the first and third embodiments of the class E power converters 200, 400 have been provided with corresponding reference numerals to ease comparison.

FIG. 5 is a simplified electrical circuit diagram of a non-isolated resonant class E DC-DC power converter 500 in accordance with a fourth embodiment of the invention. The main difference between the present class E converter 500 and the previous class E converter 200, discussed in connection with FIG. 2, lies in the lack of a galvanic isolation barrier between the input block 520 and the output block 550 and the different coupling of the second controllable semiconductor switch S2. The converter output voltage V_{out} is regulated by alternatingly activating and interrupting the first switch control signal on the gate terminal 512 of semiconductor switch S2 to turn ON and disable the resonant power converter 500 as discussed in connection with the description of the previous resonant power converter embodiments. The regulation of the DC output voltage V_{out} of the power converter 500 is carried out by an output voltage control circuit 560 comprising a conditioning circuit 515 coupled to

the converter output voltage V_{out} and comparator 508. A reference input of the comparator 508 is coupled to a DC reference voltage V_{ref} while another comparator input receives the DC output voltage after conditioning. As explained above, the comparator output signal provides a control signal to the gate terminal of the second controllable switch S2 to alternatingly switch the latter between its conducting and non-conducting states depending on the level of the DC output voltage relative to the DC reference voltage V_{ref}. The present DC-DC power converter 500 comprises a self-oscillation feedback loop, schematically illustrated by circuit box 530, to turn off and turn on the power converter 500 depending on the selected state of switch S2. The self-oscillation feedback loop may be connected between an output or drain terminal of a first controllable semiconductor switch S1 and a control terminal 504 of switch S1 as discussed above in connection with the third embodiment.

While the semiconductor switch S2 of each of the previously discussed power converter embodiments 200, 300, 400 is coupled in series between the resonant network output and the converter load, the corresponding switch S2 of the present power converter 500 is coupled across an output of the resonant network and a negative supply rail or ground rail 511 of the power converter 500. The resonant network of the power converter 500 comprises at least L1, L2 and C1. Hence, the switch S2 functions as an open circuit when it is placed in non-conducting state or off- state by the appropriate comparator output signal on the gate terminal 512 of S2. Hence, the switch S2 presents substantially no loading of the output of the resonant network in its non-conducting state so as to select a first impedance characteristic of the resonant network. In the conducting state of switch S2 it effectively short circuits the output of the resonant network to ground or the negative supply voltage line 511 via a low impedance path since the on-resistance of switch S2 may be significantly smaller than an impedance of the resonant network. Hence, the resonant network exhibits a second and preferably markedly different impedance characteristic in the conducting state of switch S2. In a similar manner as discussed above in connection with the self-oscillation network of the third embodiment 400, the second impedance characteristic of the resonant network is configured to disable oscillation of the self-oscillation feedback loop around transistor switch S1. This may be achieved by configuring the resonant network with a second impedance characteristic which exhibits a reduced Q factor and/or a changed resonance frequency com-

pared to the same features of the first impedance characteristic. The Q factor at the resonance frequency of the first impedance characteristic may for example be larger than 5 or 10 while the Q factor at the resonance frequency of the second impedance characteristic may be smaller than 2 or 1. In addition, the resonance frequency of the first impedance characteristic may lie at or above 20 MHz such as at or above 30 MHz while the resonance frequency of the second impedance characteristic may be lower for example at least 1.4 times lower.

CLAIMS

1. A resonant DC-DC power converter comprising:
an input side circuit comprising a positive and a negative input terminal for receipt of an input voltage or current,
an output side circuit comprising positive and negative output terminals for supply of a converter output power, voltage or current and connection to a converter load,
a rectification circuit connected between an output of a resonant network and the output side circuit,
wherein the resonant network is configured for alternatingly being charged from the input voltage or current and discharged through the rectification circuit by a first controllable switch arrangement in accordance with a first switch control signal, wherein a frequency of the switch control signal is at or above 20 MHz, more preferably at or above 30 MHz,
a second controllable switch arrangement configured to select a first impedance characteristic of the resonant network in a first switch state and select a second impedance characteristic of the resonant network in a second switch state,
an output voltage or current control circuit configured to adjust the converter output voltage and/or current by activating and interrupting the first switch control signal in accordance with a switch state of the second controllable switch arrangement.

2. A resonant DC-DC power converter according to claim 1, wherein the second controllable switch arrangement is coupled in series between an output of the rectification circuit and the positive or the negative output terminal to connect the converter load in a conducting switch state and disconnect the converter load in a non-conducting switch state.

3. A resonant DC-DC power converter according to claim 1, wherein the second controllable switch arrangement is coupled across the output of the resonant network to select the first impedance characteristic of the resonant network in a non-conducing state and the second impedance characteristic of the resonant network in in a conducing state.

4. A resonant DC-DC power converter according to claim 2 or 3, wherein the rectifi-

cation circuit comprises the second controllable switch arrangement; and
a control circuit configured for generating a control signal for the second controllable switch arrangement synchronously to the first switch control signal.

5. A resonant DC-DC power converter according to any of claims 1-4, wherein the output voltage or current control circuit comprises:
a self-oscillation feedback loop coupled between an output terminal and a control terminal of the first controllable switch arrangement; wherein the first impedance characteristic of the resonant network is configured to enable oscillation of the self-oscillation feedback loop; and
the second impedance characteristic of the resonant network is configured to disable oscillation of the self-oscillation feedback loop

6. A resonant DC-DC power converter according to any of the preceding claims, wherein a Q factor of the first impedance characteristic is larger than 5 at a resonance frequency of the first impedance characteristic; and
a Q factor of the second impedance characteristic is smaller than 2 at a resonance frequency of the second impedance characteristic

7. A resonant DC-DC power converter according to any of the preceding claims, wherein a resonance frequency of the first impedance characteristic is at least 1.4 times larger than a resonance frequency of the second impedance characteristic.

8. A resonant DC-DC power converter according to any of the preceding claims, wherein the output voltage or current control circuit comprises:
a voltage or current regulation loop connected between the converter output voltage and a control terminal of the second controllable switch arrangement to adjust the converter output voltage in accordance with one or more DC reference voltage(s) or current(s).

9. A resonant DC-DC power converter according to claim 8, wherein the voltage or current regulation loop comprises:
a DC reference voltage generator configured to supply the one or more DC reference voltage(s) or current(s),

one or more comparator(s) configured for comparing the converter output voltage to at least a first DC reference voltage and select the conducting state or the non-conducting state of the second controllable switch arrangement depending on a result of the comparison.

10. A resonant DC-DC power converter according to claim 9, wherein the DC reference voltage generator is configured to supply at first DC reference voltage and a second DC reference voltage where the first DC reference voltage is higher than the second DC reference voltage;
wherein the one or more comparator(s) is configured to:
comparing the converter output voltage to the first and second DC reference voltages; and
selecting one of the conducting and non-conducting states of the second controllable switch arrangement in response to the converter output voltage exceeding the first DC reference voltage,
selecting the opposite state of the second controllable switch arrangement in response to the converter output voltage falls below the second DC reference voltage.

11. A resonant DC-DC power converter according to any of claims 5-10, wherein the self-oscillation feedback loop comprises:
a first intrinsic switch capacitance coupled between the output and control terminals of the first controllable switch arrangement,
a first bias voltage source configured to generate a first adjustable bias voltage,
a first inductor, preferably with substantially fixed inductance, coupled in-between the first bias voltage source and the control terminal of the first controllable switch arrangement.

12. A resonant DC-DC power converter according to any of the preceding claims, comprising a galvanic isolation barrier arranged between the input side circuit and the output side circuit.

13. A resonant DC-DC power converter according to claim 12, wherein the galvanic isolation barrier comprises first and second coupling capacitors.

13. A resonant DC-DC power converter according to any of the preceding claims, comprising a converter topology selected from a group of {class E, class F, class DE}.

14. A resonant DC-DC power converter according to any of the preceding claims, wherein the first controllable switch arrangement comprises one or more semiconductor switches and the second controllable switch arrangement comprises one or more semiconductor switches;
wherein each of the semiconductor switches comprises a semiconductor transistor such as a MOSFET or IGBT such as a Gallium Nitride (GaN) or Silicon Carbide (SiC) MOSFET.

15. A resonant DC-DC power converter according to any of the preceding claims, further comprising:
a wireless or wired data receiver for receipt of remote data commands to control the switch state of the second controllable switch arrangement.

16. A resonant DC-DC power converter according to any of the preceding claims, further comprising:
a single substantially flat carrier substrate comprising a first surface and a second, opposing, surface,
wherein the input side circuit, the output side circuit, the rectification circuit, the resonant network, the first controllable switch arrangement, the second controllable switch arrangement and the output voltage or current control circuit are attached on the first surface and/or the second surface.

17. A resonant DC-DC power converter according to claim 16, wherein the single substantially flat carrier substrate comprises a single sided or double-sided printed circuit board.

18. A method of operating a resonant DC-DC power converter to generate a converter output voltage or current, said method comprising steps of:
a) alternatingly charging and discharging a resonant network of the resonant converter from an input voltage source by a first controllable switch arrangement in

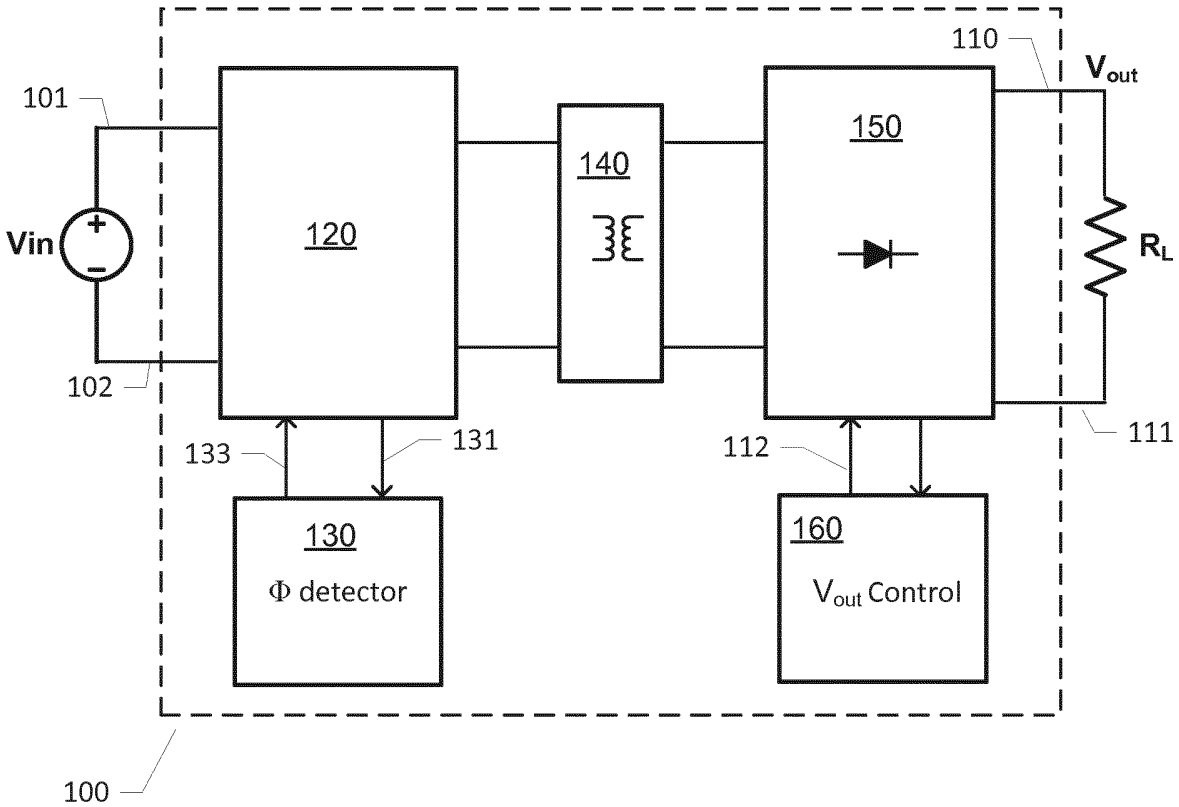
accordance with a first switch control signal,

b) rectifying a resonant current of the resonant network,

c) discharging a rectified resonant current to a rectification circuit to produce a rectified output voltage,

d) switching between a first impedance characteristic or a second impedance characteristic of the resonant network by selecting a first or a second switch state of a second controllable switch arrangement,

e) adjusting a converter output voltage or current by alternatingly activating and interrupting the first switch control signal in accordance with first and second switch states of the second controllable switch arrangement.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Φ detector
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Vout Control
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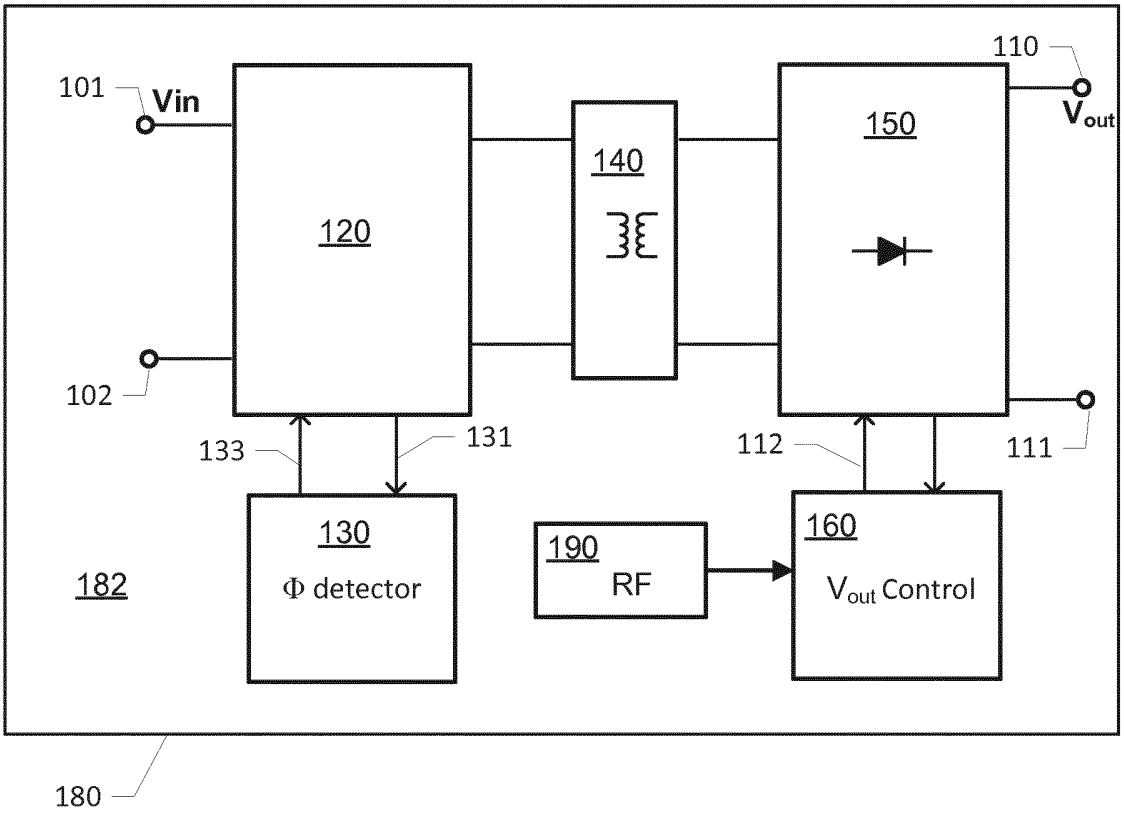
FIG. 1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Φ detector
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RF
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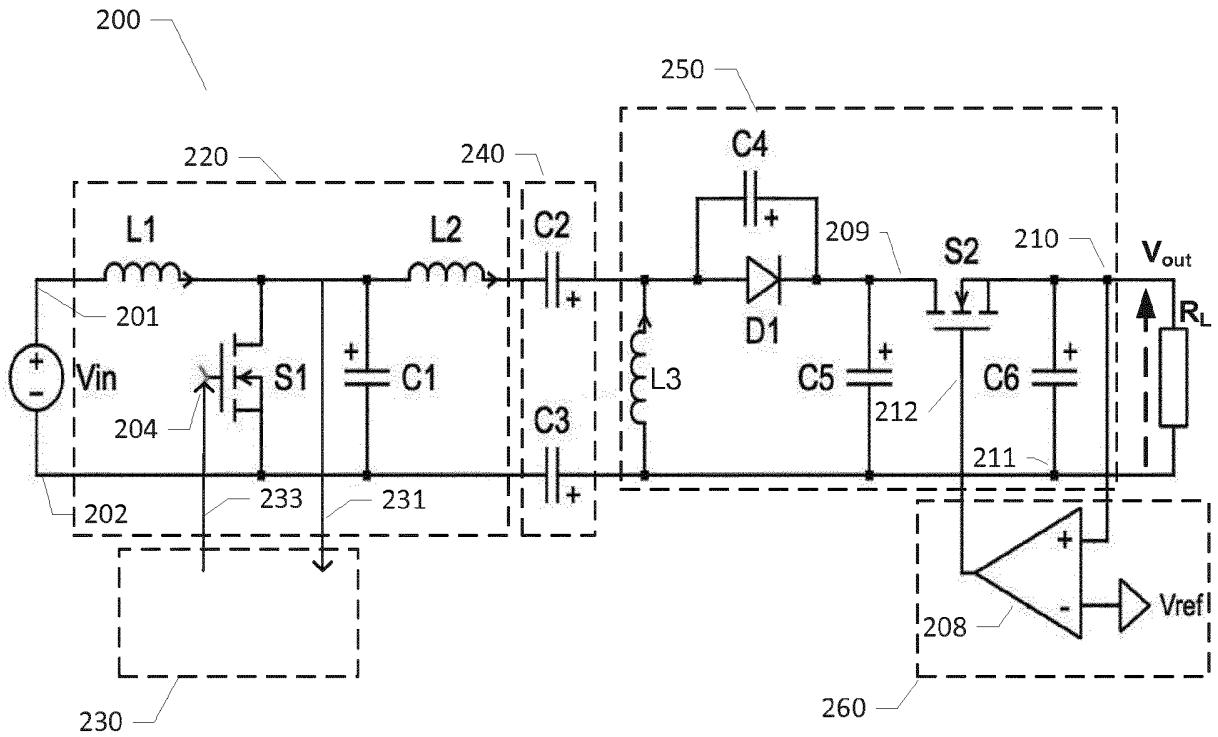
Vout Control
180

FIG. 1A)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L2
C2
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S2
210
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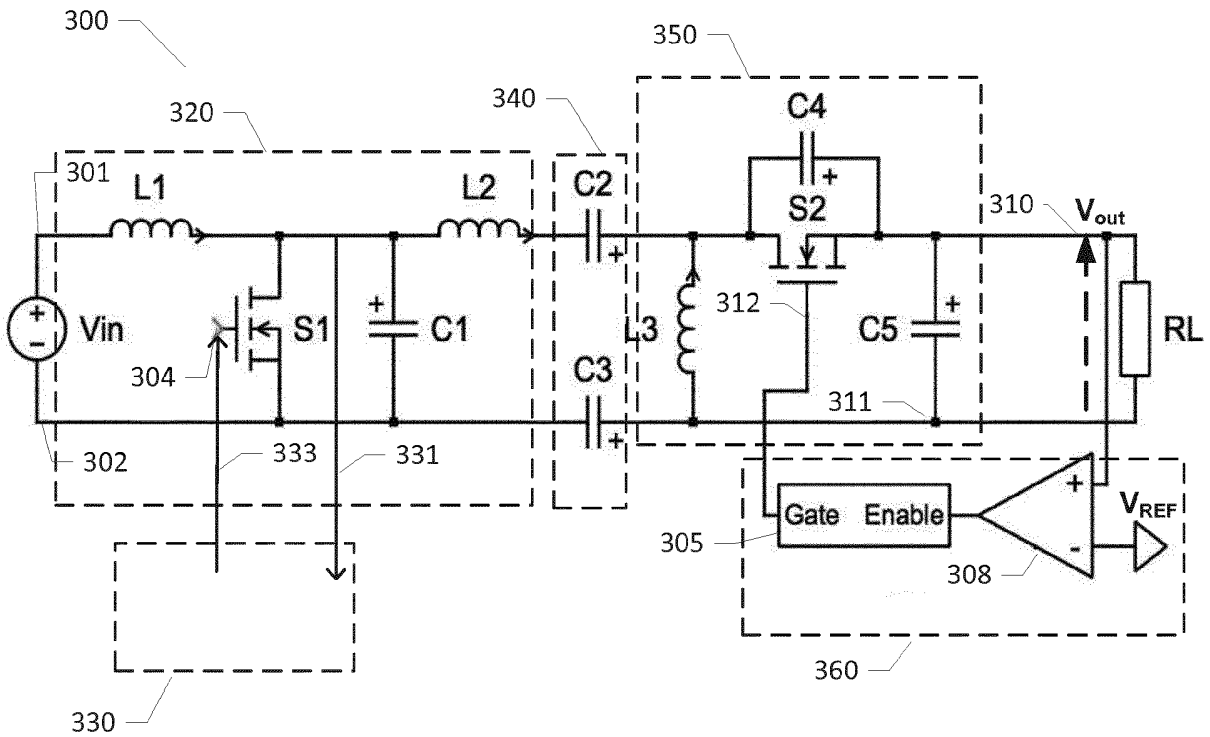
201
D1
R_L
Vin
S1
C1
L3
C5
C6
204
C3
212
211
202
233
231
Vref
208
230
260

FIG. 2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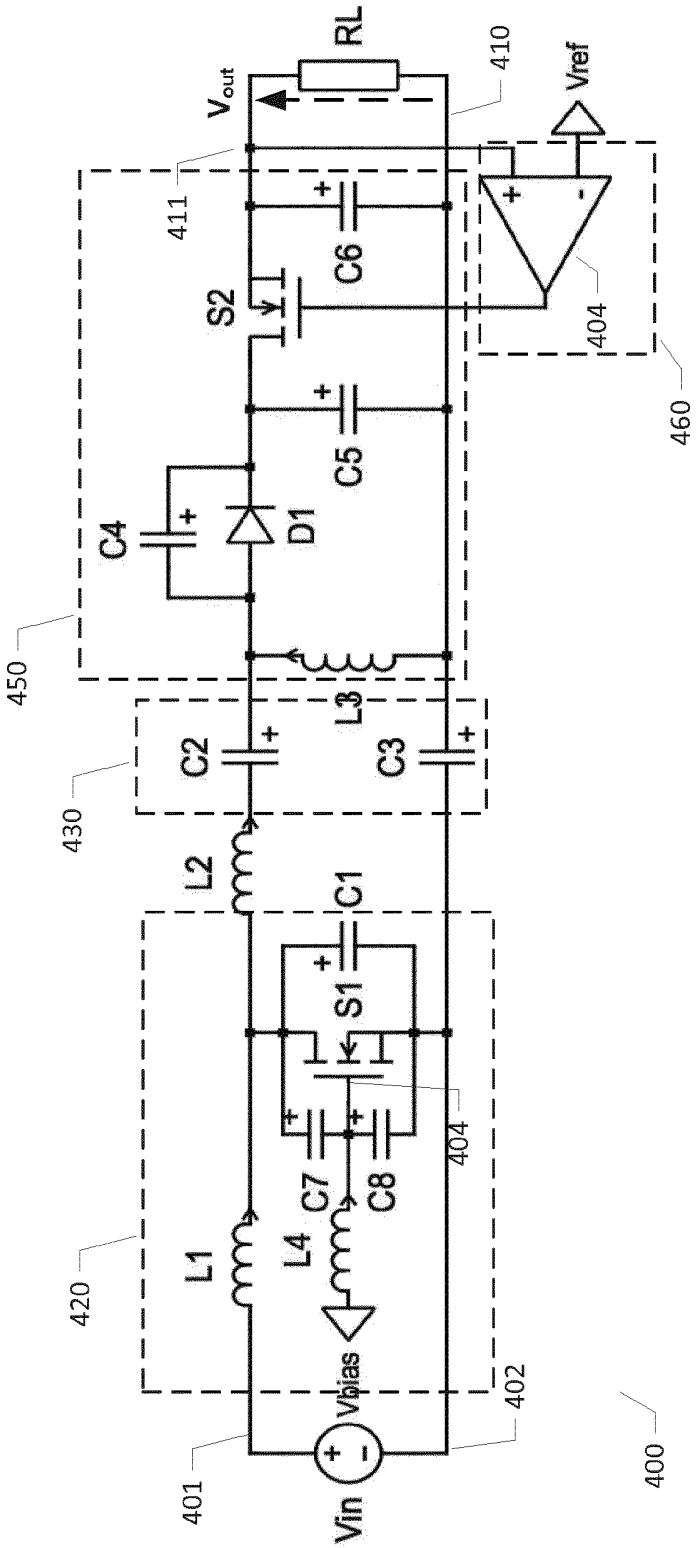
L1
L2
C2
C4
S2
310
V_{out}
Vin
S1
C1
L3
312
C5
RL
304
C3
311
302
333
331
Gate
Enable
V_{REF}
305
308
360
330

FIG. 3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S2
404
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C5
C4
D1
450
L3
C2
C3
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404
C7
C8
L1
L4
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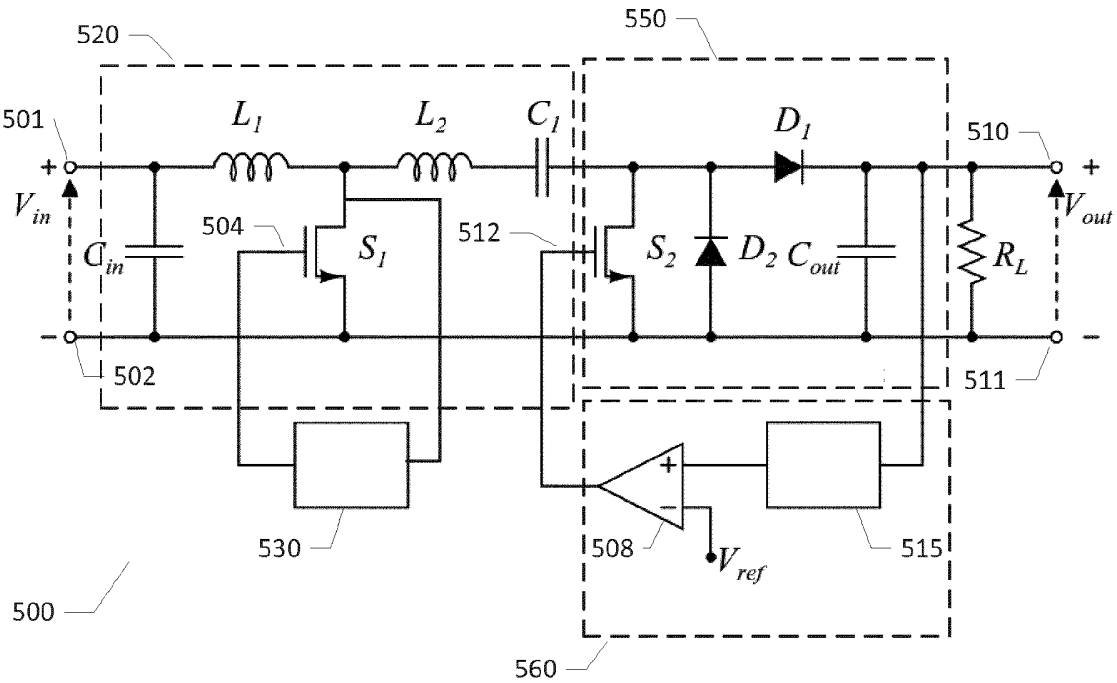
Vbias
402
401
Vin
400

FIG. 4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550
501
L_1
L_2
C_1
D_1
510
V_{in}
C_{in}
504
S_1
512
S_2
D_2 C_{out}
R_L
V_{out}
502
511
530
508
V_{ref}
515
500
560

FIG. 5

A.22 M. Madsen et. al.: *"Confidential"*, DTU ref 95513

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